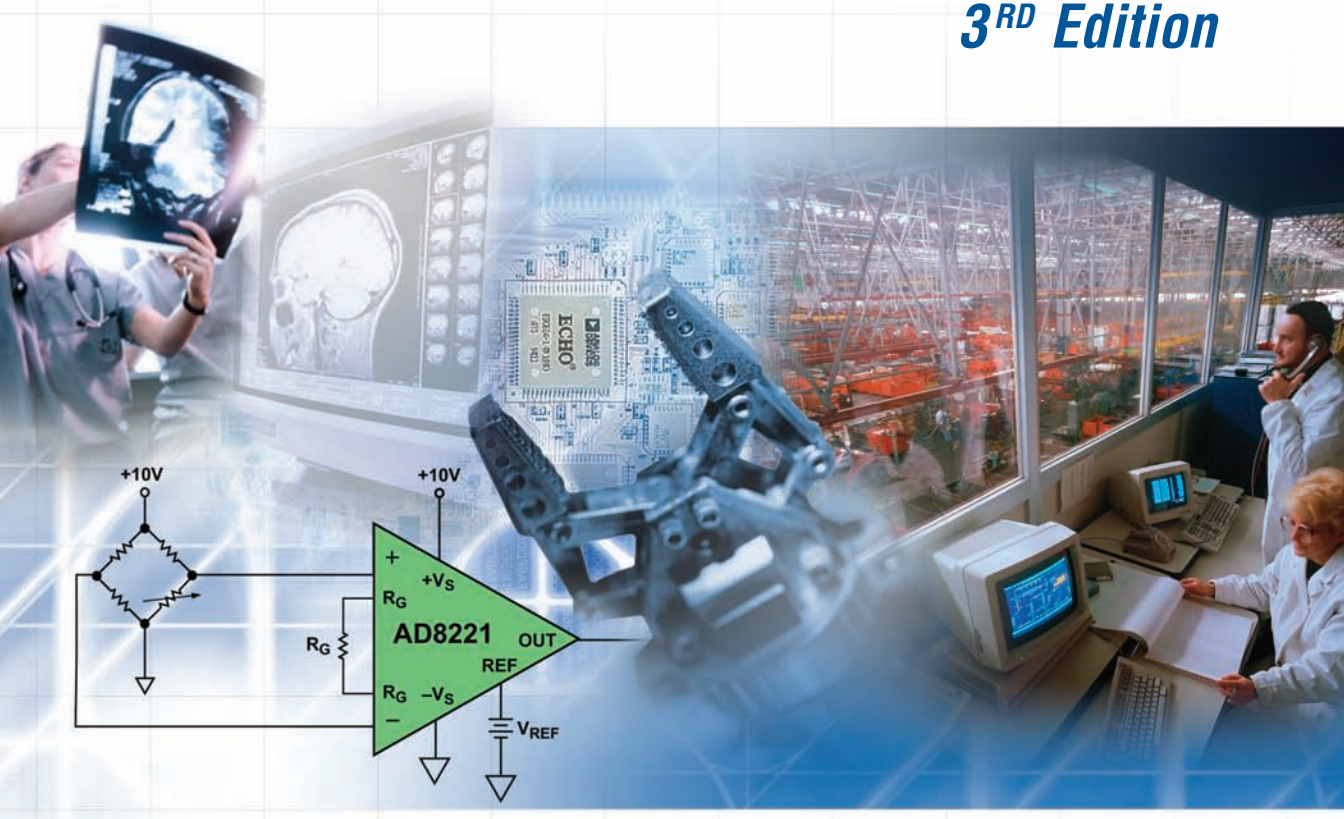
# A Designer's Guide to Instrumentation Amplifiers

## 3RD Edition

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# A DESIGNER'S GUIDE TO INSTRUMENTATION AMPLIFIERS

## 3RD Edition

*by*

*Charles Kitchin and Lew Counts*

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# Chapter I

# IN-AMP BASICS

## INTRODUCTION

Instrumentation amplifiers (in-amps) are sometimes misunderstood. Not all amplifiers used in instrumentation applications are instrumentation amplifiers, and by no means are all in-amps used only in instrumentation applications. In-amps are used in many applications, from motor control to data acquisition to automotive. The intent of this guide is to explain the fundamentals of what an instrumentation amplifier is, how it operates, and how and where to use it. In addition, several different categories of instrumentation amplifiers are addressed in this guide.

## IN-AMPS vs. OP AMPS: WHAT ARE THE DIFFERENCES?

An instrumentation amplifier is a closed-loop gain block that has a differential input and an output that is single-ended with respect to a reference terminal. Most commonly, the impedances of the two input terminals are balanced and have high values, typically $10^9$ Ω, or greater. The input bias currents should also be low, typically 1 nA to 50 nA. As with op amps, output impedance is very low, nominally only a few milliohms, at low frequencies.

Unlike an op amp, for which closed-loop gain is determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network that is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user set (via pins) by an internal or external gain resistor, which is also isolated from the signal inputs.

Figure 1-1 shows a bridge preamp circuit, a typical in-amp application. When sensing a signal, the bridge resistor values change, unbalancing the bridge and causing a change in differential voltage across the bridge. The signal output of the bridge is this differential voltage, which connects directly to the in-amp's inputs. In addition, a constant dc voltage is also present on both lines. This dc voltage will normally be equal or *common mode* on both input lines. In its primary function, the in-amp will normally reject the common-mode dc voltage, or any other voltage common to both lines, while amplifying the *differential* signal voltage, the difference in voltage between the two lines.

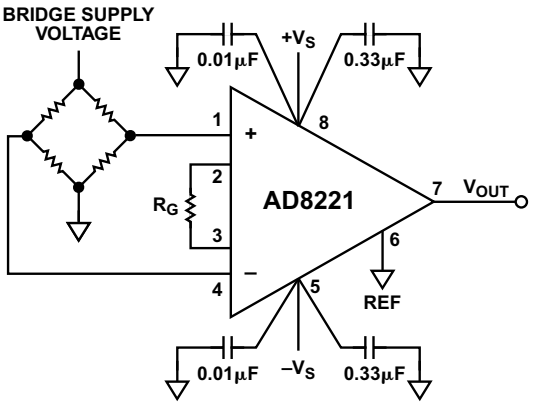



*Figure 1-1. AD8221 bridge circuit.*

In contrast, if a standard op amp amplifier circuit were used in this application, it would simply amplify *both* the signal voltage and any dc, noise, or other common-mode voltages. As a result, the signal would remain buried under the dc offset and noise. Because of this, even the best op amps are far less effective in extracting weak signals. Figure 1-2 contrasts the differences between op amp and in-amp input characteristics.

### Signal Amplification and Common-Mode Rejection

An instrumentation amplifier is a device that amplifies the *difference* between two input signal voltages while rejecting any signals that are common to both inputs. The in-amp, therefore, provides the very important function of extracting small signals from transducers and other signal sources.

Common-mode rejection (CMR), the property of canceling out any signals that are common (the same potential on both inputs), while amplifying any signals that are differential (a potential difference between the inputs), is the most important function an instrumentation amplifier provides. Both dc and ac common-mode rejection are important in-amp specifications. Any errors due to dc common-mode voltage (i.e., dc voltage present at both inputs) will be reduced 80 dB to 120 dB by any modern in-amp of decent quality.

However, inadequate ac CMR causes a large, time-varying error that often changes greatly with frequency and, therefore, is difficult to remove at the IA's output. Fortunately, most modern monolithic IC in-amps provide excellent ac and dc common-mode rejection.

Common-mode gain ($A_{CM}$), the ratio of change in output voltage to change in common-mode input voltage, is related to common-mode rejection. It is the net gain (or attenuation) from input to output for voltages common to both inputs. For example, an in-amp with a common-mode gain of 1/1000 and a 10 V common-mode voltage at its inputs will exhibit a 10 mV output change. The differential or normal mode gain ($A_D$) is the gain between input and output for voltages applied differentially (or across) the two inputs. The common-mode rejection ratio (CMRR) is simply the ratio of the differential gain, $A_D$, to the common-mode gain. Note that in an ideal in-amp, CMRR will increase in proportion to gain.

Common-mode rejection is usually specified for full range common-mode voltage (CMV) change at a given frequency and a specified imbalance of source impedance (e.g., 1 kΩ source imbalance, at 60 Hz).

Mathematically, common-mode rejection can be represented as

$$CMRR = A_D\left(\frac{V_{CM}}{V_{OUT}}\right)$$

where:

$A_D$ is the differential gain of the amplifier;

$V_{CM}$ is the common-mode voltage present at the amplifier inputs;

$V_{OUT}$ is the output voltage present when a common-mode input signal is applied to the amplifier.

The term CMR is a logarithmic expression of the common-mode rejection ratio (CMRR). That is, $CMR = 20 \log_{10} CMRR$.

To be effective, an in-amp needs to be able to amplify microvolt-level signals while rejecting common-mode voltage at its inputs. It is particularly important for the in-amp to be able to reject common-mode signals over the bandwidth of interest. This requires that instrumentation amplifiers have very high common-mode rejection over the main frequency of interest and its harmonics.

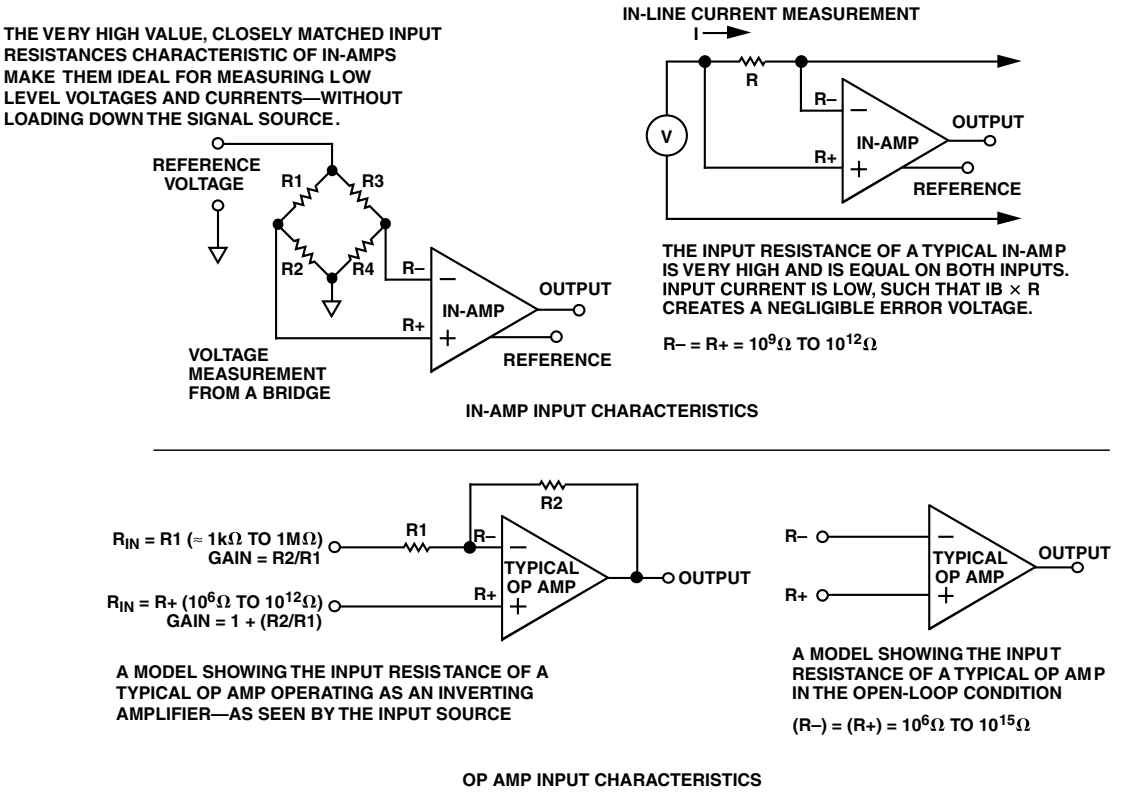



*Figure 1-2. Op amp vs. in-amp input characteristics.*

For techniques on reducing errors due to out-of-band signals that may appear as a dc output offset, please refer to the RFI section of this guide.

At unity gain, typical dc values of CMR are 70 dB to more than 100 dB, with CMR usually improving at higher gains. While it is true that operational amplifiers connected as subtractors also provide common-mode rejection, the user must provide closely matched external resistors (to provide adequate CMRR). On the other hand, monolithic in-amps, with their pretrimmed resistor networks, are far easier to apply.

**Common-Mode Rejection: Op Amp vs. In-Amp**

Op amps, in-amps, and difference amps all provide common-mode rejection. However, in-amps and diff amps are designed to reject common-mode signals so that they do not appear at the amplifier's output. In contrast, an op amp operated in the typical inverting or noninverting amplifier configuration will process common-mode signals, passing them through to the output, but will not normally reject them.

Figure 1-3a shows an op amp connected to an input source that is riding on a common-mode voltage. Because of feedback applied externally between the output and the summing junction, the voltage on the "–" input is forced to be the same as that on the "+" input voltage. Therefore, the op amp ideally will have zero volts *across* its input terminals. As a result, the voltage at the op amp output *must* equal $V_{CM}$, for zero volts differential input.

Even though the op amp has *common-mode rejection*, the common-mode voltage is transferred to the output along with the signal. In practice, the signal is amplified by the op amp's closed-loop gain, while the common-mode voltage receives only unity gain. This difference in gain does provide some reduction in common-mode voltage as a percentage of signal voltage. However, the common-mode voltage still appears at the output, and its presence reduces the amplifier's available output swing. For many reasons, any common-mode signal (dc or ac) appearing at the op amp's output is highly undesirable.

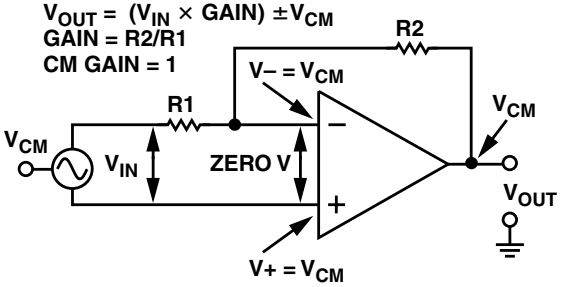



*Figure 1-3a. In a typical inverting or noninverting amplifier circuit using an op amp, both the signal voltage and the common-mode voltage appear at the amplifier output.*

Figure 1-3b shows a 3-op amp in-amp operating under the same conditions. Note that, just like the op amp circuit, the input buffer amplifiers of the in-amp pass the common-mode signal through at unity gain. In contrast, the signal is amplified by both buffers. The output signals from the two buffers connect to the subtractor section of the IA. Here the differential signal is amplified (typically at low gain or unity) while the common-mode voltage is attenuated (typically by 10,000:1 or more). Contrasting the two circuits, both provide signal amplification (and buffering), but because of its subtractor section, the in-amp rejects the common-mode voltage.

Figure 1-3c is an in-amp bridge circuit. The in-amp effectively rejects the dc common-mode voltage appearing at the two bridge outputs while amplifying the very weak bridge signal voltage. In addition, many modern in-amps provide a common-mode rejection approaching 80 dB, which allows powering of the bridge from an inexpensive, nonregulated dc power supply. In contrast, a self constructed in-amp, using op amps and 0.1% resistors, typically only achieves 48 dB CMR, thus requiring a regulated dc supply for bridge power.

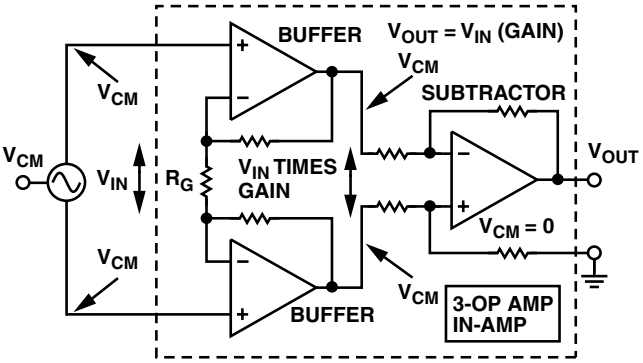



*Figure 1-3b. As with the op amp circuit above, the input buffers of an in-amp circuit amplify the signal voltage while the common-mode voltage receives unity gain. However, the common-mode voltage is then rejected by the in-amp's subtractor section.*

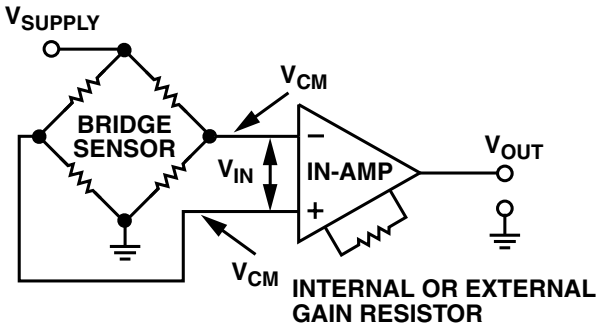



*Figure 1-3c. An in-amp used in a bridge circuit. Here the dc common-mode voltage can easily be a large percentage of the supply voltage.*

Figure 1-3d shows a difference (subtractor) amplifier being used to monitor the voltage of an individual cell that is part of a battery bank. Here the common-mode dc voltage can easily be much higher than the amplifier's supply voltage. Some monolithic difference amplifiers, such as the **AD629**, can operate with common-mode voltages as high as ±270 V.

## DIFFERENCE AMPLIFIERS

Figure 1-4 is a block diagram of a difference amplifier. This type of IC is a special-purpose in-amp that normally consists of a subtractor amplifier followed by an output buffer, which may also be a gain stage. The four resistors used in the subtractor are normally internal to the IC, and, therefore, are closely matched for high CMR.

Many difference amplifiers are designed to be used in applications where the common-mode and signal voltages may easily exceed the supply voltage. These diff amps typically use very high value input resistors to attenuate both signal and common-mode input voltages.

## WHERE ARE IN-AMPS AND DIFFERENCE AMPS USED?

### Data Acquisition

In-amps find their primary use amplifying signals from low level output transducers in noisy environments. The amplification of pressure or temperature transducer signals is a common in-amp application. Common bridge applications include strain and weight measurement using load cells and temperature measurement using resistive temperature detectors, or RTDs.

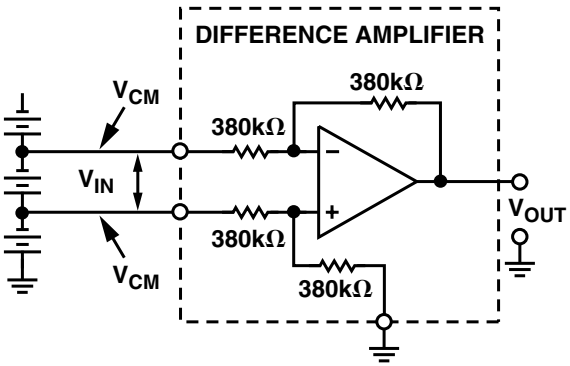



*Figure 1-3d. A difference amp is especially useful in applications such as battery cell measurement, where the dc (or ac) common-mode voltage may be greater than the supply voltage.*

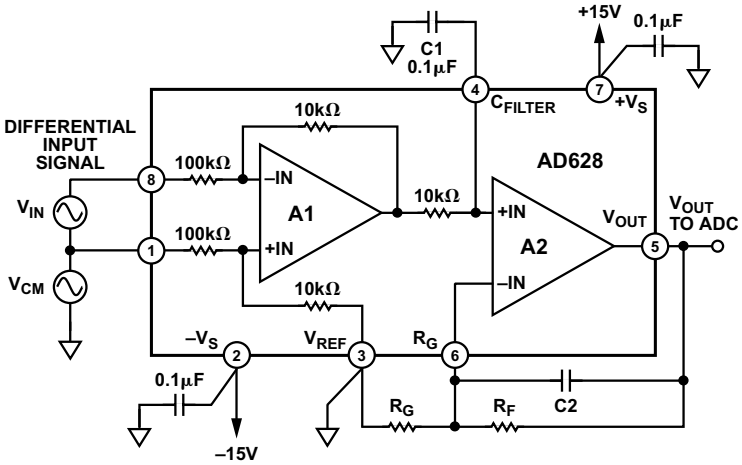



*Figure 1-4. A difference amplifier IC.*

**Medical Instrumentation**
In-amps are widely used in medical equipment such as EKG and EEG monitors, blood pressure monitors, and defibrillators.

**Monitor and Control Electronics**
Diff amps may be used to monitor voltage or current in a system and then trigger alarm systems when nominal operating levels are exceeded. Because of their ability to reject high common-mode voltages, diff amps are often used in these applications.

**Software-Programmable Applications**
An in-amp may be used with a software-programmable resistor chip to allow software control of hardware systems.

**Audio Applications**
Because of their high common-mode rejection, instrumentation amplifiers are sometimes used for audio applications (as microphone preamps, for example), to extract a weak signal from a noisy environment, and to minimize offsets and noise due to ground loops. Refer to Table 6-4 (page 6-26), Specialty Products Available from Analog Devices.

**High Speed Signal Conditioning**
Because the speed and accuracy of modern video data acquisition systems have improved, there is now a growing need for high bandwidth instrumentation amplifiers, particularly in the field of CCD imaging equipment where offset correction and input buffering are required. Double-correlated sampling techniques are often used in this area for offset correction of the CCD image. Two sample-and-hold amplifiers monitor the pixel and reference levels, and a dc-corrected output is provided by feeding their signals into an instrumentation amplifier.

**Video Applications**
High speed in-amps may be used in many video and cable RF systems to amplify or process high frequency signals.

**Power Control Applications**
In-amps can also be used for motor monitoring (to monitor and control motor speed, torque, etc.) by measuring the voltages, currents, and phase relationships of a 3-phase ac-phase motor. Diff amps are used in applications where the input signal exceeds the supply voltages.

## IN-AMPS: AN EXTERNAL VIEW

Figure 1-5 provides a functional block diagram of an instrumentation amplifier.

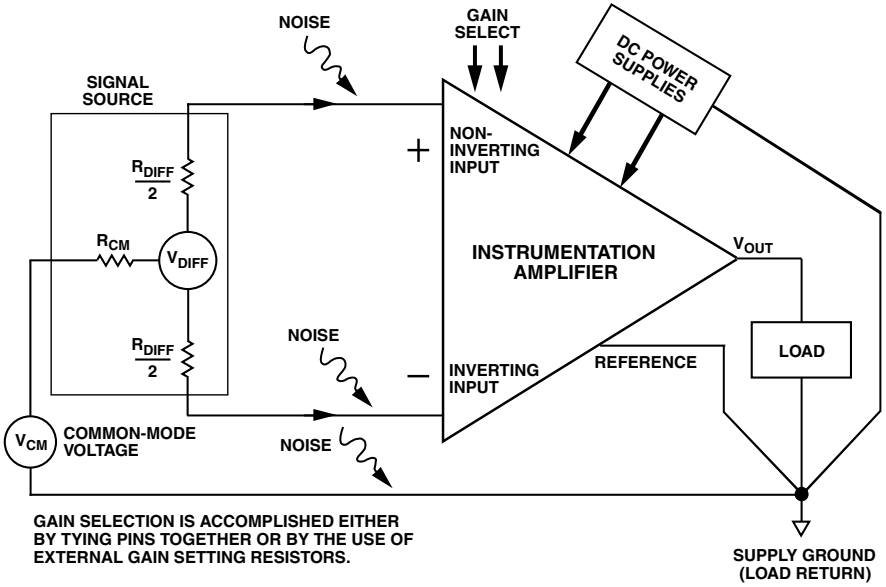



*Figure 1-5. Differential vs. common-mode input signals.*

Since an ideal instrumentation amplifier detects only the difference in voltage between its inputs, any common-mode signals (equal potentials for both inputs), such as noise or voltage drops in ground lines, are rejected at the input stage without being amplified.

Either internal or external resistors may be used to set the gain. Internal resistors are the most accurate and provide the lowest gain drift over temperature.

One common approach is to use a single external resistor, working with two internal resistors, to set the gain. The user can calculate the required value of resistance for a given gain, using the gain equation listed in the in-amp's spec sheet. This permits gain to be set anywhere within a very large range. However, the external resistor can seldom be exactly the correct value for the desired gain, and it will always be at a slightly different temperature than the IC's internal resistors. These practical limitations always contribute additional gain error and gain drift.

Sometimes two external resistors are employed. In general, a 2-resistor solution will have lower drift than a single resistor as the ratio of the two resistors sets the gain, and these resistors can be within a single IC array for close matching and very similar temperature coefficients (TC). Conversely, a single external resistor will always be a TC mismatch for an on-chip resistor.

The output of an instrumentation amplifier often has its own reference terminal, which, among other uses, allows the in-amp to drive a load that may be at a distant location.

Figure 1-5 shows the input and output commons being returned to the same potential, in this case to power supply ground. This star ground connection is a very effective means of minimizing ground loops in the circuit; however, some residual common-mode ground currents will still remain. These currents flowing through $R_{CM}$ will develop a common-mode voltage error, $V_{CM}$. The in-amp, by virtue of its high common-mode rejection, will amplify the differential signal while rejecting $V_{CM}$ and any common-mode noise.

Of course, power must be supplied to the in-amp. As with op amps, the power would normally be provided by a dual-supply voltage that operates the in-amp over a specified range. Alternatively, an in-amp specified for single-supply (rail-to-rail) operation may be used.

An instrumentation amplifier may be assembled using one or more operational amplifiers, or it may be of monolithic construction. Both technologies have their advantages and limitations.

In general, discrete (op amp) in-amps offer design flexibility at low cost and can sometimes provide performance unattainable with monolithic designs, such as very high bandwidth. In contrast, monolithic designs provide complete in-amp functionality and are fully specified and usually factory trimmed, often to higher dc precision than discrete designs. Monolithic in-amps are also much smaller, lower in cost, and easier to apply.

## WHAT OTHER PROPERTIES DEFINE A HIGH QUALITY IN-AMP?

Possessing a high common-mode rejection ratio, an instrumentation amplifier requires the properties described below.

### High AC (and DC) Common-Mode Rejection

At a minimum, an in-amp's CMR should be high over the range of input frequencies that need to be rejected. This includes high CMR at power line frequencies and at the second harmonic of the power line frequency.

### Low Offset Voltage and Offset Voltage Drift

As with an operational amplifier, an in-amp must have low offset voltage. Since an instrumentation amplifier consists of two independent sections, an input stage and an output amplifier, total output offset will equal the sum of the gain times the input offset plus the offset of the output amplifier (within the in-amp). Typical values for input and output offset drift are 1 μV/°C and 10 μV/°C, respectively. Although the initial offset voltage may be nulled with external trimming, offset voltage drift cannot be adjusted out. As with initial offset, offset drift has two components, with the input and output section of the in-amp each contributing its portion of error to the total. As gain is increased, the offset drift of the input stage becomes the dominant source of offset error.

**A Matched, High Input Impedance**
The impedances of the inverting and noninverting input terminals of an in-amp must be high and closely matched to one another. High input impedance is necessary to avoid loading down the input signal source, which could also lower the input signal voltage.

Values of input impedance from $10^9$ Ω to $10^{12}$ Ω are typical. Difference amplifiers, such as the AD629, have lower input impedances, but can be very effective in high common-mode voltage applications.

**Low Input Bias and Offset Current Errors**
Again, as with an op amp, an instrumentation amplifier has bias currents that flow into, or out of, its input terminals; bipolar in-amps have base currents and FET amplifiers have gate leakage currents. This bias current flowing through an imbalance in the signal source resistance will create an offset error. Note that if the input source resistance becomes infinite, as with ac (capacitive) input coupling, without a resistive return to power supply ground, the input common-mode voltage will climb until the amplifier saturates. A high value resistor connected between each input and ground is normally used to prevent this problem. Typically, the input bias current multiplied by the resistor's value in ohms should be less than 10 mV (see Chapter V). Input offset current errors are defined as the mismatch between the bias currents flowing into the two inputs. Typical values of input bias current for a bipolar in-amp range from 1 nA to 50 nA; for a FET input device, values of 1 pA to 50 pA are typical at room temperature.

**Low Noise**
Because it must be able to handle very low level input voltages, an in-amp must not add its own noise to that of the signal. A minimum input noise level of 10 nV/$\sqrt{\text{Hz}}$ @ 1 kHz (gain > 100) referred to input (RTI) is desirable. Micropower in-amps are optimized for the lowest possible input stage current and, therefore, typically have higher noise levels than their higher current cousins.

**Low Nonlinearity**
Input offset and scale factor errors can be corrected by external trimming, but nonlinearity is an inherent performance limitation of the device and cannot be removed by external adjustment. Low nonlinearity must be designed in by the manufacturer. Nonlinearity is normally specified as a percentage of full scale, whereas the manufacturer measures the in-amp's error at the plus and minus full-scale voltage and at zero. A nonlinearity error of 0.01% is typical for a high quality in-amp; some devices have levels as low as 0.0001%.

**Simple Gain Selection**
Gain selection should be easy. The use of a single external gain resistor is common, but an external resistor will affect the circuit's accuracy and gain drift with temperature. In-amps, such as the **AD621**, provide a choice of internally preset gains that are pin-selectable, with very low gain TC.

**Adequate Bandwidth**
An instrumentation amplifier must provide bandwidth sufficient for the particular application. Since typical unity-gain, small-signal bandwidths fall between 500 kHz and 4 MHz, performance at low gains is easily achieved, but at higher gains bandwidth becomes much more of an issue. Micropower in-amps typically have lower bandwidth than comparable standard in-amps, as micropower input stages are operated at much lower current levels.

**Differential to Single-Ended Conversion**

Differential to single-ended conversion is, of course, an integral part of an in-amp's function: A differential input voltage is amplified and a buffered, single-ended output voltage is provided. There are many in-amp applications that require amplifying a differential voltage that is *riding* on top of a much larger common-mode voltage. This common-mode voltage may be noise, or ADC offset, or both. The use of an op amp rather than an in-amp would simply amplify *both* the common mode and the signal by equal amounts. The great benefit provided by an in-amp is that it selectively amplifies the (differential) signal while rejecting the common-mode signal.

**Rail-to-Rail Input and Output Swing**

Modern in-amps often need to operate on single-supply voltages of 5 V or less. In many of these applications, a rail-to-rail input ADC is often used. So-called rail-to-rail operation means that an amplifier's maximum input or output swing is essentially equal to the power supply voltage. In fact, the input swing can sometimes exceed the supply voltage slightly, while the output swing is often within 100 mV of the supply voltage or ground. Careful attention to the data sheet specifications is advised.

**Power vs. Bandwidth, Slew Rate, and Noise**

As a general rule, the higher the operating current of the in-amp's input section, the greater the bandwidth and slew rate and the lower the noise. But higher operating current means higher power dissipation and heat. Battery-operated equipment needs to use low power devices, and densely packed printed circuit boards must be able to dissipate the collective heat of all their active components. Device heating also increases offset drift and other temperature-related errors. IC designers often must trade off some specifications to keep power dissipation and drift to acceptable levels.

# Chapter II

# INSIDE AN INSTRUMENTATION AMPLIFIER

**A Simple Op Amp Subtractor Provides an In-Amp Function**

The simplest (but still very useful) method of implementing a differential gain block is shown in Figure 2-1.

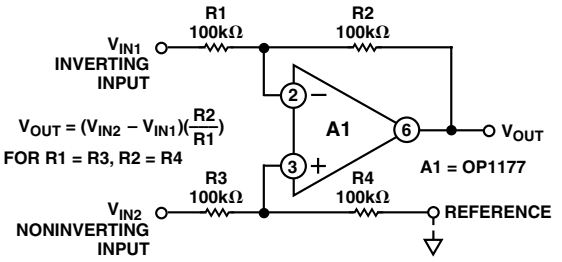



*Figure 2-1. A 1-op amp in-amp difference amplifier circuit functional block diagram.*

If R1 = R3 and R2 = R4, then

$$V_{OUT} = \left(V_{IN2} - V_{IN1}\right)\left(R2/R1\right)$$

Although this circuit provides an in-amp function, amplifying differential signals while rejecting those that are common mode, it also has some limitations. First, the impedances of the inverting and noninverting inputs are relatively low and unequal. In this example, the input impedance to $V_{IN1}$ equals 100 kΩ, while the impedance of $V_{IN2}$ is twice that, at 200 kΩ. Therefore, when voltage is applied to one input while grounding the other, different currents will flow depending on which input receives the applied voltage. (This unbalance in the sources' resistances will degrade the circuit's CMRR.)

Furthermore, this circuit requires a very close ratio match between resistor pairs R1/R2 and R3/R4; otherwise, the gain from each input would be different—directly affecting common-mode rejection. For example, at a gain of 1, with all resistors of equal value, a 0.1% mismatch in just one of the resistors will degrade the CMR to a level of 66 dB (1 part in 2000). Similarly, a source resistance imbalance of 100 Ω will degrade CMR by 6 dB.

In spite of these problems, this type of bare bones in-amp circuit, often called a difference amplifier or subtractor, is useful as a building block within higher performance in-amps. It is also very practical as a standalone functional circuit in video and other high speed uses, or in low frequency, high common-mode voltage (CMV) applications, where the input resistors divide down the input voltage as well as provide input protection for the amplifier. Some monolithic difference amplifiers such as Analog Devices' AD629 employ a variation of the simple subtractor in their design. This allows the IC to handle common-mode input voltages higher than its own supply voltage. For example, when powered from a ±15 V supply, the AD629 can amplify signals with common-mode voltages as high as ±270 V.

**Improving the Simple Subtractor with Input Buffering**

An obvious way to significantly improve performance is to add high input impedance buffer amplifiers ahead of the simple subtractor circuit, as shown in the 3-op amp instrumentation amplifier circuit of Figure 2-2.

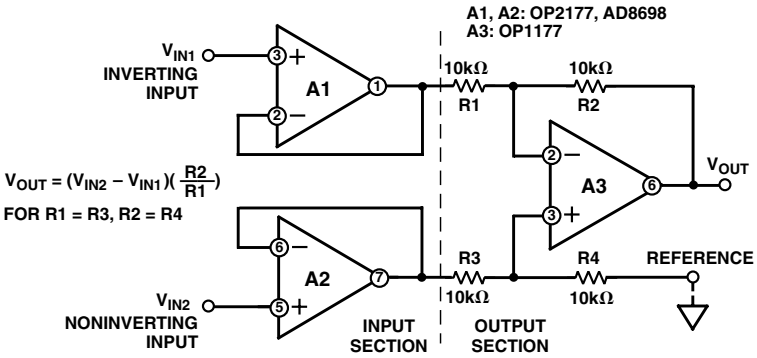



*Figure 2-2. A subtractor circuit with input buffering.*

This circuit provides matched, high impedance inputs so that the impedances of the input sources will have a minimal effect on the circuit's common-mode rejection. The use of a dual op amp for the 2-input buffer amplifiers is preferred because they will better track each other over temperature and save board space. Although the resistance values are different, this circuit has the same transfer function as the circuit of Figure 2-1.

Figure 2-3 shows further improvement: Now the input buffers are operating with gain, which provides a circuit with more flexibility. If the value of R5 = R8 and R6 = R7 and, as before, R1 = R3 and R2 = R4, then

$$V_{OUT} = (V_{IN2} - V_{IN1})\ (1 + R5/R6)\ (R2/R1)$$

While the circuit of Figure 2-3 does increase the gain (of $A_1$ and $A_2$) equally for differential signals, it also increases the gain for common-mode signals.

**The 3-Op Amp In-Amp**

The circuit of Figure 2-4 provides further refinement and has become the most popular configuration for instrumentation amplifier design. The classic 3-op amp in-amp circuit is a clever modification of the buffered subtractor circuit of Figure 2-3. As with the previous circuit, op amps A1 and A2 of Figure 2-4 buffer the input voltage. However, in this configuration, a single gain resistor, $R_G$, is connected between the summing junctions of the two input buffers, replacing R6 and R7. The full differential input voltage will now appear across $R_G$ (because the voltage at the summing junction of each amplifier is equal to the voltage applied to its positive input). Since the amplified input voltage (at the outputs of A1 and A2) appears differentially across the three resistors, R5, $R_G$, and R6, the differential gain may be varied by just changing $R_G$.

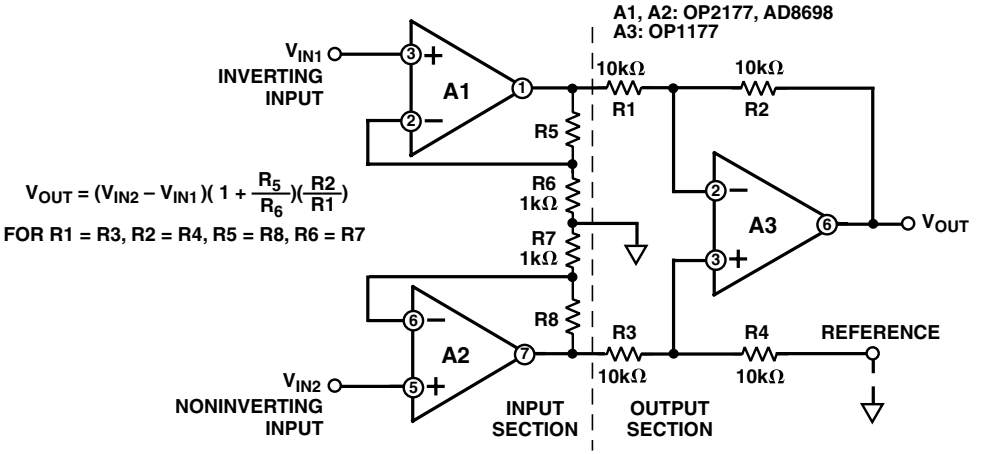



*Figure 2-3. A buffered subtractor circuit with buffer amplifiers operating with gain.*

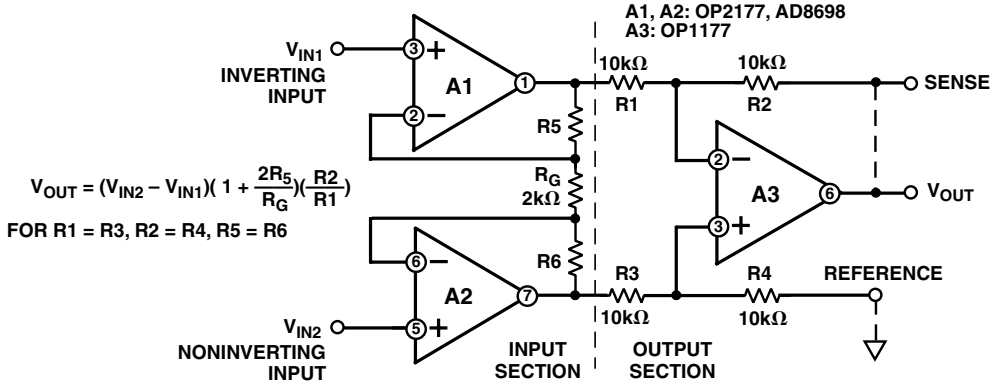



*Figure 2-4. The classic 3-op amp in-amp circuit.*

There is another advantage of this connection: Once the subtractor circuit has been set up with its ratio-matched resistors, no further resistor matching is required when changing gains. If the value of R5 = R6, R1 = R3, and R2 = R4, then

$$V_{OUT} = (V_{IN2} - V_{IN1})\ (1 + 2R5/R_G)(R2/R1)$$

Since the voltage across $R_G$ equals $V_{IN}$, the current through $R_G$ will equal ($V_{IN}/R_G$). Amplifiers A1 and A2, therefore, will operate with gain and amplify the input signal. Note, however, that if a common-mode voltage is applied to the amplifier inputs, the voltages on each side of $R_G$ will be equal, and no current will flow through this resistor. Since no current flows through $R_G$ (nor, therefore, through R5 and R6), amplifiers A1 and A2 will operate as unity-gain followers. Therefore, common-mode signals will be passed through the input buffers at unity gain, but differential voltages will be amplified by the factor ($1 + (2\ R_F/R_G)$).

In theory, this means that the user may take as much gain in the front end as desired (as determined by $R_G$) without increasing the common-mode gain and error. That is, the differential signal will be increased by gain, but the common-mode error will not, so the ratio (Gain ($V_{DIFF}$)/($V_{ERROR\ CM}$)) will increase. Thus, CMRR will theoretically increase in direct proportion to gain—a very useful property.

Finally, because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. This includes such errors as common-mode rejection vs. frequency. These features explain the popularity of this configuration.

**3-Op Amp In-Amp Design Considerations**

Two alternatives are available for constructing 3-op amp instrumentation amplifiers: using FET or bipolar input operational amplifiers. FET input op amps have very low bias currents and are generally well-suited for use with very high (>$10^6$ Ω) source impedances. FET amplifiers usually have lower CMR, higher offset voltage, and higher offset drift than bipolar amplifiers. They also may provide a higher slew rate for a given amount of power.

The sense and reference terminals (Figure 2-4) permit the user to change A3's feedback and ground connections. The sense pin may be externally driven for servo applications and others for which the gain of A3 needs to be varied. Likewise, the reference terminal allows an external offset voltage to be applied to A3. For normal operation, the sense and output terminals are tied together, as are reference and ground.

Amplifiers with bipolar input stages tend to achieve both higher CMR and lower input offset voltage drift than FET input amplifiers. Superbeta bipolar input stages combine many of the benefits of FET and bipolar processes, with even lower IB drift than FET devices.

A common (but frequently overlooked) issue for the unwary designer using a 3-op amp in-amp design is the reduction of common-mode voltage range that occurs when the in-amp is operating at high gain. Figure 2-5 is a schematic of a 3-op amp in-amp operating at a gain of 1000.

In this example, the input amplifiers, A1 and A2, are operating at a gain of 1000, while the output amplifier is providing unity gain. This means that the voltage at the output of each input amplifier will equal one-half

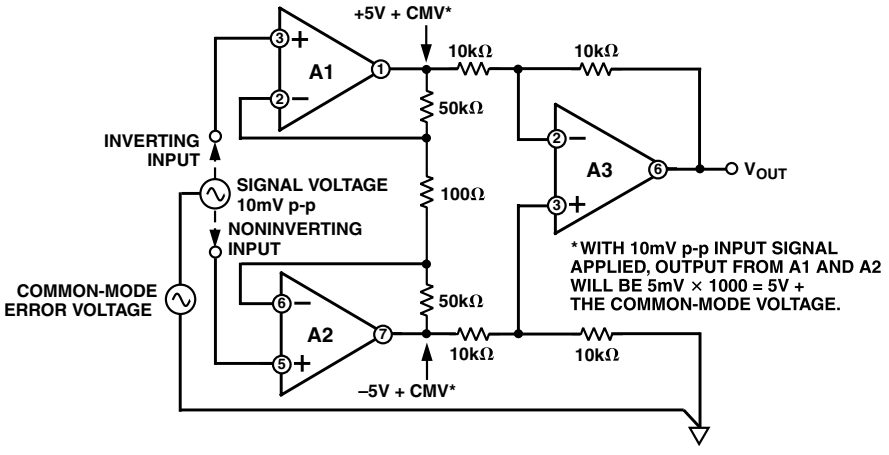



*Figure 2-5. A 3-op amp in-amp showing reduced CMV range.*

the peak-to-peak input voltage × 1000, plus any common-mode voltage that is present on the inputs (the common-mode voltage will pass through at unity gain regardless of the differential gain). Therefore, if a 10 mV differential signal is applied to the amplifier inputs, amplifier A1's output will equal +5 V, plus the common-mode voltage, and A2's output will be –5 V, plus the common-mode voltage. If the amplifiers are operating from 15 V supplies, they will usually have 7 V or so of headroom left, thus permitting an 8 V common-mode voltage—but not the full 12 V of CMV, which, typically, would be available at unity gain (for a 10 mV input). Higher gains or lower supply voltages will further reduce the common-mode voltage range.

**The Basic 2-Op Amp Instrumentation Amplifier**

Figure 2-6 is a schematic of a typical 2-op amp in-amp circuit. It has the obvious advantage of requiring only two, rather than three, operational amplifiers and providing savings in cost and power consumption. However, the nonsymmetrical topology of the 2-op amp in-amp circuit can lead to several disadvantages, most notably lower ac CMRR compared to the 3-op amp design, limiting the circuit's usefulness.

The transfer function of this circuit is

$$V_{OUT} = (V_{IN2} - V_{IN1})\ (1 + R4/R3)$$

$$for\ R1 = R4\ and\ R2 = R3$$

Input resistance is high and balanced, thus permitting the signal source to have an unbalanced output impedance. The circuit's input bias currents are set by the input current requirements of the noninverting input of the two op amps, which typically are very low.

Disadvantages of this circuit include the inability to operate at unity gain, a decreased common-mode voltage range as circuit gain is lowered, and poor ac common-mode rejection. The poor CMR is due to the unequal phase shift occurring in the two inputs, $V_{IN1}$ and $V_{IN2}$. That is, the signal must travel through amplifier A1 *before* it is subtracted from $V_{IN2}$ by amplifier A2. Thus, the voltage at the output of A1 is slightly delayed or phase-shifted with respect to $V_{IN1}$.

Minimum circuit gains of 5 are commonly used with the 2-op amp in-amp circuit because this permits an adequate dc common-mode input range, as well as sufficient bandwidth for most applications. The use of rail-to-rail (single-supply) amplifiers will provide a common-mode voltage range that extends down to $-V_S$ (or ground in single-supply operation), plus true rail-to-rail output voltage range (i.e., an output swing from $+V_S$ to $-V_S$).

Table 2-1 shows amplifier gain vs. circuit gain for the circuit of Figure 2-6 and gives practical 1% resistor values for several common circuit gains.

**Table 2-1. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 2-6.**

| Circuit Gain | Gain of A1 | Gain of A2 | R2, R3 | R1, R4 |
|---|---|---|---|---|
| 1.10 | 11.00 | 1.10 | 499 kΩ | 49.9 kΩ |
| 1.33 | 4.01 | 1.33 | 150 kΩ | 49.9 kΩ |
| 1.50 | 3.00 | 1.50 | 100 kΩ | 49.9 kΩ |
| 2.00 | 2.00 | 2.00 | 49.9 kΩ | 49.9 kΩ |
| 10.1 | 1.11 | 10.10 | 5.49 kΩ | 49.9 kΩ |
| 101.0 | 1.01 | 101.0 | 499 Ω | 49.9 kΩ |
| 1001 | 1.001 | 1001 | 49.9 Ω | 49.9 kΩ |

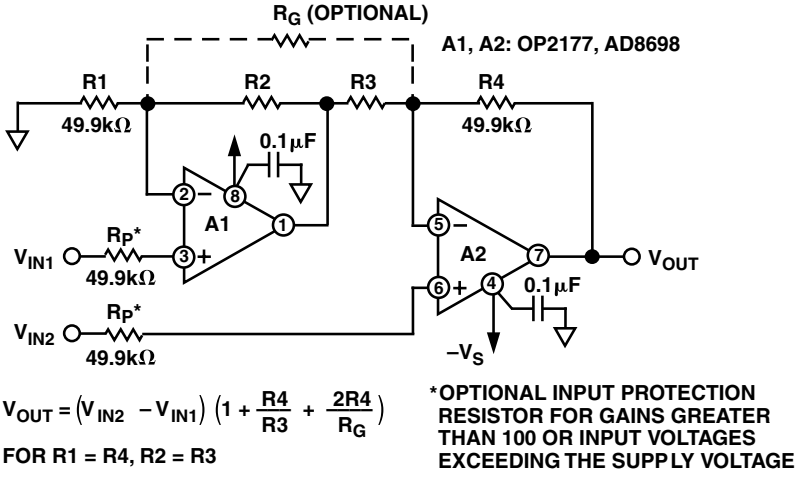



*Figure 2-6. A 2-op amp in-amp circuit.*

**2-Op Amp In-Amps—Common-Mode Design Considerations for Single-Supply Operation**

When the 2-op amp in-amp circuit of Figure 2-7 is examined from the reference input, it is apparent that it is simply a cascade of two inverters.

Assuming that the voltage at both of the signal inputs, $V_{IN1}$ and $V_{IN2}$, is 0, the output of A1 will equal

$$V_{O1} = -V_{REF}\ (R2/R1)$$

A positive voltage applied to $V_{REF}$ will tend to drive the output voltage of A1 negative, which is clearly *not* possible if the amplifier is operating from a single power supply voltage (+$V_S$ and 0 V).

The gain from the output of amplifier A1 to the circuit's output, $V_{OUT}$, at A2, is equal to

$$V_{OUT} = -V_{O1}\ (R4/R3)$$

The gain from $V_{REF}$ to $V_{OUT}$ is the product of these two gains and equals

$$V_{OUT} = (-V_{REF}\ (R2/R1))(-R4/R3)$$

In this case, R1 = R4 and R2 = R3. Therefore, the reference gain is +1, as expected. Note that this is the result of two inversions, in contrast to the noninverting signal path of the reference input in a typical 3-op amp in-amp circuit.

Just as with the 3-op amp in-amp, the common-mode voltage range of the 2-op amp in-amp can be limited by single-supply operation and by the choice of reference voltage.

Figure 2-8 is a schematic of a 2-op amp in-amp operating from a single 5 V power supply. The reference input is tied to $V_S/2$, which in this case is 2.5 V. The output voltage should ideally be 2.5 V for a differential input voltage of 0 V and for any common-mode voltage within the power supply voltage range (0 V to 5 V).

As the common-mode voltage is increased from 2.5 V toward 5 V, the output voltage of A1 ($V_{O1}$) will equal

$$V_{O1} = V_{CM} + ((V_{CM} - V_{REF})\ (R2/R1))$$

In this case, $V_{REF}$ = 2.5 V and R2/R1 = 1/4. The output voltage of A1 will reach 5 V when $V_{CM}$ = 4.5 V. Further increases in common-mode voltage obviously cannot be rejected. In practice, the input voltage range limitations of amplifiers A1 and A2 may limit the in-amp's common-mode voltage range to less than 4.5 V.

Similarly, as the common-mode voltage is reduced from 2.5 V toward 0 V, the output voltage of A1 will hit zero for a $V_{CM}$ of 0.5 V. Clearly, the output of A1 cannot go more negative than the negative supply line (assuming no charge pump), which, for a single-supply connection, equals 0 V. This negative or zero-in common-mode range limitation can be overcome by proper design of the in-amp's internal level shifting, as in the **AD627** monolithic 2-op amp instrumentation amplifier. However, even with good design, some positive common-mode voltage range will be traded off to achieve operation at zero common-mode voltage.

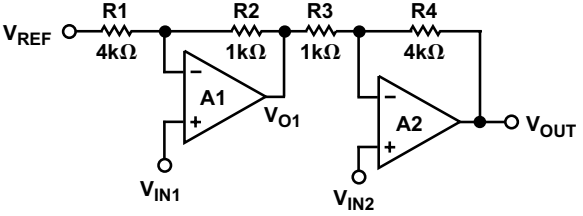



*Figure 2-7. The 2-op amp in-amp architecture.*

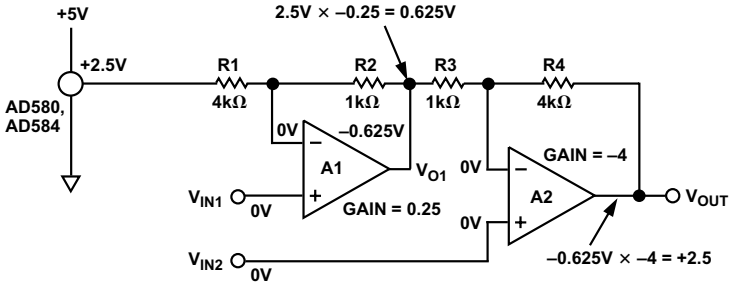



*Figure 2-8. Output swing limitations of 2-op amp in-amp using a 2.5 V reference.*

Another, and perhaps more serious, limitation of the standard 2-amplifier instrumentation amplifier circuit compared to 3-amplifier designs, is the intrinsic difficulty of achieving high ac common-mode rejection. This limitation stems from the inherent imbalance in the common-mode signal path of the 2-amplifier circuit.

Assume that a sinusoidal common-mode voltage, $V_{CM}$, at a frequency, $F_{CM}$, is applied (common mode) to inputs $V_{IN1}$ and $V_{IN2}$ (Figure 2-8). Ideally, the amplitude of the resulting ac output voltage (the common-mode error) should be 0 V, independent of frequency, $F_{CM}$, at least over the range of normal ac power line (mains) frequencies: 50 Hz to 400 Hz. Power lines tend to be the source of much common-mode interference.

If the ac common-mode error is zero, amplifier A2 and gain network R3, R4 must see zero instantaneous difference between the common-mode voltage, applied directly to $V_{IN2}$, and the version of the common-mode voltage that is amplified by A1 and its associated gain network R1, R2. Any dc common-mode error (assuming negligible error from the amplifier's own CMRR) can be nulled by trimming the ratios of R1, R2, R3, and R4 to achieve the balance

$$R1 \equiv R4 \text{ and } R2 \equiv R3$$

However, any phase shift (delay) introduced by amplifier A1 will cause the phase of $V_{O1}$ to slightly lag behind the phase of the directly applied common-mode voltage of $V_{IN2}$. This difference in phase will result in an instantaneous (vector) difference in $V_{O1}$ and $V_{IN2}$, even if the amplitudes of both voltages are at their ideal levels. This will cause a frequency-dependent common-mode error voltage at the circuit's output, $V_{OUT}$. Further, this ac common-mode error will increase linearly with common-mode frequency because the phase shift through A1 (assuming a single-pole roll-off) will increase directly with frequency. In fact, for frequencies less than 1/10th the closed-loop bandwidth ($f_{T1}$) of A1, the common-mode error (referred to the input of the in-amp) can be approximated by

$$\%CM\ Error = \frac{V_E/G}{V_{CM}}(100\%) = \frac{f_{CM}}{f_{TI}}(100\%)$$

where $V_E$ is the common-mode error voltage at $V_{OUT}$, and $G$ is the differential gain—in this case, 5.

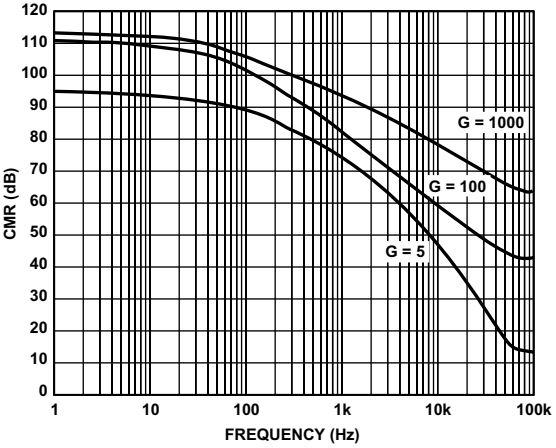



*Figure 2-9. CMR vs. frequency of AD627 in-amp circuit.*

For example, if A1 has a closed-loop bandwidth of 100 kHz (a typical value for a micropower op amp), when operating at the gain set by R1 and R2, and the common-mode frequency is 100 Hz, then

$$\%CM\ Error = \frac{100\,\text{Hz}}{100\,\text{kHz}}(100\%) = 0.1\%$$

A common-mode error of 0.1% is equivalent to 60 dB of common-mode rejection. So, in this example, even if this circuit were trimmed to achieve 100 dB CMR at dc, this would be valid only for frequencies less than 1 Hz. At 100 Hz, the CMR could never be better than 60 dB.

The AD627 monolithic in-amp embodies an advanced version of the 2-op amp instrumentation amplifier circuit that overcomes these ac common-mode rejection limitations. As illustrated in Figure 2-9, the AD627 maintains over 80 dB of CMR out to 8 kHz (gain of 1000), even though the bandwidth of amplifiers A1 and A2 is only 150 kHz.

The four resistors used in the subtractor are normally internal to the IC and are usually of very high resistance. High common-mode voltage difference amps (diff amps) typically use input resistors selected to provide voltage attenuation. Therefore, both the differential signal voltage and the common-mode voltage are attenuated, the common mode is rejected, and then the signal voltage is amplified.

# Chapter III

# MONOLITHIC INSTRUMENTATION AMPLIFIERS

## ADVANTAGES OVER OP AMP IN-AMPS

Monolithic IC instrumentation amplifiers were developed to satisfy the demand for in-amps that would be easier to apply. These circuits incorporate variations in the 3-op amp and 2-op amp in-amp circuits previously described, while providing laser-trimmed resistors and other benefits of monolithic IC technology. Since both active and passive components are now within the same die, they can be closely matched—this will ensure that the device provides a high CMR. In addition, these components will stay matched over temperature, ensuring excellent performance over a wide temperature range. IC technologies such as laser wafer trimming allow monolithic integrated circuits to be tuned up to very high accuracy and provide low cost, high volume manufacturing. An additional advantage of monolithic devices is that they are available in very small, very low cost SOIC, MSOP, or LFCSP (chip scale) packages designed for use in high volume production. Table 3-1 provides a quick performance summary of Analog Devices in-amps.

### Which to Use—an In-Amp or a Diff Amp?

Although instrumentation amplifiers and difference amplifiers share many properties, the first step in the design process should be which type of amplifier to use.

A difference amplifier is basically an op amp subtractor, typically using high value input resistors. The resistors provide protection by limiting the amplifier's input current. They also reduce the input common-mode and differential voltage to a range that can be handled by the internal subtractor amplifier. In general, difference amplifiers should be used in applications where the common-mode voltage or voltage transients may exceed the supply voltage.

**Table 3-1. Latest Generation Analog Devices In-Amps Summarized[1]**

| Product | Features | Power Supply Current Typ | –3 dB BW Typ (G = 10) | CMR G = 10 (dB) Min | Input Offset Voltage Max | $V_{OS}$ Drift (µV/°C) Max | RTI Noise[2] (nV/√Hz) (G = 10) | Input Bias Current (nA) Max |
|---|---|---|---|---|---|---|---|---|
| AD8221 | Precision, high BW | 0.9 mA | 560 kHz | 100[3] | 60 µV | 0.4 | 11 max | 1.5 |
| AD620 | General-purpose | 0. 9 mA | 800 kHz | 95[3] | 125 µV | 1 | 16 max | 2 |
| AD8225 | Precision gain = 5 | 1.1 mA | 900 kHz[4] | 83[4, 5] | 150 µV | 0.3 | 45 typ[4] | 1.2 |
| AD8220 | R-R, JFET input | 750 µA | 1500 kHz | 100 | 250 µV | 5 | 17 typ | 10 pA |
| AD8222 | Dual, precision, high BW | 1.8 mA | 750 kHz | 100[3] | 120 µV | 0.4 | 11 max | 2 |
| AD8230 | R-R, zero drift | 2.7 mA | 2 kHz | 110 | 10 µV | 10 | 240 typ | 1 |
| AD8250 | High BW, programmable gain | 3.5 mA | 3.5 MHz | 100 | 100 µV | 1 | 13 typ | 15 |
| AD8251 | High BW, programmable gain | 3.5 mA | 3.5 MHz | 100 | 100 µV | 1 | 13 typ | 15 |
| AD8553 | Auto-zero with shutdown | 1.1 mA | 1 kHz | 100 | 20 µV | 0.1 | 150 typ | 1 |
| AD8555 | Zero drift dig prog | 2.0 mA | 700 kHz[6] | 80[6] | 10 µV | 0.07 | 32 typ | 22 |
| AD8556 | Dig prog IA with filters | 2.0 mA | 700 kHz[6] | 80[6] | 10 µV | 0.07 | 32 typ | 54 |
| AD622 | Low cost | 0.9 mA | 800 kHz | 86[3] | 125 µV | 1 | 14 typ | 5 |
| AD621 | Precise gain | 0.9 mA | 800 kHz | 93[3] | 250 µV[7] | 2.5[7] | 17 max[7] | 2 |
| AD623 | Low cost, S.S. | 375 µA | 800 kHz | 90[3] | 200 µV | 2 | 35 typ | 25 |
| AD627 | Micropower, S.S. | 60 µA | 80 kHz | 100 | 250 µV | 3 | 42 typ | 10 |

NOTES
S.S. = single supply.
[1]Refer to ADI website at www.analog.com for latest products and specifications.
[2]At 1 kHz. RTI noise = $\sqrt{((e_{ni})^2 + (e_{no/G})^2)}$.
[3]For dc to 60 Hz, 1 kΩ source imbalance.
[4]Operating at a gain of 5.
[5]For 10 kHz, 1 kΩ source imbalance.
[6]Operating at a gain of 70.
[7]Referred to input (RTI).

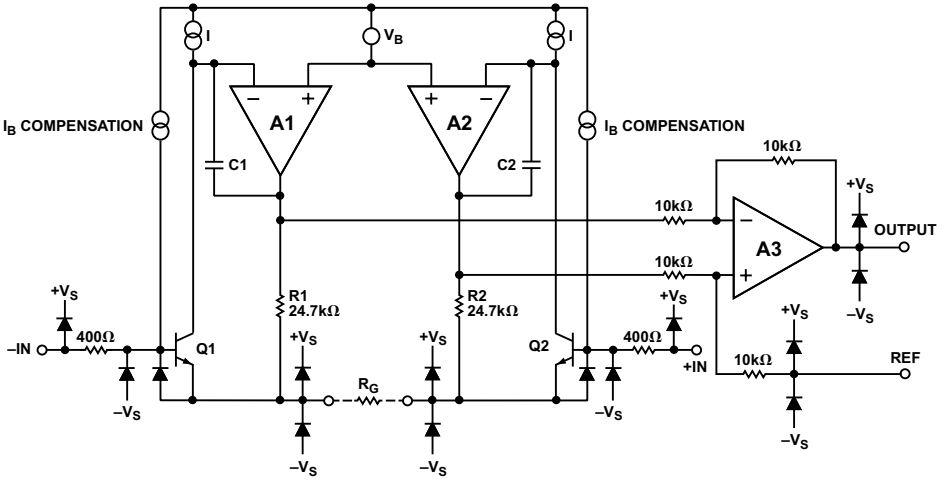



*Figure 3-1. AD8221 simplified schematic.*

In contrast, an instrumentation amplifier is most commonly an op amp subtractor with two input buffer amplifiers (these increase the input Z and thus reduce loading of the input source). An in-amp should be used when the total input common-mode voltage plus the input differential voltage, including transients, is less than the supply voltage. In-amps are also needed in applications where the highest accuracy, best signal-to-noise ratio, and lowest input bias current are essential.

## MONOLITHIC IN-AMP DESIGN—THE INSIDE STORY

### High Performance In-Amps

Analog Devices introduced the first high performance monolithic instrumentation amplifier, the **AD520**, in 1971.

In 2003, the **AD8221** was introduced. This in-amp is in a tiny MSOP package and offers increased CMR at higher bandwidths than other competing in-amps. It also has improved ac and dc specifications over the industry-standard **AD620** series in-amps.

The AD8221 is a monolithic instrumentation amplifier based on the classic 3-op amp topology (Figure 3-1). Input transistors Q1 and Q2 are biased at a constant current so that any differential input signal will force the output voltages of A1 and A2 to be equal. A signal applied to the input creates a current through $R_G$, R1, and R2 such that the outputs of A1 and A2 deliver the correct voltage. Topologically, Q1, A1, R1 and Q2, A2, R2 can be viewed as precision current feedback amplifiers. The amplified differential and common-mode signals are applied to a difference amplifier, A3, which rejects the common-mode voltage, but processes the differential voltage. The difference amplifier has a low output offset voltage as well as low output offset voltage drift. Laser-trimmed resistors allow for a highly accurate in-amp with gain error typically less than 20 ppm and CMRR that exceeds 90 dB (G = 1).

Using superbeta input transistors and an $I_B$ compensation scheme, the AD8221 offers extremely high input impedance, low $I_B$, low $I_{OS}$, low $I_B$ drift, low input bias current noise, and extremely low voltage noise of 8 nV/$\sqrt{\text{Hz}}$.

The transfer function of the AD8221 is

$$G = \frac{49.4\,\text{k}\Omega}{R_G} + 1$$

$$R_G = \frac{49.4\,\text{k}\Omega}{G - 1}$$

Care was taken to ensure that a user could easily and accurately set the gain using a single external standard value resistor.

Since the input amplifiers employ a current feedback architecture, the AD8221's gain bandwidth product increases with gain, resulting in a system that does not suffer from the expected bandwidth loss of voltage feedback architectures at higher gains.

In order to maintain precision even at low input levels, special care was taken with the AD8221's design and layout, resulting in an in-amp whose performance satisfies even the most demanding applications (see Figures 3-3 and 3-4).

A unique pinout enables the AD8221 to meet an unparalleled CMRR specification of 80 dB at 10 kHz (G = 1) and 110 dB at 1 kHz (G = 1000). The balanced pinout, shown in Figure 3-2, reduces the parasitics that had, in the past, adversely affected CMR performance. In addition, the new pinout simplifies board layout because associated traces are grouped. For example, the gain setting resistor pins are adjacent to the inputs, and the reference pin is next to the output.

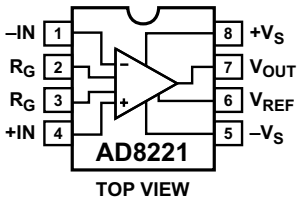



*Figure 3-2. AD8221 pinout.*

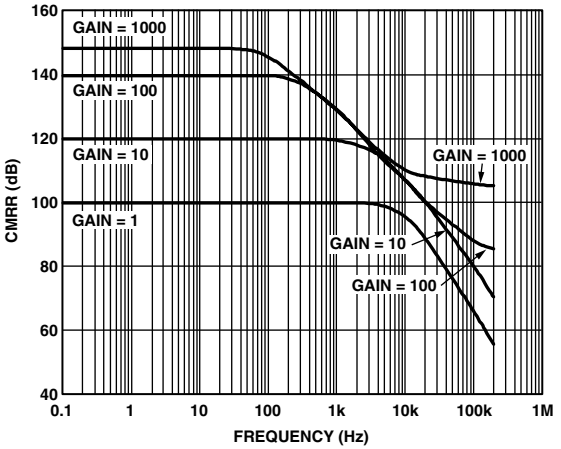



*Figure 3-3. CMRR vs. frequency (RTI) of the AD8221.*

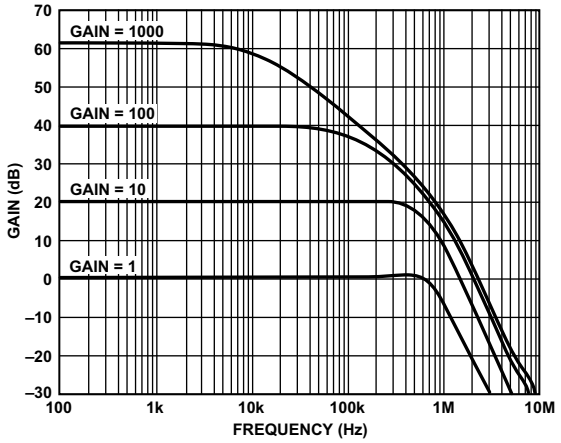



*Figure 3-4. AD8221 closed-loop gain vs. frequency.*

The **AD8222** (Figure 3-5) is a dual version of the AD8221 in-amp, with similar performance and specifications. Its small size allows more amplifiers per PC board. In addition, the AD8222 is the first in-amp to be specified for differential output performance. It is available in a 4 mm × 4 mm, 16-lead LFCSP package.

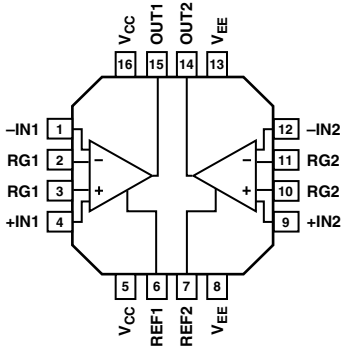



*Figure 3-5. AD8222 connection diagram.*

For many years, the **AD620** has been the industry-standard, high performance, low cost in-amp. The AD620 is a complete monolithic instrumentation amplifier offered in both 8-lead DIP and SOIC packages. The user can program any desired gain from 1 to 1000 using a single external resistor. By design, the required resistor values for gains of 10 and 100 are standard 1% metal film resistor values.

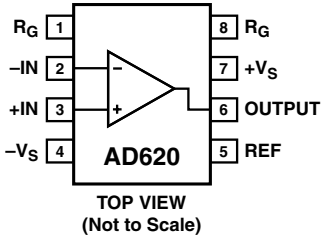



*Figure 3-6. AD620 pin configuration.*

The AD620 (see Figure 3-7) is a second-generation version of the classic **AD524** in-amp and embodies a modification of its 3-op amp circuit. Laser trimming of on-chip thin film resistors, R1 and R2, allows the user to accurately set the gain to 100 within ±0.3% max error, using only one external resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components.

A preamp section comprised of Q1 and Q2 provides additional gain up front. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains a constant collector current through the input devices Q1 and Q2,

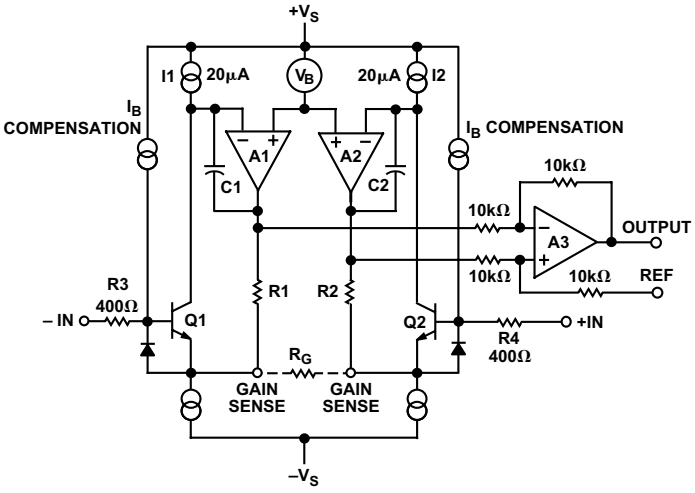



*Figure 3-7. A simplified schematic of the AD620.*

thereby impressing the input voltage across the external gain setting resistor, $R_G$. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity-gain subtractor, A3, removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of $R_G$ also determines the transconductance of the preamp stage. As $R_G$ is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has important advantages: First, the open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors. Second, the gain bandwidth product (determined by C1, C2, and the preamp transconductance) increases with programmed gain, thus optimizing the amplifier's frequency response. Figure 3-8 shows the AD620's closed-loop gain vs. frequency.

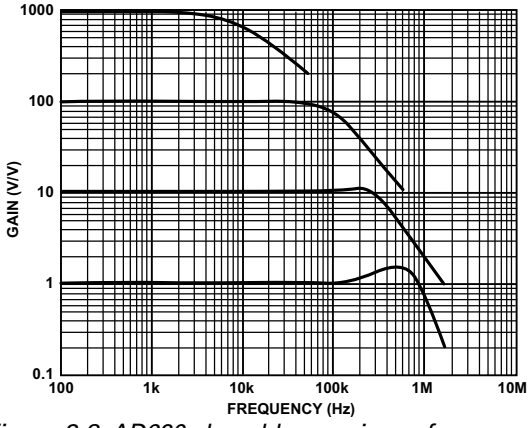



*Figure 3-8. AD620 closed-loop gain vs. frequency.*

The AD620 also has superior CMR over a wide frequency range, as shown in Figure 3-9.

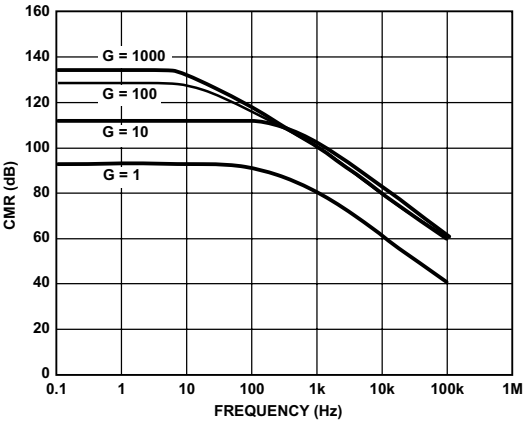



*Figure 3-9. AD620 CMR vs. frequency.*

Figures 3-10 and 3-11 show the AD620's gain nonlinearity and small signal pulse response.

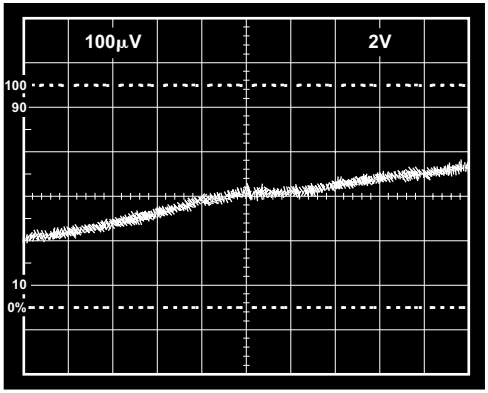



*Figure 3-10. AD620 gain nonlinearity (G = 100, $R_L$ = 10 kΩ, vertical scale: 100 µV = 10 ppm, horizontal scale: 2 V/div).*

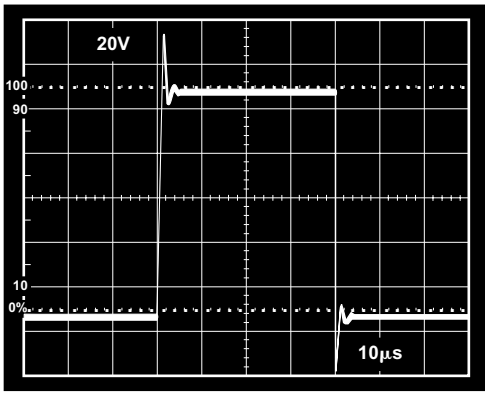



*Figure 3-11. Small signal pulse response of the AD620 (G = 10, $R_L$= 2 kΩ, $C_L$ = 100 pF).*

Finally, the input voltage noise is reduced to a value of 9 nV/$\sqrt{\text{Hz}}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor. The gain equation is then

$$G = \frac{49.4\,\text{k}\Omega}{R_G} + 1$$

So that

$$R_G = \frac{49.4\,\text{k}\Omega}{G - 1}$$

Where resistor $R_G$ is in kΩ.

The value of 24.7 kΩ was chosen so that standard 1% resistor values could be used to set the most popular gains.

**Low Cost In-Amps**

The **AD622** is a low cost version of the AD620 (see Figure 3-6). The AD622 uses streamlined production methods to provide most of the performance of the AD620 at lower cost.

Figures 3-12, 3-13, and 3-14 show the AD622's CMR vs. frequency, gain nonlinearity, and closed-loop gain vs. frequency.

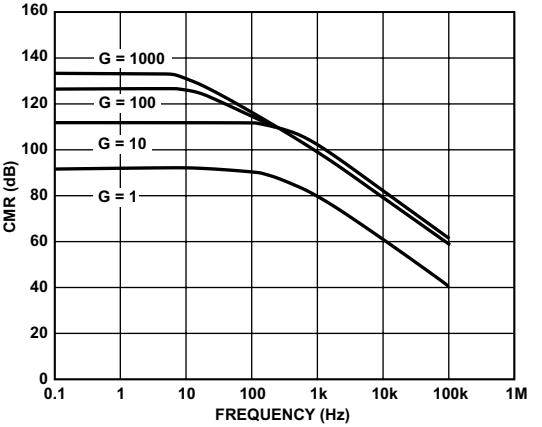



*Figure 3-12. AD622 CMR vs. frequency ((RTI) 0 to 1 kΩ source imbalance).*

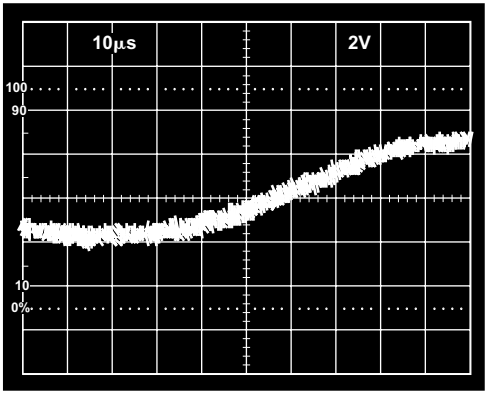



*Figure 3-13. AD622 Gain nonlinearity (G = 1, $R_L$ = 10 kΩ, vertical scale: 20 µV = 2 ppm).*

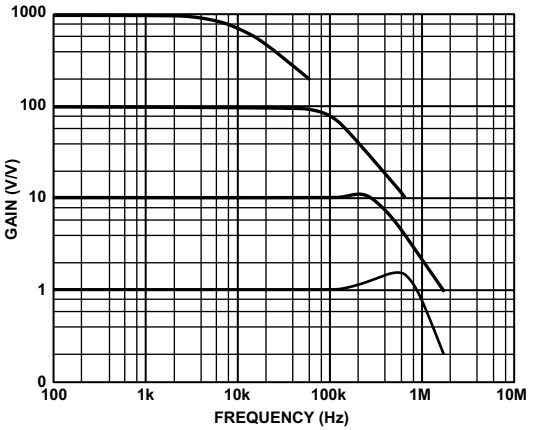



*Figure 3-14. AD622 closed-loop gain vs. frequency.*

**Pin-Programmable, Precise Gain In-Amps**

The **AD621** is similar to the AD620, except that for gains of 10 and 100 the gain setting resistors are on the die—no external resistors are used. A single external jumper (between Pins 1 and 8) is all that is needed to select a gain of 100. For a gain of 10, leave Pin 1 and Pin 8 open. This provides excellent gain stability over temperature, as the on-chip gain resistor tracks the TC of the feedback resistor. Figure 3-15 is a simplified schematic of the AD621. With a max total gain error of 0.15% and ±5 ppm/°C gain drift, the AD621 has much greater built-in accuracy than the AD620.

The AD621 may also be operated at gains between 10 and 100 by using an external gain resistor, although gain error and gain drift over temperature will be degraded. Using external resistors, device gain is equal to

$$G = (R1 + R2)/R_G + 1$$

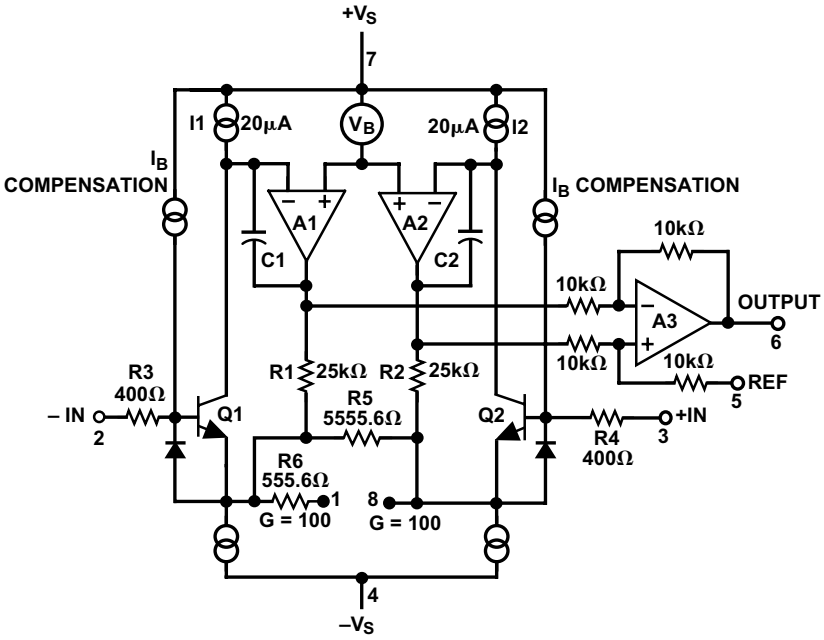



*Figure 3-15. A simplified schematic of the AD621.*

Figures 3-16 and 3-17 show the AD621's CMR vs. frequency and closed-loop gain vs. frequency.

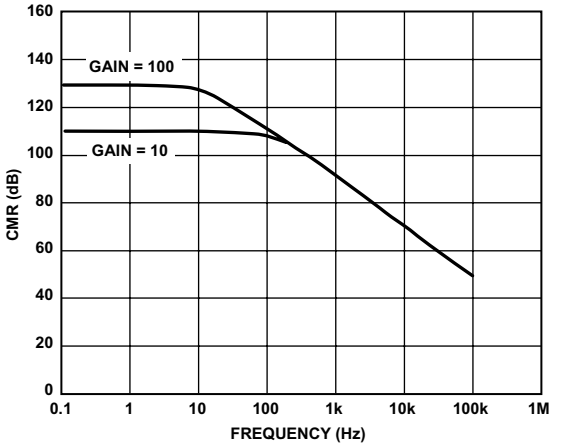



*Figure 3-16. AD621 CMR vs. frequency.*

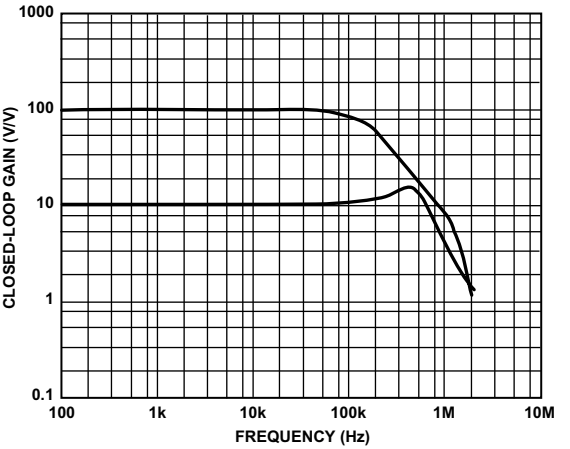



*Figure 3-17. AD621 closed-loop gain vs. frequency.*

Figures 3-18 and 3-19 show the AD621's gain nonlinearity and small signal pulse response.

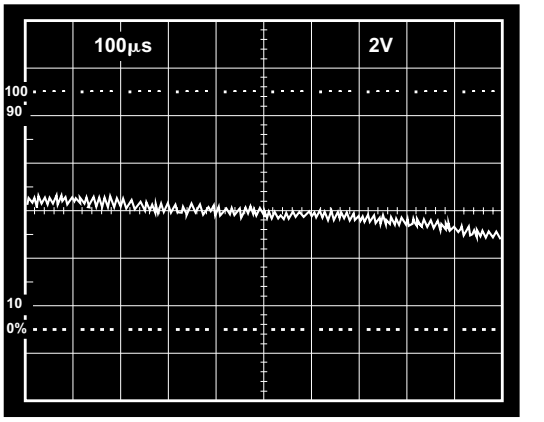



*Figure 3-18. AD621 gain nonlinearity (G = 10, $R_L$ = 10 kΩ, vertical scale: 100 µV/div = 100 ppm/div, horizontal scale 2 V/div).*

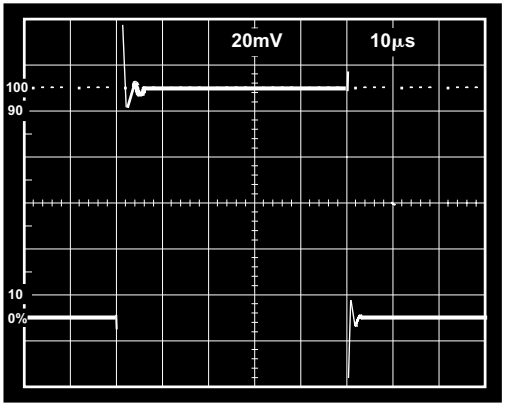



*Figure 3-19. Small signal pulse response of the AD621 (G = 10, $R_L$ = 2 kΩ, $C_L$ = 100 pF).*

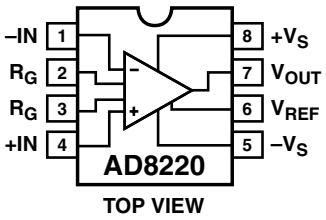



*Figure 3-20. AD8220 connection diagram.*

The **AD8220** is a FET input, gain-programmable, high performance instrumentation amplifier with a max input bias current of 10 pA. It also features excellent high frequency common-mode rejection (see Figure 3-20). The AD8220 maintains a minimum CMRR of 70 dB up to 20 kHz, at G = 1. The combination of extremely high input impedance and high CMRR over frequency makes the AD8220 useful in applications such as patient monitoring. In these applications, input impedance is high and high frequency interference must be rejected.

The rail-to-rail output, low power consumption and small MSOP/CSP package make this precision instrumentation amplifier attractive for use in multi-channel applications.

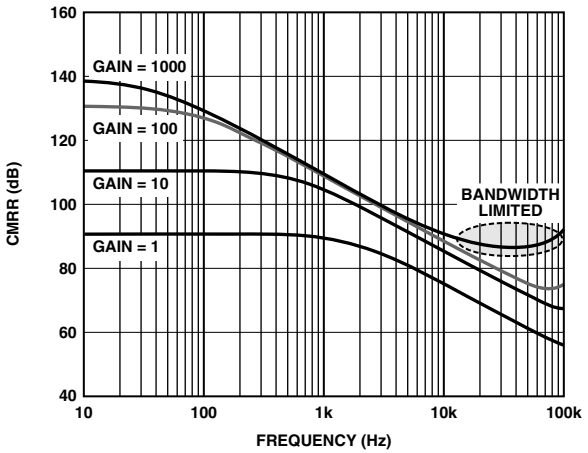



*Figure 3-21. Typical AD8220 CMRR vs. frequency.*

A single resistor sets the gain from 1 to 1000. The AD8220 operates on both single and dual supplies and is well-suited for applications where input voltages close to those of the supply are encountered. In addition, its rail-to-rail output stage allows for maximum dynamic range, when constrained by low single-supply voltages.

**Auto-Zeroing Instrumentation Amplifiers**

Auto-zeroing is a dynamic offset and drift cancellation technique that reduces input referred voltage offset to the μV level, and voltage offset drift to the nV/°C level.

The **AD8230** (Figure 3-22) is an instrumentation amplifier that utilizes an auto-zeroing topology and combines it with high common-mode signal rejection.

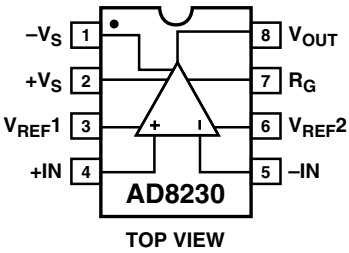



*Figure 3-22. AD8230 connection diagram.*

The internal signal path consists of an active differential sample-and-hold stage (preamp), followed by a differential amplifier (gain amp). Both amplifiers implement auto-zeroing to minimize offset and drift. A fully differential topology increases the immunity of the signals to parasitic noise and temperature effects. Amplifier gain is set by two external resistors for convenient TC matching. The AD8230 can accept input common-mode voltages within and including the supply voltages (±5 V).

The signal sampling rate is controlled by an on-chip, 10 kHz oscillator and logic to derive the required nonoverlapping clock phases. For simplification of the functional description, two sequential clock phases, A and B, will be used to distinguish the order of internal operation as depicted in Figures 3-23 and 3-24, respectively.

During Phase A, the sampling capacitors are connected to the input signals at the common-mode potential. The input signal's difference voltage, $V_{DIFF}$, is stored across the sampling capacitors, $C_{SAMPLE}$. The common-mode potential of the input affects $C_{SAMPLE}$ insofar as the sampling capacitors are at a different common-mode potential than the preamp. During this period, the gain amp is disconnected from the preamp so that its output remains at the level set by the previously sampled input signal, held on $C_{HOLD}$ in Figure 3-23.

In Phase B, upon sampling the analog input signals, the input common-mode component is removed. The common-mode output of the preamp is held at the reference potential, $V_{REF}$. When the bottom plates of the sampling capacitors connect to the output of the preamp, the input signal common-mode voltage is pulled to the amplifier's common-mode voltage, $V_{REF}$. In this manner, the sampling capacitors are brought to the same common-mode voltage as the preamp. The remaining differential signal is presented to the gain amp, refreshing the hold capacitors' signal potentials, as shown in Figure 3-24.

Figures 3-25 through 3-28 show the internal workings of the AD8230 in depth. As noted, both the preamp and gain amp auto-zero. The preamp auto-zeroes during phase A, shown in Figure 3-25, while the sampling caps are connected to the signal source. By connecting the

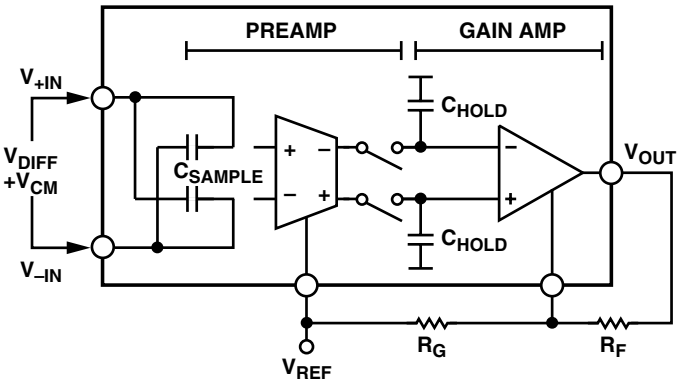



*Figure 3-23. The AD8230 in Phase A sampling phase. The differential component of the input signal is stored on sampling capacitors, $C_{SAMPLE}$. The gain amp conditions the signal stored on the hold capacitors, $C_{HOLD}$. Gain is set with the $R_G$ and $R_F$ resistors.*

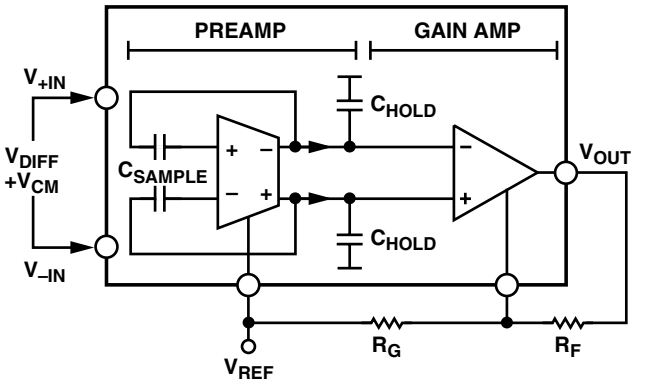



*Figure 3-24. In Phase B, the differential signal is transferred to the hold capacitors, refreshing the value stored on $C_{HOLD}$. The gain amp continues to condition the signal stored on the hold capacitors, $C_{HOLD}$.*

preamp differential inputs together, the resulting output referred offset is connected to an auxiliary input port to the preamp. Negative feedback operation forces a canceling potential at the auxiliary port, which is subsequently held on a storage capacitor, $C_{P\_HOLD}$.

While in Phase A, the gain amp shown in Figure 3-26 reads the previously sampled signal held on the holding capacitors, $C_{HOLD}$. The gain amp implements feedforward offset compensation to allow for transparent nulling of the main amp and a continuous output signal. A differential signal regimen is maintained throughout the main amp and feedforward nulling amp by utilizing a double differential input topology. The nulling amp compares the input of the two differential signals. As a result, the offset error is fed into the null port of the main amp, $V_{NULL}$, and stored on $C_{M\_HOLD}$. This operation effectively forces the differential input potentials at both the signal and feedback ports of the main amp to be equal. This is the requirement for zero offset.

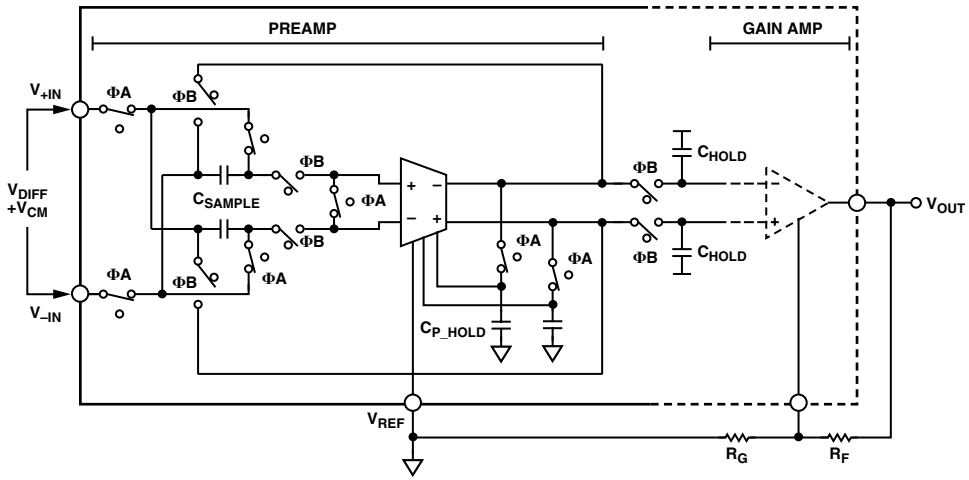



*Figure 3-25. Detailed schematic of the preamp during Phase A. The differential signal is stored on the sampling capacitors. Concurrently, the preamp nulls its own offset and stores the correction voltage on its hold capacitors, $C_{P\_HOLD}$.*

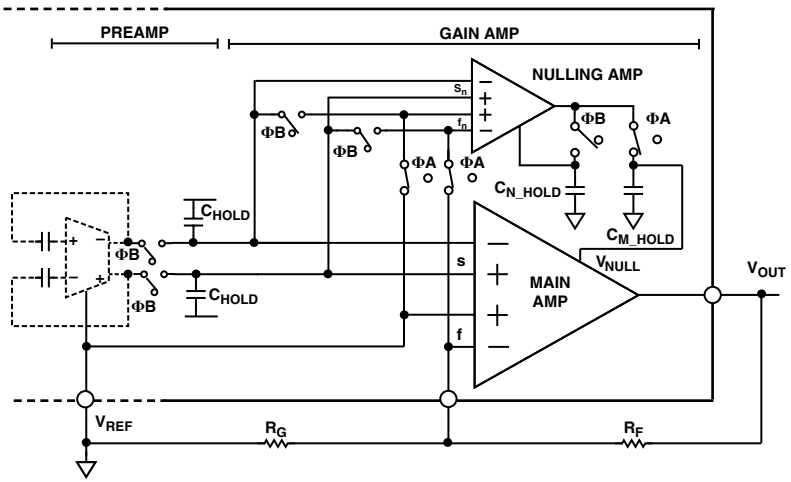



*Figure 3-26. Detailed schematic of the gain amp during Phase A. The main amp conditions the signal held on the hold capacitors, $C_{HOLD}$. The nulling amplifier forces the inputs of the main amp to be equal by injecting a correction voltage into the $V_{NULL}$ port, removing the offset of the main amp. The correction voltage is stored on $C_{M\_HOLD}$.*

During Phase B, the inputs of the preamp are no longer shorted, and the sampling capacitors are connected to the input and output of the preamp as shown in Figure 3-27. The preamp, having been auto-zeroed in Phase A, has minimal offset. When the sampling capacitors are connected to the preamp, the common mode of the sampling capacitors is brought to $V_{REF}$. The preamp outputs the difference signal onto the hold capacitors, $C_{HOLD}$.

The main amp continues to output the gained difference signal, shown in Figure 3-28. Its offset is kept to a minimum by using the nulling amp's correction potential stored on $C_{M\_HOLD}$ from the previous phase. During this phase, the nulling amp compares its two differential inputs and corrects its own offset by driving a correction voltage into its nulling port and, ultimately, onto $C_{N\_HOLD}$. In this fashion, the nulling amp reduces its own offset in Phase B before it corrects for the main amp's offset in the next phase, Phase A.

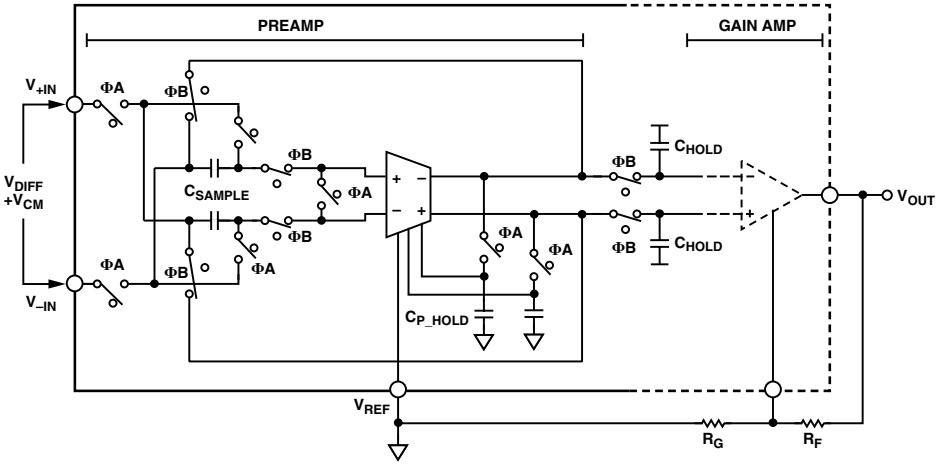



*Figure 3-27. Detailed schematic of the preamp during Phase B. The preamp's offset remains low because it was corrected in the previous phase. The sampling capacitors connect to the input and output of the preamp, and the difference voltage is passed onto the holding capacitors, $C_{HOLD}$.*

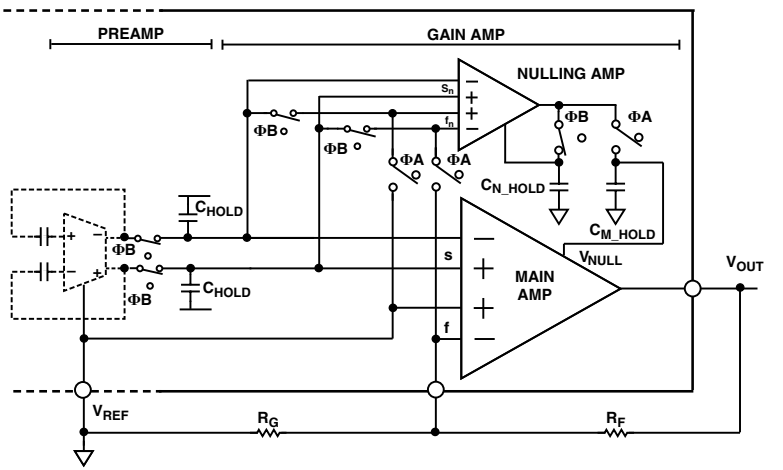



*Figure 3-28. Detailed schematic of the gain amp during Phase B. The nulling amplifier nulls its own offset by injecting a correction voltage into its own auxiliary port and storing it on $C_{N\_HOLD}$. The main amplifier continues to condition the differential signal held on $C_{HOLD}$, yet maintains minimal offset because its offset was corrected in the previous phase.*

Two external resistors set the gain of the AD8230. The gain is expressed in the following function:

$$Gain = 2\left(1 + \frac{R_F}{R_G}\right)$$

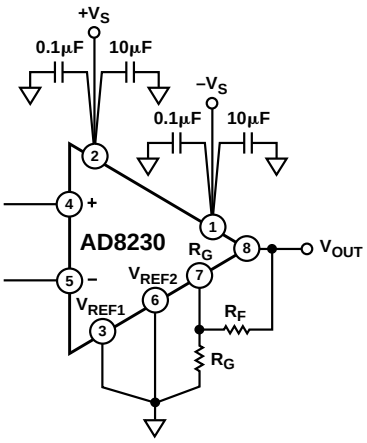



*Figure 3-29. Gain setting.*

**Table 3-2. Gains Using Standard 1% Resistors**

| Gain | $R_F$ | $R_G$ | Actual Gain |
|---|---|---|---|
| 2 | 0 Ω (short) | None | 2 |
| 10 | 8.06 kΩ | 2 kΩ | 10 |
| 50 | 12.1 kΩ | 499 Ω | 50.5 |
| 100 | 9.76 kΩ | 200 Ω | 99.6 |
| 200 | 10 kΩ | 100 Ω | 202 |
| 500 | 49.9 kΩ | 200 Ω | 501 |
| 1000 | 100 kΩ | 200 Ω | 1002 |

Figure 3-29 and Table 3-2 provide an example of some gain settings. As Table 3-2 shows, the AD8230 accepts a wide range of resistor values. Since the instrumentation apmplifier has finite driving capability, ensure that the output load in parallel with the sum of the gain setting resistors is greater than 2 kΩ.

$$R_L \left\| \left(R_F + R_G\right) > 2\ \text{k}\Omega \right.$$

Offset voltage drift at high temperature can be minimized by keeping the value of the feedback resistor, $R_F$, small. This is due to the junction leakage current on the $R_G$ pin, Pin 7.

Figure 3-30 shows the AD8230's common-mode rejection vs. frequency. Figure 3-31 is a plot of AD8230's gain flatness vs. frequency at a gain of 10.

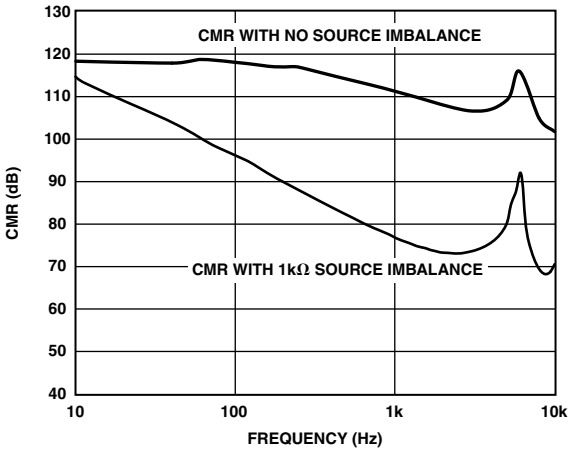



*Figure 3-30. Common-mode rejection vs. frequency.*

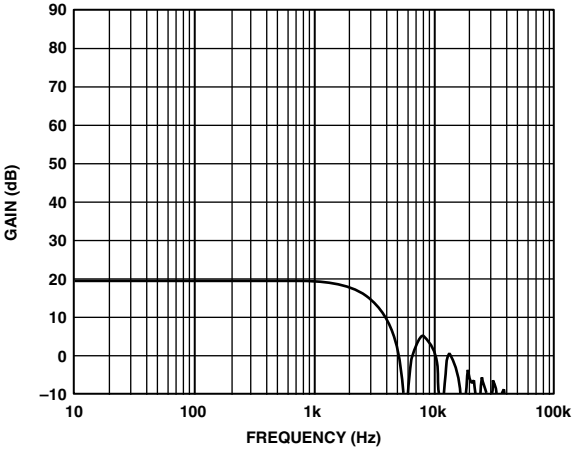



*Figure 3-31. Gain vs. frequency, G = 10.*

The **AD8553** is a precision current-mode auto-zero instrumentation amplifier capable of single-supply operation. The current-mode correction topology results in excellent accuracy, without the need for trimmed resistors on the die.

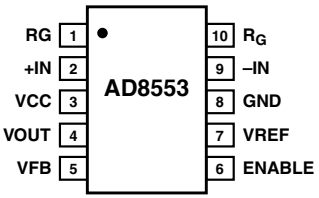



*Figure 3-32. AD8553 connection diagram.*

Figure 3-32 is the AD8553 connection diagram while Figure 3-33 shows a simplified schematic illustrating the basic operation of the AD8553 (without correction). The circuit consists of a voltage-to-current amplifier (M1 to M6), followed by a current-to-voltage amplifier (R2 and A1). Application of a differential input voltage forces a current through external resistor R1, resulting in conversion of the input voltage to a signal current. Transistors M3 to M6 transfer twice this signal current to the inverting input of the op amp A1. Amplifier A1 and external resistor R2 form a current-to-voltage converter to produce a rail-to-rail output voltage at VOUT.

Op amp A1 is a high precision auto-zero amplifier. This amplifier preserves the performance of the autocorrection current-mode amplifier topology while offering the user a true voltage-in, voltage-out instrumentation amplifier. Offset errors are corrected internally.

An external reference voltage is applied to the noninverting input of A1 for output-offset adjustment. Because the AD8553 is essentially a *chopper* in-amp, some type of low-pass filtering of the ouput is usually required. External capacitor C2 is used to filter out high frequency noise.

The pinout of the AD8553 allows the user to access the signal current from the output of the voltage-to-current converter (Pin 5). The user can choose to use the AD8553 as a current-output device instead of a voltage-output device.

The **AD8555** is a zero-drift, sensor signal amplifier with digitally programmable gain and output offset. Designed to easily and accurately convert variable pressure sensor and strain bridge outputs to a well-defined output voltage range, the AD8555 also accurately amplifies many other differential or single-ended sensor outputs.

Figure 3-34 shows the pinout and Figure 3-35 the simplified schematic.

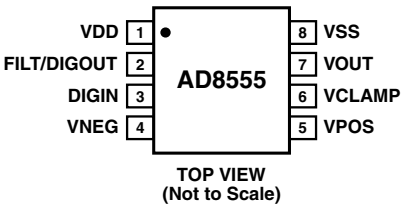



*Figure 3-34. AD8555 connection diagram.*

The AD8555 (and **AD8556**) use both auto-zeroing and "chopping" techniques to maintin zero drift. A1, A2, R1, R2, R3, P1, and P2 form the first gain stage of the differential amplifier. A1 and A2 are auto-zeroed op amps that minimize input offset errors. P1 and P2 are digital potentiometers, guaranteed to be monotonic. Programming P1 and P2 allows the first stage gain to be varied from 4.0 to 6.4 with 7-bit resolution, giving a fine gain adjustment resolution of 0.37%. R1, R2, R3, P1, and P2 each have a similar temperature coefficient, so the first stage gain temperature coefficient is lower than 100 ppm/°C.

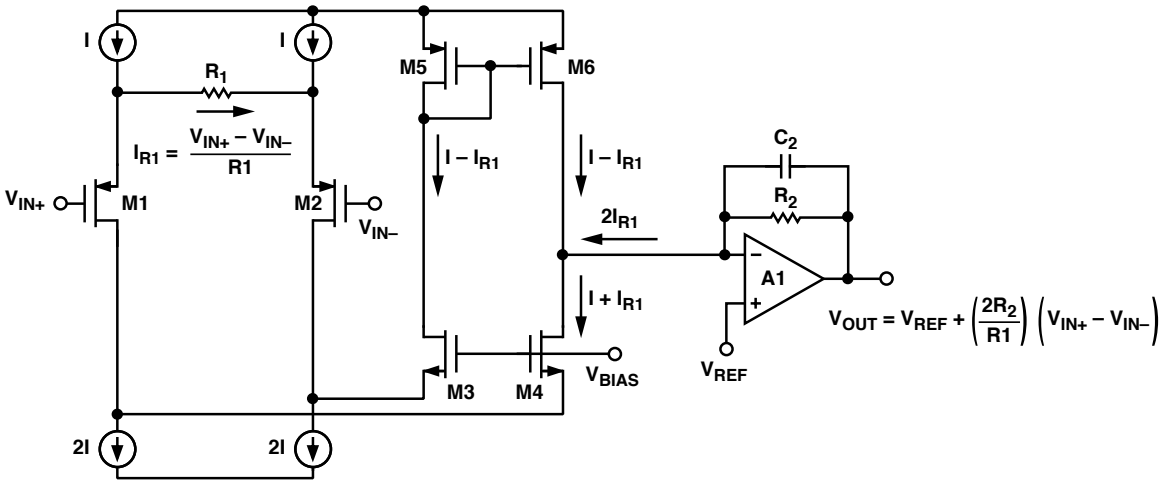



*Figure 3-33. AD8553 simplified schematic.*

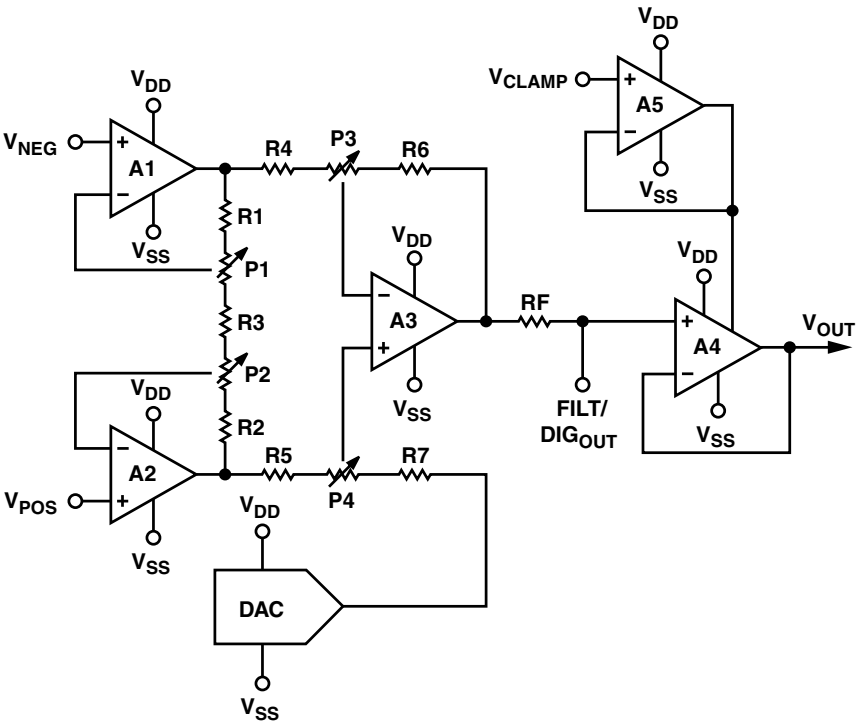



*Figure 3-35. AD8555 simplified schematic.*

A3, R4, R5, R6, R7, P3, and P4 form the second gain stage of the differential amplifier. A3 is also an auto-zeroed op amp that minimizes input offset errors. P3 and P4 are digital potentiometers, allowing the second stage gain to be varied from 17.5 to 200 in eight steps; they allow the gain to be varied over a wide range. R4, R5, R6, R7, P3, and P4 each have a similar temperature coefficient, so the second stage gain temperature coefficient is lower than 100 ppm/°C.

A5 implements a voltage buffer, which provides the positive supply to the amplifier output buffer A4. Its function is to limit $V_{OUT}$ to a maximum value, useful for driving analog-to-digital converters (ADC) operating on supply voltages lower than $V_{DD}$. The input to A5, $V_{CLAMP}$, has a very high input resistance. It should be connected to a known voltage and not left floating. However, the high input impedance allows the clamp voltage to be set using a high impedance source (e.g., a potential divider). If the maximum value of $V_{OUT}$ does not need to be limited, $V_{CLAMP}$ should be connected to $V_{DD}$.

A4 implements a rail-to-rail input and output unity-gain voltage buffer. The output stage of A4 is supplied from a buffered version of $V_{CLAMP}$ instead of $V_{DD}$, allowing the positive swing to be limited. The maximum output current is limited between 5 to 10 mA.

An 8-bit digital-to-analog converter (DAC) is used to generate a variable offset for the amplifier output. This DAC is guaranteed to be monotonic. To preserve the ratiometric nature of the input signal, the DAC references are driven from $V_{SS}$ and $V_{DD}$, and the DAC output can swing from $V_{SS}$ (Code 0) to $V_{DD}$ (Code 255). The 8-bit resolution is equivalent to 0.39% of the difference between $V_{DD}$ and $V_{SS}$ (e.g., 19.5 mV with a 5V supply). The DAC output voltage ($V_{DAC}$) is given approximately by

$$V_{DAC} \approx \left( \frac{Code + 0.5}{256} \right) \left( V_{DD} - V_{SS} \right) + V_{SS}$$

The temperature coefficient of $V_{DAC}$ is lower than 200 ppm/°C.

The amplifier output voltage ($V_{OUT}$) is given by

$$V_{OUT} = GAIN\left(V_{POS} - V_{NEG}\right) + V_{DAC}$$

where GAIN is the product of the first and second stage gains.

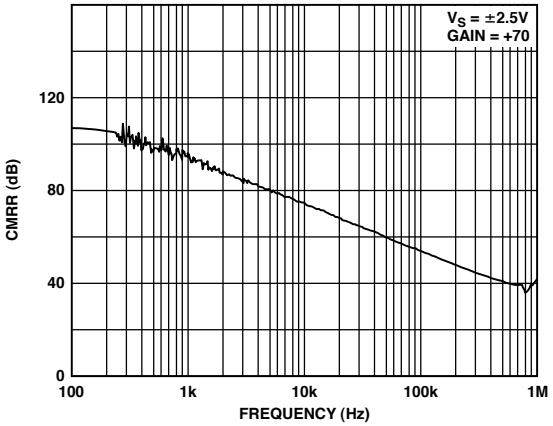



*Figure 3-36. AD8555 CMRR vs. frequency.*

Figures 3-36 and 3-37 show the AD8555's CMRR vs. frequency and its closed-loop gain vs. frequency.

See the AD8555 product data sheet for more details.

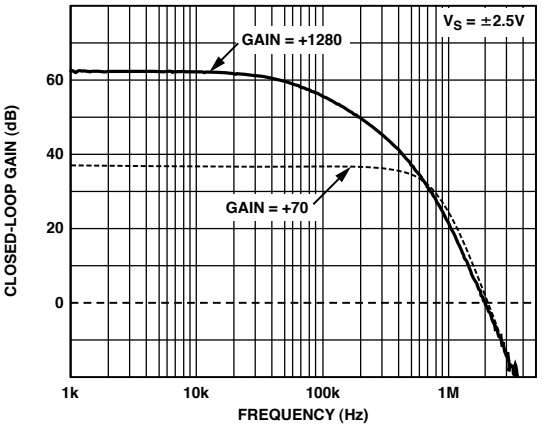



*Figure 3-37. AD8555 closed-loop gain vs. frequency measured at output pin.*

The **AD8556** is essentially the same product as the AD8555, except that the former includes internal RFI filtering. The block diagram for the AD8556 is shown in Figure 3-38. For theory of operation, refer to the previous section that covers the AD8555.

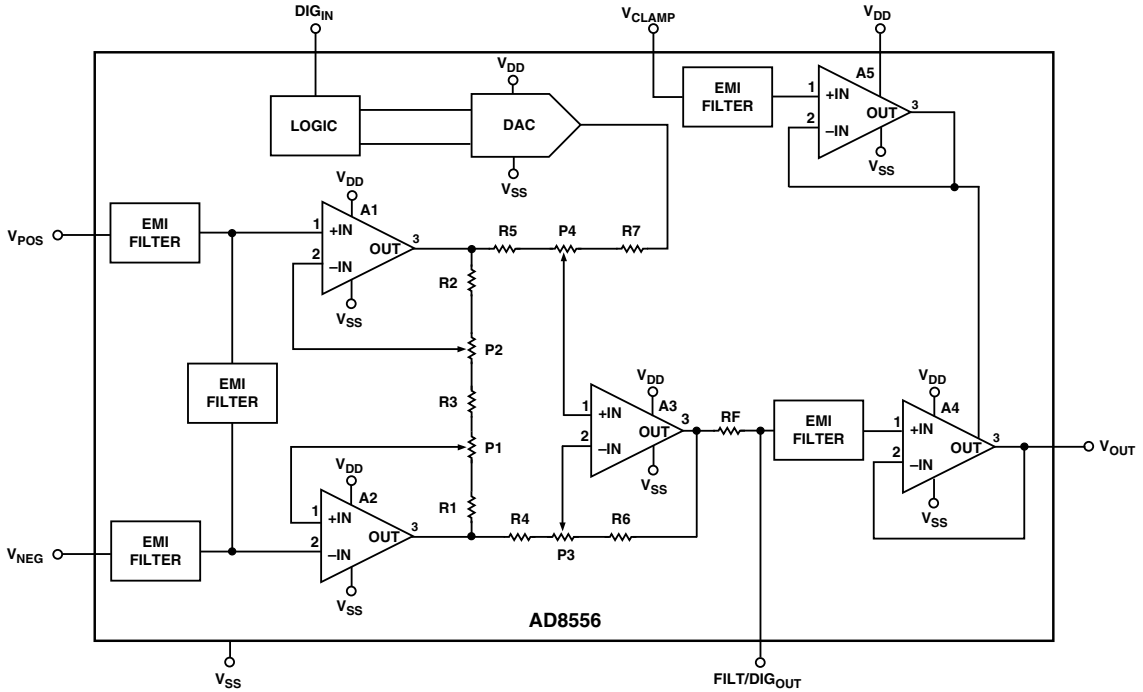



*Figure 3-38. AD8556 block diagram showing EMI/RFI built-in filters.*

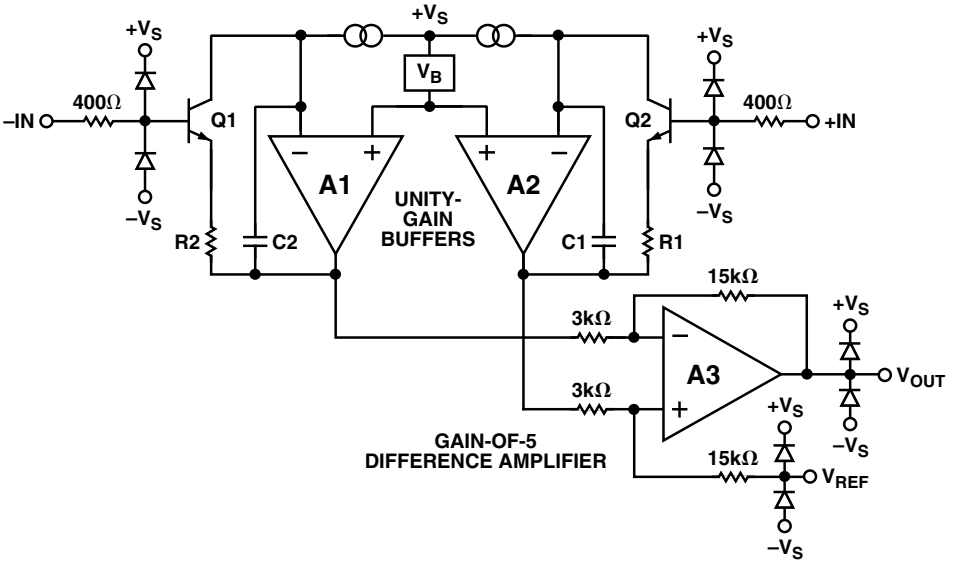



*Figure 3-39. AD8225 simplified schematic.*

**Fixed Gain (Low Drift) In-Amps**

The **AD8225** is a precision, gain-of-5, monolithic in-amp. Figure 3-39 shows that it is a 3-op amp instrumentation amplifier. The unity-gain input buffers consist of superbeta NPN transistors Q1 and Q2 and op amps A1 and A2. These transistors are compensated so that their input bias currents are extremely low, typically 100 pA or less. As a result, current noise is also low, only 50 fA/$\sqrt{\text{Hz}}$. The input buffers drive a gain-of-5 difference amplifier. Because the 3 kΩ and 15 kΩ resistors are ratio matched, gain stability is better than 5 ppm/°C over the rated temperature range.

The AD8225 has a wide gain bandwidth product, resulting from its being compensated for a fixed gain of 5, as opposed to the usual unity-gain compensation of variable gain in-amps. High frequency performance is also enhanced by the innovative pinout of the AD8225. Since Pin 1 and Pin 8 are uncommitted, Pin 1 may be connected to Pin 4. Since Pin 4 is also ac common, the stray capacitance at Pins 2 and 3 is balanced.

Figure 3-40 shows the AD8225's CMR vs. frequency while Figure 3-41 shows its gain nonlinearity.

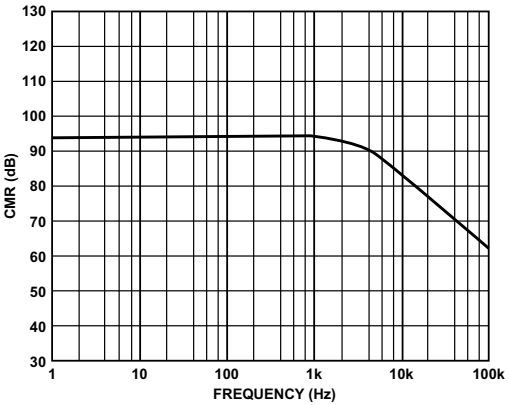



*Figure 3-40. AD8225 CMR vs. frequency.*

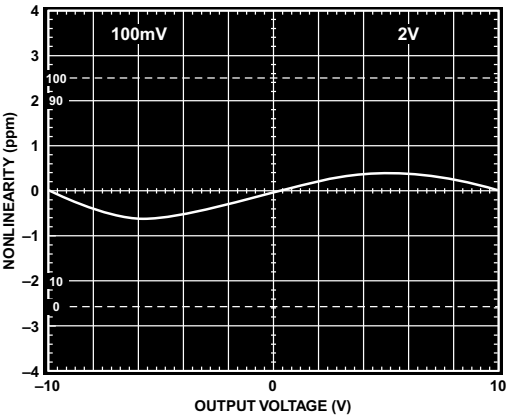



*Figure 3-41. AD8225 gain nonlinearity.*

**Monolithic In-Amps Optimized for Single-Supply Operation**

Single-supply in-amps have special design problems that need to be addressed. The input stage must be able to amplify signals that are at ground potential (or very close to ground), and the output stage needs to be able to swing to within a few millivolts of ground or the supply rail. Low power supply current is also important. And, when operating from low power supply voltages, the in-amp needs to have an adequate gain bandwidth product, low offset voltage drift, and good CMR vs. gain and frequency.

The **AD623** is an instrumentation amplifier based on the 3-op amp in-amp circuit, modified to ensure operation on either single- or dual-power supplies, even at common-mode voltages at, or even below, the negative supply rail (or below *ground* in single-supply operation). Other features include rail-to-rail output voltage swing, low supply current, MSOP packaging, low input and output voltage offset, microvolt/dc offset level drift, high common-mode rejection, and only one external resistor to set the gain.

As shown in Figure 3-42, the input signal is applied to PNP transistors acting as voltage buffers and dc level shifters. A resistor trimmed to within 0.1% of 50 kΩ in each amplifier's (A1 and A2) feedback path ensures accurate gain programmability.

The differential output is

$$\left(V_O = 1 + \frac{100\,\text{k}\Omega}{R_G}\right)V_C$$

where $R_G$ is in kΩ.

The differential voltage is then converted to a single-ended voltage using the output difference amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Since all the amplifiers can swing to either supply rail, as well as have their common-mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced.

Note that the base currents of Q1 and Q2 flow directly *out* of the input terminals, unlike dual-supply, input-current-compensated in-amps such as the AD620. Since the inputs (i.e., the bases of Q1 and Q2) can operate at ground (i.e., 0 V or, more correctly, 200 mV below ground), it is not possible to provide input current compensation for the AD623. However, the input bias current of the AD623 is still very small: only 25 nA max.

The output voltage at Pin 6 is measured with respect to the *reference* potential at Pin 5. The impedance of the reference pin is 100 kΩ. Internal ESD clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand overvoltages of 0.3 V above or below the supplies. This is true for all gains, and with power on or off. This last case is particularly important, since the signal source and the in-amp may be powered separately. If the overvoltage is expected to exceed this value, the current through these diodes should be limited to 10 mA, using external current limiting resistors (see Input Protection Basics for ADI In-Amps section in Chapter 5). The value of these resistors is defined by the in-amp's noise level, the supply voltage, and the required overvoltage protection needed.

The bandwidth of the AD623 is reduced as the gain is increased since A1 and A2 are voltage feedback op amps. However, even at higher gains, the AD623 still has enough bandwidth for many applications.

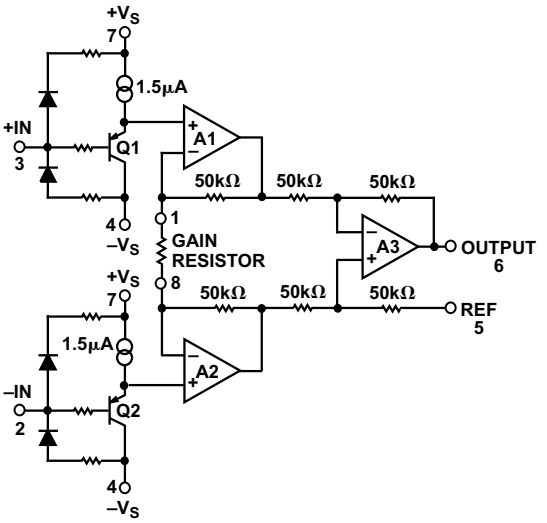



*Figure 3-42. AD623 simplified schematic.*

The AD623's gain is resistor-programmed by $R_G$ or more precisely by whatever impedance appears between Pins 1 and 8. Figure 3-43 shows the gain vs. frequency of the AD623. The AD623 is laser-trimmed to achieve accurate gains using 0.1% to 1% tolerance resistors.

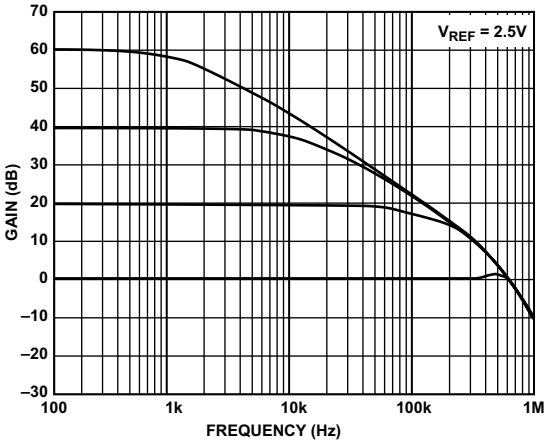



*Figure 3-43. AD623 closed-loop gain vs. frequency.*

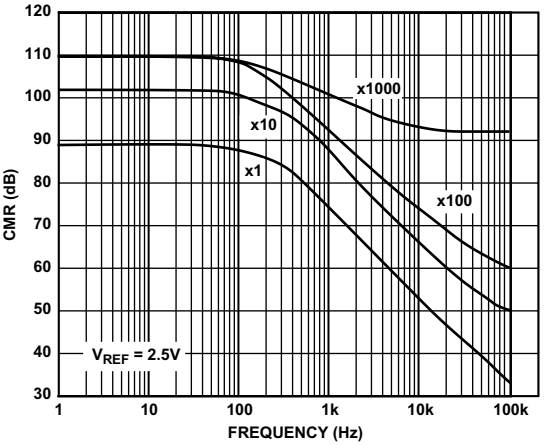



*Figure 3-44. AD623 CMR vs. frequency ($V_S$ = ±5 V).*

**Table 3-3. Required Value of Gain Resistor**

| Desired Gain | 1% Std. Value of $R_G$ (Ω) | Calculated Gain Using 1% Resistors |
|---|---|---|
| 2 | 100 k | 2 |
| 5 | 24.9 k | 5.02 |
| 10 | 11 k | 10.09 |
| 20 | 5.23 k | 20.12 |
| 33 | 3.09 k | 33.36 |
| 40 | 2.55 k | 40.21 |
| 50 | 2.05 k | 49.78 |
| 65 | 1.58 k | 64.29 |
| 100 | 1.02 k | 99.04 |
| 200 | 499 | 201.4 |
| 500 | 200 | 501 |
| 1000 | 100 | 1001 |

Table 3-3 shows required values of $R_G$ for various gains. Note that for G = 1, the $R_G$ terminals are unconnected ($R_G = \infty$). For any arbitrary gain, $R_G$ can be calculated using the formula

$$R_G = 100\ \text{k}\Omega/(G - 1)$$

Figure 3-44 shows the AD623's CMR vs. frequency. Note that the CMR increases with gain up to a gain of 100 and that CMR also remains high over frequency, up to 200 Hz. This ensures the attenuation of power line common-mode signals (and their harmonics).

Figure 3-45 shows the gain nonlinearity of the AD623.

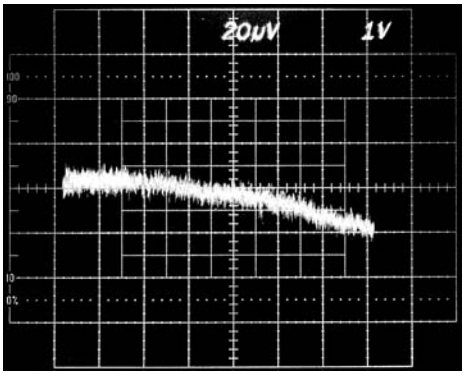



*Figure 3-45. AD623 gain nonlinearity (G = –10, 50 ppm/div).*

Figure 3-46 shows the small signal pulse response of the AD623.

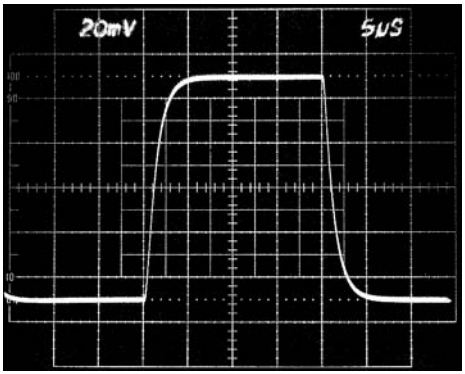



*Figure 3-46. AD623 small signal pulse response (G = 10, $R_L$ = 10 kΩ, $C_L$ = 100 pF).*

**Low Power, Single-Supply In-Amps**

The **AD627** is a single-supply, micropower instrumentation amplifier that can be configured for gains between 5 and 1000 using just a single external resistor. It provides a rail-to-rail output voltage swing using a single 3 V to 30 V power supply. With a quiescent supply current of only 60 μA (typical), its total power consumption is less than 180 μW, operating from a 3 V supply.

Figure 3-47 is a simplified schematic of the AD627. The AD627 is a true instrumentation amplifier built using two feedback loops. Its general properties are similar to those of the classic 2-op amp instrumentation amplifier configuration and can be regarded as such, but internally the details are somewhat different. The AD627 uses a modified current feedback scheme, which, coupled with interstage feedforward frequency compensation, results in a much better CMRR at frequencies above dc (notably the line frequency of 50 Hz to 60 Hz) than might otherwise be expected of a low power instrumentation amplifier.

As shown in Figure 3-47, A1 completes a feedback loop, which, in conjunction with V1 and R5, forces a constant collector current in Q1. Assume for the moment that the gain-setting resistor ($R_G$) is not present. Resistors R2 and R1 complete the loop and force the output of A1 to be equal to the voltage on the inverting terminal with a gain of (almost exactly) 1.25. A nearly identical feedback loop completed by A2 forces a current in Q2, which is substantially identical to that in Q1, and A2 also provides the output voltage. When both loops are balanced, the gain from the noninverting terminal to $V_{OUT}$ is equal to 5, whereas the gain from the output of A1 to $V_{OUT}$ is equal to –4. The inverting terminal gain of A1 (1.25), times the gain of A2 (–4), makes the gain from the inverting and noninverting terminals equal.

The differential mode gain is equal to 1 + R4/R3, nominally 5, and is factory trimmed to 0.01% final accuracy (AD627B typ). Adding an external gain setting resistor ($R_G$) increases the gain by an amount equal to (R4 + R1)/$R_G$. The gain of the AD627 is given by the following equation:

$$G = 5 + \left( \frac{200\,\text{k}\Omega}{R_G} \right)$$

Laser trims are performed on resistors R1 through R4 to ensure that their values are as close as possible to the absolute values in the gain equation. This ensures low gain error and high common-mode rejection at all practical gains.

Figure 3-48 shows the AD627's CMR vs. frequency.

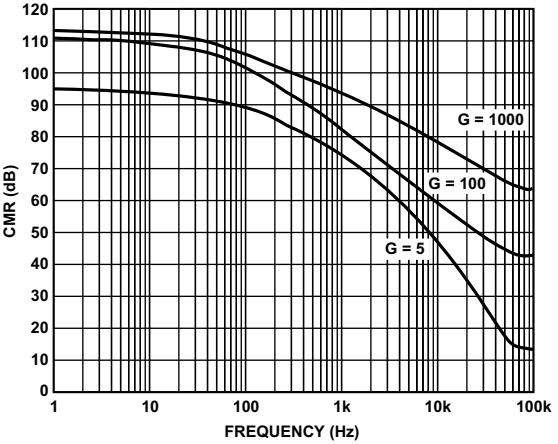



*Figure 3-48. AD627 CMR vs. frequency.*

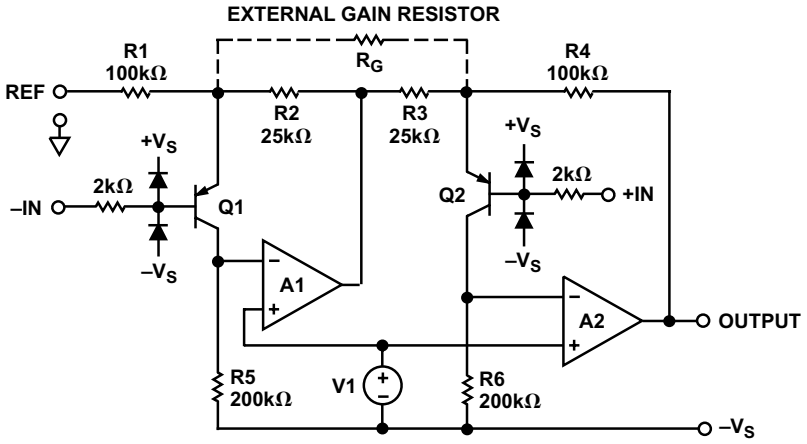



*Figure 3-47. AD627 simplified schematic.*

Figures 3-49 and 3-50 show the AD627's gain vs. frequency and gain nonlinearity.

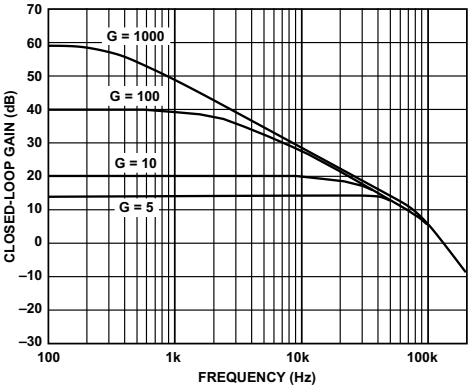



*Figure 3-49. AD627 closed-loop gain vs. frequency.*

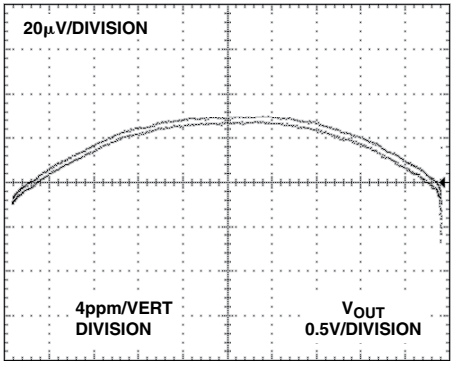



*Figure 3-50. AD627 gain nonlinearity ($V_S$ = ±2.5 V, G = 5, 4 ppm/vertical division).*

The AD627 also has excellent dynamic response, as shown in Figure 3-51.

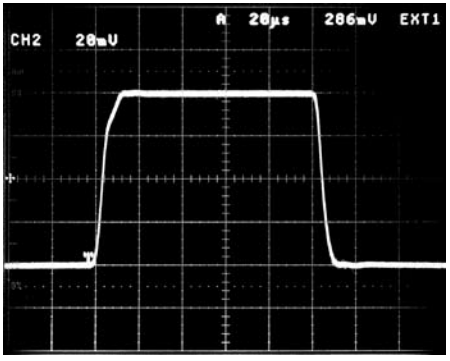



*Figure 3-51. Small signal pulse response of the AD627 ($V_S$ = ±5 V, G = +10, $R_L$ = 20 kΩ, $C_L$ = 50 pF, 20 μs/horizontal division, 20 mV/vertical division).*

**Gain-Programmable In-Amps**

The **AD8250** and **AD8251** (Figure 3-52) are digitally gain-programmable instrumentation amplifiers that have high (GΩ) input impedances and low distortion, making them suitable for sensor interfacing and driving high sample rate analog-to-digital converters. The two products are nearly identical, except for their gain ranges. The AD8250 has programmable gains of 1, 2, 5, and 10, while the AD8251 has a range of 1, 2, 4, and 8 (for binary applications). Both products have high bandwidths of 10 MHz, low distortion, and a settling time of 0.5 μs to 0.01%. Input offset drift and gain drift are only 1 μV/°C and 10 ppm/°C, respectively. In addition to their wide input common-voltage range, they boast a high common-mode rejection of 80 dB at G = 1 from dc to 100 kHz. The combination of precision dc performance coupled with high speed capabilities makes the AD8250 and AD8251 excellent candidates for data acquisition and medical applications. Furthermore, these monolithic solutions simplify design and manufacturing, while boosting their performance, by maintaining a tight match of internal resistors and amplifiers.

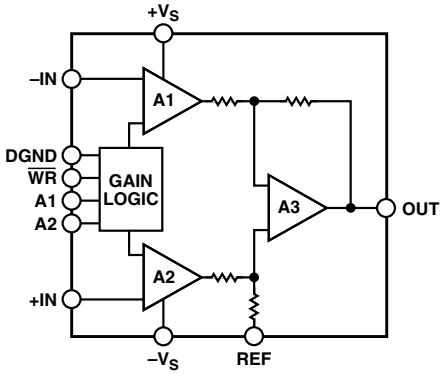



*Figure 3-52. AD8250 and AD8251 simplified schematic.*

The AD8250 and AD8251 user interfaces are comprised of a parallel port that allows users to set the gain in one of three different ways (Figure 3-52). A 2-bit word sent to A1 and A2 via a bus may be latched using the CLK input. An alternative is to set the gain within 1 μs by using the gain port in transparent mode. The last method is to strap A1 and A2 to a high or low voltage potential, permanently setting the gain.

The AD8250 and AD8251 are available in a 10-lead MSOP package and are specified over the –40°C to +125°C temperature range, making them an excellent solution for applications where size and packing density are important considerations. To simplify matters, their pinout was chosen to optimize layout and increase ac performance.

# Chapter IV

# MONOLITHIC DIFFERENCE AMPLIFIERS

**Difference (Subtractor) Amplifier Products**

Monolithic difference amplifiers are a special category of in-amps that are usually designed to be used in applications where large dc or ac common-mode voltages are present. This includes many general current sensing applications, such as motor control, battery chargers, and power converters. In addition, there are numerous high common-mode voltage automotive current sensing applications, including: battery cell voltage monitoring, transmission controls, fuel injection controls, engine management, suspension controls, electronic steering, electronic parking brake, and hybrid vehicle drive/hybrid battery control. Because these amplifiers are typically used to sense current by accurately amplifying the small differential voltage across a shunt resistor in the load path, they are often called current shunt amplifiers.

The **AD8200 family** of current shunt amplifiers is based on a traditional difference amplifier input stage which includes a resistor-divider configuration. These on-chip precision resistors provide matching to within 0.01%, which results in very good total error when compared with a difference amplifier built from discrete op amps and resistors. Unlike the AD8200 amplifiers, which can withstand high common-mode input voltages by dividing these voltages down at the input, the **AD8210** amplifiers tolerate the high common-mode input voltages by virtue of the high breakdown voltages of their input transistors. This provides numerous advantages over the AD8200 series amplifiers, including higher bandwidth, higher input impedance, and lower overall noise amplification. Combined, these advantages reduce total system error.

Table 4-1 provides a performance summary of Analog Devices difference amplifier products.

**Table 4-1. Latest Generation of Analog Devices Difference Amps Summarized[1]**

| Product | Features | Power Supply Current Typ | –3 dB BW Typ (G = 10) | CMR G = 10 (dB) Min | Input Offset Voltage Max | $V_{OS}$ Drift (µV/°C) Max | RTI Noise[2] (nV/√Hz) (G = 10) |
|---|---|---|---|---|---|---|---|
| AD8202 | S.S., 28 V CMV, G = 20 | 250 µA | 50 kHz | 80[3, 4, 5] | 1 mV[6] | 10 | 300 typ[3] |
| AD8203 | S.S., 28 V CMV, G = 14 | 250 µA | 60 kHz[7] | 80[5, 7] | 1 mV[6] | 10 | 300 typ[7] |
| AD8205 | S.S., 65 V CMV, G = 50 | 1 mA | 50 kHz[8] | 80[4, 5, 6] | 2 mV[6] | 15 typ | 500 typ[8] |
| AD8206 | S.S., 65 V CMV, G = 20 | 1 mA | 100 kHz[3] | 76[3, 9] | 2 mV[6] | 15 typ | 500 typ[3] |
| AD8210 | S.S., current shunt monitor | 500 µA | 500 kHz[3] | 100[3, 5] | 1 mV[6] | 5 typ | 80 typ[3] |
| AD8212 | Adjustable gain; CMV up to 500 V[10] | 200 µA | 500 kHz | 90 | 1 mV | 10 | 100 typ |
| AD8213 | Dual channel | 1.3 mA[11] | 500 kHz | 100 | 1 mV | 10 | 70 typ |
| AD8130 | 270 MHz receiver | 12 mA | 270 MHz | 83[12, 13] | 1.8 mV | 3.5 mV | 12.5 typ[12, 14] |
| AD628 | High CMV | 1.6 mA | 600 kHz[15] | 75[15] | 1.5 mV | 4 | 300 typ[15] |
| AD629 | High CMV, G = 1 | 0.9 mA | 500 kHz | 77[12] | 1 mV | 6 | 550 typ[12] |
| AD626 | High CMV | 1.5 mA | 100 kHz | 55[16] | 500 µV | 1 | 250 typ |
| AMP03 | High BW, G = 1 | 3.5 mA | 3 MHz | 85[12] | 400 µV | NS | 750 typ[12] |

NOTES
NS = not specified, NA = not applicable, S.S. = single supply.
[1]Refer to ADI website at www.analog.com for latest products and specifications.
[2]At 1 kHz. RTI noise = $\sqrt{(e_{ni})^2 + (e_{no}/G)^2}$.
[3]Operating at a gain of 20.
[4]For 10 kHz, <2 kΩ source imbalance.
[5]DC to 10 kHz.
[6]Referred to input (RTI).
[7]Operating at a gain of 14.
[8]Operating at a gain of 50.
[9]DC to 20 kHz.
[10]With inexpensive external transistor.
[11]Note that this is 0.65 mA per channel.
[12]Operating at a gain of 1.
[13]At frequency = 4 MHz.
[14]At frequency ≥ 10 kHz.
[15]Operating at a gain of 0.1.
[16]f = 10 kHz, $V_{CM}$ = 6 V.

The AD8200 family of current sensing difference amplifiers has multiple gain options, which provide design flexibility for the following important trade-offs:

1.) The shunt resistance value vs. the power dissipated in the circuit being measured

2.) The shunt resistance value vs. the signal-to-noise ratio

3.) The shunt resistance value vs. the amplifier gain needed

The automotive industry standard calls for a gain of 20, which, in most cases, gives an excellent trade-off between all three variables. However, there are conditions which favor other gains. For example, the AD8203 operates at a gain of 14. This allows for convenient scaling of the output to accommodate both 5 V and 3.3 V A/D converters, while still using the same value resistive shunt.

Similarly, the **AD8205** has a gain of 50, for use in applications where it is most important to minimize the power dissipation in the resistive shunt. This higher gain is used with lower resistance shunts, which, of course, have a lower output voltage. This slightly reduces the signal-to-noise performance of the system.

The **AD8202** consists of a preamp and buffer arranged as shown in Figure 4-1.

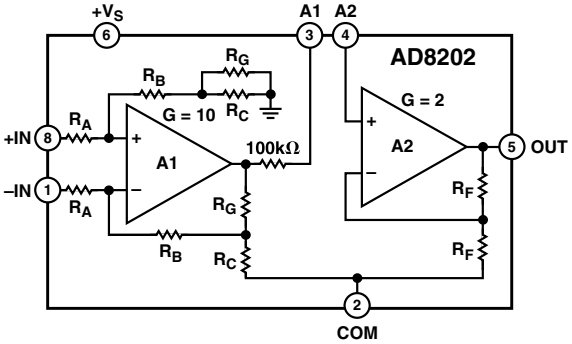



*Figure 4-1. AD8202 connection diagram.*

Figure 4-2 provides more details. The preamp incorporates a dynamic bridge (subtractor) circuit. Identical networks (within the shaded areas) consisting of $R_A$, $R_B$, $R_C$, and $R_G$ attenuate input signals applied to Pins 1 and 8. Note that when equal amplitude signals are asserted at inputs 1 and 8, and the output of A1 is equal to the common potential (i.e., zero), the two attenuators form a balanced-bridge network. When the bridge is balanced, the differential input voltage at A1, and thus its output, will be zero.

Any common-mode voltage applied to both inputs will keep the bridge balanced and the A1 output at zero. Because the resistor networks are carefully matched, the common-mode signal rejection approaches this ideal state. However, if the signals applied to the inputs differ, the result is a difference at the input to A1. A1 responds by adjusting its output to drive $R_B$, by way of $R_G$, to adjust the voltage at its inverting input until it matches the voltage at its noninverting input.

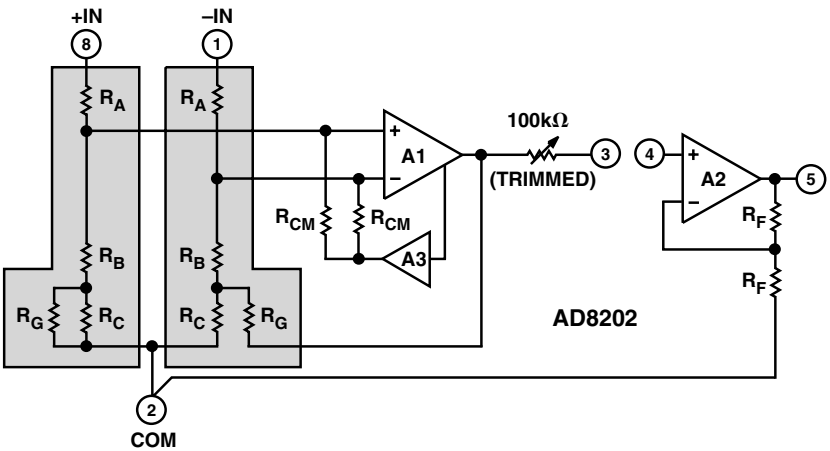



*Figure 4-2. AD8202 simplified schematic.*

By attenuating voltages at Pins 1 and 8, the amplifier inputs are held within the power supply range, even if the input levels of Pins 1 and 8 exceed the supply or fall below common (ground). The input network also attenuates normal (differential) mode voltages. $R_C$ and $R_G$ form an attenuator that scales A1 feedback, forcing large output signals to balance relatively small differential inputs. The resistor ratios establish the preamp gain at 10.

Because the differential input signal is attenuated and then amplified to yield an overall gain of 10, the amplifier A1 operates at a higher noise gain, multiplying deficiencies such as input offset voltage and noise with respect to Pins 1 and 8.

To minimize these errors while extending the common-mode range, a dedicated feedback loop is employed to reduce the range of common-mode voltage applied to A1 for a given overall range at the inputs. By offsetting the range of voltage applied to the compensator, the input common-mode range is also offset to include voltages more negative than the power supply. Amplifier A3 detects the common-mode signal applied to A1 and adjusts the voltage on the matched $R_{CM}$ resistors to reduce the common-mode voltage range at the A1 inputs. By adjusting the common voltage of these resistors, the common-mode input range is extended while the normal mode signal attenuation is reduced, leading to better performance referred to input.

The output of the dynamic bridge taken from A1 is connected to Pin 3 by way of a 100 kΩ series resistor, provided for low-pass filtering and gain adjustment. The resistors in the input networks of the preamp and the buffer feedback resistors are ratio-trimmed for high accuracy.

The output of the preamp drives a gain-of-2 buffer amplifier, A2, implemented with carefully matched feedback resistors, $R_F$.

The two-stage system architecture of the AD8202 (Figure 4-2) enables the user to incorporate a low-pass filter prior to the output buffer. By separating the gain into two stages, a full-scale, rail-to-rail signal from the preamp can be filtered at Pin 3, and a half-scale signal resulting from filtering can be restored to full scale by the output buffer amp. The source resistance seen by the inverting input of A2 is approximately 100 kΩ, to minimize the effects of A2's input bias current. Typically, this current is quite small, and errors resulting from applications that mismatch the resistance are correspondingly small. The simplified schematic and theory of operation given for the AD8202 also applies to the **AD8203**. The two products are almost identical, except for their internal preset gains and their power consumption.

**AD8205 Difference Amplifier**

The **AD8205** is a single-supply difference amplifier that uses a unique architecture to accurately amplify small differential current shunt voltages in the presence of rapidly changing common-mode voltages. It is offered in both packaged and die form.

In typical applications, the AD8205 is used to measure current by amplifying the voltage across a current shunt placed across the inputs.

The gain of the AD8205 is 50 V/V, with an accuracy of 1.2%. This accuracy is guaranteed over the operating temperature range of –40°C to +125°C. The die temperature range is –40°C to +150°C with a guaranteed gain accuracy of 1.3%.

The input offset is less than 2 mV referred to the input at 25°C, and 4.5 mV maximum referred to the input over the full operating temperature range for the packaged part. The die input offset is less than 6 mV referred to the input over the die operating temperature range.

The AD8205 operates with a single supply from 4.5 V to 10 V (absolute maximum = 12.5 V). The supply current is less than 2 mA.

High accuracy trimming of the internal resistors allows the AD8205 to have a common-mode rejection ratio better than 78 dB from dc to 20 kHz. The common-mode rejection ratio over the operating temperature is 76 dB for both the die and the packaged part.

The output offset can be adjusted from 0.05 V to 4.8 V (V+ = 5 V) for unipolar and bipolar operation.

The AD8205 consists of two amplifiers (A1 and A2), a resistor network, a small voltage reference, and a bias circuit (not shown). See Figure 4-3.

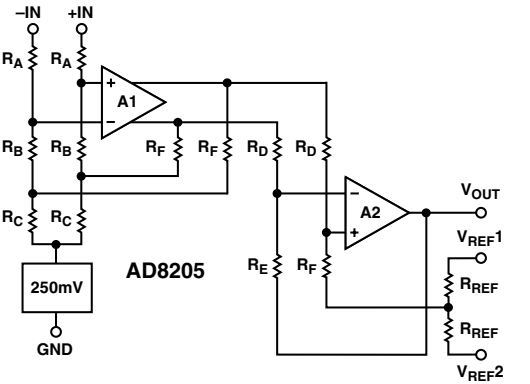



*Figure 4-3. AD8205 simplified schematic.*

The set of input attenuators preceding A1 consists of $R_A$, $R_B$, and $R_C$, which reduces the common-mode voltage to match the input voltage range of A1. The two attenuators form a balanced-bridge network. When the bridge is balanced, the differential voltage created by a common-mode voltage is 0 V at the inputs of A1. The input attenuation ratio is 1/16.7. The combined series resistance of $R_A$, $R_B$, and $R_C$ is approximately 200 kΩ ± 20%.

By attenuating the voltages at Pin 1 and Pin 8, the A1 amplifier inputs are held within the power supply range, even if Pin 1 and Pin 8 exceed the supply or fall below common (ground). A reference voltage of 250 mV biases the attenuator above ground. This allows the amplifier to operate in the presence of negative common-mode voltages.

The input network also attenuates normal (differential) mode voltages. A1 amplifies the attenuated signal by 26. The input and output of this amplifier are differential to maximize the ac common-mode rejection.

A2 converts the differential voltage from A1 into a single-ended signal and provides further amplification. The gain of this second stage is 32.15.

The reference inputs, $V_{REF}1$ and $V_{REF}2$, are tied through resistors to the positive input of A2, which allows the output offset to be adjusted anywhere in the output operating range. The gain is 1 V/V from the reference pins to the output when the reference pins are used in parallel. The gain is 0.5 V/V when they are used to divide the supply.

The ratios of Resistors $R_A$, $R_B$, $R_C$, $R_D$, and $R_F$ are trimmed to a high level of precision to allow the common-mode rejection ratio to exceed 80 dB. This is accomplished by laser trimming the resistor ratio matching to better than 0.01%.

The total gain of 50 is made up of the input attenuation of 1/16.7 multiplied by the first stage gain of 26 and the second stage gain of 32.15.

The output stage is Class A with a PNP pull-up transistor and a 300 μA current sink pull-down.

The **AD8206** is nearly identical to the AD8205, except for gain and power consumption. Please see the AD8205 circuit description for AD8206 theory of operation.

The **AD8210** is a current shunt monitor IC. Figure 4-4 shows the block diagram.

The gain of the AD8210 is 20 V/V, with an accuracy of 0.7%. This accuracy is guaranteed over the operating temperature range of –40°C to +125°C.

The AD8210 operates with a single supply between 4.5 V to 5.5 V. The supply current is typically less than 2 mA.

The AD8210 is comprised of two main blocks: a differential amplifier and an instrumentation amplifier. A load current flowing through the external shunt resistor produces a voltage at the input terminals. The input terminals are connected to the differential amplifier (A1) by Resistors R1 and R2. A1 nulls the voltage appearing across its own input terminals by adjusting (balancing) the current through R1 and R2 with Transistors Q1 and Q2. When the input signal to the AD8210 is zero, the currents in R1 and R2 are equal. When the differential signal is nonzero, the current increases through one of the resistors and decreases in the other. The current difference is proportional to the size and polarity of the input signal. Since the differential input voltage is converted into a current, common-mode rejection is not dependent on resistor matching; therefore, both high accuracy and performance are provided throughout the wide common-mode voltage range.

The differential currents through QI and Q2 are converted into a differential voltage due to R3 and R4. A2 is configured as an instrumentation amplifier, and this differential input signal is converted into a single-ended output voltage by A2. The gain is internally set with thin-film resistors to 20 V/V.

The output reference voltage is easily programmed by the $V_{REF}1$ and $V_{REF}2$ pins. In a typical configuration, $V_{REF}1$ is connected to $V_{CC}$ while $V_{REF}2$ is connected to GND. In this case, the output is centered at $V_{CC}/2$ when the input signal is zero.

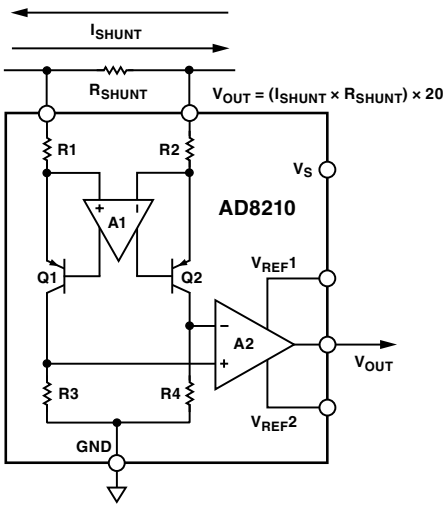



*Figure 4-4. AD8210 block diagram.*

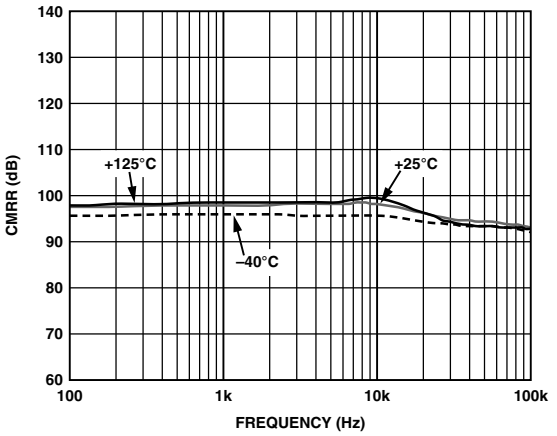



*Figure 4-5. AD8210 CMRR vs. frequency and temperature (common-mode voltage < 5 V).*

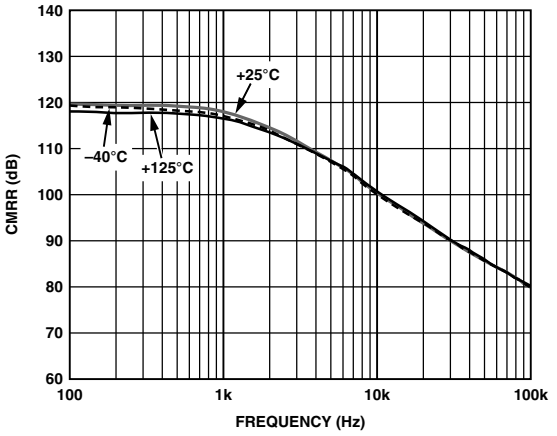



*Figure 4-6. AD8210 CMRR vs. frequency and temperature (common-mode voltage > 5 V).*

The **AMP03** is a monolithic, unity-gain, 3 MHz differential amplifier. Incorporating a matched thin-film resistor network, the AMP03 features stable operation over temperature without requiring expensive external matched components. The AMP03 is a basic analog building block for differential amplifier and instrumentation applications (Figure 4-7).

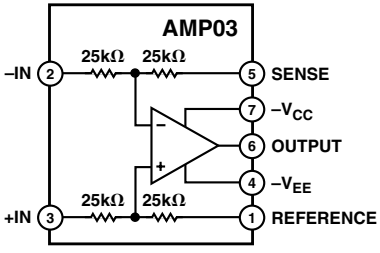



*Figure 4-7. AMP03 functional block diagram.*

The differential amplifier topology of the AMP03 serves both to amplify the difference between two signals and to provide extremely high rejection of the common-mode input voltage. With a typical common-mode rejection of 100 dB, the AMP03 solves common problems encountered in instrumentation design. It is ideal for performing either the addition or subtraction of two input signals without using expensive externally matched precision resistors. Because of its high CMRR over frequency, the AMP03 is an ideal general-purpose amplifier for data acquisition systems that must operate in a noisy environment. Figures 4-8 and 4-9 show the AMP03's CMRR and closed-loop gain vs. frequency.

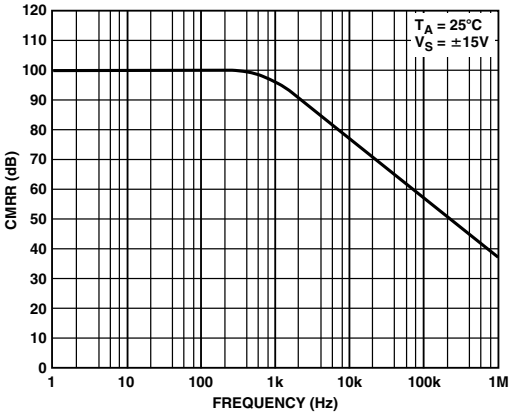



*Figure 4-8. AMP03 CMRR vs. frequency.*

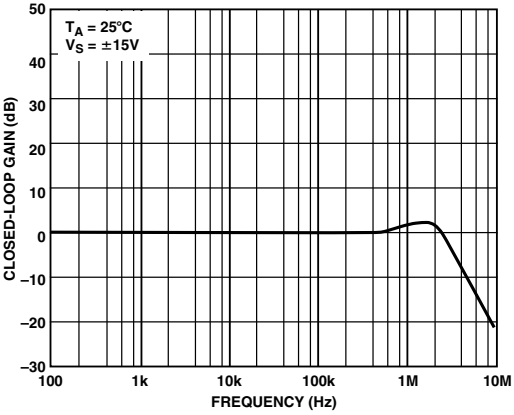



*Figure 4-9. AMP03 closed-loop gain vs. frequency.*

Figure 4-10 shows the small signal pulse response of the AMP03.

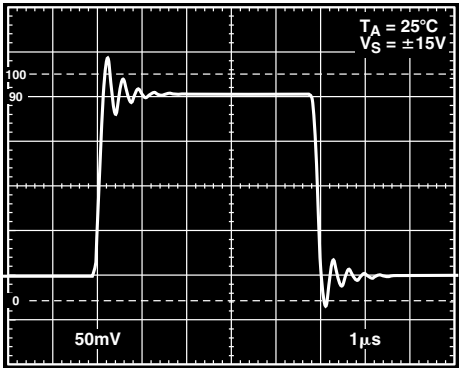



*Figure 4-10. AMP03 small signal pulse response.*

The **AD628** is a high common-mode voltage difference amplifier, combined with a user-configurable output amplifier (see Figure 4-11 and Figure 4-12). Differential mode voltages in excess of 120V are accurately scaled by a precision 11:1 voltage divider at the input. A reference voltage input is available to the user at Pin 3 ($V_{REF}$). The output common-mode voltage of the difference amplifier is the same as the voltage applied to the reference pin. If the uncommitted amplifier is configured for gain, connecting Pin 3 to one end of the external gain resistor establishes the output common-mode voltage at Pin 5 (OUT).

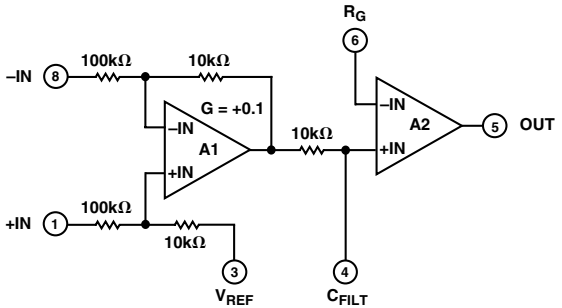



*Figure 4-11. AD628 simplified schematic.*

The output of the difference amplifier is internally connected to a 10 kΩ resistor trimmed to better than ±0.1% absolute accuracy. The resistor is connected to the noninverting input of the output amplifier and is accessible to the user at Pin 4 ($C_{FILT}$). A capacitor can be connected to implement a low-pass filter, a resistor can be connected to further reduce the output voltage, or a clamp circuit can be connected to limit the output swing.

The uncommitted amplifier is a high open-loop gain, low offset, low drift op amp, with its noninverting input connected to the internal 10 kΩ resistor. Both inputs are accessible to the user.

Careful layout design has resulted in exceptional common-mode rejection at higher frequencies. The inputs are connected to Pin 1 (+IN) and Pin 8 (–IN), which are adjacent to the power pins, Pin 2 ($-V_S$) and Pin 7 ($+V_S$). Because the power pins are at ac ground, input impedance balance and, therefore, common-mode rejection are preserved at higher frequencies.

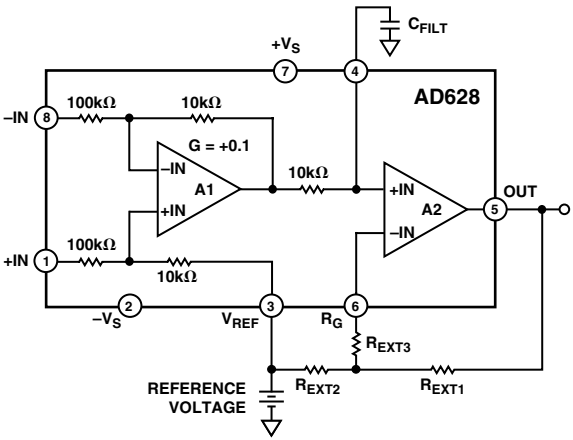



*Figure 4-12. AD628 circuit connections.*

**Gain Adjustment**

The AD628 system gain is provided by an architecture consisting of two amplifiers. The gain of the input stage is fixed at 0.1; the output buffer is user-adjustable as $G_{A2} = 1 + R_{EXT1}/R_{EXT2}$.

$$G_{TOTAL} = 0.1 \times \left(1 + \frac{R_{EXT1}}{R_{EXT2}}\right)$$

At 2 nA maximum, the input bias current of the buffer amplifier is very low, and any offset voltage induced at the buffer amplifier by its bias current may normally be neglected (2 nA × 10 kΩ = 20 µV). However, to absolutely minimize bias current effects, $R_{EXT1}$ and $R_{EXT2}$ can be selected so that their parallel combination is 10 kΩ. If practical resistor values force the parallel combination of $R_{EXT1}$ and $R_{EXT2}$ below 10 kΩ, a series resistor ($R_{EXT3}$) can be added to make up for the difference. Table 4-2 lists several values of gain and corresponding resistor values.

**Table 4-2. Nearest Standard 1% Resistor Values for Various Gains (See Figure 4-12)**

| Total Gain (V/V) | A2 Gain (V/V) | $R_{EXT1}$ (Ω) | $R_{EXT2}$ (Ω) | $R_{EXT3}$ (Ω) |
|---|---|---|---|---|
| 0.1 | 1 | 10 k | ∞ | 0 |
| 0.2 | 2 | 20 k | 20 k | 0 |
| 0.25 | 2.5 | 25.9 k | 18.7 k | 0 |
| 0.5 | 5 | 49.9 k | 12.4 k | 0 |
| 1 | 10 | 100 k | 11 k | 0 |
| 2 | 20 | 200 k | 10.5 k | 0 |
| 5 | 50 | 499 k | 10.2 k | 0 |
| 10 | 100 | 1 M | 10.2 k | 0 |

To set the system gain to less than 0.1, an attenuator can be created by placing a resistor, $R_{EXT4}$, from Pin 4 ($C_{FILT}$) to the reference voltage. A divider would be formed by the 10 kΩ resistor, which is in series with the positive input of A2 and $R_{EXT4}$. A2 would be configured for unity gain.

Using a divider and setting A2 to unity gain yields

$$G_{W/DIVIDER} = 0.1 \times \left( \frac{R_{EXT4}}{10\,k\Omega + R_{EXT4}} \right) \times 1$$

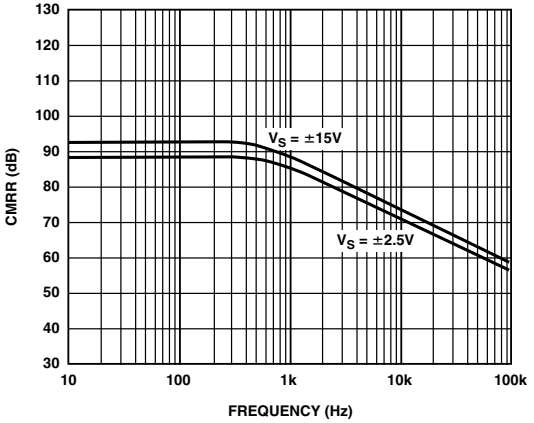



*Figure 4-13. AD628 CMRR vs. frequency.*

For extensive coverage of AD628 applications circuits, refer to Chapter 6 of this guide.

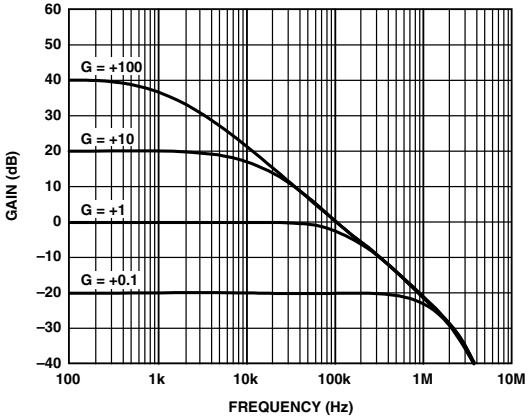



*Figure 4-14. AD628 small signal frequency response, $V_{OUT}$ = 200 mV p-p, G = +0.1, +1, +10, and +100.*

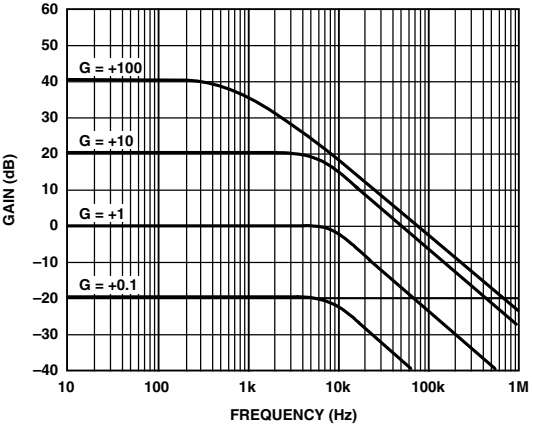



*Figure 4-15. AD628 large signal frequency response, $V_{OUT}$ = 20 V p-p, G = +0.1, +1, +10, and +100.*

The **AD626** is a single- or dual-supply differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (much greater than the supply voltage) without the use of any other active components.

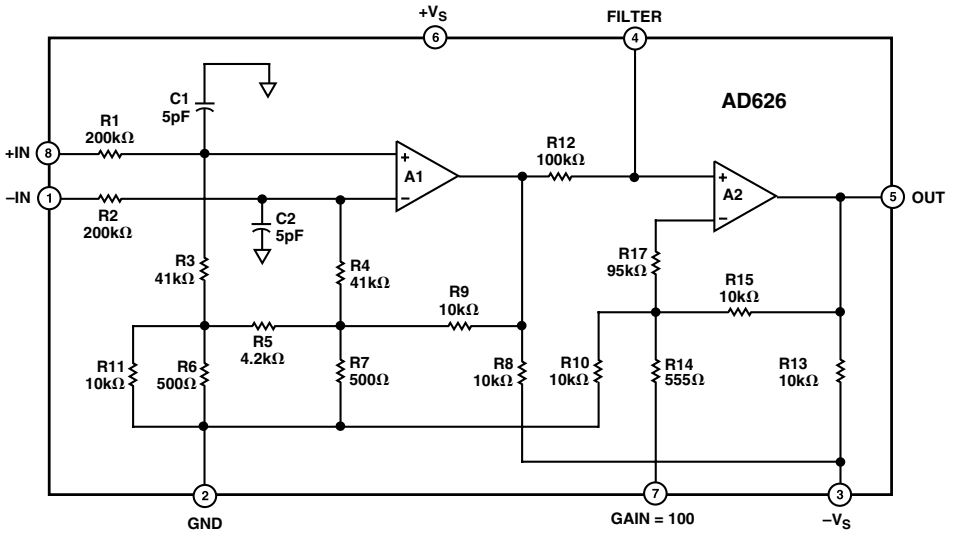



*Figure 4-16. AD626 simplified schematic.*

Figure 4-16 shows the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators, R1 through R4, whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages—six times greater than that which can be tolerated by the actual input to A1. As a result, the input common-mode range extends to six times the quantity ($V_S - 1V$). The overall common-mode error is minimized by precise laser trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio of at least 10,000:1 (80 dB). The output of A1 is connected to the input of A2 via 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest. The AD626 is easily configured for gains of 10 or 100. For a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded. Gains between 10 and 100 are easily set by connecting a resistor between Pin 7 and analog GND. Because the on-chip resistors have an absolute tolerance of ±20% (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The nominal value for this gain setting resistor is equal to

$$R = \left(\frac{50{,}000\ \Omega}{GAIN - 10}\right) - 555\ \Omega$$

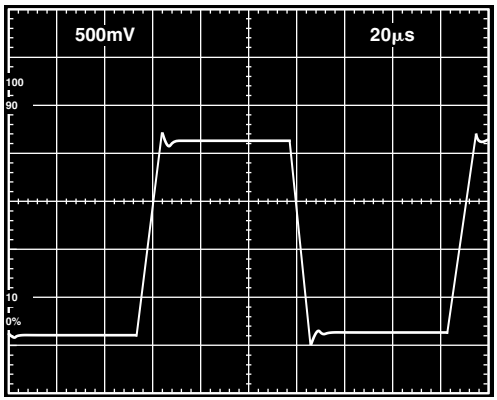



*Figure 4-17. The large signal pulse response of the AD626. G = 10.*

Figure 4-17 shows the large signal pulse response of the AD626.

The **AD629** is a unity-gain difference amplifier designed for applications that require the measurement of signals with common-mode input voltages of up to ±270 V. The AD629 keeps error to a minimum by providing excellent CMR in the presence of high common-mode input voltages. Finally, it can operate from a wide power supply range of ±2.5 V to ±18 V.

The AD629 can replace costly isolation amplifiers in applications that do not require galvanic isolation. Figure 4-18 is the connection diagram of the AD629. Figure 4-19 shows the AD629's CMR vs. frequency.

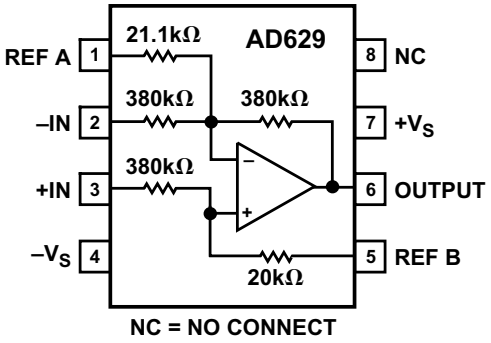



*Figure 4-18. AD629 connection diagram.*

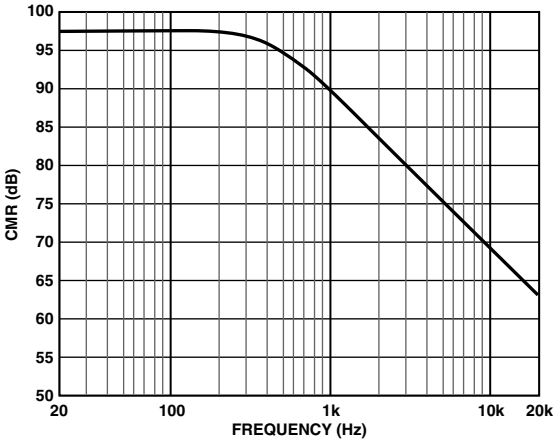



*Figure 4-19 AD629 common-mode rejection vs. frequency.*

**High Frequency Differential Receiver/Amplifiers**

Although not normally associated with difference amplifiers, the **AD8130** series of very high speed differential receiver/amplifiers represent a new class of products that provide effective common-mode rejection at VHF frequencies. The AD8130 has a –3 dB bandwidth of 270 MHz, an 80 dB CMR at 2 MHz, and a 70 dB CMR at 10 MHz.

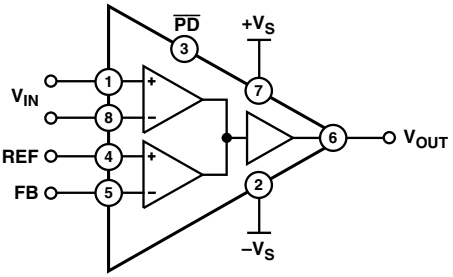



*Figure 4-20. AD8130 block diagram.*

Figure 4-20 is a block diagram of the AD8130. Its design uses an architecture called active feedback, which differs from that of conventional op amps. The most obvious differentiating feature is the presence of two separate pairs of differential inputs compared to a conventional op amp's single pair. Typically for the active feedback architecture, one of these input pairs is driven by a differential input signal, while the other is used for the feedback. This active stage in the feedback path is where the term *active feedback* is derived. The active feedback architecture offers several advantages over a conventional op amp in several types of applications. Among these are excellent common-mode rejection, wide input common-mode range, and a pair of inputs that are high impedance and totally balanced in a typical application.

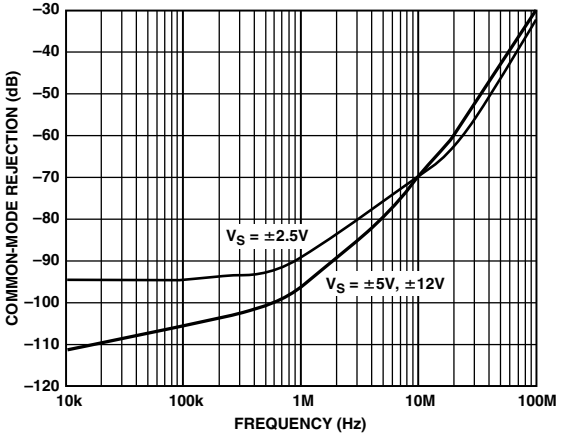



*Figure 4-21. AD8130 CMR vs. frequency.*

In addition, while an external feedback network establishes the gain response as in a conventional op amp, its separate path makes it totally independent of the signal input. This eliminates any interaction between the feedback and input circuits, which traditionally causes problems with CMRR in conventional differential-input op amp circuits.

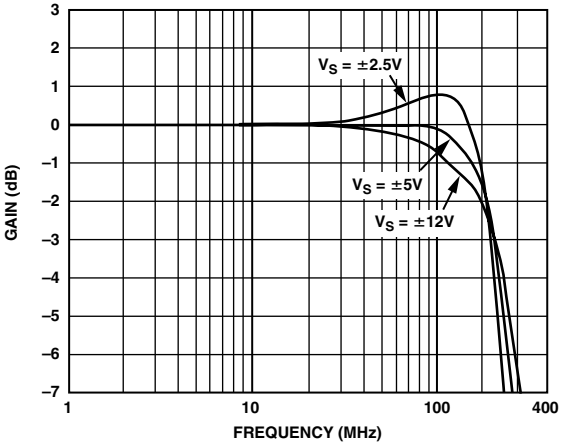



*Figure 4-22. AD8130 frequency response vs. gain and supply voltage.*

Figure 4-21 shows the CMR vs. frequency of the AD8130. Figure 4-22 shows its gain vs. frequency for various supply voltages.

# Chapter V

# APPLYING IN-AMPS EFFECTIVELY

**Dual-Supply Operation**

The conventional way to power an in-amp has been from a *split* or dual polarity power supply. This has the obvious advantage of allowing both a positive and a negative input and output swing.

**Single-Supply Operation**

Single-supply operation has become an increasingly desirable characteristic of a modern in-amp. Many present day data acquisition systems are powered from a single low voltage supply. For these systems, there are two vitally important characteristics. First, the in-amp's input range should extend between the positive supply and the negative supply (or ground). Second, the amplifier's output should be rail-to-rail as well.

**The Need for True R-R Devices in Low Voltage, Single-Supply IA Circuits**

Sometimes problems arise when designers forget about amplifier headroom and use standard (non rail-to-rail) products in low voltage, single-supply in-amp applications. Many dual-supply in-amps will only have an output swing within about 2 V of either rail. However, even the very best cannot swing as close to the rails as a single-supply device.

A good quality rail-to-rail in-amp, such as the AD623, can swing its output to within 0.5 V of the supply and within 0.1 V above ground. Its input voltage range is similar. Note that these numbers are conservative: with very light output loading the performance is even better. So, when using a 5 V single supply, the amplifier has at least a 4 V output swing, in many cases, more than that.

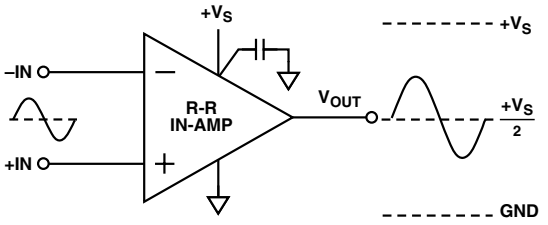



*Figure 5-1. A modern rail-to-rail in-amp can swing more than 4 V p-p with a 5 V supply, but this is NOT possible using a standard dual-supply device. Note that the in-amp's $V_{REF}$ pin would normally be set at $V_S/2$ for maximum output swing.*

In the example shown in Figure 5-1, the p-p output swing would only be about 1 V p-p for a standard product vs. 4 V p-p or more for a rail-to-rail in-amp.

**Power Supply Bypassing, Decoupling, and Stability Issues**

Power supply decoupling is an important detail that is often overlooked by designers. Normally, bypass capacitors (values of 0.1 μF are typical) are connected between the power supply pins of each IC and ground. Although usually adequate, this practice can be ineffective or even create worse transients than no bypassing at all. It is important to consider where the circuit's currents originate, where they will return, and by what path. Once that has been established, bypass these currents around ground and other signal paths.

In general, like op amps, most monolithic in-amps have their integrators referenced to one or both power supply lines and should be decoupled with respect to the output reference terminal. This means that for each chip, a bypass capacitor should be connected between each power supply pin and the point on the board where the in-amp's reference terminal is connected, as shown in Figure 5-2.

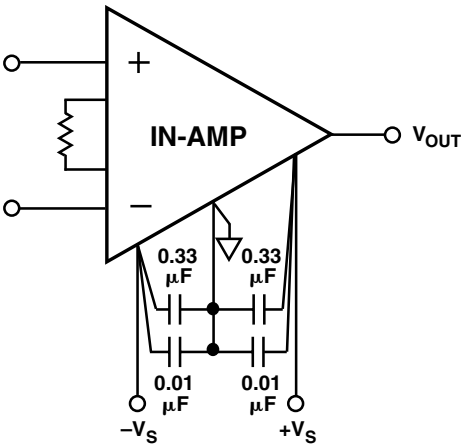



*Figure 5-2. Recommended method for power supply bypassing.*

For a much more comprehensive discussion of these issues, refer to Application Note AN-202, *An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change*, by Paul Brokaw, on the ADI website at *www.analog.com*.

## THE IMPORTANCE OF AN INPUT GROUND RETURN

AC coupling is an easy way to block dc voltages that are present at the in-amp's inputs. But ac coupling into a high impedance in-amp input without providing a dc return renders the circuit nonfunctional! This is one of the most common applications problems that arises when using in-amp circuits. Figure 5-3 shows two common (incorrect) arrangements.

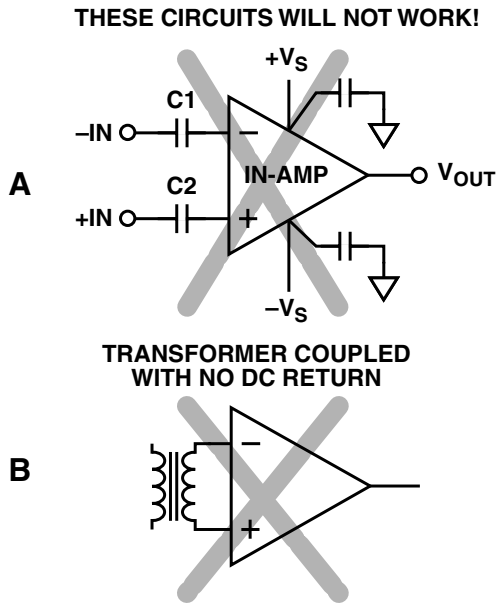



*Figure 5-3. Nonfunctional, ac-coupled in-amp circuits.*

In Figure 5-3A, the input bias currents will charge up the ac coupling capacitors until the input common-mode voltage is exceeded. In other words, the caps will charge up to the supply line or down to ground depending on the direction of the input bias currents. Now, with a FET input device, and very large capacitors, it could take several minutes before the in-amp is rendered inoperative. As a result, a casual lab test might not detect this problem, so it's very important to avoid it altogether. Figure 5-3B shows a transformer-coupled input with no center tap or other means for a dc return; so, the same problem occurs.

A simple solution for the circuit in Figure 5-3A is to add a high value resistance (R1, R2) between each input and ground, as shown in Figure 5-4. The input bias currents can now flow freely to ground and do not build up a large input offset as before.

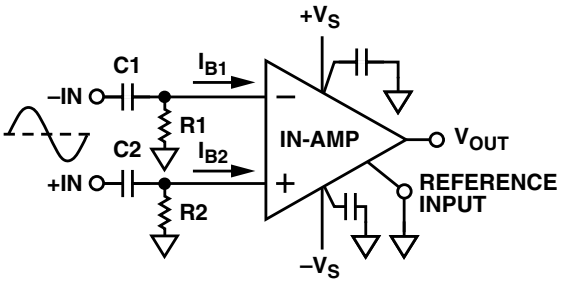



*Figure 5-4. A high value resistor between each input and ground provides an effective dc return path (see Table 5-1).*

This is a simple and practical solution for dual-supply in-amp circuits. The resistors allow a discharge path for input bias currents. Now both inputs are referenced to ground. There will be a small offset voltage error due to the mismatch between the input bias currents flowing through the two nonidentical resistors. To avoid errors due to an R1/R2 mismatch, a third resistor, about one-tenth their value, can be connected between the two in-amp inputs.

Figure 5-5 shows the recommended dc return for a transformer-coupled input.

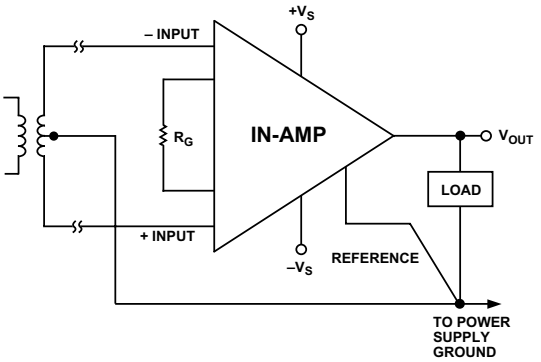



*Figure 5-5. Recommended dc return path for a transformer-coupled input.*

For transformers without a center tap, two resistors, one from each input pin to ground, can be used to provide a dc return path.

**Providing Adequate Input and Output Swing ("Headroom") When AC Coupling a Single-Supply In-Amp**

AC coupling using an in-amp powered by a single supply is more complicated than dual-supply operation and normally requires applying a dc common-mode voltage, $V_{CM}$, to both inputs, as shown in Figure 5-6. This is necessary because the internal buffer amplifiers of a typical 3-op amp in-amp cannot swing more than a few millivolts below the negative supply (in this case ground) without clipping the signal. In addition, the output can never swing below the negative supply.

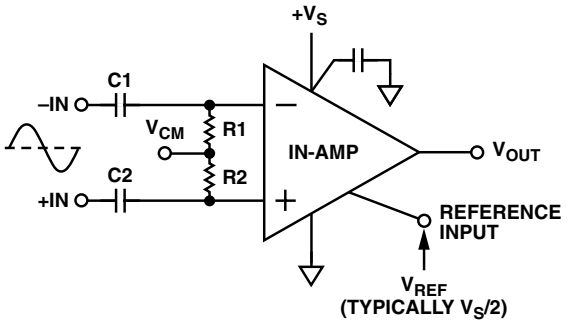



*Figure 5-6. An ac-coupled, single-supply, in-amp circuit. For maximum dynamic range, set $V_{CM}$ to the center of the maximum input range. $V_{REF}$ is typically set to $V_S/2$.*

Choosing appropriate voltages for $V_{CM}$ and $V_{REF}$ is an important design consideration, especially in low supply voltage applications. In general terms, $V_{CM}$ should be set to the middle of the expected *input* dynamic range, while $V_{REF}$ should be centered on the expected *output* dynamic rage. As an example, say the input signal (the difference between +IN and –IN) is expected to be between +1 V and –2 V. Under these conditions, the in-amp's input buffers will need to swing both positive and negative with respect to ground. Assume the in-amp is operating at unity gain, $V_{CM}$ can be set to +2 V (or a bit higher), which will allow 2 V of headroom in the minus direction. The trade-off is that there is now 2 V less swing in the positive direction. If the in-amp is operating with gain, $V_{CM}$ needs to be tailored to allow the buffer outputs to swing fully without clipping (that is, without exceeding their maximum voltage swing in either direction).

Output centering is similar: estimate the amount and the direction of the in-amp's output swing (in most cases this will be $V_{IN} \times$ gain + $V_{REF}$) and then apply a reference voltage at $V_{REF}$ that is in the center of that range.

**Selecting and Matching RC Coupling Components**

In ac-coupled applications, selecting values for the capacitors and dc return resistors is a trade-off between –3 dB bandwidth, noise, input bias current, and the physical size of the capacitors. RC components should be reasonably matched so that the time constant of R1/C1 is close to that of R2, C2. Otherwise, a common-mode voltage can be converted into a differential error.

Higher value input capacitors provide greater low frequency bandwidths and allow smaller value input resistors. But these caps are physically larger, requiring more board space. As a rule, capacitors larger than 0.1 microFarad need to be polarized types such as tantalums to keep their size manageable. But polarized caps require a known, constant polarity dc voltage to keep them properly biased.

Smaller cap values require higher value input resistors which have higher noise. And with larger input resistors, dc offset voltage errors also become larger. So, there is always a trade-off that needs to be made here.

Since $(I_{B1}R_1) - (I_{B2}R_2) = \Delta V_{OS}$, any mismatch between R1 and R2 will cause an input offset imbalance $(I_{B1} - I_{B2})$. The input bias currents of Analog Devices in-amps vary widely, depending on input architecture. However, the vast majority have maximum input bias currents between 1.5 nA and 10 nA. A good guideline is to keep $I_BR < 10$ mV.

**Table 5-1. Recommended Component Values for AC Coupling In-Amp Inputs**

| –3 dB BW | RC Coupling Components C1, C2 | R1, R2 | Input Bias Current (IB) | $V_{OS}$ at Each Input | $V_{OS}$ Error for 2% R1, R2 Mismatch |
|---|---|---|---|---|---|
| 2 Hz | 0.1 µF | 1 MΩ | 2 nA | 2 mV | 40 µV |
| 2 Hz | 0.1 µF | 1 MΩ | 10 nA | 10 mV | 200 µV |
| 30 Hz | 0.047 µF | 115 kΩ | 2 nA | 230 µV | 5 µV |
| 30 Hz | 0.1 µF | 53.6 kΩ | 10 nA | 536 µV | 11 µV |
| 100 Hz | 0.01 µF | 162 kΩ | 2 nA | 324 µV | 7 µV |
| 100 Hz | 0.01 µF | 162 kΩ | 10 nA | 1.6 mV | 32 µV |
| 500 Hz | 0.002 µF | 162 kΩ | 2 nA | 324 µV | 7 µV |
| 500 Hz | 0.002 µF | 162 kΩ | 10 nA | 1.6 mV | 32 µV |

Table 5-1 gives typical R and C cookbook values for ac coupling using 1% metal film resistors and two values of input bias current.

**Properly Driving an In-Amp's Reference Input**

Another common applications problem occurs when a high impedance source is used to drive an in-amp's reference terminal. In the example shown in Figure 5-7, R2's added resistance unbalances the otherwise closely matched resistors in subtractor amplifier A3. A resistor divider is shown here, but the same problem is created with any input source that is even a small percentage of $R_{REF}$. This results in both a CMR error and a reference voltage error.

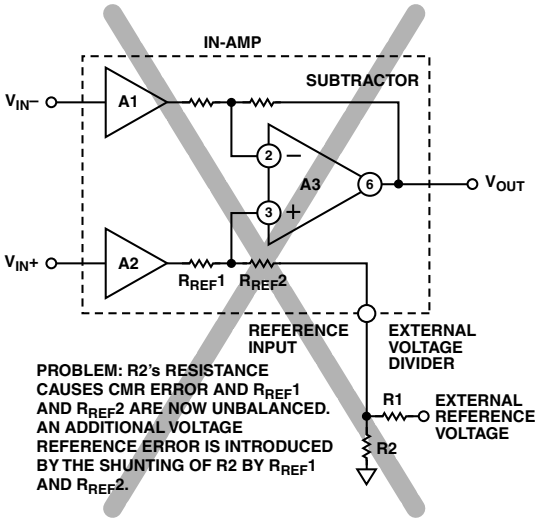



*Figure 5-7. When using this simple voltage divider, $R_{REF}1$ and $R_{REF}2$ are now unbalanced, which introduces a large CMR error in A3.*

A CMR error is introduced because $R_{REF}2$ no longer equals $R_{REF}1$ (R2 is in series). Note that $R_{REF}1$ and $R_{REF}2$ are not always equal but that introducing any significant series resistance between the $V_{REF}$ terminal and ground will unbalance A3 and cause a CMR error. A reference voltage error is also produced because R2 becomes loaded by the in-amp's finite reference impedance.

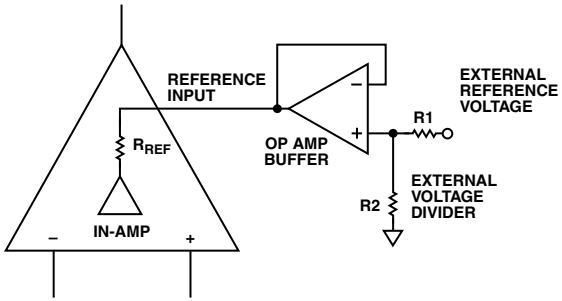



*Figure 5-8. A simple op amp buffer provides a low impedance for driving an in-amp's input.*

Figure 5-8 shows a simple solution to this problem. An op amp buffer is added between the voltage divider (or other high-Z source) and the in-amp's reference terminal. Now, the in-amp only sees the very low output impedance of the op amp, which typically is much less than one ohm.

Many other solutions are possible, as long as the impedance driving the reference terminal is kept very low.

## CABLE TERMINATION

When in-amps are used at frequencies above a few hundred kilohertz, properly terminated 50 Ω or 75 Ω coaxial cable should be used for input and output connections. Normally, cable termination is simply a 50 Ω or 75 Ω resistor connected between the cable center conductor, and its shield is at the end of the coaxial cable. Note that a buffer amplifier may be required to drive these loads to useful levels.

## INPUT PROTECTION BASICS FOR ADI IN-AMPS

### Input Protection from ESD and DC Overload

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of their full scale for the selected gain range or even in excess of the supply voltage. These overloads fall into two general classes: steady state and transient (ESD, etc.), both of which occur for only a fraction of a second. With 3-op amp in-amp designs, when operating at low gains (10 or less), the gain resistor acts as a current-limiting element in series with their resistor inputs. At high gains, the lower value of $R_G$ may not adequately protect the inputs from excessive currents.

Standard practice is to place current-limiting resistors in each input, but adding this protection also increases the circuit's noise level. A reasonable balance needs to be found between the protection provided and the increased resistor (Johnson) noise introduced. Circuits using in-amps with a relatively high noise level can tolerate more series protection without seriously increasing their total circuit noise.

Of course, the less added noise the better, but a good guideline is that circuits needing this extra protection can easily tolerate resistor values that generate 30% of the total circuit noise. For example, a circuit using an in-amp with a rated noise level of 20 nV/$\sqrt{\text{Hz}}$ can tolerate an additional 6 nV/$\sqrt{\text{Hz}}$ of Johnson noise.

Use the following cookbook method to translate this number into a practical resistance value. The Johnson noise of a 1 kΩ resistor is approximately 4 nV/$\sqrt{\text{Hz}}$. This value varies as the square root of the resistance. So, a 20 kΩ resistor would have $\sqrt{20}$ times as much noise as the 1 kΩ resistor, which is 17.88 nV/$\sqrt{\text{Hz}}$ (4.4721 × 4 nV/$\sqrt{\text{Hz}}$). Because *both* inputs need to be protected, two resistors are needed, and their combined noise will add as the square root of the number of resistors (the root sum of squares value). In this case, the total added noise from the two 20 kΩ resistors will be 25.3 nV/$\sqrt{\text{Hz}}$ (17.88 × 1.414).

Figure 5-9 provides details on the input architecture of the AD8221 in-amp. As shown, they have internal 400 Ω resistors that are in series with each input transistor junction.

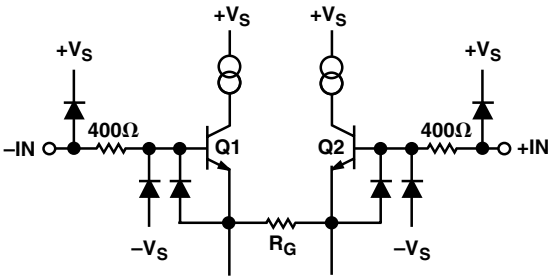



*Figure 5-9. AD8221 in-amp input circuit.*

The AD8221 was designed to handle maximum input currents of 6 mA steady state (or dc), at room temperature. Its internal resistors and diodes will protect the device from input voltages 0.7 V above the positive supply, or 2.4 V more negative than the minus supply (6 mA × 0.4 kΩ). Therefore, for ±15 V supplies, the maximum safe input level is +15.7 V, –17.4 V. Additional external series resistors can be added to increase this level considerably, at the expense of a higher circuit noise level.

The AD8221 in-amp is a very low noise device, with a maximum ($e_{NI}$) 8 nV/$\sqrt{\text{Hz}}$. A single 1 kΩ resistor will add approximately 4 nV/$\sqrt{\text{Hz}}$ of Johnson noise. The addition of this resistor would raise the maximum dc level to approximately 22.5 V above each supply or ±37.5 V with ±15 V supplies.

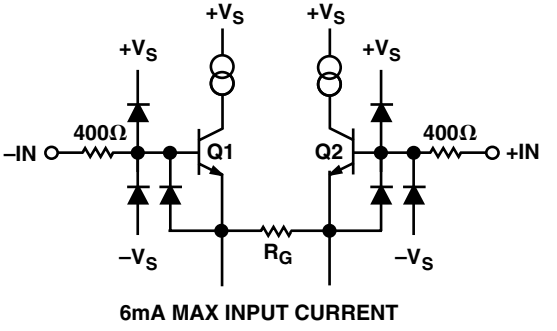



*Figure 5-10. AD8222 and AD8225 in-amp input circuit.*

The AD8222 and AD8225 have a very similar input section to that of the AD8221. Except that now, all six diodes are located on the Q1/Q2 side of the 400 Ω input resistor (see Figure 5-10).

Figure 5-11 shows the input section of the AD620 series (AD620, AD621, and AD622) in-amps. This is very similar to that of the AD8221: Both use a 400 Ω resistor in series with each input, and both use diode protection. The chief differences are the four additional AD8221 diodes. One set is tied between each input and the positive supply, and the other set is connected between the base of each input transistor and the negative supply. The AD620 uses its 400 Ω internal resistor and a single set of diodes to protect against negative input voltages. For positive voltage overloads, it relies on its own base-emitter input junction to act as the clamping diode.

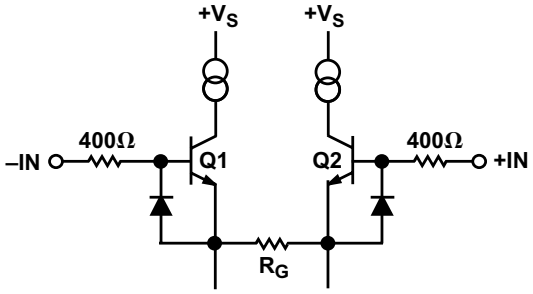



*Figure 5-11. AD620 series (AD620, AD621, and AD622) in-amp input circuit.*

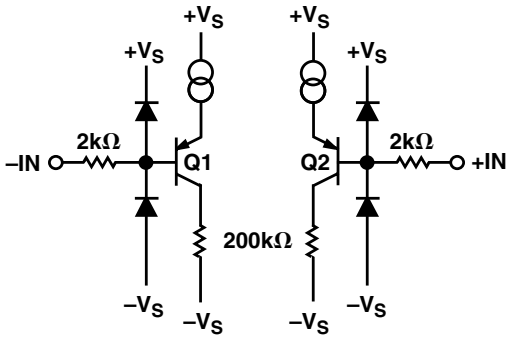



*Figure 5-12. AD627 in-amp input circuit.*

The AD627 can tolerate 20 mA transient input currents (Figure 5-12). In addition, it has built-in 2 kΩ resistors and can handle input voltages 40 volts higher than its supply lines (20 mA × 2 kΩ). This level of protection is quite beneficial. Because of its low power, many of the AD627's applications will use a low voltage single power supply. If even more protection is needed, quite large external resistors can be added without seriously degrading the AD627's 38 nV/√Hz noise level. In this case, adding two 5 kΩ resistors will raise the circuit's noise approximately 13 nV/√Hz (30 percent) but would provide an additional ±100 V of transient overload protection.

Figure 5-13 shows the input architecture of the AD623 in-amp. In this design, the internal (ESD) diodes are located *before* the input resistors and, as a consequence, provide less protection than the designs previously discussed. The AD623 can tolerate 10 mA maximum input current, but in many cases, some external series resistance will be needed to keep input current below this level.

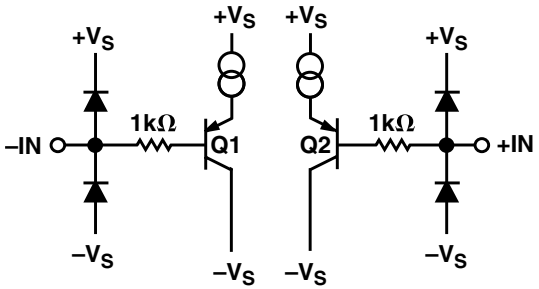



*Figure 5-13. AD623 in-amp input circuit.*

Since the AD623's device noise is approximately 35 nV/√Hz, up to 5 kΩ of external resistance can be added here to provide 50 V of dc overload protection, while only increasing input noise to 38 nV/√Hz total.

Figure 5-14 shows the simplified input circuitry for the AD8230 zero-drift in-amp. As shown, the AD8230 only has a single ESD diode connected between each input and the negative supply line. This diode offers ESD protection for negative pulses larger than 0.7 below the negative supply. However, it was not designed to protect the in-amp against positive voltage transients or long duration voltage overloads in either direction. To protect against these, external low leakage diodes and resistors are needed, as shown in Figure 5-20.

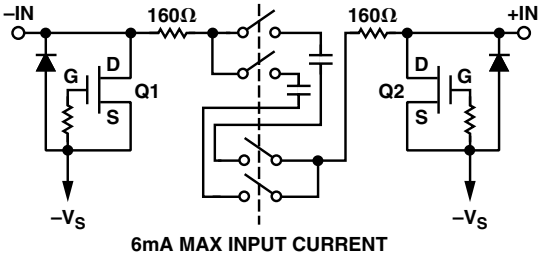



*Figure 5-14. AD8230 in-amp input circuit.*

Figure 5-15 is a simplified diagram showing the input structure for the AD8220 JFET in-amp. The input circuit has a very high impedance: typically 1000 GΩ and 6 pF. There are two ESD protection diodes at each input but no internal series resistance between the input terminals and the JFET input stage. Therefore, external resistors need to be added to limit the current in applications subject to an input overvoltage condition.

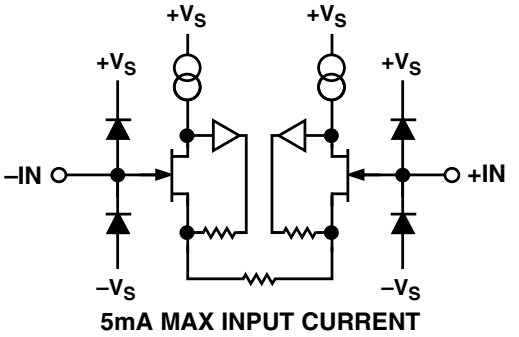



*Figure 5-15. AD8220 in-amp input circuit.*

Figure 5-16 shows a simplified version of the AD8250 input circuitry. Here, two internal resistors and two diodes protect each input. The AD8250 can tolerate maximum sustained input currents of 20 mA. Note that there are two pairs of input protection resistors—one between each input and the two ESD diodes, and the other between these diodes and the transistor base. This offers more protection to the transistor bases than to the ESD diodes. Therefore, designers should take precautions to protect the ESD diodes from being destroyed.

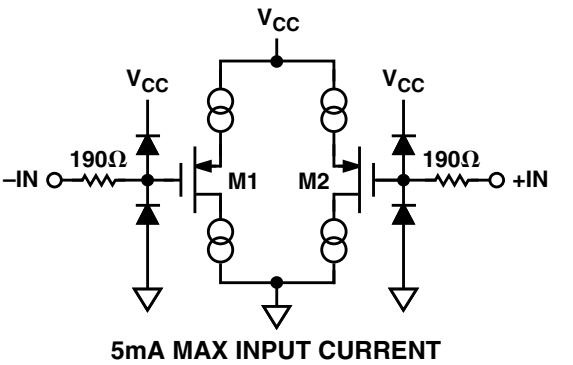



*Figure 5-17. AD8553 in-amp simplified input circuit.*

Figure 5-17 shows the input section of the AD8553 zero drift in-amp. This has a 190 Ω internal protection resistor between each input pin and the diode clamping circuitry.

The maximum input current of the AD8553 is approximately 5 mA, so additional external resistance may be needed in some applications (see table 5-2).

Also note that when the input voltage approaches $V_{CC} - 0.2$ V (outside the input common-mode range), current will begin to flow into the inputs of the AD8553. If the enable pin is also held low during this period of time, the output of the AD8553 will no longer be high impedance. In some applications, multiple AD8553 instrumentation amplifier outputs can be connected together to mux many inputs to one output. In these applications, only one AD8553 enable pin will be high, while all of the other AD8553 enable pins will be low.

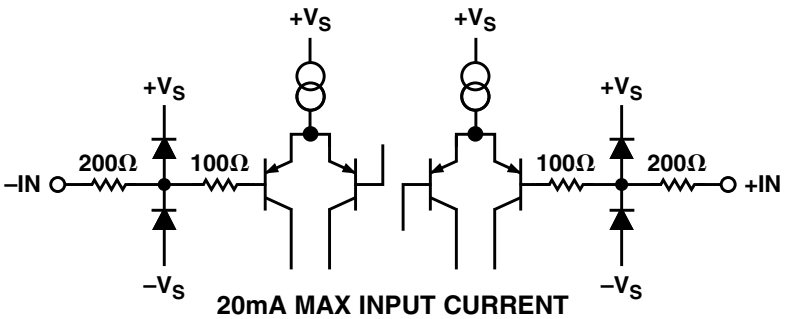



*Figure 5-16. AD8250 in-amp input circuit.*

If an input overload voltage of $V_{CC}$ – 0.2 V or greater occurs on any of the AD8553 instrumentation amplifier inputs while its enable pin is low, the output of that amplifier can overload the AD8553 that is driving the output (enable pin is high).

The AD8555 and AD8556 products are instrumentation amplifiers designed to be used in sensor applications. Figure 5-18 is a simplified input circuit for the AD8555. Here, protection diodes are connected between each input terminal and the supplies. The input signal then travels through a series resistor before arriving at the amplification and switching circuitry.

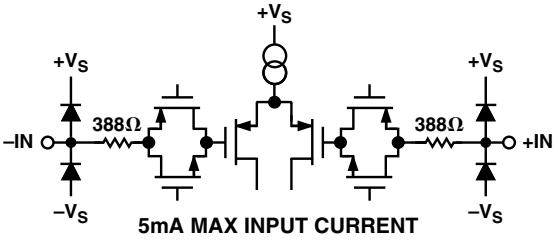



*Figure 5-18. AD8555 in-amp simplified input circuit.*

The AD8556 input circuitry (Figure 5-19) is very similar to that of the AD8555, except that there is a larger value resistor (3.6 kΩ) and other components between the diode and the amplifying and switching circuitry. These provide an internal RFI/EMI filtering capability.

Because the input circuitry in both products lacks an internal resistor, before the first set of clamping diodes, some external resistance is usually necessary to ensure adequate overvoltage protection.

Table 5-2 provides recommended series protection resistor values for a 10% or 40% increase in circuit noise.

**Table 5-2. Recommended Series Protection Resistor Values**

| Device | In-Amp Noise ($e_{NI}$) | Max Input Overload Current | Recommended External Protection Resistors Adding Additional Noise* | |
|---|---|---|---|---|
| | | | of 10% | of 40% |
| AD8220 | 15 nV/√Hz | 5 mA | 1.74 kΩ | 6.98 kΩ |
| AD8221 | 8 nV/√Hz | 6 mA | 500 Ω | 2.0 kΩ |
| AD8222 | 8 nV/√Hz | 6 mA | 500 Ω | 2.0 kΩ |
| AD8225 | 8 nV/√Hz | 6 mA | 500 Ω | 2.0 kΩ |
| AD8230 | 160 nV/√Hz | 6 mA | 4.99 kΩ | 4.99 kΩ |
| AD8250 | 13 nV/√Hz | 20 mA | 1.30 kΩ | 5.23 kΩ |
| AD8251 | 13 nV/√Hz | 20 mA | 1.30 kΩ | 5.23 kΩ |
| AD8553 | 30 nV/√Hz | 5 mA | 6.98 kΩ | 28.0 kΩ |
| AD8555 | 32 nV/√Hz | 5 mA | 8.06 kΩ | 32.4 kΩ |
| AD8556 | 32 nV/√Hz | 5 mA | 8.06 kΩ | 32.4 kΩ |
| AD620 | 9 nV/√Hz | 6 mA | 634 Ω | 2.55 kΩ |
| AD621 | 9 nV/√Hz | 6 mA | 634 Ω | 2.55 kΩ |
| AD622 | 9 nV/√Hz | 6 mA | 634 Ω | 2.55 kΩ |
| AD623 | 35 nV/√Hz | 10 mA | 9.53 kΩ | 38.3 kΩ |
| AD627 | 38 nV/√Hz | 20 mA | 11.3 kΩ | 45.3 kΩ |

*This noise level is for two resistors, one in series with each input.

### Adding External Protection Diodes

Device input protection may be increased with the addition of external clamping diodes as shown in Figure 5-20. As high current diodes are used, input protection is increased, which allows the use of much lower resistance input protection resistors that, in turn, reduces the circuit's noise.

Unfortunately, most ordinary diodes (Schottky, silicon, etc.) have high leakage currents that will cause large offset errors at the in-amp's output; this leakage increases exponentially with temperature. This tends to rule out the use of external diodes in applications where the in-amp is used with high impedance sources.

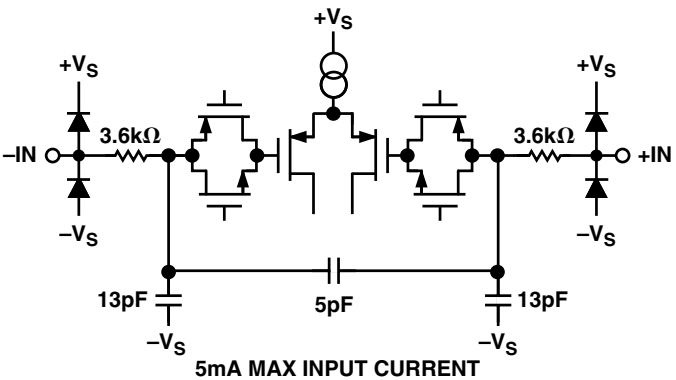
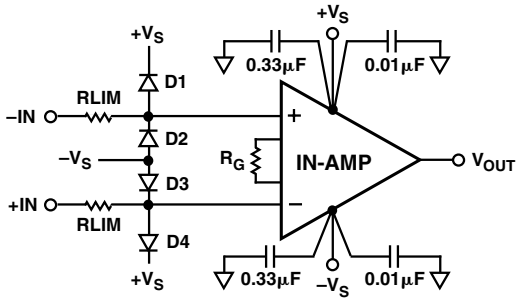



*Figure 5-19. AD8556 simplified input circuit.*

Specialty diodes with much lower leakage are available, but these are often difficult to find and are expensive. For the vast majority of applications, limiting resistors alone provide adequate protection for ESD and longer duration input transients.




**D1–D4 ARE INTERNATIONAL RECTIFIER SD101 SERIES FAST SCHOTTKY BARRIER RECTIFIERS**

*Figure 5-20. Using external components to increase input protection.*

Despite their limitations, external diodes are often required in some special applications, such as electric shock defibrillators, which utilize short duration, high voltage pulses. The combination of external diodes and very large input resistors (as high as 100 kΩ) may be needed to adequately protect the in-amp.

It is a good idea to check the diodes' specifications to ensure that their conduction begins well before the in-amp's internal protection diodes start drawing current. Although they provide excellent input protection, standard Schottky diodes can have leakage up to several mA. However, as in the example of Figure 5-20, fast Schottky barrier rectifiers, such as the international rectifier type SD101 series, can be used; these devices have 200 nA max leakage currents and 400 mW typical power dissipation.

**ESD and Transient Overload Protection**

Protecting in-amp inputs from high voltage transients and ESD events is very important for a circuit's long-term reliability. Power dissipation is often a critical factor, as input resistors, whether internal or external, must be able to handle most of the power of the input pulse without failing.

ESD events, while they may be very high voltage, are usually of very short duration and are normally one-time events. Since the circuit has plenty of time to cool down before the next event occurs, modest input protection is sufficient to protect the device from damage.

On the other hand, regularly occurring short duration input transients can easily overheat and burn out the input resistors or the in-amps input stage. A 1 kΩ resistor, in series with an in-amp input terminal drawing 20 mA, will dissipate 0.4 W, which can easily be handled by a standard 0.5 W or greater surface-mount resistor. If the input current is doubled, power consumption quadruples as it increases as the square of the input current (or as the square of the applied voltage).

Although it is a simple matter to use a higher power protection resistor, this is a dangerous practice, as the power dissipation will also increase in the in-amp's input stage. This can easily lead to device failure (see the preceding section on input protection basics for input current limitations of ADI in-amps). Except for ESD events, it is always best to adopt a conservative approach and treat all transient input signals as full duration inputs.

Designs that are expected to survive such events over long periods of time must use resistors with enough resistance to protect the in-amp's input circuitry from failure and enough power to prevent resistor burnout.

## DESIGN ISSUES AFFECTING DC ACCURACY

The modern in-amp is continually being improved, providing the user with ever increasing accuracy and versatility at a lower price. Despite these improvements in product performance, there remain some fundamental applications issues that seriously affect device accuracy. Now that low cost, high resolution ADCs are commonly used, system designers need to ensure that if an in-amp is used as a preamplifier ahead of the converter, the in-amp's accuracy matches that of the ADC.

**Designing for the Lowest Possible Offset Voltage Drift**

Offset drift errors include not just those associated with the active device being used (IC in-amp or discrete in-amp design using op amps), but also thermocouple effects in the circuit's components or wiring. The in-amp's input bias and input offset currents flowing through unbalanced source impedances also create additional offset errors. In discrete op amp in-amp designs, these errors can increase with temperature unless precision op amps are used.

**Designing for the Lowest Possible Gain Drift**

When planning for gain errors, the effects of board layout, the circuit's thermal gradients, and the characteristics of any external gain setting resistors are often overlooked. A gain resistor's absolute tolerance, its thermal temperature coefficient, its physical position relative to other resistors in the same gain network, and even its physical orientation (vertical or horizontal) are all-important design considerations if high dc accuracy is needed.

In many ADC preamp circuits, an external user-selected resistor sets the gain of the in-amp, so the absolute tolerance of this resistor and its variation over temperature, compared to that of the IC's on-chip resistors, will affect the circuit's gain accuracy. Resistors commonly used include through-hole 1% 1/4 W metal film types and 1% 1/8 W chip resistors. Both types typically have a 100 ppm/°C temperature coefficient. However, some chip resistors can have TCs of 200 ppm/°C or even 250 ppm/°C.

Even when a 1% 100 ppm/°C resistor is used, the gain accuracy of the in-amp will be degraded. The resistor's initial room temperature accuracy is only ±1%, and the resistor will drift another 0.01% (100 ppm/°C) for every °C change in temperature. The initial gain error can easily be subtracted out in software, but to correct for the error vs. temperature, frequent recalibrations (and a temperature sensor) would be required.

If the circuit is calibrated initially, the overall gain accuracy is reduced to approximately 10 bits (0.1%) accuracy for a 10°C change. An in-amp with a standard 1% metal film gain resistor should never be used ahead of even a 12-bit converter: It would destroy the accuracy of a 14-bit or 16-bit converter.

Additional error sources associated with external resistors also affect gain accuracy. The first are variations in resistor heating caused by input signal level. Figure 5-21, a simple op amp voltage amplifier, provides a practical example.

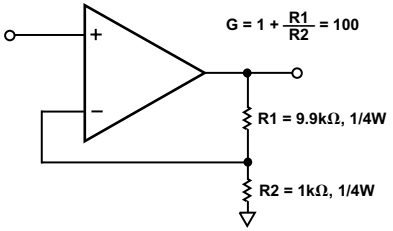



*Figure 5-21. An example of how differences in input signal level can introduce gain errors.*

Under zero signal conditions, there is no output signal and no resistor heating. When an input signal is applied, however, an amplified voltage appears at the op amp output. When the amplifier is operating with gain, Resistor R1 will be greater than R2. This means that there will be more voltage across R1 than across R2. The power dissipated in each resistor equals the square of the voltage across it divided by its resistance in ohms. The power dissipated and, therefore, the internal heating of the resistor will increase in proportion to the value of the resistor.

In the example, R1 is 9.9 kΩ and R2 is 1 kΩ. Consequently, R1 will dissipate 9.9 times more power than R2. This leads to a gain error that will vary with input level. The use of resistors with different temperature coefficients can also introduce gain errors.

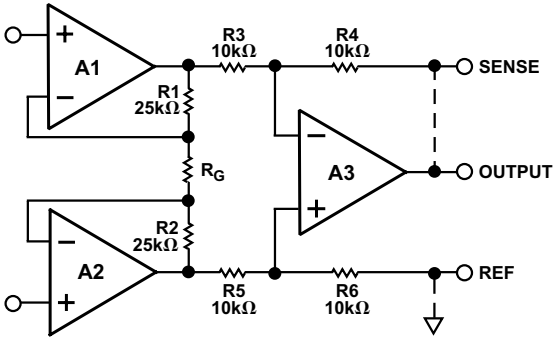


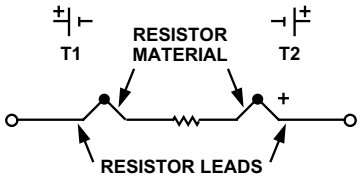

*Figure 5-22. A typical discrete 3-op amp in-amp using large value, low TC feedback resistors.*

Even when resistors with matched temperature coefficients (TC) are used, gain errors that vary with input signal level can still occur. The use of larger (i.e., higher power) resistors will reduce these effects, but accurate, low TC power resistors are expensive and hard to find.

When a discrete 3-op amp in-amp is used, as shown in Figure 5-22, these errors will be reduced. In a 3-op amp in-amp, there are two feedback resistors, R1 and R2, and one gain resistor, $R_G$. Since the in-amp uses two feedback resistors while the op amp uses only one, each of the in-amp's resistors only needs to dissipate half the power (for the same gain). Monolithic in-amps, such as the AD620, offer a further advantage by using relatively large value (25 kΩ) feedback resistors. For a given gain and output voltage, large feedback resistors will dissipate less power (i.e., $P = V^2/R_F$). Of course, a discrete in-amp can be designed to use large value, low TC resistors as well, but with added cost and complexity.

Another less serious but still significant error source is the so-called thermocouple effect, sometimes referred to as thermal EMF. This occurs when two different conductors, such as copper and metal film, are tied together. When this bimetallic junction is heated, a simple thermocouple is created. When using similar metals, such as a copper-to-copper junction, a thermoelectric error voltage of up to 0.2 mV/°C may be produced. An example of these effects is shown in Figure 5-23.

A final error source occurs when there is a thermal gradient across the external gain resistor. Something as simple as mounting a resistor on end to conserve board space will invariably produce a temperature gradient across the resistor. Placing the resistor flat down against the PC board will cure this problem unless there is air flowing along the axis of the resistor (where the air flow cools one side of the resistor more than the other side). Orienting the resistor so that its axis is perpendicular to the airflow will minimize this effect.




| TYPICAL RESISTOR THERMOCOUPLE EMFs | |
|---|---|
| • CARBON COMPOSITION | 400μV/°C |
| • METAL FILM | 20μV/°C |
| • EVENOHM OR MANGANIN WIRE-WOUND | 2μV/°C |
| • RCD COMPONENTS HP-SERIES | 0.05μV/°C |

*Figure 5-23. Thermocouple effects inside discrete resistors.*

**Practical Solutions**

As outlined, a number of dc offset and gain errors are introduced when external resistors are used with a monolithic in-amp. Discrete designs tend to have even larger errors. There are three practical solutions to this problem: use higher quality resistors, use software correction, or, better still, use an in-amp that has *all* of its gain resistors on-chip, such as the AD621.

***Option 1: Use a Better Quality Gain Resistor***

As a general rule, only 12-bit or 13-bit gain performance is possible using commonly available 1% resistors, which assumes that some type of initial calibration is performed.

A practical solution to this problem is to simply use a better quality resistor. A significant improvement can be made using a 0.1%, 1/10 W, surface-mount resistor. Aside from having a 10× better initial accuracy, it typically has a TC of only 25 ppm/°C, which will provide better than 13-bit accuracy over a 10°C temperature range.

If even better gain accuracy is needed, there are specialty houses that sell resistors with lower TCs, but these are usually expensive military varieties.

***Option 2: Use a Fixed-Gain In-Amp***

By far, the best overall dc performance is provided by using a monolithic in-amp, such as the AD621 or AD8225, in which all the resistors are contained within the IC. Now all resistors have identical TCs, all are at virtually the same temperature. Any thermal gradients across the chip are very small, and gain error drift is guaranteed and specified to very high standards.

At a gain of 10, the AD621 has a guaranteed maximum dc offset shift of less than 2.5 μV/°C and a maximum gain drift of ±5 ppm/°C, which is only 0.0005%/°C.

The AD8225 is an in-amp with a fixed gain of 5. It has a maximum offset shift of 2 μV/°C and a maximum drift of 0.3 μV/°C.

**RTI AND RTO ERRORS**

Another important design consideration is how circuit gain affects many in-amp error sources such as dc offset and noise. An in-amp should be regarded as a two stage amplifier with both an input and an output section. Each section has its own error sources.

Because the errors of the output section are multiplied by a fixed gain (usually 2), this section is often the principal error source at low circuit gains. When the in-amp is operating at higher gains, the gain of the input stage is increased. As the gain is raised, errors contributed by the input section are multiplied, while output errors are not. So, at high gains, the input stage errors dominate.

Since device specifications on different data sheets often refer to different types of errors, it is very easy for the unwary designer to make an inaccurate comparison between products. Any (or several) of four basic error categories may be listed: input errors, output errors, total error RTI, and total error RTO. Here follows an attempt to list, and hopefully simplify, an otherwise complicated set of definitions.

Input errors are those contributed by the amplifier's input stage alone; output errors are those due to the output section. Input related specifications are often combined and classified together as a referred to input (RTI) error, while all output related specifications are considered referred to output (RTO) errors.

For a given gain, an in-amp's input and output errors can be calculated using the following formulas:

$$\textit{Total Error, RTI} = \textit{Input Error} + (\textit{Output Error}/\textit{Gain})$$

$$\textit{Total Error, RTO} = (\textit{Gain} \times \textit{Input Error}) + \textit{Output Error}$$

Sometimes the specifications page will list an error term as RTI or RTO for a specified gain. In other cases, it is up to the user to calculate the error for the desired gain.

***Offset Error***

Using the **AD620A** as an example, the total voltage offset error of this in-amp when operating at a gain of 10 can be calculated using the individual errors listed on its specifications page. The (typical) input offset of the AD620 ($V_{OSI}$) is listed as 30 μV. Its output offset ($V_{OSO}$) is listed as 400 μV. Thus, the total voltage offset referred to input (RTI) is equal to

$$Total\ RTI\ Error = V_{OSI} + (V_{OSO}/G) = 30\ \mu V + (400\ \mu V/10) = 30\ \mu V + 40\ \mu V = 70\ \mu V$$

The total voltage offset referred to the output (RTO) is equal to

$$Total\ Offset\ Error\ RTO = (G\ (V_{OSI})) + V_{OSO} = (10\ (30\ \mu V)) + 400\ \mu V = 700\ \mu V$$

Note that the two error numbers (RTI vs. RTO) are different: the RTO numbers are 10× larger, and logically they should be, as at a gain of 10, the error at the output of the in-amp should be 10 times the error at its input.

***Noise Errors***

In-amp noise errors also need to be considered in a similar way. Since the output section of a typical 3-op amp in-amp operates at unity gain, the noise contribution from the output stage is usually very small. But there are 3-op amp in-amps that operate the output stage at higher gains, and 2-op amp in-amps regularly operate the second amplifier at gain. When either section is operated at gain, its noise is amplified along with the input signal. Both RTI and RTO noise errors are calculated the same way as offset errors, except that the noise of two sections adds as the root mean square. That is,

$$Input\ Noise = eni, Output\ Noise = eno$$

$$Total\ Noise\ RTI = \sqrt{(eni)^2 + (eno/Gain)^2}$$

$$Total\ Noise\ RTO = \sqrt{(Gain(eni))^2 + (eno)^2}$$

For example, the (typical) noise of the AD620A is specified as 9 nV/√Hz eni and 72 nV/√Hz eno. Therefore, the total RTI noise of the AD620A operating at a gain of 10 is equal to

$$Total\ Noise\ RTI = \sqrt{(eni)^2 + (eno/Gain)^2} = \sqrt{(9)^2 + (72/10)^2} = 11.5\,nV/\sqrt{Hz}$$

## REDUCING RFI RECTIFICATION ERRORS IN IN-AMP CIRCUITS

Real-world applications must deal with an ever increasing amount of radio frequency interference (RFI). Of particular concern are situations in which signal transmission lines are long and signal strength is low. This is the classic application for an in-amp, since its inherent common-mode rejection allows the device to extract weak differential signals riding on strong common-mode noise and interference.

One potential problem that is frequently overlooked, however, is that of radio frequency rectification inside the in-amp. When strong RF interference is present, it may become rectified by the IC and then appear as a dc output offset error. Common-mode signals present at an in-amp's input are normally greatly reduced by the amplifier's common-mode rejection.

Unfortunately, RF rectification occurs because even the best in-amps have virtually no common-mode rejection at frequencies above 20 kHz. A strong RF signal may become rectified by the amplifier's input stage and then appear as a dc offset error. Once rectified, no amount of low-pass filtering at the in-amp output will remove the error. If the RF interference is of an intermittent nature, this can lead to measurement errors that go undetected.

**Designing Practical RFI Filters**

The best practical solution is to provide RF attenuation *ahead* of the in-amp by using a differential low-pass filter. The filter needs to do three things: remove as much RF energy from the input lines as possible, preserve the ac signal balance between each line and ground (common), and maintain a high enough input impedance over the measurement bandwidth to avoid loading the signal source.

Figure 5-24 provides a basic building block for a wide number of differential RFI filters. Component values shown were selected for the AD8221, which has a typical –3 dB bandwidth of 1 MHz and a typical voltage noise level of 7 nV/$\sqrt{\text{Hz}}$. This same filter is recommended for the AD8222 dual in-amp and for the AD8220 JFET input in-amp. In addition to RFI suppression, the filter provides additional input overload protection, as resistors R1a and R1b help isolate the in-amp's input circuitry from the external signal source.

Figure 5-25 is a simplified version of the RFI circuit. It reveals that the filter forms a bridge circuit whose output appears across the in-amp's input pins. Because of this, any mismatch between the time constants of C1a/R1a and C1b/R1b will unbalance the bridge and reduce high frequency common-mode rejection. Therefore, resistors R1a and R1b and capacitors C1a and C1b should always be equal.

As shown, C2 is connected across the bridge output so that C2 is effectively in parallel with the series combination of C1a and C1b. Thus connected, C2 very effectively reduces any ac CMR errors due to mismatching. For example, if C2 is made 10 times larger than C1, this provides a 20× reduction in CMR errors due to C1a/C1b mismatch. Note that the filter does not affect dc CMR.

The RFI filter has two different bandwidths: differential and common mode. The differential bandwidth defines the frequency response of the filter with a differential input signal applied between the circuit's two inputs, +IN and –IN. This RC time constant is established by the sum of the two equal-value input resistors (R1a, R1b), together with the differential capacitance, which is C2 in parallel with the series combination of C1a and C1b.

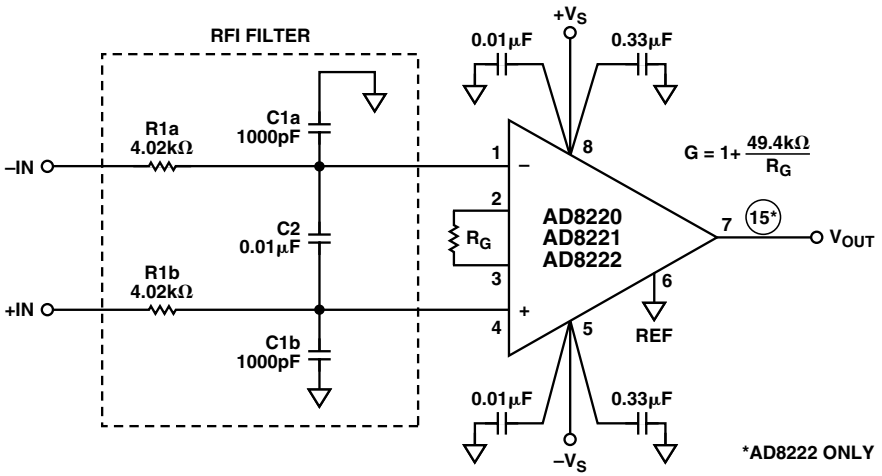



*Figure 5-24. LP filter circuit used to prevent RFI rectification errors in AD8220, AD8221, and AD8222 in-amps.*

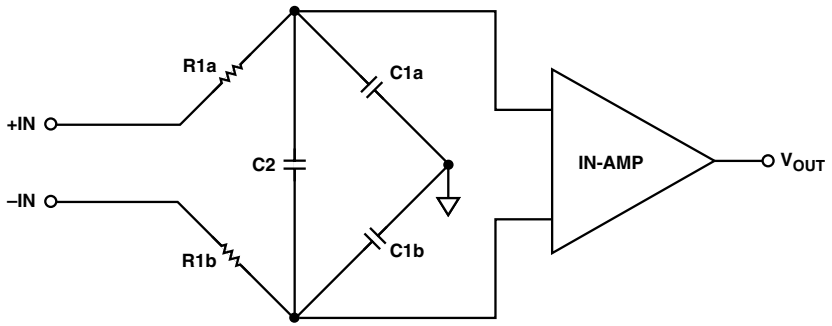



*Figure 5-25. Capacitor C2 shunts C1a/C1b and very effectively reduces ac CMR errors due to component mismatching.*

The –3 dB *differential* bandwidth of this filter is equal to

$$BW_{DIFF} = \frac{1}{2\pi R(2C2 + C1)}$$

The common-mode bandwidth defines what a common-mode RF signal *sees* between the two inputs tied together and ground. It's important to realize that C2 does not affect the bandwidth of the common-mode RF signal, as this capacitor is connected between the two inputs (helping to keep them at the same RF signal level). Therefore, common-mode bandwidth is set by the parallel impedance of the two RC networks (R1a/C1a and R1b/C1b) to ground.

The –3 dB *common-mode* bandwidth is equal to

$$BW_{CM} = \frac{1}{2\pi R1C1}$$

Using the circuit of Figure 5-24, with a C2 value of 0.01 μF as shown, the –3 dB differential signal bandwidth is approximately 1900 Hz. When operating at a gain of 5, the circuit's measured dc offset shift over a frequency range of 10 Hz to 20 MHz was less than 6 μV RTI. At unity gain, there was no measurable dc offset shift.

The RFI filter should be built using a PC board with ground planes on both sides. All component leads should be made as short as possible. The input filter common should be connected to the amplifier common using the most direct path. Avoid building the filter and the in-amp circuits on separate boards or in separate enclosures, as this extra lead length can create a loop antenna. Instead, physically locate the filter right at the in-amp's input terminals. A further precaution is to use good quality resistors that are both noninductive and nonthermal (low TC). Resistors R1 and R2 can be common 1% metal film units. However, all three capacitors need to be reasonably high Q, low loss components. Capacitors C1a and C1b need to be ±5% tolerance devices to avoid degrading the circuit's common-mode rejection. The traditional 5% silver micas, miniature size micas, or the new Panasonic ±2% PPS film capacitors (Digi-Key part # PS1H102G-ND) are recommended.

**Selecting RFI Input Filter Component Values Using a Cookbook Approach**

The following general rules will greatly ease the design of an RC input filter.

1. First, decide on the value of the two series resistors while ensuring that the previous circuitry can adequately drive this impedance. With typical values between 2 kΩ and 10 kΩ, these resistors should not contribute more noise than that of the in-amp itself. Using a pair of 2 kΩ resistors will add a Johnson noise of 8 nV/$\sqrt{\text{Hz}}$; this increases to 11 nV/$\sqrt{\text{Hz}}$ with 4 kΩ resistors and to 18 nV/$\sqrt{\text{Hz}}$ with 10 kΩ resistors.
2. Next, select an appropriate value for capacitor C2, which sets the filter's differential (signal) bandwidth. It's always best to set this as low as possible without attenuating the input signal. A differential bandwidth of 10 times the highest signal frequency is usually adequate.
3. Then select values for capacitors C1a and C1b, which set the common-mode bandwidth. For decent ac CMR, these should be 10% the value of C2 or less. The common-mode bandwidth should always be less than 10% of the in-amp's bandwidth at unity gain.

**Specific Design Examples**

***An RFI Circuit for AD620 Series In-Amps***

Figure 5-26 is a circuit for general-purpose in-amps such as the AD620 series, which have higher noise levels (12 nV/√Hz) and lower bandwidths than the AD8221. Accordingly, the same input resistors were used, but capacitor C2 was increased approximately five times to 0.047 μF to provide adequate RF attenuation. With the values shown, the circuit's –3 dB bandwidth is approximately 400 Hz; the bandwidth may be increased to 760 Hz by reducing the resistance of R1 and R2 to 2.2 kΩ. Note that this increased bandwidth does not come free. It requires the circuitry preceding the in-amp to drive a lower impedance load and results in somewhat less input overload protection.

***An RFI Circuit for Micropower In-Amps***

Some in-amps are more prone to RF rectification than others and may need a more robust filter. A micropower in-amp, such as the AD627, with its low input stage operating current, is a good example. The simple expedient of increasing the value of the two input resistors, R1a/R1b, and/or that of capacitor C2, will provide further RF attenuation, at the expense of a reduced signal bandwidth.

Since the AD627 in-amp has higher noise (38 nV/√Hz) than general-purpose ICs, such as the AD620 series devices, higher value input resistors can be used without seriously degrading the circuit's noise performance. The basic RC RFI circuit of Figure 5-24 was modified to include higher value input resistors, as shown in Figure 5-27.

The filter bandwidth is approximately 200 Hz. At a gain of 100, the maximum dc offset shift with a 1 V p-p input applied is approximately 400 μV RTI over an input range of 1 Hz to 20 MHz. At the same gain, the circuit's RF signal rejection (RF level at output/RF applied to the input) will be better than 61 dB.

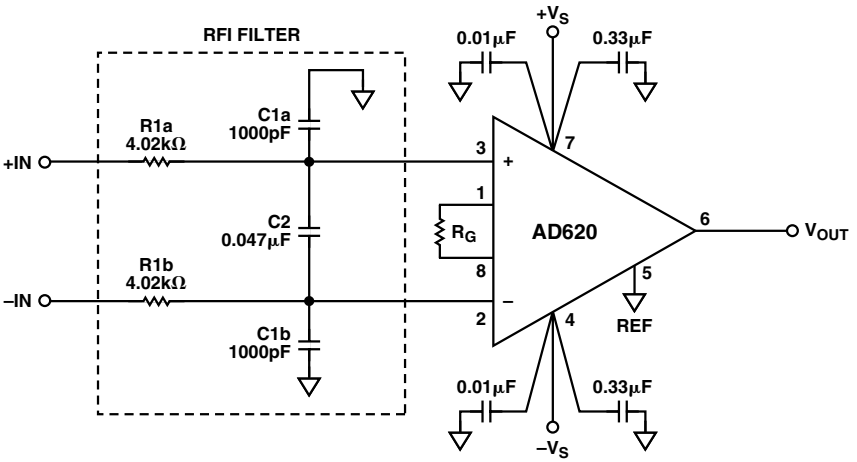



*Figure 5-26. RFI circuit for AD620 series in-amp.*

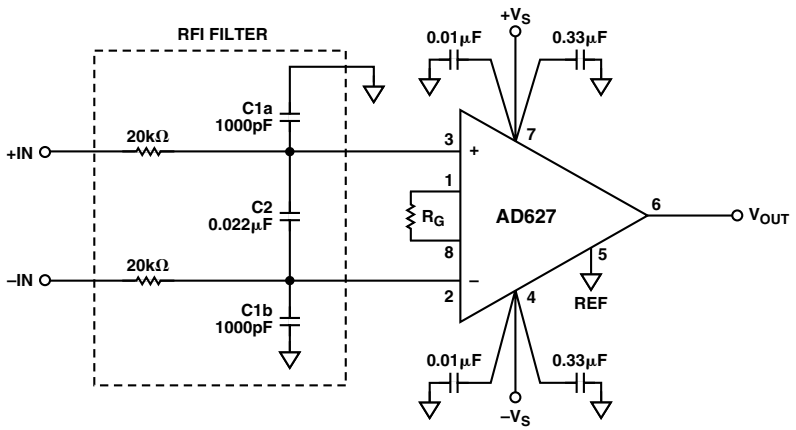



*Figure 5-27. RFI suppression circuit for the AD627.*

### *An RFI Filter for the AD623 In-Amp*

Figure 5-28 shows the recommended RFI circuit for use with the AD623 in-amp. Because this device is less prone to RFI than the AD627, the input resistors can be reduced in value from 20 kΩ to 10 kΩ; this increases the circuit's signal bandwidth and lowers the resistors' noise contribution. Moreover, the 10 kΩ resistors still provide very effective input protection. With the values shown, the bandwidth of this filter is approximately 400 Hz. Operating at a gain of 100, the maximum dc offset shift with a 1 V p-p input is less than 1 μV RTI. At the same gain, the circuit's RF signal rejection is better than 74 dB.

### *AD8225 RFI Filter Circuit*

Figure 5-29 shows the recommended RFI filter for this in-amp. The AD8225 in-amp has a fixed gain of 5 and a bit more susceptibility to RFI than the AD8221. Without the RFI filter, with a 2 V p-p, 10 Hz to 19 MHz sine wave applied, this in-amp measures about 16 mV RTI of dc offset. The filter used provides a heavier RF attenuation than that of the AD8221 circuit by using larger resistor values: 10 kΩ instead of 4 kΩ. This is permissible because of the AD8225's higher noise level. Using the filter, there was no measurable dc offset error.

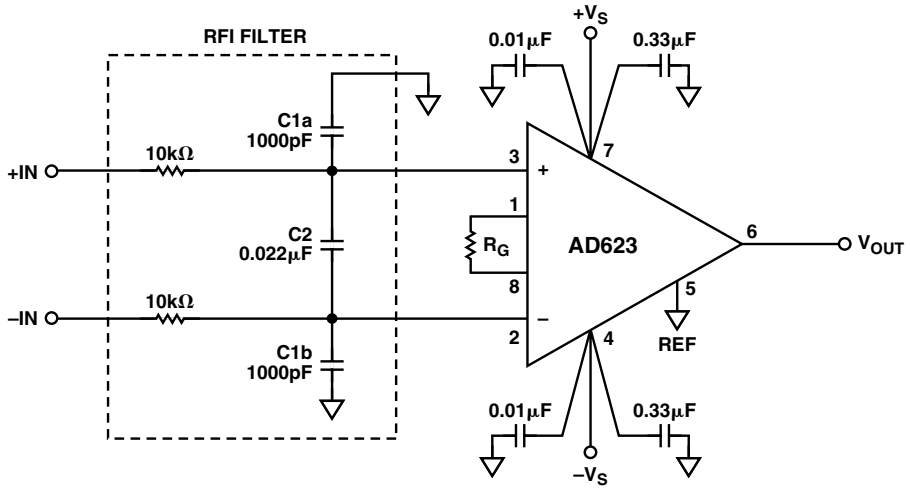



*Figure 5-28. AD623 RFI suppression circuit.*

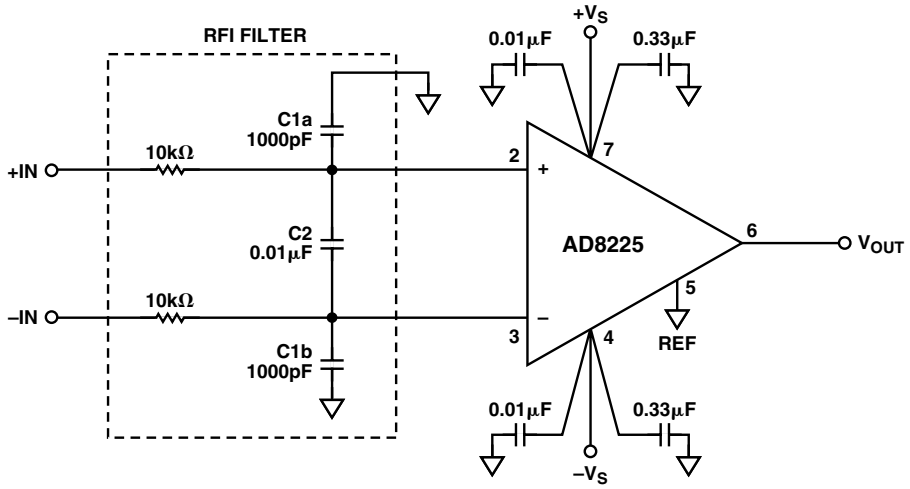



*Figure 5-29. AD8225 RFI filter circuit.*

## AN RFI FILTER FOR THE AD8555 SENSOR AMPLIFIER

The circuit in Figure 5-30 provides good RFI suppression without reducing performance within the AD8555 pass band. Using the component values shown, this filter has a common-mode bandwidth of approximately 40 kHz. To preserve common-mode rejection in the AD8555's pass band, capacitors need to be 5% (silver mica) or better and should be placed as close to its inputs as possible. Resistors should be 1% metal film. The circuit's differential bandwidth is approximately 4 kHz when a C3 value of 0.047 μF is used.

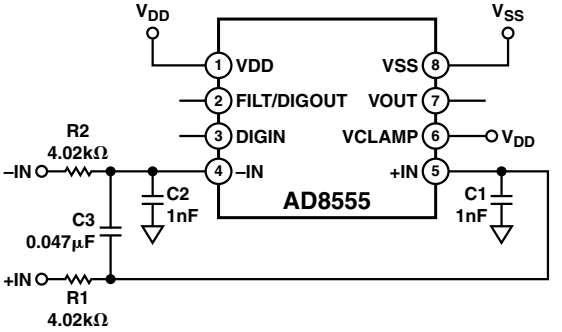



*Figure 5-30. AD8555 RFI filter circuit.*

## In-Amps with On-Chip EMI/RFI Filtering

The AD8556 is very similar to the AD8555. The AD8556 features internal EMI filters on the –IN, +IN, FILT, and VCLAMP pins. These built-in filters on the pins limit the interference bandwidth and provide good RFI suppression without reducing performance within the pass band of the in-amp. A functional diagram of AD8556 along with its EMI/RFI filters is shown in Figure 5-31.

AD8556 has on-chip filters on its inputs, VCLAMP, and filter pins. The first-order low-pass filters inside the AD8556 are useful to reject high frequency EMI signals picked up by wires and PCB traces outside the AD8556. The most sensitive pin of any amplifier to RFI/EMI signal is the noninverting pin. Signals present at this pin appear as common-mode signals and create problems.

The filters at the input of the AD8556 have two different bandwidths: common and differential mode. The EMI filters placed on the input pins of the AD8556 reject EMI/RFI suppressions that appear as common-mode signals.

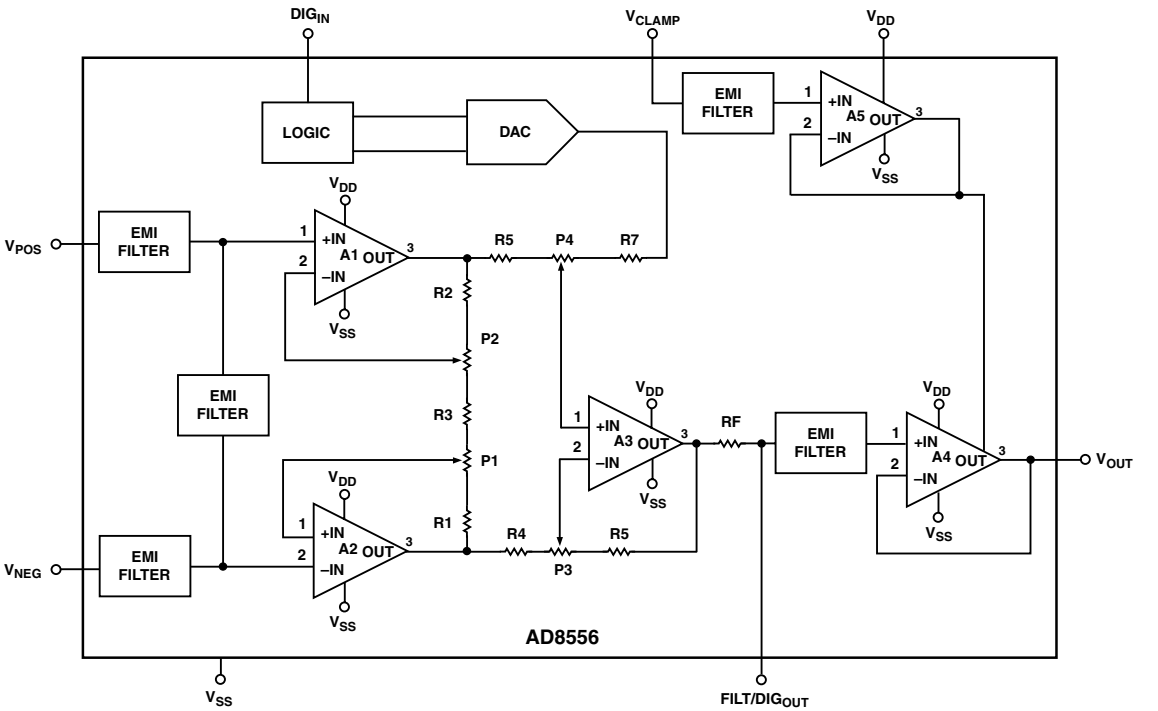



*Figure 5-31. AD8556 block diagram showing on-chip EMI/RFI filter.*

Figure 5-32 simulates the presence of a noisy common-mode signal, and Figure 5-33 shows the response dc values at $V_{OUT}$.

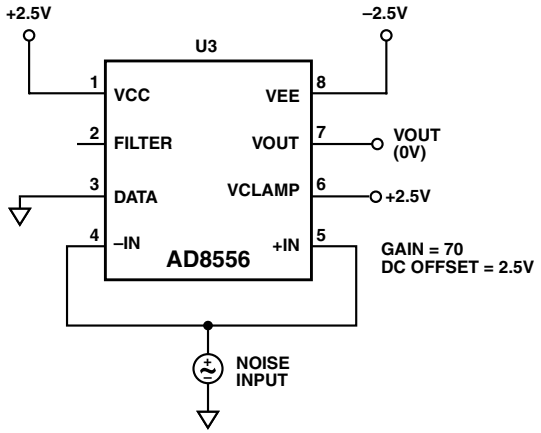



*Figure 5-32. Test circuit to show AD8556 performance exposed to common-mode RFI/EMI signals.*

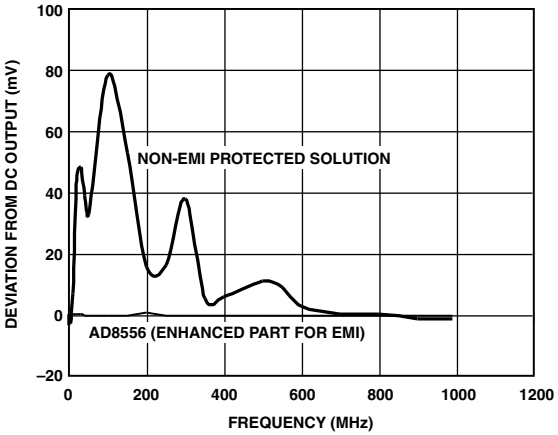



*Figure 5-33. DC input offset values at $V_{OUT}$ caused by common-mode RFI vs. frequency.*

The differential bandwidth defines the frequency response of the filters with a differential signal applied between the two inputs, VPOS (that is, +IN ) and VNEG (that is, –IN). Figure 5-34 shows the test circuit for AD8556 EMI/RFI susceptibility.

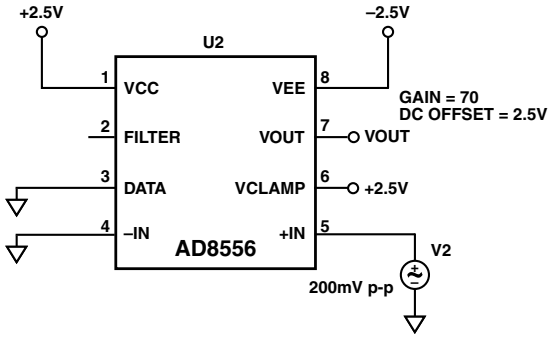



*Figure 5-34. Test circuit to show AD8556 performance exposed to differential-mode RFI/EMI signals.*

The response of AD8556 to EMI/RFI differential signals is shown in Figure 5-35.

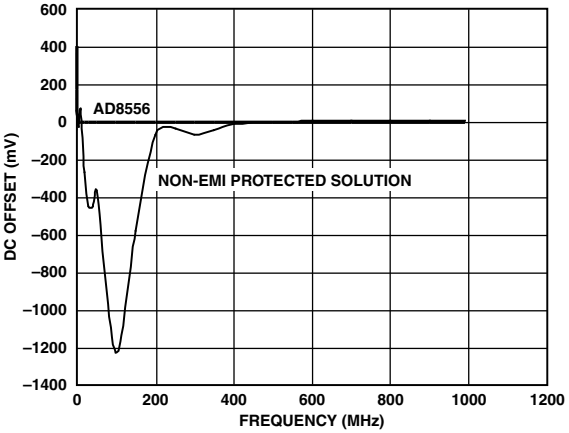



*Figure 5-35. DC offset shift of AD8556 due to EMI/RFI differential signals vs. frequency.*

For the most effective EMI rejection, the printed circuit board leads at VPOS and VNEG should be as similar as possible. In this way, any EMI received by the VPOS and VNEG pins will be similar (that is, a common-mode input), and rejected by the AD8556. Furthermore, additional filtering at the VPOS and VNEG pins should provide better reduction of unwanted behavior compared with filtering at the other pins.

**Common-Mode Filters Using X2Y® Capacitors***

Figure 5-36 shows the connection diagram for an X2Y capacitor. These are very small, three terminal devices with four external connections—A, B, G1, and G2. The G1 and G2 terminals connect internally within the device. The internal plate structure of the X2Y capacitor forms an integrated circuit with very interesting properties. Electrostatically, the three electrical nodes form two capacitors that share the G1 and G2 terminals. The manufacturing process automatically matches both capacitors very closely. In addition, the X2Y structure includes an effective autotransformer/common-mode choke. As a result, when these devices are used for common-mode filters, they provide greater attenuation of common-mode signals above the filter's corner frequency than a comparable RC filter. This usually allows the omission of capacitor C2, with subsequent savings in cost and board space.

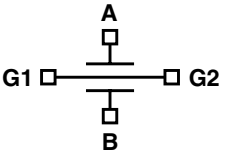



*Figure 5-36. X2Y electrostatic model.*

Figure 5-37a illustrates a conventional RC common-mode filter, while Figure 5-37b shows a common-mode filter circuit using an X2Y device. Figure 5-38 is a graph contrasting the RF attenuation provided by these two filters.

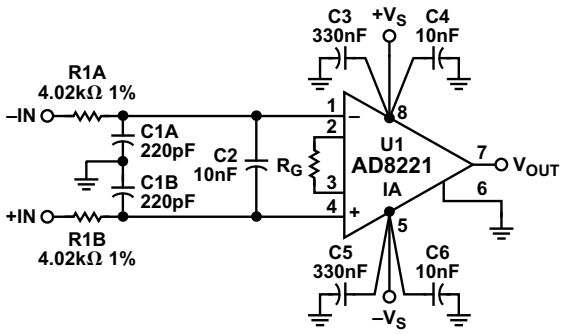



*Figure 5-37a. Conventional RC common-mode filter.*

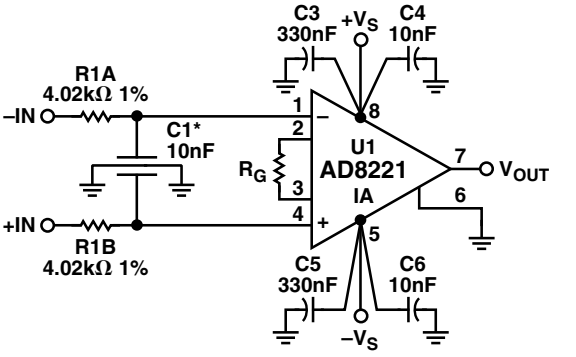



*Figure 5-37b. Common-mode filter using X2Y capacitor.*

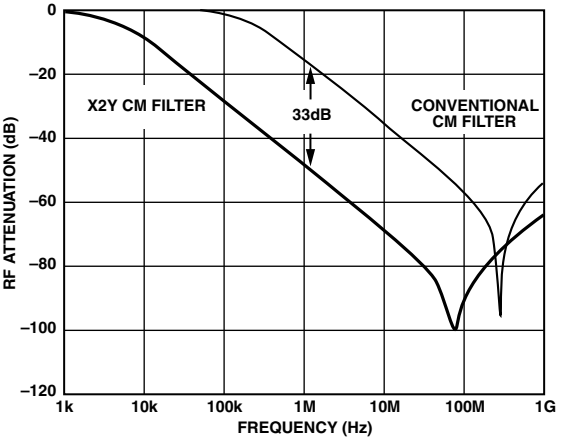



*Figure 5-38. RF attenuation, X2Y vs. conventional RC common-mode filter.*

*C1 is part number 500X14W103KV4. X2Y components may be purchased from Johanson Dielectrics, Sylmar, CA 91750, (818) 364-9800. For a full listing of X2Y manufacturers, visit *www.x2y.com/manufacturers*.

### *Using Common-Mode RF Chokes for In-Amp RFI Filters*

As an alternative to using an RC input filter, a commercial common-mode RF choke may be connected in front of an in-amp, as shown in Figure 5-39. A common-mode choke is a two-winding RF choke using a common core. Any RF signals that are common to both inputs will be attenuated by the choke. The common-mode choke provides a simple means for reducing RFI with a minimum of components and provides a greater signal pass band, but the effectiveness of this method depends on the quality of the particular common-mode choke being used. A choke with good internal matching is preferred. Another potential problem with using the choke is that there is no increase in input protection as is provided by the RC RFI filters.

Using an AD620 in-amp with the RF choke specified, at a gain of 1000, and a 1 V p-p common-mode sine wave applied to the input, the circuit of Figure 5-39 reduces the dc offset shift to less than 4.5 μV RTI. The high frequency common-mode rejection ratio was also greatly improved, as shown in Table 5-3.

**Table 5-3. AC CMR vs. Frequency Using the Circuit of Figure 5-39**

| Frequency | CMRR (dB) |
|---|---|
| 100 kHz | 100 |
| 333 kHz | 83 |
| 350 kHz | 79 |
| 500 kHz | 88 |
| 1 MHz | 96 |

Because some in-amps are more susceptible to RFI than others, the use of a common-mode choke may sometimes prove inadequate. In these cases, an RC input filter or an X2Y-based filter is a better choice.

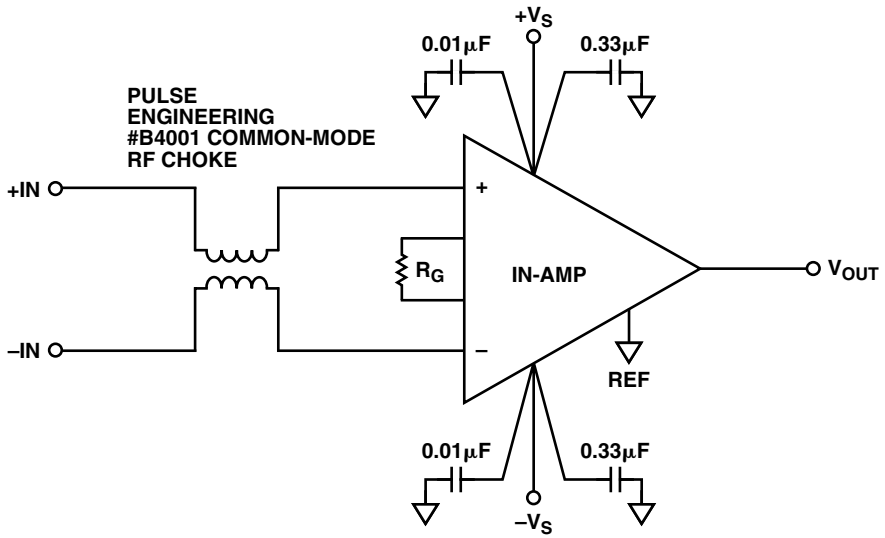



*Figure 5-39. Using a commercial common-mode RF choke for RFI suppression.*

**RFI TESTING**

Figure 5-40 shows a typical setup for measuring RFI rejection. To test these circuits for RFI suppression, connect the two input terminals together using very short leads. Connect a good quality sine wave generator to this input via a 50 Ω terminated cable.

Using an oscilloscope, adjust the generator for a 1 V peak-to-peak output at the generator end of the cable. Set the in-amp to operate at high gain (such as a gain of 100). DC offset shift is simply read directly at the in-amp's output using a DVM. For measuring high frequency CMR, use an oscilloscope connected to the in-amp output by a compensated scope probe and measure the peak-to-peak output voltage (i.e., feedthrough) vs. input frequency. When calculating CMRR vs. frequency, remember to take into account the input termination ($V_{IN}/2$) and the gain of the in-amp.

$$CMR = 20\log\frac{\left(\frac{V_{IN}}{2}\right)}{\left(\frac{V_{OUT}}{Gain}\right)}$$

**USING LOW-PASS FILTERING TO IMPROVE SIGNAL-TO-NOISE RATIO**

To extract data from a noisy measurement, low-pass filtering can be used to greatly improve the signal-to-noise ratio of the measurement by removing all signals that are not within the signal bandwidth. In some cases, band-pass filtering (reducing response both below and above the signal frequency) can be employed for an even greater improvement in measurement resolution.

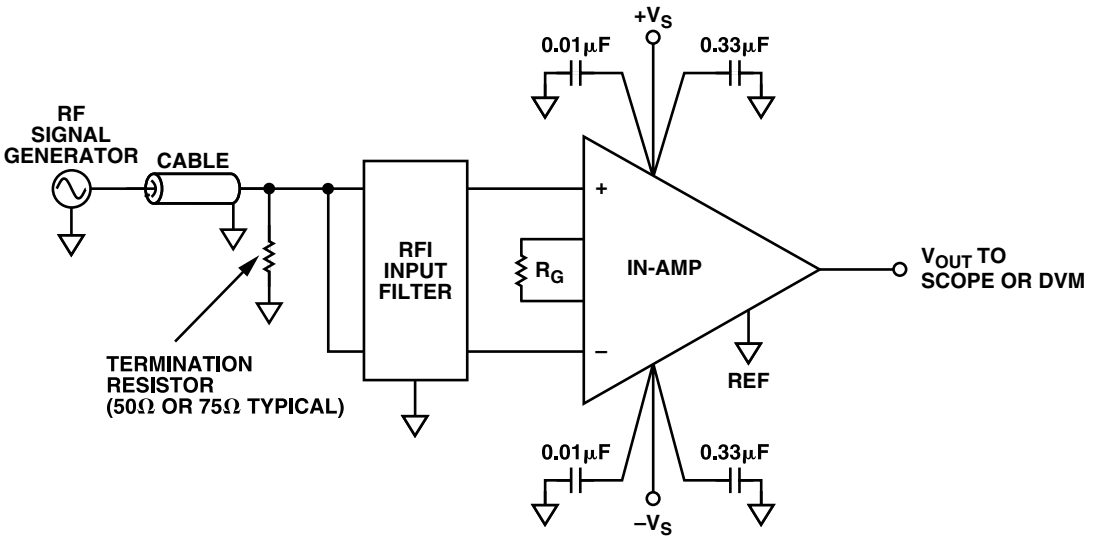



*Figure 5-40. Typical test setup for measuring an in-amp's RFI rejection.*

The 1 Hz, 4-pole, active filter of Figure 5-41 is an example of a very effective low-pass filter that normally would be added after the signal has been amplified by the in-amp. This filter provides high dc precision at low cost while requiring a minimum number of components.

Note that component values can simply be scaled to provide corner frequencies other than 1 Hz (see Table 5-4). If a 2-pole filter is preferred, simply take the output from the first op amp.

The low levels of current noise, input offset, and input bias currents in the quad op amp (either an **AD704** or **OP497**) allow the use of 1 MΩ resistors without sacrificing the 1 μV/°C drift of the op amp. Thus, lower capacitor values may be used, reducing cost and space.

Furthermore, since the input bias current of these op amps is as low as their input offset currents over most of the MIL temperature range, there is rarely a need to use the normal balancing resistor (along with its noise-reducing bypass capacitor). Note, however, that adding the optional balancing resistor will enhance performance at temperatures above 100°C.

Specified values are for a –3 dB point of 1.0 Hz. For other frequencies, simply scale capacitors C1 through C4 directly; i.e., for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, and C4 = 0.0205 μF.

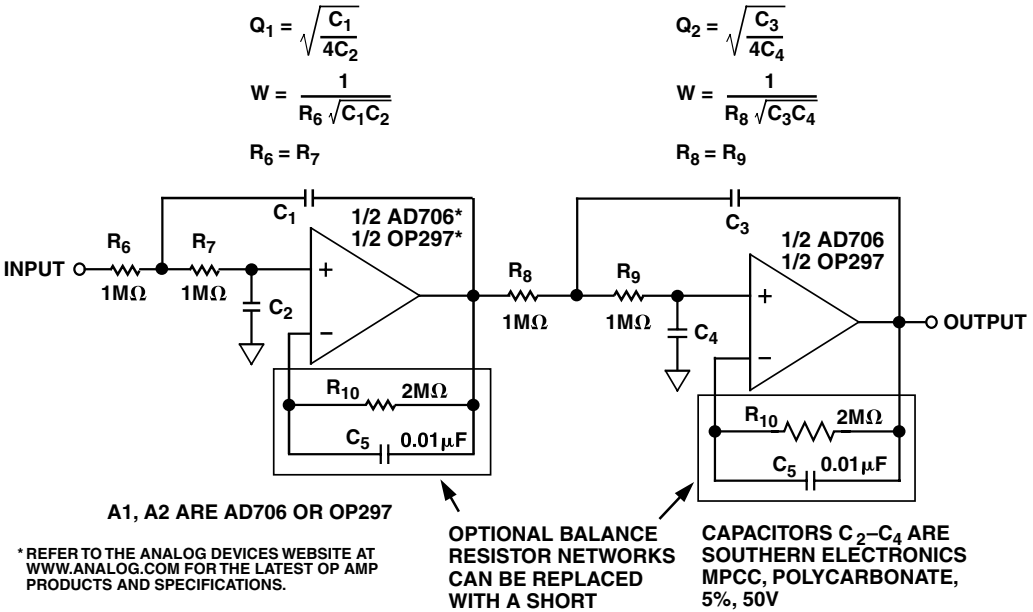



*Figure 5-41. A 4-pole low-pass filter for data acquisition.*

**Table 5-4. Recommended Component Values for a 1 Hz, 4-Pole, Low-Pass Filter**

| Desired Low-Pass Response | Section 1 | | Section 2 | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Frequency (Hz) | Q | Frequency (Hz) | (Q) | C1 (μF) | C2 (μF) | C3 (μF) | C4 (μF) |
| Bessel | 1.43 | 0.522 | 1.60 | 0.806 | 0.116 | 0.107 | 0.160 | 0.0616 |
| Butterworth | 1.00 | 0.541 | 1.00 | 1.31 | 0.172 | 0.147 | 0.416 | 0.0609 |
| 0.1 dB Chebychev | 0.648 | 0.619 | 0.948 | 2.18 | 0.304 | 0.198 | 0.733 | 0.0385 |
| 0.2 dB Chebychev | 0.603 | 0.646 | 0.941 | 2.44 | 0.341 | 0.204 | 0.823 | 0.0347 |
| 0.5 dB Chebychev | 0.540 | 0.705 | 0.932 | 2.94 | 0.416 | 0.209 | 1.00 | 0.0290 |
| 1.0 dB Chebychev | 0.492 | 0.785 | 0.925 | 3.56 | 0.508 | 0.206 | 1.23 | 0.0242 |

**EXTERNAL CMR AND SETTLING TIME ADJUSTMENTS**

When a very high speed, wide bandwidth in-amp is needed, one common approach is to use several op amps or a combination of op amps and a high bandwidth subtractor amplifier. These discrete designs may be readily tuned up for best CMR performance by external trimming. A typical circuit is shown in Figure 5-42. The dc CMR should always be trimmed first, since it affects CMRR at all frequencies.

The $+V_{IN}$ and $-V_{IN}$ terminals should be tied together and a dc input voltage applied between the two inputs and ground. The voltage should be adjusted to provide a 10 V dc input. A dc CMR trimming potentiometer would then be adjusted so that the outputs are equal and as low as possible, with both a positive and a negative dc voltage applied.

AC CMR trimming is accomplished in a similar manner, except that an ac input signal is applied. The input frequency used should be somewhat lower than the –3 dB bandwidth of the circuit.

The input amplitude should be set at 20 V p-p with the inputs tied together. The ac CMR trimmer is then nulled-set to provide the lowest output possible. If the best possible settling time is needed, the ac CMR trimmer may be used, while observing the output wave form on an oscilloscope. Note that, in some cases, there will be a compromise between the best CMR and the fastest settling time.

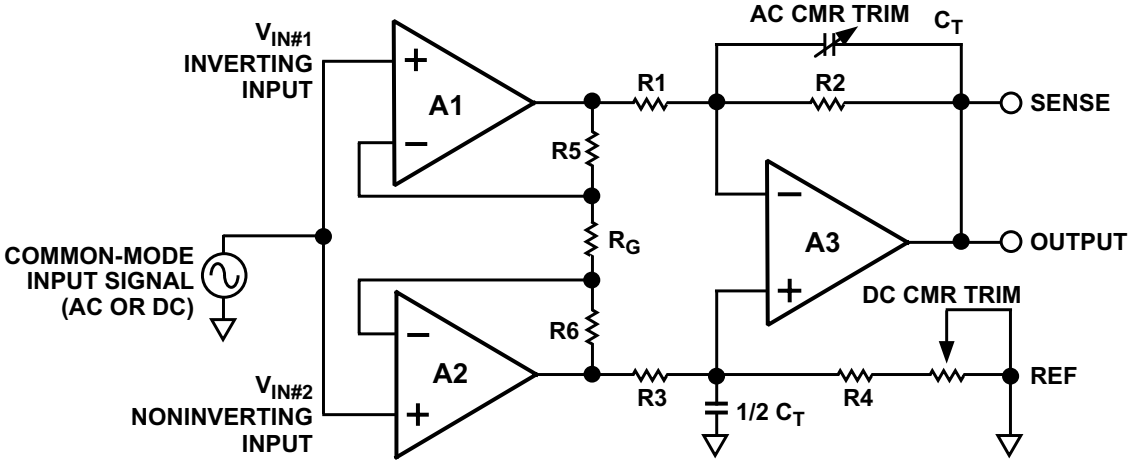



*Figure 5-42. External dc and ac CMR trim circuit for a discrete 3-op amp in-amp.*

# Chapter VI

# IN-AMP AND DIFF AMP APPLICATIONS CIRCUITS

**A True Differential Output In-Amp Circuit**
The AD8222 can be easily configured as a true differential output in-amp, as shown in Figure 6-1. Note that this connection provides a low impedance output at both +OUT and –OUT.

Because the differential voltage is set solely by Amplifier A1, all of the precision specifications (offset voltage, offset drift, and 1/f noise) are the same as if Amplifier A1 were operating in single-ended mode.

Amplifier A1 sets the differential output voltage by maintaining the following equation:

$$V_{DIFFOUT} = V_{+OUT} - V_{-OUT} = (V_{+IN} - V_{-IN}) \times Gain_{A1}$$

The output common-mode voltage is set by the average of $V_{REF2}$ voltage and $V_{REF1}$.

Amplifier A2 sets the output common-mode voltage by maintaining the following equation:

$$V_{CMOUT} = \frac{(V_{-OUT} + V_{+OUT})}{2} = \frac{(V_{REF2} + V_{REF1})}{2}$$

Because the $V_{REF1}$ and $V_{REF2}$ pins have different properties, the reference voltage may be easily set for a wide variety of applications. Note that $V_{REF2}$ is high impedance but cannot swing to the supply rails of the part. In contrast, $V_{REF1}$ must be driven with a low impedance but can go 300 mV beyond the supply rails. One very common application sets the common-mode output voltage to the midscale of a differential ADC. In this case, the ADC reference voltage would be sent to the $V_{REF2}$ terminal and ground would be connected to the $V_{REF1}$ terminal. This would produce a common-mode output voltage of half the ADC reference voltage.

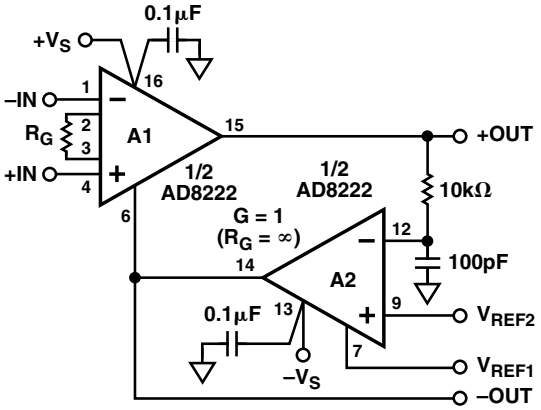



*Figure 6-1. Differential output in-amp circuit.*

**DIFFERENCE AMPLIFIER MEASURES HIGH VOLTAGES**

Figure 6-2 shows two conventional methods used to measure a large signal. One comprises a 2-resistor divider and an output buffer, the other an inverter with a large value input resistor. Both approaches suffer from the fact that only one resistor dissipates power and, therefore, is self-heating and the change in resistance due to temperature change results in a large nonlinearity error. Another problem associated with these approaches concerns the amplifier: The combination of offset current, offset voltage, CMRR, gain error, and drifts of the amplifier and resistors may significantly reduce the overall system performance.

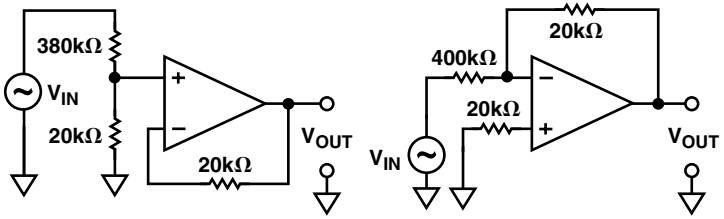



*Figure 6-2. Two conventional methods of measuring high voltage.*

Clearly, something better is needed. Figure 6-3 is a schematic of a circuit that can measure in excess of 400 volts peak-to-peak input with less than five parts per million nonlinearity error. The circuit attenuates an input signal 20 times and also provides output buffering. The amplifier, as well as the attenuator resistors, are all packaged together inside the AD629 IC so that both resistors in the attenuator string are at the same temperature. The amplifier stage employs superbeta transistors, so that offset current error and bias current errors are small. Also, since there is no noise gain (i.e., there is 100% feedback at low frequencies), the AD629's offset voltage and its drift add almost no additional error.

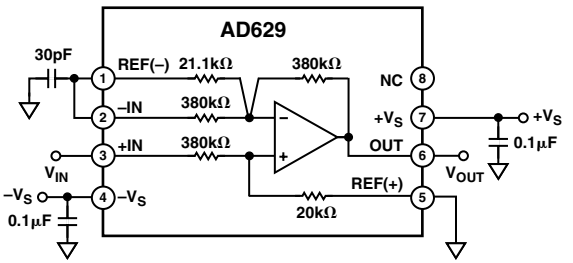



*Figure 6-3. New high voltage measurement system.*

The AD629 cannot work with a 100% feedback. A 30 pF capacitor adds a pole and a zero to the feedback gain, so stability is maintained and the system bandwidth is maximized. The pole is at

$$fp = 1/(2\pi\ (380\ k\Omega + 20\ k\Omega)\ 30\ pF) = 13\ kHz$$

The zero frequency is at

$$fz = 1/(2\pi\ (20\ k\Omega)\ 30\ pF) = 265\ kHz$$

Figure 6-4 is a performance photo showing a 400 V p-p input (top) and a 20 V p-p output (bottom). Figure 6-5 is a performance photo showing the output at 5 V p-p per division vs. the input signal at 50 V p-p per division. Figure 6-6, also a cross plot, shows nonlinearity vs. the input signal.

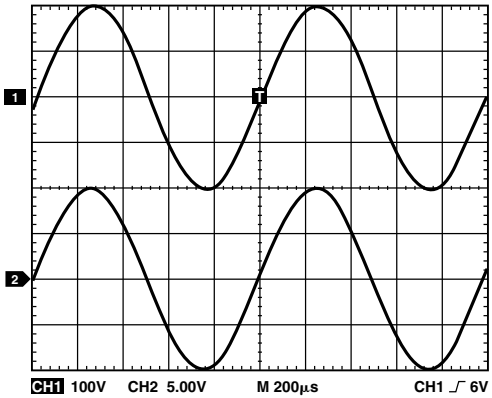



*Figure 6-4. Performance photo: top, input voltage (400 V p-p), bottom, output voltage (20 V p-p).*

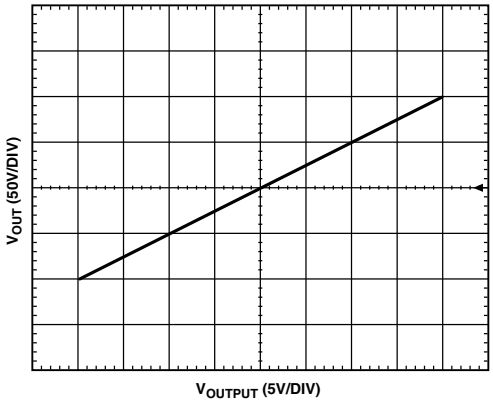



*Figure 6-5. Cross plot of the high voltage measurement system.*

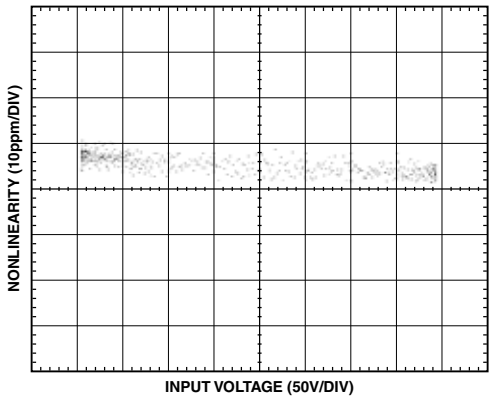



*Figure 6-6. Nonlinearity error of the high voltage measurement system:*
*Y axis: output nonlinearity error, 10 ppm/division.*
*X axis: input voltage, 50 volts/division.*

**Precision Current Source**

Figure 6-7 shows the AD8553 configured as a current source. The current output node voltage (labeled $I_{OUT}$) sets the voltage at the $V_{REF}$ pin of the AD8553. The input signal to the AD8553, $V_{IN}$, sets the current that flows through R1. Consequently, the voltage drop across R2 is set by $V_{IN}$, according to the following equation:

$$VR2 = 2(V_{IN}/R1)R2$$

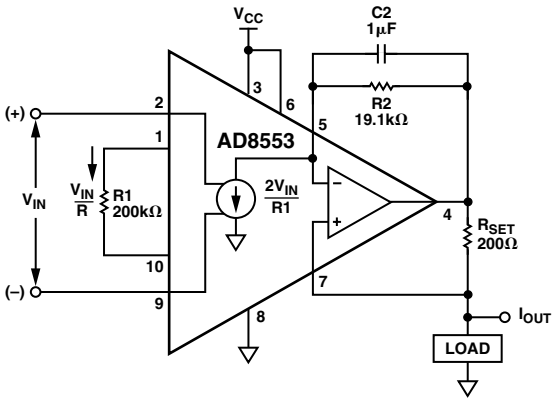
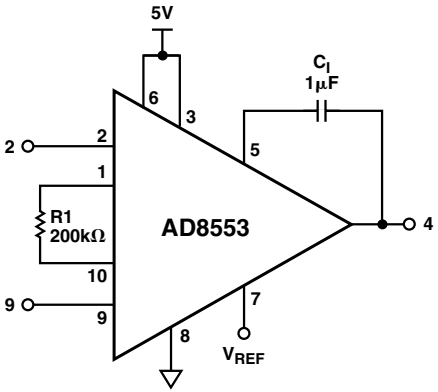



*Figure 6-7. Precision ±1 mA dc current source.*




$$f_U = \frac{1}{2\pi\left(\frac{R1}{2}\right)(C_I)}$$

*Figure 6-8. Low frequency differential input integrators for PID loop.*

**Integrator for PID Loop**

Figure 6-8 shows the AD8553 configured as an integrator. This configuration can be used within a PID (proportional integral differential) loop in a control system. In this case, the integrator's gain becomes one at $F_{UNITY} = 1/(\pi(R1)C_I)$. Note that this result is due to the fact that the AD8553 doubles the current through R1, resulting in an effective resistance (R1)/2. The input offset voltage of this configuration will be proportional to the size of R1, assuming that the system is in a steady state condition. Therefore, the input offset voltage of the integrator is determined primarily by the size of R1 along with the internal offsets of the AD8553, assuming that the system is in a steady state condition.

Now, the voltage between $V_{OUT}$ and $V_{REF}$ is equal to VR2. As a result, the output current from this current source is $I_{OUT} = (VR2/R_{SET})$. The value of this current can range between ±1 mA. This is $0.8\,V < V(@I_{OUT}) < V_{CC} - 0.8$ (single supply). Note that this range is limited by the dynamic range of the $V_{REF}$ pin on the AD8553. This compliance range would include ground on dual-supply systems. If R1 is adjusted, ensure that the current in R1 stays below 19 µA. If R2 values are adjusted, ensure that Pin 4 of the AD8553 does not exceed its valid output range (75 mV from each supply). This current source could be used to transmit a signal from one location to another distant location and transform it back into a voltage at the distant location using a transimpedance amplifier.

**Composite In-Amp Circuit Has Excellent High Frequency CMR**

The primary benefit of an in-amp circuit is that it provides common-mode rejection. While the AD8221 and AD8225 both have an extended CMR frequency range, most in-amps fail to provide decent CMR at frequencies above the audio range.

The circuit in Figure 6-9 is a composite instrumentation amplifier with a high common-mode rejection ratio. It features an extended frequency range over which the instrumentation amplifier has good common-mode rejection (Figure 6-10). The circuit consists of three instrumentation amplifiers. Two of these, U1 and U2, are correlated to one another and connected in antiphase. It is not necessary to match these devices because they are correlated by design. Their outputs, OUT1 and OUT2, drive a third instrumentation amplifier that rejects common-mode signals and amplifiers' differential signals. The overall gain of the system can be determined by adding external resistors. Without any external resistors, the system gain is 2 (Figure 6-11). The performance of the circuit with a gain of 100 is shown in Figure 6-12.

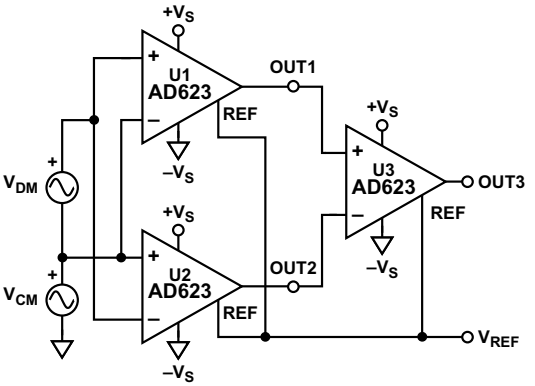



*Figure 6-9. A composite instrumentation amplifier.*

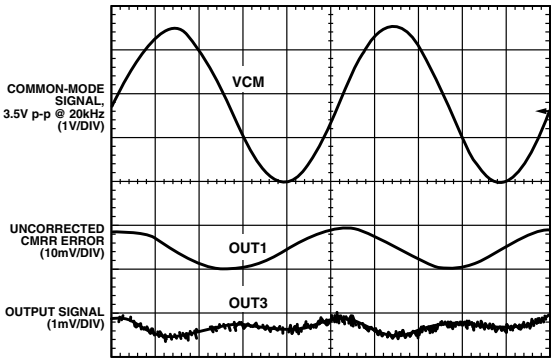



*Figure 6-10. CMR of the circuit in Figure 6-9 at 20 kHz.*

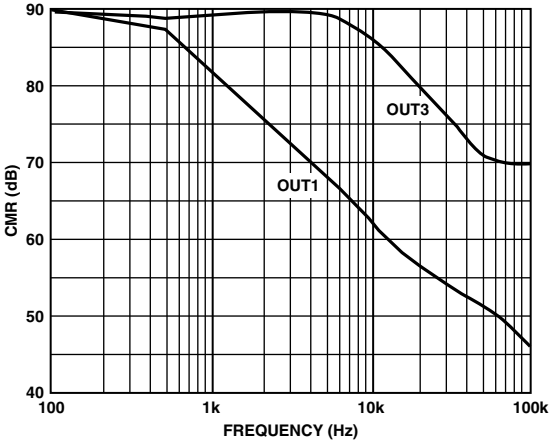



*Figure 6-11. CMR vs. frequency at a gain of 2.*

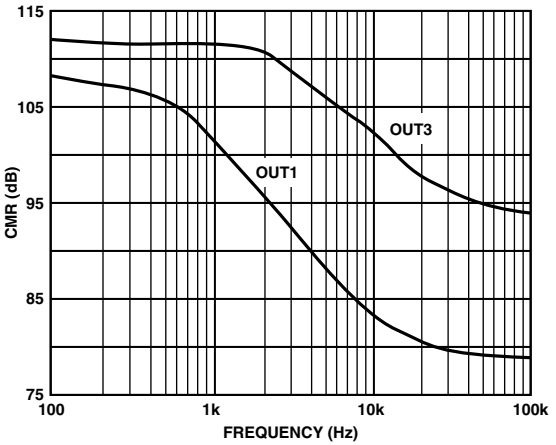



*Figure 6-12. CMR of the system at a gain of 100.*

Since U1 and U2 are correlated, their common-mode errors are the same. Therefore, these errors appear as common-mode input signal to U3, which rejects them. In fact, if it is necessary, OUT1 and OUT2 can directly drive an analog-to-digital converter (ADC), as seen in Figure 6-13. The differential-input stage of the ADC normally will reject the common-mode signal.

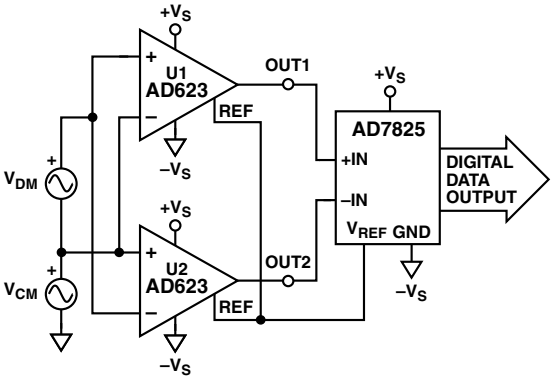



*Figure 6-13. The OUT1 and OUT2 signals of the first stage can directly drive an analog-to-digital converter, allowing the ADC to reject the common-mode signal.*

## STRAIN GAGE MEASUREMENT USING AN AC EXCITATION

Strain gage measurements are often plagued by offset drift, 1/f noise, and line noise. One solution is to use an ac signal to excite the bridge, as shown in Figure 6-14. The AD8221 gains the signal and an **AD630AR** synchronously demodulates the waveform. What results is a dc output proportional to the strain on the bridge. The output signal is devoid of all dc errors associated with the in-amp and the detector, including offset and offset drift.

In Figure 6-14, a 400 Hz signal excites the bridge. The signal at the AD8221's input is an ac voltage. Similarly, the signal at the input of the AD630 is ac; the signal is dc at the end of the low-pass filter following the AD630.

The 400 Hz ac signal is rectified and then averaged; dc errors are converted in an ac signal and removed by the AD630. Ultimately, a precision dc signal is obtained.

The AD8221 is well-suited for this application because its high CMRR over frequency ensures that the signal of interest, which appears as a small difference voltage riding on a large sinusoidal common-mode voltage, is gained and the common-mode signal is rejected. In typical instrumentation amplifiers, CMRR falls off at about 200 Hz. In contrast, the AD8221 continues to reject common-mode signals beyond 10 kHz.

If an ac source is not available, a commutating voltage may be constructed using switches. The AD8221's high CMRR over frequency rejects high frequency harmonics from a commutating voltage source.

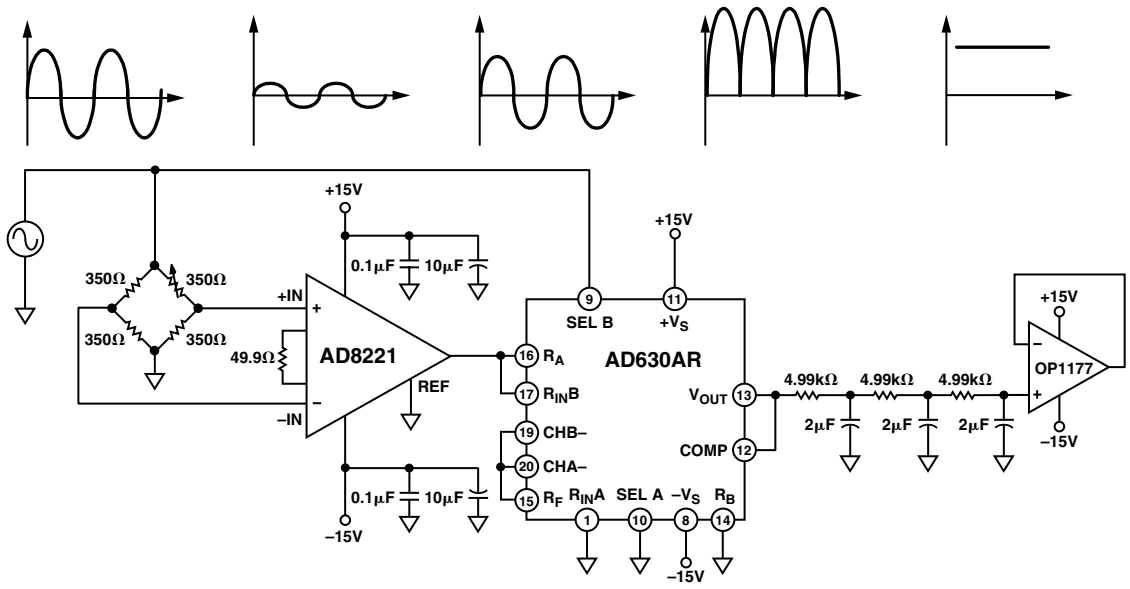



*Figure 6-14. Using an ac signal to excite the bridge.*

## APPLICATIONS OF THE AD628 PRECISION GAIN BLOCK

The AD628 can be operated as either a differential/scaling amplifier or as a pin-strapped precision gain block. Specifically designed for use ahead of an analog-to-digital converter, the AD628 is extremely useful as an input scaling and buffering amplifier. As a differential amplifier, it can extract small differential voltages riding on large common-mode voltages up to ±120 V. As a prepackaged precision gain block, the pins of the AD628 can be strapped to provide a wide range of precision gains, allowing for high accuracy data acquisition with very little gain or offset drift.

The AD628 uses an absolute minimum of external components. Its tiny MSOP provides these functions in the smallest size package available on the market. Besides high gain accuracy and low drift, the AD628 provides a very high common-mode rejection, typically more than 90 dB at 1 kHz while still maintaining a 60 dB CMRR at 100 kHz.

The AD628 includes a $V_{REF}$ pin to allow a dc (midscale) offset for driving single-supply ADCs. In this case, the $V_{REF}$ pin may simply be tied to the ADC's reference pin, which also allows easy ratiometric operation.

### Why Use a Gain Block IC?

Real-world measurement requires extracting weak signals from noisy sources. Even when a differential measurement is made, high common-mode voltages are often present. The usual solution is to use an op amp or, better still, an in-amp, and then perform some type of low-pass filtering to reduce the background noise level.

The problem with this traditional approach is that a discrete op amp circuit will have poor common-mode rejection and its input voltage range will always be less than the power supply voltage. When used with a differential signal source, an in-amp circuit using a monolithic IC will improve common-mode rejection. However, signal sources greater than the power supply voltage, or signals riding on high common-mode voltages, cannot handle standard in-amps. In addition, in-amps using a single external gain resistor suffer from gain drift. Finally, low-pass filtering usually requires the addition of a separate op amp, along with several external components. This drains valuable board space.

The AD628 eliminates these common problems by functioning as a scaling amplifier between the sensor, the shunt resistor, or another point of data acquisition, as well as the ADC. Its 120 V max input range permits the direct measurement of large signals or small signals riding on large common-mode voltages.

### Standard Differential Input ADC Buffer Circuit with Single-Pole LP Filter

Figure 6-15 shows the AD628 connected to accept a differential input signal riding on a very high common-mode voltage. The AD628 gain block has two internal amplifiers: A1 and A2. Pin 3 is grounded, thus operating amplifier A1 at a gain of 0.1. The 100 kΩ input resistors and other aspects of its design allow the AD628 to process small input signals riding on common-mode voltages up to ±120 V.

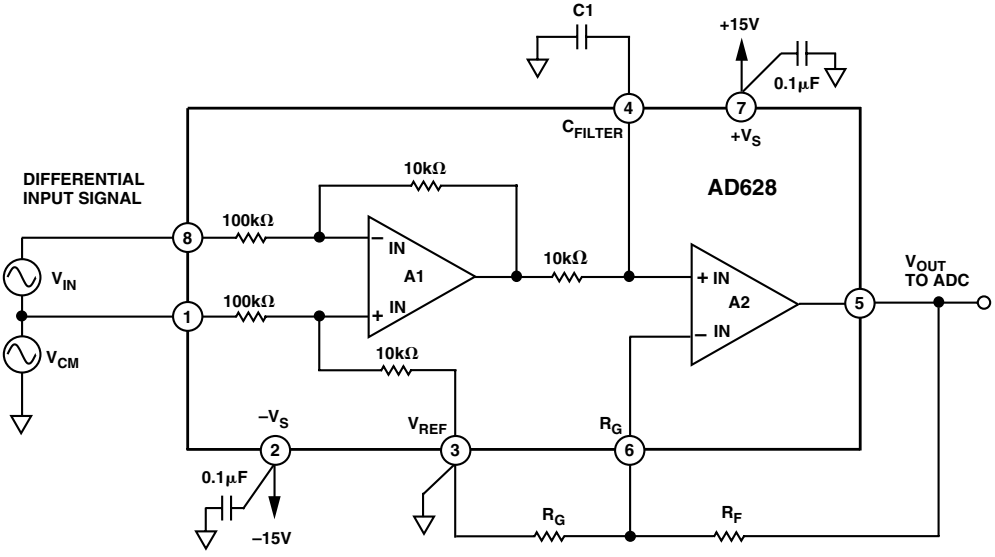



*Figure 6-15. Basic differential input connection with single-pole LP filter.*

The output of A1 connects to the plus input of amplifier A2 through a 10 kΩ resistor. Pin 4 allows connecting an external capacitor to this point, providing single-pole low-pass filtering.

**Changing the Output Scale Factor**

Figure 6-15 reveals that the output scale factor of the AD628 may be set by changing the gain of amplifier A2. This uncommitted op amp may be operated at any convenient gain higher than unity. When configured, the AD628 may be set to provide circuit gains between 0.1 and 1000.

Since the gain of A1 is 0.1, the combined gain of A1 and A2 equals

$$\frac{V_{OUT}}{V_{IN}} = G = 0.1\left(1+\left(R_F/R_G\right)\right)$$

Therefore,

$$(10G-1) = \frac{R_F}{R_G}$$

For ADC-buffering applications, the gain of A2 should be chosen so that the voltage driving the ADC is close to its full-scale input range. The use of external resistors, $R_F$ and $R_G$ to set the output scale factor (i.e., gain of A2) will degrade gain accuracy and drift essentially to the resistors themselves.

A separate $V_{REF}$ pin is available for offsetting the AD628 output signal, so it is centered in the middle of the ADC's input range. Although Figure 6-15 indicates ±15 V, the circuit may be operated from ±2.25 V to ±18 V dual supplies. This $V_{REF}$ pin may also be used to allow single-supply operation; $V_{REF}$ may simply be biased at $V_S/2$.

**Using an External Resistor to Operate the AD628 at Gains Below 0.1**

The AD628 gain block may be modified to provide any desired gain from 0.01 to 0.1, as shown in Figure 6-16.

This connection is the same as the basic wide input range circuit of Figure 6-15, but with Pins 5 and 6 strapped, and with an external resistor, $R_G$, connection between Pin 4 and ground. The pin strapping operates amplifier A2 at unity gain. Acting with the on-chip 10 kΩ resistor at the output of A1, $R_{GAIN}$ forms a voltage divider that attenuates the signal between the output of A1 and the input of A2. The gain for this connection equals 0.1 $V_{IN}$ ((10 kΩ + $R_G$)/$R_G$).

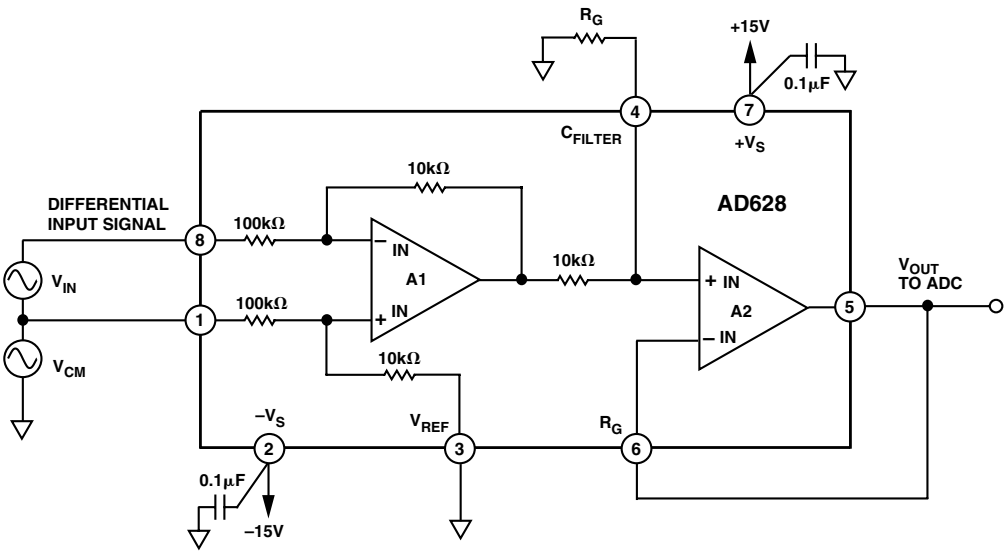



*Figure 6-16. AD628 connection for gains less than 0.1.*

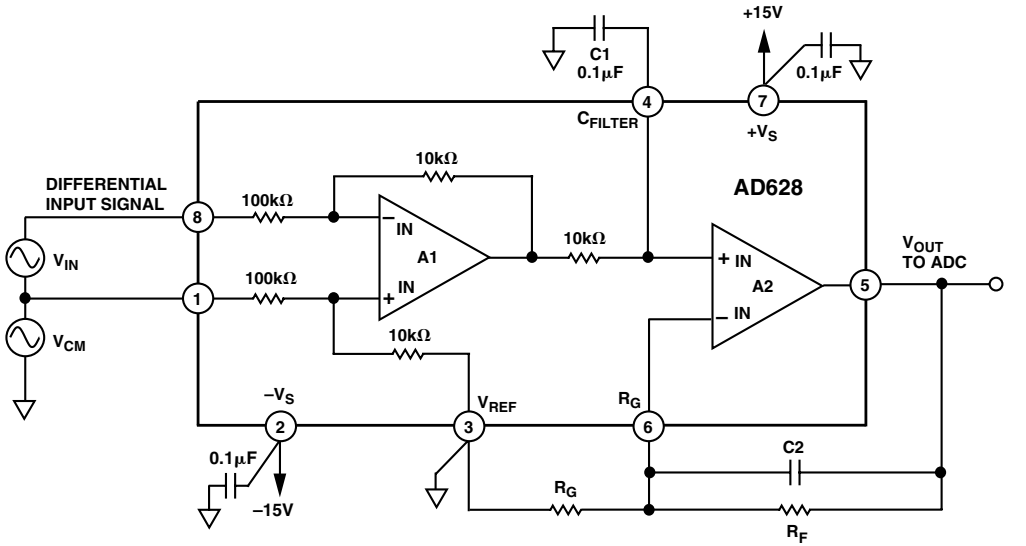



*Figure 6-17. Differential input circuit with 2-pole low-pass filtering.*

**Differential Input Circuit with 2-Pole Low-Pass Filtering**

The circuit in Figure 6-17 is a modification of the basic ADC interface circuit. Here, 2-pole low-pass filtering is added for the price of one additional capacitor (C2).

As before, the first pole of the low-pass filter is set by the internal 10 kΩ resistor at the output of A1 and the external capacitor C1. The second pole is created by an external RC time constant in the feedback path of A2, consisting of capacitor C2 across resistor $R_F$. Note that this second pole provides a more rapid roll-off of frequencies above its RC *corner* frequency ($1/(2\pi RC)$) than a single-pole LP filter. However, as the input frequency is increased, the gain of amplifier A2 eventually drops to unity and will not be further reduced. So, amplifier A2 will have a voltage gain set by the ratio of $R_F/R_G$ at frequencies below its –3 dB corner and will have unity gain at higher frequencies.

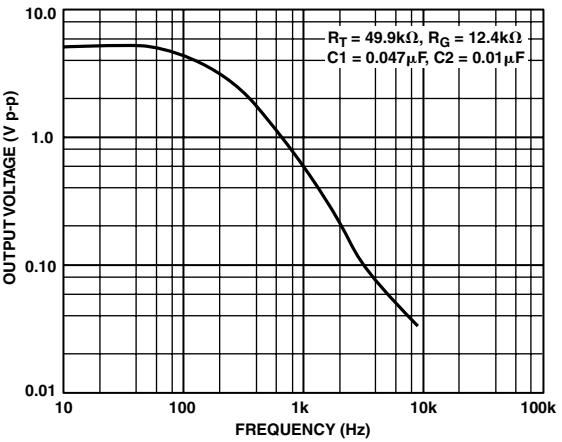



*Figure 6-18. Frequency response of the 2-pole low-pass filter.*

Figure 6-18 shows the filter's output vs. frequency using components chosen to provide a 200 Hz, –3 dB corner frequency. There is a sharp roll-off between the corner frequency and approximately 10× the corner frequency. Above this point, the second pole starts to become less effective, and the rate of attenuation is close to that of a single-pole response.

**Table 6-1.**

2-Pole LP Filter
Input Range: 10 V p-p FS for a 5 V p-p Output
$R_F$ = 49.9 kΩ, $R_G$ = 12.4 kΩ

| –3 dB Corner Frequency | | | | |
|---|---|---|---|---|
| | **200 Hz** | **1 kHz** | **5 kHz** | **10 kHz** |
| Capacitor C2 | 0.01 μF | 0.002 μF | 390 pF | 220 pF |
| Capacitor C1 | 0.047 μF | 0.01 μF | 0.002 μF | 0.001 μF |

**Table 6-2.**

2-Pole LP Filter
Input Range: 20 V p-p FS for a 5 V p-p Output
$R_F$ = 24.3 kΩ, $R_G$ = 16.2 kΩ

| –3 dB Corner Frequency | | | | |
|---|---|---|---|---|
| | **200 Hz** | **1 kHz** | **5 kHz** | **10 kHz** |
| Capacitor C2 | 0.02 μF | 0.0039 μF | 820 pF | 390 pF |
| Capacitor C1 | 0.047 μF | 0.01 μF | 0.002 μF | 0.001 μF |

Tables 6-1 and 6-2 provide typical filter component values for various –3 dB corner frequencies and two different full-scale input ranges. Values have been rounded off to match standard resistor and capacitor values. Capacitors C1 and C2 need to be high Q, low drift devices; low grade disc ceramics should be avoided. High quality NPO ceramic, Mylar, or polyester film capacitors are recommended for the lowest drift and best settling time.

**Using the AD628 to Create Precision Gain Blocks**
Real-world data acquisition systems require amplifying weak signals enough to apply them to an ADC. Unfortunately, when configured as gain blocks, most common amplifiers have both gain errors and offset drift.

In op amp circuits, the usual two-resistor gain setting arrangement has accuracy and drift limitations. Using standard 1% resistors, amplifier gain can be off by 2%. The gain will also vary with temperature because each resistor will drift differently. Monolithic resistor networks can be used for precise gain setting, but these components increase cost, complexity, and board space.

The gain block circuits of Figures 6-19 to 6-23 overcome all of these performance limitations, are very inexpensive, and offer a single MSOP solution. The AD628 provides this complete function using the smallest IC package available. Since all resistors are internal to the AD628 gain block, both accuracy and drift are excellent.

All of these pin-strapped circuits (using no external components) have a gain accuracy better than 0.2%, with a gain TC better than 50 ppm/°C.

**Operating the AD628 as a +10 or –10 Precision Gain Block**
Figure 6-19 shows an AD628 precision gain block IC connected to provide a voltage gain of +10. The gain block may be configured to provide different gains by strapping or grounding the appropriate pin. The gain block itself consists of two internal amplifiers: a gain of 0.1 difference amplifier (A1) followed by an uncommitted buffer amplifier (A2).

The input signal is applied between the $V_{REF}$ pin (Pin 3) and ground. With the input tied to Pin 3, the voltage at the positive input of A1 equals $V_{IN}$ (100 kΩ/110 kΩ), which is $V_{IN}$ (10/11). With Pin 6 grounded, the minus

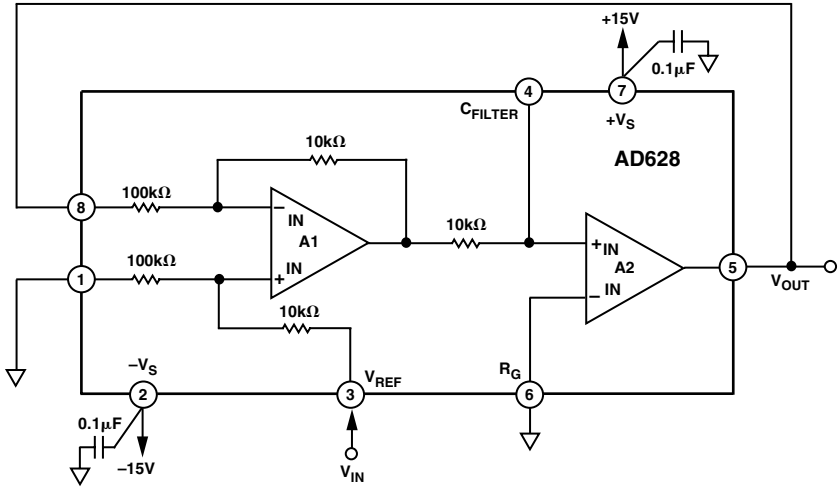



*Figure 6-19. Circuit with a gain of +10 using no external components.*

input of A2 equals 0 V. Therefore, the positive input of A2 will be forced by feedback from the output of A2 to be 0 V as well. The output of A1 then must also be at 0 V. Since the negative input of A1 must be equal to the positive input of A1, both will equal $V_{IN}$ (10/11).

This means that the output voltage of A2 ($V_{OUT}$) will equal

$$V_{OUT} = V_{IN}\,(10/11)\,(1+100\text{k}/10\text{k}) =$$
$$V_{IN}\,(10/11)\,11 = 10\,V_{IN}$$

The companion circuit in Figure 6-20 provides a gain of –10. This time the input is applied between the negative input of A2 (Pin 6) and ground. Operation is exactly the same, but now the input signal is inverted 180° by A2. With Pin 3 grounded, the positive input of A1 is at 0 V, so feedback will force the negative input of A1 to zero as well. Since A1 operates at a gain of 1/10 (0.1), the output of A2 that is needed to force the negative input of A1 to zero is *minus* 10 $V_{IN}$.

The two connections will have different input impedances. When driving Pin 3 (Figure 6-19), the input impedance to ground is 110 kΩ, while it is approximately 50 GΩ when driving Pin 6 (Figure 6-20). The –3 dB bandwidth for both circuits is approximately 110 kHz for 10 mV and 95 kHz for 100 mV input signals.

**Operating the AD628 at a Precision Gain of +11**

The gain of +11 circuit (Figure 6-21) is almost identical to the gain of +10 connection, except that Pin 1 is strapped to Pin 3, rather than being grounded. This connects the two internal resistors (100 kΩ and 10 kΩ)

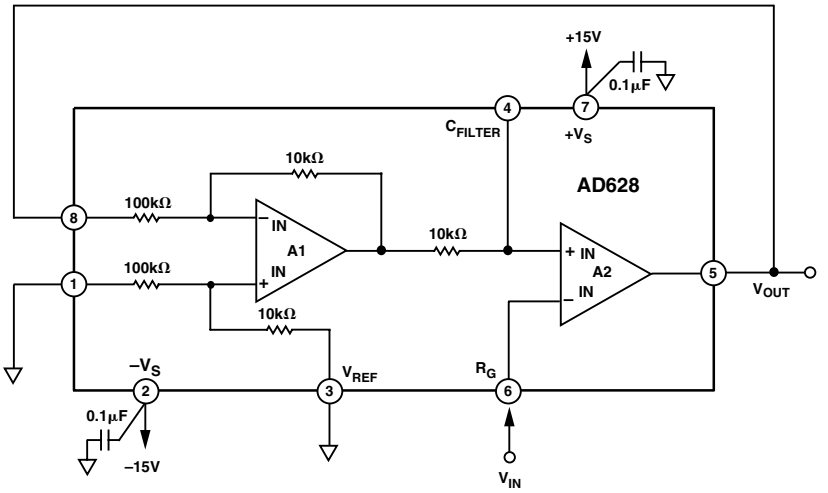



*Figure 6-20. Companion circuit providing a gain of –10.*

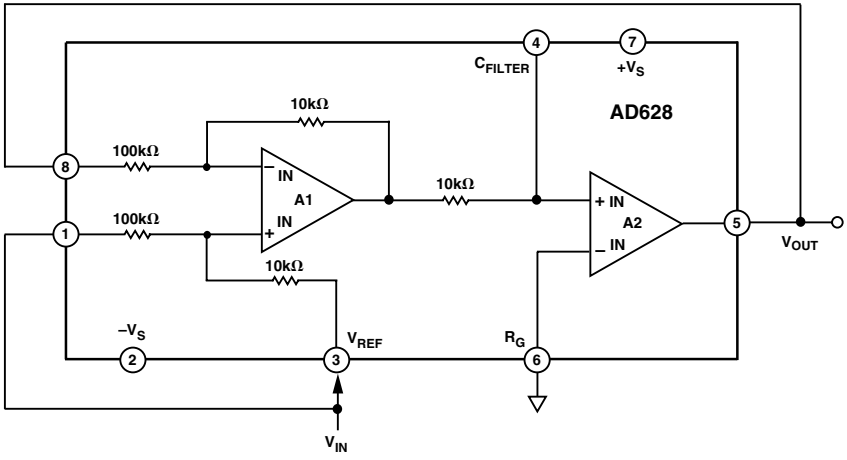



*Figure 6-21. A gain of +11 circuit.*

that are tied in parallel to the plus input of A1. So, this now removes the 10 kΩ/110 kΩ voltage divider between $V_{IN}$ and the positive input of A1. Thus modified, $V_{IN}$ drives the positive input through approximately a 9 kΩ resistor. Note that this series resistance is negligible compared to the very high input impedance of amplifier A1. The gain from Pin 8 to the output of A1 is 0.1. Therefore, feedback will force the output of A2 to equal 10 $V_{IN}$. The –3 dB bandwidth of this circuit is approximately 105 kHz for 10 mV and 95 kHz for 100 mV input signals.

**Operating the AD628 at a Precision Gain of +1**

Figure 6-22 shows the AD628 connected to provide a precision gain of +1. As before, this connection uses the gain block's internal resistor networks for high gain accuracy and stability.

The input signal is applied between the $V_{REF}$ pin and ground. Because Pins 1 and 8 are grounded, the input signal runs through a 100 kΩ/110 kΩ input attenuator to the plus input of A1. The voltage equals $V_{IN}$ (10/11) = 0.909 $V_{IN}$. The gain from this point to the output of A1 will equal 1 + (10 kΩ/100 kΩ) = 1.10. Therefore, the voltage at the output of A1 will equal $V_{IN}$ (1.10) (0.909) = 1.00. Amplifier A2 is operated as a unity-gain buffer (as Pins 5 and 6 tied together), providing an overall circuit gain of +1.

**Increased BW Gain Block of –9.91 Using Feedforward**

The circuit of Figure 6-20 can be modified slightly by applying a small amount of positive feedback to increase its bandwidth, as shown in Figure 6-23. The output of amplifier A1 feeds back its positive input by connecting Pin 4 and Pin 1 together. Now, Gain = –(10 – 1/11) = –9.91.

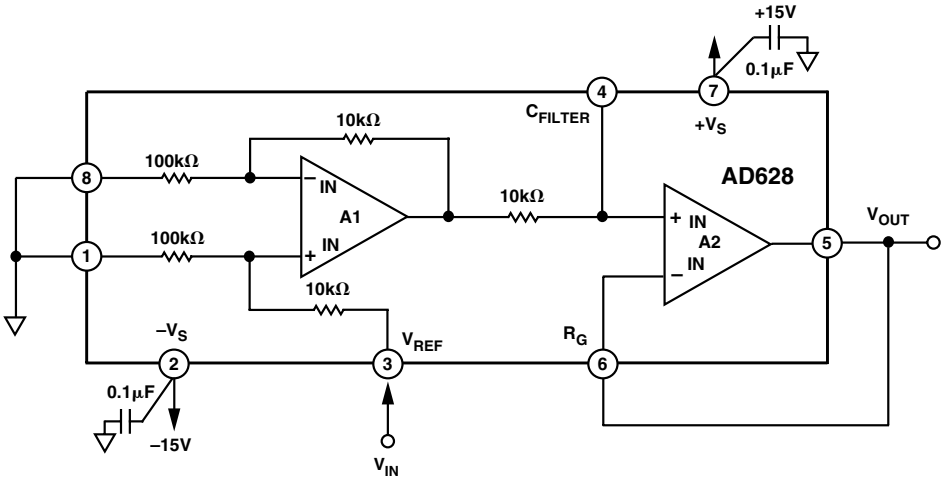



*Figure 6-22. AD628 precision gain of +1.*

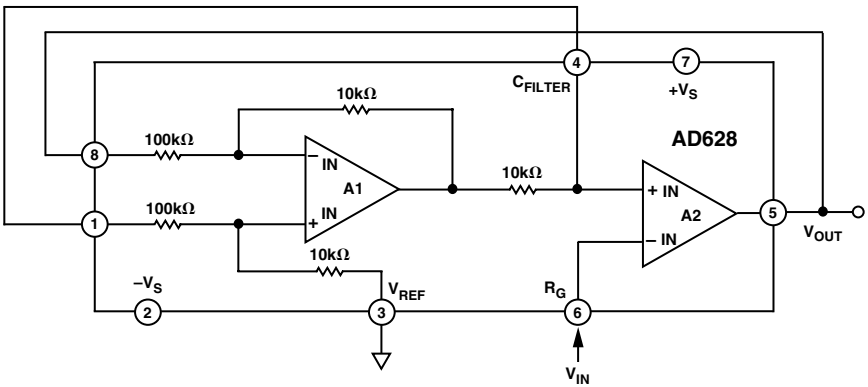



*Figure 6-23. Precision –10 gain block with feedforward.*

The resulting circuit is still stable because of the large amount of negative feedback applied around the entire circuit (from the output of A2 back to the negative input of A1). This connection actually results in a small signal –3 dB bandwidth of approximately 140 kHz. This is a 27% increase in bandwidth over the unmodified circuit in Figure 6-17. However, gain accuracy is reduced to ±2%.

## CURRENT TRANSMITTER REJECTS GROUND NOISE

Many systems use current flow to control remote instrumentations. The advantage of such a system is its ability to operate with two remotely connected power supplies, even if their grounds are not the same. In such cases, it is necessary for the output to be linear with respect to the input signal, and any interference between the grounds must be rejected. Figure 6-24 shows such a circuit.

For this circuit,

$$I_{OUT} = \frac{(V_{IN}/10)}{1\text{k}\Omega}$$

$$I_{OUT} = \frac{V_{IN}(\text{V})}{1\text{k}\Omega}$$

The AD629, a difference amplifier with very high common-mode range, is driven by an input signal Pin 3. Its transfer function is

$$V_{OUT} = V_{IN}$$

where:

$V_{OUT}$ is measured between Pin 6 and its reference (Pin 1 and Pin 5), and the input $V_{IN}$ is measured between Pin 3 and Pin 2. The common-mode signal, VCM, will be rejected.

In order to reduce the voltage at Pin 6, an inverter with a gain of 9 is connected between Pin 6 and its reference. The inverter sets the gain of the transmitter such that for a 10 V input, the voltage at Pin 6 only changes by 1 V; yet, the difference between Pin 6 and its reference is 10 V.

Since the gain between the noninverting terminal of the **OP27** and the output of the AD629 is 1, no modulation of the output current will take place as a function of the output voltage $V_{OUT}$. The scaling resistor R3 is 100 Ω to make 1 mA/V of input signal.

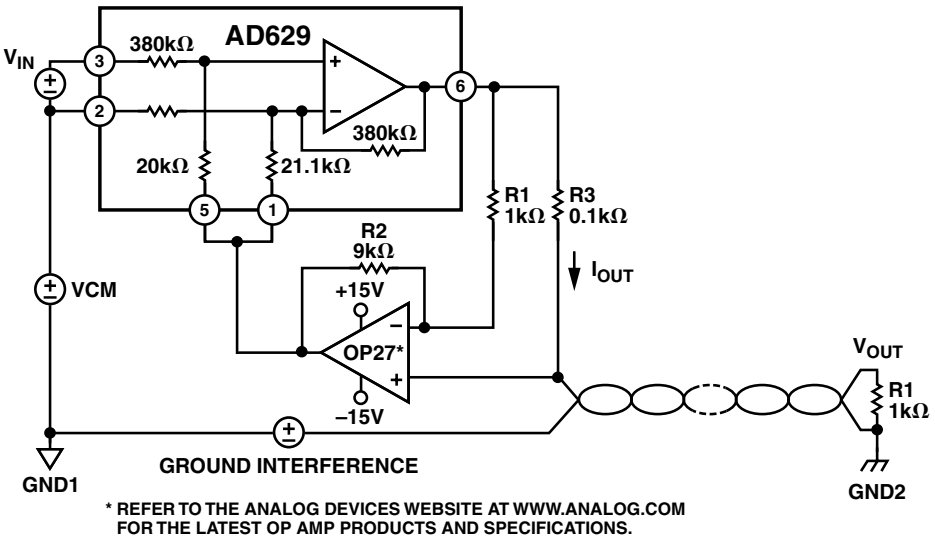



*Figure 6-24. Current transmitter.*

OP27 was chosen because, at a noise gain of 10, its bandwidth does not compromise the transmitter. Figure 6-25 is the transfer function of the output voltage $V_{OUT}$ vs. the input voltage $V_{IN}$. Figure 6-26 is a demonstration of how well the transmitter rejects ground noise.

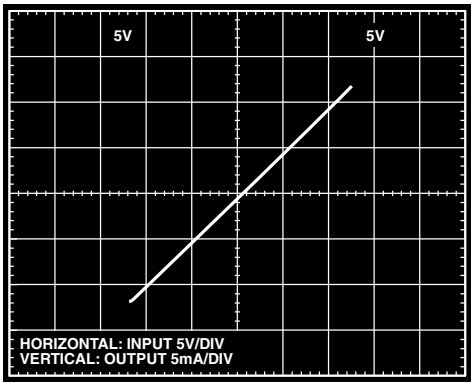



*Figure 6-25. Transfer function.*

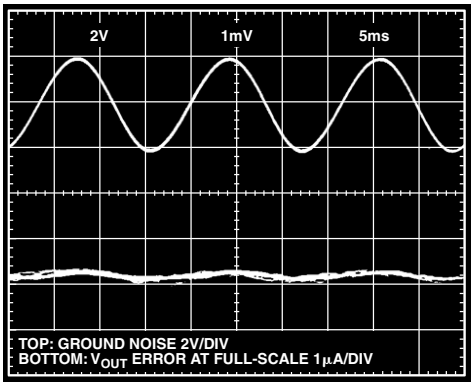



*Figure 6-26. Interference rejection.*

## HIGH LEVEL ADC INTERFACE

The circuit of Figure 6-27 provides an interface between large level analog inputs as high as ±10 V operating on dual supplies and a low level, differential input ADC, operating on a single supply.

As shown, two AD628 difference amplifiers are connected in antiphase. The differential output, $V_1 - V_2$, is an attenuated version of the input signal

$$V_1 - V_2 = \frac{(V_A - V_B)}{5}$$

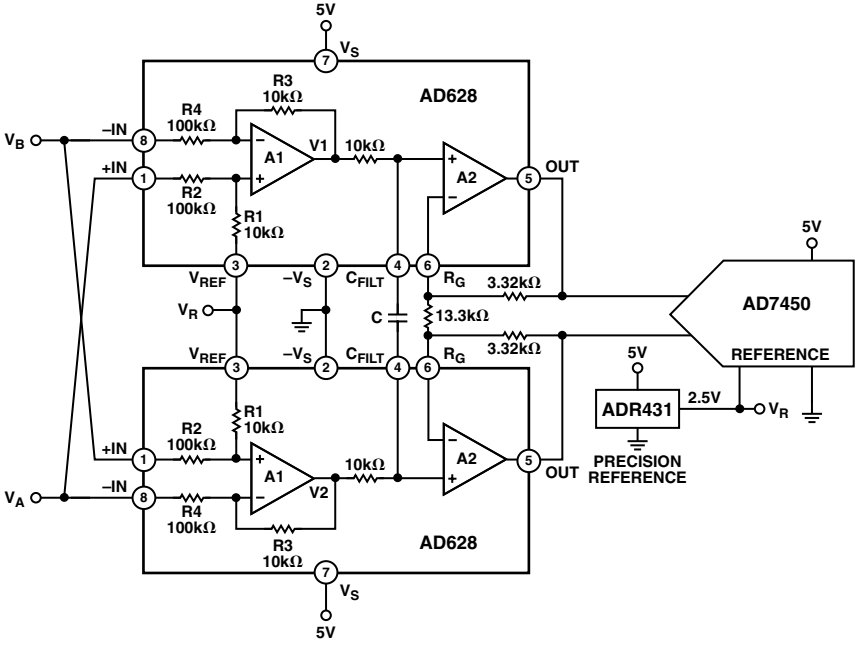



*Figure 6-27. This ADC interface circuit attenuates and level shifts a ± 10 V differential signal while operating from a single 5 V supply.*

The difference amplifiers reject the common-mode voltage on inputs $V_A$ and $V_B$. The reference voltage, $V_R$, which the **ADR431** develops and the ADC and the amplifier share, sets the output common-mode voltage. A single capacitor, C, placed across the $C_{FILT}$ pins low-pass filters the difference signal, $V_1 - V_2$. The –3 dB pole frequency is $f_P = 1/(40{,}000 \times \pi \times C)$. The difference signal is amplified by 1.5. Thus, the total gain of this circuit is 3/10.

Figure 6-28 shows a 10 V input signal (top), the signals at the output of each AD628 (middle), and the differential output (bottom). The benefits of this configuration go beyond simply interfacing with the ADC. The circuit improves specifications such as common-mode rejection ratio, offset voltage, drift, and noise by a factor of $\sqrt{2}$ because the errors of each AD628 are not correlated.

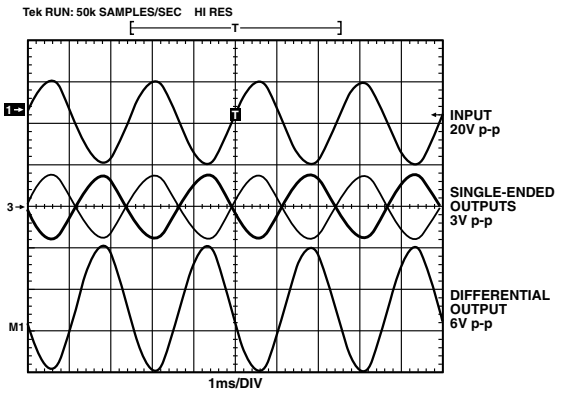



*Figure 6-28. The waveforms show a 10 V input signal (top), the signals at the output of each AD628 (middle), and the differential output (bottom).*

The output demonstrates an 85 dB SNR (Figure 6-29). The two AD628s interface with an **AD7450** 12-bit, differential-input ADC. The AD7450 easily rejects residual common-mode signals at the output of the difference amplifiers. Figure 6-30 shows the common-mode error at the output of the AD628.

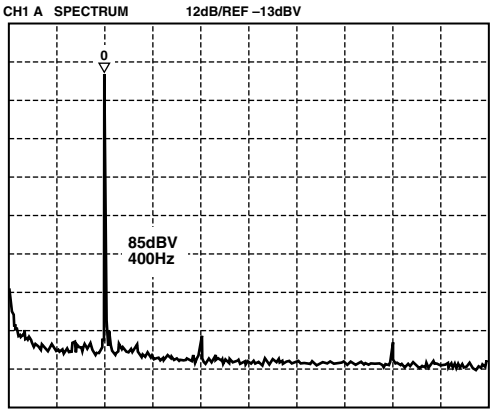



*Figure 6-29. The circuit in Figure 6-27 has an 85 dBV SNR.*

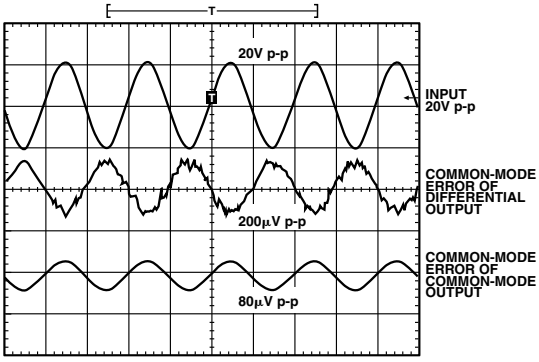



*Figure 6-30. The common-mode input (top) measures 20 V p-p. The common-mode error of the differential output (middle) is 20 μV p-p. The error of the common-mode output (bottom) is 80 μV p-p.*

The topmost waveform is a 10 V, common-mode input signal. The middle waveform, measuring 150 μV, is the common-mode error measured differentially from the output of the two AD628s. The bottom waveform, measuring 80 μV, is the common-mode error that results.

**A HIGH SPEED NONINVERTING SUMMING AMPLIFIER**

The schematic in Figure 6-31 is that of a common summing amplifier with multiple inputs and one single-ended output. It is a variation of an inverting amplifier. Point X is a virtual ground and referred to as a summing junction. The transfer function for this circuit is

$$V_O = -\left[(RF/R1)V1 + (RF/R2)V2 + (RF/R3)V3\right]$$

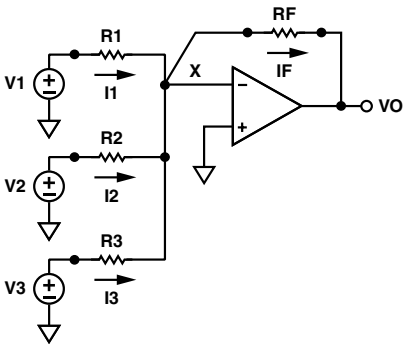



*Figure 6-31. A traditional summing amplifier.*

This indicates that the output is a weighted sum of the inputs, with the weights being determined by the resistance ratio. If all resistances are equal, the circuit yields the inverted sum of its inputs.

$$V_O = -(V1 + V2 + V3)$$

Note that if we want the result $V_O = (V1 + V2 + V3)$, we need an additional inverter with gain = –1. Furthermore, this circuit has many disadvantages, such as a low input impedance, plus different impedances for positive and negative inputs. It requires low bandwidth, and highly matched resistors are needed.

Figure 6-32 is the schematic of a high speed summing amplifier, which can sum up as many as four input voltages without the need for an inverter to change the sign of the output. This could prove very useful in audio and video applications. The circuit contains three, low cost, high speed instrumentation amplifiers. The first two interface with input signals, and their total sum is taken at the third amplifier's output with respect to ground. The inputs are very high impedance, and the signal that appears at the network output is noninverting.

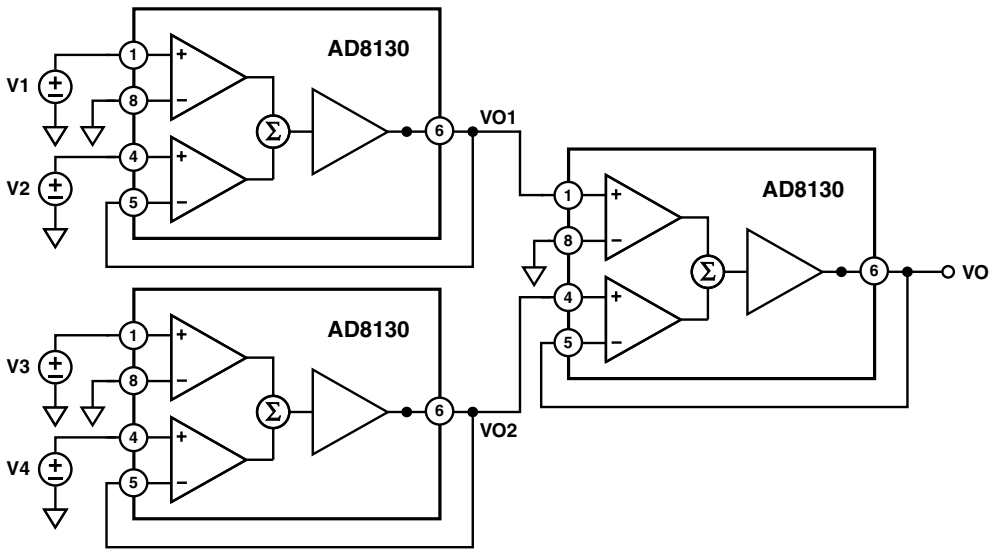



*Figure 6-32. A summing circuit with high input impedance.*

Figure 6-33 is the performance photo at 1 MHz. The top trace is the input signal for all four inputs. The middle trace is the sum of inputs V1 and V2. The bottom trace is the output of the system, which is the total sum of all four inputs.

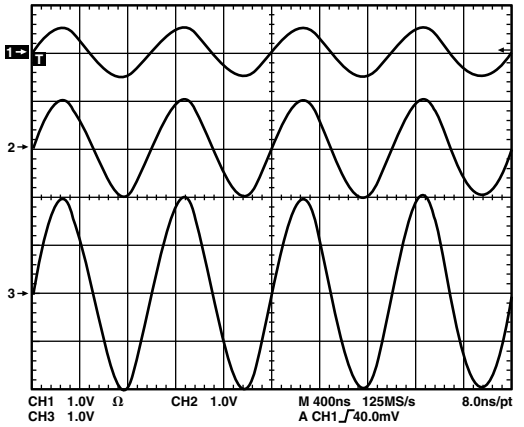



*Figure 6-33. Performance photo of the circuit in Figure 6-32.*

Figure 6-34 demonstrates the high bandwidth of the system in Figure 6-32. As we can see, the –3 dB point is about 220 MHz.

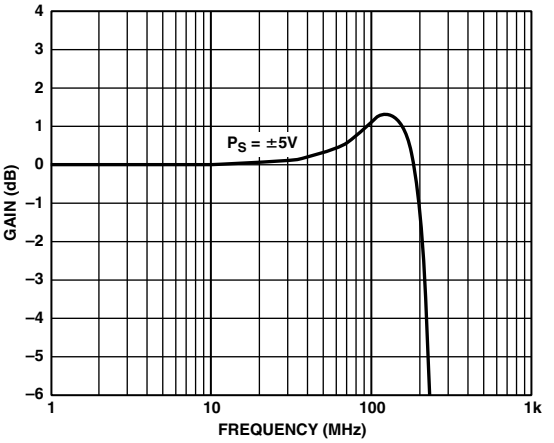
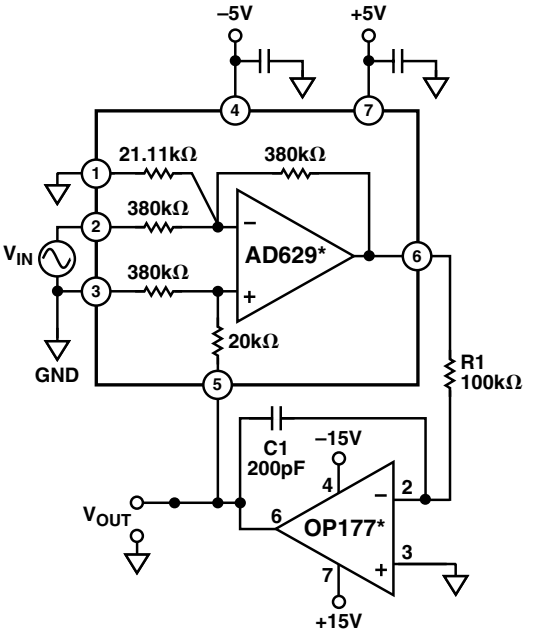



*Figure 6-34. Frequency response of summing circuit in Figure 6-32.*

## HIGH VOLTAGE MONITOR

A high accuracy, high voltage monitor is shown in Figure 6-35.




*** REFER TO THE ANALOG DEVICES WEBSITE AT WWW.ANALOG.COM FOR THE LATEST OP AMP PRODUCT NUMBERS AND SPECIFICATIONS.**

*Figure 6-35. High voltage monitor.*

An integrator (**OP177**) supplies negative feedback around a difference amplifier (AD629), forcing its output to stay at 0 V. The voltage divider on the inverting input sets the common-mode voltage of the difference amplifier to $V_{IN}/20$. $V_{OUT}$, the integrator output and the measurement output, sources the required current to maintain the common-mode voltage. R1 and C1 compensate the system to a bandwidth of 200 kHz.

The transfer function is $V_{OUT} = V_{IN}/19$. For example, a 400 V p-p input signal will produce a 21 V p-p output.

Figure 6-36 shows that the measured system nonlinearity is less than 20 ppm over the entire 400 V p-p input range. System noise is about 550 nV/√Hz referred to the input, or around 2 mV peak noise voltage (10 ppm of full scale) over a 300 kHz bandwidth.

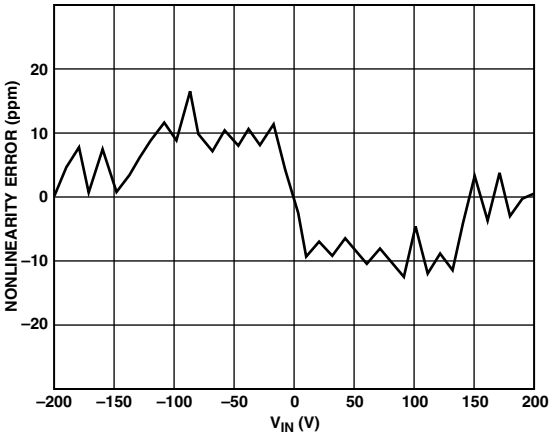



*Figure 6-36. Nonlinearity vs. $V_{IN}$.*

## PRECISION 48 V BUS MONITOR

Telephone equipment power supplies normally consist of a 48 V dc power source and an array of batteries. The batteries provide backup power during ac power line outages and help regulate the 48 V dc supply voltage.

Although nominally –48 V, the dc voltage on the telephone lines can vary anywhere from –40 V to –80 V and is subject to surges and fluctuations. Supply regulation at the source has little effect on remote voltage levels, and equipment failures resulting from surges, brownouts, or other line faults may not always be detected.

Capturing power supply information from remote communications equipment requires precise measurement of the voltages, sometimes under outdoor temperature conditions. High common-mode voltage difference amplifiers have been used to monitor current. However, these versatile components can also be used as voltage dividers, enabling remote monitoring of voltage levels as well.

Figure 6-37 shows a precision monitor using just two integrated circuits that derives its power from the –48 V supply. A low cost transistor and Zener diode combination provide 15 V supply voltage for the amplifiers.

The AD629 IC is a self-contained, high common-mode voltage difference amplifier. Connected as shown, it reduces the differential input voltage by approximately 19 V, thus acting as a precision voltage divider. An additional amplifier is required for loop stability.

The output from the **OP777AR** drives an **AD7476** ADC.

The circuit features several advantages over alternative solutions. The AD629's laser-trimmed divider resistors exhibit essentially perfect matching and tracking over temperature. Linearity errors from –40 V to –80 V are nearly immeasurable. Figures 6-38 and 6-39 are linearity and temperature drift curves for this circuit.

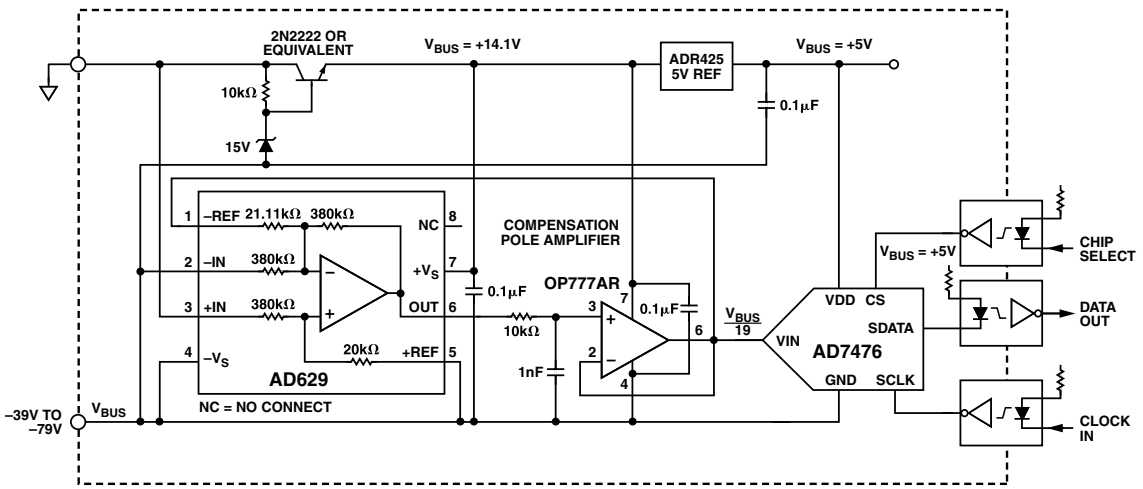



*Figure 6-37. Precision remote voltage measurement of –48 V power distribution bus.*

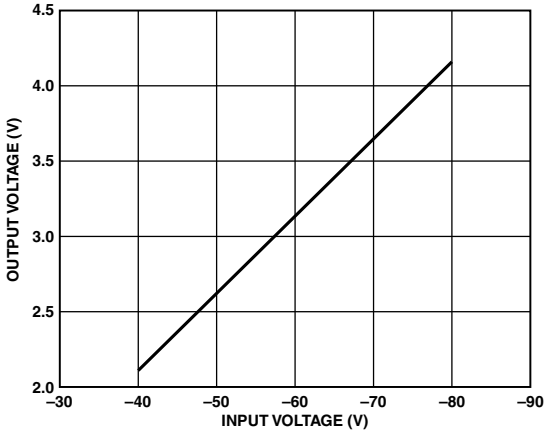



*Figure 6-38. Output vs. input linearity for the circuit of the 48 V bus monitor.*

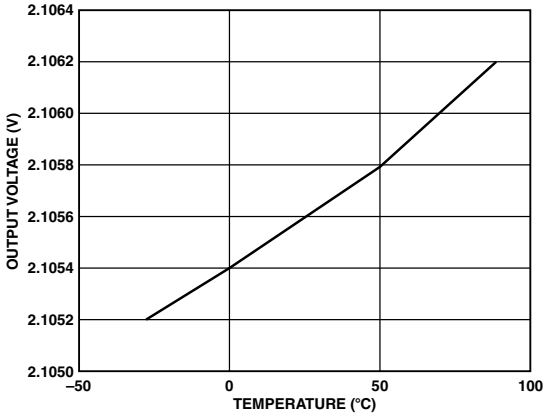



*Figure 6-39. Temperature drift of the 48 V bus monitor.*

## HIGH-SIDE CURRENT SENSE WITH A LOW-SIDE SWITCH

A typical application for the AD8202 is high-side measurement of a current through a solenoid for PWM control of the solenoid opening. Typical applications include hydraulic transmission control and diesel injection control.

Two typical circuit configurations are used for this type of application.

In this case, the PWM control switch is ground referenced. An inductive load (solenoid) is tied to a power supply. A resistive shunt is placed between the switch and the load (see Figure 6-40). An advantage of placing the shunt on the high side is that the entire current, including the recirculation current, can be measured, since the shunt remains in the loop when the switch is off. In addition, diagnostics can be enhanced because shorts to ground can be detected with the shunt on the high side.

In this circuit configuration, when the switch is closed, the common-mode voltage moves down to near the negative rail. When the switch is opened, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop above the battery by the clamp diode.

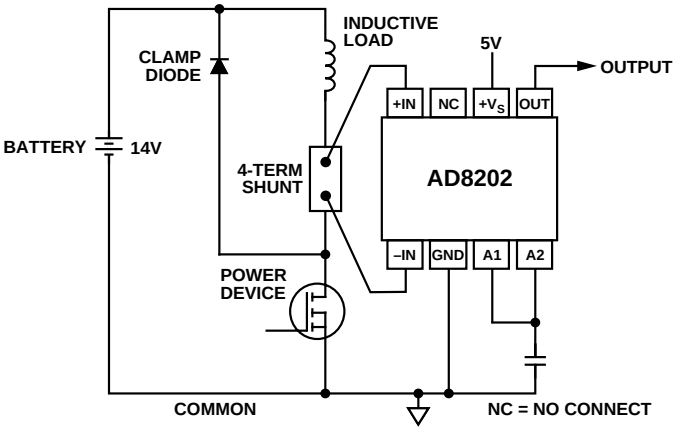



*Figure 6-40. Low-side switch.*

## HIGH-SIDE CURRENT SENSE WITH A HIGH-SIDE SWITCH

This configuration minimizes the possibility of unexpected solenoid activation and excessive corrosion (see Figure 6-41). In this case, both the switch and the shunt are on the high side. When the switch is off, this removes the battery from the load, which prevents damage from potential shorts to ground while still allowing the recirculating current to be measured and providing for diagnostics. Removing the power supply from the load for the majority of the time minimizes the corrosive effects that could be caused by the differential voltage between the load and ground.

When using a high-side switch, the battery voltage is connected to the load when the switch is closed, causing the common-mode voltage to increase to the battery voltage. In this case, when the switch is opened, the voltage reversal across the inductive load causes the common-mode voltage to be held one diode drop below ground by the clamp diode.

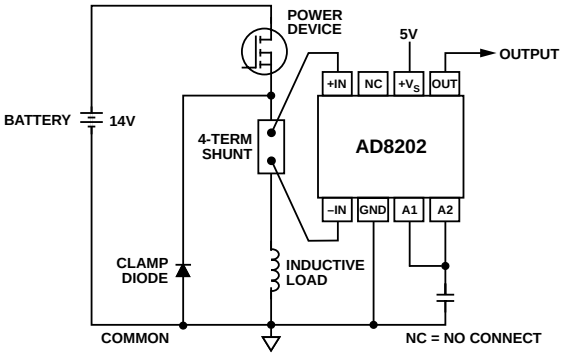



*Figure 6-41. High-side switch.*

### Motor Control

A typical application for the AD8210 is as part of the control loop in H-bridge motor control. In this case, the AD8210 is placed in the middle of the H-bridge (see Figure 6-42) so that it can accurately measure current in both directions by using the shunt available at the motor. This is a better solution than a ground referenced op amp because ground is not typically a stable reference voltage in this type of application. This instability in the ground reference causes the measurements that could be made with a simple ground referenced op amp to be inaccurate.

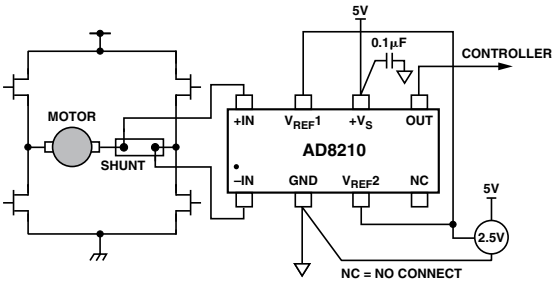



*Figure 6-42. Motor control application.*

The AD8210 measures current in both directions as the H-bridge switches and the motor changes direction. The output of the AD8210 is configured in an external reference bidirectional mode.

## BRIDGE APPLICATIONS

Instrumentation amplifiers are widely used for buffering and amplifying the small voltage output from transducers that make use of the classic 4-resistor Wheatstone bridge.

### A Classic Bridge Circuit

Figure 6-43 shows the AD627 configured to amplify the signal from a classic resistive bridge. This circuit will work in either dual- or single-supply mode. Typically, the bridge will be excited by the same voltage used to power the in-amp. Connecting the bottom of the bridge to the negative supply of the in-amp (usually either 0, –5 V, –12 V, or –15 V) sets up an input common-mode voltage that is optimally located midway between the supply voltages. It is also appropriate to set the voltage on the REF pin to midway between the supplies, especially if the input signal will be bipolar. However, the voltage

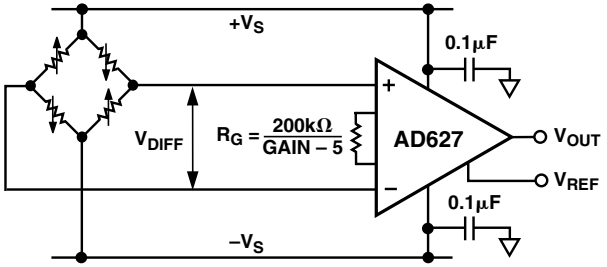



*Figure 6-43. A classic bridge circuit for low power applications.*

on the REF pin can be varied to suit the application. A good example of this is when the REF pin is tied to the $V_{REF}$ pin of an analog-to-digital converter (ADC) whose input range is ($V_{REF} \pm V_{IN}$). With an available output swing on the AD627 of ($-V_S$ + 100 mV) to ($+V_S$ – 150 mV), the maximum programmable gain is simply this output range divided by the input range.

**A Single-Supply Data Acquisition System**

The bridge circuit of Figure 6-44 is excited by a +5 V supply. The full-scale output voltage from the bridge (±10 mV), therefore, has a common-mode level of 2.5 V. The AD623 removes the common-mode voltage component and amplifies the input signal by a factor of 100 ($R_{GAIN}$ = 1.02 kΩ). This results in an output signal of ±1 V.

In order to prevent this signal from running into the AD623's ground rail, the voltage on the REF pin has to be raised to at least 1 V. In this example, the 2 V reference voltage from the **AD7776** ADC is used to bias the AD623's output voltage to 2 V ± 1 V. This corresponds to the input range of the ADC.

**A Low Dropout Bipolar Bridge Driver**

The **AD822** can be used for driving a 350 Ω Wheatstone bridge. Figure 6-45 shows one-half of the AD822 being used to buffer the **AD589**, a 1.235 V low power reference. The output of +4.5 V can be used to drive an A/D converter front end. The other half of the AD822 is configured as a unity-gain inverter and generates the other bridge input of –4.5 V.

Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor, $R_G$, and determined by

$$G = \frac{49.4\,\text{k}\Omega}{R_G} + 1$$

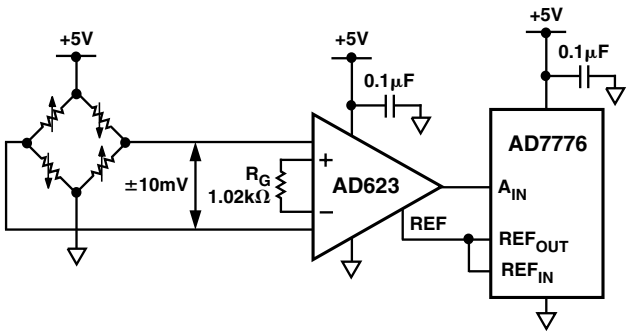



*Figure 6-44. A single-supply data acquisition system.*

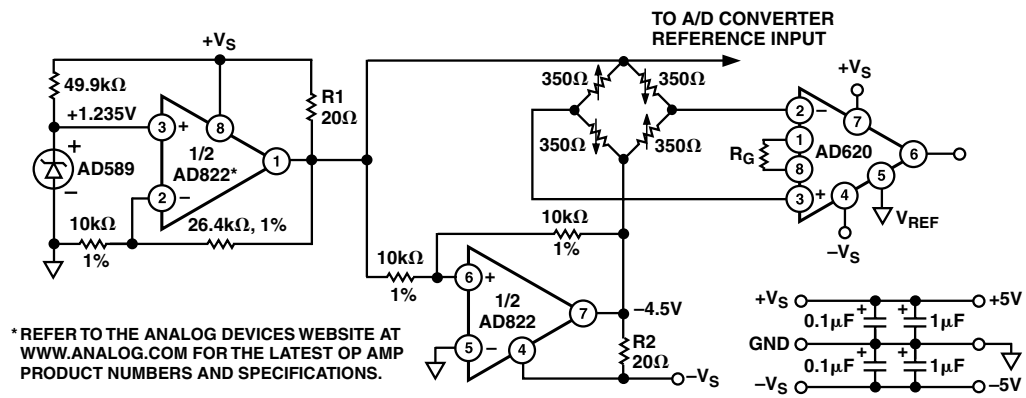



*Figure 6-45. Low dropout bipolar bridge driver.*

## TRANSDUCER INTERFACE APPLICATIONS

Instrumentation amplifiers have long been used as preamplifiers in transducer applications. High quality transducers typically provide a highly linear output, but at a very low level and a characteristically high output impedance. This requires the use of a high gain buffer/preamplifier that will not contribute any discernible noise of its own to that of the signal. Furthermore, the high output impedance of the typical transducer may require that the in-amp have a low input bias current.

Table 6-3 gives typical characteristics for some common transducer types.

Since most transducers are slow, bandwidth requirements of the in-amp are modest: A 1 MHz small signal bandwidth at unity gain is adequate for most applications.

## ELECTROCARDIOGRAM SIGNAL CONDITIONING

The AD8220 makes an excellent input amplifier for next generation ECGs. Its small size, high CMRR over frequency, rail-to-rail output, and JFET inputs are well-suited for this application. Potentials measured on the skin range from 0.2 mV to 2 mV. The AD8220 solves many of the typical challenges of measuring these body surface potentials. The AD8220's high CMRR helps reject common-mode signals that come in the form of line noise or high frequency EMI from equipment in the operating room. Its rail-to-rail output offers wide dynamic range allowing for higher gains than would be possible using other instrumentation amplifiers. JFET inputs offer a large input capacitance of 5 pF. A natural RC filter is formed reducing high frequency noise when series input resistors are used in front of the AD8220 (see the RF Interference section (Reducing RFI Rectification Errors in In-Amp Circuits), Chapter 5). In addition, the AD8220 JFET inputs have ultralow input bias current and no current noise, making it useful for ECG applications where there are often large impedances. The MSOP package and the AD8220's optimal pinout allow smaller footprints and more efficient layout, paving the way for next generation portable ECGs.

Figure 6-46 shows an example of an ECG schematic. Following the AD8220 is a 0.03 Hz, high-pass filter, formed by the 4.7 μF capacitor and the 1 MΩ resistor, which removes the dc offset that develops between the electrodes. An additional gain of 50, provided by the **AD8618**, makes use of the 0 V to 5 V input range of the ADC. An active, fifth-order, low-pass Bessel filter removes signals greater than approximately 160 Hz. An **OP2177** buffers, inverts, and gains the common-mode voltage taken at the midpoint of the AD8220 gain setting resistors. This right leg drive circuit helps cancel common-mode signals by inverting the common-mode signal and driving it back into the body. A 499 kΩ series resistor at the output of the OP2177 limits the current driven into the body.

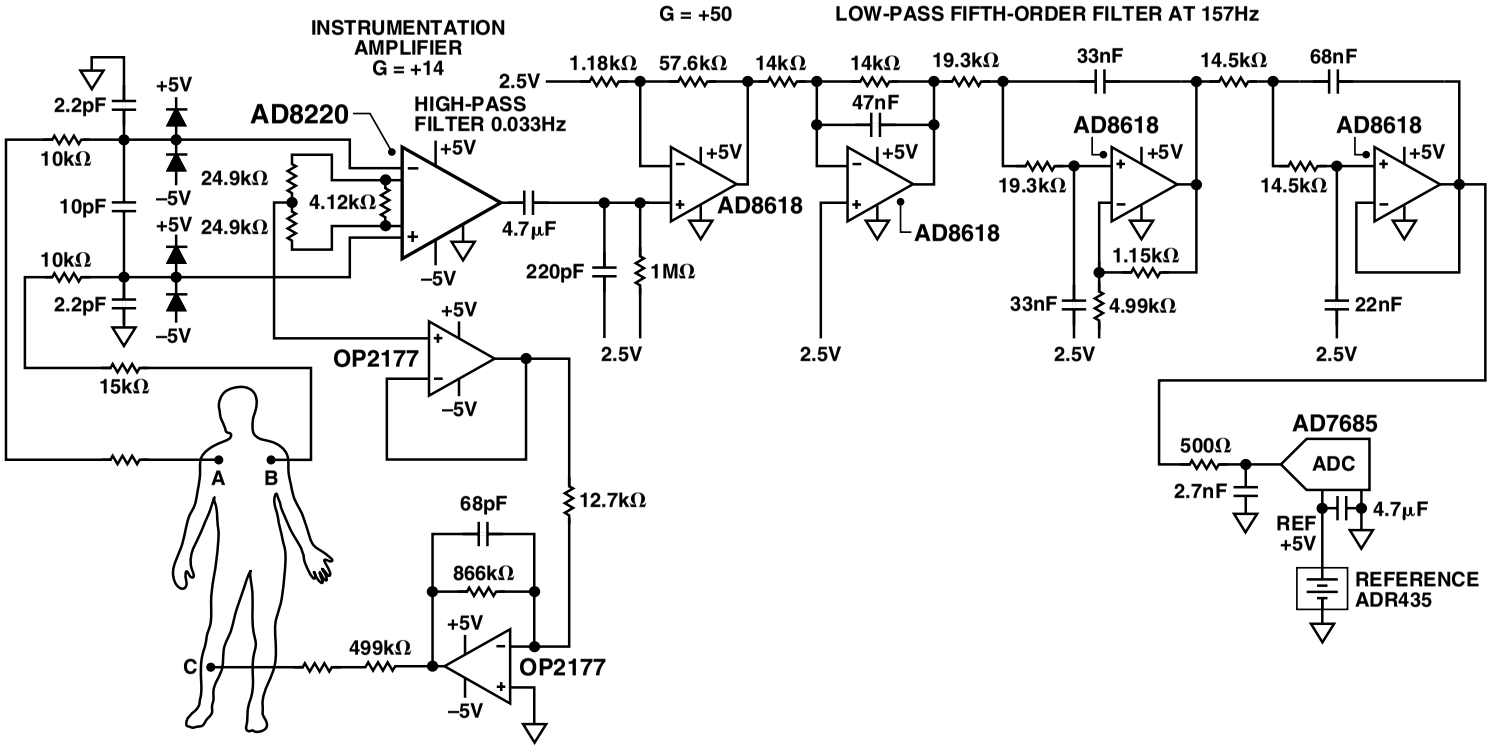



*Figure 6-46. An example of an ECG schematic.*

**Table 6-3. Typical Transducer Characteristics**

| Transducer Type | Type of Output | Output Z | Recommended ADI In-Amp/Diff Amp |
|---|---|---|---|
| Thermistor | Resistance changes with temperature (–TC), 4%/°C @ +25°C, high nonlinear output, single-supply | 50 Ω to 1 MΩ @ +25°C | AD620, AD621, AD623, AD627, AD629, AD8221, AD8225 |
| Thermocouple | Low source Z, 10 μV/°C to 100 μV/°C, mV output level @ +25°C single-supply | 20 Ω to 20 kΩ (10 Ω typ) | AD620, AD621, AD623, AD627, AD8221, AD8222, AD8230 |
| Resistance Temperature Detector (RTD) (In Bridge Circuit) | Low source Z with temperature (+TC), 0.1%/°C to 0.66%/°C, single- or dual-supply | 20 Ω to 20 kΩ @ 0°C | AD620, AD621, AD623, AD627, AD8221, AD8225, AD8230, AD8250, AD8251, AD8555, AD8556 |
| Level Sensors<br>Thermal Types<br>Float Types | Thermistor output (low), variable resistance, output of mV to several volts, single-supply | 500 Ω to 2 kΩ<br>100 Ω to 2 kΩ | AD626, AD628, AD629, AD8225, AD8553 |
| Load Cell (Strain Gage Bridge) (Weight Measurement) | Variable resistance, 2 mV/V of excitation, 0.1% typical full-scale change, single- or dual-supply | 120 Ω to 1 kΩ | AD620, AD621, AD8221, AD8222, AD8225, AD8230, AD8555, AD8556 |
| Current Sense (Shunt) | Low value resistor output, high common-mode voltage | A few ohms (or less) | AD626, AD628, AD629, AD8202, AD8205 |
| EKG Monitors (Single-Supply Bridge Configuration) | Low level differential, output voltage, 5 mV output typical, single- or dual-supply | 500 kΩ | AD620, AD621, AD623, AD627, AD8220, AD8221, AD8222, AD8225, AD8553 |
| Photodiode Sensor | Current increases with light intensity, 1 pA to 1 μA $I_{OUTPUT,}$ single-supply | $10^9$ Ω | AD620, AD621, AD622, AD623, AD627, AD8220, AD8221, AD8222, AD8555 |
| Hall Effect Magnetic | 5 mV/kg to 120 mV/kg | 1 Ω to 1 kΩ | AD620, AD621, AD622, AD623, AD627, AD8221, AD8222, AD8230, AD8250, AD8251 |

Three in-amps are used to provide three separate outputs for monitoring the patient's condition. Suitable ADI products include AD8221, AD627, and AD623 in-amps and **AD8641**, **AD8642** (dual), and **AD8643** (quad) op amps for use as the buffer. Each in-amp is followed by a high-pass filter that removes the dc component from the signal. It is common practice to omit one of the in-amps and determine the third output by software (or hardware) calculation.

Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

## REMOTE LOAD-SENSING TECHNIQUE

The circuit of Figure 6-47 is a unity-gain instrumentation amplifier that uses its sense and reference pins to minimize any errors due to parasitic voltage drops within the circuit. If heavy output currents are expected, and there is a need to sense a load that is some distance away from the circuit, voltage drops due to trace or wire resistance can cause errors. These voltage drops are particularly troublesome with low resistance loads, such as 50 Ω.

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the in-amp output. Similarly, the reference terminal sets the reference voltage about which the in-amp's output will swing. This connection puts the IR drops inside the feedback loop of the in-amp and virtually eliminates any IR errors.

This circuit will provide a 3 dB bandwidth better than 3 MHz. Note that any net capacitance between the twisted pairs is isolated from the in-amp's output by 25 kΩ resistors, but any net capacitance between the twisted pairs and ground needs to be minimized to maintain stability. So, *unshielded* twisted pair cable is recommended for this circuit. For low speed applications that require driving long lengths of *shielded* cable, the **AMP01** should be substituted for the AMP03 device. The AMP01 can drive capacitance loads up to 1 μF, while the AMP03 is limited to driving a few hundred pF.

## A PRECISION VOLTAGE-TO-CURRENT CONVERTER

Figure 6-48 is a precision voltage-to-current converter whose scale factor is easily programmed for exact decade ratios using standard 1% metal film resistor values. The AD620 operates with full accuracy on standard 5 V power supply voltages. Note that although the quiescent current of the AD620 is only 900 μA, the addition of the **AD705** will add an additional 380 μA current consumption.

## A CURRENT SENSOR INTERFACE

Figure 6-49 shows a novel circuit for sensing low level currents. It makes use of the large common-mode range of the AD626. The current being measured is sensed across resistor $R_S$. The value of $R_S$ should be less than 1 kΩ and should be selected so that the average differential voltage across this resistor is typically 100 mV.

To produce a full-scale output of +4 V, a gain of 40 is used, adjustable by +20% to absorb the tolerance in the sense resistor. Note that there is sufficient headroom to allow at least a 10% overrange (to +4.4 V).

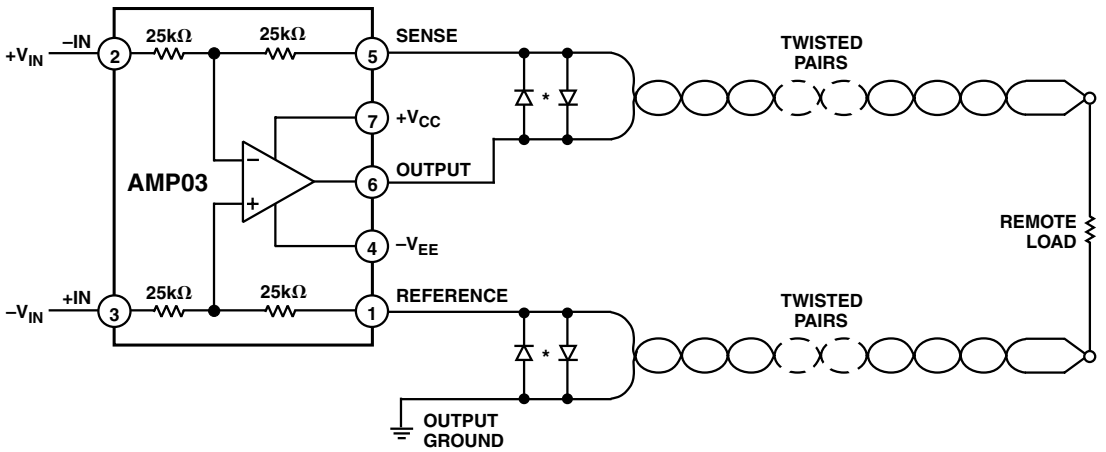



*Figure 6-47. A remote load sensing connection.*

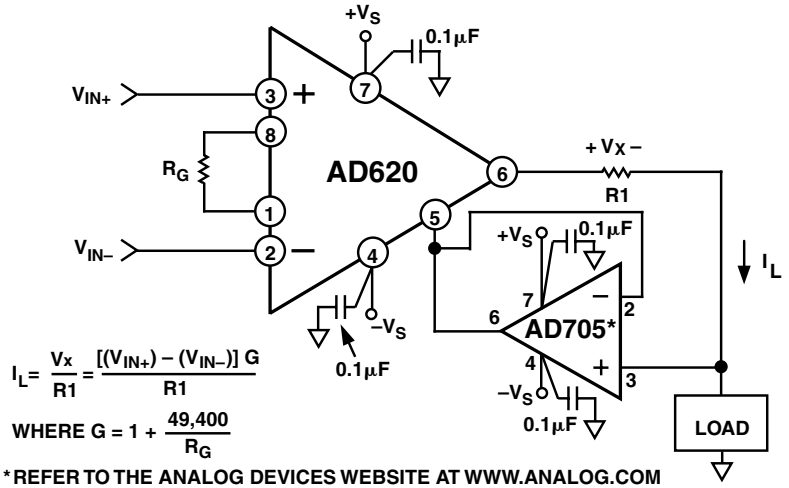



*Figure 6-48. A precision voltage-to-current converter that operates on ±5 V supplies.*

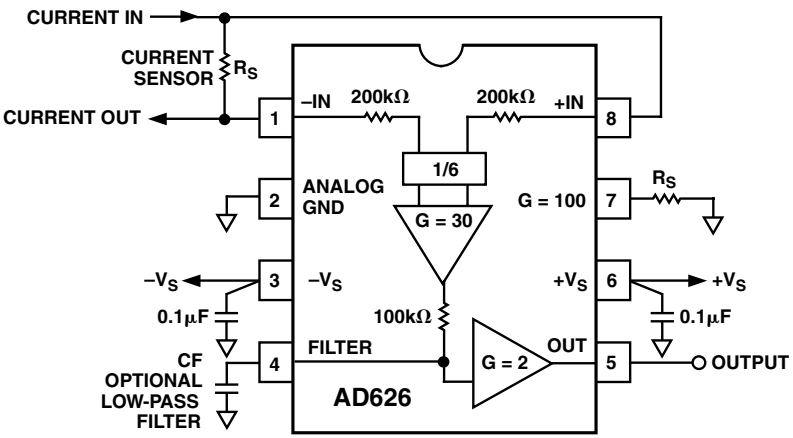



*Figure 6-49. Current sensor interface.*

**OUTPUT BUFFERING, LOW POWER IN-AMPS**

The AD627 low power in-amp is designed to drive load impedances of 20 kΩ or higher, but can deliver up to 20 mA to heavier loads with low output voltage swings. If more than 20 mA of output current is required, the AD627's output should be buffered with a precision low power op amp, such as the AD820, as shown in Figure 6-50. This op amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω. The addition of the **AD820** isolates the in-amp from the load, thus greatly reducing any thermal effects.

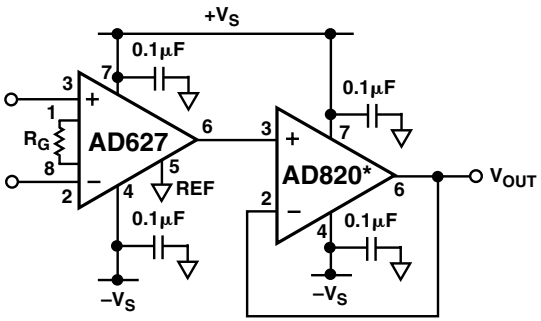



*Figure 6-50. Output buffer for low power in-amps.*

### A 4 TO 20 mA SINGLE-SUPPLY RECEIVER

Figure 6-51 shows how a signal from a 4 to 20 mA transducer can be interfaced to the **ADuC812**, a 12-bit ADC with an embedded microcontroller. The signal from a 4 to 20 mA transducer is single-ended. This initially suggests the need for a simple shunt resistor to convert the current to a voltage at the high impedance analog input of the converter. However, any line resistance in the return path (to the transducer) will add a current-dependent offset error. So, the current must be sensed differentially. In this example, a 24.9 Ω shunt resistor generates a maximum differential input voltage to the AD627 of between 100 mV (for 4 mA in) and 500 mV (for 20 mA in). With no gain resistor present, the AD627 amplifies the 500 mV input voltage by a factor of 5 to 2.5 V, the full-scale input voltage of the ADC. The zero current of 4 mA corresponds to a code of 819, and the LSB size is 0.61 mV.

### A SINGLE-SUPPLY THERMOCOUPLE AMPLIFIER

Because the common-mode input range of the AD627 extends 0.1 V below ground, it is possible to measure small differential signals with little or no common-mode component. Figure 6-52 shows a thermocouple application where one side of the J-type thermocouple is grounded. Over a temperature range from –200°C to +200°C, the J-type thermocouple delivers a voltage ranging from –7.890 mV to +10.777 mV.

A programmed gain on the AD627 of 100 ($R_G$ = 2.1 kΩ) and a voltage on the AD627 REF pin of 2 V results in the AD627's output voltage ranging from 1.110 V to 3.077 V relative to ground.

### SPECIALTY PRODUCTS

Analog Devices sells a number of specialty products, many of which were designed for the audio market that are useful for some in-amp applications. Table 6-4 lists some of these products.

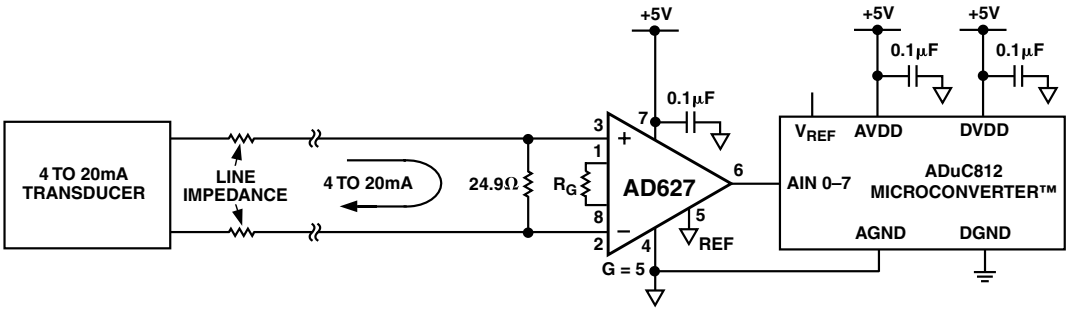



*Figure 6-51. A 4 to 20 mA receiver circuit.*

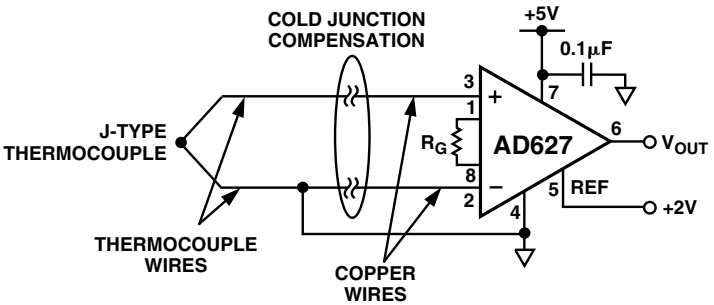



*Figure 6-52. A thermocouple amplifier using a low power, single-supply in-amp.*

**Table 6-4. Specialty Products Available from Analog Devices**

| Part Number | Description | BW | CMR (DC) | Supply | Features |
|---|---|---|---|---|---|
| SSM2141 | Diff line receiver | 3 MHz | 100 dB | ±18 V | High CMR, audio subtractor |
| SSM2143 | Diff line receiver | 7 MHz (G = 0.5) | 90 dB | ±6 V to ±18 V | Low distortion, audio subtractor |
| SSM2019 | Audio preamp | 2 MHz (G = 1) | 74 dB | ±5 V to ±18 V | Low noise, low distortion, audio IA |

# *Chapter VII*

# MATCHING IN-AMP CIRCUITS TO MODERN ADCs

**Calculating ADC Requirements**

The resolution of commercial ADCs is specified in bits. In an ADC, the available resolution equals $(2^n) - 1$, where n is the number of bits. For example, an 8-bit converter provides a resolution of $(2^8) - 1$, which equals 255. In this case, the full-scale input range of the converter divided by 255 will equal the smallest signal it can resolve. For example, an 8-bit ADC with a 5 V full-scale input range will have a limiting resolution of 19.6 mV.

In selecting an appropriate ADC to use, we need to find a device that has a resolution better than the measurement resolution but, for economy's sake, not a great deal better.

Table 7-1 provides input resolution and full-scale input range using an ADC with or without an in-amp preamplifier. Note that the system resolution specified in the figure refers to that provided by the converter together with the in-amp preamp (if used). Also, note that for any low level measurement, not only are low noise semiconductor devices needed, but also careful attention to component layout, grounding, power supply bypassing, and often, the use of balanced, shielded inputs.

For many applications, an 8-bit or 10-bit converter is appropriate. The decision to use a high resolution converter alone, or to use a gain stage ahead of a lower resolution converter, depends on which is more important: component cost, or parts count and ease of assembly.

One very effective way to raise system resolution is to amplify the signal first, to allow full use of the dynamic range of the ADC. However, this added gain ahead of the converter will also increase noise. Therefore, it is often useful to add low-pass filtering between the output of an in-amp (or other gain stage) and the input of the converter. Also, in most cases, the system bandwidth should not be set higher than that required to accurately measure the signal of interest. A good rule of thumb is to set the –3 dB corner frequency of the low-pass filter at 10 to 20 times the highest frequency that will be measured.

Adding amplification before the ADC will also reduce the circuit's full-scale input range, but it will lower the resolution requirements (and, therefore, the cost) of the ADC (see Figure 7-1).

For example, using an in-amp with a gain of 10 ahead of an 8-bit, 5 V ADC will increase circuit resolution from 19.5 mV (5 V/256) to 1.95 mV. At the same time, the full-scale input range of the circuit will be reduced to 500 mV (5 V/10).

**Table 7-1. Typical System Resolutions vs. Converter Resolution and Preamp (IA) Gain**

| Converter Type | $(2^n) - 1$ | Converter Resolution mV/Bit $(5\text{ V}/((2^n) - 1))$ | In-Amp Gain | FS Range (V p-p) | System Resolution (mV p-p) |
|---|---|---|---|---|---|
| 10-Bit | 1023 | 4.9 mV | 1 | 5 | 4.9 |
| 10-Bit | 1023 | 4.9 mV | 2 | 2.5 | 2.45 |
| 10-Bit | 1023 | 4.9 mV | 5 | 1 | 0.98 |
| 10-Bit | 1023 | 4.9 mV | 10 | 0.5 | 0.49 |
| 12-Bit | 4095 | 1.2 mV | 1 | 5 | 1.2 |
| 12-Bit | 4095 | 1.2 mV | 2 | 2.5 | 0.6 |
| 12-Bit | 4095 | 1.2 mV | 5 | 1 | 0.24 |
| 12-Bit | 4095 | 1.2 mV | 10 | 0.5 | 0.12 |
| 14-Bit | 16,383 | 0.305 mV | 1 | 5 | 0.305 |
| 14-Bit | 16,383 | 0.305 mV | 2 | 2.5 | 0.153 |
| 14-Bit | 16,383 | 0.305 mV | 5 | 1 | 0.061 |
| 14-Bit | 16,383 | 0.305 mV | 10 | 0.5 | 0.031 |
| 16-Bit | 65,535 | 0.076 mV | 1 | 5 | 0.076 |
| 16-Bit | 65,535 | 0.076 mV | 2 | 2.5 | 0.038 |
| 16-Bit | 65,535 | 0.076 mV | 5 | 1 | 0.015 |
| 16-Bit | 65,535 | 0.076 mV | 10 | 0.5 | 0.008 |

**Matching ADI In-Amps with Some Popular ADCs**

Table 7-2 shows recommended ADCs for use with the latest generation of ADI in-amps.

**Table 7-2. Recommended ADCs for Use with ADI In-Amps**

| **ADI In-Amp** | **AD8221AR** |
|---|---|
| Small Signal BW: | 562 kHz |
| Noise ($e_{NI}$): | 8 nV/√Hz |
| $V_{OS}$: | 60 µV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | ±3.9 V |
| CMR: | 90 dB (dc to 60 Hz) |
| Nonlinearity: | 10 ppm max |
| Supply Voltage: | ±5 V |
| Supply Current: | 1 mA max |
| 0.01% Settling Time for 5 V Step: | 5 µs |
| 0.001% Settling Time for 5 V Step: | 6 µs |
| **Recommended ADI ADC#1** | |
| **AD7685, AD7687** | |
| Resolution: | 16 bits |
| Input Range: | 0 V to 5 V |
| Sampling Rate: | Up to 250 kSPS |
| S/D Supply: | 3 V or 5 V |
| Power: | 1.7 mW @ 2.5 V and 6 mW typ @ 5 V |
| Comments: | Same package, the AD7685 can be driven through a simple RC from the AD8221 directly. The REF pin can be driven to fit the ADC range. |
| **Recommended ADI ADC#2** | |
| **AD7453/AD7457** | |
| Resolution: | 12 bits |
| Input Range: | 0 V to $V_{DD}$ |
| Sampling Rate: | 555 kSPS/100 kSPS |
| S/D Supply: | 3 V or 5 V |
| Power: | 0.3 mA @ 100 kSPS |
| Comments: | Single channel, pseudo differential inputs in a SOT-23 package |

| **ADI In-Amp** | **AD620AR** |
|---|---|
| Small Signal BW: | 800 kHz |
| Noise ($e_{NI}$): | 9 nV/√Hz |
| $V_{OS}$: | 125 µV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | ±3.9 V |
| CMR: | 73 dB (dc to 60 Hz) |
| Nonlinearity: | 40 ppm max |
| Supply Voltage: | ±5 V |
| Supply Current: | 1.3 mA max |
| 0.01% Settling Time for 5 V Step: | 7 µs |
| **Recommended ADI ADC#1** | |
| **AD7610, AD7663** | |
| Resolution: | 16 bits |
| Input Range: | Multiple, such as ±10 V, ±5 V, ... |
| Sampling Rate: | Up to 250 kSPS |
| S/D Supply: | 5 V |
| Power: | 2.7 mA @ 100 kSPS |
| Comments: | Allow more and larger input ranges |
| **Recommended ADI ADC#2** | |
| **AD7895** | |
| Resolution: | 12 bits |
| Input Range: | Multiple, such as ±10 V, ±2.5 V, 0 V to 2.5 V |
| Sampling Rate: | 200 kSPS |
| S/D Supply: | 5 V |
| Power: | 2.2 mA @ 100 kSPS |
| Comments: | Allows a bipolar or unipolar input with a single supply |

**Table 7-2. Recommended ADCs for Use with ADI In-Amps (continued)**

| ADI In-Amp | AD8225 Fixed Gain of 5 |
|---|---|
| Small Signal BW: | 900 kHz |
| Noise ($e_{NI}$): | 8 nV/√Hz |
| $V_{OS}$: | 125 µV max |
| In-Amp Gain: | 5 |
| Maximum Output Voltage Swing: | ±4 V |
| CMR: | 90 dB (dc to 60 Hz) |
| Nonlinearity: | 10 ppm max |
| Supply Voltage: | ±5 V |
| Supply Current: | 1.2 mA max |
| 0.01% Settling Time for 5 V Step: | 3.2 µs |
| 0.001% Settling Time for 5 V Step: | 4 µs |
| **Recommended ADI ADC#1** | |
| AD7661 | |
| Resolution: | 16 bits |
| Input Range: | 0 V to 2.5 V |
| Sampling Rate: | Up to 100 kSPS |
| S/D Supply: | 5 V |
| Power: | 8 mA @ 100 kSPS with reference |
| Comments: | Provide a reference voltage |
| **Recommended ADI ADC#2** | |
| AD7940 | |
| Resolution: | 14 bits |
| Input Range: | 0 V to $V_{DD}$ |
| Sampling Rate: | 100 kSPS |
| S/D Supply: | 3 V or 5 V |
| Power: | 0.83 mA @ 100 kSPS |
| Comments: | Single channel in an SOT-23 |

| ADI In-Amp | AD623AR |
|---|---|
| Small Signal BW: | 100 kHz |
| Noise ($e_{NI}$): | 35 nV/√Hz |
| $V_{OS}$: | 200 µV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | ±4.5 V |
| CMR: | 90 dB (dc to 60 Hz) |
| Nonlinearity: | 50 ppm typ |
| Supply Voltage: | ±5 V |
| Supply Current: | 0.55 mA max |
| 0.01% Settling Time for 5 V Step: | 20 µs |

| Recommended ADI ADC#1 | |
|---|---|
| AD7866 | |
| Resolution: | 12 bits |
| Input Range: | 0 V to $V_{REF}$ V or 0 V to 2 × $V_{REF}$ V |
| Sampling Rate: | 1 MSPS for both ADCs |
| S/D Supply: | Single, 2.7 V to 5.25 V |
| Power: | 24 mW max at 1 MSPS with 5 V supply 11.4 mW max at 1 MSPS with 3 V supply |
| Comments: | Dual, 2-channel, simultaneous sampling ADC with a serial interface |
| **Recommended ADI ADC#2** | |
| AD7862/AD7864 | |
| Resolution: | 12 bits |
| Input Range: | 0 V to +2.5 V, 0 V to +5 V, ±2.5 V, ±5 V, ±10 V |
| Sampling Rate: | 600 kSPS for one channel |
| S/D Supply: | Single, 5 V |
| Power: | 90 mW typ |
| Comments: | 4-channel, simultaneous sampling ADC with a parallel interface |
| **Recommended ADI ADC#3** | |
| AD7863/AD7865 | |
| Resolution: | 14 bits |
| Input Range: | 0 V to +2.5 V, 0 V to +5 V, ±2.5 V, ±5 V, ±10 V |
| Sampling Rate: | 175 kSPS for both channels/ 360 kSPS for one channel, respectively |
| S/D Supply: | Single, 5 V |
| Power: | 70 mW typ/115 mV typ, respectively |
| Comments: | 2-/4-channel, respectively, simultaneous sampling ADC with a parallel interface |
| **Recommended ADI ADC#4** | |
| AD7890/AD7891/AD7892 | |
| Resolution: | 12 bits |
| Input Range: | 0 V to +2.5 V, 0 V to +4.096 V, 0 V to +5 V, ±2.5 V, ±5 V±10 V |
| Sampling Rate: | 117/500/600 kSPS, respectively |
| S/D Supply: | Single, 5 V |
| Power: | 30/85/60 mW typ, respectively |
| Comments: | 8-/8-/1-channel, respectively |

**Table 7-2. Recommended ADCs for Use with ADI In-Amps (continued)**

| ADI In-Amp | AD627AR |
|---|---|
| Small Signal BW: | 30 kHz |
| Noise ($e_{NI}$): | 38 nV/√Hz |
| $V_{OS}$: | 200 µV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | ±4.9 V |
| CMR: | 77 dB (dc to 60 Hz) |
| Nonlinearity: | 100 ppm max |
| Supply Voltage: | ±5 V |
| Supply Current: | 85 µA max |
| 0.01% Settling Time for 5 V Step: | 135 µs |
| **Recommended ADI ADC#1** | |
| **AD7923/AD7927** | |
| Resolution: | 12 bits |
| Input Range: | 0 V to $V_{REF}$ or 0 V to 2 × $V_{REF}$ |
| Sampling Rate: | 200 kSPS |
| S/D Supply: | Single, 2.7 V to 5.25 V |
| Power: | 3.6 mW max @ 200 kSPS with a 3 V supply |
| Comments: | 8-/4-channel ADCs, respectively, with a serial interface and channel sequencer |
| **Recommended ADI ADC#2** | |
| **AD7920** | |
| Resolution: | 12 bits |
| Input Range: | 0 to $V_{DD}$ |
| Sampling Rate: | 250 kSPS |
| S/D Supply: | 2.35 V or 5.25 V |
| Power: | 3 mW typ @ 250 kSPS with 3 V supply |
| Comments: | Single channel, serial ADC in 6-lead SC70 |

| ADI In-Amp JFET In-Amp | AD8220AR |
|---|---|
| Small Signal BW: | 1000 kHz |
| Noise ($e_{NI}$): | 15 nV/√Hz |
| $V_{OS}$: | 1 mV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | ±4.8 V |
| CMRR: | 110 dB (dc to 60 Hz) |
| Nonlinearity: | 10 ppm max |
| Supply Voltage: | Dual, ±5 V |
| Supply Current: | 1 mA max |
| 0.01% Settling Time for 5 V step: | 5 ms |
| **Recommended ADI ADC#1** | |
| **AD7610/AD7663** | |
| Resolution: | 16 bits |
| Input Range: | ±2.5 V, ±5 V, ±10 V |
| Sampling Rate: | 250 kSPS for both ADCs |
| S/D Supply: | ±5 V to ±15 V and 5 V |
| **Recommended ADC#2** | |
| **AD7321, AD7323, and AD7327** | |
| Resolution: | 13 bits |
| Input Range: | ±2.5 V, ±5 V, ±10 V |
| Sampling Rate: | 500 kSPS |
| S/D Supply: | ±5 V to ±15 V and +5 V |
| Power: | 17 mW max at 0.5 MSPS with ±15 V, and 5 V supply |
| **Recommended ADI ADC#3** | |
| **AD7898-3** | |
| Resolution: | 12 bits |
| Input Range: | ±2.5 V |
| Sampling Rate: | 220 kSPS |
| S/D Supply: | 5 V |
| Power: | 22.5 mW max at 220 kSPS with 5 V supply |

**Table 7-2. Recommended ADCs for Use with ADI In-Amps (continued)**

| **ADI In-Amp Zero Drift In-Amp** | **AD8230RZ** |
|---|---|
| Small Signal BW: | 2 kHz |
| Noise ($e_{NI}$): | 240 nV/√Hz |
| $V_{OS}$: | 10 mV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | ±4.7 V |
| CMRR: | 120 dB (dc to 60 Hz) |
| Nonlinearity: | 20 ppm max |
| Supply Voltage: | ±5 V |
| Supply Current: | 3.5 mA max |
| **Recommended ADI ADC#1** | |
| **AD7942** | |
| Resolution: | 14 bits |
| Input Range: | 5 V |
| Sampling Rate: | 250 kSPS |
| S/D Supply: | 2.7 V to 5.25 V |
| Power: | 1.25 mW, 2.5 V supply |
| **Recommended ADI ADC#2** | |
| **AD7321** | |
| Resolution: | 13 bits |
| Input Range: | ±2.5 V |
| Sampling Rate: | 500 kSPS |
| S/D Supply: | ±5 V to ±15 V, 2.7 V to 5.25 V |
| Power: | 17 mW max at 500 kSPS with ±15 V, 5 V supply |

NOTE: Specifications are preliminary. Refer to www.analog.com.

| **ADI In-Amp High Speed Programmable Gain In-Amp** | **AD8250/AD8251** |
|---|---|
| Small Signal BW: | 10 MHz |
| Noise ($e_{NI}$): | 13 nV/√Hz |
| $V_{OS}$: | 100 mV |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | $V_{CC}$ – 1.2 V, $V_{CC}$ + 1.2 V |
| CMRR: | 100 dB (dc to 60 Hz) |
| Nonlinearity: | 40 ppm max |
| Supply Voltage: | Dual, ±5 V to ±12 V |
| Supply Current: | 3 mA typ |
| 0.01% Settling Time for 5 V step: | 0.5 µs |
| **Recommended ADI ADC#1** | |
| **AD7685, AD7687** | |
| Resolution: | 16 bits |
| Input Range: | 5 V |
| Sampling Rate: | 250 kSPS |
| S/D Supply: | Single, 2.5 V to 5 V |
| Power: | 4 mW at 0.1 kSPS, 5 V supply |
| **Recommended ADI ADC#2** | |
| **AD7327, AD7323, and AD7321** | |
| Resolution: | 13 bits/12 bits |
| Input Range: | ±2.5 V |
| Sampling Rate: | 0.5 MSPS |
| S/D Supply: | ±5 V to ±15 V, single, 5 V |
| Power: | 17 mW max at 500 kSPS with ±15 V, 5 V supply |

**Table 7-2. Recommended ADCs for Use with ADI In-Amps (continued)**

| ADI In-Amp Zero Drift In-Amp | AD8553RM |
|---|---|
| Small Signal BW: | 1 kHz |
| Noise ($e_{NI}$): | 150 nV/√Hz |
| $V_{OS}$: | 50 mV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | 0.075 V to 4.925 V |
| CMRR: | 120 dB (dc to 60 Hz) |
| Nonlinearity: | 600 ppm max |
| Supply Voltage: | Single, 5 V |
| Supply Current: | 1.3 mA max |
| **Recommended ADI ADC#1** | |
| AD7476 | |
| Resolution: | 12 bits |
| Input Range: | 0 to $V_{DD}$ |
| Sampling Rate: | 1 MSPS |
| S/D Supply: | 2.35 V to 5.25 V |
| Power: | 3.6 mW max at 1 MSPS with 3 V supply<br>15 mW max at 1 MSPS with 5 V supply |
| **Recommended ADI ADC#2** | |
| AD7466 | |
| Resolution: | 12 bits |
| Input Range: | 0 to $V_{DD}$ |
| Sampling Rate: | 100 kSPS |
| S/D Supply: | 1.6 V to 3.6 V |
| Power: | 0.62 mW max at 100 kSPS with 3 V supply<br>0.12 mW max at 100 kSPS with 1.6 V supply |

| ADI In-Amp Zero Drift In-Amp | AD8555AR/AD8556ARZ |
|---|---|
| Small Signal BW: | 150 kHz |
| Noise ($e_{NI}$): | 32 nV√Hz |
| $V_{OS}$: | 10 mV max |
| In-Amp Gain: | 10 |
| Maximum Output Voltage Swing: | 30 mV to 4.94 V |
| CMRR: | 100 dB (G = 70, dc to 200 Hz) |
| Nonlinearity: | 1000 ppm typ |
| Supply Voltage: | Single, 5 V |
| Supply Current: | 2.5 mA max |
| 0.1% Settling Time for 4 V step: | 8 ms |
| **Recommended ADI ADC#1** | |
| AD7685 | |
| Resolution: | 16 bits |
| Input Range: | 5 V |
| Sampling Rate: | 250 kSPS |
| S/D Supply: | Single, 2.5 V to 5 V |
| Power: | 4 mW at 0.1 SPS with 5 V supply |
| **Recommended ADI ADC#2** | |
| AD7476 | |
| Resolution: | 12 bits |
| Input Range: | 0 to $V_{DD}$ |
| Sampling Rate: | 1 MSPS |
| S/D Supply: | 2.35 V to 5.25 V |
| Power: | 3.6 mW max at 1 MSPS with 3 V supply<br>15 mW max at 1 MSPS with 5 V supply |
| **Recommended ADI ADC#3** | |
| AD7476A | |
| Resolution: | 12 bits |
| Input Range: | 0 to $V_{DD}$ |
| Sampling Rate: | 1 MSPS |
| S/D Supply: | 2.7 V to 5.25 V |
| Power: | 3.6 mW max at 1 MSPS with 3 V supply<br>12.5 mW max at 1 MSPS with 5 V supply |

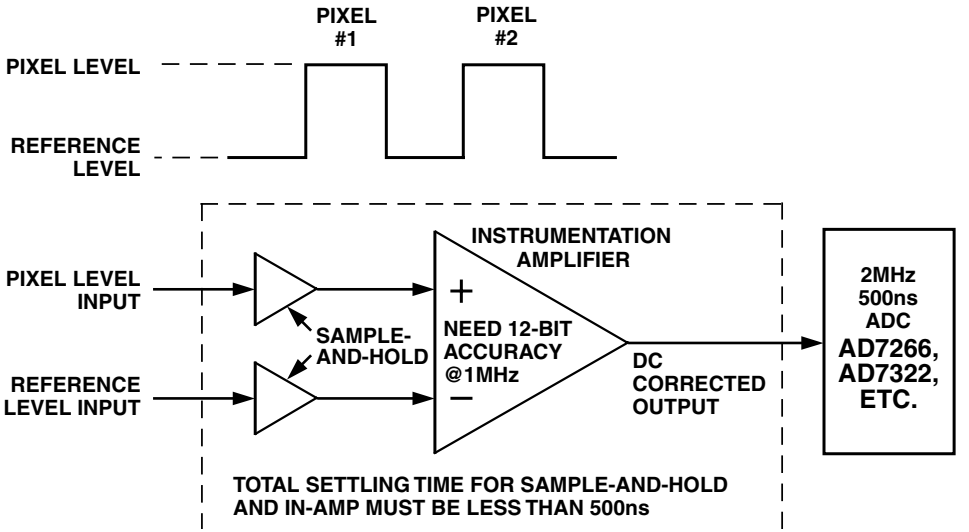



*Figure 7-1. In-amp buffers ADC and provides dc correction.*

**High Speed Data Acquisition**

As the speed and accuracy of modern data acquisition systems have increased, a growing need for high bandwidth instrumentation amplifiers has developed—particularly in the field of CCD imaging equipment where offset correction and input buffering are required. Here, double-correlated sampling techniques are often used for offset correction of the CCD imager. As shown in Figure 7-1, two sample-and-hold amplifiers monitor the pixel and reference levels, and a dc-corrected output is provided by feeding their signals into an instrumentation amplifier.

Figure 7-2 shows how a single multiplexed high bandwidth in-amp can replace several slow speed nonmultiplexed buffers. The system benefits from the common-mode noise reduction and subsequent increase in dynamic range provided by the in-amp.

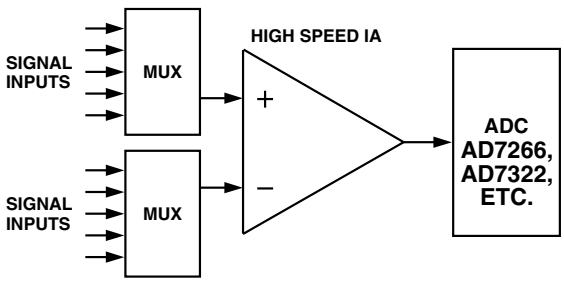



*Figure 7-2. Single high speed in-amp and mux replace several slow speed buffers.*

Previously, the low bandwidths of commonly available instrumentation amplifiers, plus their inability to drive 50 Ω loads, restricted their use to low frequency applications—generally below 1 MHz. Some higher bandwidth amplifiers have been available, but these have been fixed-gain types with internal resistors. With these amplifiers, there was no access to the inverting and noninverting terminals of the amplifier. Using modern op amps and employing the complementary bipolar (CB) process, video bandwidth instrumentation amplifiers that offer both high bandwidths and impressive dc specifications may now be constructed. Common-mode rejection may be optimized by trimming or by using low cost resistor arrays.

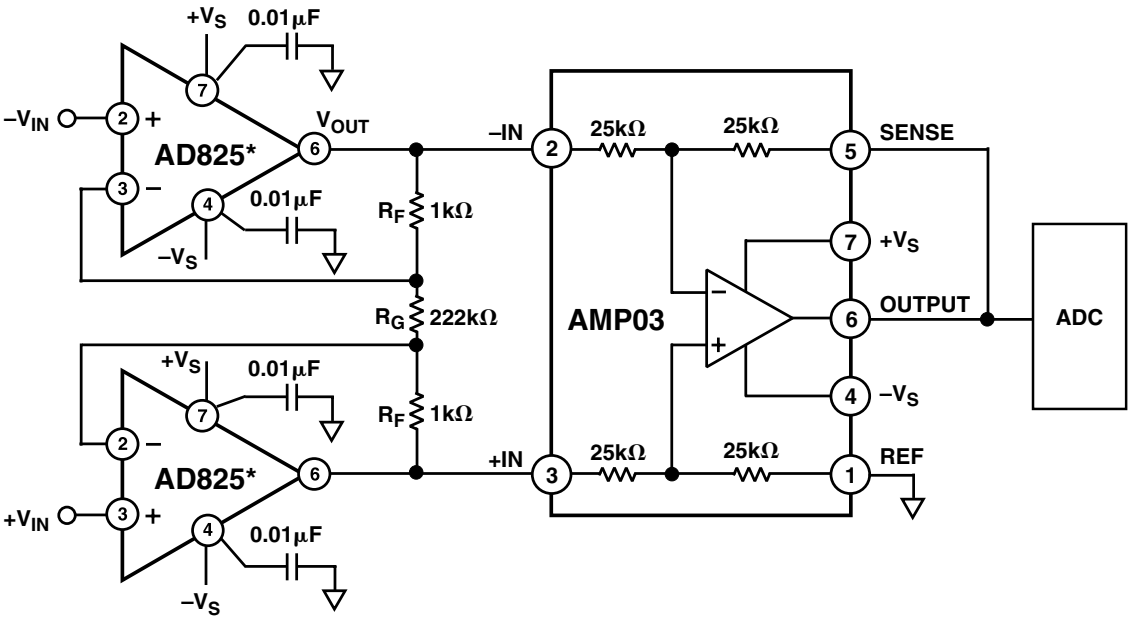
The bandwidth and settling time requirements demanded of an in-amp buffering an ADC, and for the sample-and-hold function preceding it, can be quite severe. The input buffer must pass the signal along fast enough so that the signal is fully settled before the ADC takes its next sample. At least two samples per cycle are required for an ADC to unambiguously process an input signal (FS/2)—this is referred to as the *Nyquist criteria*. Therefore, a 2 MHz ADC, such as the **AD7266** or **AD7322**, requires that the input buffer/sample-and-hold sections preceding it provide 12-bit accuracy at a 1 MHz bandwidth. Settling time is equally important: the sampling rate of an ADC is the inverse of its sampling frequency—for the 2 MHz ADC, the sampling rate is 500 ns. This means that for a total throughput rate of less than 1 µs, these same input buffer/sample-and-hold sections must have a total settling time of less than 500 ns.

**A High Speed In-Amp Circuit for Data Acquisition**

Figure 7-3 shows a discrete in-amp circuit using two **AD825** op amps and an AMP03 differential (subtractor) amplifier. This design provides both high performance and high speed at moderate gains. Circuit gain is set by resistor $R_G$ where gain = 1 + 2 $R_F/R_G$. The $R_F$ resistors should be kept at around 1 kΩ to ensure maximum bandwidth. Operating at a gain of 10 (using a 222 Ω resistor for $R_G$) the –3 dB bandwidth of this circuit is approximately 3.4 MHz. The ac common-mode rejection ratio (gain of 10, 1 V p-p common-mode signal applied to the inputs) is 60 dB from 1 Hz to 200 kHz and 43 dB at 2 MHz. And it provides better than 46 dB CMRR from 4 MHz to 7 MHz. The RFI rejection characteristics of this amplifier are also excellent—the change in dc offset voltage vs. common-mode frequency is better than 80 dB from 1 Hz up to 15 MHz. Quiescent supply current for this circuit is 15 mA.

For lower speed applications requiring a low input current device, the **AD823** FET input op amp can be substituted for the AD825.

This circuit can be used to drive a modern, high speed ADC such as the **AD871** or **AD9240**, and to provide very high speed data acquisition. The AD830 can also be used for many high speed applications.




*REFER TO ANALOG DEVICES WEBSITE AT WWW.ANALOG.COM FOR THE LATEST OP AMP PRODUCTS AND SPECIFICATIONS.

*Figure 7-3. A High performance, high speed in-amp circuit.*

# *Appendix A*

# INSTRUMENTATION AMPLIFIER SPECIFICATIONS

To successfully apply any electronic component, a full understanding of its specifications is required. That is to say, the numbers contained in a data sheet are of little value if the user does not have a clear picture of what each specification means.

In this section, a typical monolithic instrumentation amplifier data sheet is reviewed. Some of the more important specifications are discussed in terms of how they are measured and what errors they might contribute to the overall performance of the circuit.

Table A-1 shows a portion of the data sheet for the Analog Devices AD8221 instrumentation amplifier.

**Table A-1. AD8221 Specifications[1]**

| Parameter | Conditions | AR Grade Min | AR Grade Typ | AR Grade Max | BR Grade Min | BR Grade Typ | BR Grade Max | ARM Grade Min | ARM Grade Typ | ARM Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| COMMON-MODE REJECTION RATIO (CMRR) | | | | | | | | | | | |
| CMRR DC to 60 Hz with 1 kΩ Source Imbalance | $V_{CM}$ = –10 V to +10 V | | | | | | | | | | |
| G = 1 | | 80 | | | 90 | | | 80 | | | dB |
| G = 10 | | 100 | | | 110 | | | 100 | | | dB |
| G = 100 | | 120 | | | 130 | | | 120 | | | dB |
| G = 1000 | | 130 | | | 140 | | | 130 | | | dB |
| CMRR at 10 kHz | $V_{CM}$ = –10 V to +10 V | | | | | | | | | | |
| G = 1 | | 80 | | | 80 | | | 80 | | | dB |
| G = 10 | | 90 | | | 100 | | | 90 | | | dB |
| G = 100 | | 100 | | | 110 | | | 100 | | | dB |
| G = 1000 | | 100 | | | 110 | | | 100 | | | dB |
| NOISE | *RTI noise* = $\sqrt{e_{NI}^2 + (e_{NO}/G)^2}$ | | | | | | | | | | |
| Voltage Noise, 1 kHz | | | | | | | | | | | |
| Input Voltage Noise, $e_{NI}$ | $V_{IN+}$, $V_{IN-}$, $V_{REF}$ = 0 | | | 8 | | | 8 | | | 8 | nV/√Hz |
| Output Voltage Noise, $e_{NO}$ | | | | 75 | | | 75 | | | 75 | nV/√Hz |
| RTI | f = 0.1 Hz to 10 Hz | | | | | | | | | | |
| G = 1 | | | 2 | | | 2 | | | 2 | | µV p-p |
| G = 10 | | | 0.5 | | | 0.5 | | | 0.5 | | µV p-p |
| G = 100 to 1000 | | | 0.25 | | | 0.25 | | | 0.25 | | µV p-p |
| Current Noise | f = 1 kHz | | 40 | | | 40 | | | 40 | | fA/√Hz |
| | f = 0.1 Hz to 10 Hz | | 6 | | | 6 | | | 6 | | pA p-p |
| VOLTAGE OFFSET[2] | | | | | | | | | | | |
| Input Offset, $V_{OSI}$ | $V_S$ = ±5 V to ±15 V | | | 60 | | | 25 | | | 70 | µV |
| Over Temperature | T = –40°C to +85°C | | | 86 | | | 45 | | | 135 | µV |
| Average TC | | | | 0.4 | | | 0.3 | | | 0.9 | µV/°C |
| Output Offset, $V_{OSO}$ | $V_S$ = ±5 V to ±15 V | | | 300 | | | 200 | | | 600 | µV |
| Over Temperature | T = –40°C to +85°C | | | 0.66 | | | 0.45 | | | 1.00 | mV |
| Average TC | | | | 6 | | | 5 | | | 9 | µV/°C |
| Offset RTI vs. Supply (PSR) | $V_S$ = ±2.3 V to ±18 V | | | | | | | | | | |
| G = 1 | | 90 | 110 | | 94 | 110 | | 90 | 100 | | dB |
| G = 10 | | 110 | 120 | | 114 | 130 | | 100 | 120 | | dB |
| G = 100 | | 124 | 130 | | 130 | 140 | | 120 | 140 | | dB |
| G = 1000 | | 130 | 140 | | 140 | 150 | | 120 | 140 | | dB |
| INPUT CURRENT | | | | | | | | | | | |
| Input Bias Current | | | 0.5 | 1.5 | | 0.2 | 0.4 | | 0.5 | 2 | nA |
| Over Temperature | T = –40°C to +85°C | | | 2.0 | | | 1 | | | 3 | nA |
| Average TC | | | 1 | | | 1 | | | 3 | | pA/°C |
| Input Offset Current | | | 0.2 | 0.6 | | 0.1 | 0.4 | | 0.3 | 1 | nA |
| Over Temperature | T = –40°C to +85°C | | | 0.8 | | | 0.6 | | | 1.5 | nA |
| Average TC | | | 1 | | | 1 | | | 3 | | pA/°C |

| Parameter | Conditions | AR Grade Min | AR Grade Typ | AR Grade Max | BR Grade Min | BR Grade Typ | BR Grade Max | ARM Grade Min | ARM Grade Typ | ARM Grade Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| REFERENCE INPUT | | | | | | | | | | | |
| $R_{IN}$ | | | 20 | | | 20 | | | 20 | | kΩ |
| $I_{IN}$ | $V_{IN+}$, $V_{IN-}$, $V_{REF}$ = 0 | | 50 | 60 | | 50 | 60 | | 50 | 60 | µA |
| Voltage Range | | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | V |
| Gain to Output | | | 1 ± 0.0001 | | | 1 ± 0.0001 | | | 1 ± 0.0001 | | V/V |
| POWER SUPPLY | | | | | | | | | | | |
| (F) Operating Range | $V_S$ = ±2.3 V to ±18 V | ±2.3 | | ±18 | ±2.3 | | ±18 | ±2.3 | | ±18 | V |
| (G) Quiescent Current | | | 0.9 | 1 | | 0.9 | 1 | | 0.9 | 1 | mA |
| Over Temperature | T = –40°C to +85°C | | 1 | 1.2 | | 1 | 1.2 | | 1 | 1.2 | mA |
| DYNAMIC RESPONSE | | | | | | | | | | | |
| Small Signal, –3 dB Bandwidth | | | | | | | | | | | |
| G = 1 | | | 825 | | | 825 | | | 825 | | kHz |
| G = 10 | | | 562 | | | 562 | | | 562 | | kHz |
| G = 100 | | | 100 | | | 100 | | | 100 | | kHz |
| G = 1000 | | | 14.7 | | | 14.7 | | | 14.7 | | kHz |
| (H) Settling Time 0.01% | 10 V step | | | | | | | | | | |
| G = 1 to 100 | | | 10 | | | 10 | | | 10 | | µs |
| G = 1000 | | | 80 | | | 80 | | | 80 | | µs |
| (H) Settling Time 0.001% | 10 V step | | | | | | | | | | |
| G = 1 to 100 | | | 13 | | | 13 | | | 13 | | µs |
| G = 1000 | | | 110 | | | 110 | | | 110 | | µs |
| Slew Rate | G = 1 | 1.5 | 1.7 | | 1.5 | 1.7 | | 1.5 | 1.7 | | V/µs |
| | G = 5 to 100 | 2 | 2.5 | | 2 | 2.5 | | 2 | 2.5 | | V/µs |
| (I) GAIN | G = 1 + (49.4 kΩ/$R_G$) | | | | | | | | | | |
| (J) Gain Range | | 1 | | 1000 | 1 | | 1000 | 1 | | 1000 | V/V |
| (K) Gain Error | $V_{OUT}$ ±10 V | | | | | | | | | | |
| G = 1 | | | | 0.03 | | | 0.02 | | | 0.1 | % |
| G = 10 | | | | 0.3 | | | 0.15 | | | 0.3 | % |
| G = 100 | | | | 0.3 | | | 0.15 | | | 0.3 | % |
| G = 1000 | | | | 0.3 | | | 0.15 | | | 0.3 | % |
| (L) Gain Nonlinearity | $V_{OUT}$ = –10 V to +10 V | | | | | | | | | | |
| G = 1 to 10 | $R_L$ = 10 kΩ | | 3 | 10 | | 3 | 10 | | 5 | 15 | ppm |
| G = 100 | $R_L$ = 10 kΩ | | 5 | 15 | | 5 | 15 | | 7 | 20 | ppm |
| G = 1000 | $R_L$ = 10 kΩ | | 10 | 40 | | 10 | 40 | | 10 | 50 | ppm |
| G = 1 to 100 | $R_L$ = 2 kΩ | | 10 | 95 | | 10 | 95 | | 15 | 100 | ppm |
| (M) Gain vs. Temperature | | | | | | | | | | | |
| G = 1 | | | 3 | 10 | | 2 | 5 | | 3 | 10 | ppm/°C |
| G > 1[3] | | | | –50 | | | –50 | | | –50 | ppm/°C |
| INPUT | | | | | | | | | | | |
| Input Impedance | | | | | | | | | | | |
| Differential | | | 100 \|\|2 | | | 100 \|\|2 | | | 100 \|\|2 | | GΩ \|\|pF |
| Common Mode | | | 100 \|\|2 | | | 100 \|\|2 | | | 100 \|\|2 | | GΩ \|\|pF |
| Input Operating Voltage Range[4] | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.9 | | $+V_S$ – 1.1 | $-V_S$ + 1.9 | | $+V_S$ – 1.1 | $-V_S$ + 1.9 | | $+V_S$ – 1.1 | V |
| Over Temperature | T = –40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ – 1.2 | $-V_S$ + 2.0 | | $+V_S$ – 1.2 | $-V_S$ + 2.0 | | $+V_S$ – 1.2 | V |
| Input Operating Voltage Range | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.9 | | $+V_S$ – 1.2 | $-V_S$ + 1.9 | | $+V_S$ – 1.2 | $-V_S$ + 1.9 | | $+V_S$ – 1.2 | V |
| Over Temperature | T = –40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ – 1.2 | $-V_S$ + 2.0 | | $+V_S$ – 1.2 | $-V_S$ + 2.0 | | $+V_S$ – 1.2 | V |
| OUTPUT | $R_L$ = 10 kΩ | | | | | | | | | | |
| Output Swing | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | $-V_S$ + 1.1 | | $+V_S$ – 1.2 | V |
| Over Temperature | T = –40°C to +85°C | $-V_S$ + 1.4 | | $+V_S$ – 1.3 | $-V_S$ + 1.4 | | $+V_S$ – 1.3 | $-V_S$ + 1.4 | | $+V_S$ – 1.3 | V |
| (N) Output Swing | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | $-V_S$ + 1.2 | | $+V_S$ – 1.4 | V |
| Over Temperature | T = –40°C to +85°C | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | $-V_S$ + 1.6 | | $+V_S$ – 1.5 | V |
| Short-Circuit Current | | | 18 | | | 18 | | | 18 | | mA |
| TEMPERATURE RANGE | | | | | | | | | | | |
| Specified Performance | | –40 | | +85 | –40 | | +85 | –40 | | +85 | °C |
| Operational[4] | | –40 | | +125 | –40 | | +125 | –40 | | +125 | °C |

NOTES
[1]$V_S$ = ±15 V, $V_{REF}$ = 0 V, $T_A$ = +25°C, G = 1, $R_L$ = 2 kΩ, unless otherwise noted.
[2]Total RTI $V_{OS}$ = ($V_{OSI}$) + ($V_{OSO}$/G).
[3]Does not include the effects of external resistor $R_G$.
[4]One input grounded. G = 1.

**(A) Specifications (Conditions)**

A statement at the top of the data sheet explains that the listed specifications are typically @ $T_A$ = 25°C, $V_S$ = ±15 V, and $R_L$ = 10 kΩ, unless otherwise noted. This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. For situations where deviations from the normal conditions (such as a change in temperature) are likely, the significant effects are usually indicated within the specs. The statement at the top of the specifications table also tells us what all numbers are unless noted; typical is used to state that the manufacturer's characterization process has shown a number to be average; however, individual devices may vary.

Instrumentation amplifiers designed for true rail-to-rail operation have a few critical specifications that need to be considered. Their input voltage range should allow the in-amp to accept input signal levels that are close to the power supply or ground. Their output swing should be within 0.1 V of the supply line or ground. In contrast, a typical dual-supply in-amp can swing only within 2 V or more of the supply or ground. In 5 V single-supply data acquisition systems, an extended output swing is vital because it allows the full input range of the ADC to be used, providing high resolution.

**(B) Common-Mode Rejection**

Common-mode rejection is a measure of the change in output voltage when the same voltage is applied to both inputs. CMR is normally specified as input, which allows for in-amp gain. As the gain is increased, there will be a higher output voltage for the same common-mode input voltage. These specifications may be given for either a full range input voltage change or for a specified source imbalance in ohms.

Common-mode rejection ratio is a ratio expression, while common-mode rejection is the logarithm of that ratio. Both specifications are normally referred to output (RTO).

That is,

$$CMRR = \frac{Change\ in\ Output\ Voltage}{Change\ in\ Common\text{-}Mode\ Input\ Voltage}$$

While

$$CMR = 20\ Log10\ CMRR$$

For example, a CMRR of 10,000 corresponds to a CMR of 80 dB. For most in-amps, the CMR increases with gain because most designs have a front-end configuration that rejects common-mode signals while amplifying differential (i.e., signal) voltages.

Common-mode rejection is usually specified for a full range common-mode voltage change at a given frequency, and a specified imbalance of source impedance (e.g., 1 kΩ source unbalance, at 60 Hz).

**(C) AC Common-Mode Rejection**

As might be expected, an in-amp's common-mode rejection *does* vary with frequency. Usually, CMR is specified at dc or at very low input frequencies. At higher gains, an in-amp's bandwidth does decrease, lowering its gain and introducing additional phase shift in its input stage.

Since any imbalance in phase shift in the differential input stage will show up as a common-mode error, ac CMRR will usually decrease with frequency. Figure A-1 shows the CMR vs. frequency of the AD8221.

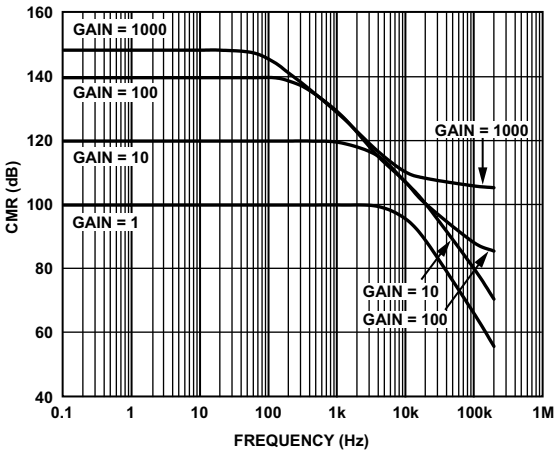



*Figure A-1. AD8221 CMR vs. frequency.*

**(D) Voltage Offset**

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While any initial offset may be adjusted to zero through the use of hardware or software, shifts in offset voltage due to temperature variations are more difficult to correct. Intelligent systems using a microprocessor can use a temperature reference and calibration data to correct for this, but there are many small signal, high gain applications that do not have this capability.

Voltage offset and drift comprise four separate error definitions: room temperature (25°C), input and output, offset, and offset drift over temperature referred to both input and output.

An in-amp should be regarded as a 2-stage amplifier with both an input and an output section. Each section has its own error sources. Because the errors of the output section are multiplied by a fixed gain (usually 2), this section is often the principal error source at low circuit gains. When the in-amp is operating at higher gains, the gain of the input stage is increased. As the gain is raised, errors contributed by the input section are multiplied, while output errors are reduced. Thus, at high gains, the input stage errors dominate.

Input errors are those contributed by the input stage alone; output errors are those due to the output section. Input-related specifications are often combined and classified together as referred to input (RTI) errors, while all output-related specifications are considered referred to output (RTO) errors. It is important to understand that although these two specifications often provide numbers that are not the same, either error term is correct because each defines the total error in a different way.

For a given gain, an in-amp's input and output errors can be calculated using the following formulas:

*Total Error, RTI* = *Input Error* + (*Output Error*/*Gain*)

*Total Error, RTO* = (*Gain* × *Input Error*) + *Output Error*

Sometimes the specification page will list an error term as RTI or RTO for a specified gain. In other cases, it is up to the user to calculate the error for the desired gain.

As an example, the total voltage offset error of the AD620A in-amp when it is operating at a gain of 10 can be calculated using the individual errors listed on its specifications page. The (typical) input offset of the AD620 ($V_{OSI}$) is listed as 30 μV. Its output offset ($V_{OSO}$) is listed as 400 μV. The total voltage offset referred to input (RTI) is equal to

$$\textit{Total RTI Error} = V_{OSI} + (V_{OSO}/G) = 30\ \mu V + (400\ \mu V/10) = 30\ \mu V + 40\ \mu V = 70\ \mu V$$

The total voltage offset referred to the output (RTO) is equal to

$$\textit{Total Offset Error RTO} = (G\ (V_{OSI})) + V_{OSO} = (10\ (30\ \mu V)) + 400\ \mu V = 700\ \mu V.$$

Note that the RTO error is 10 times greater in value than the RTI error. Logically, it should be, because at a gain of 10, the error at the output of the in-amp should be 10 times the error at the input.

**(E) Input Bias and Offset Currents**

Input bias currents are those currents flowing into or out of the input terminals of the in-amp. In-amps using FET input stages have lower room temperature bias currents than their bipolar cousins, but FET input currents double approximately every 11°C. Input bias currents can be considered a source of voltage offset error (i.e., input current flowing through a source resistance causes a voltage offset). Any change in bias current is usually of more concern than the magnitude of the bias current.

Input offset current is the difference between the two input bias currents. It leads to offset errors in in-amps when source resistances in the two input terminals are unequal.

Although instrumentation amplifiers have differential inputs, there must be a return path for their bias currents to flow to common (ground).

If this return path is not provided, the bases (or gates) of the input devices are left floating (unconnected), and the in-amp's output will rapidly drift either to common or to the supply.

Therefore, when amplifying floating input sources such as transformers (those without a center tap ground connection), ungrounded thermocouples, or any ac-coupled input sources, there must still be a dc path from each input to ground. A high value resistor of 1 MΩ to 10 MΩ connected between each input and ground will normally be all that is needed to correct this condition.

**(F) Operating Voltage Range**

A single-supply in-amp should have the same overall operating voltage range whether it is using single or dual supplies. That is, a single-supply in-amp, which is specified to operate with dual-supply voltages from ±1 V to ±18 V, should also operate over a 2 V to 36 V range with a single supply, but this may not always be the case. In fact, some in-amps, such as the AD623, will operate to even lower equivalent voltage levels in single-supply mode than with a dual-supply mode. For this reason, it is always best to check the data sheet specifications.

**(G) Quiescent Supply Current**

This specifies the quiescent or nonsignal power supply current consumed by an in-amp within a specified operating voltage range.

With the increasing number of battery-powered applications, device power consumption becomes a critical design factor. Products such as the AD627 have a very low quiescent current consumption of only 60 μA, which at 5 V is only 0.3 mW. Compare this power level to that of an older, vintage dual-supply product, such as the AD526. That device draws 14 mA with a ±15 V supply

(30 V total) for a whopping 420 mW, 1400 times the power consumption of the AD627. The implications for battery life are dramatic.

With the introduction of products such as the AD627, very impressive overall performance is achieved while only microamps of supply current are consumed. Of course, some trade-offs are usually necessary, so micropower in-amps tend to have lower bandwidth and higher noise than full power devices. The ability to operate rail-to-rail from a single-supply voltage is an essential feature of any micropower in-amp.

**(H) Settling Time**

Settling time is defined as the length of time required for the output voltage to approach, and remain within, a certain tolerance of its final value. It is usually specified for a fast full-scale input step and includes output slewing time. Since several factors contribute to the overall settling time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors to long settling times include slew rate limiting, underdamping (ringing), and thermal gradients (long tails).

**(I) Gain**

These specifications relate to the transfer function of the device. The product's gain equation is normally listed at the beginning of the specifications page.

The gain equation of the AD8221 is

$$Gain = \frac{49{,}400\ \Omega}{R_G} + 1$$

To select an $R_G$ for a given gain, solve the following equation for $R_G$:

$$R_G = \frac{49{,}400\ \Omega}{G - 1}$$

The following are samples of calculated resistance for some common gains:

G = 1: $R_G = \infty$ (open circuit)
G = 9.998: $R_G$ = 5.49 kΩ
G = 100: $R_G$ = 499 Ω
G = 991: $R_G$ = 49.9 Ω

Note that there will be a gain error if the standard resistance values are different from those calculated. In addition, the tolerance of the resistors used (normally 1% metal film) will also affect accuracy. There also will be gain drift, typically 50 ppm/°C to 100 ppm/°C, if standard resistors are used. Of course, the user must provide a very clean (low leakage) circuit board to realize an accurate gain of 1, since even a 200 MΩ leakage resistance will cause a gain error of 0.2%.

Normal metal film resistors are within 1% of their stated value, which means that any two resistors could be as much as 2% different in value from one another. Thin film resistors in monolithic integrated circuits have an absolute tolerance of only 20%. The matching between resistors on the same chip, however, can be excellent —typically better than 0.1%—and resistors on the same chip will track each other thermally, so gain drift over temperature is greatly reduced.

**(J) Gain Range**

Often specified as having a gain range of 1 to 1000, many instrumentation amplifiers will often operate at higher gains than 1000, but the manufacturer will not promise a specific level of performance.

**(K) Gain Error**

In practice, as the gain resistor becomes increasingly smaller, any errors due to the resistance of the metal runs and bond wires inside the IC package become significant. These errors, along with an increase in noise and drift, may make higher gains impractical.

In 3-op amp and in-amp designs, both gain accuracy and gain drift may suffer because the external resistor does not exactly ratio match the IC's internal resistors. Moreover, the resistor chosen is usually the closest 1% metal film value commonly available, rather than the calculated resistance value; so this adds an additional gain error. Some in-amps, such as the AD8230, use two resistors to set gain. Assuming that gain is set solely by the ratio of these two resistors in the IC, this can provide potentially significant improvement in both gain accuracy and drift. The best possible performance is provided by monolithic in-amps that have all their resistors internal to the IC, such as the AD621.

The number provided for this specification describes maximum deviation from the gain equation. Monolithic in-amps, such as the AD8221, have very low factory-trimmed gain errors. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of these external resistors and the temperature differences between individual resistors within the network all contribute to the circuit's overall gain error.

If the data eventually is digitized and fed to an intelligent system (such as a microprocessor), it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

**(L) Nonlinearity**

Nonlinearity is defined as the deviation from a straight line on the plot of an in-amp's output voltage vs. input voltage. Figure A-2 shows the transfer function of a device with exaggerated nonlinearity.

The magnitude of this error is equal to

$$Nonlinearity = \frac{Actual\ Output - Calculated\ Output}{Rated\ Full\ Scale\ Output\ Range}$$

This deviation can be specified relative to any straight line or to a specific straight line. There are two commonly used methods of specifying this ideal straight line relative to the performance of the device.

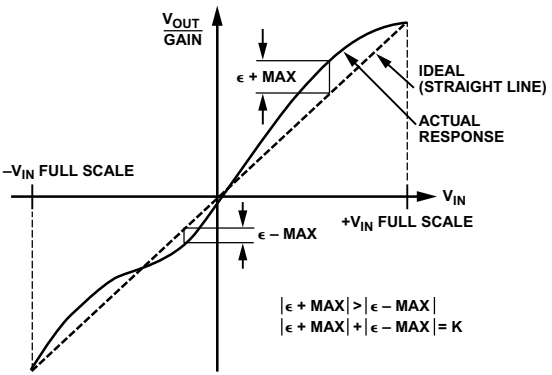



*Figure A-2. Transfer function illustrating exaggerated nonlinearity.*

The *best straight line* method of defining nonlinearity consists of measuring the peak positive and the peak negative deviation and then adjusting the gain and offset of the in-amp so that these maximum positive and negative errors are equal. For monolithic in-amps, this is usually accomplished by laser-trimming thin film resistors or by other means. The best straight line method provides impressive specifications, but it is much more difficult to perform. The entire output signal range needs to be examined before trimming to determine the maximum positive and negative deviations.

The endpoint method of specifying nonlinearity requires that any offset and/or gain calibrations are performed at the minimum and maximum extremes of the output range. Usually offset is trimmed at a very low output level, while scale factor is trimmed near the maximum output level. This makes trimming much easier to implement but may result in nonlinearity errors of up to twice those attained using the best straight line technique. This worst-case error will occur when the transfer function is bowed in one direction only.

Most linear devices, such as instrumentation amplifiers, are specified for best straight line linearity. This needs to be considered when evaluating the error budget for a particular application.

Regardless of the method used to specify nonlinearity, the errors thus created are irreducible. That is to say, these errors are neither fixed nor proportional to input or output voltage and, therefore, cannot be reduced by external adjustment.

**(M) Gain vs. Temperature**

These numbers provide both maximum and typical deviations from the gain equation as a function of temperature. As stated in the Gain Error section (K), the TC of an external gain resistor will never exactly match that of other resistors within the IC package. Therefore, the best performance over temperature is usually achieved by in-amps using all internal gain resistors. Gain drift error can be subtracted out in software by using a temperature reference and calibration data.

**(N) Key Specifications for Single-Supply In-Amps**

There are some specifications that apply to single-supply (i.e., rail-to-rail) in-amp products, which are of great importance to designers powering in-amps from low voltage, single-supply voltages.

***Input and Output Voltage Swing***

A single-supply in-amp needs to be able to handle input voltages that are very close to the supply and ground. In a typical dual-supply in-amp, the input (and output) voltage range is within about 2 V of the supply or ground. This becomes a real problem when the device is powered from a 5 V supply, or can be especially difficult when using the new 3.3 V standard. A standard in-amp operating from a 5 V single-supply line has only about 1 V of headroom remaining; with a 3.3 V supply, it has virtually none.

Fortunately, a decent single-supply in-amp, such as the AD627, will allow an output swing within 100 mV of the supply and ground. The input level is somewhat less, within 100 mV of ground and 1 V of the supply rail. In critical applications, the reference terminal of the in-amp can be moved off center to allow a symmetrical input voltage range.

# *Appendix B*

**Amplifiers Selection Table**

| Part Number | Description | Supply | Supply Volts Min to Max | Gain Setting Method | Gain Range Min to Max |
|---|---|---|---|---|---|
| AD522 | In-amp | Dual | ±5 to ±18 | Resistor | 1 to 1000 |
| AD524 | Precision IA | Dual | ±6 to ±18 | Pin select | 1 to 1000 |
| AD526 | Software-programmable amp | Dual | ±4.5 to ±16.5 | Software | 1 to 16 |
| AD620 | General-purpose IA | Dual | ±2.3 to ±18 | Resistor | 1 to 10,000 |
| AD621 | Precision IA | Dual | ±2.3 to ±18 | Pin select | 10 and 100 |
| AD622 | Low cost IA | Dual | ±2.6 to ±18 | Resistor | 1 to 1000 |
| AD623 | Single-supply, rail-to-rail IA | Both | 2.7 to 12 | Resistor | 1 to 1000 |
| AD624 | Precision IA | Dual | ±6 to ±18 | Pin select | 1 to 1000 |
| AD625 | Programmable gain IA | Dual | ±6 to ±18 | 3 resistors | 1 to 10,000 |
| AD626 | Differential amp | Both | 2.4 to 12 | Pin select | 10 and 100 |
| AD627 | Micropower IA | Both | 2.2 to 36 | Resistor | 5 to 1000 |
| AD628 | High CMV DA | Both | 4.5 to 36 | Pin/resistor | 0.1 to 100 |
| AD629 | High CMV DA | Dual | ±2.5 to ±18 | Fixed | G = 1 |
| AD8202 | High CMV DA | Single | 3.5 to 12 | Fixed | G = 20 |
| AD8203 | High CMV DA | Single | 3.5 to 13 | Fixed | G = 14 |
| AD8205 | Single-supply differential amp | Single | 4.5 to 5.5 | Fixed | G = 50 |
| AD8206 | Single-supply differential amp | Single | 4.5 to 5.5 | Fixed | G = 20 |
| AD8210 | Differential amp | Single | 4.5 to 5.5 | Fixed | G = 20 |
| AD8212 | Current sense amp | Single | 7 to 65 | Resistor | Adjustable |
| AD8213 | Dual, current sense amp | Dual | 4.5 to 5.5 | Fixed | Gain = 20 |
| AD8220 | Rail-to-rail JFET IA | Dual | ±2.3 to ±18 | Resistor | 1 to 1000 |
| AD8221 | High performance IA | Dual | ±2.3 to ±18 | Resistor | 1 to 1000 |
| AD8221 | BR grade specifications | Dual | ±2.3 to ±18 | Resistor | 1 to 1000 |
| AD8222 | High performance IA | Dual | ±2.3 to ±18 | Resistor | 1 to 1000 |
| AD8225 | Fixed G = 5 IA | Dual | ±1.7 to ±18 | Fixed | G = 5 |
| AD8230 | Zero drift IA | Both | 8 to 16 | Resistor | 2 to 1000 |
| AD8250 | Software-programmable, 10 MHz | Dual | ±5 to ±15 | Software | G = 1, 2, 5, 10 |
| AD8251 | Software-programmable, 10 MHz | Dual | ±5 to ±15 | Software | G = 1, 2, 4, 8 |
| AD8553 | Zero drift IA | Single | 1.8 to 5.5 | Resistor | 0.1 to 10,000 |
| AD8555 | Sensor amp | Single | 2.7 to 5.5 | Software | 70 to 1280 |
| AD8556 | Sensor/filter amp | Single | 2.7 to 5.5 | Software | 70 to 1280 |
| AMP03 | Precision differential amp | Dual | ±6 to ±18 | Fixed | G = 1 |

**Amplifiers Selection Table (continued)**

| Part Number | CMRR at 60 Hz G = 1, G = 1000 Min | Bandwidth G = 10 Typ | $V_{NOISE}$ p-p RTI 1 to 10 Hz Typ G = 100 | Input Offset Voltage | Temperature Range (°C) |
|---|---|---|---|---|---|
| AD522 | 75 dB[1], 100 dB[2] | 3 kHz[3] | 4 μV | 400 μV | –55 to +125 |
| AD524 | 70 dB, 110 dB | 400 kHz | 0.3 μV | 250 μV | –55 to +125 |
| AD526 | N/A | 350 kHz[4] | 3 μV | 1500 μV | –40 to +85 |
| AD620 | 73 dB, 110 dB | 800 kHz | 0.28 μV | 125 μV | –55 to +125 |
| AD621 | 93 dB, 110 dB[5] | 800 kHz | 0.28 μV | 125 μV[6] | –55 to +125 |
| AD622 | 66 dB, 103 dB | 800 kHz | 0.3 μV | 125 μV | –40 to +85 |
| AD623 | 70 dB, 105 dB | 100 kHz | 2 μV | 200 μV | –40 to +85 |
| AD624 | 70 dB, 110 dB[7] | 400 kHz | 0.3 μV | 200 μV | –55 to +125 |
| AD625 | 70 dB, 110 dB | 400 kHz | 0.3 μV | 200 μV | –40 to +85 |
| AD626 | 55 dB[5] | 100 kHz | 2 μV | 2500 μV | –40 to +85 |
| AD627 | 77 dB[8] | 30 kHz | 1.2 μV[8] | 200 μV | –40 to +85 |
| AD628 | 75 dB | 600 kHz | 15 μV | 1500 μV | –40 to +85 |
| AD629 | 77 dB | 500 kHz | 15 μV | 1000 μV | –40 to +85 |
| AD8202 | 82 dB[9] | 50 kHz[9] | 10 μV[9] | 1000 μV | –40 to +125 |
| AD8203 | 82 dB[10] | 60 kHz[10] | 10 μV[10] | 1000 μV | –40 to +125 |
| AD8205 | 78 dB[11, 12] | 50 kHz[12] | 15 μV[12] | 2000 μV | –40 to +125 |
| AD8206 | 76 dB[9, 11] | 100 kHz[9] | 15 μV[12] | 2000 μV | –40 to +125 |
| AD8210 | 100 dB[9] | 500 kHz[9] | 8 μV | 1000 μV | –40 to +150 |
| AD8212 | 90 dB[13] | 450 kHz[9] | 15 μV[12] | 1000 μV | –40 to +125 |
| AD8213 | 90 dB[13] | 450 kHz[9] | 10 μV[12] | 2000 μV | –40 to +125 |
| AD8220 | 90 dB[13], 116 dB[13] | 1 MHz | 0.8 μV | 0.8 μV | –40 to +85 |
| AD8221 | 80 dB, 130 dB | 562 kHz | 0.25 μV | 60 μV | –40 to +125 |
| AD8221 | 90 dB, 140 dB | 562 kHz | 0.25 μV | 25 μV | –40 to +125 |
| AD8222 | 80 dB, 130 dB | 750 kHz | 0.25 μV | 120 μV | –40 to +85 |
| AD8225 | 86 dB[8] | 900 kHz[8] | 1.5 μV[8] | 325 μV | –40 to +85 |
| AD8230 | 110 dB[14] | 2 kHz | 3 μV | 10 μV | –40 to +125 |
| AD8250 | 80 dB, 100 dB | 10,000 kHz | 0.4 μV | 100 μV | –40 to +125 |
| AD8251 | 80 dB, 100 dB | 10,000 kHz | 0.4 μV | 100 μV | –40 to +125 |
| AD8553 | 100 dB, 120 dB[15] | 1 kHz | 0.7 μV | 20 μV | –40 to +85 |
| AD8555 | 80 dB[16], 96 dB[17] | 700 kHz[16] | 0.5 μV | 10 μV | –40 to +125 |
| AD8556 | 80 dB[16], 94 dB[17] | 700 kHz[16] | 0.5 μV | 10 μV | –40 to +140 |
| AMP03 | 85 dB[18] | 3000 kHz[18] | 2 μV[18] | 400 μV[18] | –40 to +85 |

NOTES
[1]DC to 30 Hz
[2]DC to 1 Hz
[3]Min BW at G = 100
[4]Typ BW at G = 16
[5]CMRR at gains of 10 and 100
[6]Total offset voltage RTI at G = 100
[7]At Gain = 500
[8]At Gain = 5
[9]At Gain = 20
[10]At Gain = 14
[11]DC to 20 kHz
[12]At Gain = 50
[13]Typical
[14]At Gain of 10 to 1000
[15]At Gain = 100
[16]At Gain = 70
[17]At Gain = 1280
[18]At Gain = 1

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