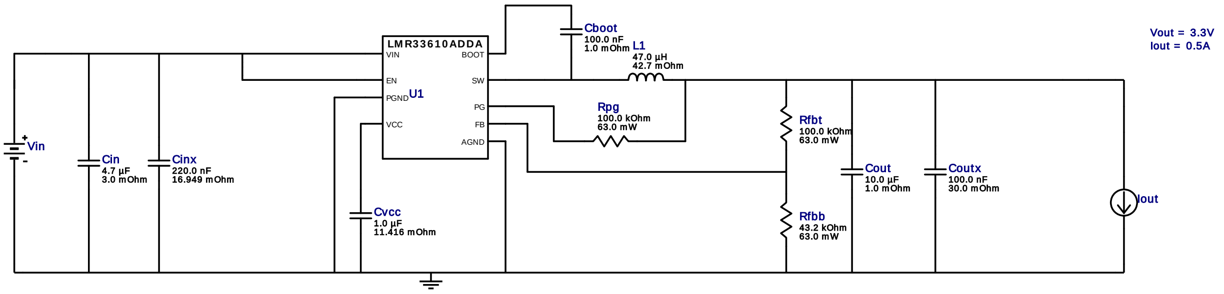
Texas Instruments

WEBENCH ® Design Report

VinMin = 5.0V
VinMax = 18.0V
Vout = 3.3V
Iout = 0.5A

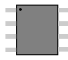
Device = LMR33610ADDAR
Topology = Buck
Created = 2025-06-02 17:38:03.887
BOM Cost = $2.85
BOM Count = 11
Total Pd = 0.07W

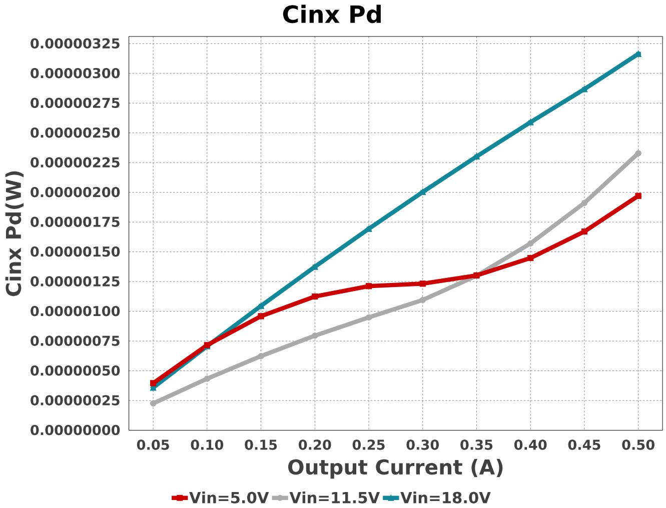
Design : 4 LMR33610ADDAR
LMR33610ADDAR 5V-18V to 3.30V @ 0.5A

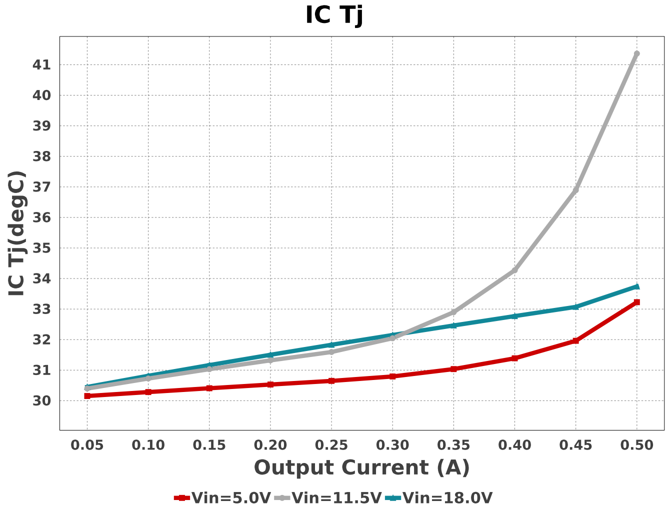


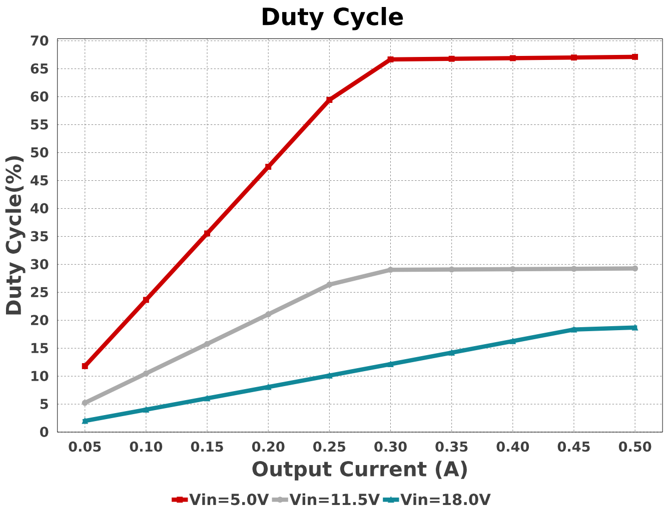
Electrical BOM

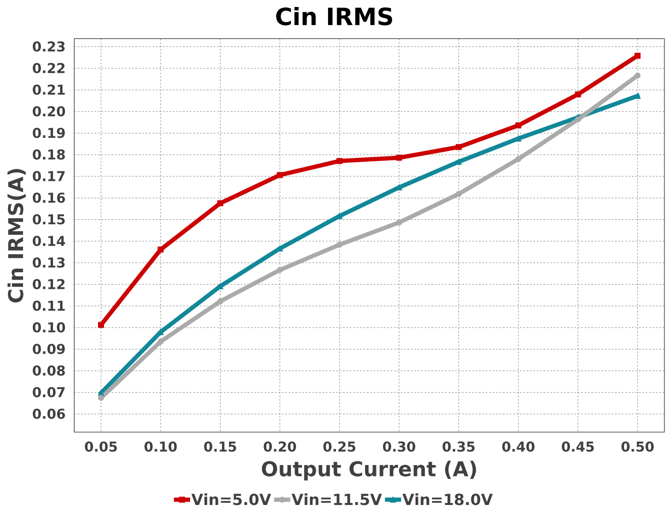
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cboot	MuRata	GRM155R71C104KA88D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 16.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
Cin	MuRata	GRM31CR71H475KA12L Series= X7R	Cap= 4.7 uF ESR= 3.0 mOhm VDC= 50.0 V IRMS= 4.98 A	1	$0.10	1206 11 mm^2
Cinx	TDK	C2012X7R1H224K125AA Series= X7R	Cap= 220.0 nF ESR= 16.949 mOhm VDC= 50.0 V IRMS= 1.5961 A	1	$0.03	0805 7 mm^2
Cout	MuRata	GRM155R60J106ME15D Series= X5R	Cap= 10.0 uF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 3.52 A	1	$0.03	0402 3 mm^2
Coutx	MuRata	GRM188R71C104KA01D Series= X7R	Cap= 100.0 nF ESR= 30.0 mOhm VDC= 16.0 V IRMS= 1.7 A	1	$0.01	0603 5 mm^2
Cvcc	TDK	C1005X5R1V105K050BC Series= X5R	Cap= 1.0 uF ESR= 11.416 mOhm VDC= 35.0 V IRMS= 1.483 A	1	$0.03	0402 3 mm^2
L1	Vishay-Dale	IHLP6767DZER470M11	L= 47.0 µH 42.7 mOhm	1	$1.98	IHLP-6767DZ 369 mm^2
Rfbb	Vishay-Dale	CRCW040243K2FKED Series= CRCW..e3	Res= 43.2 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm^2
Rfbt	Vishay-Dale	CRCW0402100KFKED Series= CRCW..e3	Res= 100.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm^2
Rpg	Vishay-Dale	CRCW0402100KFKED Series= CRCW..e3	Res= 100.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm^2

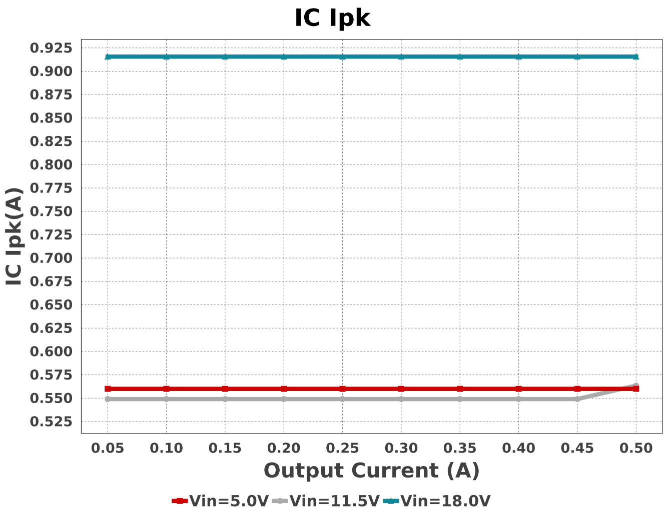
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
U1	Texas Instruments	LMR33610ADDAR	Switcher	1	$0.63	 DDA0008J 55 mm^2

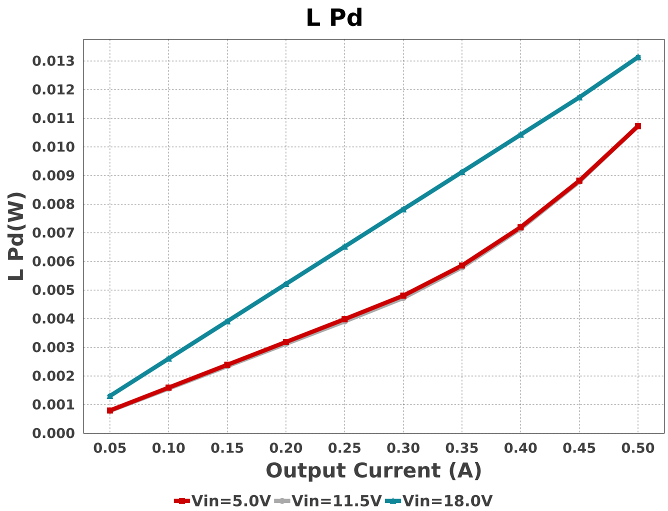


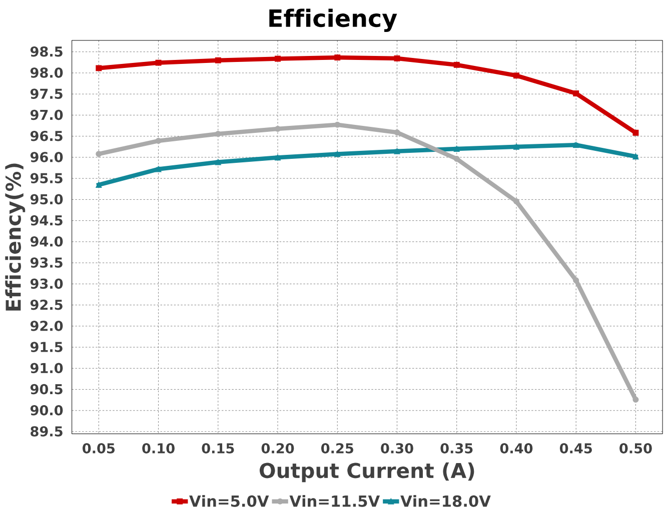


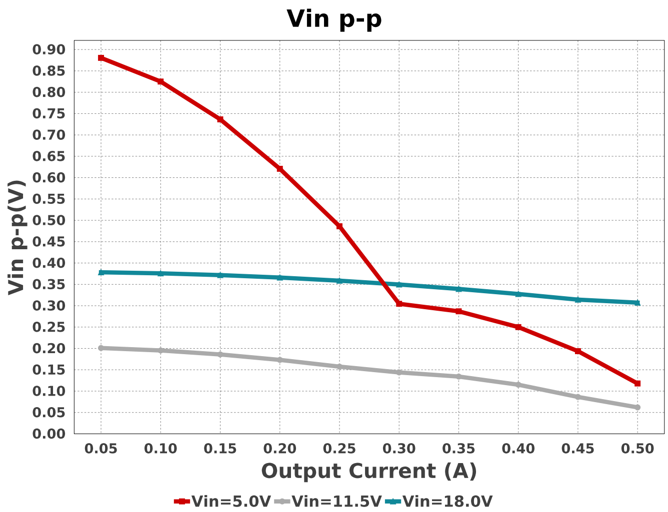


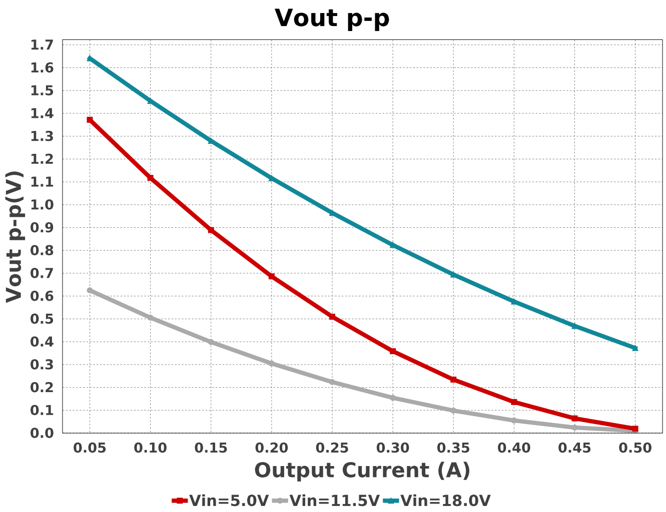


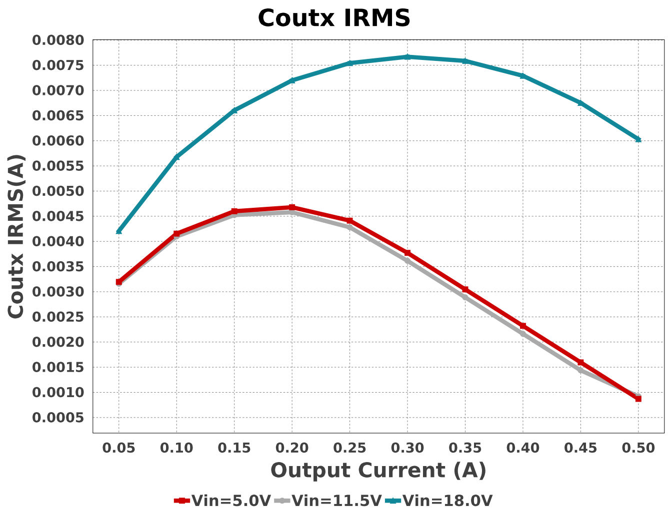


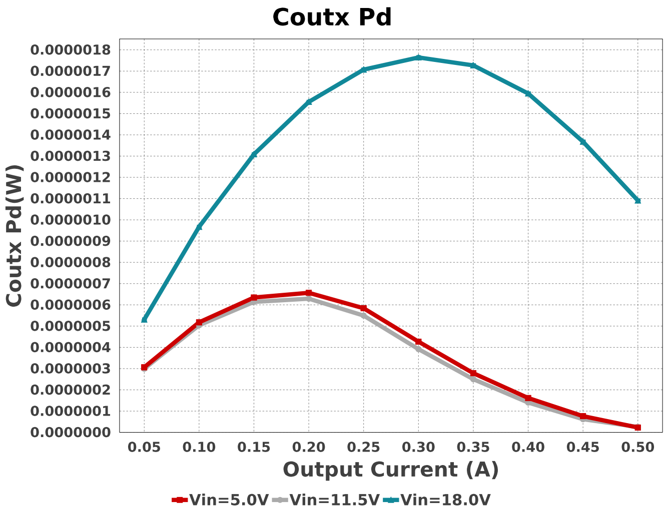


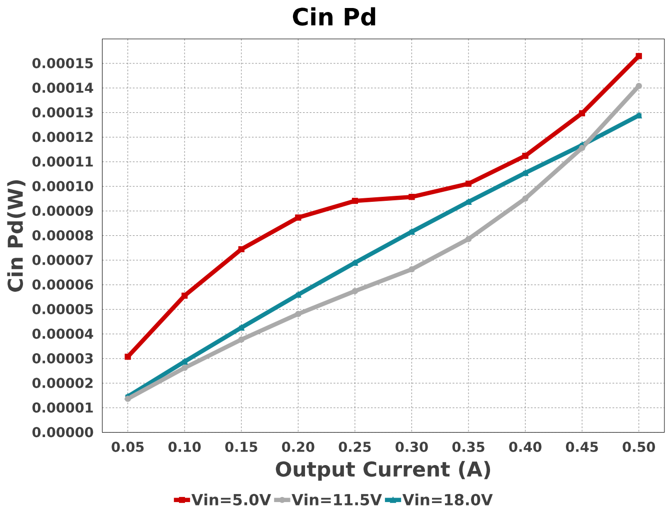

Efficiency
Efficiency(%)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

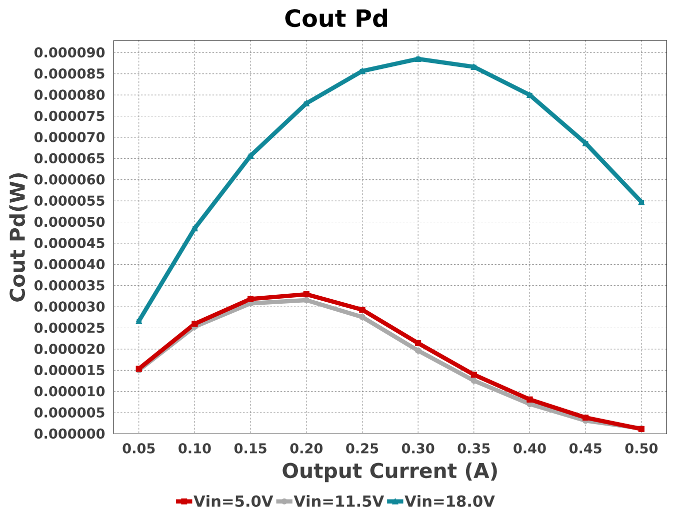

Vin p-p
Vin p-p(V)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

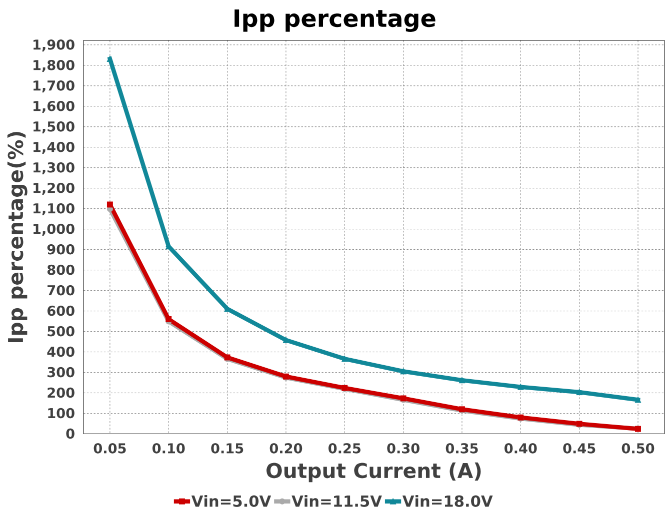

Vout p-p
Vout p-p(V)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

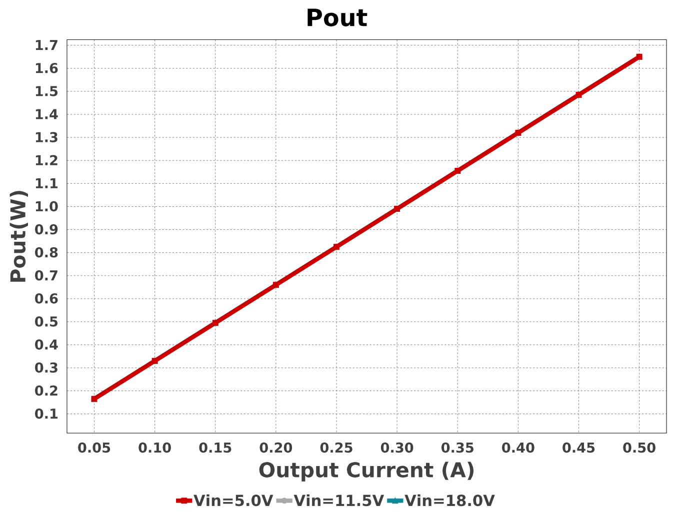

Coutx IRMS
Coutx IRMS(A)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

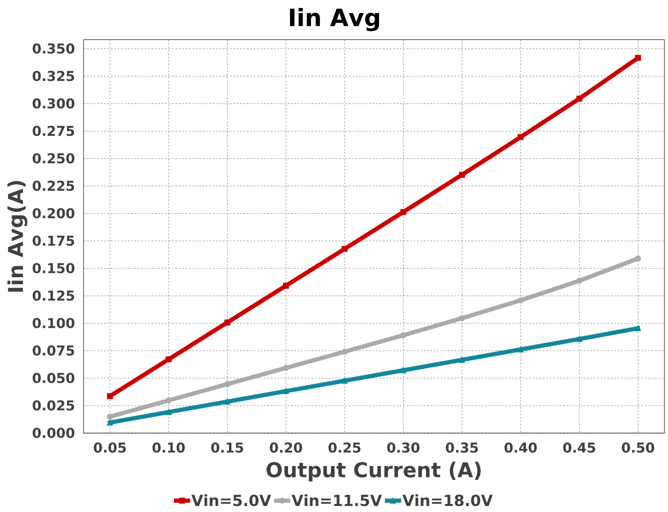

Coutx Pd
Coutx Pd(W)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

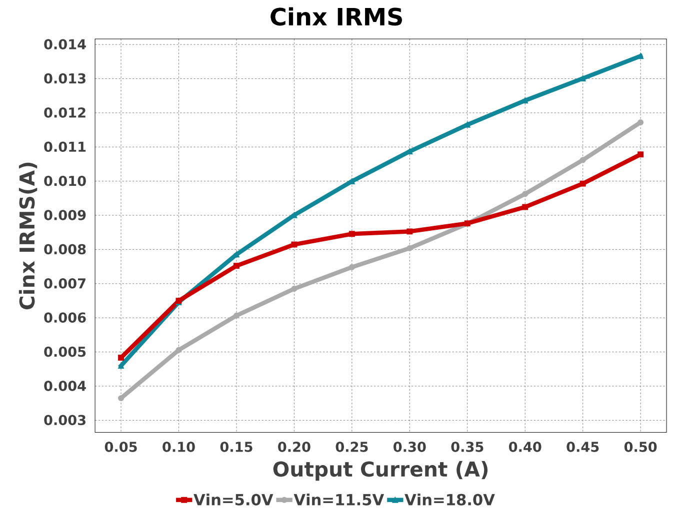

Cin Pd
Cin Pd(W)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

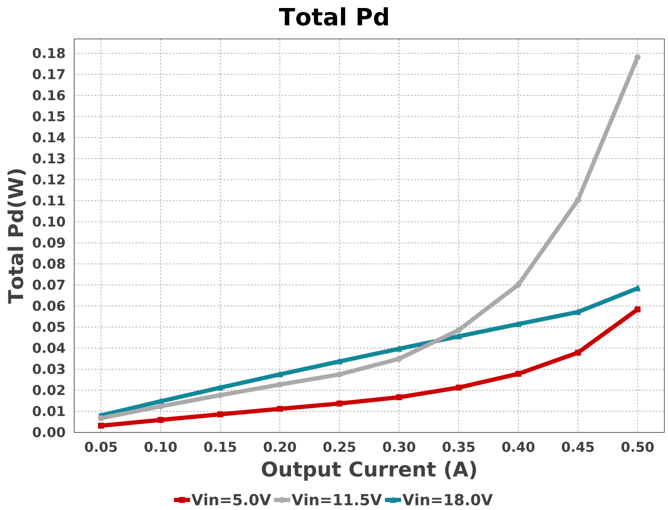

Cout Pd
Cout Pd(W)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

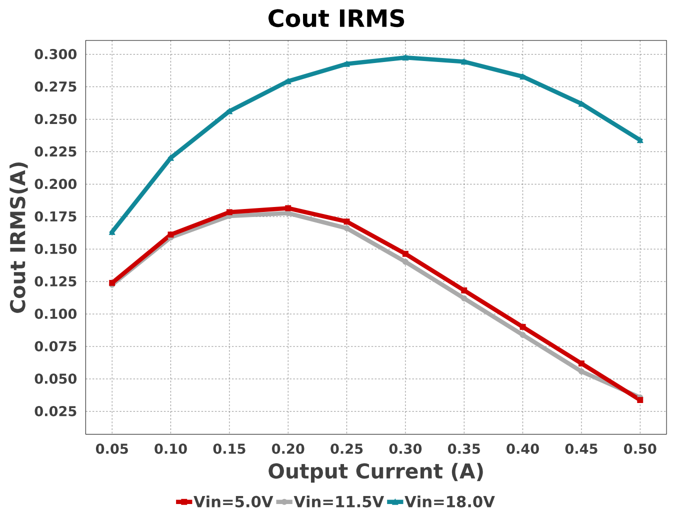

Ipp percentage
Ipp percentage(%)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

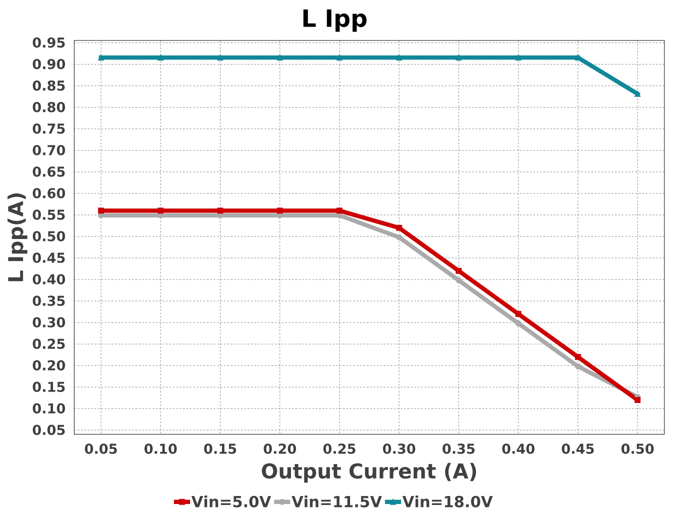

Pout
Pout(W)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

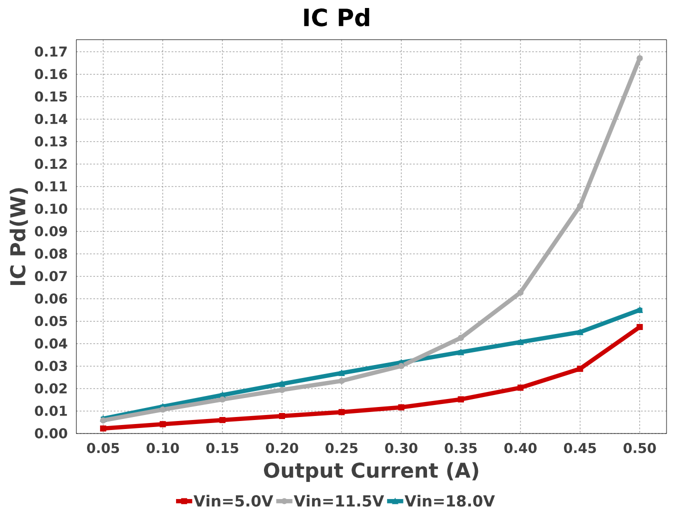

Iin Avg
Iin Avg(A)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

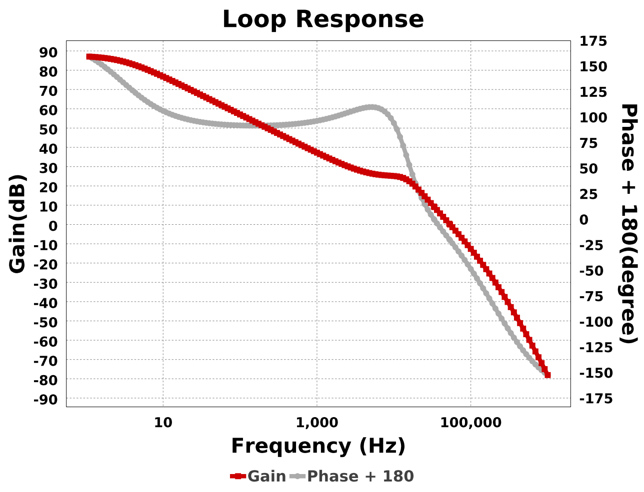

Cinx IRMS
Cinx IRMS(A)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V

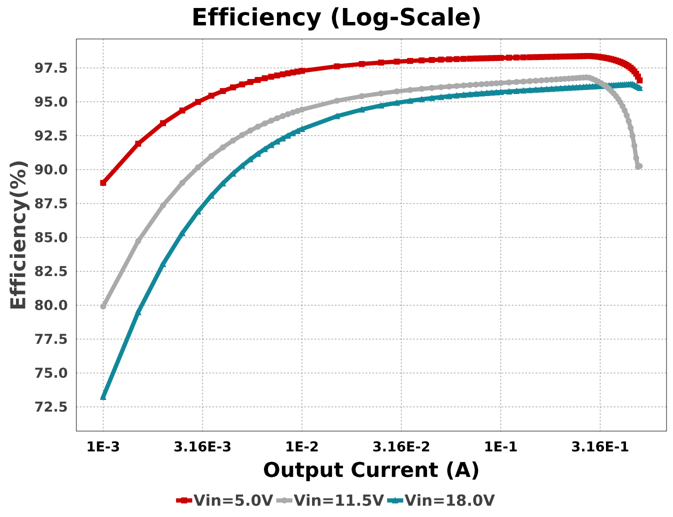

Total Pd
Total Pd(W)
Output Current (A)
Vin=5.0V Vin=11.5V Vin=18.0V











Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	207.237 mA	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	128.84 µW	Capacitor	Input capacitor power dissipation
3.	Cinx IRMS	13.662 mA	Capacitor	Bulk capacitor RMS ripple current
4.	Cinx Pd	3.164 µW	Capacitor	Bulk capacitor power dissipation
5.	Cout IRMS	233.967 mA	Capacitor	Output capacitor RMS ripple current
6.	Cout Pd	54.741 µW	Capacitor	Output capacitor power dissipation
7.	Coutx IRMS	6.031 mA	Capacitor	Output capacitor_x RMS ripple current
8.	Coutx Pd	1.091 µW	Capacitor	Output capacitor_x power loss
9.	IC Ipk	915.688 mA	IC	Peak switch current in IC
10.	IC Pd	55.013 mW	IC	IC power dissipation
11.	IC Tj	33.741 degC	IC	IC junction temperature

#	Name	Value	Category	Description
12.	IC Tolerance	15.0 mV	IC	IC Feedback Tolerance
13.	ICThetaJA	68.0 degC/W	IC	IC junction-to-ambient thermal resistance
14.	Iin Avg	95.467 mA	IC	Average input current
15.	Ipp percentage	166.275 %	Inductor	Inductor ripple current percentage (with respect to average inductor current)
16.	L Ipp	831.38 mA	Inductor	Peak-to-peak inductor ripple current
17.	L Pd	13.134 mW	Inductor	Inductor power dissipation
18.	Cin Pd	128.84 µW	Power	Input capacitor power dissipation
19.	Cinx Pd	3.164 µW	Power	Bulk capacitor power dissipation
20.	Cout Pd	54.741 µW	Power	Output capacitor power dissipation
21.	Coutx Pd	1.091 µW	Power	Output capacitor_x power loss
22.	IC Pd	55.013 mW	Power	IC power dissipation
23.	L Pd	13.134 mW	Power	Inductor power dissipation
24.	Total Pd	68.41 mW	Power	Total Power Dissipation
25.	BOM Count	11	System Information	Total Design BOM count
26.	Duty Cycle	18.708 %	System Information	Duty cycle
27.	Efficiency	96.019 %	System Information	Steady state efficiency
28.	FootPrint	465.0 mm^2	System Information	Total Foot Print Area of BOM components
29.	Frequency	70.16 kHz	System Information	Switching frequency
30.	Iout	500.0 mA	System Information	Iout operating point
31.	Mode	PFM	System Information	Conduction Mode
32.	Pout	1.65 W	System Information	Total output power
33.	Total BOM	$2.85	System Information	Total BOM Cost
34.	Vin	18.0 V	System Information	Vin operating point
35.	Vin p-p	307.262 mV	System Information	Peak-to-peak input voltage
36.	Vout	3.3 V	System Information	Operational Output Voltage
37.	Vout Actual	3.315 V	System Information	Vout Actual calculated based on selected voltage divider resistors
38.	Vout Tolerance	2.932 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
39.	Vout p-p	372.425 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	500.0 m	Maximum Output Current
VinMax	18.0	Maximum input voltage
VinMin	5.0	Minimum input voltage
Vout	3.3	Output Voltage
base_pn	LMR33610A-SOIC	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

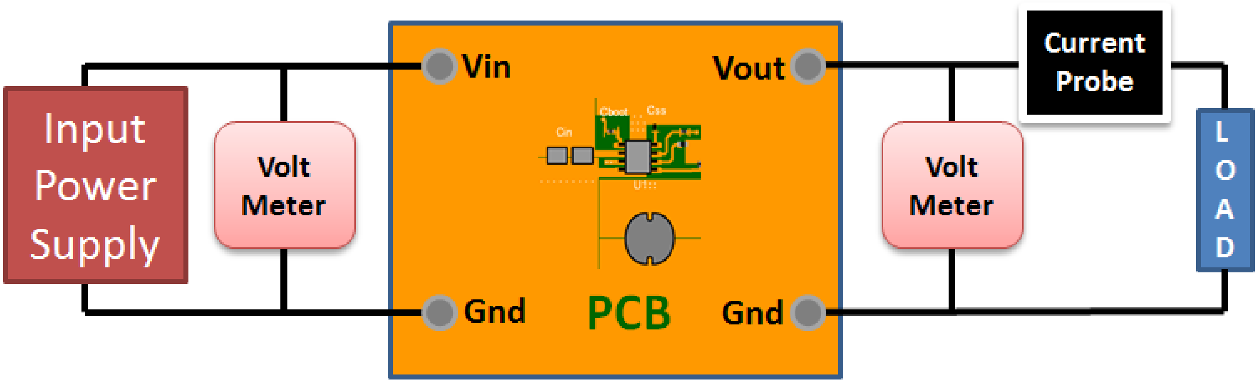
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 5.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply.
If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : EE683FB51B2946E410D522AE64B7CAAC[v1]

2. **LMR33610A-SOIC** Product Folder : http://www.ti.com/product/LMR33610 : contains the data sheet and other resources.

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