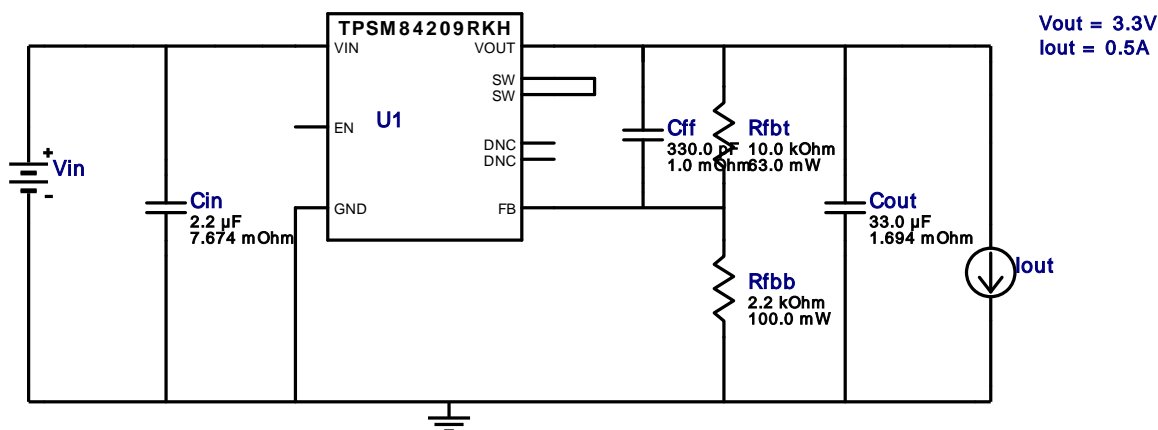


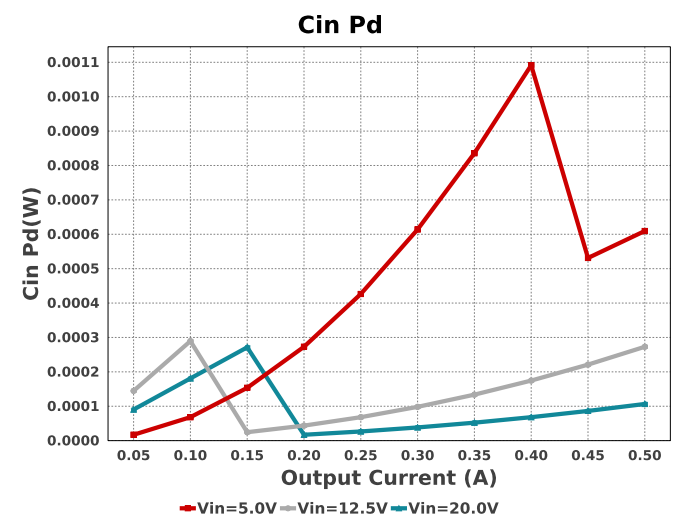
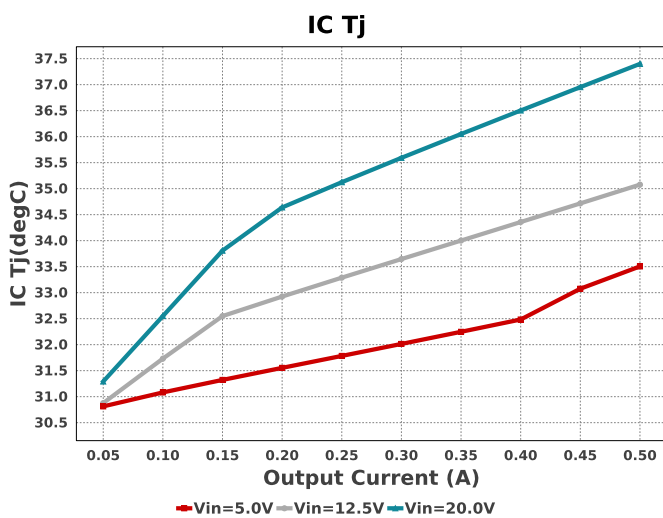
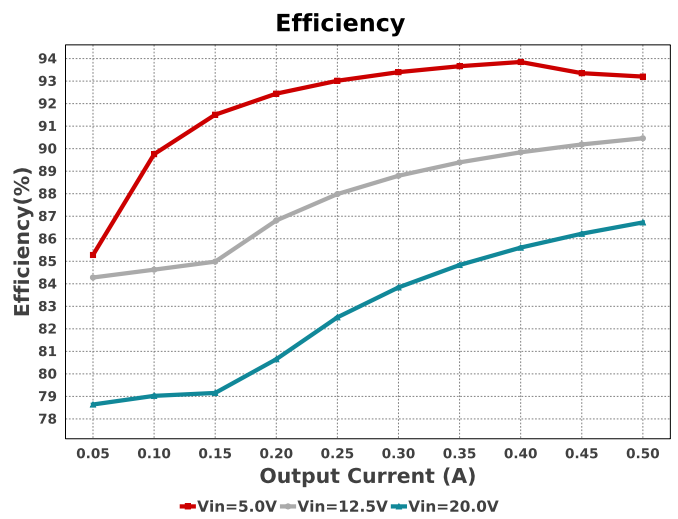
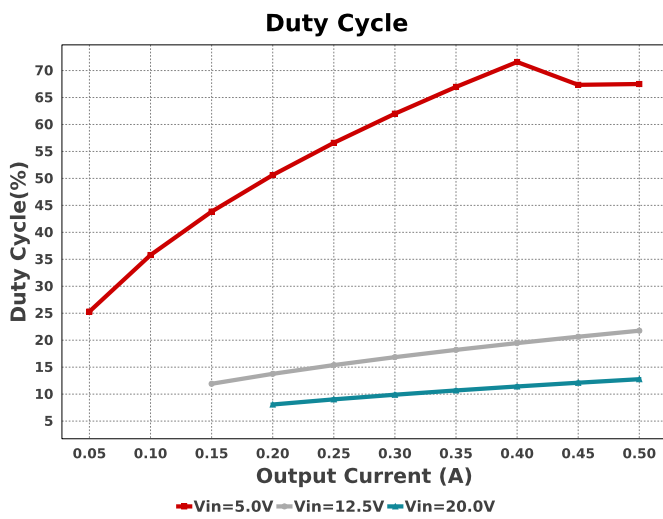
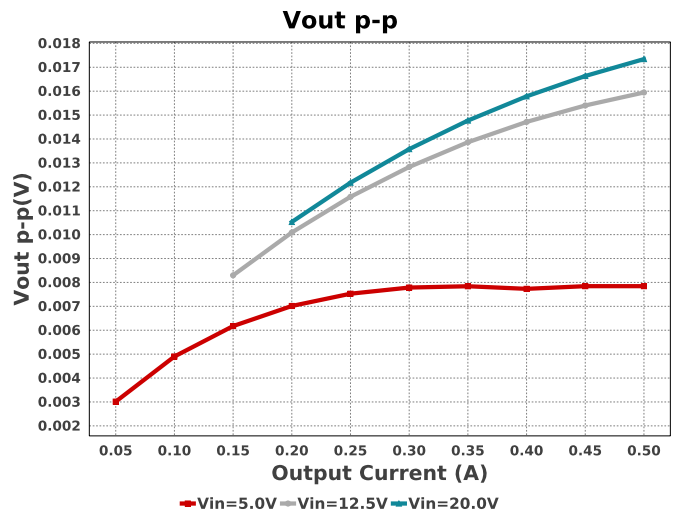
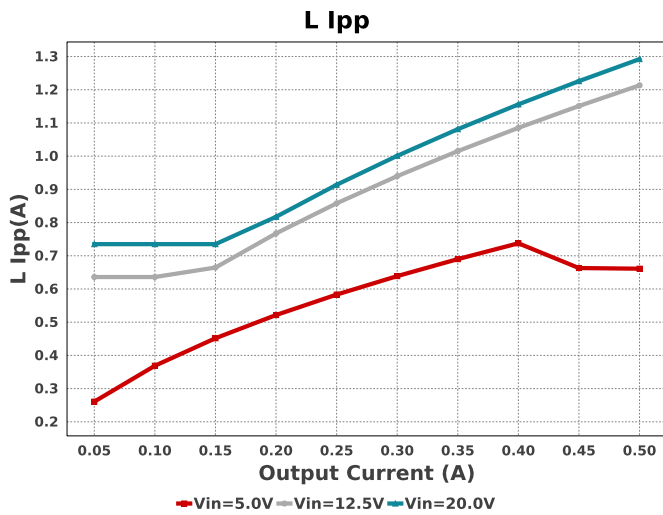
WEBENCH® Design Report

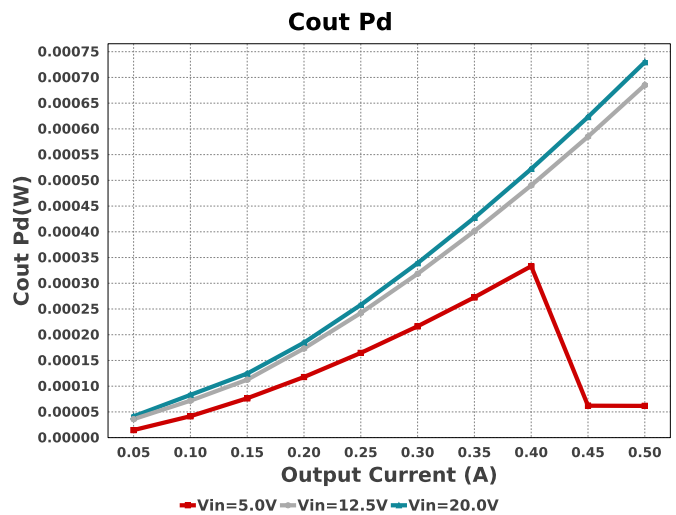
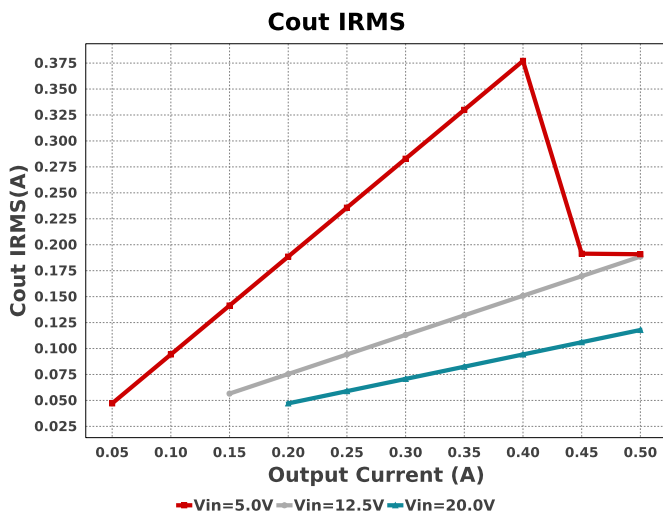
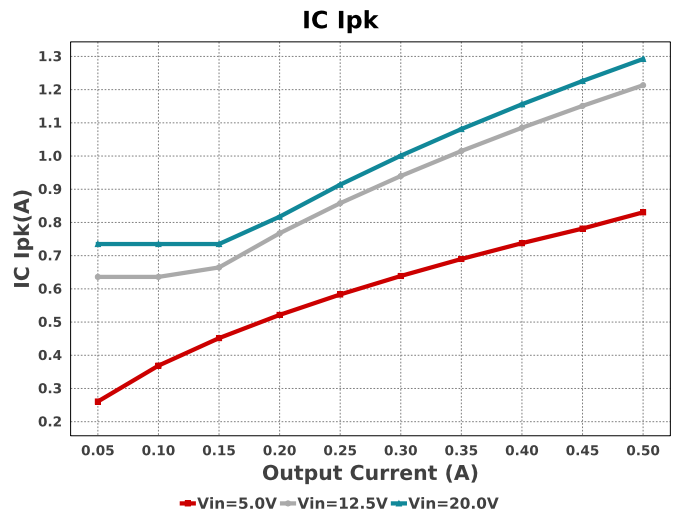
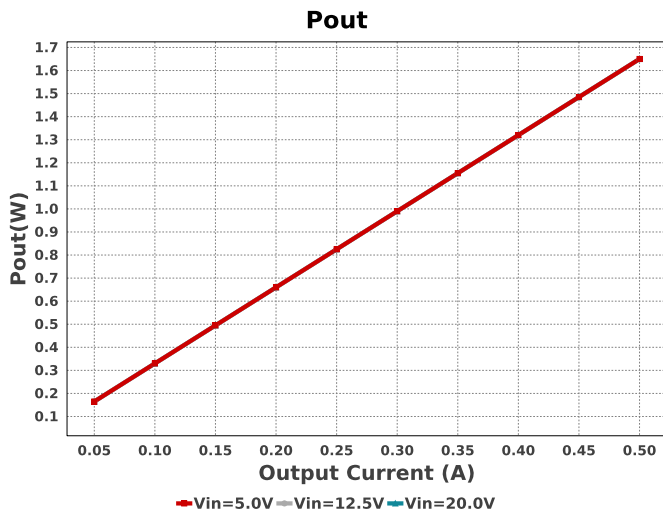
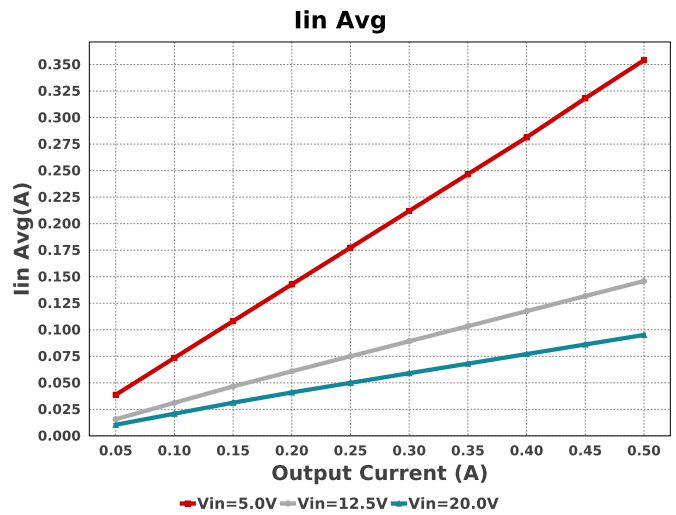
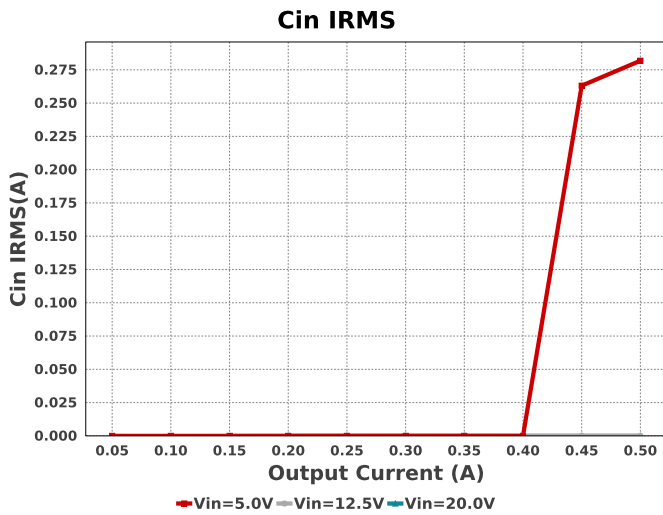
Design : 8 TPSM84209RKHR
 TPSM84209RKHR 5V-20V to 3.30V @ 0.5A

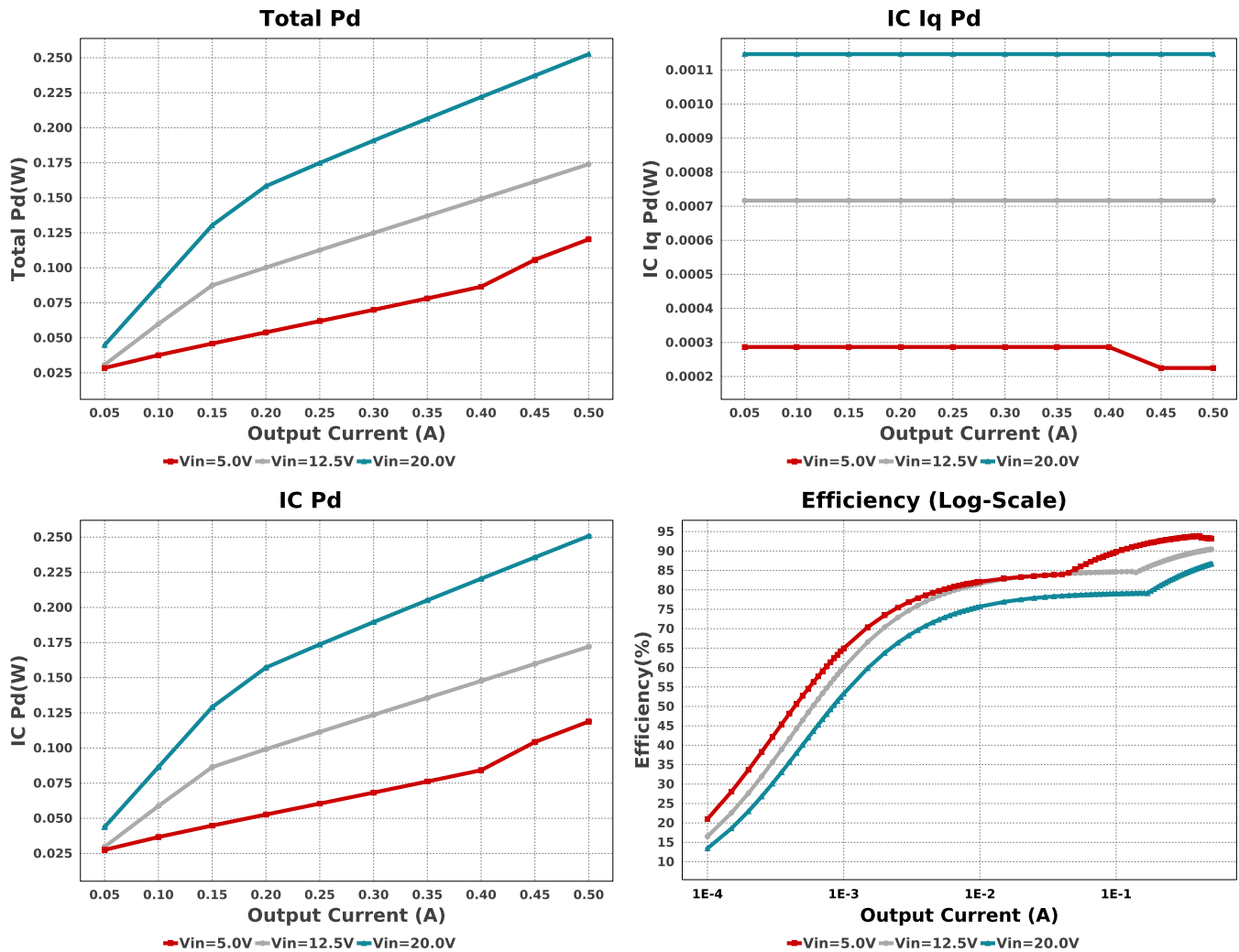


Electrical BOM

Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cff	MuRata	GRM033R71E331KA01D Series= X7R	Cap= 330.0 pF ESR= 1.0 mOhm VDC= 25.0 V IRMS= 0.0 A	1	\$0.01	0201 2 mm ²
Cin	TDK	C1608X5R1V225K080AC Series= X5R	Cap= 2.2 uF ESR= 7.674 mOhm VDC= 35.0 V IRMS= 1.87823 A	1	\$0.04	0603 5 mm ²
Cout	TDK	C2012X5R1A336M125AC Series= X5R	Cap= 33.0 uF ESR= 1.694 mOhm VDC= 10.0 V IRMS= 5.0128 A	1	\$0.26	0805 7 mm ²
Rfbb	Yageo	RC0603FR-072K2L Series= ?	Res= 2.2 kOhm Power= 100.0 mW Tolerance= 1.0%	1	\$0.01	0603 5 mm ²
Rfbb	Vishay-Dale	CRCW040210K0FKED Series= CRCW..e3	Res= 10.0 kOhm Power= 63.0 mW Tolerance= 1.0%	1	\$0.01	0402 3 mm ²
U1	Texas Instruments	TPSM84209RKHR	Switcher	1	\$1.40	RKH0009A 28 mm ²







Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	1.878 A	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	106.59 μ W	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	117.857 mA	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	729.71 μ W	Capacitor	Output capacitor power dissipation
5.	IC Ipk	1.292 A	IC	Peak switch current in IC
6.	IC Iq Pd	1.147 mW	IC	IC Iq Pd
7.	IC Pd	250.83 mW	IC	IC power dissipation
8.	IC Tj	37.4 degC	IC	IC junction temperature
9.	ICThetaJA	29.5 degC/W	IC	IC junction-to-ambient thermal resistance
10.	Iin Avg	95.128 mA	IC	Average input current
11.	L Ipp	1.292 A	Inductor	Peak-to-peak inductor ripple current
12.	Cin Pd	106.59 μ W	Power	Input capacitor power dissipation
13.	Cout Pd	729.71 μ W	Power	Output capacitor power dissipation
14.	IC Pd	250.83 mW	Power	IC power dissipation
15.	Total Pd	252.565 mW	Power	Total Power Dissipation
16.	BOM Count	6	System	Total Design BOM count
17.	Duty Cycle	12.768 %	System	Duty cycle
18.	Efficiency	86.725 %	System	Steady state efficiency
19.	FootPrint	49.0 mm ²	System	Total Foot Print Area of BOM components
20.	Frequency	750.0 kHz	System	Switching frequency
21.	Iout	500.0 mA	System	Iout operating point
22.	Mode	DCM	System	PWM/PFM Mode
23.	Pout	1.65 W	System	Total output power

#	Name	Value	Category	Description
24.	Total BOM	\$1.73	System Information	Total BOM Cost
25.	Vin	20.0 V	System Information	Vin operating point
26.	Vout Actual	3.305 V	System Information	Vout Actual calculated based on selected voltage divider resistors
27.	Vout Tolerance	1.656 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
28.	Vout p-p	17.342 mV	System Information	Peak-to-peak output ripple voltage

Design Inputs

Name	Value	Description
Iout	500.0 m	Maximum Output Current
VinMax	20.0	Maximum input voltage
VinMin	5.0	Minimum input voltage
Vout	3.3	Output Voltage
base_pn	TPSM84209	Base Product Number
source	DC	Input Source Type
Ta	30.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of C_{in} and C_{out} , and the inductance and DC resistance of $L1$ before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab down to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 5.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to V_{in} and GND. Connect a digital volt meter and a load if needed to set the minimum load of the design from V_{out} and GND. Turn on the input supply and slowly turn up the current limit on the input supply. If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between V_{in} and GND, a load is connected between V_{out} and GND and a current meter is connected in series between V_{out} and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : EE683FB51B2946E410D522AE64B7CAAC[v1]
2. **TPSM84209** Product Folder : <http://www.ti.com/product/TPSM84209> : contains the data sheet and other resources.

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