Instruction Name	opcode	func code	Instruction Format	9 bit distribution	Description of implementation	Example
blt	001	-	Type 1	3 opcode, 3 reg, 3 reg1	if reg < reg1, go to label in r0	blt reg, reg1
beq	010	-	Type 1	3 opcode, 3 reg, 3 reg1	if reg == reg1, go to label in r0	beq reg, reg1
sl	011	-	Type 1	3 opcode, 3 reg, 3 reg1	reg = reg << reg1	sl reg, reg1
sr	100	-	Type 1	3 opcode, 3 reg, 3 reg1	reg = reg >> reg1 (pad with signed bit)	sr reg, reg1
sro	101	-	Type 1	3 opcode, 3 reg, 3 reg1	reg = reg >> reg1 (pad wih ov bit)	sro reg, reg1
set	110	-	Type 2	3 opcode, 6 imm	r0 = imm	set 46
sti	111	-	Type 3	3 opcode, 3 reg, 3 imm	reg = imm	sti reg, 5
halt	000	000	Type 4	3 opcode, 3 free, 3 func	done	halt
lw	000	001	Type 4	3 opcode, 3 reg, 3 func	reg = M[r0]	lw reg
sw	000	010	Type 4	3 opcode, 3 reg, 3 func	M[r0] = reg	sw reg
add	000	011	Type 4	3 opcode, 3 reg, 3 func	r0 = r0 + reg + ov	add reg
comp	000	100	Type 4	3 opcode, 3 reg, 3 func	reg = -reg	comp reg
mov	000	101	Type 4	3 opcode, 3 reg, 3 func	reg = r0	mov reg
j	000	110	Type 4	3 opcode, 3 free, 3 func	jump to r0	j
clr	000	111	Type 4	3 opcode, 3 free, 3 func	ov = 0	clr