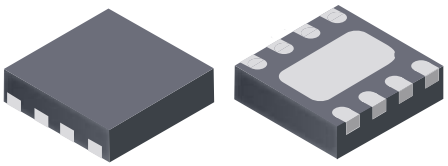
Dual Half Bridge Motor Driver

Features and Benefits

- Low $R_{DS(on)}$ outputs
- Standby mode with zero current drain
- Small 2 × 2 DFN package
- Crossover Current protection
- Thermal Shutdown protection

Package: 8-contact DFN with Exposed Thermal Pad (suffix EE)



Not to scale

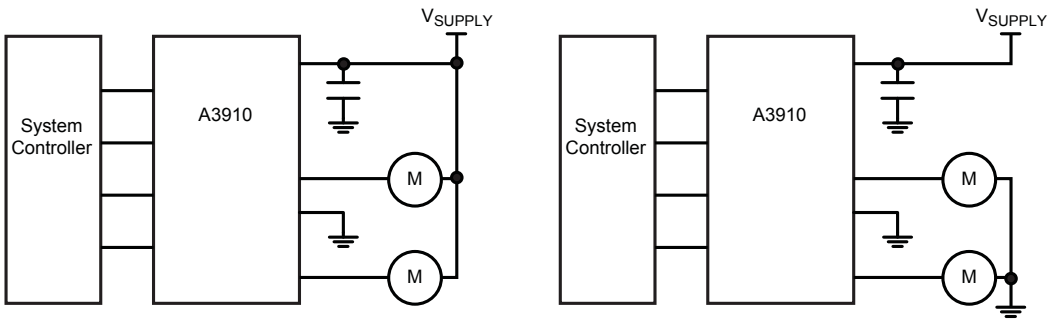
Description

The A3910 is a dual half bridge motor driver, designed for low cost, low voltage battery operated power applications. The outputs are rated for operation up to 500 mA.

Direct control of high- and low-side drivers is implemented to allow either high-side or low-side PWM. The motor can be connected to either supply or GND. Using a MOS switch results in improved braking action for the motor, compared to implementation with simple clamp diode.

The A3910 is supplied in a 2 mm × 2 mm 8-contact DFN package (EE) with exposed thermal pad. The package is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Diagram



(A) Connection to Supply

(B) Connection to Ground

Selection Guide

Part Number	Packing*	Package
A3910EEETR-T	3000 pieces per 7-in. reel	8-contact DFN with exposed thermal pad

*Contact Allegro™ for additional packing options.

Absolute Maximum Ratings*

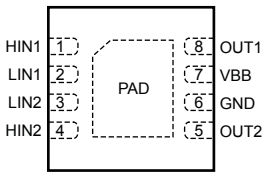
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		–0.3 to 5.5	V
Logic Input Voltage Range	V_{IN}		–0.3 to 6	V
Output Current	I_{OUT}		500	mA
Output Voltage	V_{OUT}		–0.3 to V_{BB} + 1	V
Operating Ambient Temperature	T_A	E temperature range	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	49	ºC/W
		On 2-layer PCB based with 0.23 in.^{2} exposed copper each side	92	ºC/W

*Additional thermal information available on the Allegro website.

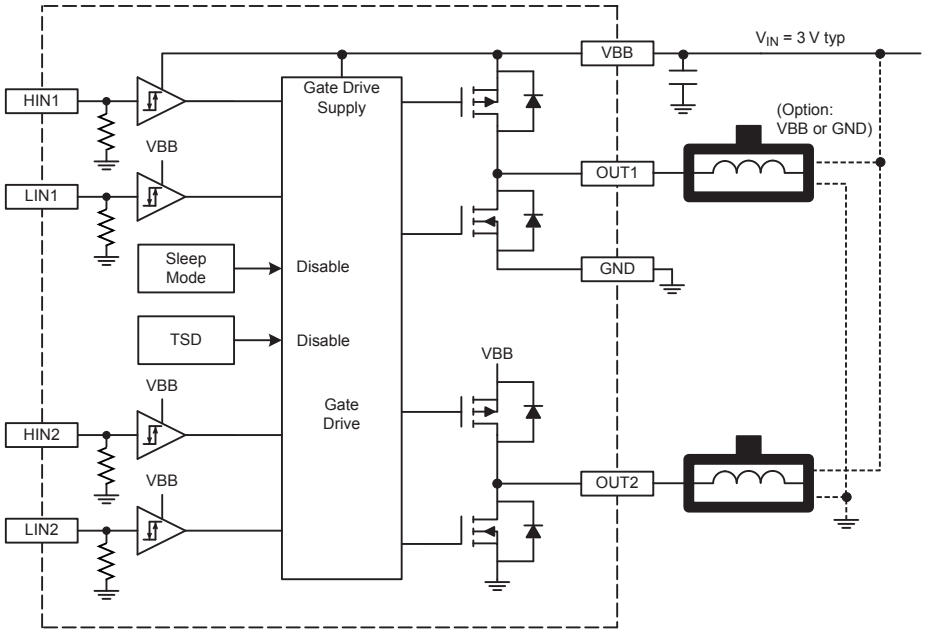
Pin-out Diagram



Terminal List Table

Number	Name	Function
1	HIN1	Logic input
2	LIN1	Logic input
3	LIN2	Logic input
4	HIN2	Logic input
5	OUT2	Motor terminal
6	GND	Ground
7	VBB	Input Supply
8	OUT1	Motor terminal

Functional Block Diagram



ELECTRICAL CHARACTERISTICS* Valid at T_A = 25°C; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBB Supply Range	V_{BB}		2.5	–	5.5	V
VBB Supply Current	I_{BB}	Both bridges, PWM = 50 kHz	–	0.3	1	mA
		Sleep mode (HIN1 = HIN2 = LIN1 = LIN2 = 0 V)	–	<1	1	µA
Output Driver On-Resistance	$R_{DS(on)}$	Source driver, I = 400 mA, V_{BB} = 3 V	–	1.1	1.4	Ω
		Source driver, I = 400 mA, V_{BB} = 5 V	–	0.8	1	Ω
		Sink driver, I = 400 mA, V_{BB} = 3 V	–	0.5	0.65	Ω
		Sink driver, I = 400 mA, V_{BB} = 5 V	–	0.4	0.52	Ω
Input Logic Low Level	V_{IL}		–	–	0.5	V
Input Logic High Level	V_{IH}		V_{BB} / 2	–	–	V
Input Hysteresis	V_{HYS}		50	150	300	mV
Logic Input Current	I_{IN}	V_{IN} = 3.3 V (Pulldown = 100 kΩ)	–	33	50	µA
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	15	–	°C

*Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

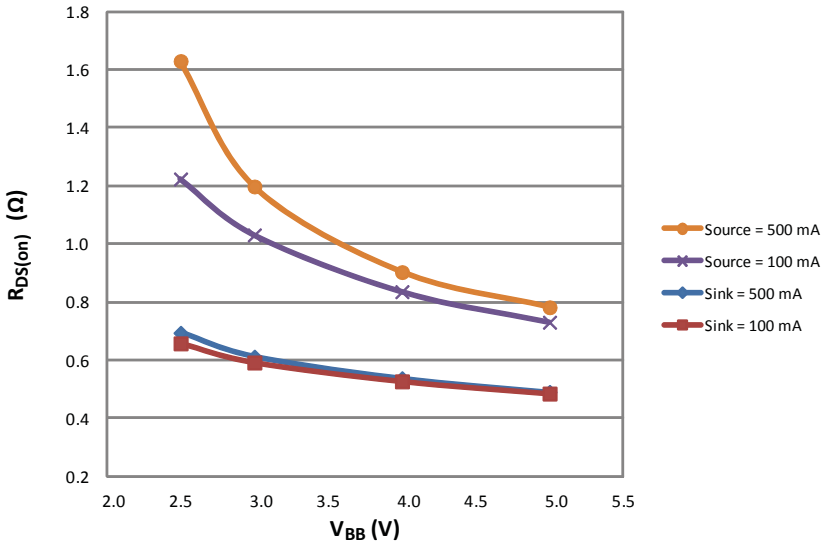
Logic Table

HINx	LINx	OUTx	Function Motor to Supply	Function Motor to GND
0	0	Hi-Z[1]	Coast (Sleep[2])	Coast (Sleep[2])
1	0	High	Brake	Drive
0	1	Low	Drive	Brake
1	1	Hi-Z[1]	Coast	Coast

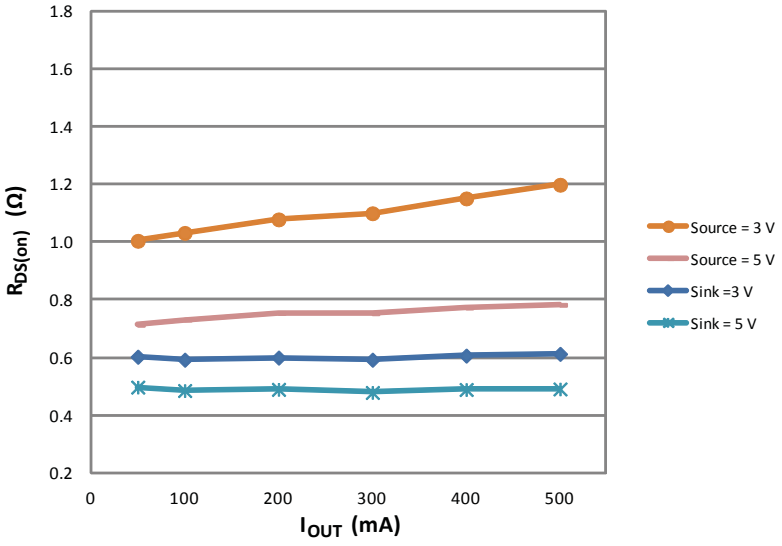
[1]Hi-Z is high impedance.
[2]Sleep mode activated by all four inputs <100 mV.

Characteristic Performance

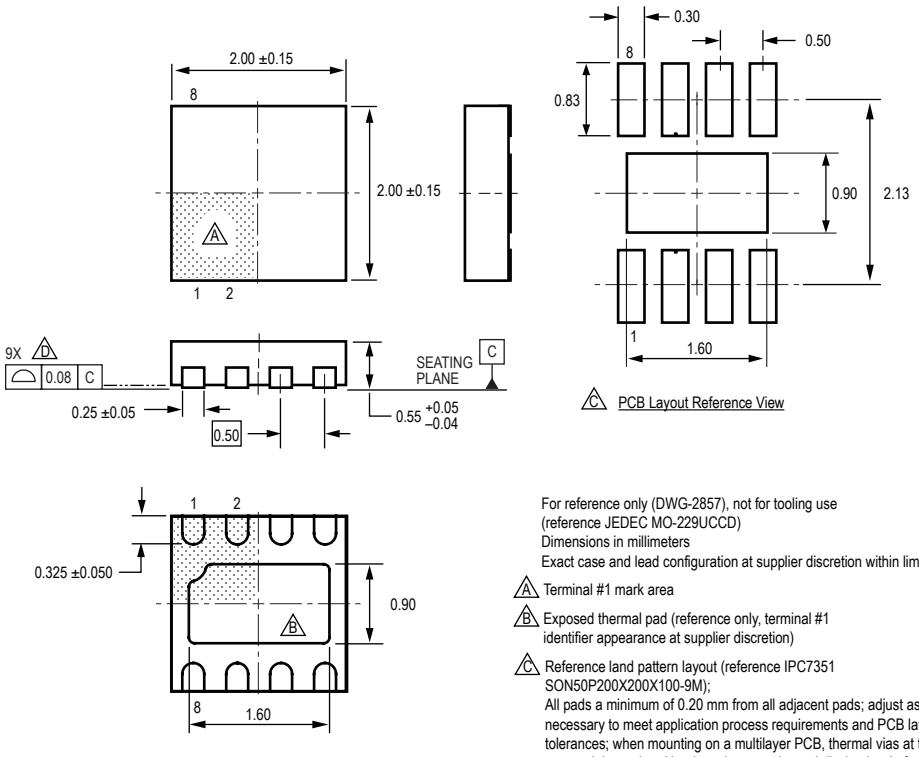
Output On-Resistance versus Load Supply Voltage



Output On-Resistance versus Output Current



Package EE, 8-Contact DFN with Exposed Thermal Pad



For reference only (DWG-2857), not for tooling use (reference JEDEC MO-229UCCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	July 23, 2013	Update Selection Guide

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