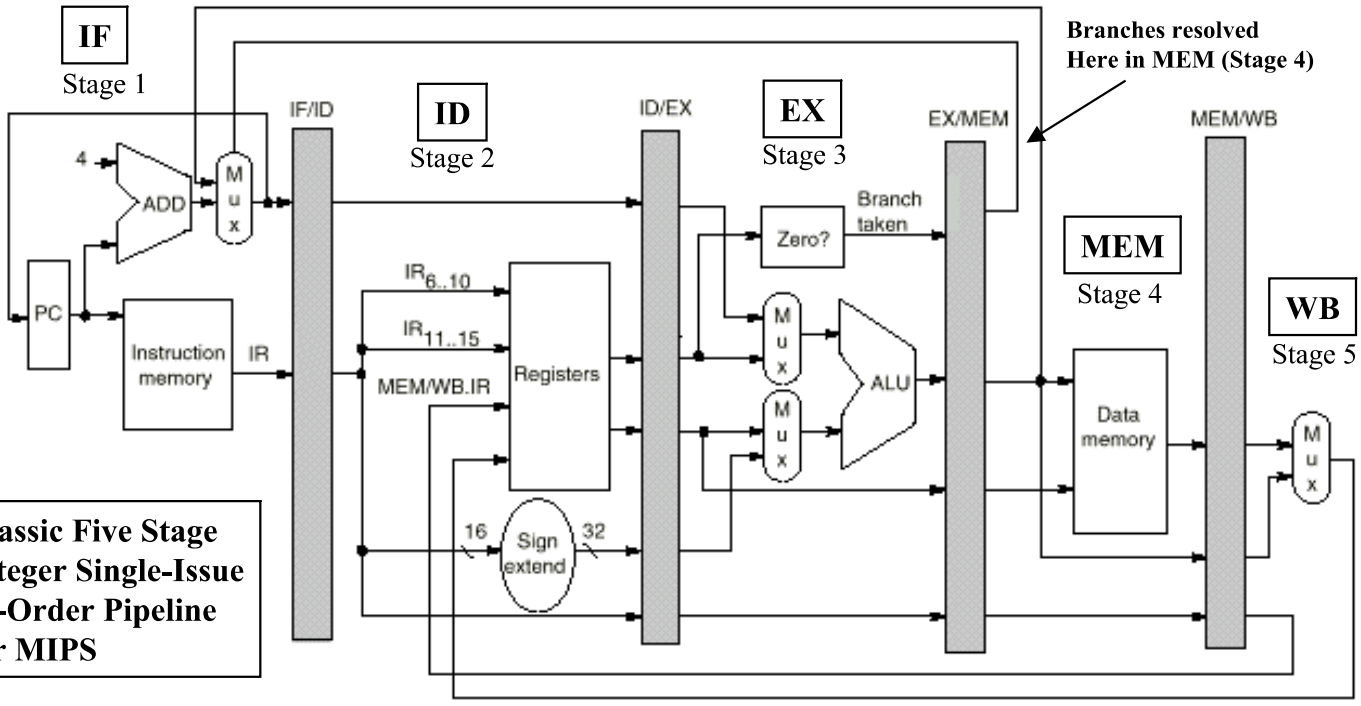
A Pipelined MIPS Integer Datapath

Pipeline Version 1 (in 550): No Forwarding, Branch resolved in MEM stage

- **Assume <u>register writes</u> occur in <u>first half of cycle</u> and <u>register reads occur in second half</u>.**



Classic Five Stage Integer Single-Issue In-Order Pipeline for MIPS

The datapath is pipelined by adding a set of registers, one between each pair of pipe stages.

Branch Penalty = 4 -1 = 3 cycles

(In Appendix A and 550)