# OMICRON

A 16-Bit Pipelined CPU

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# OVERVIEW

- General Purpose Pipelined CPU written in Verilog HDL
- Five Stages
  - Instruction Fetch
  - Instruction Decode
  - Execute
  - Memory
  - Write Back
- RISC Architecture
  - Based off of 32-bit MIPS
  - Omicron is a 16-bit processor

# INSTRUCTION SET ARCHITECTURE (ISA)

- Three Opcode Types:
  - Math Type (ADD, SUB, AND, OR, etc.)

| OpCode [15-12] | Source 1 [11-9] | Destination [8-6] | Source 2 [5-3] | Not Used [2-0] |
|---|---|---|---|---|

  - Load/Store and Branch Type (LD, STR, BEQ, BNE)

| OpCode [15-12] | Source 1 [11-9] | Destination [8-6] | Immediate [5-0] |
|---|---|---|---|

  - Jump Type (JMP)

| OpCode [15-12] | Address [11-0] |
|---|---|

# REGISTERS

- Eight Registers ($A – $G and $0)
  - Each register is 16 bits wide, allowing $2^{16}$ bytes (64 KB) to be accessed in memory
  - The zero register has a constant value of "0x0000", it cannot be overwritten

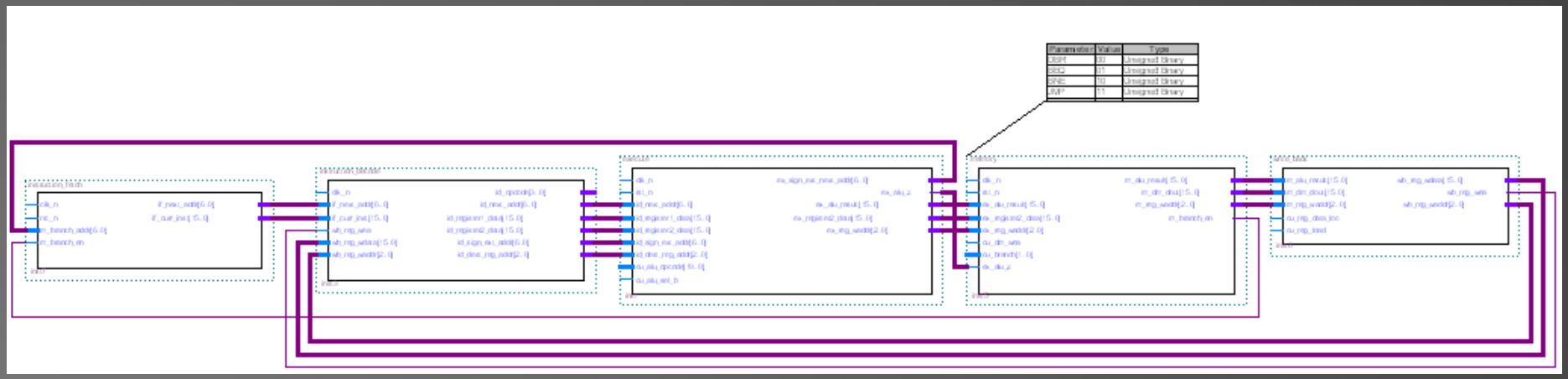
| Register Name | Register Number |
|---|---|
| **$0** | 000 |
| **$A** | 001 |
| **$B** | 010 |
| **$C** | 011 |
| **$D** | 100 |
| **$E** | 101 |
| **$F** | 110 |
| **$G** | 111 |

# CONTROL UNIT

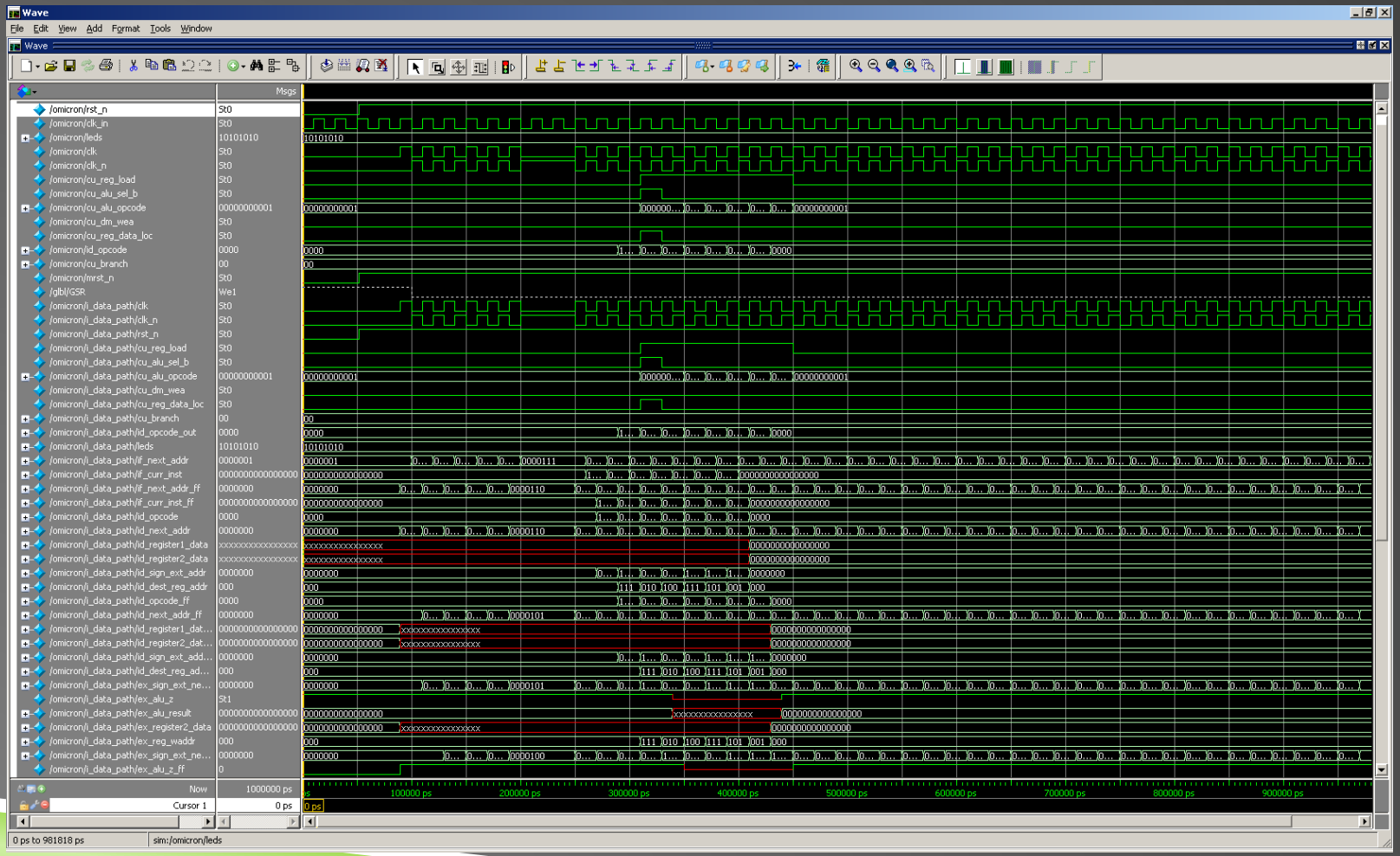
- The Control Unit is in charge of sending the correct control signals across the data path

| Instruction | Type | opcode [15:12] | cu_alu_opcode [10:0] | cu_reg_load | cu_reg_data_loc | cu_branch [1:0] | cu_dm_wea | cu_alu_sel_b | cu_reg_dest |
|---|---|---|---|---|---|---|---|---|---|
| **NOOP** | Math | 0000 | 00000000001 | 0 | 0 | 00 | 0 | 0 | 1 |
| **CPY** | Math | 0001 | 00000000010 | 1 | 0 | 00 | 0 | 0 | 1 |
| **ADD** | Math | 0010 | 00000000100 | 1 | 0 | 00 | 0 | 0 | 1 |
| **SUB** | Math | 0011 | 00000001000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **MUL** | Math | 1000 | 00000010000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **AND** | Math | 0100 | 00000100000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **OR** | Math | 0101 | 00001000000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **NOT** | Math | 0110 | 00010000000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **XOR** | Math | 0111 | 00100000000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **LS** | Math | 1001 | 01000000000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **RS** | Math | 1010 | 10000000000 | 1 | 0 | 00 | 0 | 0 | 1 |
| **BEQ** | Ld/St/Br | 1011 | 00000001000 | 0 | 0 | 01 | 0 | 0 | 1 |
| **BNE** | Ld/St/Br | 1100 | 00000001000 | 0 | 0 | 10 | 0 | 0 | 1 |
| **LD** | Ld/St/Br | 1101 | 00000000010 | 1 | 1 | 00 | 0 | 1 | 1 |
| **STR** | Ld/St/Br | 1110 | 00000000010 | 0 | 0 | 00 | 1 | 1 | 1 |
| **JMP** | Jump | 1111 | XXXXXXXXXXX | 0 | 0 | 11 | 0 | 0 | 1 |

# DATA PATH


Parameter
Value
Type
Unsigned Binary
Unsigned Binary
Unsigned Binary
Unsigned Binary

# SIMULATION


Wave
File Edit View Add Format Tools Window
Wave
Msgs
/omicron/rst_n
/omicron/clk_in
/omicron/leds
/omicron/clk
/omicron/clk_n
/omicron/cu_reg_load
/omicron/cu_alu_sel_b
/omicron/cu_alu_opcode
/omicron/cu_dm_wea
/omicron/cu_reg_data_loc
/omicron/id_opcode
/omicron/cu_branch
/omicron/mrst_n
/glbl/GSR
/omicron/i_data_path/clk
/omicron/i_data_path/clk_n
/omicron/i_data_path/rst_n
/omicron/i_data_path/cu_reg_load
/omicron/i_data_path/cu_alu_sel_b
/omicron/i_data_path/cu_alu_opcode
/omicron/i_data_path/cu_dm_wea
/omicron/i_data_path/cu_reg_data_loc
/omicron/i_data_path/cu_branch
/omicron/i_data_path/id_opcode_out
/omicron/i_data_path/leds
/omicron/i_data_path/if_next_addr
/omicron/i_data_path/if_curr_inst
/omicron/i_data_path/if_next_addr_ff
/omicron/i_data_path/if_curr_inst_ff
/omicron/i_data_path/id_opcode
/omicron/i_data_path/id_next_addr
/omicron/i_data_path/id_register1_data
/omicron/i_data_path/id_register2_data
/omicron/i_data_path/id_sign_ext_addr
/omicron/i_data_path/id_dest_reg_addr
/omicron/i_data_path/id_opcode_ff
/omicron/i_data_path/id_next_addr_ff
/omicron/i_data_path/id_register1_dat...
/omicron/i_data_path/id_register2_dat...
/omicron/i_data_path/id_sign_ext_add...
/omicron/i_data_path/id_dest_reg_ad...
/omicron/i_data_path/ex_sign_ext_ne...
/omicron/i_data_path/ex_alu_z
/omicron/i_data_path/ex_alu_result
/omicron/i_data_path/ex_register2_data
/omicron/i_data_path/ex_reg_waddr
/omicron/i_data_path/ex_sign_ext_ne...
/omicron/i_data_path/ex_alu_z_ff
Now
1000000 ps
Cursor 1
0 ps
100000 ps
200000 ps
300000 ps
400000 ps
500000 ps
600000 ps
700000 ps
800000 ps
900000 ps
0 ps to 981818 ps
sim:/omicron/leds

# SYNTHESIZING

```
### omicron.ucf ###

# ==== Clock Source ====

NET "clk_in" LOC = "C9" | IOSTANDARD = LVCMOS33;

NET "clk_in" PERIOD = 5ns HIGH 40%;

NET "clk_in" CLOCK_DEDICATED_ROUTE = FALSE;

# ==== Discrete LEDs (LED) ====

NET "leds<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<6>" LOC = "E9"  | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

NET "leds<7>" LOC = "F9"  | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

# ==== Slide Switches (SW) ====

NET "rst_n" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ; # SW
```