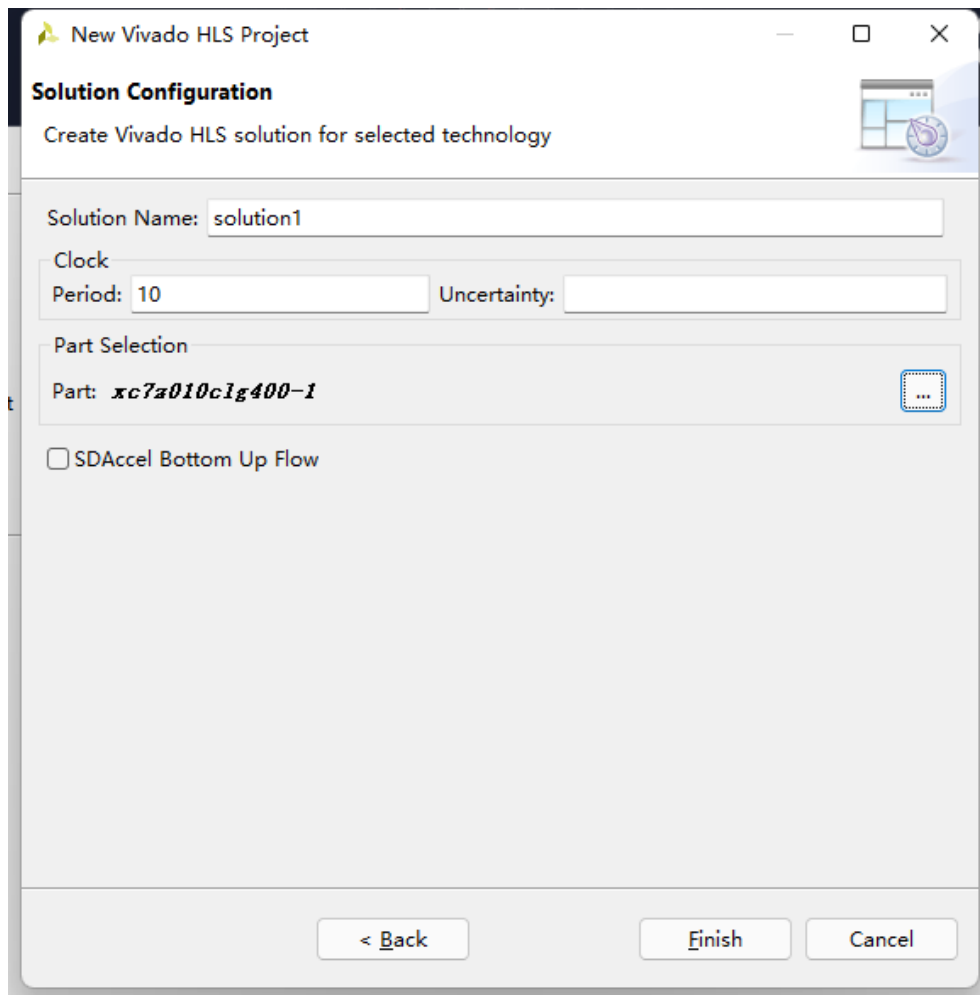


# [L12]HLS基础学习

学习本节推荐配合UG871和UG902,HLS目前依然很多BUG,不过比Vitis还是好很多,所以做一个了解其实就还好了,一开始Xilinx总是说HLS替代传统Verilog,Vits替代HLS各种,这就如ARM能替代51一样,短时间应该还是比较难.



新建工程并记得选择正确的器件.



我写了一个led.cpp文件,作为入口,代码如下.

**注:**为什么不用switch,因为我们还是为了综合结果考虑.

```
#include <stdio.h>
#include <ap_int.h>

void led(ap_int<4> &led){
    #pragma HLS interface ap_none port=led
    #pragma HLS interface ap_ctrl_none port=return

    static int ledc = 0x01;
    static long cnt = 0;

    if(cnt < 500000000){
        cnt++;
    }
    else{
        cnt = 0;

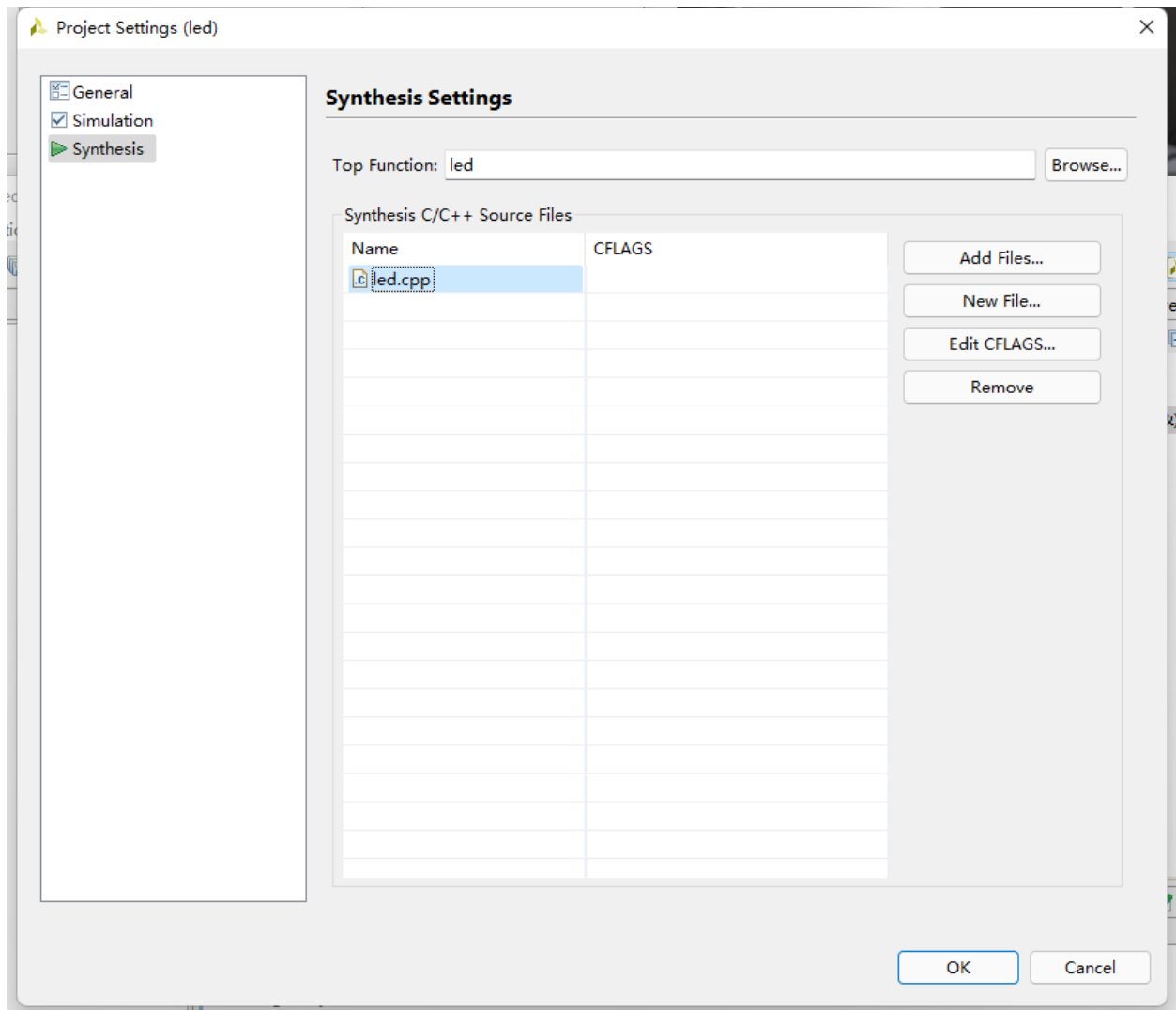
        if(ledc == 0x01){
            led = 0x02;
            ledc = 0x02;
        }else if(ledc == 0x02){
```

```

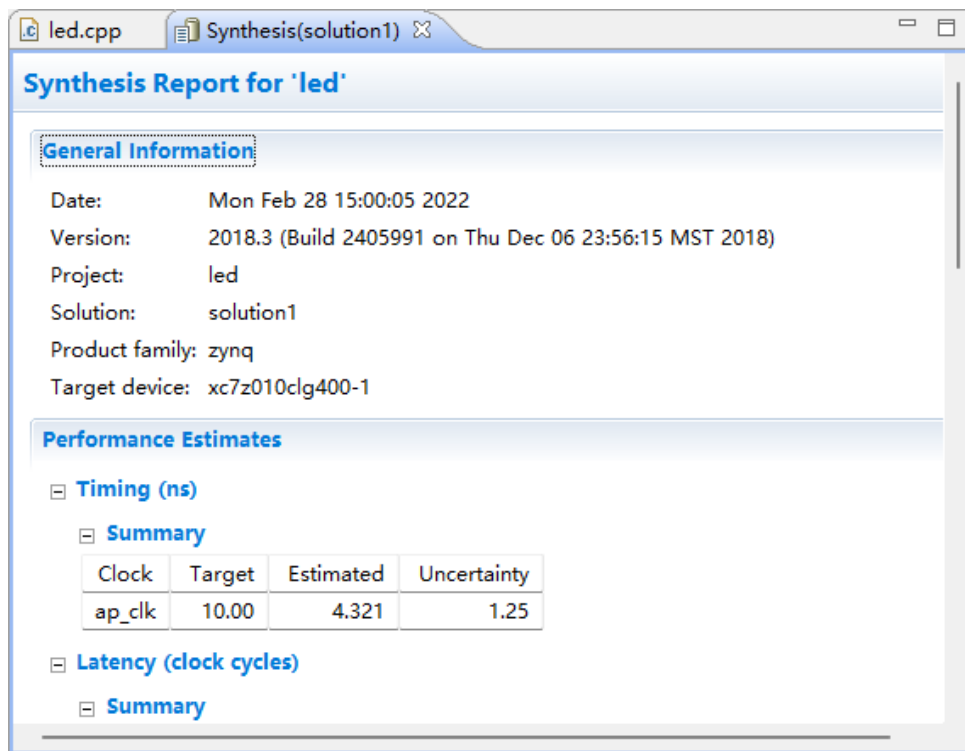
    led = 0x04;
    ledc = 0x04;
} else if (ledc == 0x04){
    led = 0x08;
    ledc = 0x08;
} else if (ledc == 0x08){
    led = 0x01;
    ledc = 0x01;
}
}
}

```

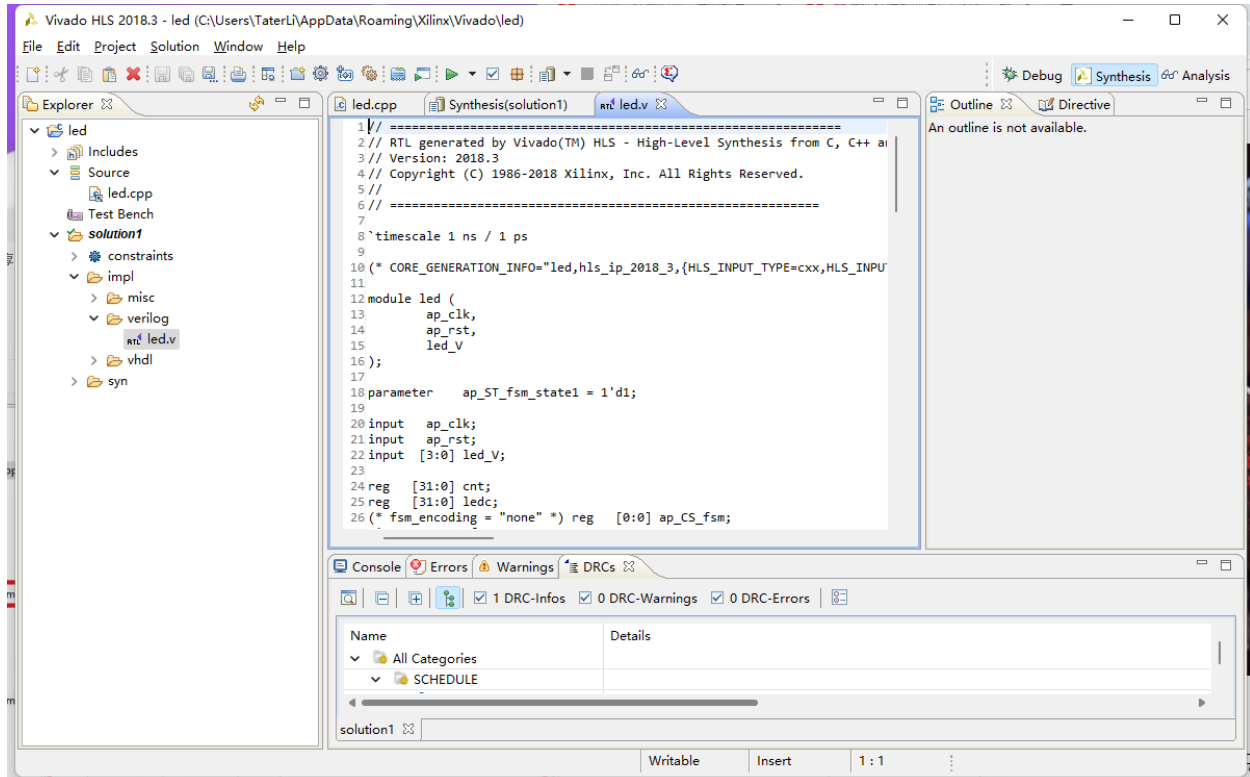
否则会有这个错误.



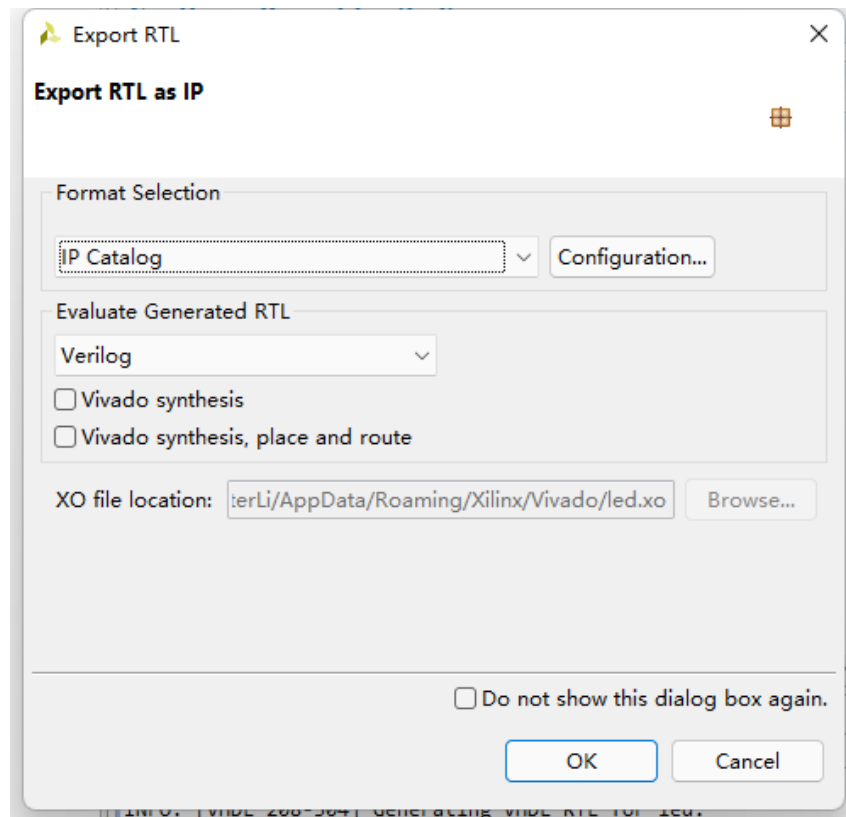
然后编译(综合)看看.



也可以看到综合结果代码。



点击Export RTL as IP按钮(橙色捆包图标),打开导出.



不过喜闻乐见失败,这里需要修改电脑时间,请查看官方论坛的吐槽:

[https://support.xilinx.com/s/question/0D52E00006uyTmwSAE/error-impl-21328-failed-to-generate-ip?language=en\\_US](https://support.xilinx.com/s/question/0D52E00006uyTmwSAE/error-impl-21328-failed-to-generate-ip?language=en_US)

Solutions

Products

Company

201170njuus567 (Customer) asked a question.  
2022年1月2日 at PM12:43

**ERROR: [IMPL 213-28] Failed to generate IP.**

```

ERROR: [IMPL 213-28] Failed to generate IP.
command 'ap_source' returned error code
while executing
"source D:/vivado_code/official_15eg_code/course_06/hls/edge_canny_detector/edge_canny_detector/solution1/export.tcl"
invoked from within
"hls::main D:/vivado_code/official_15eg_code/course_06/hls/edge_canny_detector/edge_canny_detector/solution1/export.tcl"
("uplevel" body line 1)
invoked from within
"uplevel 1 hls::main {"$args"}
(procedure "hls_proc" line 9)
invoked from within
"hls_proc $args"

```

Originally, 2020 Vitis HLS could generate IP cores normally. But I unloaded it and had this problem with the reload. There is absolutely nothing wrong with the code.

HLS

Like

Answer

Share

5 answers · 539 views

halilny (Customer)

Edited January 5, 2022 at 6:39 AM

I have the same problem. run\_ippack.tcl stops at line 1110 and can not continue.  
Could you find a solution?

bad lexical cast: source type value could not be interpreted as target  
while executing  
"rdi::set\_property core\_revision 2201050920 {component component\_1}"  
invoked from within

Expand Post

Like · Reply

201170njuus567 (Customer)

2 months ago

Setting the time of computer to 2021 years. this is a temporary method.

Like · Reply

p.ching.kuang@gmail.com (Customer)

2 months ago

I also have the same problem. (I had tried 2017.4/2018.3's HLS tool)

Like · Reply

201170njuus567 (Customer)

2 months ago

Setting the time of computer to 2021 years. this is a temporary method.

Like · Reply

Bug report: Vivado 2021.2 revision nu  
mber overflow after new year

3.82K

2022 timestamp overflow: ERROR: '220  
1011128' is an invalid argument. Pleas  
e specify an integer value

5.5K

Vivado fails to export IPs with the error  
message "Bad lexical cast: source type  
value could not be interpreted as targ  
e"

6.25K

Export IP Invalid Argument / Revision  
Number Overflow Issue

11.05K

why vitis hls is not able to export ip

1.56K

TRENDING ARTICLES

[Export IP Invalid Argument / Revision Number Overflow Issue \(Y2K22\)](#)

[AXI Basics 1 - Introduction to AXI](#)

[Debugging PCIe Issues using Ispci and setpci](#)

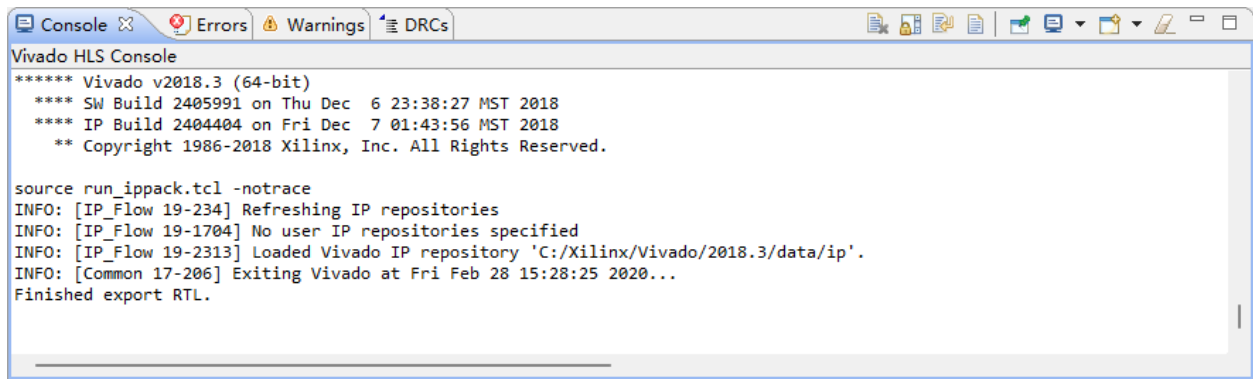
[Quickly install Cable Drivers for Xilinx Platform Cable USB II on Windows 10](#)

[65444 - Xilinx PCI Express DMA Drivers and Software Guide](#)

终于可以导出了,就这个BUG,我就可以认为毫无生产力?每次调试还得换时间,很多软件又依赖时间.

[L12]HLS基础学习

6



可以从代码中看到,语法稍微有点不同,

```
#pragma HLS interface ap_none port=led  
#pragma HLS interface ap_ctrl_none port=return
```

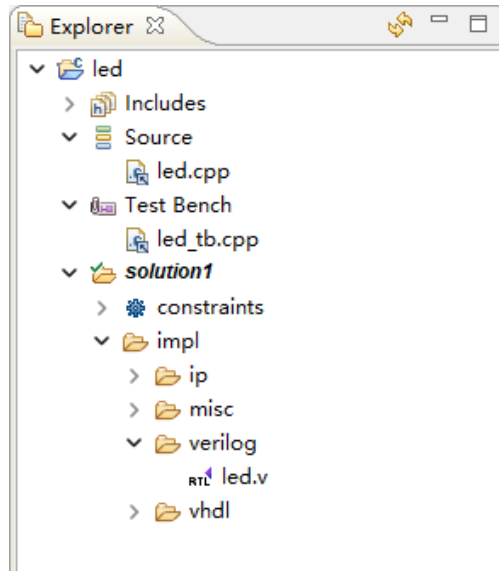
这些是综合行为指示,比如第一句,告诉综合器LED是输出信号.第二句告诉综合器这没有端口控制信号,比如下面这句是说返回值无,输出ap\_int类型,这个是什么类型呢?就是HLS类型,指定4位宽的LED,就是4只LED嘛.

```
void led(ap_int<4> &led)
```

那能不能仿真呢?当然可以,不过也要自己编写仿真激励,风格就非常C语言了,文件名要以一定格式,比如led.cpp对应led\_tb.cpp才能正确识别,当然位置也要放对.

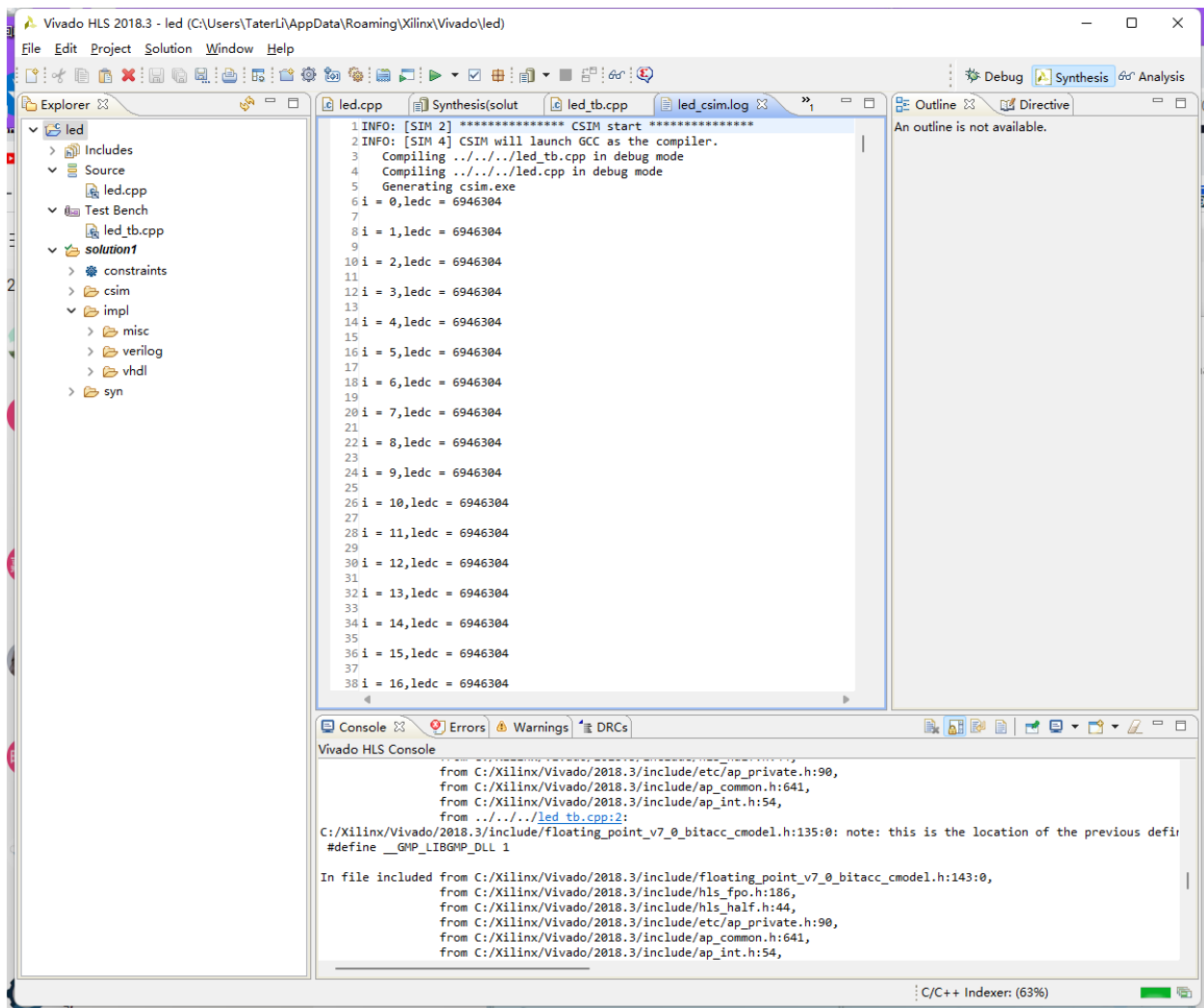
```
#include "stdio.h"  
#include "ap_int.h"  
  
extern void led(ap_int<4> &led);  
  
int main(void)  
{  
    ap_int<4> ledc=7;  
    for(int i=0;i<1000;i++)  
    {  
        led(ledc);  
        printf("i = %d,ledc = %d \r\n",i,ledc & 0xf);  
    }  
    return 0;  
}
```

工程整体.

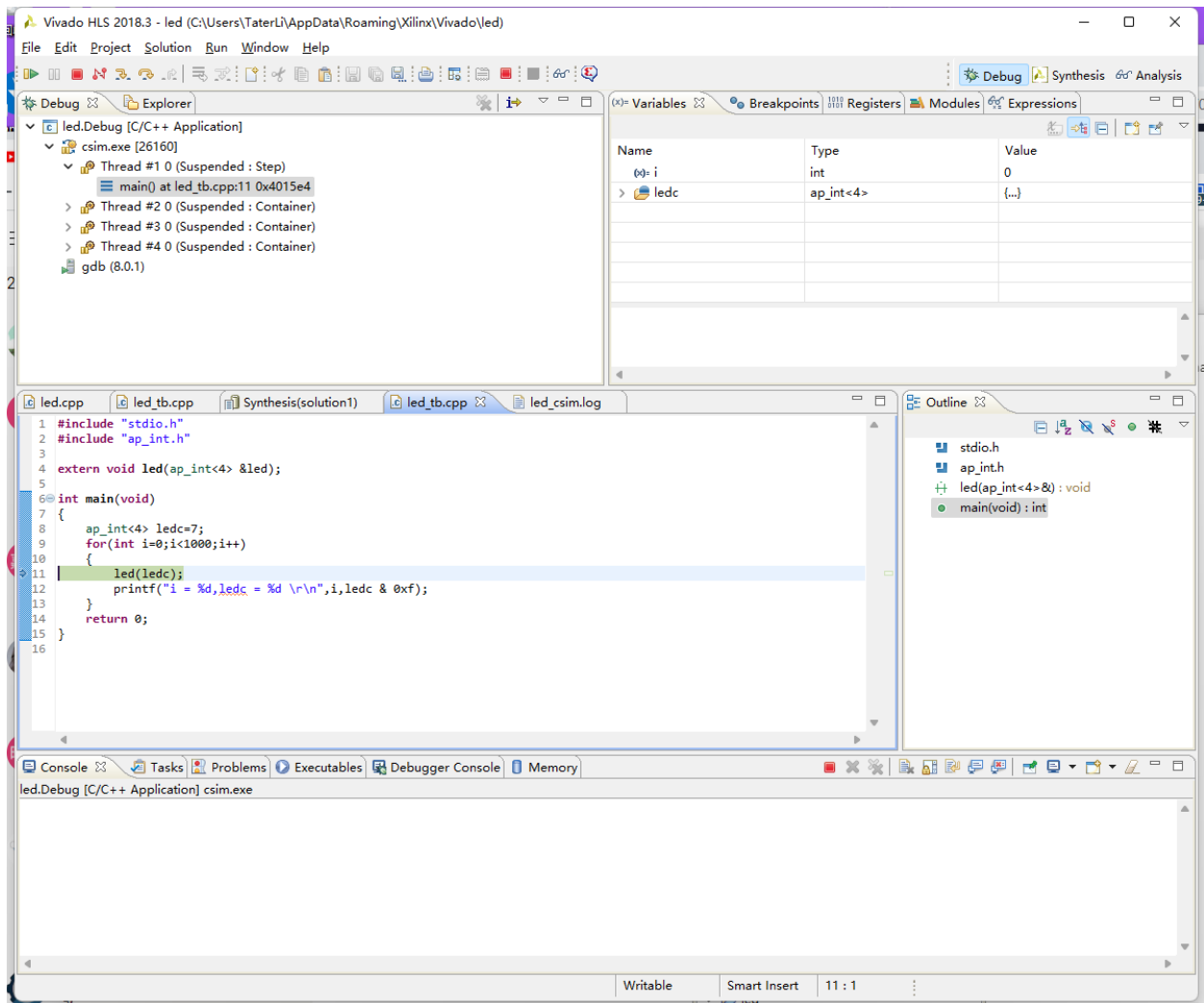


直接执行仿真会输出所有结果.

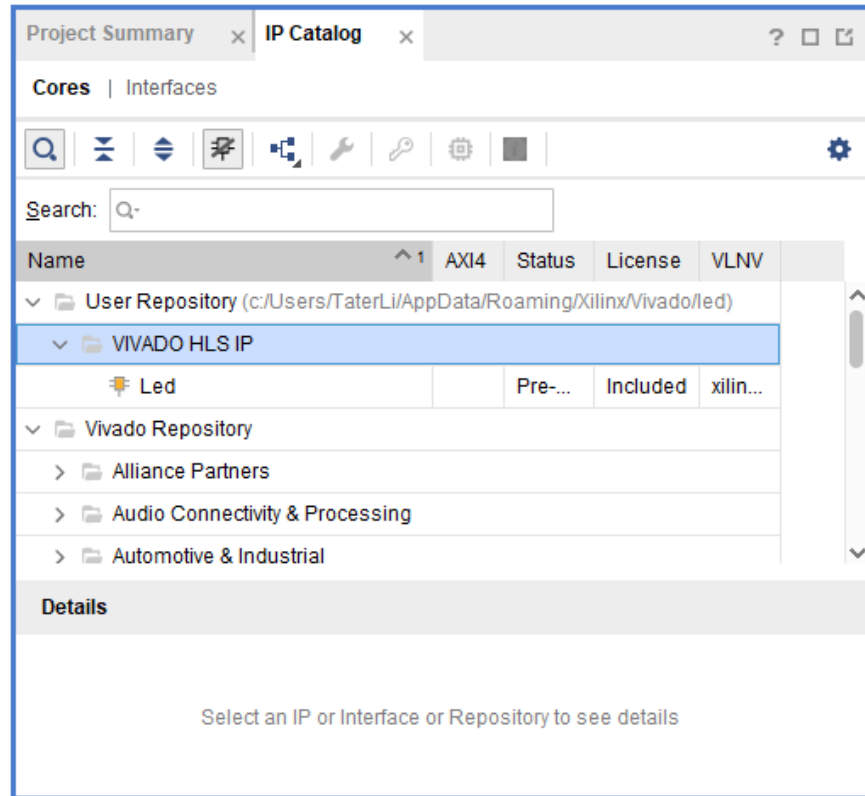




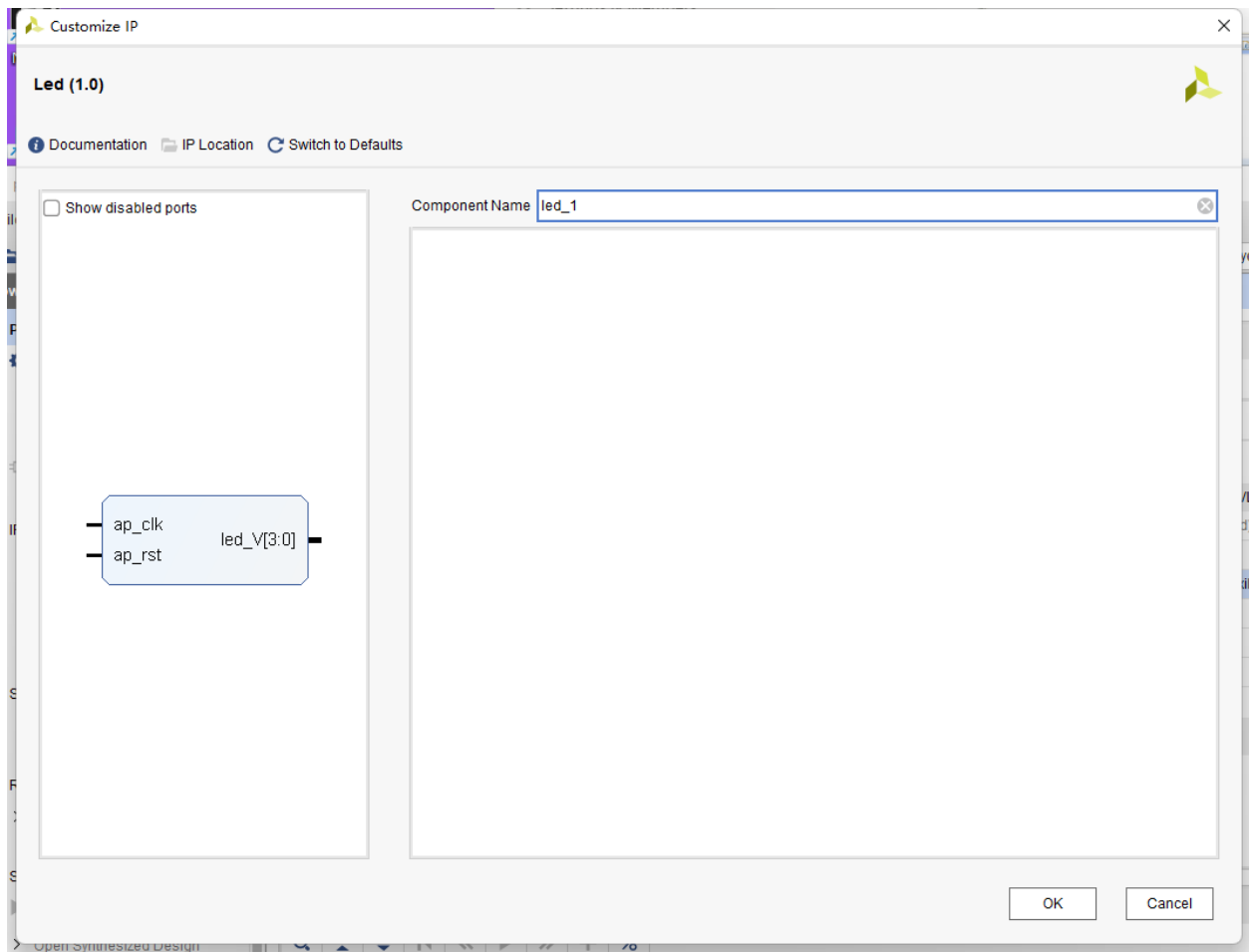
也可以尝试进入单步调试器。



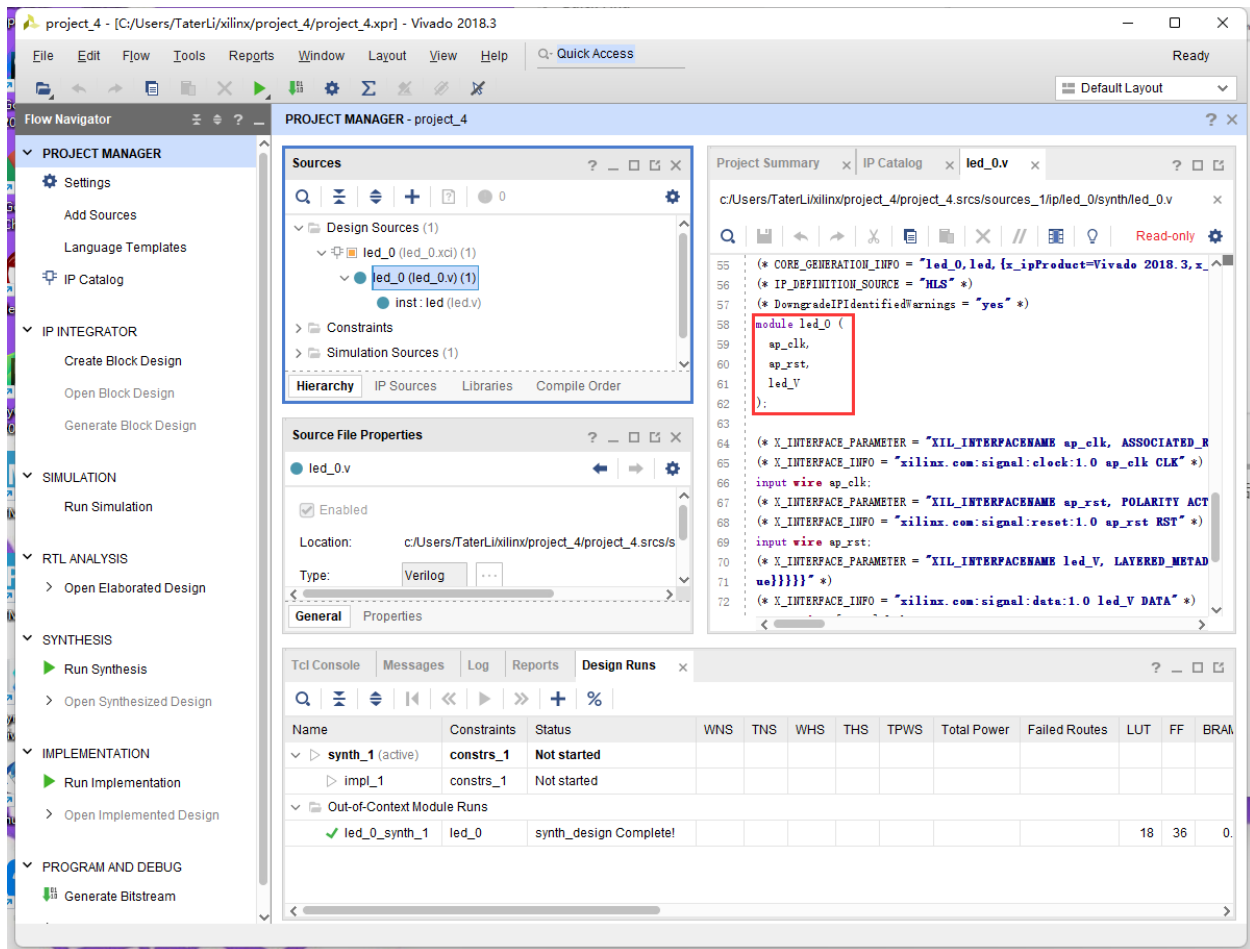
可是怎样才能到FPGA里,那就要用到刚才导出的IP,IP是位于HLS工程根目录的,因此导入即可.



现在看到IP了.



双击IP随意配置了一下,然后生成文件,然后只需要Generate Output Product,然后展开并准备实例化信号.



不过,HLS综合后的复位信号是高有效,和正常思路不同,特别要注意,可是坑了我很久,当然HLS可以以C风格写很复杂的程序,还可以自动调用一些所需IP,甚至是OpenCV之类高级库都能轻松引入,下面贴一个求均值代码,因为他用了数组,寄存器必然不够用,所以他还会自动调用一个PL核的RAM IP,并且有输入输出。

```
#include "stdio.h"
#include "ap_int.h"

#define MAX_FIR_TIME 200 //允许设置的最大平滑均值滤波次数 20

void filter_ip(unsigned int input, unsigned char fir_time, unsigned int *output, unsigned char *result_valid)
{
    #pragma HLS INTERFACE ap_ctrl_none port = return
    #pragma HLS INTERFACE ap_none port = output
    #pragma HLS INTERFACE ap_none port = result_valid

    static int filter_ptr = 0;
    static unsigned int buffer_in[256] = {0}; //缓存,存储输入进来的数据
    static unsigned char result_valid_flag = 0;
    unsigned long long tmp_add_value = 0;
    int i = 0;
    int filter_time = 0;

    filter_time = fir_time;
```

```

if (filter_time == 0)
{
    *output = 0;
    return;
}
else
{
    if (filter_time > MAX_FIR_TIME)
        filter_time = MAX_FIR_TIME;
    buffer_in[filter_ptr] = input;
    for (i = 0; i < filter_time; i++)
        tmp_add_value += buffer_in[i]; // 累加最近滤波次数的所有数据
    filter_ptr++;
    if (filter_ptr > (filter_time - 1))
    {
        filter_ptr = 0;
        result_valid_flag = 1; // 滤波数据开始有效
    }
    *result_valid = result_valid_flag;
    *output = tmp_add_value / filter_time; // 求均值
    return;
}
}

```