[L04]调试技巧

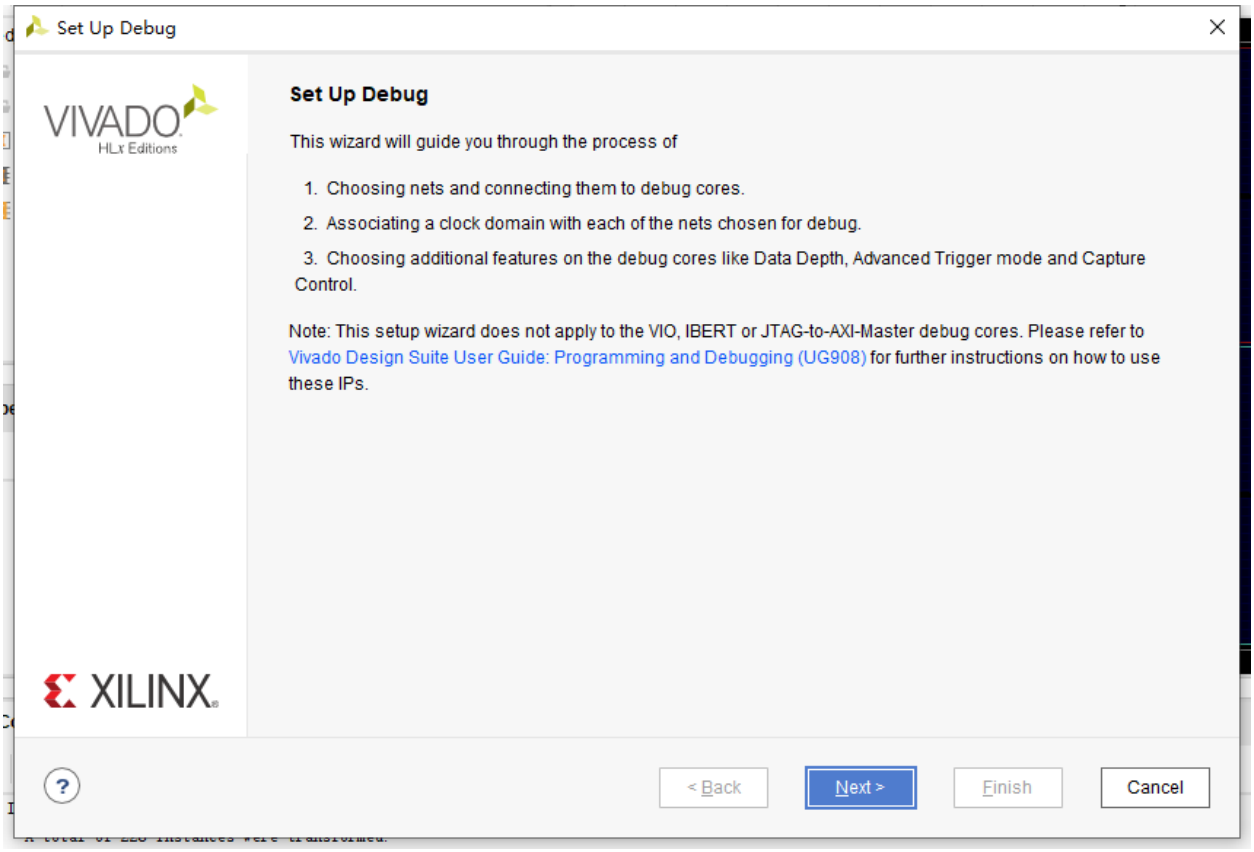
调试中可以使用标记语句,比如我把代码变成这样.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2022/02/19 23:07:24
// Design Name:
// Module Name: led_stream
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module led_stream((*mark_debug="true"*)output reg [3:0] led, // 显示4个LED
                  input clk,            // 时钟输入
                  input rst);           // 复位输入

    reg [31:0] cnt; // 这是一个32Bit计数器.

    wire [37:0] ila_probe0; // ILA探针
    assign ila_probe0[31:0] = cnt[31:0];
    assign ila_probe0[35:32] = led[3:0];
    assign ila_probe0[36] = clk;
    assign ila_probe0[37] = rst;

    wire clk_out1;

    ila_0 ila_0_inst
    (
        .clk(clk),
        .probe0(ila_probe0)
    );

    clk_wiz_0 clk_wiz_0_inst
    (
        .clk_out1(clk_out1),
```

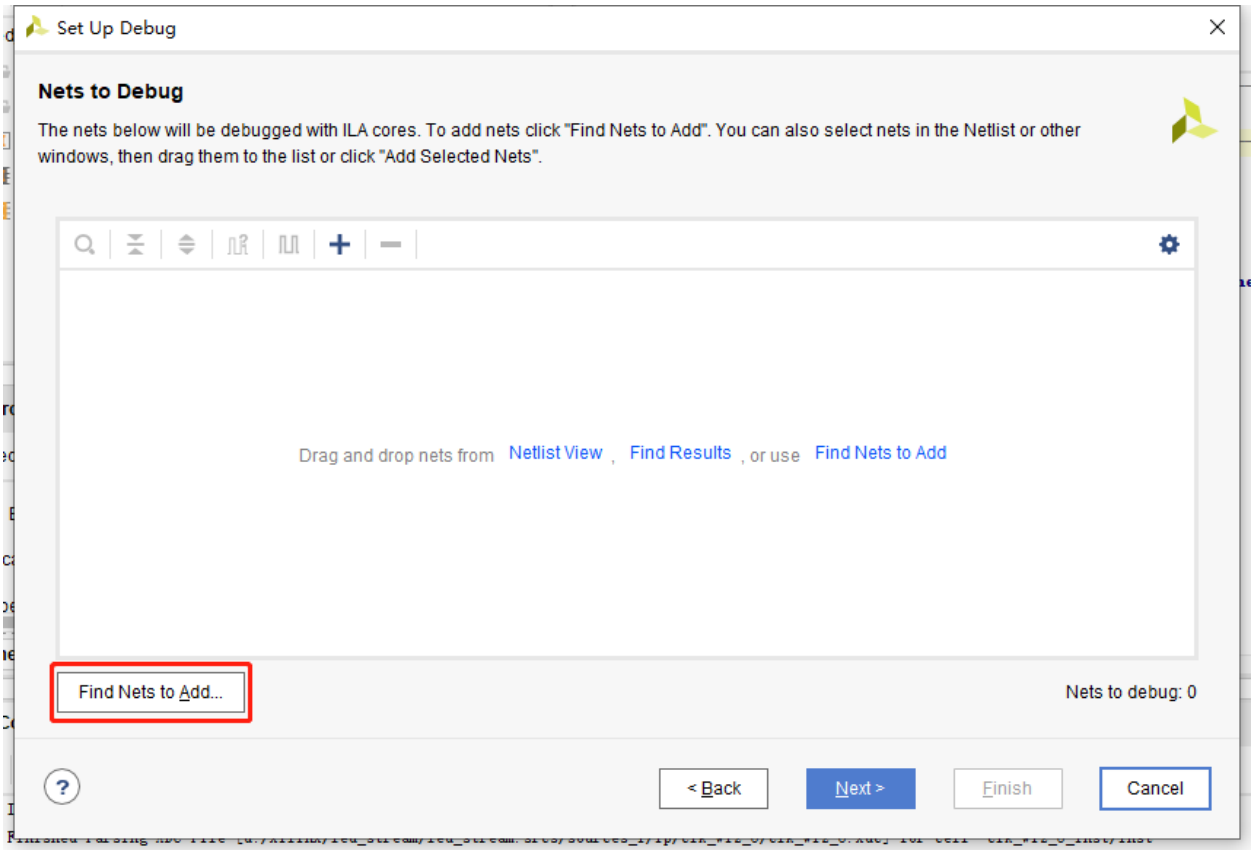
```
        .resetn(rst),
        .locked(),
        .clk_in1(clk)
    );

    always@(posedge clk_out1 or negedge rst)
    begin
        if (!rst)
        begin
            cnt <= 'b0;
            led <= 'b0001;
        end
        else
        begin
            if (cnt == 25000000)
            begin
                cnt <= 'b0;
                led <= {led[0],led[3:1]};
            end
            else
            begin
                cnt <= cnt + 'b1;
            end
        end
    end

endmodule
```

被标记之后综合信号名称不会发生变化,因为综合的时候,VIVADO有一套自己的重新命名的规则,所以一般来讲,综合之后的网表信号列表都会有所变化,但是加了这一句之后,VIVADO就不会更改名字.综合出来的信号名称也是我们编写的名称,并且,这句话还可以在综合之后,在软件进行在线调试设置的时候直接找到这些信号.

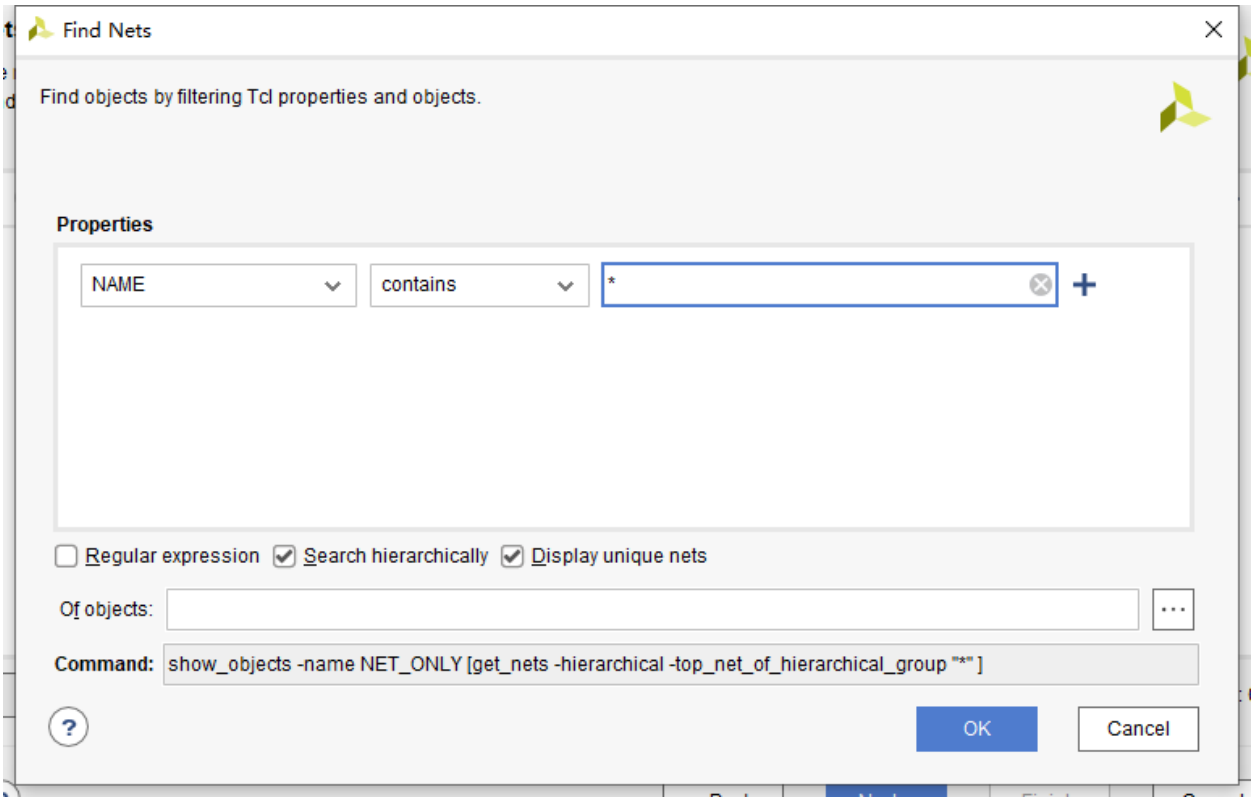
综合并写入FPGA后打开SYNTHESIS→Open Synthesized Design→Set Up Debug



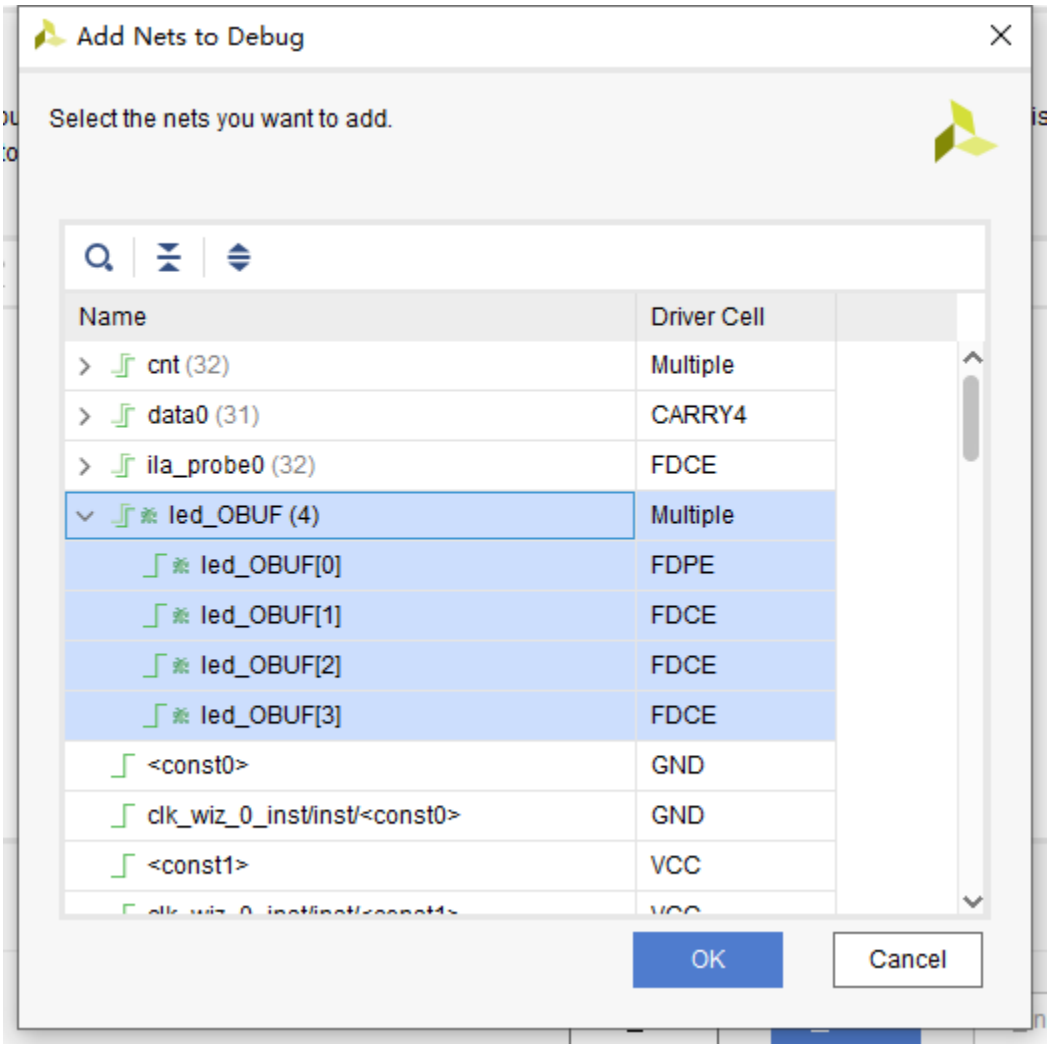
选择Find Net to Add...


Set Up Debug
Nets to Debug
The nets below will be debugged with ILA cores. To add nets click "Find Nets to Add". You can also select nets in the Netlist or other windows, then drag them to the list or click "Add Selected Nets".
Drag and drop nets from Netlist View , Find Results , or use Find Nets to Add
Find Nets to Add...
Nets to debug: 0
< Back
Next >
Finish
Cancel

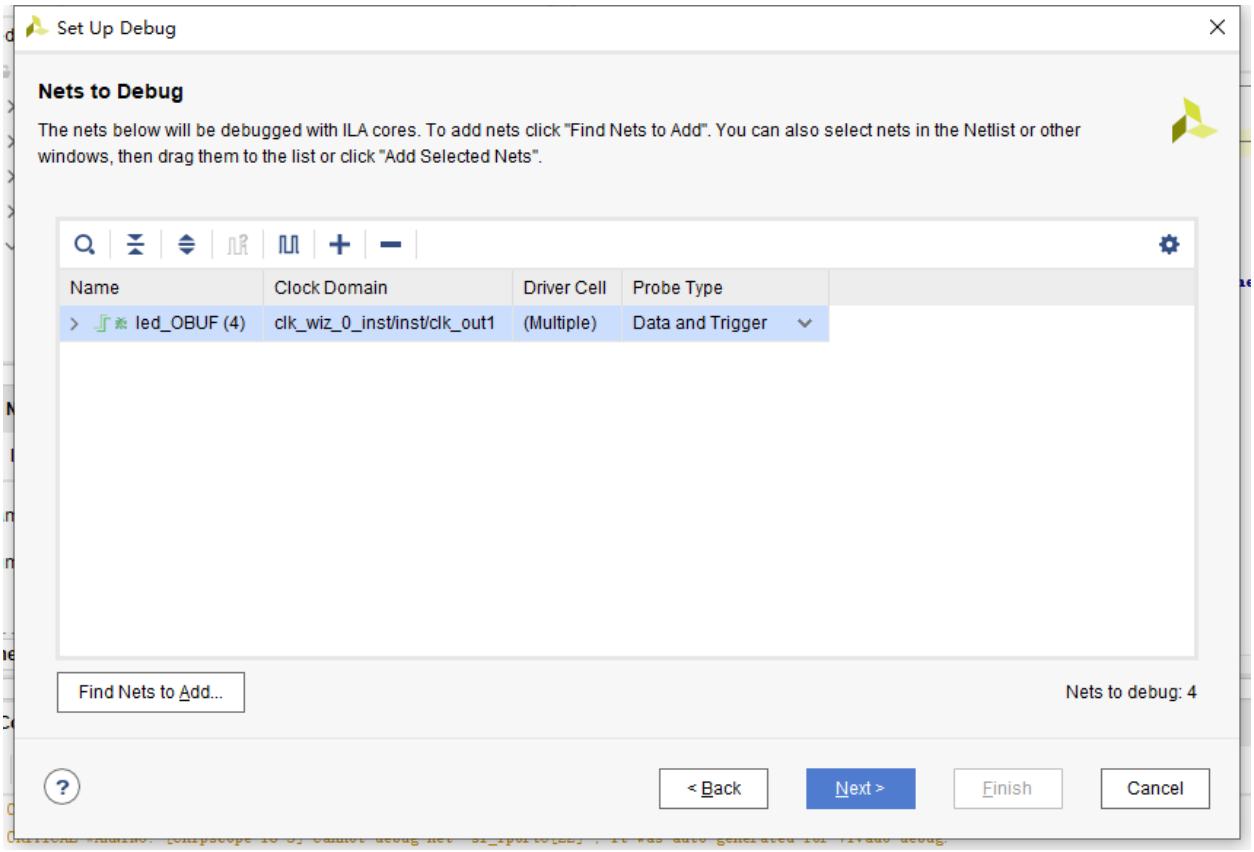
直接全部搜素.



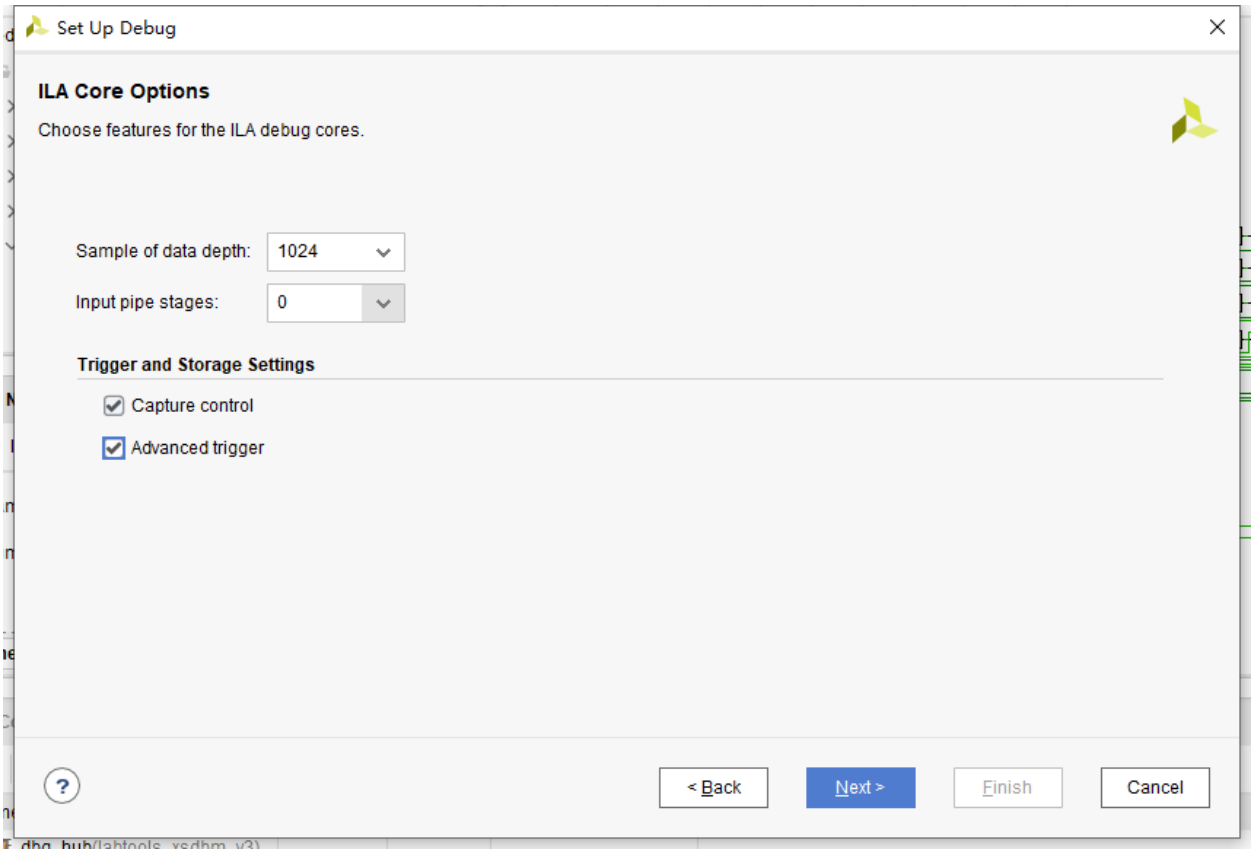
看到LED已经有虫子标记了.


Add Nets to Debug
Select the nets you want to add.
Name
Driver Cell
cnt (32)
Multiple
data0 (31)
CARRY4
ila_probe0 (32)
FDCE
led_OBUF (4)
Multiple
led_OBUF[0]
FDPE
led_OBUF[1]
FDCE
led_OBUF[2]
FDCE
led_OBUF[3]
FDCE
<const0>
GND
clk_wiz_0_inst/inst/<const0>
GND
<const1>
VCC
OK
Cancel

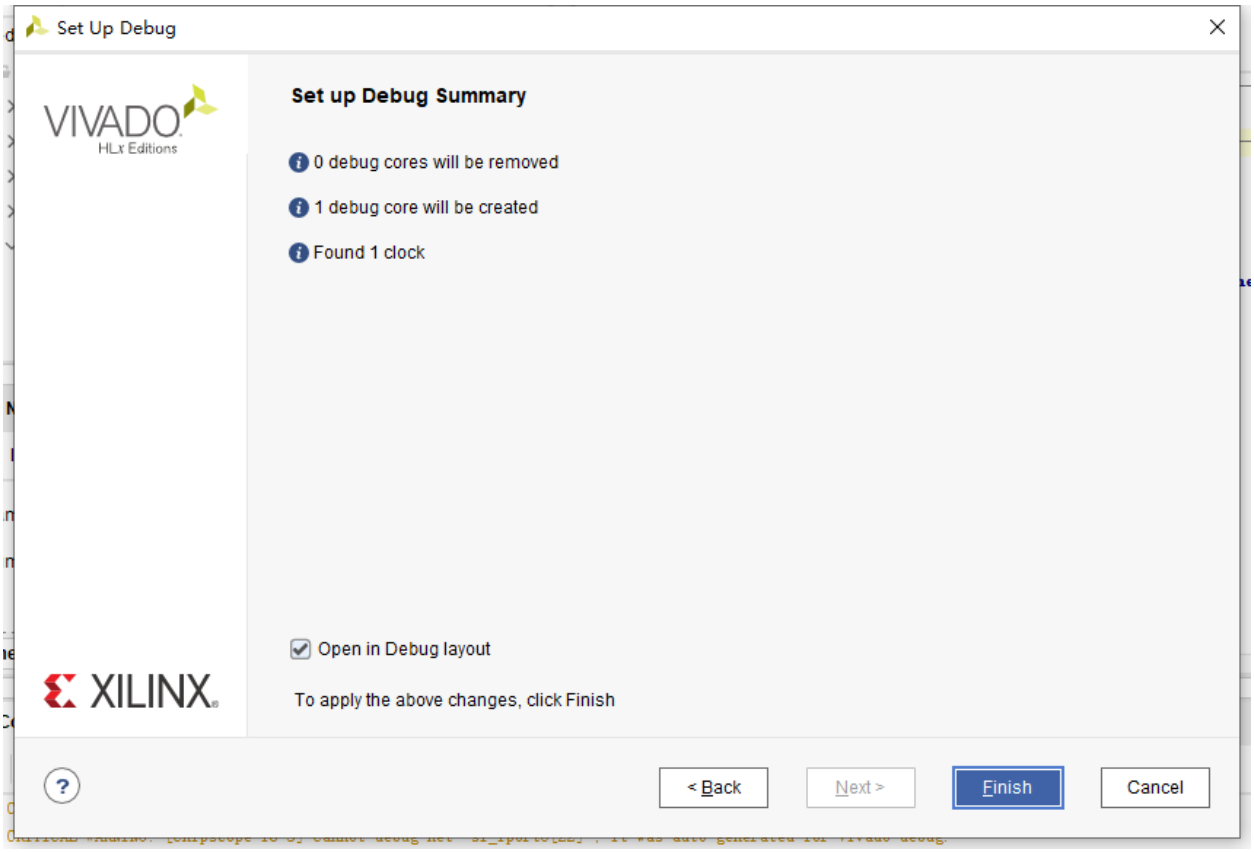
添加进去.



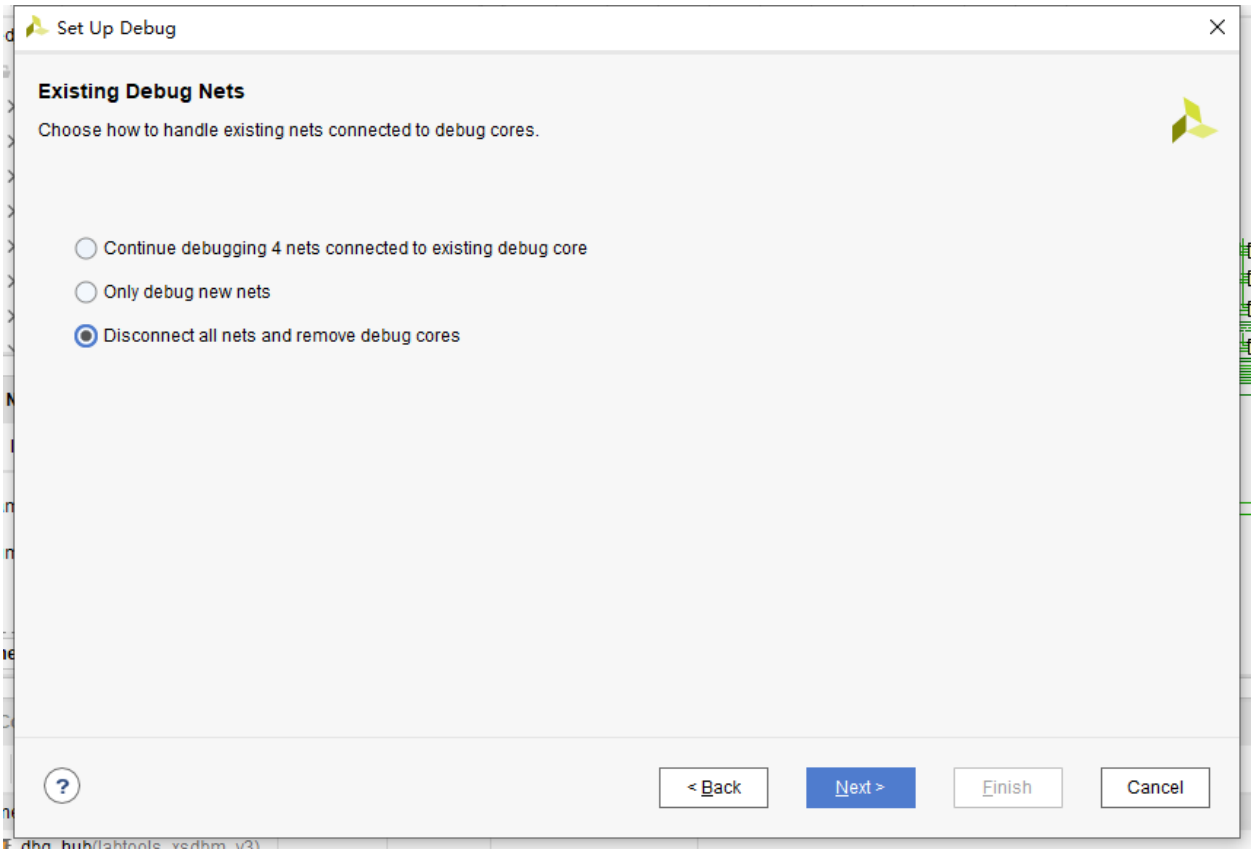
像ILA那样的设置,比如触发和捕获控制.


Set Up Debug
ILA Core Options
Choose features for the ILA debug cores.
Sample of data depth:
1024
Input pipe stages:
0
Trigger and Storage Settings
Capture control
Advanced trigger
< Back
Next >
Finish
Cancel

完成就可以了.



接下来就是ILA调试一样了,那么如果调试结束呢?那就继续Set Up Debug选择全部删除就行了.


Set Up Debug
Existing Debug Nets
Choose how to handle existing nets connected to debug cores.
Continue debugging 4 nets connected to existing debug core
Only debug new nets
Disconnect all nets and remove debug cores
< Back
Next >
Finish
Cancel