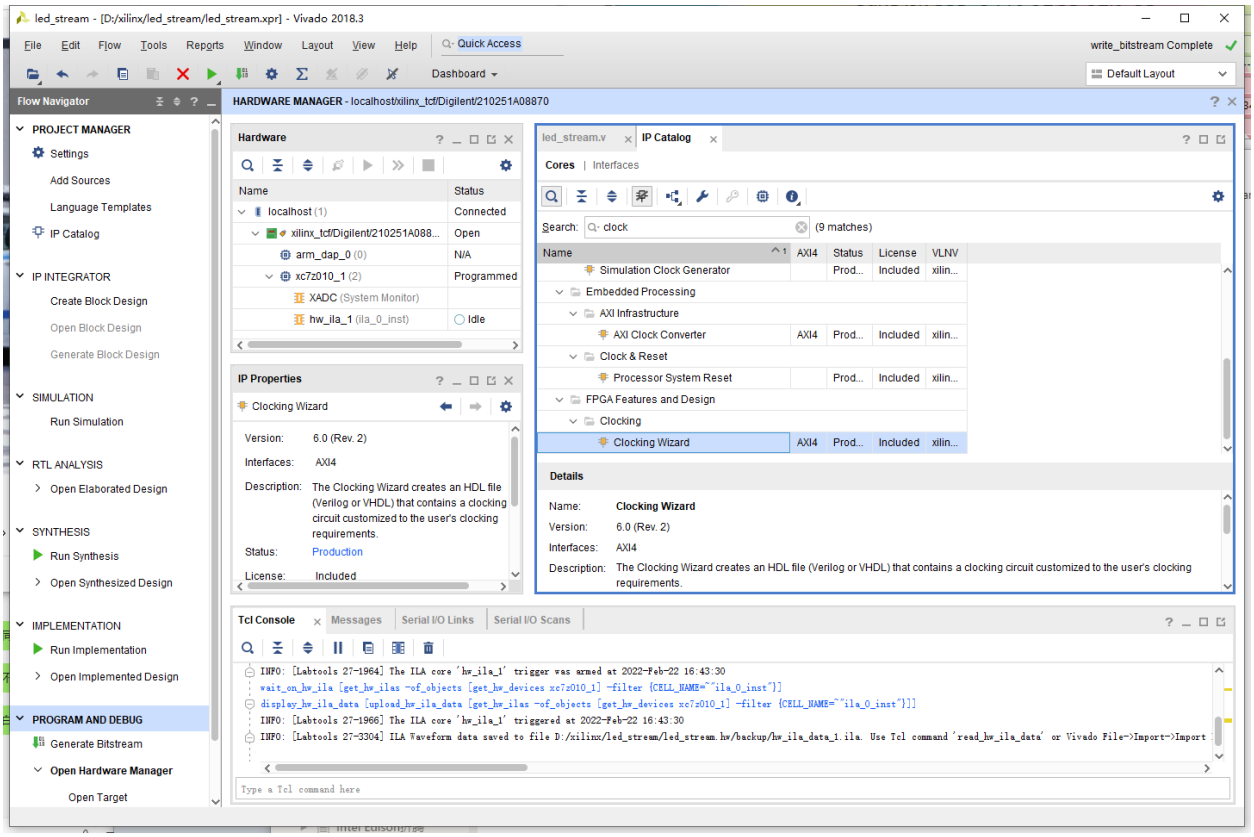
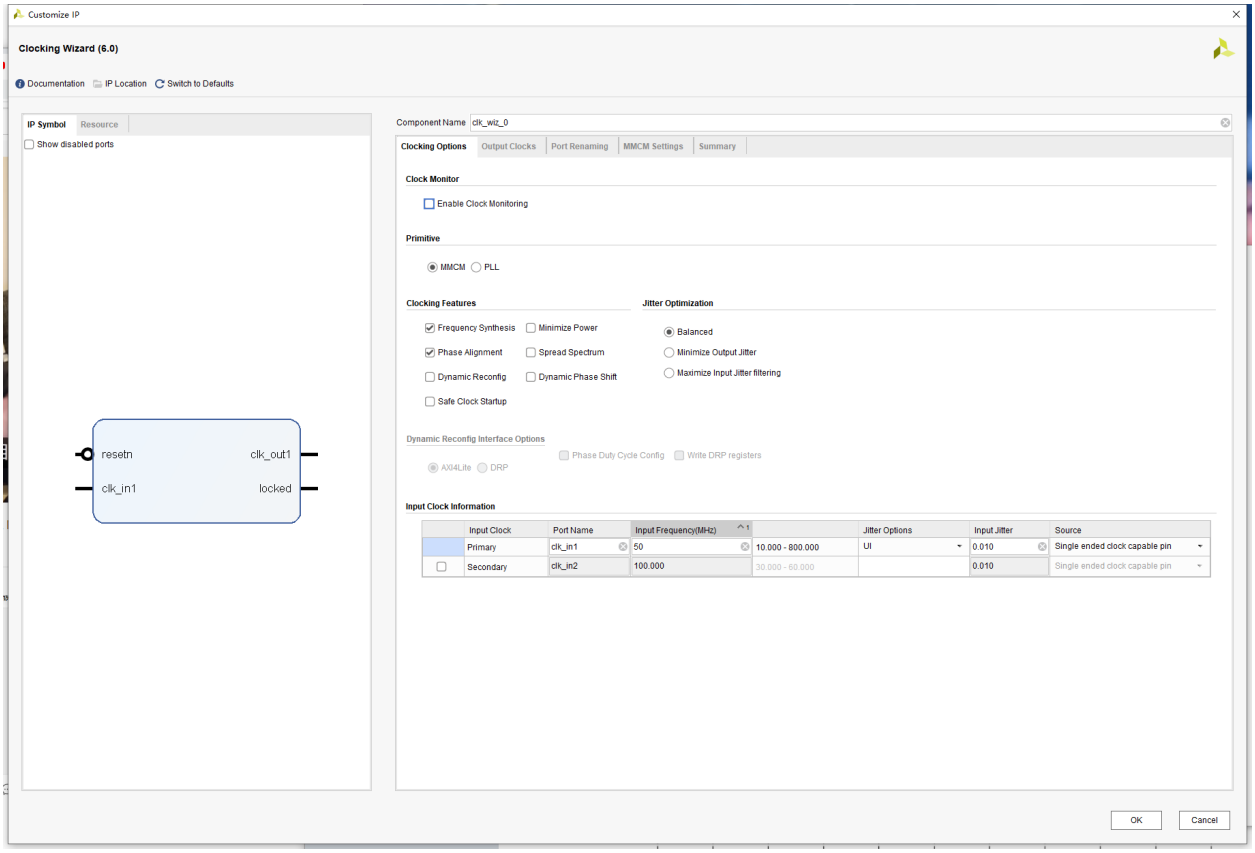
[L03]PLL IP使用

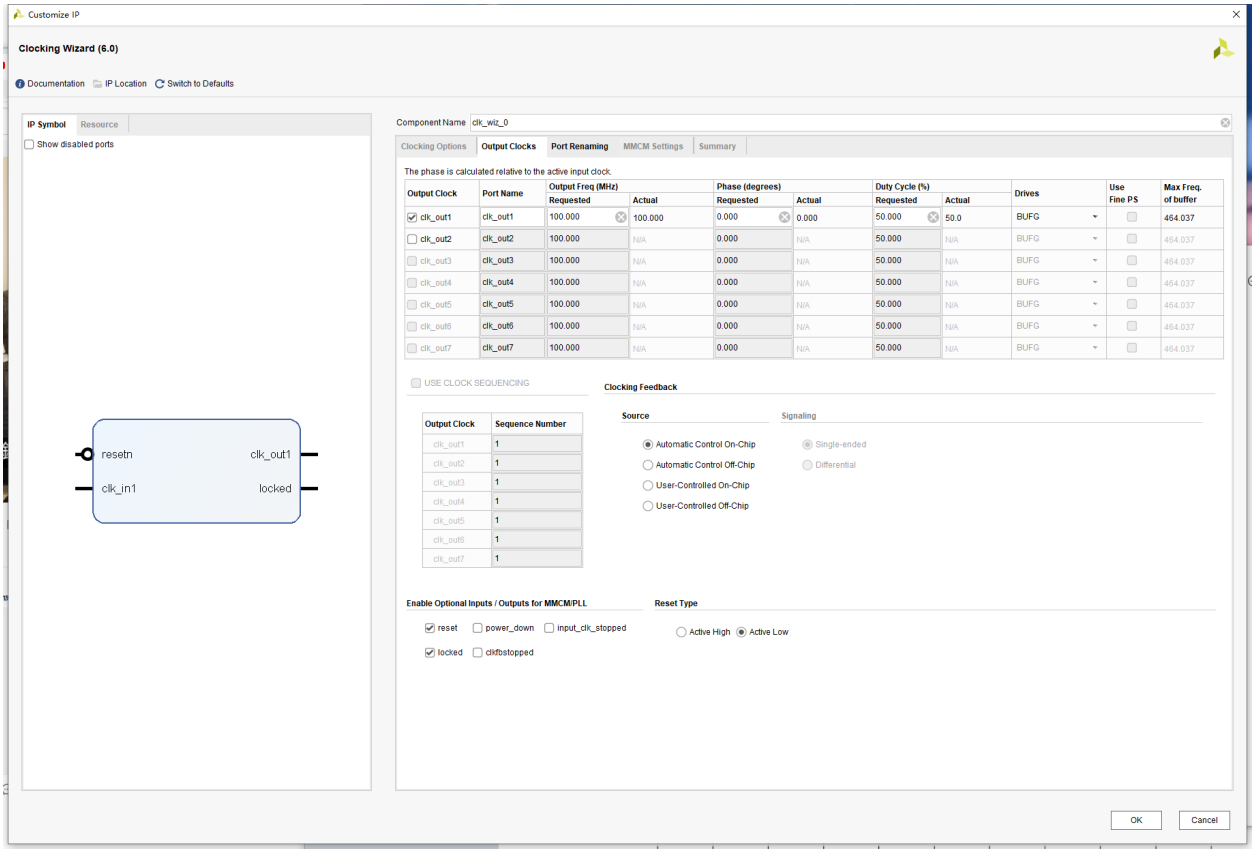
其实之前的教程里也已经说IP初始化的过程,无非是实例模块,在PLL这里也是,还是在流水灯例子里做,这里添加一个Clocking Wizard的IP.



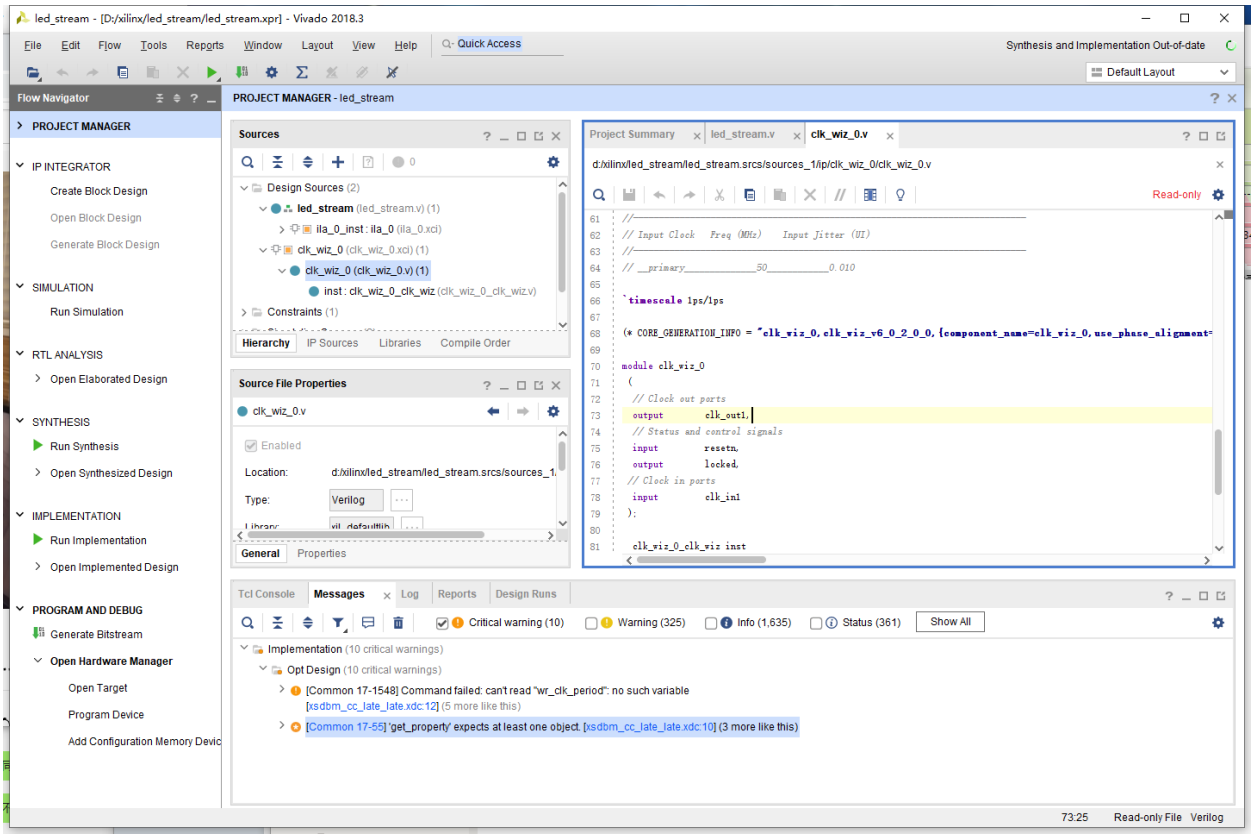
设置输入时钟,比如我们的50MHz.



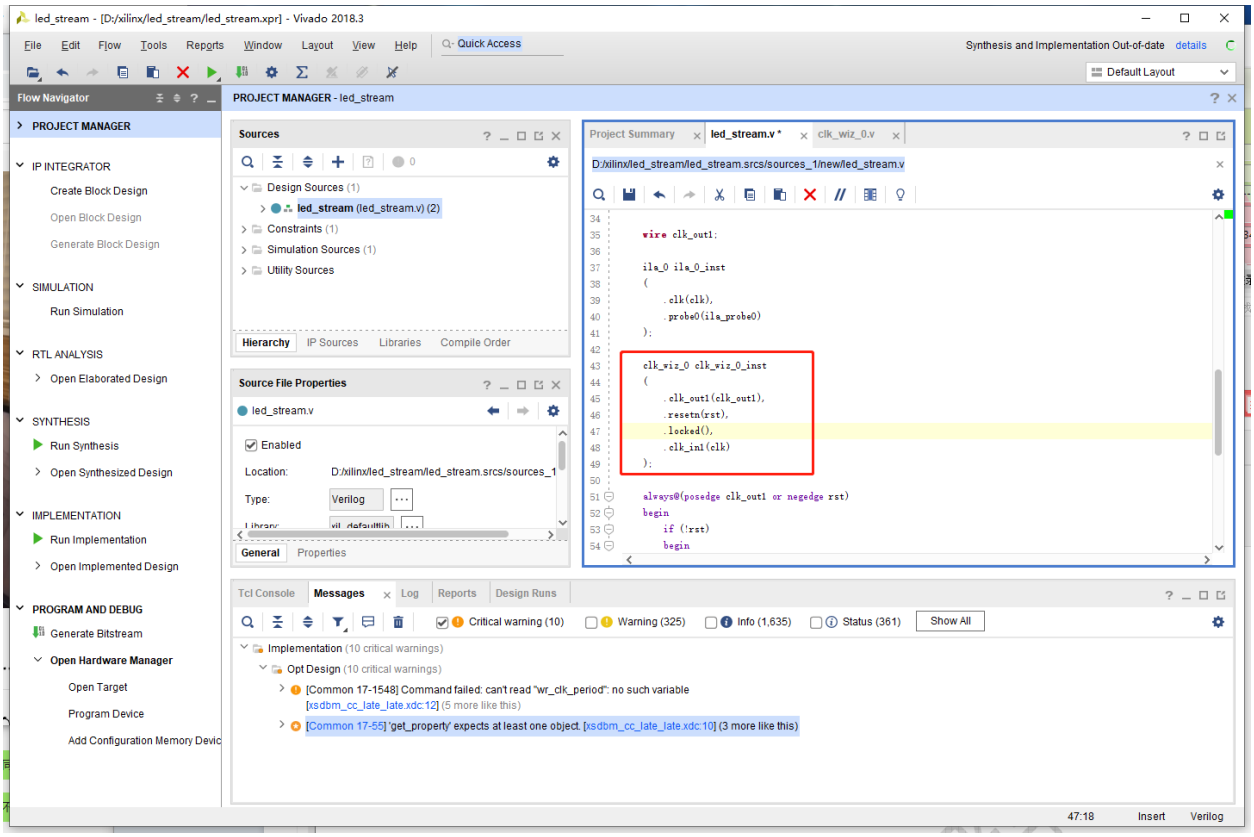
设置输出时钟,比如100MHz,设置低复位.



这里怎么知道传入什么参数才能实例化呢?展开IP看看.



实例化后并把流水灯时钟改成PLL后时钟.



代码整体这样.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2022/02/19 23:07:24
// Design Name:
// Module Name: led_stream
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module led_stream(output reg [3:0] led, // 显示4个LED
```

```
                  input clk,            // 时钟输入
                  input rst);           // 复位输入

    reg [31:0] cnt; // 这是一个32Bit计数器.

    wire [37:0] ila_probe0; // ILA探针
    assign ila_probe0[31:0] = cnt[31:0];
    assign ila_probe0[35:32] = led[3:0];
    assign ila_probe0[36] = clk;
    assign ila_probe0[37] = rst;

    wire clk_out1;

    ila_0 ila_0_inst
    (
        .clk(clk),
        .probe0(ila_probe0)
    );

    clk_wiz_0 clk_wiz_0_inst
    (
        .clk_out1(clk_out1),
        .resetn(rst),
        .locked(),
        .clk_in1(clk)
    );

    always@(posedge clk_out1 or negedge rst)
    begin
        if (!rst)
        begin
            cnt <= 'b0;
            led <= 'b0001;
        end
        else
        begin
            if (cnt == 25000000)
            begin
                cnt <= 'b0;
                led <= {led[0],led[3:1]};
            end
            else
            begin
                cnt <= cnt + 'b1;
            end
        end
    end

endmodule
```

由于FPGA厂商都会提供非常多的IP,这些IP可能需要License才能用,也可能并不需要,具体看IP自己的介绍.