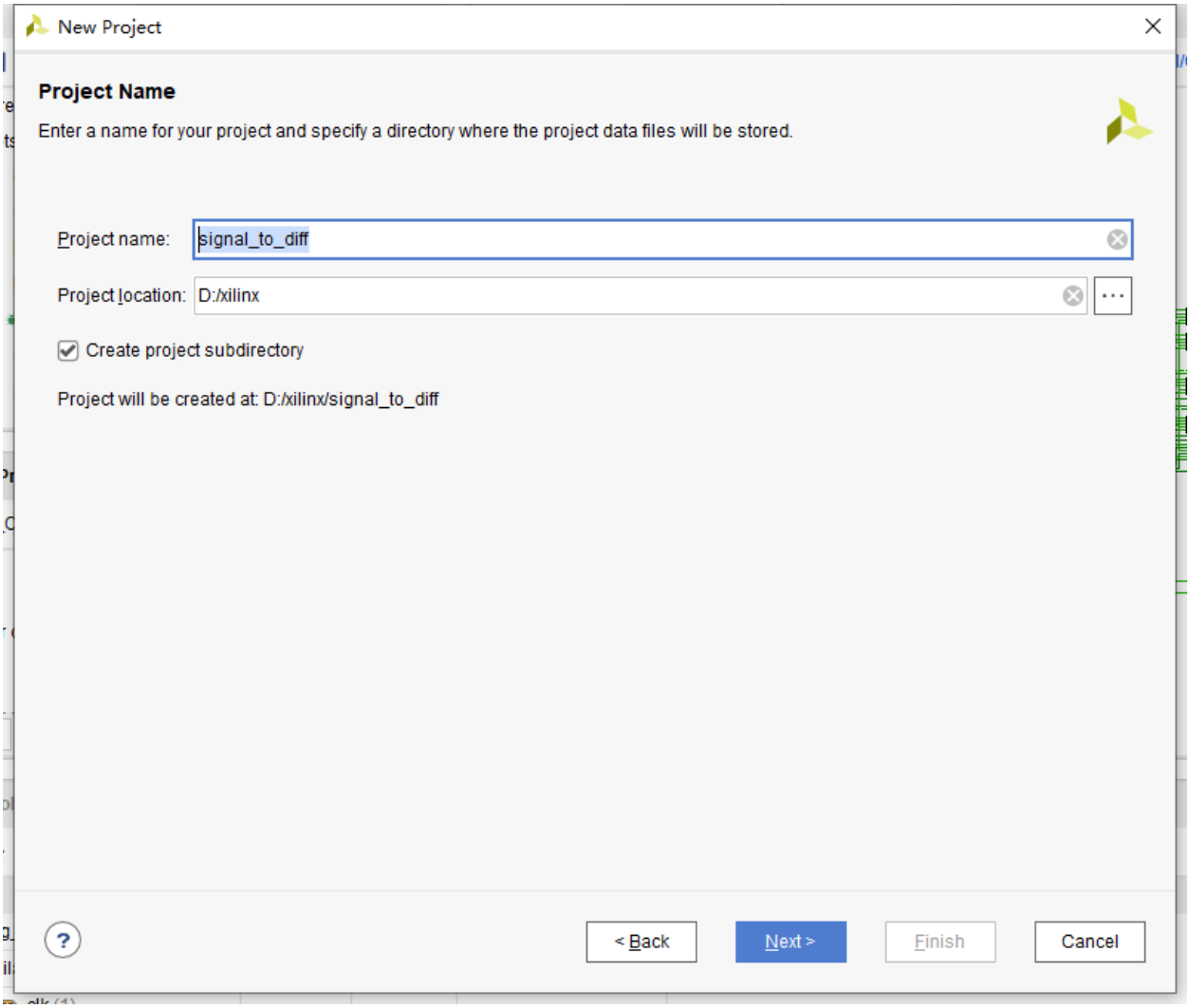
[L05]Vivado 原语 - 单端转差分

有些非常简单的功能,完全可以用原语实现,我这里重新新建一个工程,做一个单端转差分的工具,我工程名和模块都是signal_to_diff.

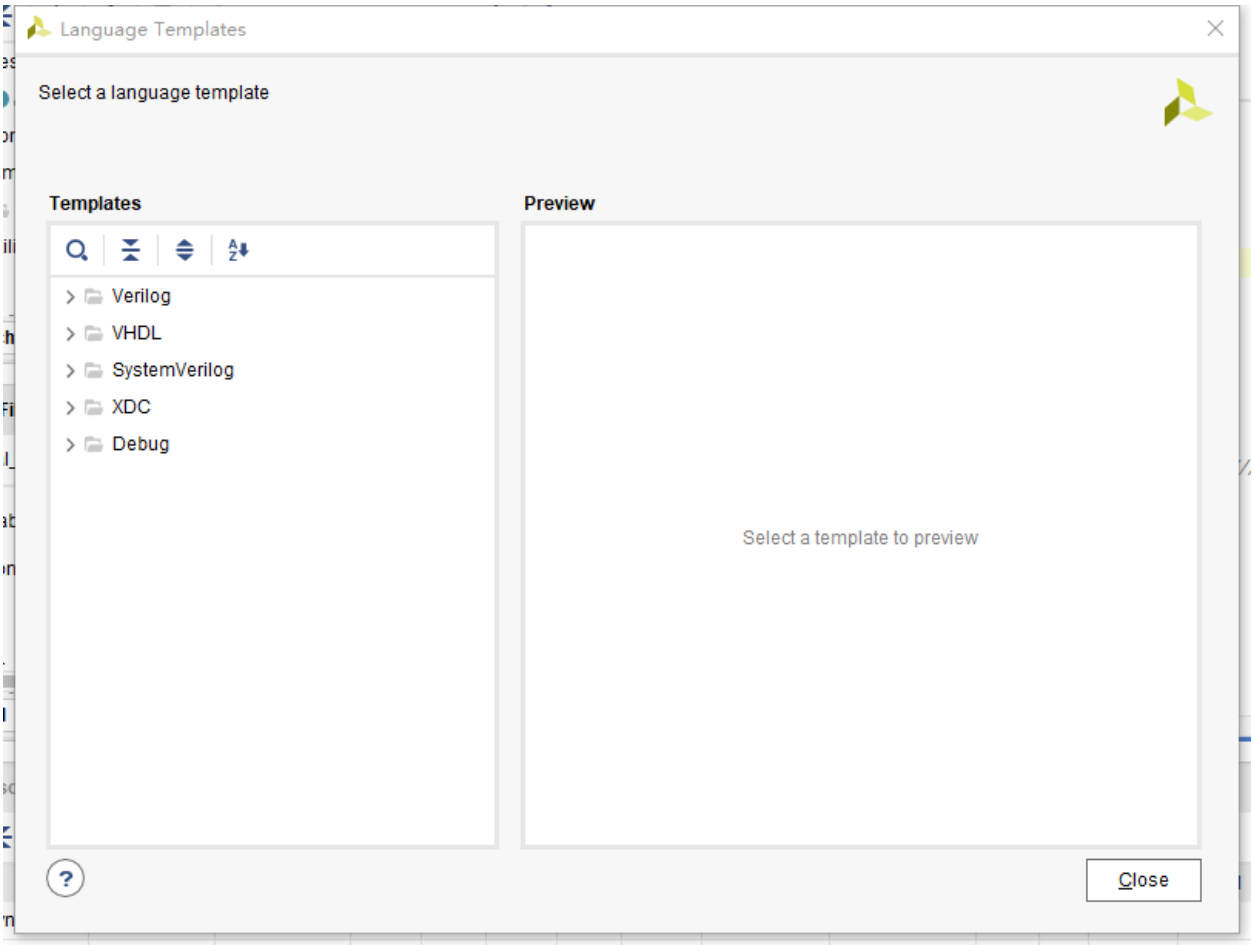


默认工程.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2022/02/22 17:57:49
```

```
// Design Name:
// Module Name: signal_to_diff
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module signal_to_diff(

    );
endmodule
```

选择菜单Tools→Language Templates



选择Verilog→Device Primitive Instantiation→Artix-7→I/O Components→Output Buffers→Differential Buffer (OBUFDS),从右侧看到了他的具体实现.

```
//     OBUFDS      : In order to incorporate this function into the design,
//     Verilog     : the following instance declaration needs to be placed
//    instance     : in the body of the design code.  The instance name
//   declaration   : (OBUFDS_inst) and/or the port declarations within the
//      code       : parenthesis may be changed to properly reference and
//                 : connect this function to the design.  Delete or comment
//                 : out inputs/outs that are not necessary.

//  <-----Cut code below this line---->

   // OBUFDS: Differential Output Buffer
   //         Artix-7
   // Xilinx HDL Language Template, version 2018.3

   OBUFDS #(
      .IOSTANDARD("DEFAULT"), // Specify the output I/O standard
      .SLEW("SLOW")           // Specify the output slew rate
   ) OBUFDS_inst (
```

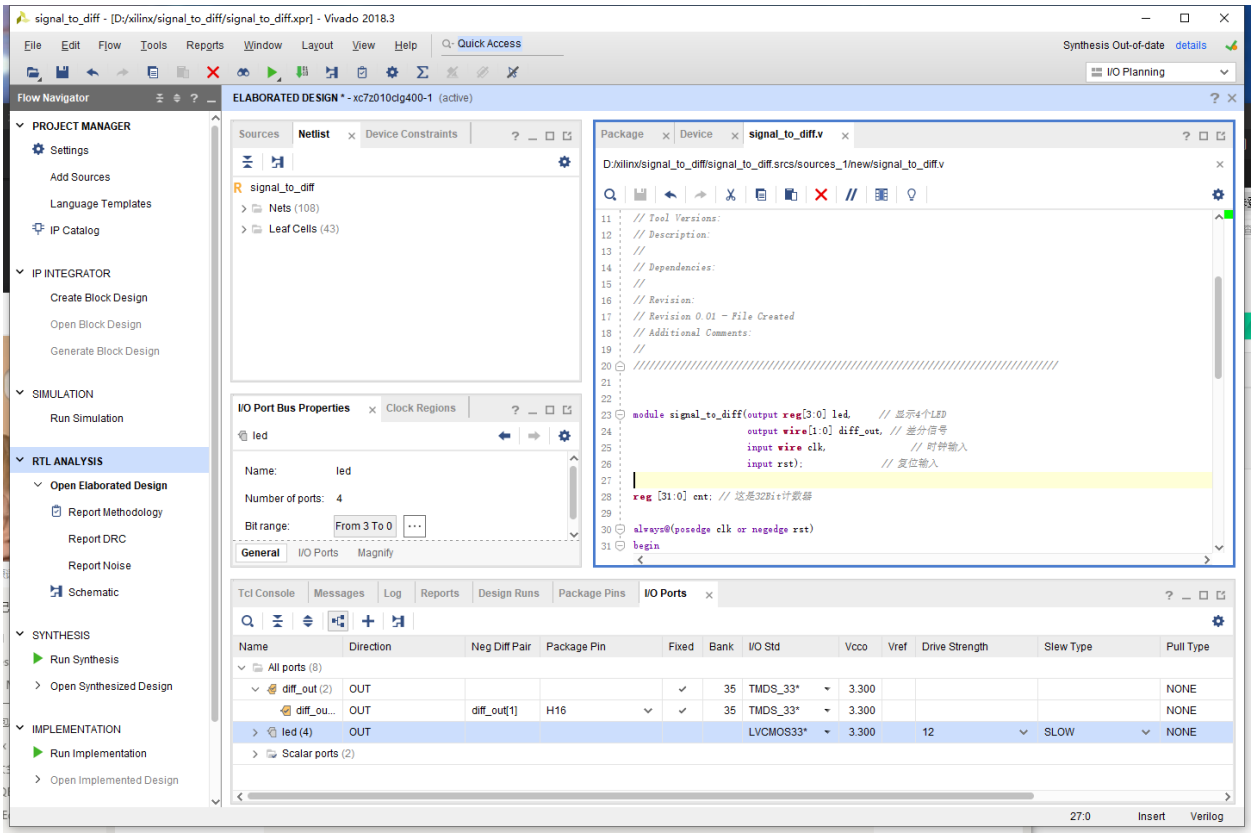
```
      .O(O),     // Diff_p output (connect directly to top-level port)
      .OB(OB),   // Diff_n output (connect directly to top-level port)
      .I(I)      // Buffer input
   );

   // End of OBUFDS_inst instantiation
```

结合一下流水灯例子.

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 2022/02/22 17:57:49
// Design Name:
// Module Name: signal_to_diff
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module signal_to_diff(output reg[3:0] led,     // 显示4个LED
                      output wire[1:0] diff_out, // 差分信号
                      input wire clk,                // 时钟输入
                      input rst);               // 复位输入

reg [31:0] cnt; // 这是32Bit计数器

always@(posedge clk or negedge rst)
begin
    if (!rst)
    begin
        cnt <= 'b0;
        led <= 'b0001;
    end
    else
    begin
        if (cnt == 25000000)
        begin
            cnt <= 'b0;
            led <= {led[0],led[3:1]};
```

```
        end
        else
        begin
            cnt <= cnt + 'b1;
        end
    end
end

OBUFDS #(
.IOSTANDARD("DEFAULT"), // Specify the output I/O standard
.SLEW("SLOW")           // Specify the output slew rate
) OBUFDS_inst (
.O(diff_out[0]),     // Diff_p output (connect directly to top-level port)
.OB(diff_out[1]),   // Diff_n output (connect directly to top-level port)
.I(clk)      // Buffer input
);

endmodule
```

差分的电平是TMDS,布线就在HDMI口上,引脚就是正常设置,差分引脚写一个另一个就会设置.



差分电平观察.

当然差分IO可以设置很多对.