3V General-Purpose CMOS Differential Input Single-Ended Rail-to-Rail Operational Amplifier

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***Abstract*—We design and simulate a rail-to-rail operational amplifier based on CMOS 0.6u technology and working at a power supply of 3V DC. The resulting circuit is robust throughout the common mode input voltage rate, low-consuming in terms of power and achieves gain larger than 87dB and unity gain frequency 43.7MHz, minimizing noise effects and combining high Power Supply Rejection Ratio (PSRR) and Common Mode Rejection Ratio (CMRR).**

I. Introduction

Operational amplifiers (OpAmps) are undoubtedly one of the most prominent fields in the spectrum of Analog Circuit Design and Electronics in general. The frenetic development of electronics has been characterized by Moore's law [1] that described a driving force of technological and social change, productivity, and economic growth [2]. In order to be in line with the rapid and greedy technological advances and demands, it is mandatory that OpAmps be continuously redesigned, aiming to increased efficiency and reliability and reduced size and power consumption.

In this work, we design and simulate a differential-input, single-ended, rail-to-rail 3V OpAmp, built on CMOS 0.6u technology. Since our work is project-based, we tackle certain specifications, presented in Table I. The problem of building a generic operational amplifier is well-known [3], [4], but novel, specifically designed and applied solutions emerge daily [5], [6]. Addressing the edifying character of our work, we first adopt and build upon standard CMOS design practices [7], [8], [9] and integrate these approaches with ideas from [10] and [11].

The rest of this report is organized as following: Section II presents our circuit design and topology, as well as the parameters we used for the simulation. The input stage, core amplifying stages and bias circuits are analyzed separately and in detail. Our choices are evaluated in Sec. III, including interesting visualization of our circuit's performance. Lastly, Sec. IV summarizes our work and several alternatives and possible future directions are discussed.

II. Circuit Design

A. Input Stage

Since our amplifier's input has to be differential, the input stage shall contain a differential pair. Furthermore, as the Common Mode Input Range (CMIR) should be nearly equal to the supply range (rail-to-rail amplifier), we combine a PMOS-based differential pair with an NMOS-based one. This topology offers the capability of high CMIR by controlling the active pairs and mirroring their currents. When common mode input voltage lies near the center of voltage supply (e.g. 1.5V in our case), both NMOS- and PMOS-based pairs are active. Carefully designing the circuit, we can ensure that equal value of current flows on both pairs and that each pair shows equal transconductance g_m. Hence, the total input transconductance should be $2g_m$. In cases of very high common mode input voltage, only the NMOS-based pair would conduct, while the inverse functionality would be observed in cases of very low common mode input voltage. This way, there is always at least one differential pair that conducts, thus leading to high CMIR. The chosen topology is shown in fig. 1.

TABLE I
THE REQUESTED PROJECT SPECIFICATIONS.

Parameter	Specification
DC Gain	>75 dB
Unity Gain Frequency	>20 MHz
Phase Margin	$>60^{\circ}$
Gain Margin	>8 dB
Input Common Mode Range	0 – 3 V
Output Swing	0.2 – 2.8 V
Current Consumption	Minimum Possible
Input-Referred Noise (f $\geq$ 1 kHz)	<60 nV/$\sqrt{\text{Hz}}$
Settling Time (0.1% error)	<40 ns
CMRR (f $\leq$ 100kHz)	>50 dB
PSRR (f $\leq$ 100kHz)	>50 dB

Extra circuits that ensure transconductance stability are also included (transistors MN4-MN6 and MP4-MP6), since, when a single pair conducts, the input transconductance is simply g_m. According to [7], a MOSFET's transconductance is directly proportional to the square root of its current, hence, theoretically, one should triple the value of the current that flows through the active pair (when the other is deactivated) in order to preserve the total input transconductance. However, deviations from this norm are more than common when concerning technologies under 1um, hence tripling the current does not solve the problem as expected. Experimentally, we chosen the transistors' widths as shown in Table II, where one can note that the current mirrors show width ratio drastically different than 3.

Notice that the differential pair's transitors are wide enough to achieve great input transconductance. Moreover, the PMOS to NMOS width ratio is approximately 3, ensuring equal transconductance for both pairs. The mirror transistors' width ratios are 2 and 1.6, proving that the assumption that a

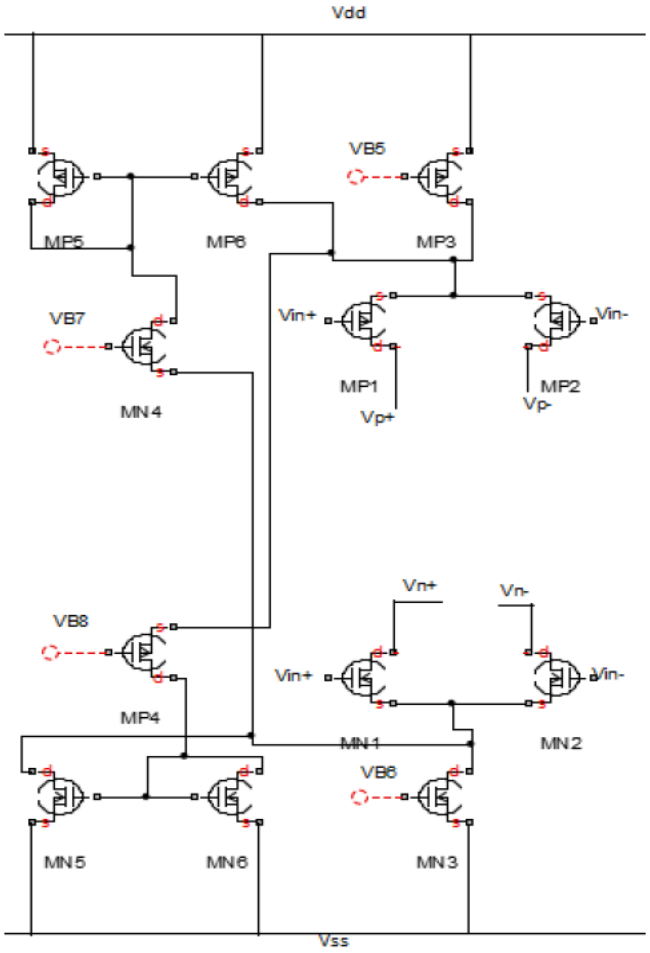

Fig. 1. The topology of the used input stage. In the core of this stage exists a combination of a PMOS-based (MP1-MP2) and an NMOS-based (MN1-MN2) differential pair that ensure high Common Mode Input Range. More transistors (MN4-MN6 and MP4-MP6) to ensure transconductance stability are also included.

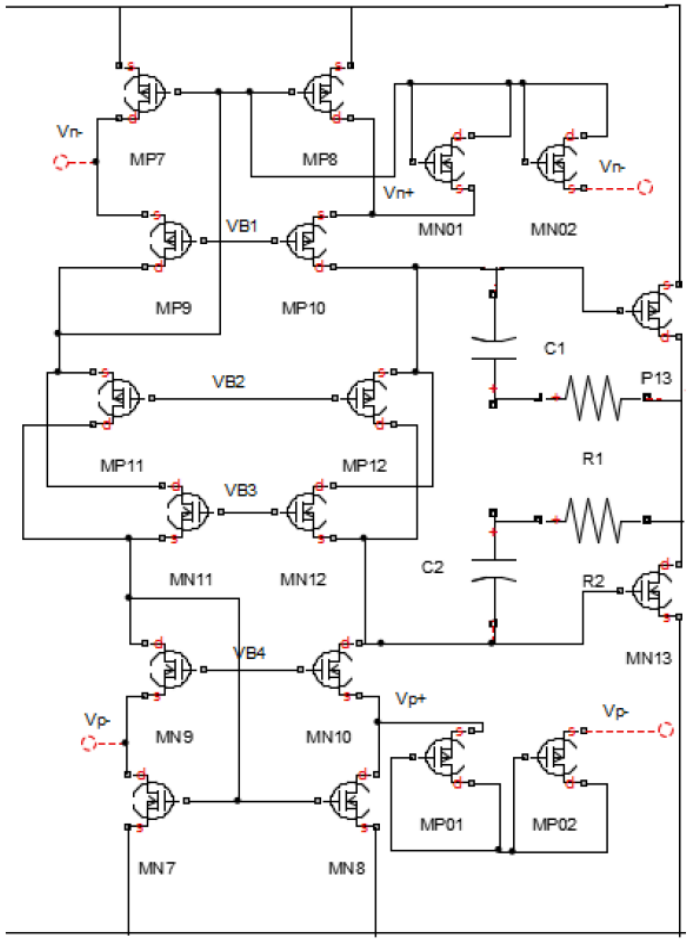

Fig. 2. The topology of the second stage's folded cascode amplifiers (transistors MN7-MN10 and MP7-MP10). The two pairs, MN11-MP11 and MN12-MP12, create translinear loops with bias transistors the MN7, MP7 and MN8, MP8 respectively. Transistors MN9-10 and MP9-10 provide the desired gain response. MN01-02 and MP01-02 serve as clamp resistors and improve settling time.

TABLE II
OUR CHOICE OF WIDTHS FOR THE TRANSISTORS OF THE INPUT STAGE.

Transistor	Width in um	Transistor	Width in um
MN1	220.5	MP1	660
MN2	220.5	MP2	660
MN3	24	MP3	24
MN4	75	MP4	105
MN5	30	MP5	15
MN6	15	MP6	24

MOSFET's transconductance is directly proportional to the square root of its current is not valid. Lastly, note that all transistors' length values are set to 1.2um. This is also true for all transistors of this design and will not be noted again.

B. Amplifier Core

Combining PMOS- and NMOS-based differential pairs is a common practice not only when designing the input stage, but throughout the whole circuit as well. More specifically, we generalize this approach by implementing a parallel connection of folded cascode amplifiers (transistors MN7-MN10 and MP7-MP10). Both the transconductance and the output resistance of these transistors are critical for the amplifier's gain and frequency response, therefore, their DC current should be stable and robust. For this reason, a wide-swing current mirror topology is employed and we apply practically constant bias current benefiting from the AB-type output stage bias technique. This approach can be seen in fig. 2. Two NMOS-PMOS pairs (MN11-MP11 and MN12-MP12), with each NMOS being parallel to the respective PMOS, are used to create translinear loops with bias transistors the MN7, MP7 and MN8, MP8 respectively. As a result, the DC current of MP9-10 and MN9-10 remains approximately the same throughout the whole CMIR.

The output stage is of AB type and is biased such as it shows a large output voltage swing. Lead compensation techniques are also used as frequency compensation methods. This is achieved with a serial connection of a 1.5pF capacitor to an 1kOhm resistance. The resistance is included in order to achieve extra phase margin in AC analysis, inserting and placing suitably a "zero" in the frequency response function.

Table III shows the choice of transistors' widths throughout the main amplifier stage. MN7-8 and MP7-8 are chosen to

TABLE III
OUR CHOICE OF WIDTHS FOR THE TRANSISTORS OF THE CORE STAGE.

Transistor	Width in um	Transistor	Width in um
MN7	144	MP7	540
MN8	144	MP8	540
MN9	108	MP9	360
MN10	108	MP10	360
MN11	90	MP11	330
MN12	90	MP12	330
MN13	252	MP13	900
MN01	150	MP01	450
MN02	150	MP02	450

TABLE IV
OUR CHOICE OF WIDTHS FOR THE TRANSISTORS OF THE BIAS CIRCUIT.

Transistor	NMOS Width(um)	PMOS Width(um)	Bias Voltage	Value (V)
M14	120	120	VB1	1.2
M15	71.4	75.6	VB2	0.4
M16	45	199.2	VB3	2.2
M17	78	360	VB4	1.5
M18	24	348	VB5	1.71
M19	158.4	24	VB6	0.92
M20	155.4	12	VB7	0.85
M21	18	489	VB8	1.8

be relatively wide in order to stabilize the DC voltage on the output stage's transistors' gates. Transistors MN9-10 and MP9-10 provide the desired gain response. MN11-12 and MP11-12 keep MN9-10 and MP9-10 transistors' current variations relatively small and standardize the DC operation point on the output stage's transistors' gates. The output stage's transistors are chosen wide, claiming for high current values and gain. Lastly, MN01-02 and MP01-02 serve as clamp resistors and improve settling time, as discussed in the 6th chapter of [9]. More discussion on these design choices will take place later on this paper.

C. Bias Circuit

The bias circuit aims to create and supply constant DC voltage that is needed throughout the circuit for biasing the different transistors. We applied the standard two-transistor bias technique as can be seen in fig. 3. The exact width values of the transistors are shown in table IV. Figure 4 also shows the whole schematic of our work. In order to facilitate the reader, some cable connections are omitted and are instead replaced by symbolic names, a standard practice that is also widely adopted by Cadence design tool. Thus, circuit points that carry a symbolic name are in fact connected to every other point that carries the same symbolic name (e.g. VB1-8).

III. SIMULATION AND RESULTS

We evaluate our design by simulating the circuit in Cadence Virtuoso. We used a single 3V supply and NCSU ami06 technology. The requested specifications and the measured results are shown in Table V.

Output transistors are always on, despite a non-constant voltage in their gates. This value can be stabilized by choosing a large size for MN7-8 and MP7-8. However, it seems that small variances of this value throughout the common mode input range, even in the order of 20mV, can cause a 10% variance on the effective voltage of the output transistors and thus, more than 20% variance on output current. Interestingly, the voltage difference between the gates of the two output

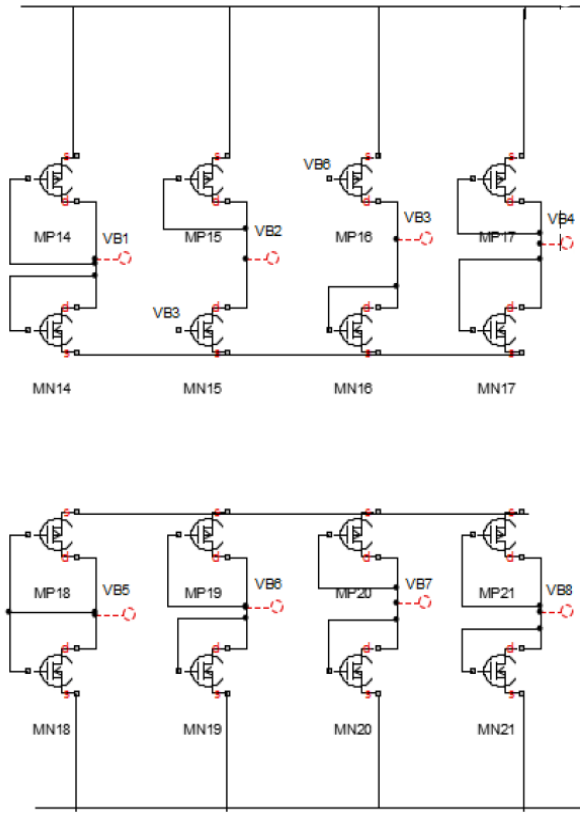

Fig. 3. Our design for the bias circuit.

TABLE V
COMPARISON BETWEEN REQUESTED SPECIFICATIONS AND ACHIEVED RESULTS.

Parameter	Specification	Specification	Vcm = 1.5 V
DC Gain	>75 dB	>87.2 dB	87.9 dB
Unity Gain Frequency	>20 MHz	>43.7 MHz	>47 MHz
Phase Margin	>60°	>70°	71°
Gain Margin	>8 dB	>9.5 dB	9.8 dB
Input Common Mode Range	0 – 3 V	-1.1 – 3.7 V	-
Output Swing	0.2 – 2.8 V	0.3 – 2.7 V	0.3 – 2.7 V
Current Consumption	Minimum Possible	13.5 mA	13.3 mA
Input-Referred Noise (f≥1kHz)	<60 nV/$\sqrt{\text{Hz}}$	<25.02 nV/$\sqrt{\text{Hz}}$	<24.6 nV/$\sqrt{\text{Hz}}$
Settling Time (0.1% error)	<40 ns	48.74 ns	48.74 ns
CMRR (f ≤ 100kHz)	>50 dB	>77 dB	>110 dB
PSRR (f ≤ 100kHz)	>50 dB	>55 dB	>95 dB

transistors remains the same, therefore, when the voltage increases in the PMOS gate, less current is forced, but at the same time the voltage also increases in the NMOS gate, making it to demand more current. This DC instability can be compensated by increasing the effective voltage, albeit reducing the output swing no less than 2.5V. The DC output voltage with respect to the common mode input voltage can be viewed in fig. 5.

A stable AC behavior throughout the common mode input range is highly desirable and can be achieved using techniques that stabilize the input transconductance, as discussed earlier. Figure 6 might be misleading, but the gain range is around only 0.8dB. Without any loss of generality, we also plot AC behavior when common mode input voltage is 1.5V (fig. 7).

The same stability is not present in the cases of CMRR

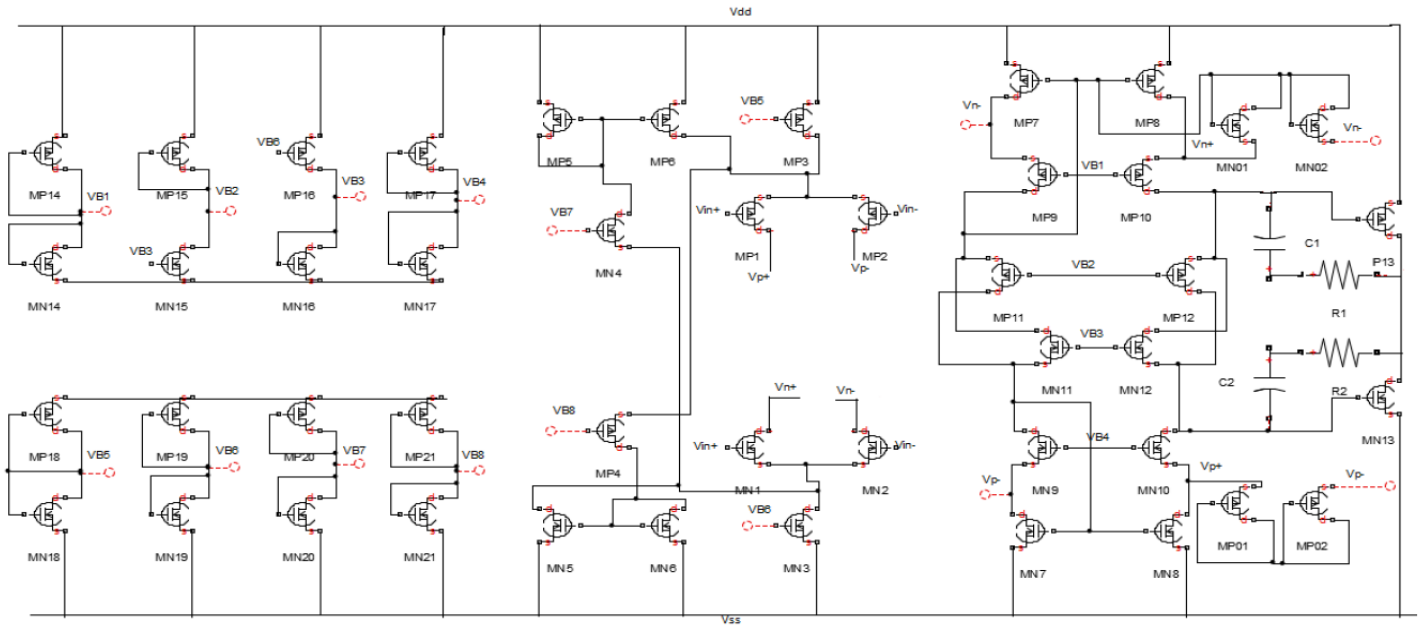

Fig. 4. The full schematic of our circuit.

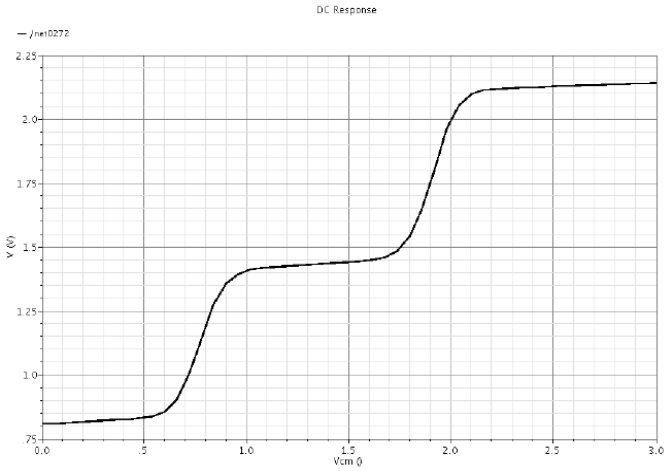

Fig. 5. DC output voltage with respect to common mode input voltage.

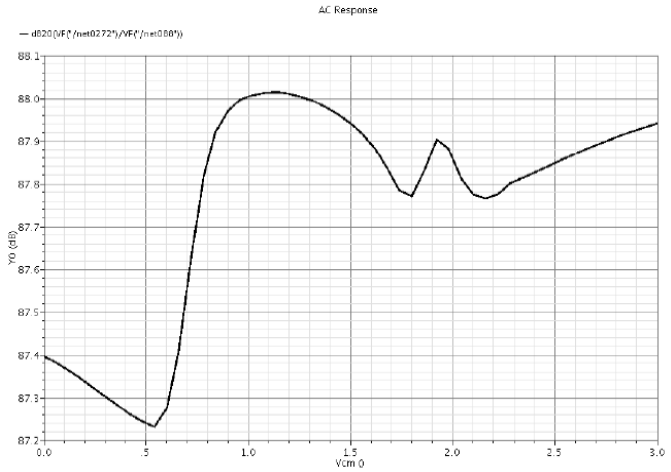

Fig. 6. AC output voltage magnitude with respect to common mode input voltage.

and PSRR, without this being vulnerable however. Figure 8 shows the common mode gain throughout the whole common mode input range. The peak at 1.92V is an interesting point to also plot common mode gain with respect to frequency (fig. 9). The way common mode input gain flows oractically allows for CMRR>77dB. Note that we measure CMRR as the difference between differential and common mode gain (in dB). Similarly, small signal supply gain is shown in fig. 10 and is decreasing when the frequency is increasing. Under 100kHz frequency, we obtain a PSRR of 55dB, as the difference between differential and small signal supply gain (in dB), when common mode voltage is 1.82V, i.e. the worst case scenario (fig. 11).

Next, to test input-referred noise, we simulate having a 10KOhms resistance connected to the input. Examining the noise levels, we observe reduction when the frequency increases, therefore, it is meaningful to plot input noise throughout the whole CMIR when the frequency is at 1kHz (fig 12). We measure the maximum noise level to be 25.02nV/$\sqrt{\text{Hz}}$.

Settling time is also measured, using unity feedback and parallel capacity-resistance load. The capacity is chosen to be 1pF, while the resistance 20KOhms. A plot for V_{cm}=1.5V can be seen in fig. 13. The settling time is the time that allows for the output to be oscillating no more than 0.1% around the desired value, here 2.5V.

Lastly, the total current consumption is about 13.5mA. It is interesting that only 2.5mA concern the main amplifier stages (input, second, output), with output current being 1.2mA. Most of the consumed current regards to biasing the different amplifier's stages.

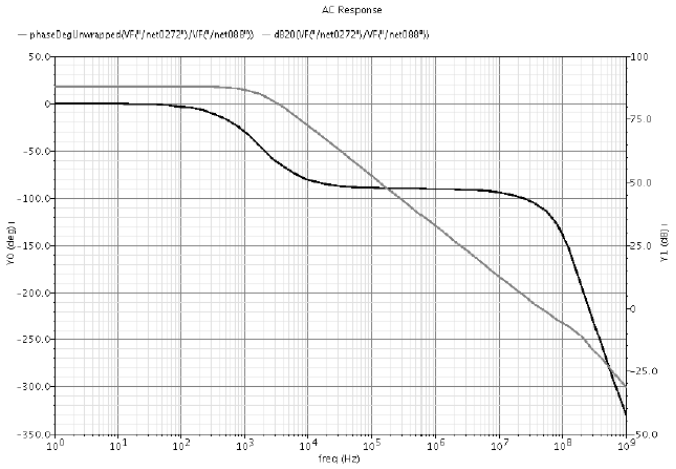

Fig. 7. Bode diagram of output voltage when common mode input voltage is 1.5V.

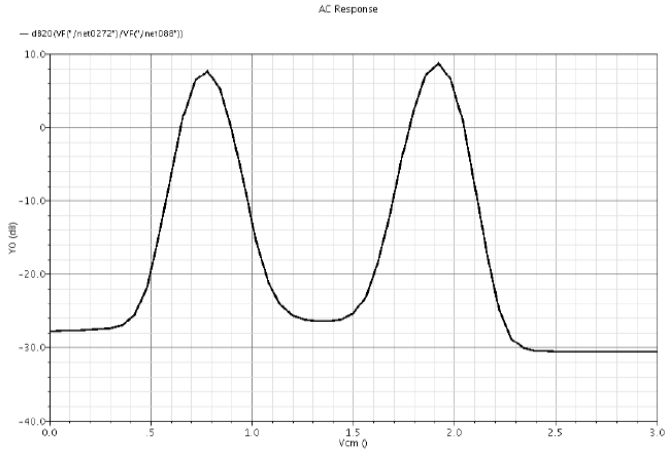

Fig. 8. Common mode gain with respect to common mode input voltage.

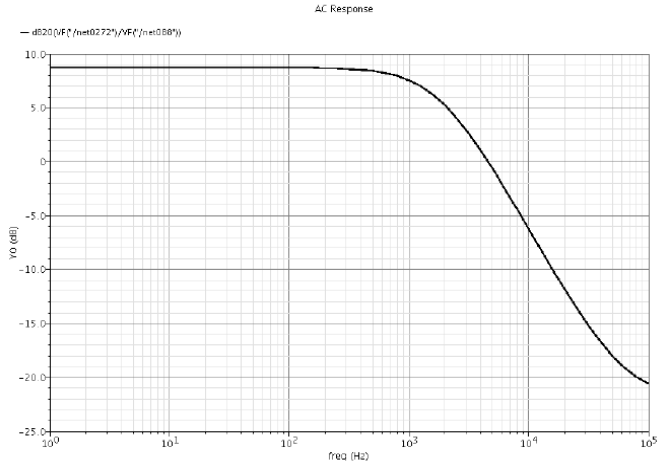

Fig. 9. Bode diagram of common mode gain when common mode input voltage is 1.92V.

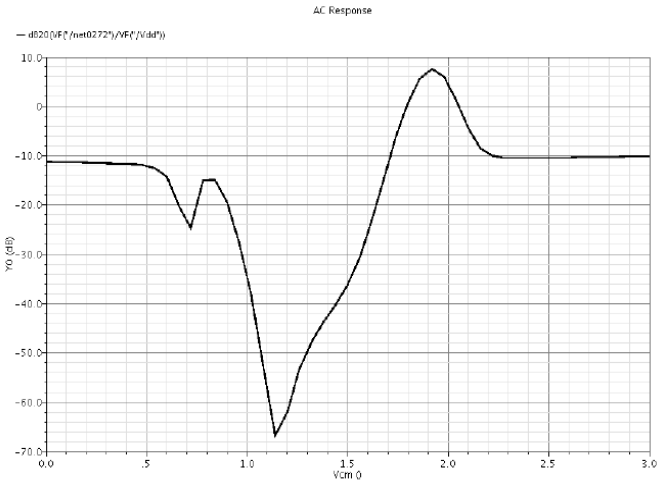

Fig. 10. Small signal supply gain with respect to common mode input voltage.

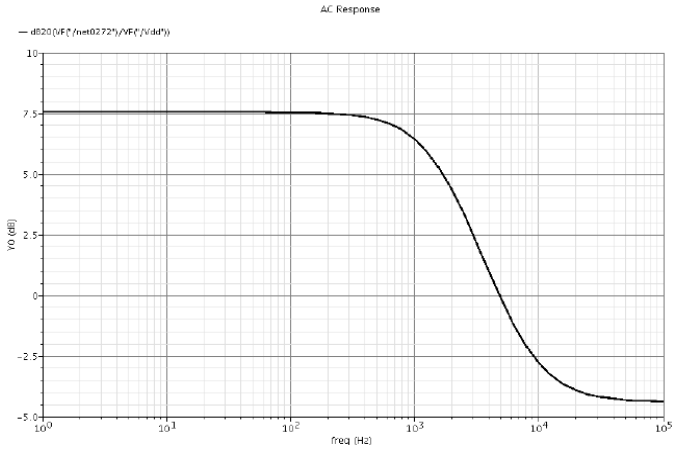

Fig. 11. Bode diagram of supply gain when common mode input voltage is 1.92V.

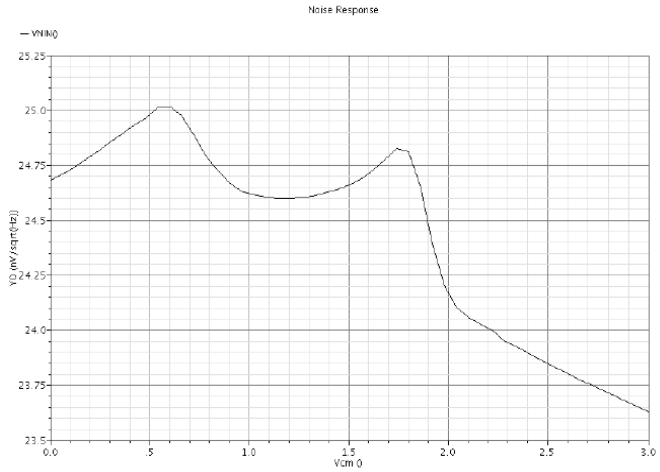

Fig. 12. Input-referred noise with respect to common mode input voltage.

IV. Discussion

We now further analyze and interpret our achieved results and justify our design choices. First, we showed that the hypothesis that a MOSFET's transconductance is directly proportional to the square root of its current is not valid for

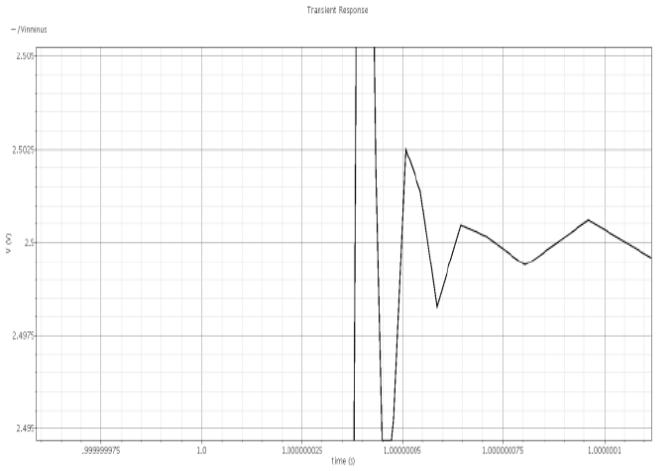

Fig. 13. Large signal (2.5V) step response when common mode input voltage is 1.5V.

small transistor sizes, such as that of the technology we used (0.6um). Thus, designing the circuit upon that assumption increased the gain of only one of the two differential pairs. A possible alternative would be to ensure that exactly one pair is active every time. In such a case, the total gain would increase and it would vacillate less. However, CMIR would then shrink, while the total would increase by a factor of 2, which is relatively small a difference in logarithmic scale, so we benefited CMIR in our design.

Regarding the phase margin, we overachieved the respective specification, providing space for improvement on both gain and unity-gain frequency. Nonetheless, since the respective specifications are successfully reached, we insisted on these choices as they ensure the output's robustness when a large input signal is applied.

The main specification that our design defaulted on, was the settling time. As one can observe in fig. 13, the cause behind this irregularity is rise time, as we designed the circuit so as to reduce overshoot, hence, settling time is approximately equal to rise time. Since slew rate mostly determines rise time, it seems that our circuit's rise speed has been limited. More specifically, slew rate is directly proportional to output current and inversely proportional to output capacity. We preferred to let a large output current value, but reducing the output capacity dramatically increases rise speed in a way that it causes overshoot. Even if settling time is reduced, we benefited a larger settling time over a not acceptable overshoot.

As explained earlier (Sec. III), some output swing was sacrificed for robustness and stability. Further stability can be achieved by increasing transistors' MN7-8 and MP7-8 current, a practice that also increases power supply demands. However, the most power consuming part is undoubtedly the bias circuit. In fact, were the current consumption a stricter specification, we should apply a different biasing topology with more transistors. That, on the other hand, increases both the circuit size and the designing complexity.

Lastly, a possible alternative for gain and unity-gain frequency is presented in [10] and includes adding mini amplifiers for driving MN9-10 and MP9-10. A similar strategy for increasing output resistance is discussed in chapter 6 of [9].

V. Conclusion

We designed and simulated a general purpose CMOS differential input single-ended rail-to-rail operational amplifier and tuned our circuit to achieve certain specifications. During our work, several practical issues arose and were addressed. Possible improvements would include more experiments on topologies to further decrease settling time. Another interesting approach could be to reimplement our circuit using an even lower transistor size, for instance, in a technology of nanometers.

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