How Does Union/Intersect

```
      setA
      ????????
      ????????
      01101011 01010100

      8
      14
      ?
      2
      13
      setB 01100011 01010100

      setA.union (setB)
      9
      6

      setA.intersect (setB)
      8
      14
      2
      13
```

Defining the Operators

The union, intersection and difference operations act on 2 sets to produce a third set. What's tricky is making sure these methods work correctly when they operate on sets of different sizes. For example,

```
Bitset union (Bitset setB)
{ Bitset temp = new Bitset (maxSize > setB.maxSize ? this : setB);
    int nbyte = Math.min (byteArray.length, setB.byteArray.length);
    for (int i = 0; i < nbyte; i++)
    {
        temp.byteArray[i] = (byte) (byteArray[i] | setB.byteArray[i]);
    }
    return temp;
}</pre>
```

Other Useful Set

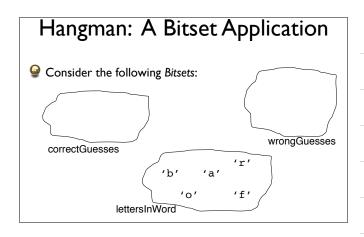
Frequently we need to operate on a single element of a set: to add it to the set, remove it from the set, or test whether it is present in the set. All these things are easy to do in terms of primitive **Bitset** operations:

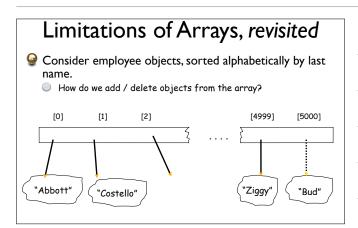
```
boolean member (int i)
{
    if (i >= maxSize) return false;
    else return (getBit (i) );
}

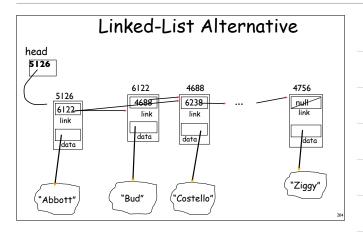
void include (int i)
{    if (i >= maxSize) error("Too big!"); setBit(i); }

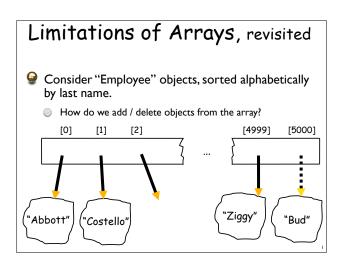
void exclude (int i)
{    if (i >= maxSize) error ("Too big!"); clearBit(i); }

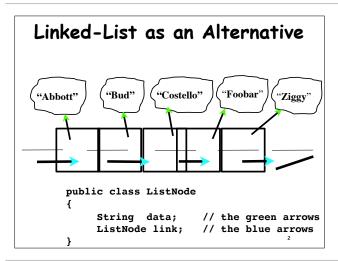
All the above check parameter i's validity.
```

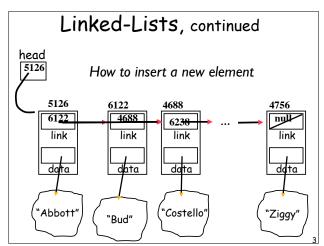


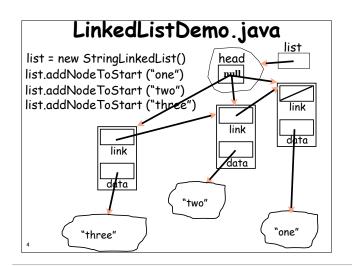


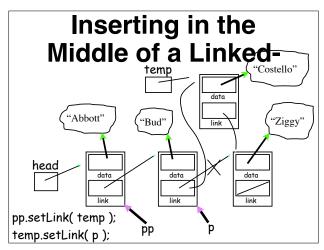


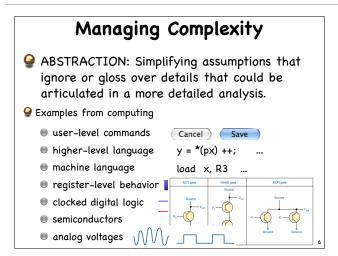




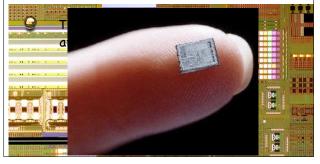


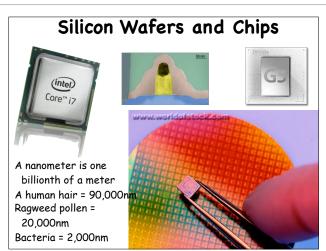


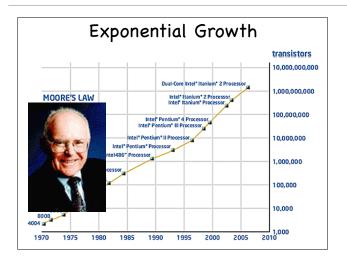




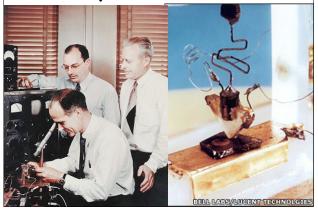
Computer Hardware







History of the Transistor



Machine Architecture

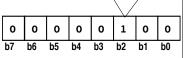
- The MIPS Processor Family
- A RISC architecture embodied by the R2000, R3000, R4000 and R6000 processors.
- MIPS Technologies = principal architect of embedded 32- and 64-bit RISC processors, licensed to system OEMs, semiconductor manufacturers, etc.
- See Britton: "Mips Assembly Language Programming" and http://www.cs.wisc.edu/~larus/spim.html
- Processor Performance
- \bigcirc Time per Task = C * T * I
 - C =Cycles per instruction
 - T = Time per cycle (clock speed)
 - I = Instructions per Task

Number Systems

Unsigned Binary Numbers

11111111

Bit Numbering



Binary Arithmetic

The usual algorithm works, with 1 + 1 = 0 (carry 1): $\begin{pmatrix} 1 & 1 \end{pmatrix}$

- Carry out of the MSB means the sum is too large to represent.
- Conversion of binary to decimal involves adding up the decimal values of the powers of 2 corresponding to the 1 bits. For example,

0 1 0 1 1 0 1 0

Signed Integers

- How many different integers can be represented using N bits?
- To "negate" an integer: form the two'scomplement by
- Taking the logical complement
- Adding one to the logical complement

What about negating zero?

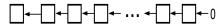
What is 1 1 1 1 1 1 1 1 7

What is 1 0 0 0 0 0 0 0

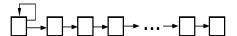
Doubling / Halving By Shifting

Doubling is accomplished via "arithmetic left shift"

Slide all bits one place to the LEFT, and make the new b₀ equal to 0.



Halving is accomplished via "arithmetic right shift"



Hexadecimal (base 16)

The 16 patterns of 4 bits are as follows:

Binary _	0000	0001	0010	0011	0100	0101	0110	0111
Decimal	0	1	2	3	4	5	6	7
Hex	0	1	2	3	4	5	6	7

Binary_	1000	1001	1010	1011	1100	1101	1110	1111
Decimal	8	9	10	11	12	13	14	15
Hex	8	9	А	В	С	D	Ε	F

So an 8-bit -1 would be FF. To distinguish such numbers from identifiers, we precede them by "0x" in C/C++ and in Java.

 $90 \times 69 = 100$

Data Sizes

The smallest unit of data that can be stored in \prime retrieved from memory is 1 byte = 8 bits



halfword

b 31	\mathbf{b}_0
	word

Memory addresses are byte addresses; ask for the byte at location 1001, and you'll get it.

Word addresses must be divisible by 4

Halfword addresses must be divisible by 2



The "Endian" Wars

- Big Endian: Most significant byte is in lowernumbered address
- e.g., M680x0, IBM mainframes, PowerPC, SPARC

msb			lsb
n	n+1	n+2	n+3

- Little Endian: Least significant byte is in lowernumbered address
- ⊕ e.g., Intel 80x86 and Core Duo, DEC Alpha & VAX

msb			lsb
n+3	n+2	n+1	n

- Total incompatibility between the two! BUT ...
- MIPS is bi-endian!