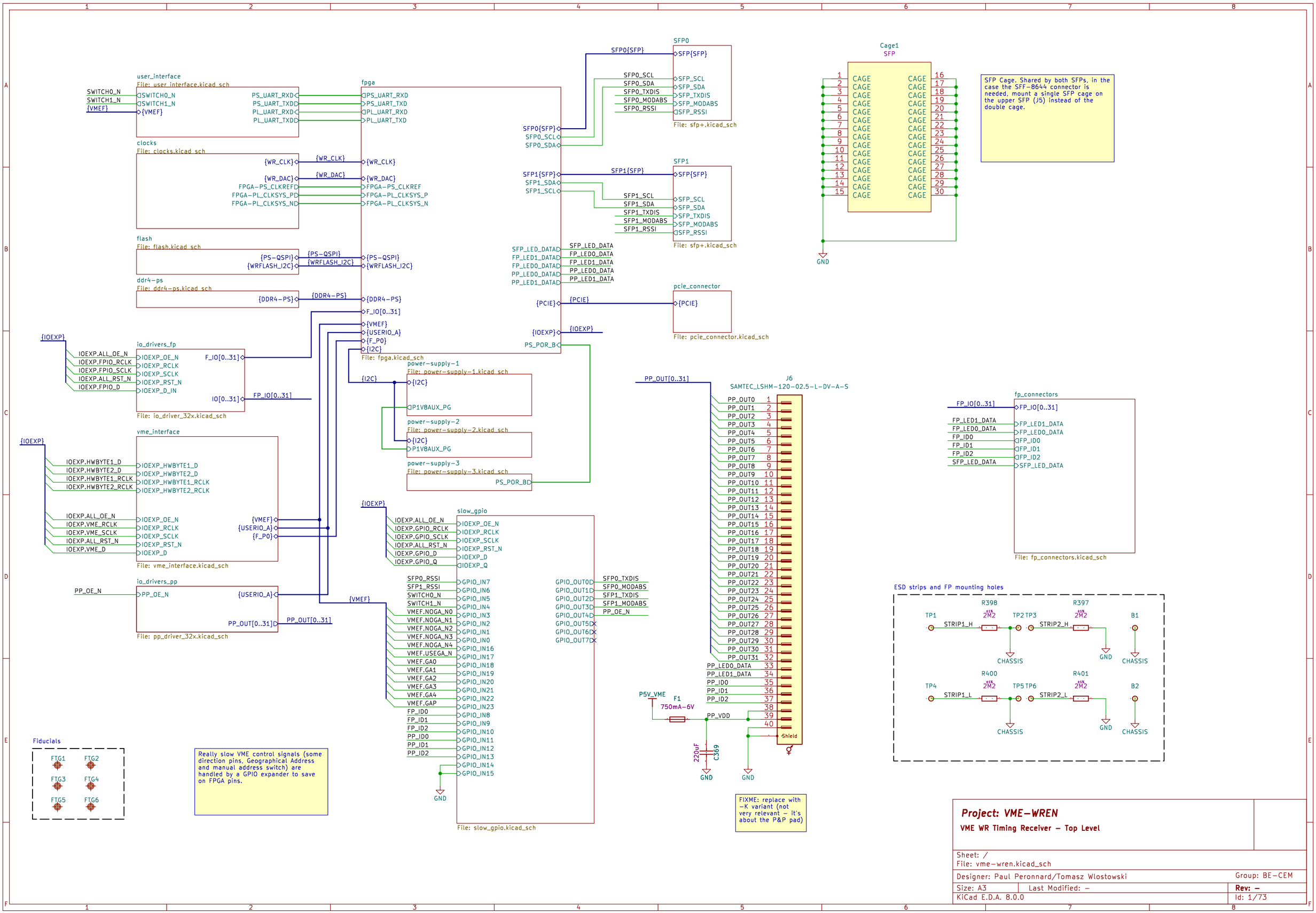
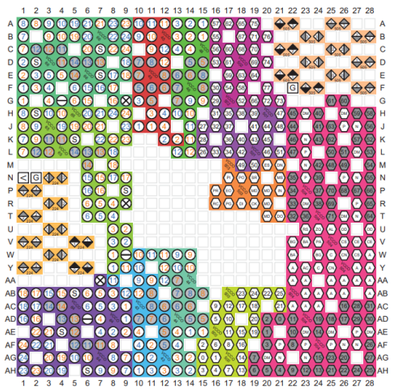
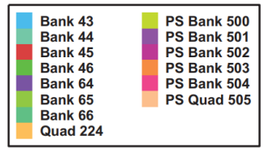
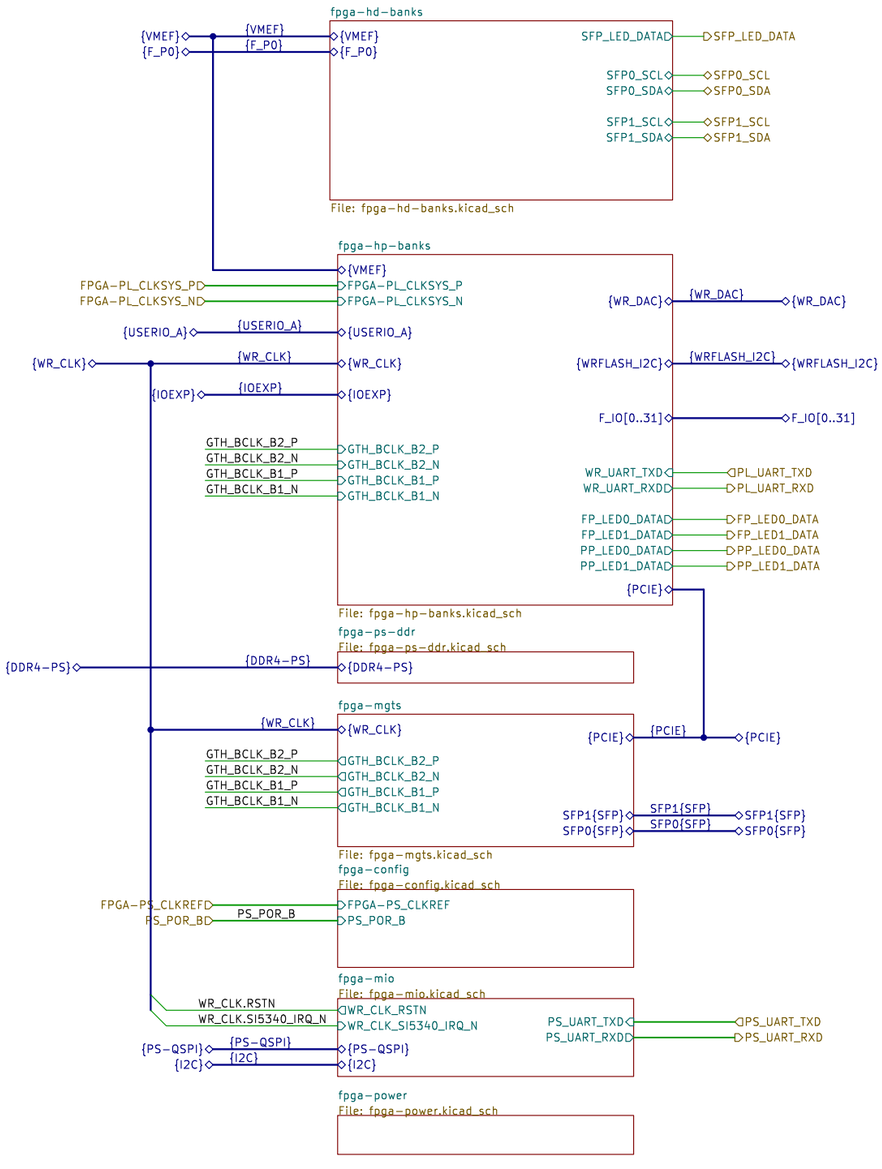

user_interface
File: user_interface.kicad_sch
SWITCH0_N
SWITCH1_N
{VMEF}
PS_UART_RXD
PS_UART_TXD
PL_UART_RXD
PL_UART_TXD
clocks
File: clocks.kicad_sch
{WR_CLK}
{WR_DAC}
FPGA-PS_CLKREFD
FPGA-PL_CLKSYS_PD
FPGA-PL_CLKSYS_ND
FPGA-PS_CLKREF
FPGA-PL_CLKSYS_P
FPGA-PL_CLKSYS_N
flash
File: flash.kicad_sch
{PS-QSPI}
{WRFLASH_I2C}
ddr4-ps
File: ddr4-ps.kicad_sch
{DDR4-PS}
fpga
F_IO[0..31]
{USERIO_A}
{F_P0}
{I2C}
File: fpga.kicad_sch
SFP0{SFP}
SFP0_SCL
SFP0_SDA
SFP0_TXDIS
SFP0_MODABS
SFP0_RSSI
SFP0
SFP{SFP}
SFP_SCL
SFP_SDA
SFP_TXDIS
SFP_MODABS
SFP_RSSI
File: sfp+.kicad_sch
SFP1{SFP}
SFP1_SDA
SFP1_SCL
SFP1_TXDIS
SFP1_MODABS
SFP1_RSSI
SFP1
SFP_LED_DATA
FP_LED0_DATA
FP_LED1_DATA
PP_LED0_DATA
PP_LED1_DATA
{PCIE}
pcie_connector
File: pcie_connector.kicad_sch
{IOEXP}
PS_POR_B
Cage1
SFP
CAGE
GND
SFP Cage. Shared by both SFPs, in the case the SFF-8644 connector is needed, mount a single SFP cage on the upper SFP (J5) instead of the double cage.
io_drivers_fp
IOEXP.ALL_OE_N
IOEXP.FPIO_RCLK
IOEXP.FPIO_SCLK
IOEXP.ALL_RST_N
IOEXP.FPIO_D
IOEXP_OE_N
IOEXP_RCLK
IOEXP_SCLK
IOEXP_RST_N
IOEXP_D_IN
IO[0..31]
FP_IO[0..31]
File: io_driver_32x.kicad_sch
power-supply-1
File: power-supply-1.kicad_sch
{I2C}
P1V8AUX_PG
power-supply-2
File: power-supply-2.kicad_sch
power-supply-3
File: power-supply-3.kicad_sch
PS_POR_BD
vme_interface
IOEXP.HWBYTE1_D
IOEXP.HWBYTE2_D
IOEXP.HWBYTE1_RCLK
IOEXP.HWBYTE2_RCLK
IOEXP_HWBYTE1_D
IOEXP_HWBYTE2_D
IOEXP_HWBYTE1_RCLK
IOEXP_HWBYTE2_RCLK
IOEXP.VME_RCLK
IOEXP.VME_SCLK
IOEXP.VME_D
IOEXP_RCLK
IOEXP_SCLK
IOEXP_D
{VMEF}
{USERIO_A}
{F_P0}
File: vme_interface.kicad_sch
io_drivers_pp
PP_OE_N
PP_OUT[0..31]
File: pp_driver_32x.kicad_sch
slow_gpio
IOEXP.GPIO_RCLK
IOEXP.GPIO_SCLK
IOEXP.GPIO_D
IOEXP.GPIO_Q
IOEXP_RCLK
IOEXP_SCLK
IOEXP_D
IOEXP_Q
SFP0_RSSI
SFP1_RSSI
SWITCH0_N
SWITCH1_N
VMEF.NOGA_N0
VMEF.NOGA_N1
VMEF.NOGA_N2
VMEF.NOGA_N3
VMEF.NOGA_N4
VMEF.USEGA_N
VMEF.GA0
VMEF.GA1
VMEF.GA2
VMEF.GA3
VMEF.GA4
VMEF.GAP
FP_ID0
FP_ID1
FP_ID2
PP_ID0
PP_ID1
PP_ID2
GPIO_IN7
GPIO_IN6
GPIO_IN5
GPIO_IN4
GPIO_IN3
GPIO_IN2
GPIO_IN1
GPIO_IN0
GPIO_IN16
GPIO_IN17
GPIO_IN18
GPIO_IN19
GPIO_IN20
GPIO_IN21
GPIO_IN22
GPIO_IN23
GPIO_IN8
GPIO_IN9
GPIO_IN10
GPIO_IN11
GPIO_IN12
GPIO_IN13
GPIO_IN14
GPIO_IN15
GPIO_OUT0
GPIO_OUT1
GPIO_OUT2
GPIO_OUT3
GPIO_OUT4
GPIO_OUT5
GPIO_OUT6
GPIO_OUT7
SFP0_TXDIS
SFP0_MODABS
SFP1_TXDIS
SFP1_MODABS
PP_OE_N
File: slow_gpio.kicad_sch
Really slow VME control signals (some direction pins, Geographical Address and manual address switch) are handled by a GPIO expander to save on FPGA pins.
PP_OUT[0..31]
J6
SAMTEC_LSHM-120-02.5-L-DV-A-S
PP_OUT0
PP_OUT1
PP_OUT2
PP_OUT3
PP_OUT4
PP_OUT5
PP_OUT6
PP_OUT7
PP_OUT8
PP_OUT9
PP_OUT10
PP_OUT11
PP_OUT12
PP_OUT13
PP_OUT14
PP_OUT15
PP_OUT16
PP_OUT17
PP_OUT18
PP_OUT19
PP_OUT20
PP_OUT21
PP_OUT22
PP_OUT23
PP_OUT24
PP_OUT25
PP_OUT26
PP_OUT27
PP_OUT28
PP_OUT29
PP_OUT30
PP_OUT31
PP_LED0_DATA
PP_LED1_DATA
PP_ID0
PP_ID1
PP_ID2
Shield
P5V_VME
F1
750mA-6V
PP_VDD
220uF
C369
GND
FIXME: replace with -K variant (not very relevant - it's about the P&P pad)
fp_connectors
FP_IO[0..31]
FP_LED1_DATA
FP_LED0_DATA
FP_ID0
FP_ID1
FP_ID2
SFP_LED_DATA
File: fp_connectors.kicad_sch
ESD strips and FP mounting holes
R398
R397
R400
R401
2M2
TP1
TP2
TP3
TP4
TP5
TP6
STRIP1_H
STRIP2_H
STRIP1_L
STRIP2_L
B1
B2
CHASSIS
GND
Fiducials
FTG1
FTG2
FTG3
FTG4
FTG5
FTG6
Project: VME-WREN
VME WR Timing Receiver - Top Level
Sheet: /
File: vme-wren.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A3
Last Modified: -
Rev: -
KiCad E.D.A. 8.0.0
Id: 1/73

PS GTR 505	PS MIO 502	HD I/O Bank 46 F	HP I/O Bank 66 D	SYSMON Configuration	GTH Quad 226 X0Y12-X0Y15
PS DDR 504	PS MIO 501	HD I/O Bank 45 E	HP I/O Bank 65 C	Configuration	GTH Quad 225 X0Y8-X0Y11
PS CONFIG 503	PS MIO 500	HD I/O Bank 44 N	HP I/O Bank 64 B	PCIE4 X0Y1 (tandem)	GTH Quad 224 X0Y4-X0Y7 A [R] (RCAL)
		HD I/O Bank 43 O	HP I/O Bank 63	PCIE4 X0Y0	GTH Quad 223 X0Y0-X0Y3

! LVPECL not supported by this FPGA (no HR banks) !







Project: VME–WREN

FPGA Main Sheet

Sheet: /fpga/
File: fpga.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE–CEM

Size: A3 — Last Modified: – — **Rev: –**

KiCad E.D.A. 8.0.0 — Id: 2/73

FPGA-PL_CLKSYS_P
FPGA-PL_CLKSYS_N
{WRFLASH_I2C}
WRFLASH_I2C.SDA
WRFLASH_I2C.SCL
{WR_DAC}
WR_DAC.SCLK
WR_DAC.DIN
WR_DAC.SYNC
{WR_CLK}
WR_CLK.25M_HELPER
WR_CLK.PPS
WR_CLK.ABSCAL
WR_CLK.AUX_P
WR_CLK.AUX_N
WR_CLK.MAIN_P
WR_CLK.MAIN_N
WR_CLK.HELPER_P
WR_CLK.HELPER_N
WR_CLK.RSTN
WR_CLK.SPI_MOSI
WR_CLK.SPI_SCK
WR_CLK.SPI_MISO
WR_CLK.SPI_HELPER_CS_N
WR_CLK.SPI_MAIN_CS_N
{PCIE}
PCIE.PERST_N
R444 100
R445 100
GTH_BCLK_B1_P
GTH_BCLK_B1_N
GTH_BCLK_B2_P
GTH_BCLK_B2_N
{USERIO_A}
F_IO[0..31]

IC14E
XCZU4CG-1SFVC784E
BANK 64

IO_L1P_T0L_N0_DBC_64	AC9	VMEF.D_OE_N
IO_L1N_T0L_N1_DBC_64	AD9	VMEF.D20
IO_L2P_T0L_N2_64	AE9	VMEF.D18
IO_L2N_T0L_N3_64	AE8	F_IOEXP_HWBYTE2_D
IO_L3P_T0L_N4_AD15P_64	AB8	VMEF.D22
IO_L3N_T0L_N5_AD15N_64	AC8	VMEF.D4
IO_L4P_T0U_N6_DBC_AD7P_64	AD7	VMEF.D21
IO_L4N_T0U_N7_DBC_AD7N_64	AE7	HP4
IO_L5P_T0U_N8_AD14P_64	AB7	HP9
IO_L5N_T0U_N9_AD14N_64	AC7	VMEF.D5
IO_L6P_T0U_N10_AD6P_64	AB6	VMEF.D15
IO_L6N_T0U_N11_AD6N_64	AC6	VMEF.D2
IO_L7P_T1L_N0_QBC_AD13P_64	AG9	VMEF.D7
IO_L7N_T1L_N1_QBC_AD13N_64	AH9	VMEF.D6
IO_L8P_T1L_N2_AD5P_64	AF8	VMEF.D19
IO_L8N_T1L_N3_AD5N_64	AG8	VMEF.D16
IO_L9P_T1L_N4_AD12P_64	AH8	VMEF.D31
IO_L9N_T1L_N5_AD12N_64	AH7	VMEF.D3
IO_L10P_T1U_N6_QBC_AD4P_64	AG6	VMEF.D1
IO_L10N_T1U_N7_QBC_AD4N_64	AG5	VMEF.D0
IO_L11P_T1U_N8_GC_64	AF7	GTH_BCLK_B1_P
IO_L11N_T1U_N9_GC_64	AF6	GTH_BCLK_B1_N
IO_L12P_T1U_N10_GC_64	AE5	GTH_BCLK_B2_P
IO_L12N_T1U_N11_GC_64	AF5	GTH_BCLK_B2_N
IO_L13P_T2L_N0_GC_QBC_64	AD5	VMEF.D13
IO_L13N_T2L_N1_GC_QBC_64	AD4	USERIO_A.IO14
IO_L14P_T2L_N2_GC_64	AC4	USERIO_A.IO6
IO_L14N_T2L_N3_GC_64	AC3	USERIO_A.IO12
IO_L15P_T2L_N4_AD11P_64	AB4	USERIO_A.IO9
IO_L15N_T2L_N5_AD11N_64	AB3	USERIO_A.IO10
IO_L16P_T2U_N6_QBC_AD3P_64	AD2	USERIO_A.IO13
IO_L16N_T2U_N7_QBC_AD3N_64	AD1	VMEF.D28
IO_L17P_T2U_N8_AD10P_64	AB2	USERIO_A.IO8
IO_L17N_T2U_N9_AD10N_64	AC2	USERIO_A.IO11
IO_L18P_T2U_N10_AD2P_64	AB1	VMEF.D30
IO_L18N_T2U_N11_AD2N_64	AC1	VMEF.D29
IO_L19P_T3L_N0_DBC_AD9P_64	AG4	VMEF.D12
IO_L19N_T3L_N1_DBC_AD9N_64	AH4	VMEF.D14
IO_L20P_T3L_N2_AD1P_64	AG3	VMEF.D10
IO_L20N_T3L_N3_AD1N_64	AH3	VMEF.D11
IO_L21P_T3L_N4_AD8P_64	AE3	VMEF.D_DIR
IO_L21N_T3L_N5_AD8N_64	AF3	VMEF.D9
IO_L22P_T3U_N6_DBC_AD0P_64	AE2	USERIO_A.IO15
IO_L22N_T3U_N7_DBC_AD0N_64	AF2	VMEF.D8
IO_L23P_T3U_N8_64	AH2	VMEF.D24
IO_L23N_T3U_N9_64	AH1	VMEF.D25
IO_L24P_T3U_N10_64	AF1	VMEF.D27
IO_L24N_T3U_N11_64	AG1	VMEF.D26
IO_T0U_N12_VRP_64	AD6	VMEF.D17
IO_T1U_N12_64	AH6	VMEF.D17
IO_T2U_N12_64	AB5	USERIO_A.IO4
IO_T3U_N12_64	AE4	VMEF.D23

AD6 — 240 R22 — GND

{VMEF}
VMEF.D0 VMEF.D1 VMEF.D2 VMEF.D3 VMEF.D4 VMEF.D5 VMEF.D6 VMEF.D7 VMEF.D8 VMEF.D9 VMEF.D10 VMEF.D11 VMEF.D12 VMEF.D13 VMEF.D14 VMEF.D15 VMEF.D16 VMEF.D17 VMEF.D18 VMEF.D19 VMEF.D20 VMEF.D21 VMEF.D22 VMEF.D23 VMEF.D24 VMEF.D25 VMEF.D26 VMEF.D27 VMEF.D28 VMEF.D29 VMEF.D30 VMEF.D31 VMEF.D_OE_N VMEF.D_DIR

Pins almost freely swappable except clocks. R444 and R445 are left deliberately (Tom's experiments with SD-DDS).

IC14F
XCZU4CG-1SFVC784E
BANK 65

IO_L1P_T0L_N0_DBC_65	W8	USERIO_A.IO5
IO_L1N_T0L_N1_DBC_65	Y8	USERIO_A.IO3
IO_L2P_T0L_N2_65	U9	HP50
IO_L2N_T0L_N3_65	V9	F_IOEXP_HWBYTE1_D
IO_L3P_T0L_N4_AD15P_65	U8	USERIO_A.IO1
IO_L3N_T0L_N5_AD15N_65	V8	USERIO_A.IO2
IO_L4P_T0U_N6_DBC_AD7P_SMBALERT_65	R8	HP54
IO_L4N_T0U_N7_DBC_AD7N_65	T8	HP55
IO_L5P_T0U_N8_AD14P_65	R7	USERIO_A.IO29
IO_L5N_T0U_N9_AD14N_65	T7	USERIO_A.IO31
IO_L6P_T0U_N10_AD6P_65	R6	USERIO_A.IO30
IO_L6N_T0U_N11_AD6N_65	T6	USERIO_A.IO0
IO_L7P_T1L_N0_QBC_AD13P_65	L1	F_IOEXP_HWBYTE2_RCLK
IO_L7N_T1L_N1_QBC_AD13N_65	K1	F_IO22
IO_L8P_T1L_N2_AD5P_65	J1	F_IO20
IO_L8N_T1L_N3_AD5N_65	H1	F_IO18
IO_L9P_T1L_N4_AD12P_65	K2	F_IO21
IO_L9N_T1L_N5_AD12N_65	J2	F_IO19
IO_L10P_T1U_N6_QBC_AD4P_65	H4	F_IO29
IO_L10N_T1U_N7_QBC_AD4N_65	H3	F_IO30
IO_L11P_T1U_N8_GC_65	K4	USERIO_A.IO22
IO_L11N_T1U_N9_GC_65	K3	USERIO_A.IO21
IO_L12P_T1U_N10_GC_65	L3	USERIO_A.IO23
IO_L12N_T1U_N11_GC_65	L2	F_IO23
IO_L13P_T2L_N0_GC_QBC_65	L7	F_IOEXP_HWBYTE1_RCLK
IO_L13N_T2L_N1_GC_QBC_65	L6	USERIO_A.IO19
IO_L14P_T2L_N2_GC_65	M6	USERIO_A.IO16
IO_L14N_T2L_N3_GC_65	L5	USERIO_A.IO25
IO_L15P_T2L_N4_AD11P_65	N7	F_WRCLK_SPI_MOSI
IO_L15N_T2L_N5_AD11N_65	N6	USERIO_A.IO26
IO_L16P_T2U_N6_QBC_AD3P_65	P7	USERIO_A.IO27
IO_L16N_T2U_N7_QBC_AD3N_65	P6	USERIO_A.IO28
IO_L17P_T2U_N8_AD10P_65	N9	F_WRCLK_SPI_SCK
IO_L17N_T2U_N9_AD10N_65	N8	F_SPI_MAIN_CS_N
IO_L18P_T2U_N10_AD2P_65	M8	F_SPI_HELPER_CS_N
IO_L18N_T2U_N11_AD2N_65	L8	F_PERST_N
IO_L19P_T3L_N0_DBC_AD9P_65	J5	USERIO_A.IO20
IO_L19N_T3L_N1_DBC_AD9N_65	J4	USERIO_A.IO24
IO_L20P_T3L_N2_AD1P_65	J6	HP72
IO_L20N_T3L_N3_AD1N_65	H6	F_IO27
IO_L21P_T3L_N4_AD8P_65	J7	F_WR_DAC_DIN
IO_L21N_T3L_N5_AD8N_65	H7	F_IO31
IO_L22P_T3U_N6_DBC_AD0P_65	K8	F_IO2
IO_L22N_T3U_N7_DBC_AD0N_65	K7	F_IOEXP_ALL_OE_N
IO_L23P_T3U_N8_I2C_SCLK_65	K9	F_WR_DAC_SCLK
IO_L23N_T3U_N9_65	J9	F_IO1
IO_L24P_T3U_N10_PERSTN1_I2C_SDA_65	H9	F_WR_UART_TXD
IO_L24N_T3U_N11_PERSTN0_65	H8	F_WR_DAC_SYNC
IO_T0U_N12_VRP_65	W9	F_IO16
IO_T1U_N12_65	H2	F_IO16
IO_T2U_N12_65	P9	F_WRCLK_SPI_MISO
IO_T3U_N12_65	K5	HP98

W9 — 240 R20 — GND

C546 P3V3 GND
C547 P1V8 GND

IC14G
XCZU4CG-1SFVC784E
BANK 66

IO_L1P_T0L_N0_DBC_66	G1	F_IO17
IO_L1N_T0L_N1_DBC_66	F1	F_IO15
IO_L2P_T0L_N2_66	E1	F_IO13
IO_L2N_T0L_N3_66	D1	F_IO11
IO_L3P_T0L_N4_AD15P_66	F2	F_IO14
IO_L3N_T0L_N5_AD15N_66	E2	F_IO12
IO_L4P_T0U_N6_DBC_AD7P_66	G3	F_IO28
IO_L4N_T0U_N7_DBC_AD7N_66	F3	F_IO25
IO_L5P_T0U_N8_AD14P_66	E4	F_IO7
IO_L5N_T0U_N9_AD14N_66	E3	F_IO24
IO_L6P_T0U_N10_AD6P_66	G5	USERIO_A.IO18
IO_L6N_T0U_N11_AD6N_66	F5	F_IO6
IO_L7P_T1L_N0_QBC_AD13P_66	C1	F_IO9
IO_L7N_T1L_N1_QBC_AD13N_66	B1	F_IO8
IO_L8P_T1L_N2_AD5P_66	A2	F_IOEXP_ALL_RST_N
IO_L8N_T1L_N3_AD5N_66	A1	F_IOEXP_VME_SCLK
IO_L9P_T1L_N4_AD12P_66	B3	F_IOEXP_VME_D
IO_L9N_T1L_N5_AD12N_66	A3	F_IOEXP_VME_RCLK
IO_L10P_T1U_N6_QBC_AD4P_66	B4	WR_CLK.PPS
IO_L10N_T1U_N7_QBC_AD4N_66	A4	WR_CLK.ABSCAL
IO_L11P_T1U_N8_GC_66	D4	FPGA-PL_CLKSYS_P
IO_L11N_T1U_N9_GC_66	C4	FPGA-PL_CLKSYS_N
IO_L12P_T1U_N10_GC_66	C3	WR_CLK.MAIN_P
IO_L12N_T1U_N11_GC_66	C2	WR_CLK.MAIN_N
IO_L13P_T2L_N0_GC_QBC_66	D7	WR_CLK.AUX_P
IO_L13N_T2L_N1_GC_QBC_66	D6	WR_CLK.AUX_N
IO_L14P_T2L_N2_GC_66	E5	WR_CLK.HELPER_N
IO_L14N_T2L_N3_GC_66	D5	WR_CLK.HELPER_P
IO_L15P_T2L_N4_AD11P_66	G6	F_IO26
IO_L15N_T2L_N5_AD11N_66	F6	F_IO5
IO_L16P_T2U_N6_QBC_AD3P_66	G8	F_IOEXP_GPIO_Q
IO_L16N_T2U_N7_QBC_AD3N_66	F7	F_IO4
IO_L17P_T2U_N8_AD10P_66	F8	F_WR_UART_RXD
IO_L17N_T2U_N9_AD10N_66	E8	USERIO_A.IO7
IO_L18P_T2U_N10_AD2P_66	E9	F_IO0
IO_L18N_T2U_N11_AD2N_66	D9	WRFLASH_I2C.SDA
IO_L19P_T3L_N0_DBC_AD9P_66	B5	F_IOEXP_FPIO_SCLK
IO_L19N_T3L_N1_DBC_AD9N_66	A5	F_IOEXP_FPIO_RCLK
IO_L20P_T3L_N2_AD1P_66	C6	F_IO3
IO_L20N_T3L_N3_AD1N_66	B6	F_IOEXP_FPIO_D
IO_L21P_T3L_N4_AD8P_66	A7	F_IOEXP_GPIO_SCLK
IO_L21N_T3L_N5_AD8N_66	A6	F_IOEXP_GPIO_RCLK
IO_L22P_T3U_N6_DBC_AD0P_66	C8	HP132
IO_L22N_T3U_N7_DBC_AD0N_66	B8	F_FP_LED1_DATA
IO_L23P_T3U_N8_66	A9	F_PP_LED0_DATA
IO_L23N_T3U_N9_66	A8	F_FP_LED0_DATA
IO_L24P_T3U_N10_66	C9	WRFLASH_I2C.SCL
IO_L24N_T3U_N11_66	B9	F_PP_LED1_DATA
IO_T0U_N12_VRP_66	G4	F_IO10
IO_T1U_N12_66	D2	F_IO10
IO_T2U_N12_66	E7	USERIO_A.IO17
IO_T3U_N12_66	C7	F_IOEXP_GPIO_D

G4 — 240 R21 — GND

USERIO_A.IO0 … USERIO_A.IO31 → F_IO0 … F_IO31

{IOEXP}

IC110
SN74LXCH8T245PWR
WR_UART_TXD
F_WR_UART_TXD
F_IOEXP_GPIO_Q
F_PERST_N
F_WRCLK_SPI_MISO
IOEXP.GPIO_Q
PCIE.PERST_N
WR_CLK.SPI_MISO
C487

IC107
SN74LXCH8T245PWR
F_WRCLK_SPI_SCK
F_WRCLK_SPI_MOSI
F_WR_DAC_SCLK
F_WR_DAC_DIN
F_WR_DAC_SYNC
F_SPI_HELPER_CS_N
F_SPI_MAIN_CS_N
WR_CLK.SPI_SCK
WR_CLK.SPI_MOSI
WR_DAC.SCLK
WR_DAC.DIN
WR_DAC.SYNC
WR_CLK.SPI_HELPER_CS_N
WR_CLK.SPI_MAIN_CS_N
C465
C464

IC108
SN74LXCH8T245PWR
WR_UART_RXD
F_WR_UART_RXD
F_IOEXP_ALL_OE_N
F_IOEXP_VME_RCLK
F_IOEXP_VME_SCLK
F_IOEXP_ALL_RST_N
F_IOEXP_VME_D
F_IOEXP_FPIO_RCLK
F_IOEXP_FPIO_SCLK
IOEXP.ALL_OE_N
IOEXP.VME_RCLK
IOEXP.VME_SCLK
IOEXP.ALL_RST_N
IOEXP.VME_D
IOEXP.FPIO_RCLK
IOEXP.FPIO_SCLK
C467
C466

IC109
SN74LXCH8T245PWR
F_IOEXP_FPIO_D
F_IOEXP_GPIO_RCLK
F_IOEXP_GPIO_SCLK
F_IOEXP_GPIO_D
F_FP_LED0_DATA
F_FP_LED1_DATA
F_PP_LED0_DATA
F_PP_LED1_DATA
IOEXP.FPIO_D
IOEXP.GPIO_RCLK
IOEXP.GPIO_SCLK
IOEXP.GPIO_D
C488
C489

IC141
SN74LXCH8T245PWR
F_IOEXP_HWBYTE1_D
F_IOEXP_HWBYTE2_D
F_IOEXP_HWBYTE1_RCLK
F_IOEXP_HWBYTE2_RCLK
IOEXP.HWBYTE1_D
IOEXP.HWBYTE2_D
IOEXP.HWBYTE1_RCLK
IOEXP.HWBYTE2_RCLK
R451 33
R453 33
R187 33
R188 33
FP_LED0_DATA
FP_LED1_DATA
PP_LED0_DATA
PP_LED1_DATA

Project: VME-WREN
FPGA HP Banks + level converters

Sheet: /fpga/fpga-hp-banks/
File: fpga-hp-banks.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A3 | Last Modified: –
KiCad E.D.A. 8.0.0
Rev: –
Id: 3/73

IC14A
XCZU4CG-1SFVC784E

BANK 43

IO_L1P_AD11P_43	AG10	VMEF.IRQ_IN_N7
IO_L1N_AD11N_43	AH10	VMEF.AS_N_OUT
IO_L2P_AD10P_43	AF11	VMEF.A7
IO_L2N_AD10N_43	AG11	VMEF.IACK_N_IN
IO_L3P_AD9P_43	AH12	VMEF.SYSCLK
IO_L3N_AD9N_43	AH11	VMEF.IACK_N_OUT
IO_L4P_AD8P_43	AE10	VMEF.A6
IO_L4N_AD8N_43	AF10	VMEF.A5
IO_L5P_HDGC_AD7P_43	AE12	VMEF.DS0_N_IN
IO_L5N_HDGC_AD7N_43	AF12	VMEF.DS0_N_OUT
IO_L6P_HDGC_AD6P_43	AC12	VMEF.IRQ_OUT_N6
IO_L6N_HDGC_AD6N_43	AD12	VMEF.A8
IO_L7P_HDGC_AD5P_43	AD11	VMEF.A15
IO_L7N_HDGC_AD5N_43	AD10	VMEF.A4
IO_L8P_HDGC_AD4P_43	AB11	VMEF.A11
IO_L8N_HDGC_AD4N_43	AC11	VMEF.IRQ_OUT_N5
IO_L9P_AD3P_43	AA11	VMEF.IRQ_IN_N5
IO_L9N_AD3N_43	AA10	VMEF.A1
IO_L10P_AD2P_43	W10	F_P0.RS485_DATA0
IO_L10N_AD2N_43	Y10	F_P0.RS485_DATA1
IO_L11P_AD1P_43	Y9	VMEF.A14
IO_L11N_AD1N_43	AA8	VMEF.LWORD_N
IO_L12P_AD0P_43	AB10	VMEF.A3
IO_L12N_AD0N_43	AB9	VMEF.A2

{VMEF} ◇{VMEF}

SFP0_SCL ◇SFP0_SCL
SFP0_SDA ◇SFP0_SDA

SFP1_SCL ◇SFP1_SCL
SFP1_SDA ◇SFP1_SDA

IC14B
XCZU4CG-1SFVC784E

BANK 44

IO_L1P_AD15P_44	AE15	VMEF.BERR_OUT
IO_L1N_AD15N_44	AE14	VMEF.A10
IO_L2P_AD14P_44	AG14	VMEF.AM4
IO_L2N_AD14N_44	AH14	VMEF.AS_N_IN
IO_L3P_AD13P_44	AG13	VMEF.DS1_N_IN
IO_L3N_AD13N_44	AH13	VMEF.IACK_OE_N
IO_L4P_AD12P_44	AE13	VMEF.A9
IO_L4N_AD12N_44	AF13	VMEF.DS1_N_OUT
IO_L5P_HDGC_44	AD15	VMEF.BERR_IN
IO_L5N_HDGC_44	AD14	VMEF.AM5
IO_L6P_HDGC_44	AC14	VMEF.AM3
IO_L6N_HDGC_44	AC13	VMEF.IRQ_OUT_N7
IO_L7P_HDGC_44	AA13	VMEF.IRQ_IN_N6
IO_L7N_HDGC_44	AB13	VMEF.A12
IO_L8P_HDGC_44	AB15	VMEF.RETRY_IN
IO_L8N_HDGC_44	AB14	VMEF.AM1
IO_L9P_AD11P_44	W14	VMEF.RETRY_OUT
IO_L9N_AD11N_44	W13	VMEF.SYSRESET_N
IO_L10P_AD10P_44	Y14	VMEF.AM0
IO_L10N_AD10N_44	Y13	VMEF.AM2
IO_L11P_AD9P_44	W12	VMEF.A16
IO_L11N_AD9N_44	W11	VMEF.IRQ_IN_N1
IO_L12P_AD8P_44	Y12	VMEF.A17
IO_L12N_AD8N_44	AA12	VMEF.A13

IC14C
XCZU4CG-1SFVC784E

BANK 45

IO_L1P_AD15P_45	J11	F_P0.BUNCHCLK1
IO_L1N_AD15N_45	J10	VMEF.IACKIN_N_IN
IO_L2P_AD14P_45	K13	VMEF.A27
IO_L2N_AD14N_45	K12	VMEF.A25
IO_L3P_AD13P_45	H11	VMEF.BR3
IO_L3N_AD13N_45	G10	VMEF.IACKOUT_N_OUT
IO_L4P_AD12P_45	J12	VMEF.A26
IO_L4N_AD12N_45	H12	F_P0.BUNCHCLK2
IO_L5P_HDGC_45	G11	VMEF.A24
IO_L5N_HDGC_45	F10	VMEF.IRQ_OUT_N4
IO_L6P_HDGC_45	F12	VMEF.AS_N_DIR
IO_L6N_HDGC_45	F11	VMEF.BERR_OE
IO_L7P_HDGC_45	E10	F_P0.TURNCLK2
IO_L7N_HDGC_45	D10	F_P0.TTC_DATA1
IO_L8P_HDGC_45	E12	VMEF.IRQ_OUT_N3
IO_L8N_HDGC_45	D11	F_P0.TTC_DATA0
IO_L9P_AD11P_45	C11	VMEF.RETRY_OE
IO_L9N_AD11N_45	B10	VMEF.WRITE_N_DIR
IO_L10P_AD10P_45	B11	VMEF.IRQ_OUT_N1
IO_L10N_AD10N_45	A10	F_SFP_LED_DATA
IO_L11P_AD9P_45	A12	VMEF.A21
IO_L11N_AD9N_45	A11	VMEF.WRITE_N
IO_L12P_AD8P_45	D12	VMEF.DS_N_OE
IO_L12N_AD8N_45	C12	SFP0_SCL

Layout note: all pins freely swappable.

R193 33
SFP_LED_DATA

{F_P0} ◇{F_P0}

F_P0.RS485_DATA0
F_P0.RS485_DATA1

F_P0.TURNCLK1
F_P0.TURNCLK2
F_P0.TTC_DATA0

F_P0.TTC_DATA1
F_P0.BUNCHCLK1
F_P0.BUNCHCLK2

IC14D
XCZU4CG-1SFVC784E

BANK 46

IO_L1P_AD11P_46	B15	SFP1_SDA
IO_L1N_AD11N_46	A15	SFP0_SDA
IO_L2P_AD10P_46	B14	VMEF.BG3IN
IO_L2N_AD10N_46	A14	VMEF.IRQ_OUT_N2
IO_L3P_AD9P_46	B13	VMEF.IRQ_IN_N2
IO_L3N_AD9N_46	A13	VMEF.A20
IO_L4P_AD8P_46	C14	VMEF.BG3OUT
IO_L4N_AD8N_46	C13	VMEF.A28
IO_L5P_HDGC_AD7P_46	D15	SFP1_SCL
IO_L5N_HDGC_AD7N_46	D14	VMEF.A29
IO_L6P_HDGC_AD6P_46	E14	VMEF.A30
IO_L6N_HDGC_AD6N_46	E13	VMEF.IRQ_IN_N4
IO_L7P_HDGC_AD5P_46	G13	VMEF.A23
IO_L7N_HDGC_AD5N_46	F13	F_P0.TURNCLK1
IO_L8P_HDGC_AD4P_46	F15	VMEF.DTACK_OE
IO_L8N_HDGC_AD4N_46	E15	VMEF.A_DIR
IO_L9P_AD3P_46	G15	VMEF.DTACK_N_IN
IO_L9N_AD3N_46	G14	VMEF.A31
IO_L10P_AD2P_46	H14	VMEF.DTACK_N_OUT
IO_L10N_AD2N_46	H13	VMEF.A22
IO_L11P_AD1P_46	K14	VMEF.A_OE_N
IO_L11N_AD1N_46	J14	VMEF.IRQ_IN_N3
IO_L12P_AD0P_46	L14	VMEF.A19
IO_L12N_AD0N_46	L13	VMEF.A18

Project: VME-WREN

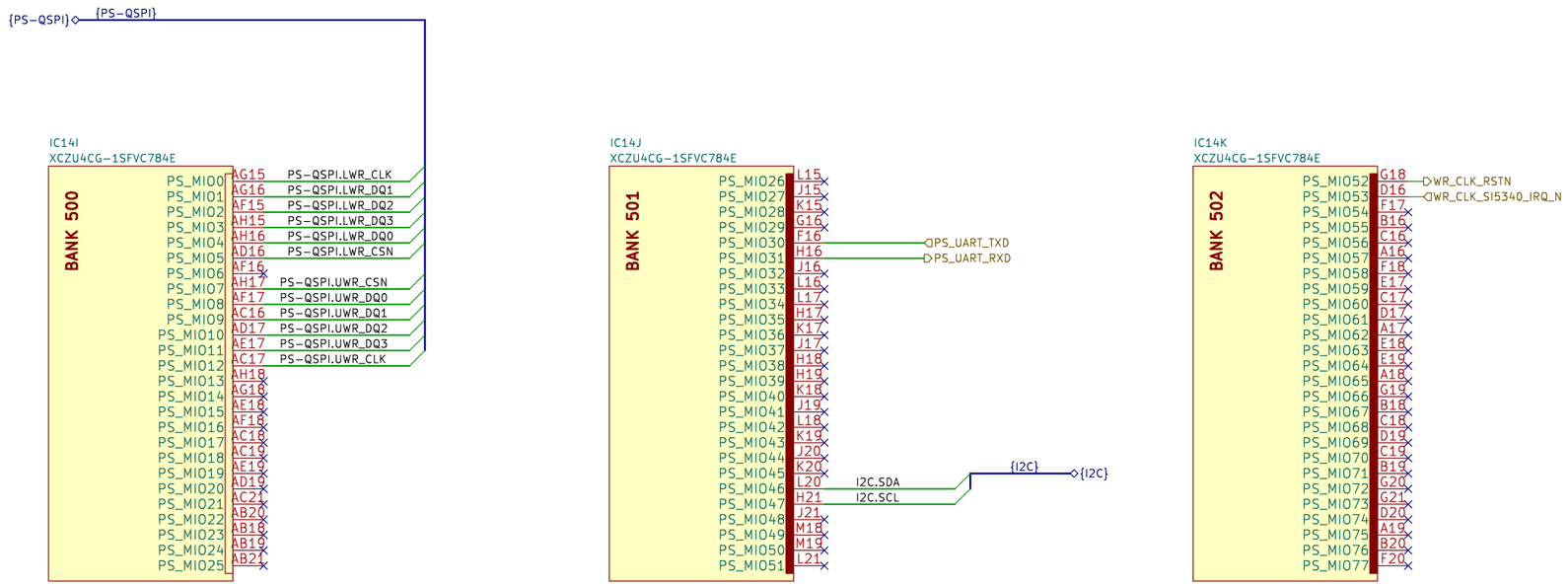
FPGA HD Banks

Sheet: /fpga/fpga-hd-banks/
File: fpga-hd-banks.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski | Group: BE-CEM

Size: A3 | Last Modified: - | **Rev:**

KiCad E.D.A. 8.0.0 | Id: 4/73



Project: VME-WREN

SoC MIO Banks

Sheet: /fpga/fpga-mio/ File: fpga-mio.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A3	Last Modified: –	**Rev: –**
KiCad E.D.A. 8.0.0		Id: 5/73

IC14L
XCZU4CG-1SFVC784E

BANK 505

PS_MGTRTXP0_505 E25
PS_MGTRTXN0_505 E26
PS_MGTRXP0_505 F27
PS_MGTRXN0_505 F28
PS_MGTREFCLK0P_505 F23
PS_MGTREFCLK0N_505 F24
PS_MGTRTXP1_505 D23
PS_MGTRTXN1_505 D24
PS_MGTRXP1_505 D27
PS_MGTRXN1_505 D28
PS_MGTREFCLK1P_505 E21
PS_MGTREFCLK1N_505 E22
PS_MGTRTXP2_505 C25
PS_MGTRTXN2_505 C26
PS_MGTRXP2_505 B27
PS_MGTRXN2_505 B28
PS_MGTREFCLK2P_505 C21
PS_MGTREFCLK2N_505 C22
PS_MGTRTXP3_505 B23
PS_MGTRTXN3_505 B24
PS_MGTRXP3_505 A25
PS_MGTRXN3_505 A26
PS_MGTREFCLK3P_505 A21
PS_MGTREFCLK3N_505 A22
PS_MGTRREF_505 F22

R11 500

GND

IC14H
XCZU4CG-1SFVC784E

BANK 224

MGTHTXP0_224 W4 SansDAC_BCLK_B1_P
MGTHTXN0_224 W3 SansDAC_BCLK_B1_N
MGTHRXP0_224 Y2
MGTHRXN0_224 Y1
MGTREFCLK0P_224 Y6 PCIE.REFCLK_P
MGTREFCLK0N_224 Y5 PCIE.REFCLK_N
MGTHTXP1_224 U4 SansDAC_BCLK_B2_P
MGTHTXN1_224 U3 SansDAC_BCLK_B2_N
MGTHRXP1_224 V2
MGTHRXN1_224 V1
MGTREFCLK1P_224 V6 WR_CLK.SFP_P
MGTREFCLK1N_224 V5 WR_CLK.SFP_N
MGTHTXP2_224 R4 SFP0.TX_P
MGTHTXN2_224 R3 SFP0.TX_N
MGTHRXP2_224 T2 SFP0.RX_P
MGTHRXN2_224 T1 SFP0.RX_N
MGTHTXP3_224 N4 SFP1.TX_P
MGTHTXN3_224 N3 SFP1.TX_N
MGTHRXP3_224 P2 SFP1.RX_P
MGTHRXN3_224 P1 SFP1.RX_N

{PCIE}
{PCIE}
PCIE.PET_P C230 SFP1.TX_P
PCIE.PET_N C233 SFP1.TX_N
PCIE.PER_P C374 SFP1.RX_P
PCIE.PER_N C375 SFP1.RX_N

Note: PCIE shares the transceiver with SFP1, place the caps next to the SFP cage to avoid stubs.

{WR_CLK}
{WR_CLK}
SFP0{SFP}
SFP0{SFP}
SFP1{SFP}
SFP1{SFP}

fpga-mgts-power
File: fpga-mgts-power.kicad_sch

IC121

SansDAC_BCLK_B1_P C477
SansDAC_BCLK_B1_N C476
IN+ 3
IN- 4
OUT1+ 11 IC121_O1_P C483 GTH_BCLK_B1_P
OUT1- 10 IC121_O1_N C481 GTH_BCLK_B1_N
OUT2+ 8 C484 BCLK_B1_DBG_P
OUT2- 9 C482 BCLK_B1_DBG_N
FILTA 1
FILTB 6
SD1 12
SD2 7
GND 5
EP 13
V+ 2
GND
P3V3
C274 1uF
C297
GND
GND

C480
C479

TR3
SEC 6 5 4
PRI 3 2 1
1:2
C485
J12 U.FL
GND
GND

Debug outputs for GTH-based SansDAC. Remove IC121/IC122 in production batches and bypass with caps.

IC122

SansDAC_BCLK_B2_P C468
SansDAC_BCLK_B2_N C469
IN+ 3
IN- 4
OUT1+ 11 IC122_O1_P C471 GTH_BCLK_B2_P
OUT1- 10 IC122_O1_N C470 GTH_BCLK_B2_N
OUT2+ 8 C473 BCLK_B2_DBG_P
OUT2- 9 C472 BCLK_B2_DBG_N
FILTA 1
FILTB 6
SD1 12
SD2 7
GND 5
EP 13
V+ 2
GND
P3V3
C490 1uF
C491
GND
GND

C475
C474

TR1
SEC 6 5 4
PRI 3 2 1
1:2
C478
J11 U.FL
GND
GND

Project: VME-WREN

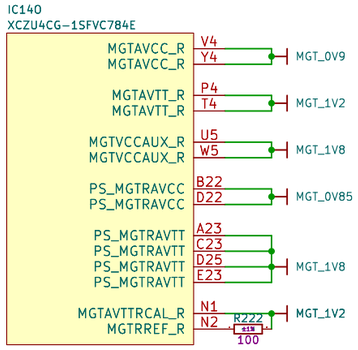
FPGA MGTs

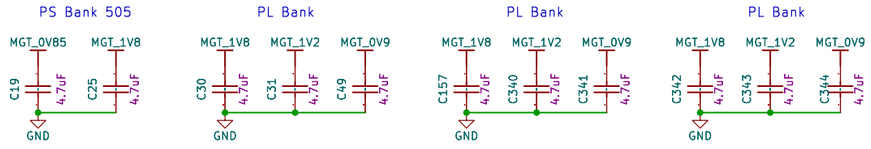
Sheet: /fpga/fpga-mgts/
File: fpga-mgts.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM

Size: A3
Last Modified: -
Rev: -

KiCad E.D.A. 8.0.0
Id: 6/73





MGTAVTTRCAL
Connect to MGTAVTT and to a 100 Ω resistor that is also connected to MGTRREF.
Use identical trace geometry for the connection between the resistor and this pin and for the connection from the other pin of the resistor to MGTRREF.
Also, limit the DC resistance of each trace to less than 0.5Ω.

Project: VME-WREN

FPGA MGT Power

Sheet: /fpga/fpga-mgts/fpga-mgts-power/
File: fpga-mgts-power.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

Size: A3 — Last Modified: — — **Rev: —**

KiCad E.D.A. 8.0.0 — Id: 7/73

According to UG1075:
* DQ byte lane swapping is allowed. A byte lane includes any signals associated with the
aligned 8-bits of DQ, such as DM, DQS, DQS_N, and DQ signals.
* DQ bits swapping within a byte lane is allowed if write CRC is not used

{DDR4-PS}

{DDR4-PS}

IC14M
XCZU4CG-1SFVC784E

DDR4-PS.DQ1	AD21	PS_DDR_DQ0	PS_DDR_A0	W28	DDR4-PS.A0
DDR4-PS.DQ5	AE20	PS_DDR_DQ1	PS_DDR_A1	Y28	DDR4-PS.A1
DDR4-PS.DQ2	AD20	PS_DDR_DQ2	PS_DDR_A2	AB28	DDR4-PS.A2
DDR4-PS.DQ3	AF20	PS_DDR_DQ3	PS_DDR_A3	AA28	DDR4-PS.A3
DDR4-PS.DQ0	AH21	PS_DDR_DQ4	PS_DDR_A4	Y27	DDR4-PS.A4
DDR4-PS.DQ4	AH20	PS_DDR_DQ5	PS_DDR_A5	AA27	DDR4-PS.A5
DDR4-PS.DQ6	AH19	PS_DDR_DQ6	PS_DDR_A6	Y22	DDR4-PS.A6
DDR4-PS.DQ7	AG19	PS_DDR_DQ7	PS_DDR_A7	AA23	DDR4-PS.A7
DDR4-PS.DQ10	AF22	PS_DDR_DQ8	PS_DDR_A8	AA22	DDR4-PS.A8
DDR4-PS.DQ12	AH22	PS_DDR_DQ9	PS_DDR_A9	AB23	DDR4-PS.A9
DDR4-PS.DQ14	AE22	PS_DDR_DQ10	PS_DDR_A10	AA25	DDR4-PS.A10
DDR4-PS.DQ15	AD22	PS_DDR_DQ11	PS_DDR_A11	AA26	DDR4-PS.A11
DDR4-PS.DQ11	AH23	PS_DDR_DQ12	PS_DDR_A12	AB25	DDR4-PS.A12
DDR4-PS.DQ13	AH24	PS_DDR_DQ13	PS_DDR_A13	AB26	DDR4-PS.A13
DDR4-PS.DQ9	AE24	PS_DDR_DQ14	PS_DDR_A14	AB24	DDR4-PS.WEN
DDR4-PS.DQ8	AG24	PS_DDR_DQ15	PS_DDR_A15	AC24	DDR4-PS.CASN
DDR4-PS.DQ19	AC26	PS_DDR_DQ16	PS_DDR_A16	AC23	DDR4-PS.RASN
DDR4-PS.DQ21	AD26	PS_DDR_DQ17	PS_DDR_A17	AC22	
DDR4-PS.DQ23	AD25	PS_DDR_DQ18			
DDR4-PS.DQ17	AD24	PS_DDR_DQ19	PS_DDR_DM0	AG20	DDR4-PS.DM0
DDR4-PS.DQ18	AG26	PS_DDR_DQ20	PS_DDR_DM1	AE23	DDR4-PS.DM1
DDR4-PS.DQ20	AH25	PS_DDR_DQ21	PS_DDR_DM2	AE25	DDR4-PS.DM2
DDR4-PS.DQ16	AH26	PS_DDR_DQ22	PS_DDR_DM3	AE28	DDR4-PS.DM3
DDR4-PS.DQ22	AG25	PS_DDR_DQ23	PS_DDR_DM4	R23	
DDR4-PS.DQ31	AH27	PS_DDR_DQ24	PS_DDR_DM5	H23	
DDR4-PS.DQ30	AH28	PS_DDR_DQ25	PS_DDR_DM6	L27	
DDR4-PS.DQ29	AF28	PS_DDR_DQ26	PS_DDR_DM7	H26	
DDR4-PS.DQ28	AG28	PS_DDR_DQ27	PS_DDR_DM8	T26	
DDR4-PS.DQ27	AC27	PS_DDR_DQ28			
DDR4-PS.DQ26	AD27	PS_DDR_DQ29			
DDR4-PS.DQ24	AD28	PS_DDR_DQ30	PS_DDR_ACT_N	Y23	DDR4-PS.ACTN
DDR4-PS.DQ25	AC28	PS_DDR_DQ31	PS_DDR_ALERT_N	U25	DDR4-PS.ALERTN
	T22	PS_DDR_DQ32	PS_DDR_PARITY	V24	DDR4-PS.PAR
	R22	PS_DDR_DQ33	PS_DDR_RAM_RST_N	U23	DDR4-PS.RSTN
	P22	PS_DDR_DQ34	PS_DDR_ZQ	U24	240 ±1% R1 GND
	N22	PS_DDR_DQ35			
	T23	PS_DDR_DQ36			
	P24	PS_DDR_DQ37	PS_DDR_DQS_P0	AF21	DDR4-PS.DQS_P0
	R24	PS_DDR_DQ38	PS_DDR_DQS_N0	AG21	DDR4-PS.DQS_N0
	N24	PS_DDR_DQ39	PS_DDR_DQS_P1	AF23	DDR4-PS.DQS_P1
	H24	PS_DDR_DQ40	PS_DDR_DQS_N1	AG23	DDR4-PS.DQS_N1
	J24	PS_DDR_DQ41	PS_DDR_DQS_P2	AF25	DDR4-PS.DQS_P2
	M24	PS_DDR_DQ42	PS_DDR_DQS_N2	AF26	DDR4-PS.DQS_N2
	K24	PS_DDR_DQ43	PS_DDR_DQS_P3	AE27	DDR4-PS.DQS_P3
	J22	PS_DDR_DQ44	PS_DDR_DQS_N3	AF27	DDR4-PS.DQS_N3
	H22	PS_DDR_DQ45	PS_DDR_DQS_P4	N23	
	K22	PS_DDR_DQ46	PS_DDR_DQS_N4	M23	
	L22	PS_DDR_DQ47	PS_DDR_DQS_P5	L23	
	M25	PS_DDR_DQ48	PS_DDR_DQS_N5	K23	
	M26	PS_DDR_DQ49	PS_DDR_DQS_P6	N26	
	L25	PS_DDR_DQ50	PS_DDR_DQS_N6	N27	
	L26	PS_DDR_DQ51	PS_DDR_DQS_P7	J26	
	K28	PS_DDR_DQ52	PS_DDR_DQS_N7	J27	
	L28	PS_DDR_DQ53	PS_DDR_DQS_P8	R27	
	M28	PS_DDR_DQ54	PS_DDR_DQS_N8	T27	
	N28	PS_DDR_DQ55			
	J28	PS_DDR_DQ56			
	K27	PS_DDR_DQ57	PS_DDR_BA0	V23	DDR4-PS.BA0
	H28	PS_DDR_DQ58	PS_DDR_BG0	W24	DDR4-PS.BG0
	H27	PS_DDR_DQ59	PS_DDR_CK0	W25	DDR4-PS.CK_P
	G26	PS_DDR_DQ60	PS_DDR_CKE0	V28	DDR4-PS.CKE
	G25	PS_DDR_DQ61	PS_DDR_CK_N0	W26	DDR4-PS.CK_N
	K25	PS_DDR_DQ62	PS_DDR_CS_N0	W27	DDR4-PS.CSN
	J25	PS_DDR_DQ63	PS_DDR_ODT0	U28	DDR4-PS.ODT
	T28	PS_DDR_DQ64			
	R28	PS_DDR_DQ65	PS_DDR_BA1	W22	DDR4-PS.BA1
	P28	PS_DDR_DQ66	PS_DDR_BG1	V22	
	P27	PS_DDR_DQ67	PS_DDR_CK1	Y24	
	P26	PS_DDR_DQ68	PS_DDR_CKE1	V27	
	R25	PS_DDR_DQ69	PS_DDR_CK_N1	Y25	
	P25	PS_DDR_DQ70	PS_DDR_CS_N1	V26	
	T25	PS_DDR_DQ71	PS_DDR_ODT1	U26	

Project: VME-WREN

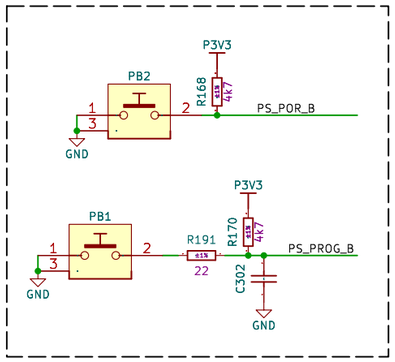
SoC PS DDR4

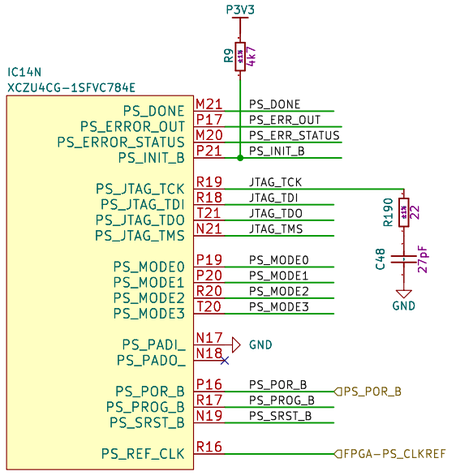
Sheet: /fpga/fpga-ps-ddr/
File: fpga-ps-ddr.kicad_sch

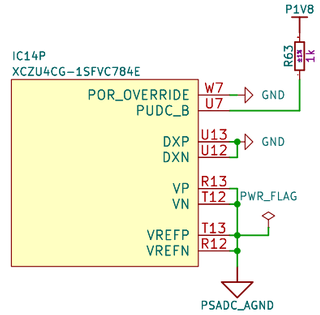
Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

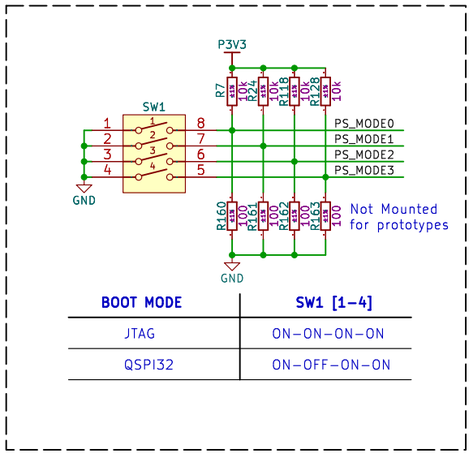
Size: A3 — Last Modified: — — **Rev: —**

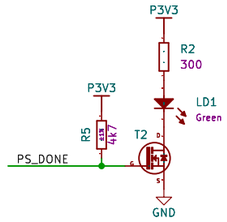
KiCad E.D.A. 8.0.0 — Id: 8/73

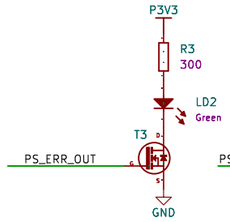


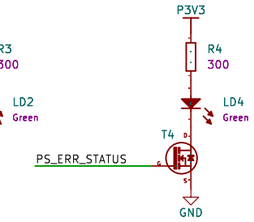


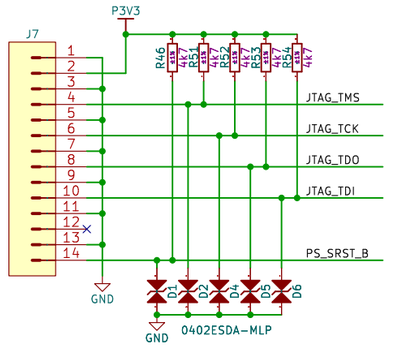












Project: VME-WREN

FPGA Configuration

Sheet: /fpga/fpga-config/
File: fpga-config.kicad_sch

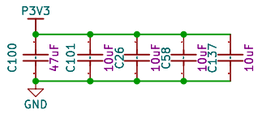
Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

Size: A3 — Last Modified: – — **Rev: –**

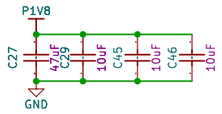
KiCad E.D.A. 8.0.0 — Id: 9/73

Recommended capacitors given in UG583 p26 and checklist xtp427

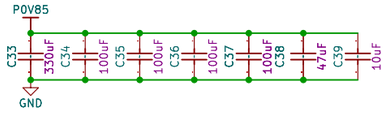
VCCO_43-44



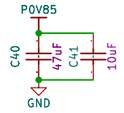
VCCO_64-65-66



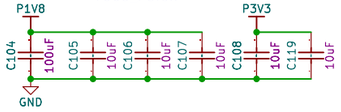
VCCINT/VCCINT_IO



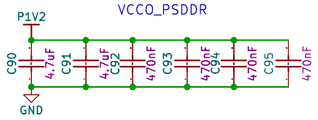
VCCBRAM/VCCINT_IO



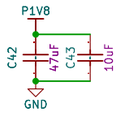
VCCO_PSIOx



VCCO_PSDDR

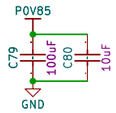


VCCAUX/VCCAUX_IO

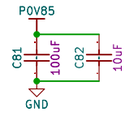


VCC_PSAUX

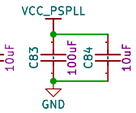
VCC_PSINTFP



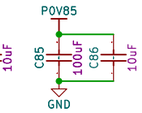
VCC_PSINTLP

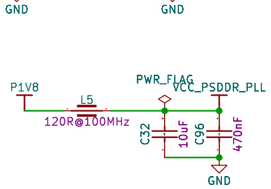


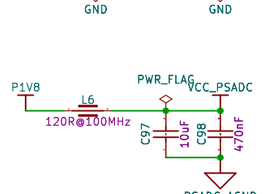
VCC_PSPLL



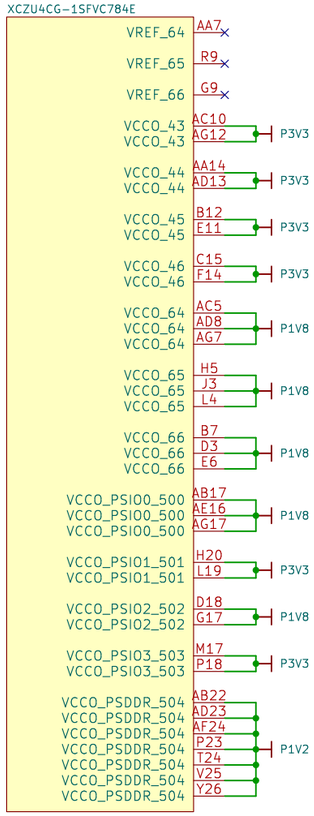
VCC_PSINTFP_DDR



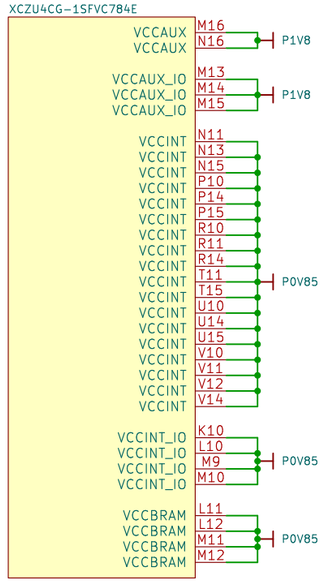




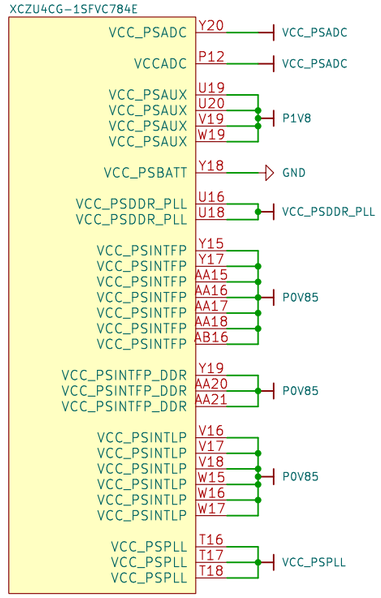
IC14Q
XCZU4CG-1SFVC784E



IC14R
XCZU4CG-1SFVC784E



IC14S
XCZU4CG-1SFVC784E



fpga-power-gnd
File: fpga-power-gnd.kicad_sch

Project: VME-WREN

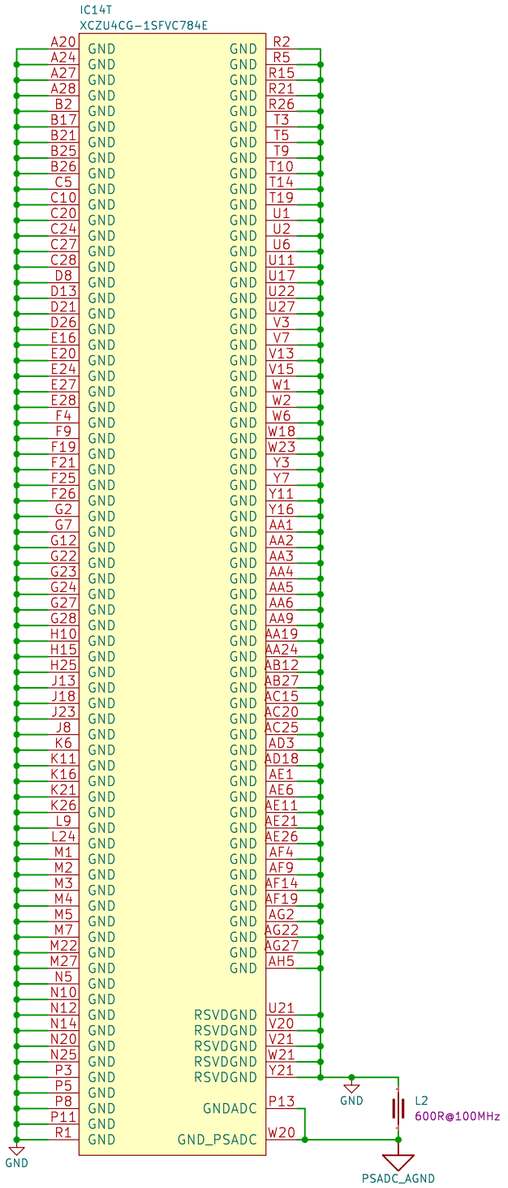
FPGA Power Pins

Sheet: /fpga/fpga-power/
File: fpga-power.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski | Group: BE-CEM

Size: A3 | Last Modified: - | **Rev: -**

KiCad E.D.A. 8.0.0 | Id: 10/73



Project: VME-WREN

FPGA GND Pins

Sheet: /fpga/fpga-power/fpga-power-gnd/	
File: fpga-power-gnd.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A3 — Last Modified: –	**Rev: –**
KiCad E.D.A. 8.0.0	Id: 11/73

All outputs LVDS

PWR_FLAG

P3V3 — L7 50R@100MHz — C117 220uF — C116 47uF — GND

OSC4 10MHz: VDD, OUT, VCO, GND; PLLDAC_OUT1; R199 523; R200 442; C162; GND

C59 — C65 — GND

IC60 SI5340B-D-GM

IN0	OUT0	WR_CLK_SFP_AC_P	C265 10nF WR_CLK.SFP_P
IN0	OUT0	WR_CLK_SFP_AC_N	C266 10nF WR_CLK.SFP_N
IN1	OUT1		WR_CLK.MAIN_P
IN1	OUT1		WR_CLK.MAIN_N
IN2	OUT2		FPGA-PL_CLKSYS_N → FPGA-PL_CLKSYS_N
IN2	OUT2		FPGA-PL_CLKSYS_P → FPGA-PL_CLKSYS_P
FB_IN	OUT3		WR_CLK.AUX_P
FB_IN	OUT3		WR_CLK.AUX_N
X1	LOL		
XA	LOS_XAXB		
XB	INTR		WR_CLK.SI5340_IRQ_N
X2			
SDA/SDIO		WR_CLK.SPI_MOSI	
SCLK		WR_CLK.SPI_SCK	
A1/SDO		WR_CLK.SPI_MISO	
A0/CS		WR_CLK.SPI_MAIN_CS_N	
I2C_SEL		GND	
OE			
IN_SEL0		P3V3_CLK	
IN_SEL1			
RST		WR_CLK.RSTN	
VDD	VDDO0	P1V8	P3V3_CLK
VDD	VDDO1		
VDD	VDDO2		
VDD	VDDO3		
VDDA	NC	P3V3_CLK	
VDDA			
VDDS	GND	GND	GND

{WR_CLK} → WR_CLK.SFP_P, WR_CLK.SFP_N, WR_CLK.MAIN_P, WR_CLK.MAIN_N, WR_CLK.HELPER_P, WR_CLK.HELPER_N, WR_CLK.SI5340_IRQ_N, WR_CLK.PPS, WR_CLK.ABSCAL, WR_CLK.RSTN, WR_CLK.AUX_P, WR_CLK.AUX_N, WR_CLK.SPI_MOSI, WR_CLK.SPI_MISO, WR_CLK.SPI_HELPER_CS_N, WR_CLK.SPI_MAIN_CS_N, WR_CLK.SPI_SCK

P3V3 — L13 220R@100MHz — L14 220R@100MHz — PWR_FLAG — P3V3_CLK — C15 22uF — C16 22uF — C17 22uF — C18 22uF — GND

P1V8 — C123 1uF — C129 1uF — C263 1uF — GND

P3V3_CLK — C121 1uF — C122 1uF — C255 1uF — C256 1uF — C257 1uF — C258 1uF — C259 1uF — C264 1uF — GND

WR_CLK.MAIN_P — C246 — TRAFO1_P
WR_CLK.MAIN_N — C248 — TRAFO1_N
TR2 (SEC, PRI) 1:2 — C247 — J9 U.FL — GND

DAC REQUIRES LEVEL TRANSLATOR!

WR DAC bypass

R66 No 0 — R86 No 0 — R57 240 — C75 — PLLDAC_OUT2 — GND
R58 240 — C76 — PLLDAC_OUT1 — GND

IC10 DAC8562SDSC

DIN	VOUTB		PLLDAC_OUT2
SCLK	VOUTA		PLLDAC_OUT1
SYNC	VREF		
LDAC	GND		GND
CLR	EP		GND
AVDD		P3V3_CLK	C260 100pF, C218

WR_DAC.DIN, WR_DAC.SCLK, WR_DAC.SYNC

R94 0 No — Optional external VREF

IC12: IN, NC, TEMP, GND, OUT, NC, NC, TRIM — P3V3_CLK — C77 4.7uF — C78 4.7uF — GND

{WR_DAC} → WR_DAC.SCLK, WR_DAC.DIN, WR_DAC.SYNC

7-bit I2C address: 0x75

Compatible with 20MHz LFVCXO026156

OSC3 25MHz KV7050B25.0000C3GD00: VCC, VC, INH, OUT, NC, GND — P3V3_CLK — PLLDAC_OUT2 — C267 — GND

Helper PLL bypass

WR_CLK.25M_HELPER — R65 0 — R201 523 — R202 442 — C165 — C353 — C66 — GND

IC18 SI5340B-D-GM

IN0	OUT0		WR_CLK.HELPER_N
IN0	OUT0		WR_CLK.HELPER_P → LVDS
IN1	OUT1		
IN1	OUT1		
IN2	OUT2		
IN2	OUT2		
FB_IN	OUT3		
FB_IN	OUT3		
X1	LOL		
XA	LOS_XAXB		
XB	INTR		
X2			
SDA/SDIO		WR_CLK.SPI_MOSI	
SCLK		WR_CLK.SPI_SCK	
A1/SDO		WR_CLK.SPI_MISO	
A0/CS		WR_CLK.SPI_HELPER_CS_N	
I2C_SEL		GND	
OE			
IN_SEL0		P3V3_CLK	
IN_SEL1			
RST		WR_CLK.RSTN	
VDD	VDDO0	P1V8	P3V3_CLK
VDD	VDDO1		
VDD	VDDO2		
VDD	VDDO3		
VDDA	NC	P3V3_CLK	
VDDA			
VDDS	GND	GND	GND

P1V8 — C115 1uF — C149 1uF — C151 1uF — C152 1uF — GND
P3V3_CLK — C68 1uF — C69 1uF — C261 1uF — C262 1uF — GND

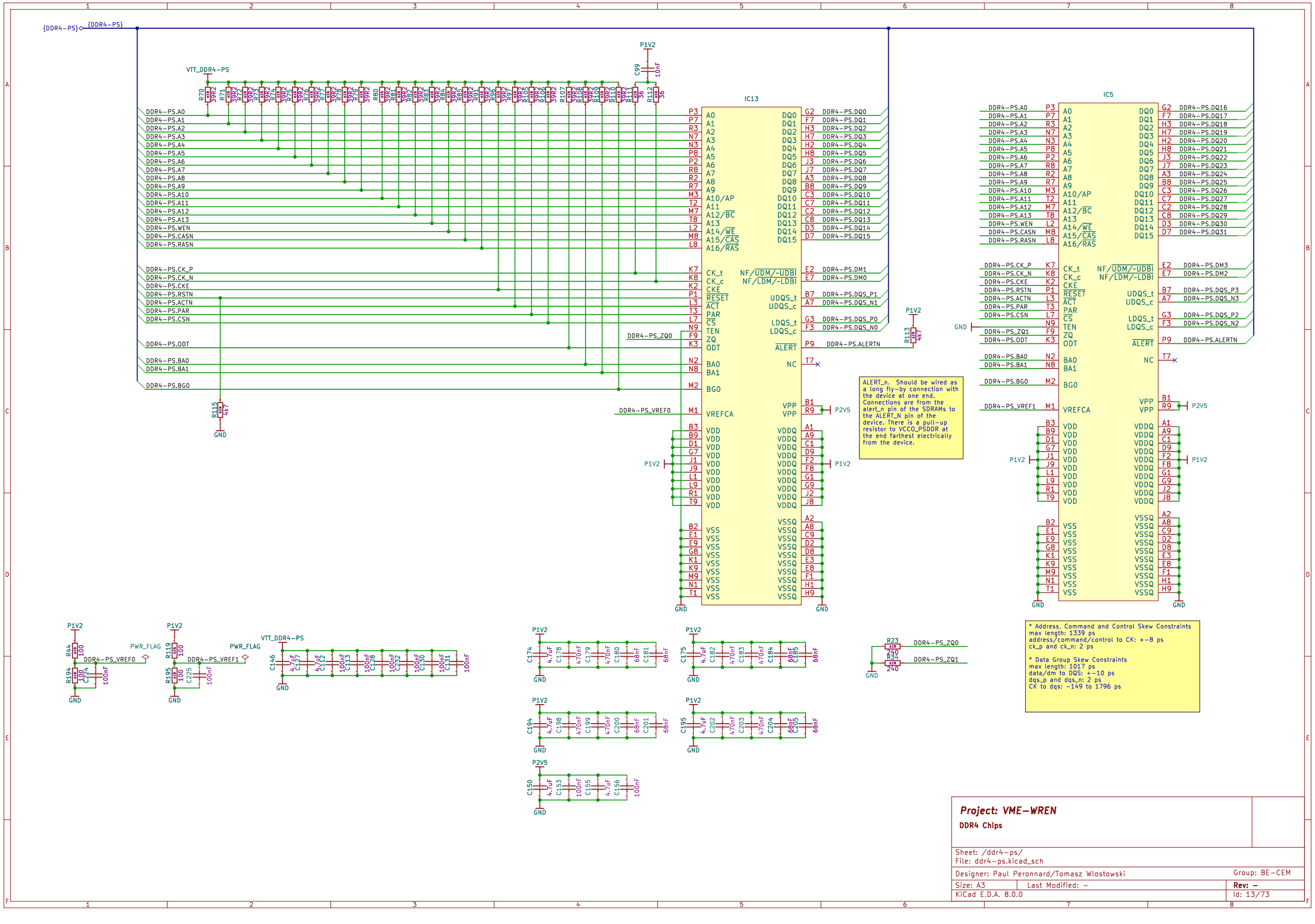
7-bit I2C address: 0x74

P3V3 — OSC1 50MHz: VCC, OUT, OE, GND — C118 — R27 22 — FPGA-PS_CLKREF — GND

P3V3 — IC20A — WR_CLK.PPS — R38 4R7 — J8 U.FL — GND
P3V3 — IC20B — WR_CLK.ABSCAL — R39 4R7 — J4 U.FL — GND
P3V3 — C268 — GND

Project: VME-WREN
Clock Generation

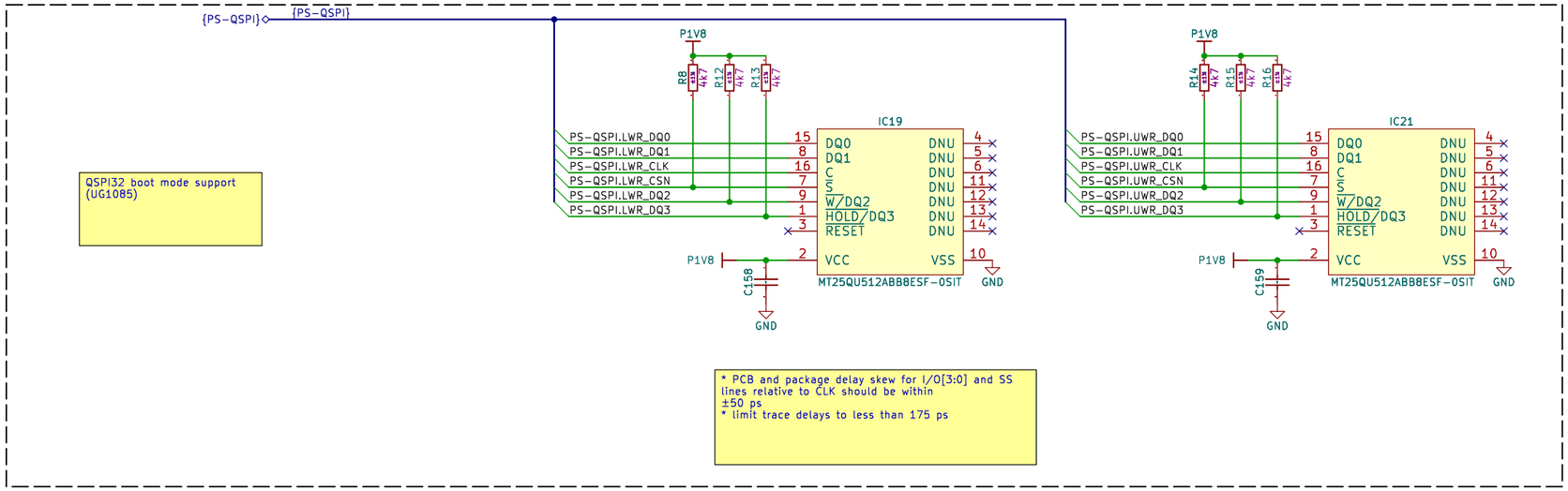
Sheet: /clocks/	
File: clocks.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A3 — Last Modified: –	Rev: –
KiCad E.D.A. 8.0.0	Id: 12/73

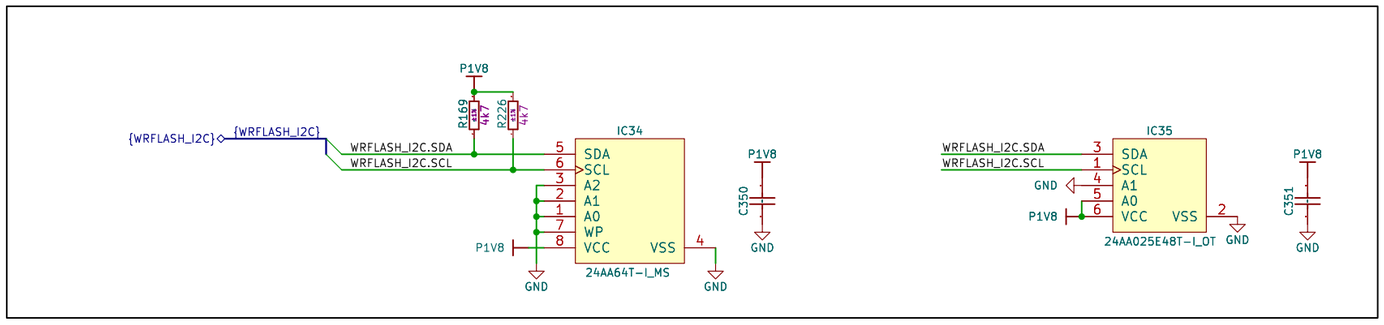


Project: VME-WREN

DDR4 Chips

Sheet: /ddr4-ps/	
File: ddr4-ps.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A3 — Last Modified: -	**Rev: -**
KiCad E.D.A. 8.0.0	Id: 13/73





Project: VME-WREN

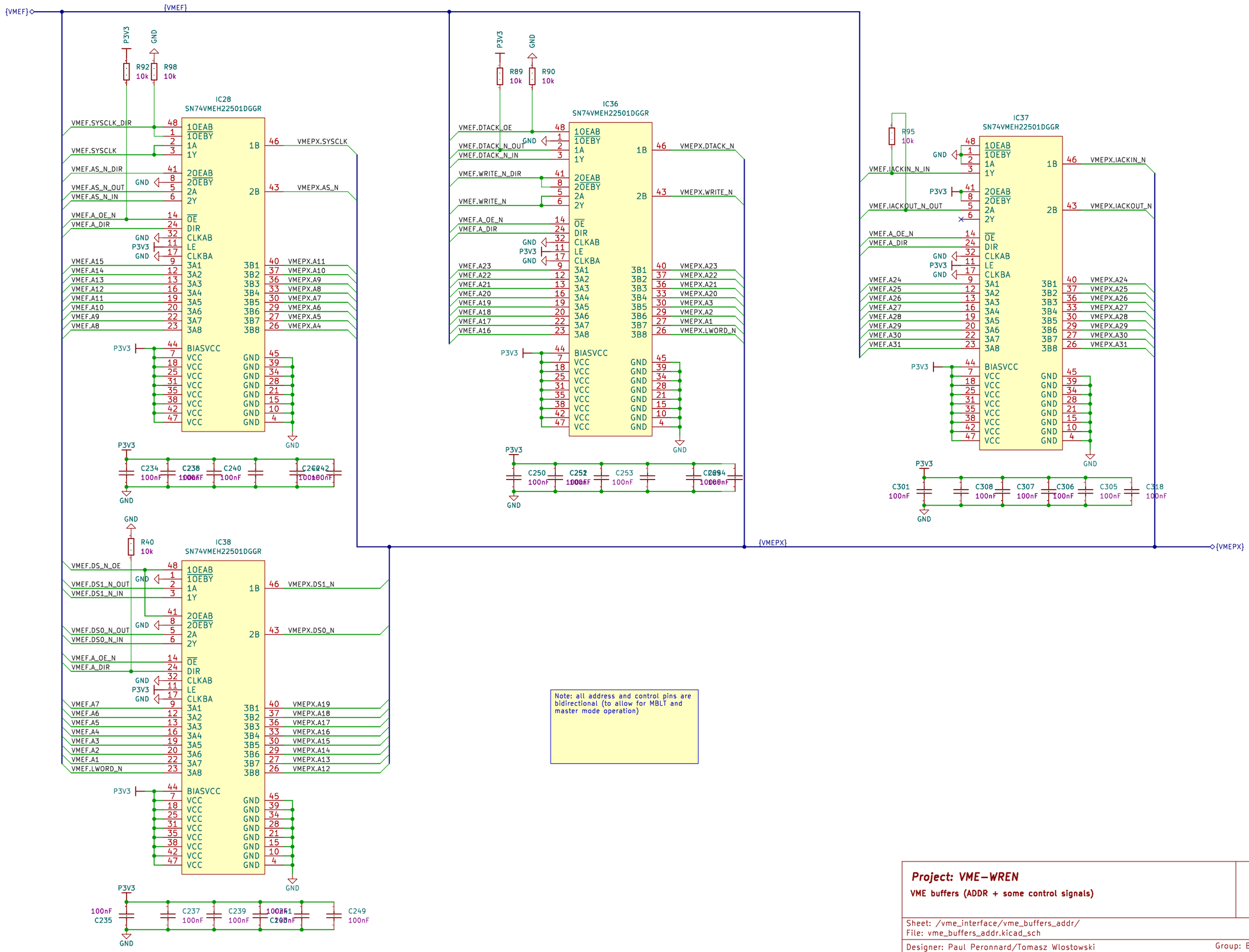
NV Memories

Sheet: /flash/
File: flash.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

Size: A3 — Last Modified: – — **Rev: –**

KiCad E.D.A. 8.0.0 — Id: 14/73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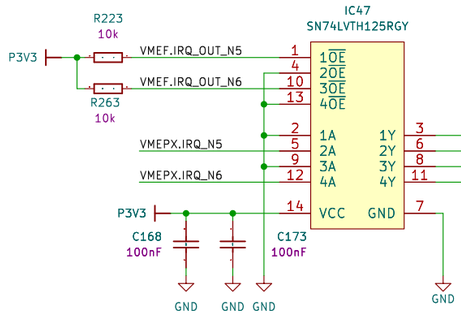
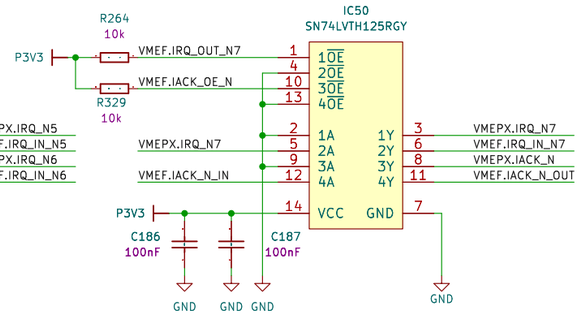
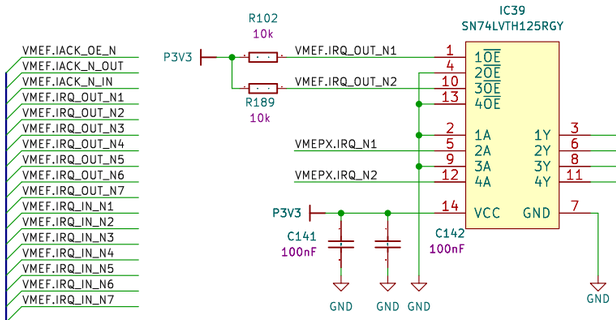
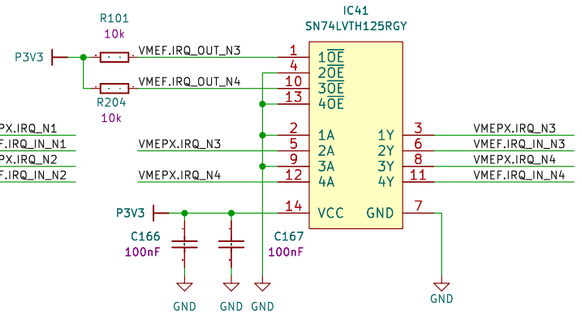
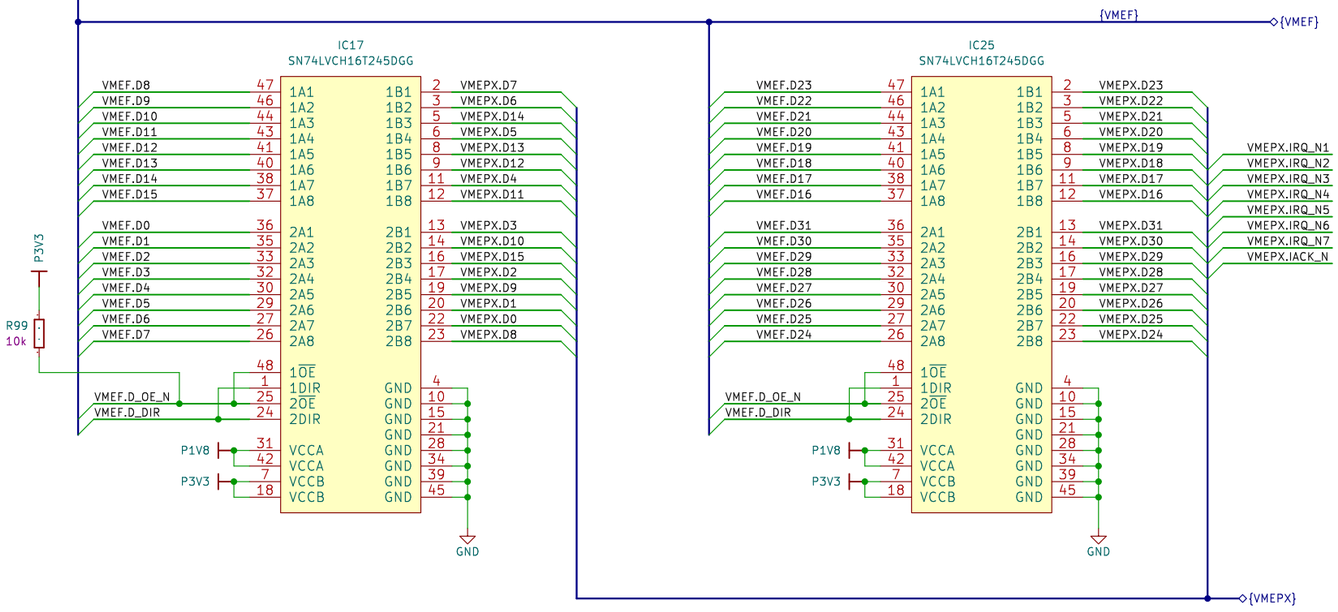
{VMEF}
P3V3
GND
R92
10k
R98
10k
IC28
SN74VMEH22501DGGR
VMEF.SYSCLK_DIR
VMEF.SYSCLK
VMEF.AS_N_DIR
VMEF.AS_N_OUT
VMEF.AS_N_IN
VMEF.A_OE_N
VMEF.A_DIR
VMEF.A15
VMEF.A14
VMEF.A13
VMEF.A12
VMEF.A11
VMEF.A10
VMEF.A9
VMEF.A8
VMEPX.SYSCLK
VMEPX.AS_N
VMEPX.A11
VMEPX.A10
VMEPX.A9
VMEPX.A8
VMEPX.A7
VMEPX.A6
VMEPX.A5
VMEPX.A4
C234
C238
C240
C242
100nF
R89
10k
R90
10k
IC36
SN74VMEH22501DGGR
VMEF.DTACK_OE
VMEF.DTACK_N_OUT
VMEF.DTACK_N_IN
VMEF.WRITE_N_DIR
VMEF.WRITE_N
VMEF.A_OE_N
VMEF.A_DIR
VMEF.A23
VMEF.A22
VMEF.A21
VMEF.A20
VMEF.A19
VMEF.A18
VMEF.A17
VMEF.A16
VMEPX.DTACK_N
VMEPX.WRITE_N
VMEPX.A23
VMEPX.A22
VMEPX.A21
VMEPX.A20
VMEPX.A3
VMEPX.A2
VMEPX.A1
VMEPX.LWORD_N
C250
C252
C253
C254
100nF
R95
10k
IC37
SN74VMEH22501DGGR
VMEF.IACKIN_N_IN
VMEF.IACKOUT_N_OUT
VMEF.A_OE_N
VMEF.A_DIR
VMEF.A24
VMEF.A25
VMEF.A26
VMEF.A27
VMEF.A28
VMEF.A29
VMEF.A30
VMEF.A31
VMEPX.IACKIN_N
VMEPX.IACKOUT_N
VMEPX.A24
VMEPX.A25
VMEPX.A26
VMEPX.A27
VMEPX.A28
VMEPX.A29
VMEPX.A30
VMEPX.A31
C301
C308
C307
C306
C305
C318
100nF
R40
10k
IC38
SN74VMEH22501DGGR
VMEF.DS_N_OE
VMEF.DS1_N_OUT
VMEF.DS1_N_IN
VMEF.DS0_N_OUT
VMEF.DS0_N_IN
VMEF.A_OE_N
VMEF.A_DIR
VMEF.A7
VMEF.A6
VMEF.A5
VMEF.A4
VMEF.A3
VMEF.A2
VMEF.A1
VMEF.LWORD_N
VMEPX.DS1_N
VMEPX.DS0_N
VMEPX.A19
VMEPX.A18
VMEPX.A17
VMEPX.A16
VMEPX.A15
VMEPX.A14
VMEPX.A13
VMEPX.A12
C235
C237
C239
C241
C249
100nF
{VMEPX}
{VMEPX}
Note: all address and control pins are bidirectional (to allow for MBLT and master mode operation)
Project: VME–WREN
VME buffers (ADDR + some control signals)
Sheet: /vme_interface/vme_buffers_addr/
File: vme_buffers_addr.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE–CEM
Size: A3
Last Modified: –
KiCad E.D.A. 8.0.0
Rev:
Id: 15/73

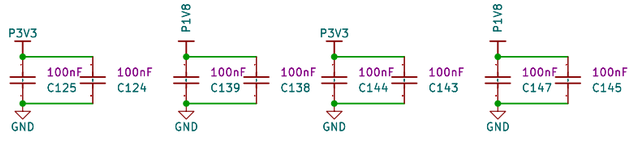












Note: all IRQ pins are bidirectional (to allow master mode operation)

Project: VME–WREN

VME buffers (DATA + IRQs)

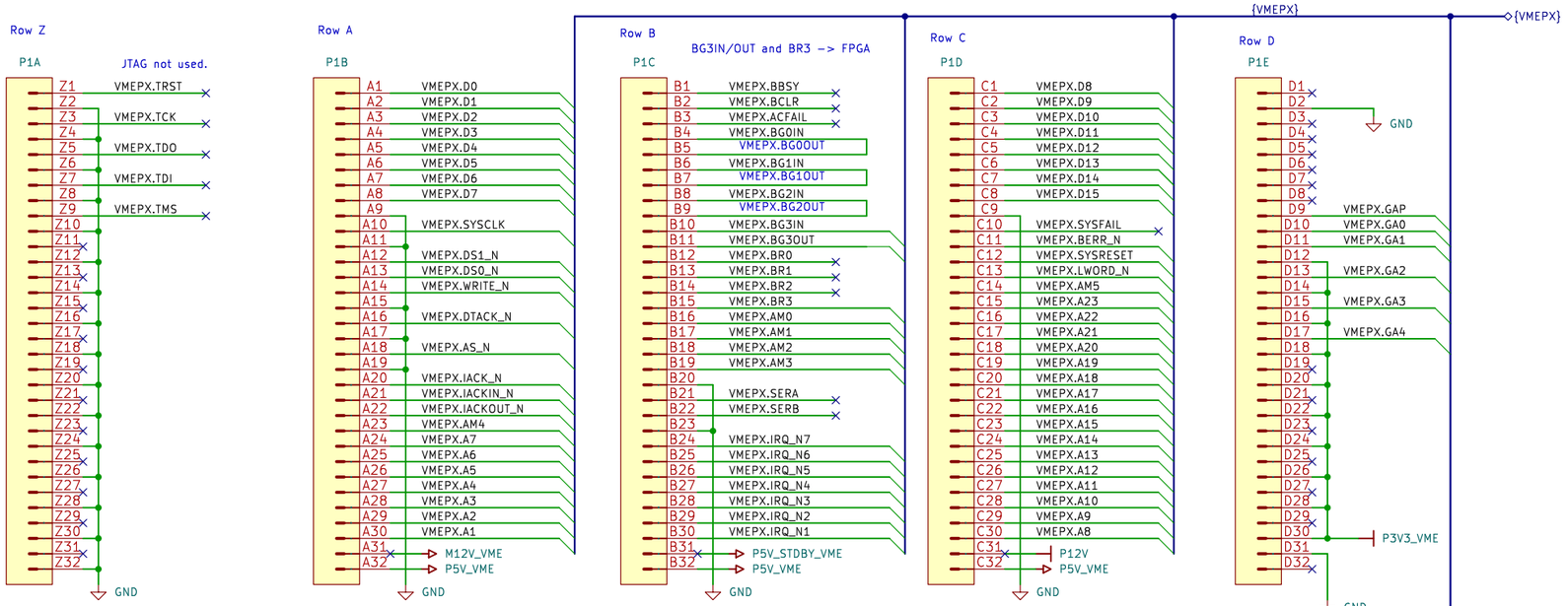
Sheet: /vme_interface/vme_buffers_data/
File: vme_buffers_data.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE–CEM

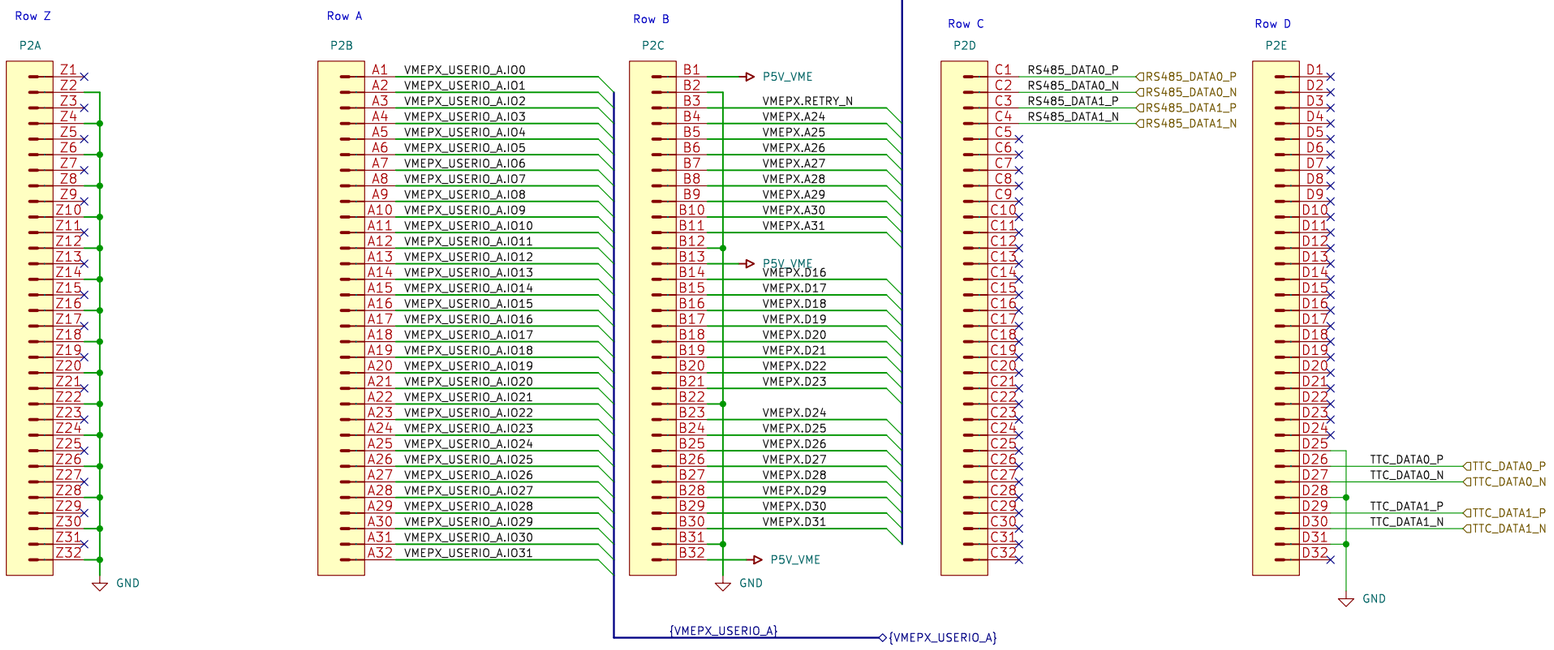
Size: A3 — Last Modified: – — **Rev:**

KiCad E.D.A. 8.0.0 — Id: 16/73

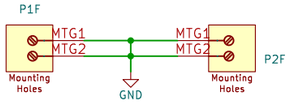
VME P1



VME P2



Front panel mounting holes



Fixing for P1 & P2

Project: VME-WREN

VME P1/P2 connector fanout + mechanics

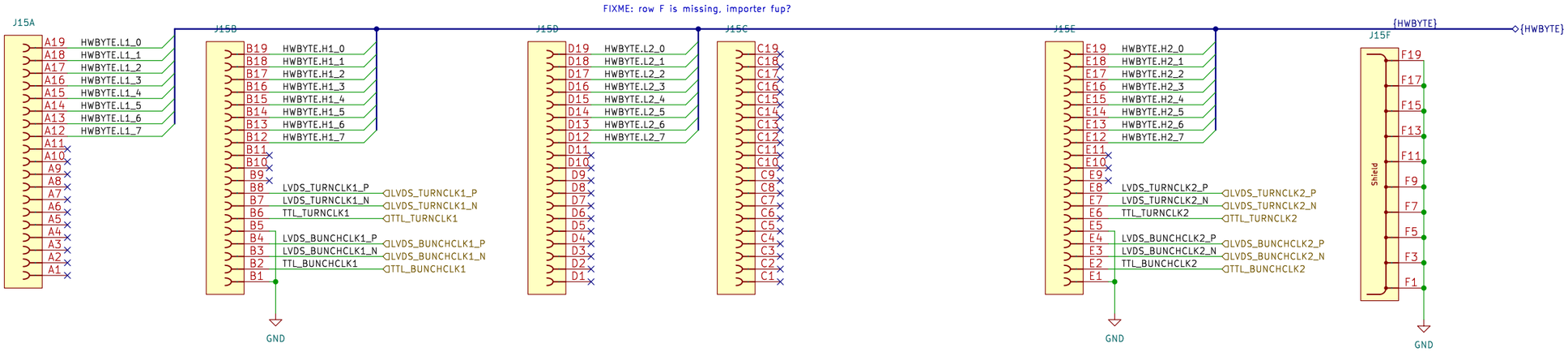
Sheet: /vme_interface/vme_p1_p2/
File: vme_p1_p2.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski | Group: BE-CEM

Size: A3 | Last Modified: - | **Rev:**

KiCad E.D.A. 8.0.0 | Id: 17/73

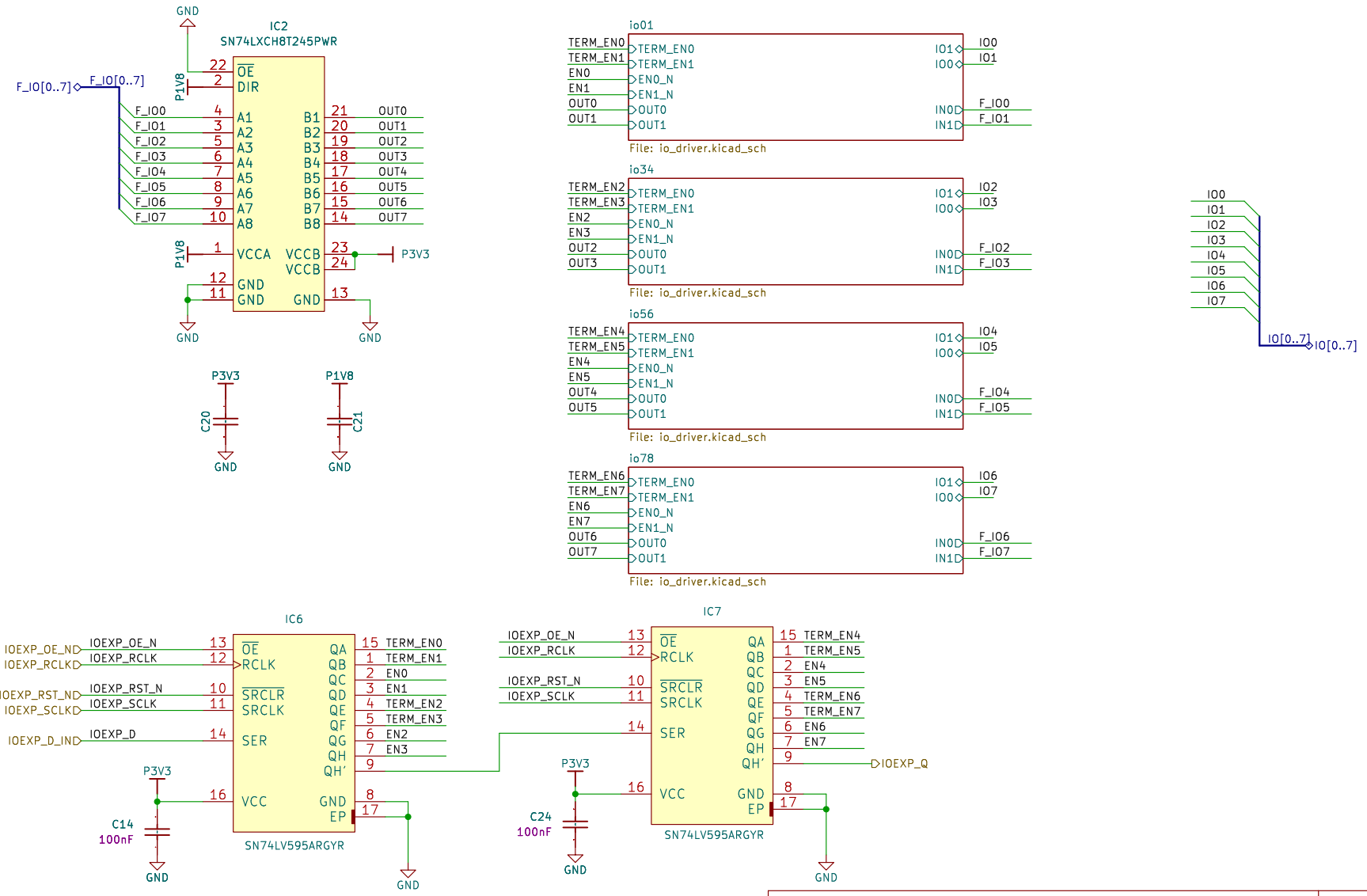
VME P0

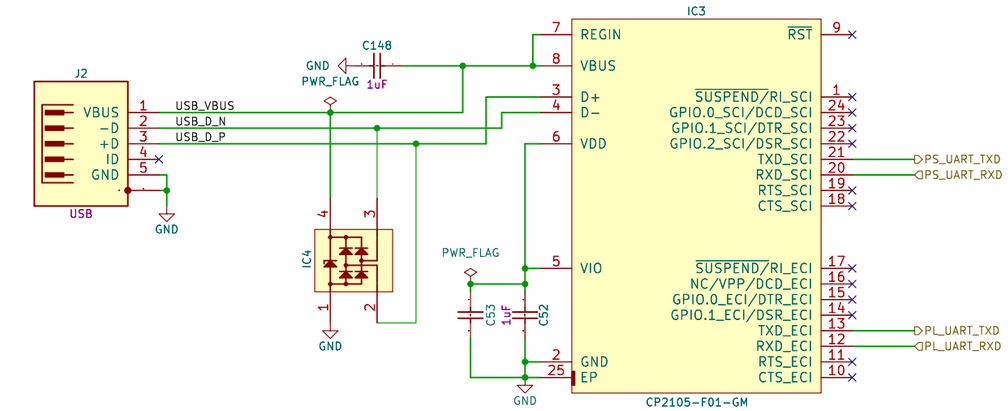


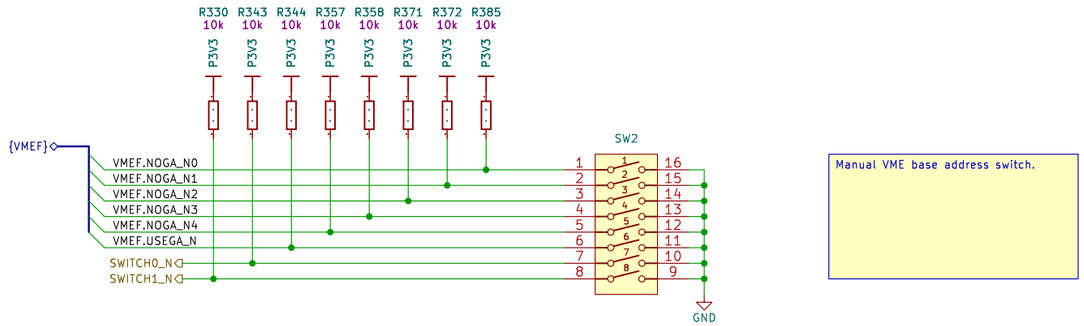
Project: VME-WREN

VME P0 connector fanout + mechanics

Sheet: /vme_interface/vme_p0/	
File: vme_p0.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A3 — Last Modified: —	**Rev:**
KiCad E.D.A. 8.0.0	Id: 18/73


IC2
SN74LXCH8T245PWR
F_IO[0..7]
P1V8
P3V3
GND
C20
C21
io01
io34
io56
io78
File: io_driver.kicad_sch
IO[0..7]
IC6
IC7
SN74LV595ARGYR
IOEXP_OE_N
IOEXP_RCLK
IOEXP_RST_N
IOEXP_SCLK
IOEXP_D_IN
IOEXP_Q
C14
100nF
C24
100nF
Project: VME-WREN
Front/Patch Panel I/O driver - 8 channels
Sheet: /io_drivers_fp/bank1/
File: io_driver_8x.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A4
Last Modified: -
KiCad E.D.A. 8.0.0
Rev:
Id: 19/73



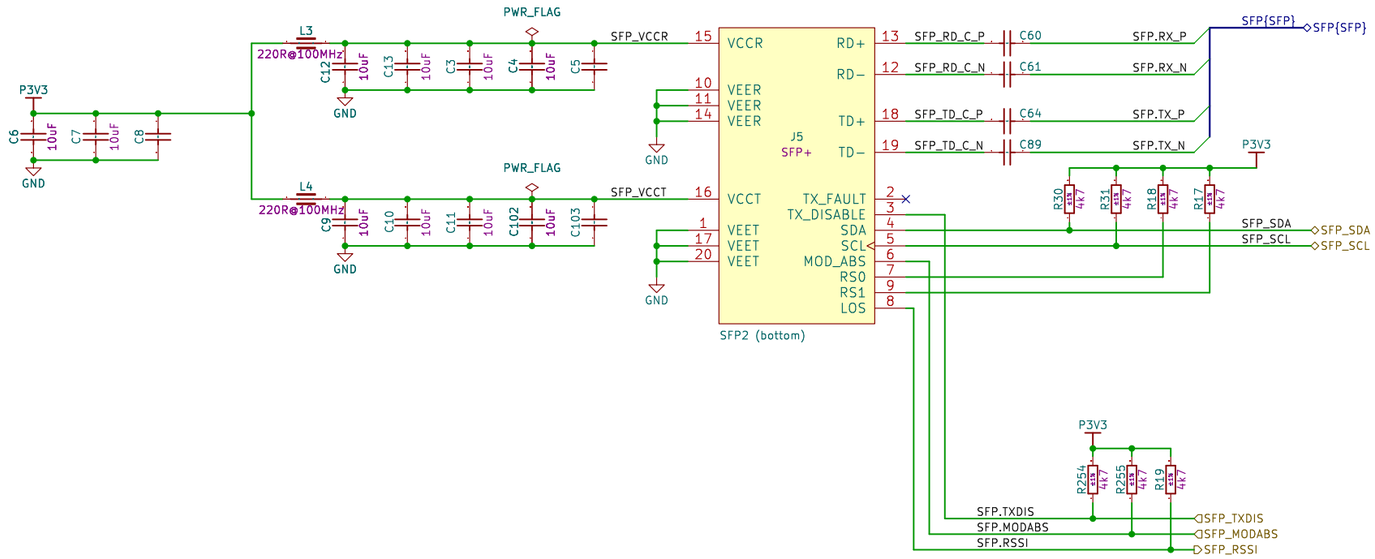


Manual VME base address switch.

Project: VME−WREN

User Interface

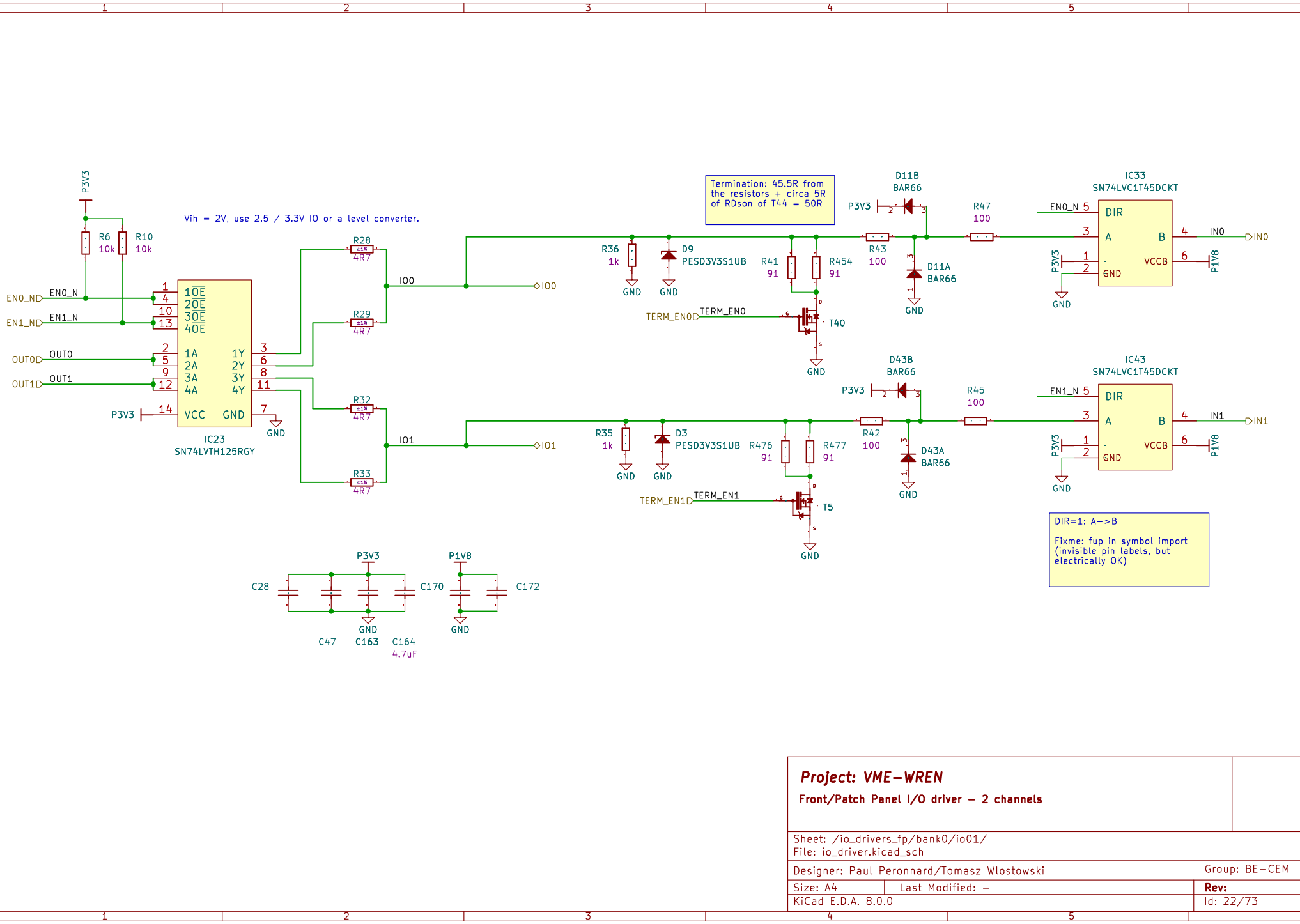
Sheet: /user_interface/ File: user_interface.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE−CEM
Size: A3	Last Modified: −	**Rev: −**
KiCad E.D.A. 8.0.0		Id: 20/73



Project: VME−WREN

SFP+ Cage

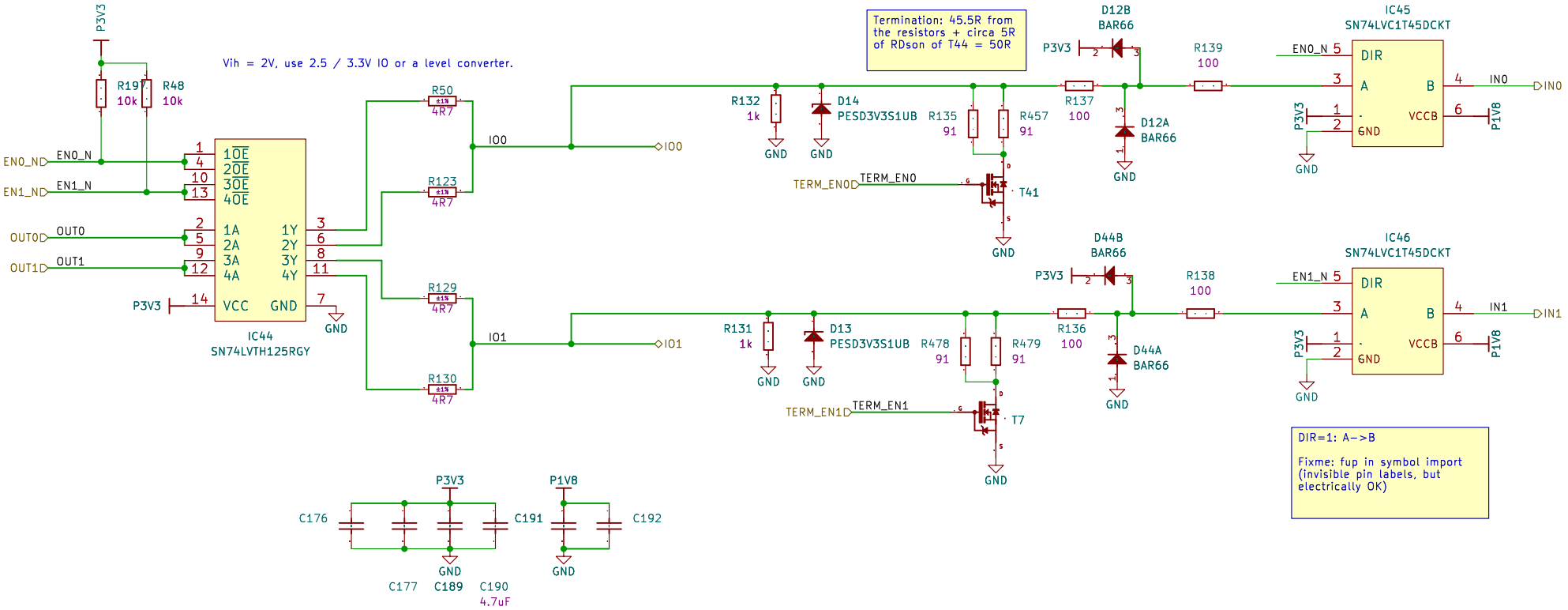
Sheet: /SFP0/ File: sfp+.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE−CEM
Size: A3	Last Modified: −	**Rev: −**
KiCad E.D.A. 8.0.0		Id: 21/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

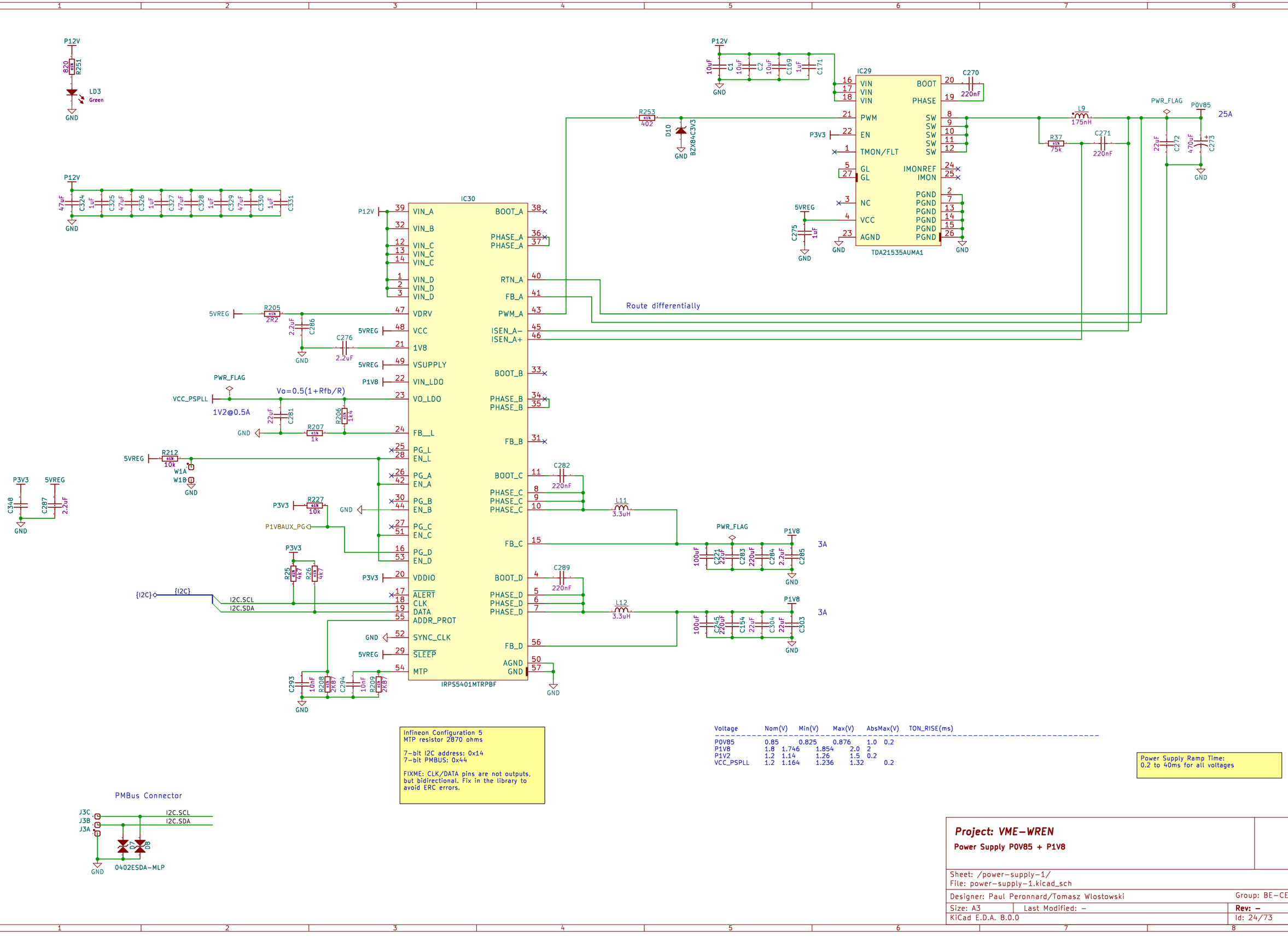
Sheet: /io_drivers_fp/bank0/io01/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 22/73



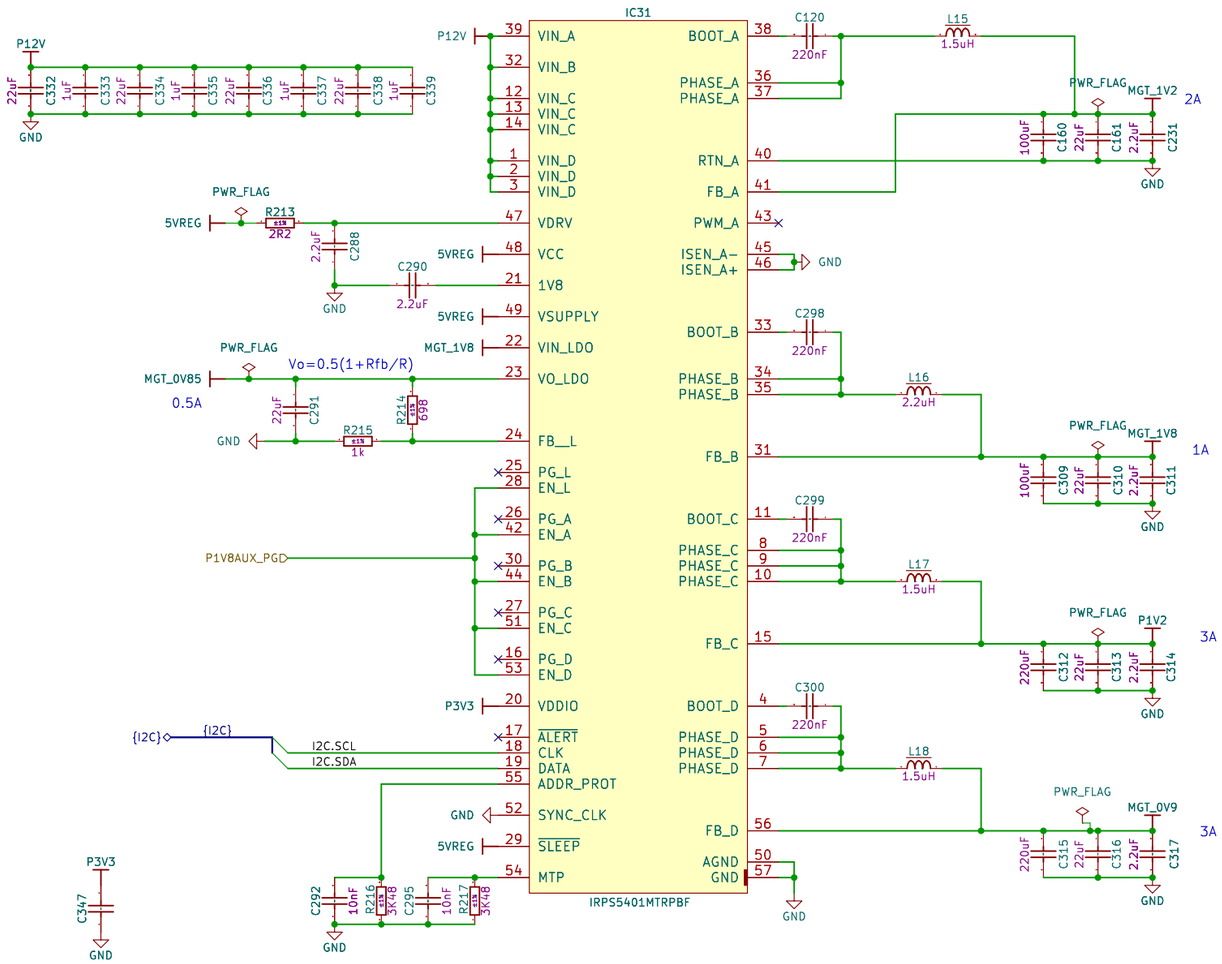
Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

Sheet: /io_drivers_fp/bank0/io34/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 23/73



Voltage	Nom(V)	Min(V)	Max(V)	AbsMax(V)	TON_RISE(ms)
P0V85	0.85	0.825	0.876	1.0	0.2
P1V8	1.8	1.746	1.854	2.0	2
P1V2	1.2	1.14	1.26	1.5	0.2
VCC_PSPLL	1.2	1.164	1.236	1.32	0.2



Power Supply Ramp Time:
0.2 to 40ms for all voltages

Infineon Configuration 6
MTP resistor 3480 ohms

7-bit I2C address: 0x15
7-bit PMBUS: 0x45

Voltage	Nom(V)	Min(V)	Max(V)	AbsMax(V)	TON_RISE(ms)
P3V3	3.3	3.2	3.4	3.4	5
MGT_1V8	1.8	1.746	1.854	1.9	0.2
MGT_0V9	0.9	0.873	0.927	1.0	0.2
MGT_1V2	1.2	1.164	1.236	1.3	0.2
MGT_0V85	0.85	0.825	0.875	1.0	0.2

Project: VME-WREN

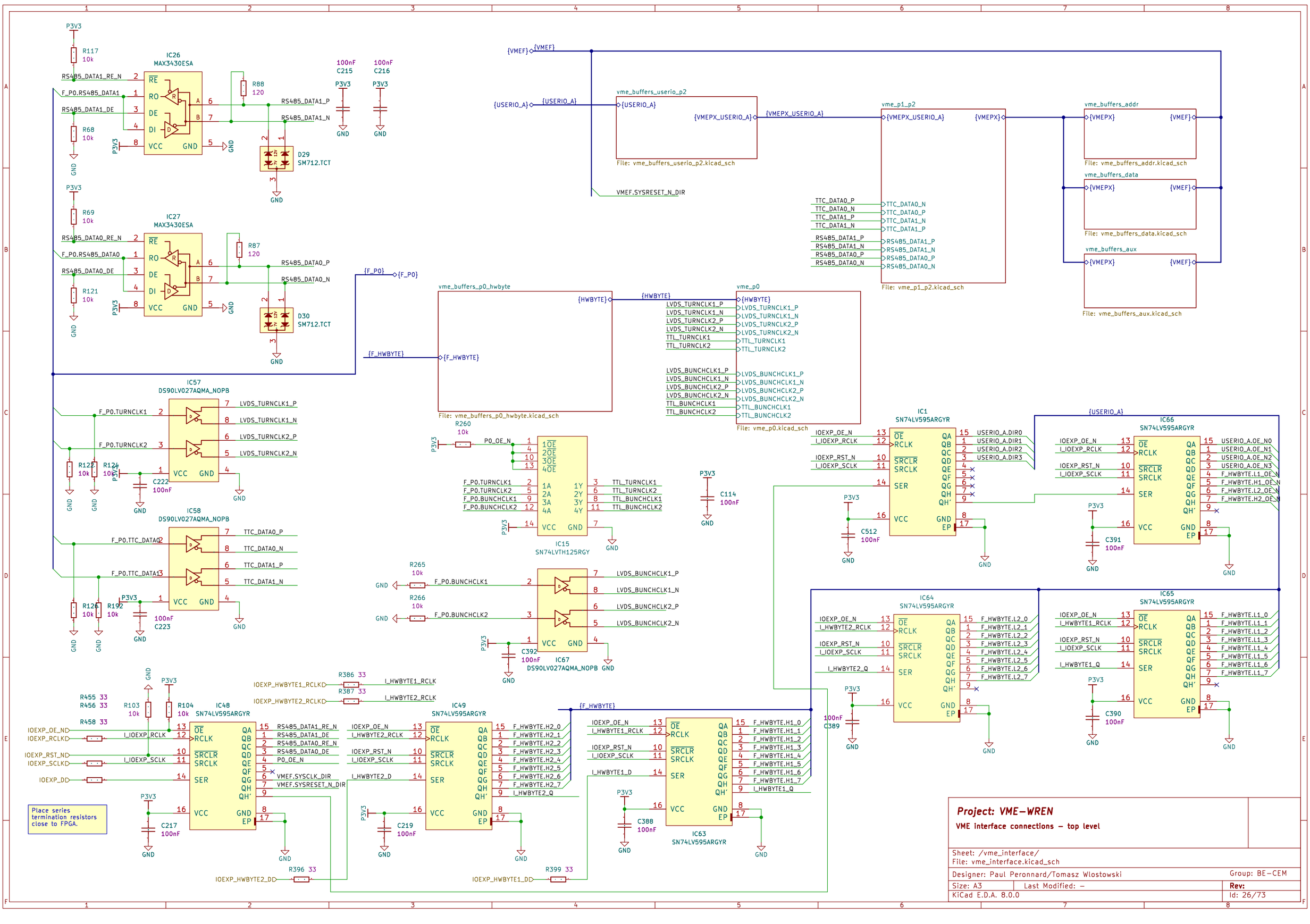
Power Supply P1V2 + P1V8_MGT + P1V2_MGT + P0V9_MGT

Sheet: /power-supply-2/
File: power-supply-2.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM

Size: A3
Last Modified: -
Rev: -

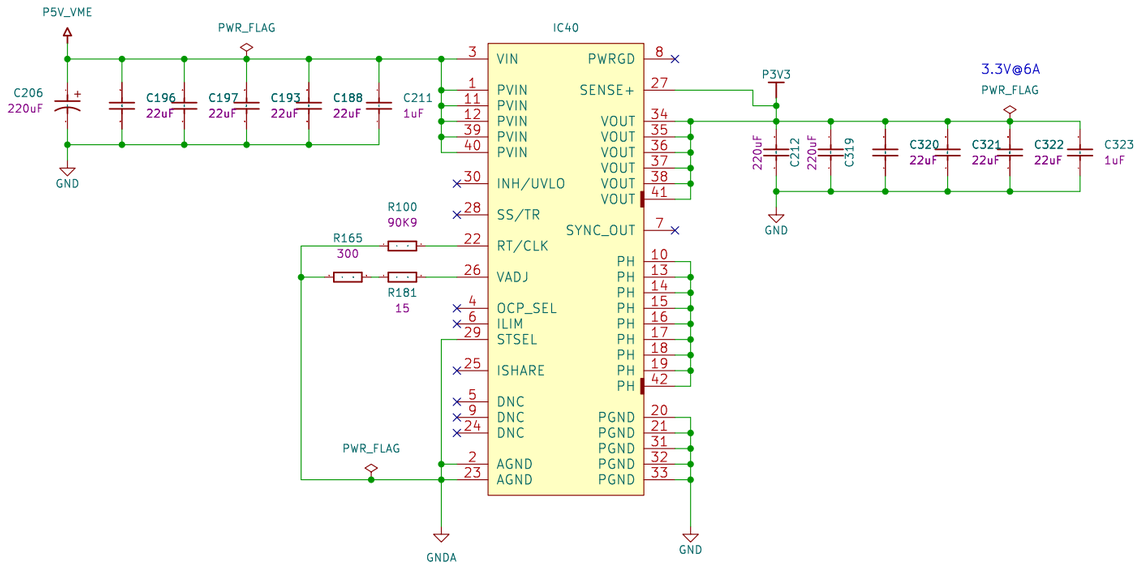
KiCad E.D.A. 8.0.0
Id: 25/73


P3V3
R117
10k
IC26
MAX3430ESA
RS485_DATA1_RE_N
F_P0.RS485_DATA1
RS485_DATA1_DE
R68
10k
R88
120
RS485_DATA1_P
RS485_DATA1_N
D29
SM712.TCT
100nF
C215
C216
GND
R69
10k
IC27
MAX3430ESA
RS485_DATA0_RE_N
F_P0.RS485_DATA0
RS485_DATA0_DE
R121
10k
R87
120
RS485_DATA0_P
RS485_DATA0_N
D30
SM712.TCT
{F_P0}
{F_HWBYTE}
vme_buffers_p0_hwbyte
File: vme_buffers_p0_hwbyte.kicad_sch
R260
10k
P0_OE_N
IC15
SN74LVTH125RGY
F_P0.TURNCLK1
F_P0.TURNCLK2
F_P0.BUNCHCLK1
F_P0.BUNCHCLK2
TTL_TURNCLK1
TTL_TURNCLK2
TTL_BUNCHCLK1
TTL_BUNCHCLK2
C114
100nF
IC57
DS90LV027AQMA_NOPB
F_P0.TURNCLK1
F_P0.TURNCLK2
LVDS_TURNCLK1_P
LVDS_TURNCLK1_N
LVDS_TURNCLK2_P
LVDS_TURNCLK2_N
R122
10k
R124
10k
C222
100nF
IC58
DS90LV027AQMA_NOPB
F_P0.TTC_DATA0
F_P0.TTC_DATA1
TTC_DATA0_P
TTC_DATA0_N
TTC_DATA1_P
TTC_DATA1_N
R125
10k
R192
10k
C223
100nF
R265
10k
R266
10k
F_P0.BUNCHCLK1
F_P0.BUNCHCLK2
LVDS_BUNCHCLK1_P
LVDS_BUNCHCLK1_N
LVDS_BUNCHCLK2_P
LVDS_BUNCHCLK2_N
C392
100nF
IC67
DS90LV027AQMA_NOPB
{VMEF}
{USERIO_A}
vme_buffers_userio_p2
{VMEPX_USERIO_A}
File: vme_buffers_userio_p2.kicad_sch
VMEF.SYSRESET_N_DIR
vme_p1_p2
{VMEPX}
File: vme_p1_p2.kicad_sch
TTC_DATA0_P
TTC_DATA0_N
TTC_DATA1_P
TTC_DATA1_N
RS485_DATA1_P
RS485_DATA1_N
RS485_DATA0_P
RS485_DATA0_N
vme_buffers_addr
File: vme_buffers_addr.kicad_sch
vme_buffers_data
File: vme_buffers_data.kicad_sch
vme_buffers_aux
File: vme_buffers_aux.kicad_sch
vme_p0
{HWBYTE}
LVDS_TURNCLK1_P
LVDS_TURNCLK1_N
LVDS_TURNCLK2_P
LVDS_TURNCLK2_N
TTL_TURNCLK1
TTL_TURNCLK2
LVDS_BUNCHCLK1_P
LVDS_BUNCHCLK1_N
LVDS_BUNCHCLK2_P
LVDS_BUNCHCLK2_N
TTL_BUNCHCLK1
TTL_BUNCHCLK2
File: vme_p0.kicad_sch
IC1
SN74LV595ARGYR
IOEXP_OE_N
I_IOEXP_RCLK
IOEXP_RST_N
I_IOEXP_SCLK
USERIO_A.DIR0
USERIO_A.DIR1
USERIO_A.DIR2
USERIO_A.DIR3
C512
100nF
IC66
SN74LV595ARGYR
USERIO_A.OE_N0
USERIO_A.OE_N1
USERIO_A.OE_N2
USERIO_A.OE_N3
F_HWBYTE.L1_OE_N
F_HWBYTE.H1_OE_N
F_HWBYTE.L2_OE_N
F_HWBYTE.H2_OE_N
C391
100nF
IC64
SN74LV595ARGYR
I_HWBYTE2_RCLK
I_HWBYTE2_Q
F_HWBYTE.L2_0
F_HWBYTE.L2_1
F_HWBYTE.L2_2
F_HWBYTE.L2_3
F_HWBYTE.L2_4
F_HWBYTE.L2_5
F_HWBYTE.L2_6
F_HWBYTE.L2_7
100nF
C389
IC65
SN74LV595ARGYR
I_HWBYTE1_RCLK
I_HWBYTE1_Q
F_HWBYTE.L1_0
F_HWBYTE.L1_1
F_HWBYTE.L1_2
F_HWBYTE.L1_3
F_HWBYTE.L1_4
F_HWBYTE.L1_5
F_HWBYTE.L1_6
F_HWBYTE.L1_7
C390
100nF
R386 33
R387 33
IOEXP_HWBYTE1_RCLK
IOEXP_HWBYTE2_RCLK
I_HWBYTE1_RCLK
I_HWBYTE2_RCLK
R455 33
R456 33
R458 33
R103
10k
R104
10k
IC48
SN74LV595ARGYR
IOEXP_OE_ND
IOEXP_RCLK
IOEXP_RST_ND
IOEXP_SCLK
IOEXP_DD
RS485_DATA1_RE_N
RS485_DATA1_DE
RS485_DATA0_RE_N
RS485_DATA0_DE
P0_OE_N
VMEF.SYSCLK_DIR
VMEF.SYSRESET_N_DIR
C217
100nF
IC49
SN74LV595ARGYR
I_HWBYTE2_D
F_HWBYTE.H2_0
F_HWBYTE.H2_1
F_HWBYTE.H2_2
F_HWBYTE.H2_3
F_HWBYTE.H2_4
F_HWBYTE.H2_5
F_HWBYTE.H2_6
F_HWBYTE.H2_7
I_HWBYTE2_Q
C219
100nF
R396 33
IOEXP_HWBYTE2_DD
R399 33
IOEXP_HWBYTE1_DD
I_HWBYTE1_D
F_HWBYTE.H1_0
F_HWBYTE.H1_1
F_HWBYTE.H1_2
F_HWBYTE.H1_3
F_HWBYTE.H1_4
F_HWBYTE.H1_5
F_HWBYTE.H1_6
F_HWBYTE.H1_7
I_HWBYTE1_Q
C388
100nF
IC63
SN74LV595ARGYR
Place series termination resistors close to FPGA.
Project: VME-WREN
VME interface connections - top level
Sheet: /vme_interface/
File: vme_interface.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A3
Last Modified: -
Rev:
KiCad E.D.A. 8.0.0
Id: 26/73

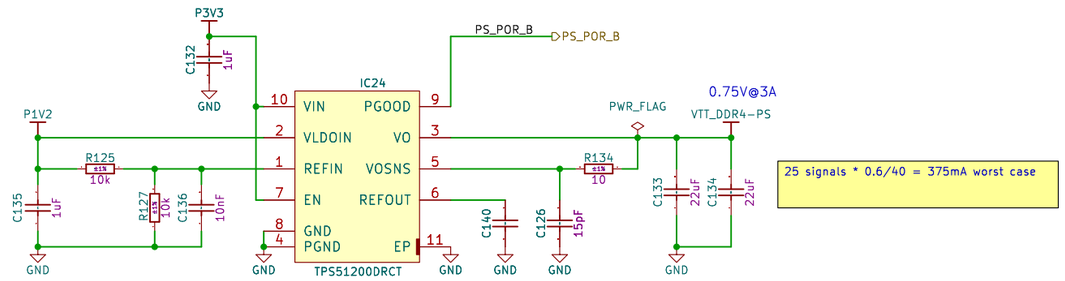
5V -> 3.3V regurgitator, 6A

Due to special request by the Computer History Museum and the CERN Retrocomputing Club, we cannot rely on the +3.3V VME64x power rail as it is not available in certain models of VME crates...

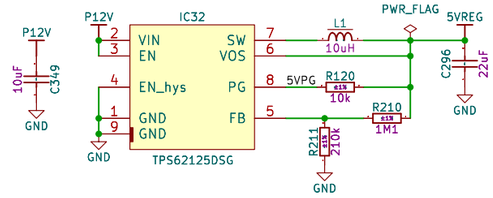
So we must produce the 3.3V from 5V here.

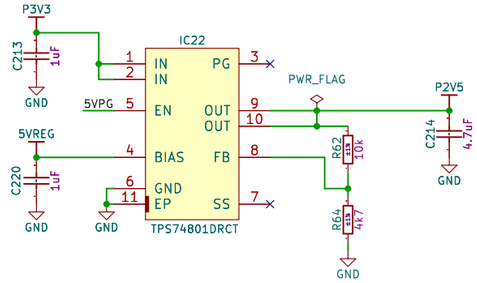


AGND pins are associated with the internal analog ground of the device. Keep AGND seperate from PGND, as a single connection is made internal to the device



25 signals * 0.6/40 = 375mA worst case

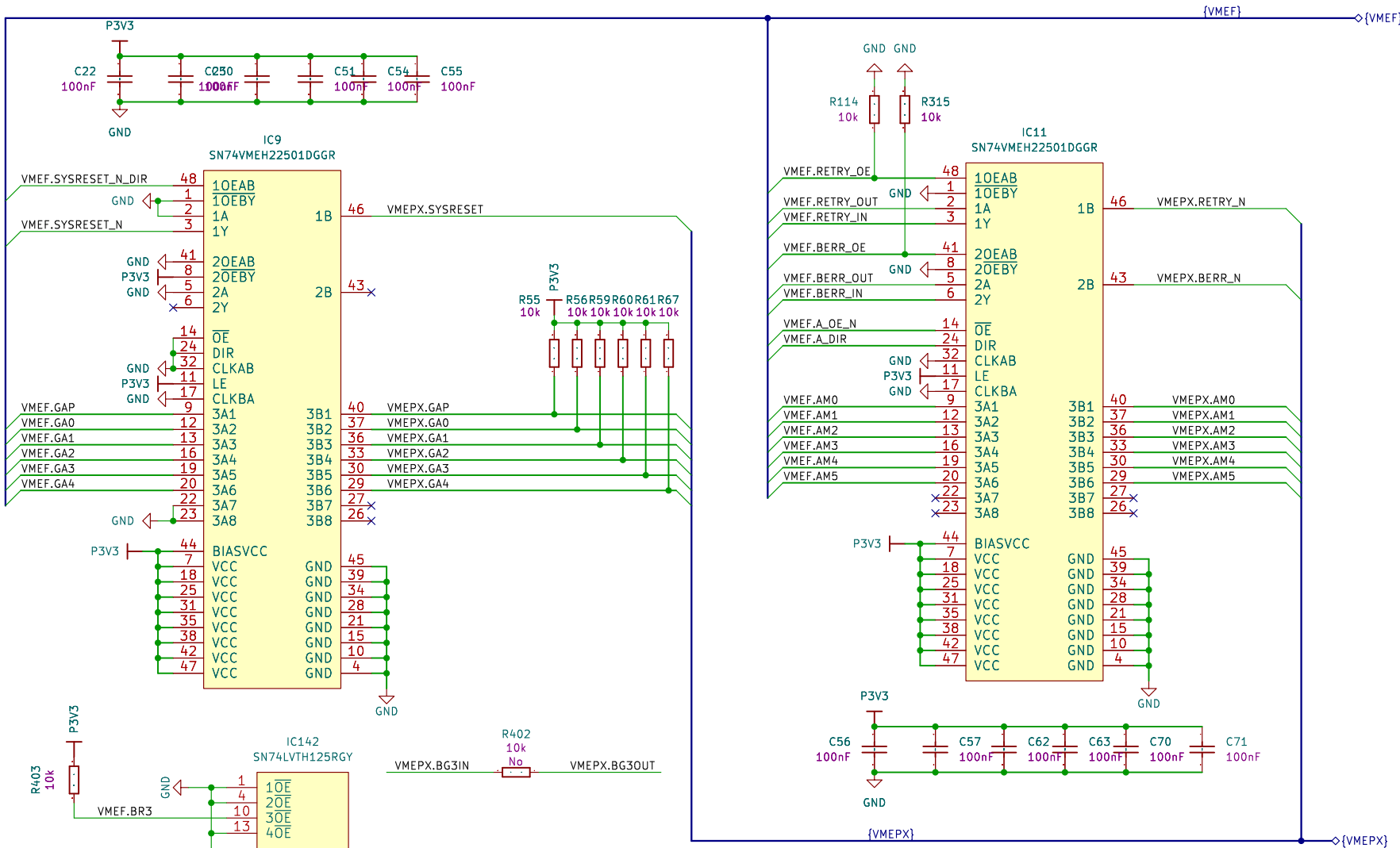




Project: VME-WREN

Power Supply - P3V3, DDR VTT, P2V5, P5VREG

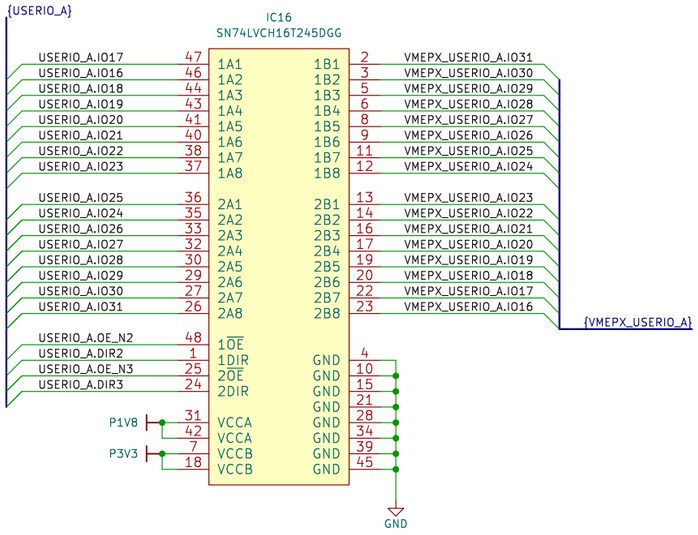
Sheet: /power-supply-3/ File: power-supply-3.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A3 Last Modified: -	**Rev: -**
KiCad E.D.A. 8.0.0	Id: 26/73

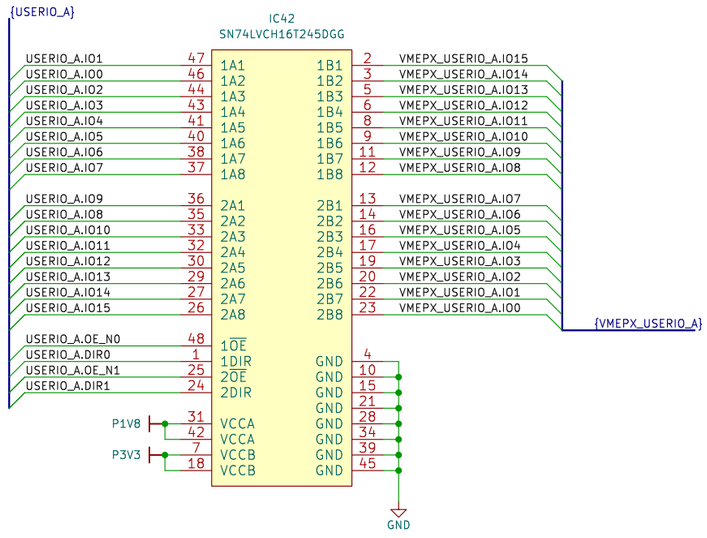


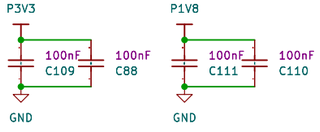
Project: VME-WREN

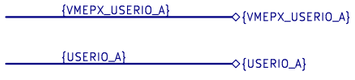
VME buffers – auxillary signals (AM, BERR, RETRY)

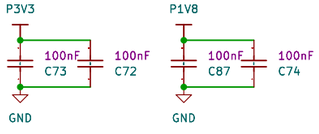
Sheet: /vme_interface/vme_buffers_aux/ File: vme_buffers_aux.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: –	**Rev:**
KiCad E.D.A. 8.0.0	Id: 27/73











Project: VME–WREN

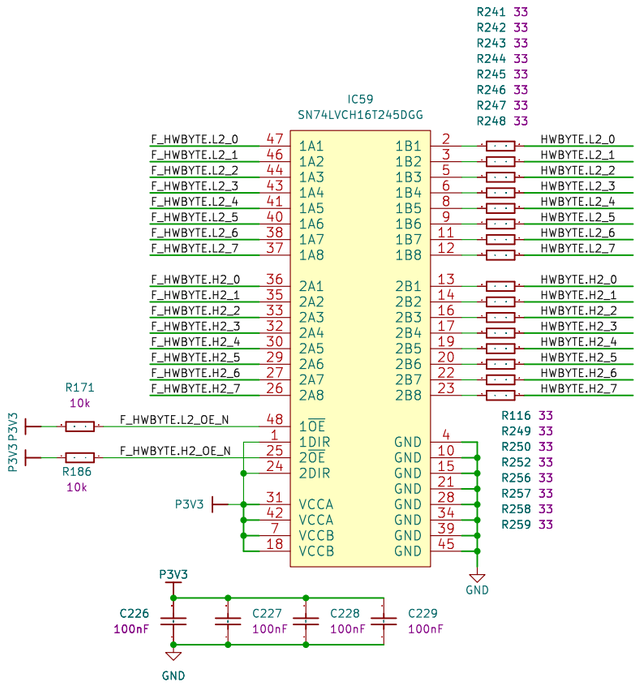
VME buffers – P2 row A timing I/O

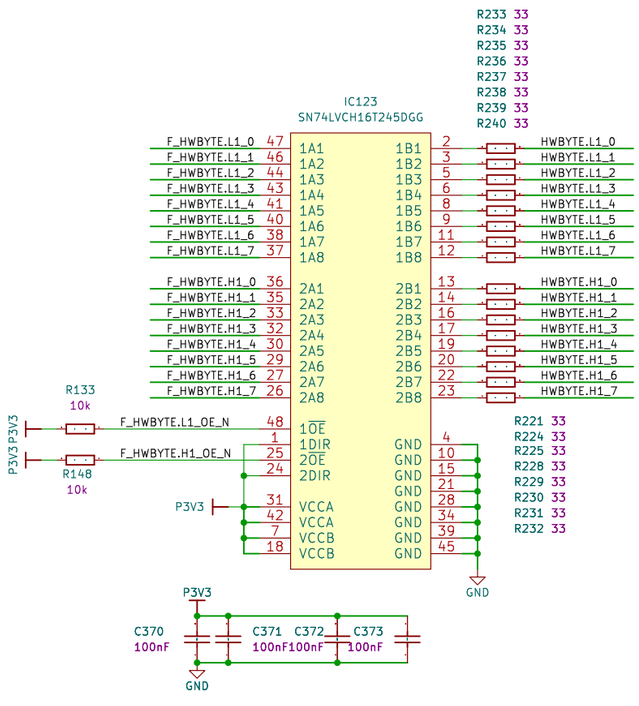
Sheet: /vme_interface/vme_buffers_userio_p2/
File: vme_buffers_userio_p2.kicad_sch

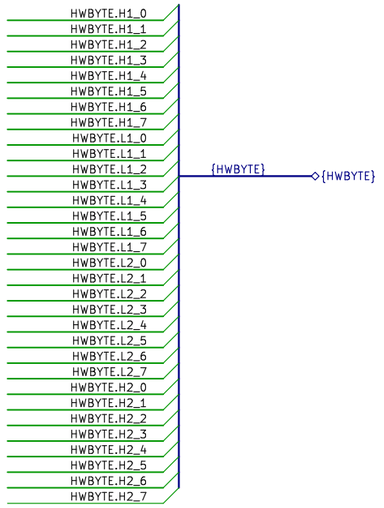
Designer: Paul Peronnard/Tomasz Wlostowski | Group: BE–CEM

Size: A3 | Last Modified: – | **Rev:**

KiCad E.D.A. 8.0.0 | Id: 28/73







Project: VME–WREN

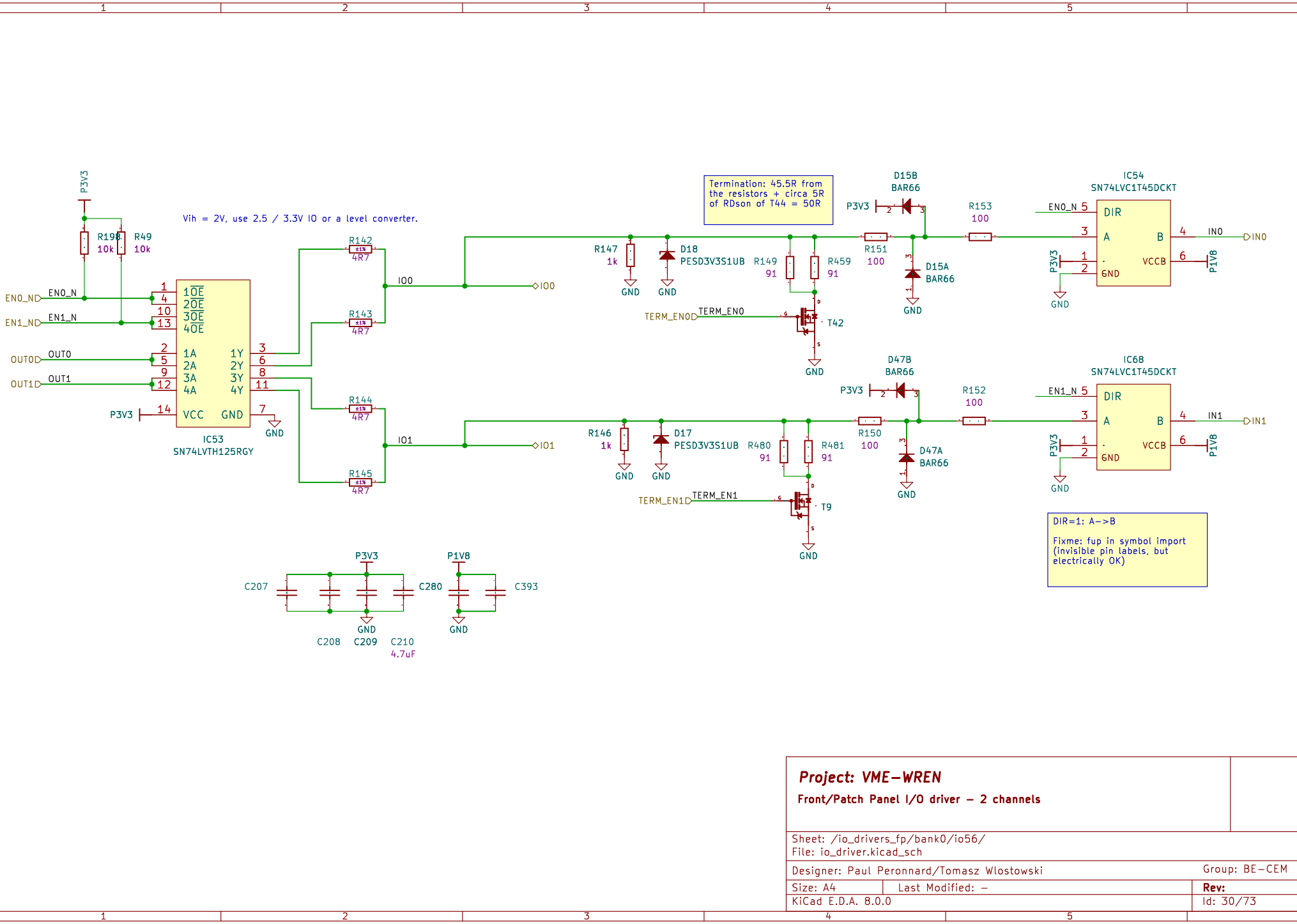
VME buffers – P0 HWByte

Sheet: /vme_interface/vme_buffers_p0_hwbyte/
File: vme_buffers_p0_hwbyte.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski | Group: BE–CEM

Size: A3 | Last Modified: – | **Rev:**

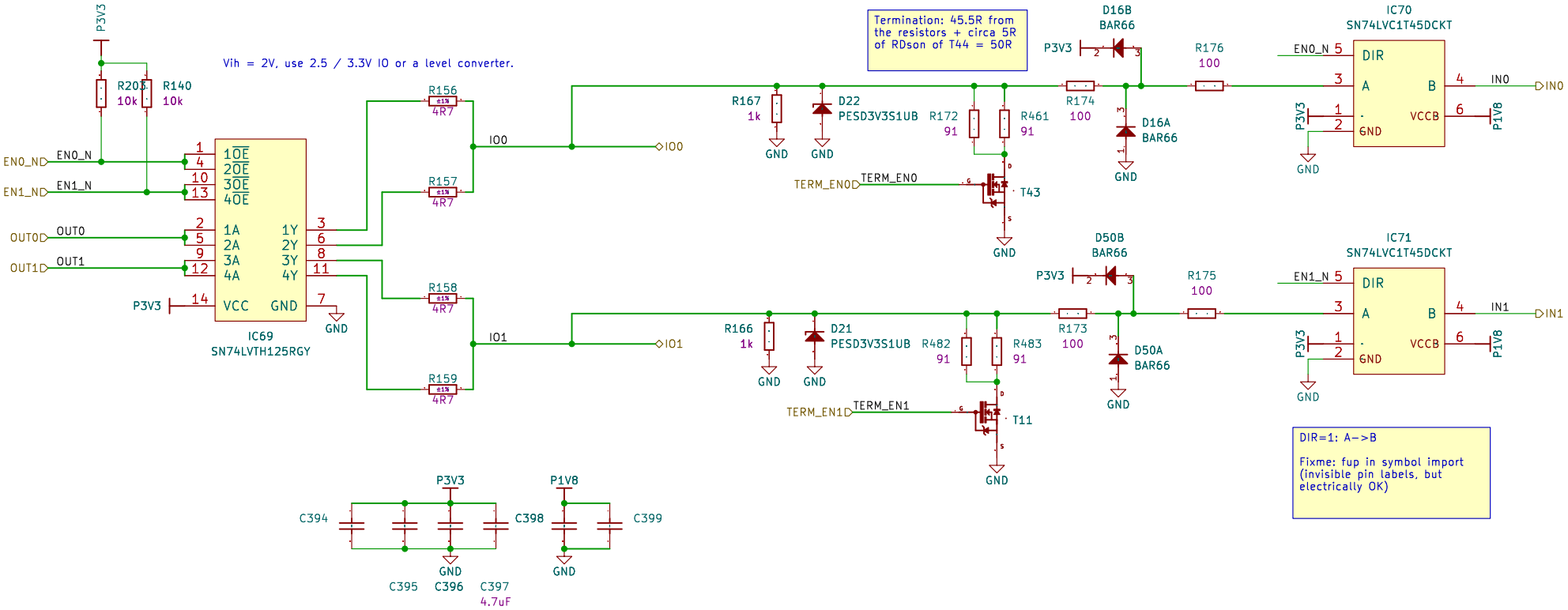
KiCad E.D.A. 8.0.0 | Id: 29/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

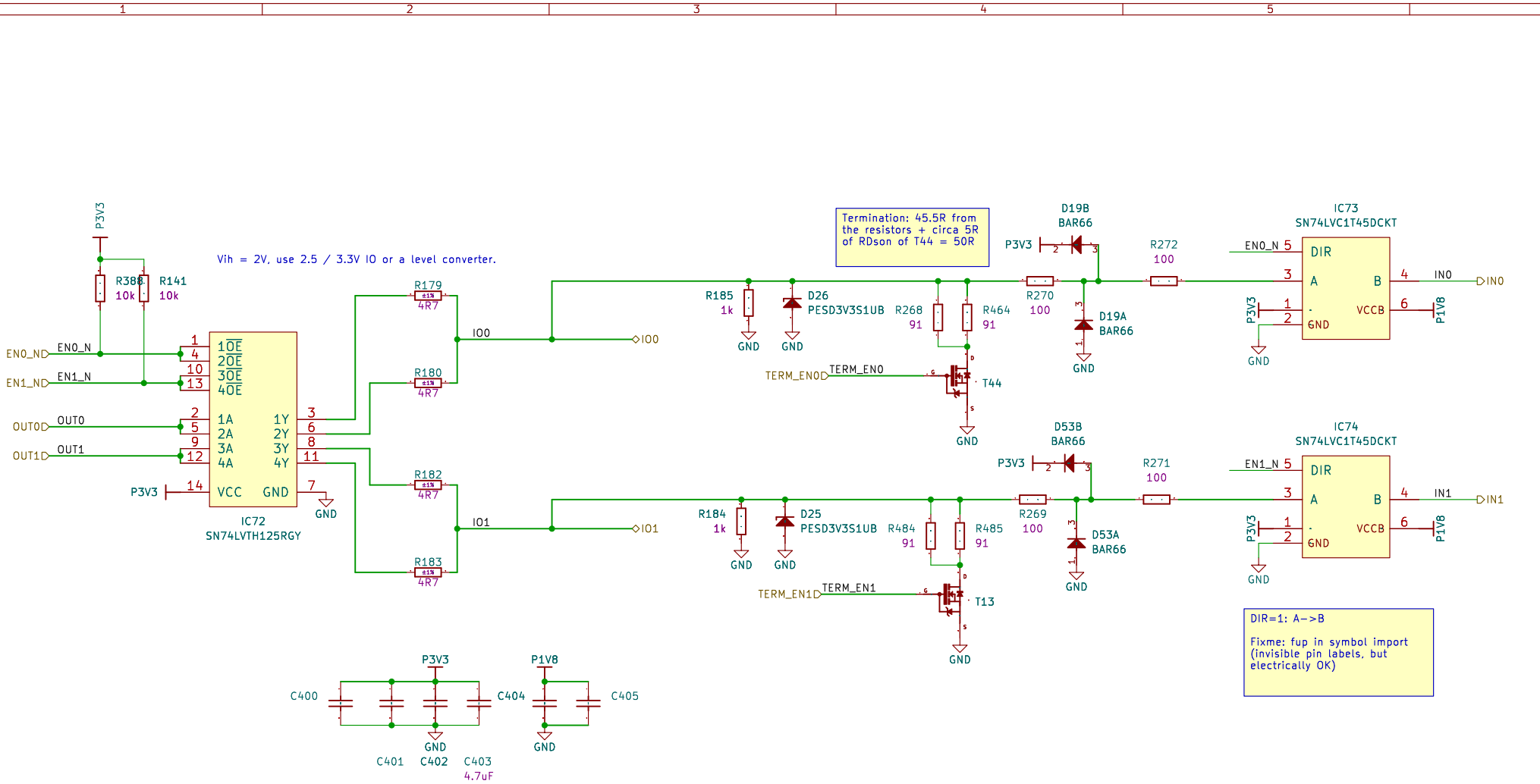
Sheet: /io_drivers_fp/bank0/io56/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 30/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

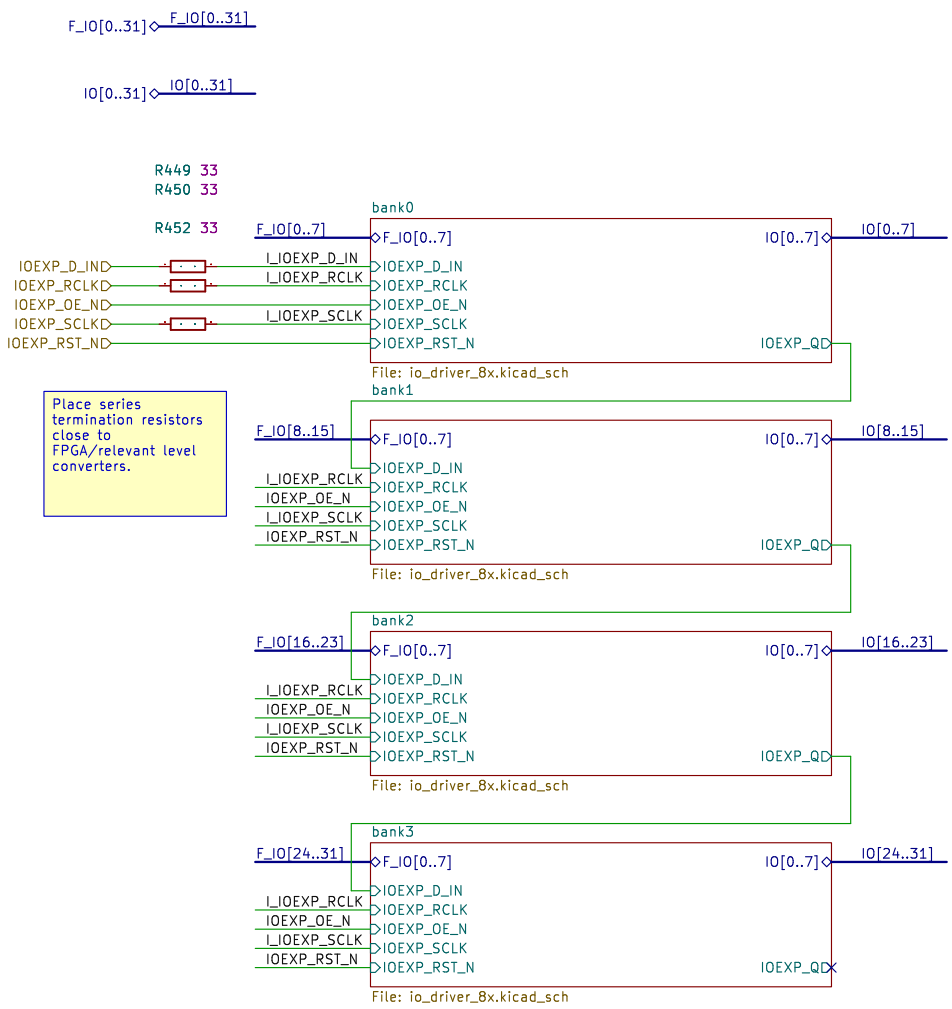
Sheet: /io_drivers_fp/bank0/io78/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 31/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

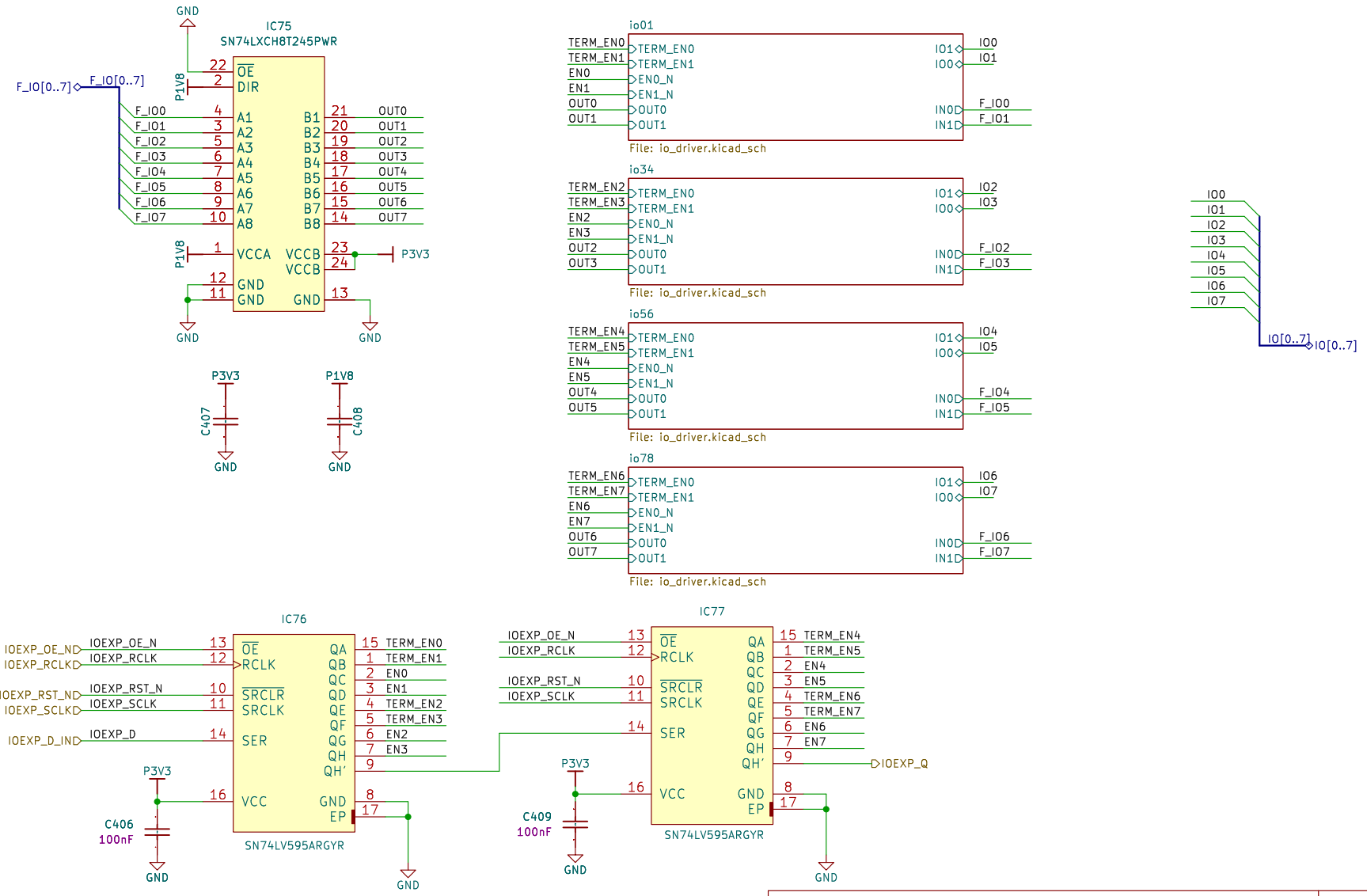
Sheet: /io_drivers_fp/bank1/io78/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 32/73

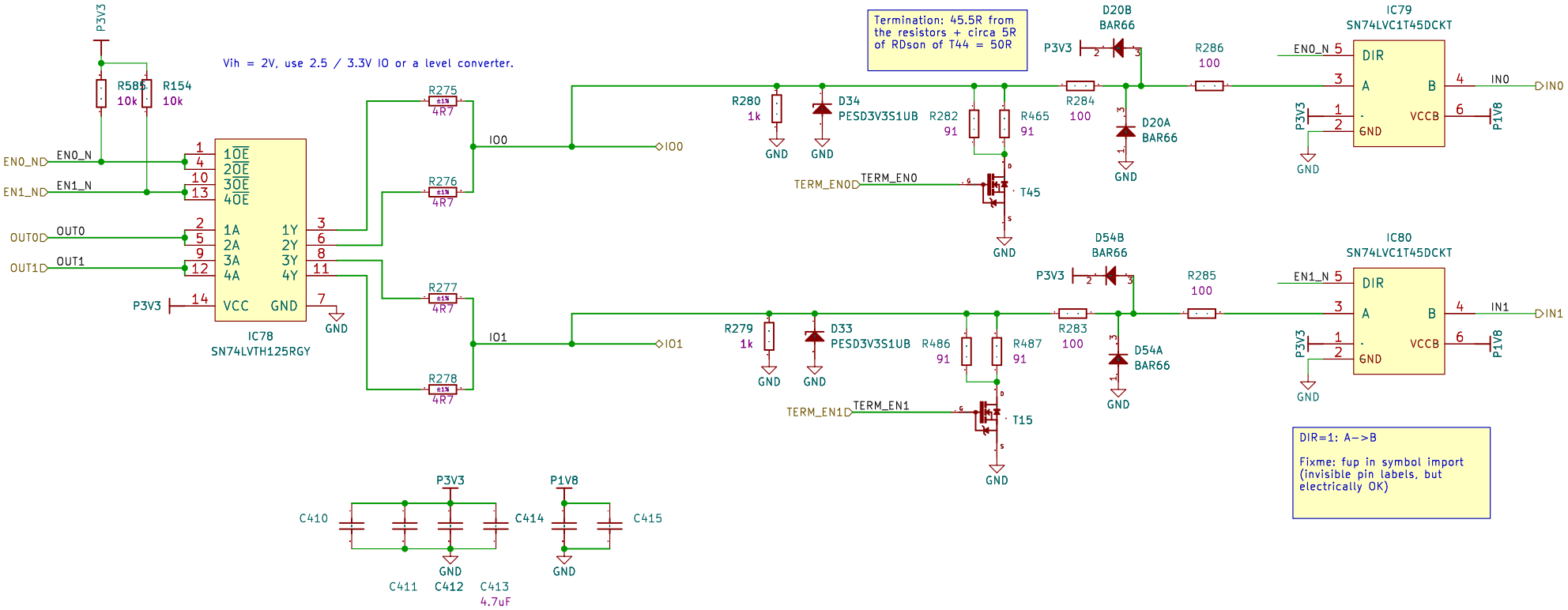


Project: VME-WREN

Front/Patch panel I/O driver (32 channels)

Sheet: /io_drivers_fp/ File: io_driver_32x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: –	**Rev:**
KiCad E.D.A. 8.0.0		Id: 33/73

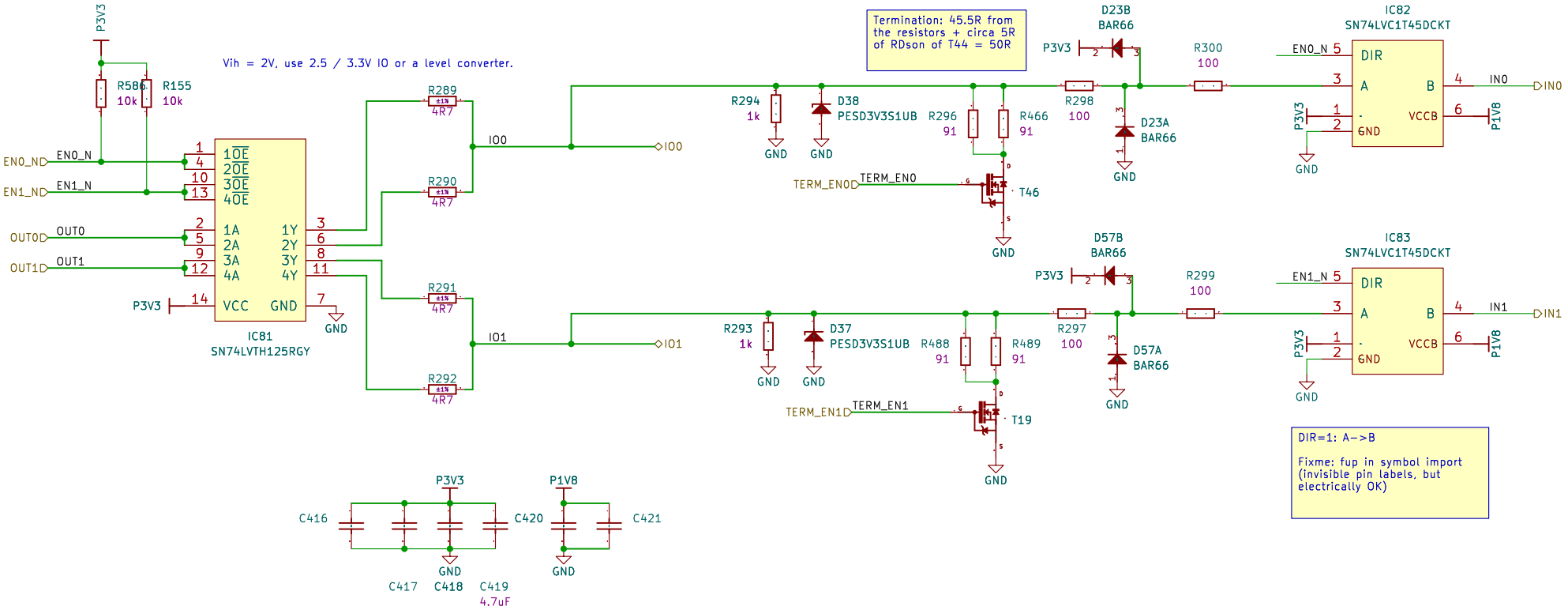

IC75
SN74LXCH8T245PWR
F_IO[0..7]
P1V8
P3V3
GND
C407
C408
io01
io34
io56
io78
File: io_driver.kicad_sch
IO[0..7]
IC76
IC77
SN74LV595ARGYR
IOEXP_OE_N
IOEXP_RCLK
IOEXP_RST_N
IOEXP_SCLK
IOEXP_D_IN
IOEXP_Q
C406
100nF
C409
100nF
Project: VME-WREN
Front/Patch Panel I/O driver - 8 channels
Sheet: /io_drivers_fp/bank0/
File: io_driver_8x.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A4
Last Modified: -
KiCad E.D.A. 8.0.0
Rev:
Id: 33/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

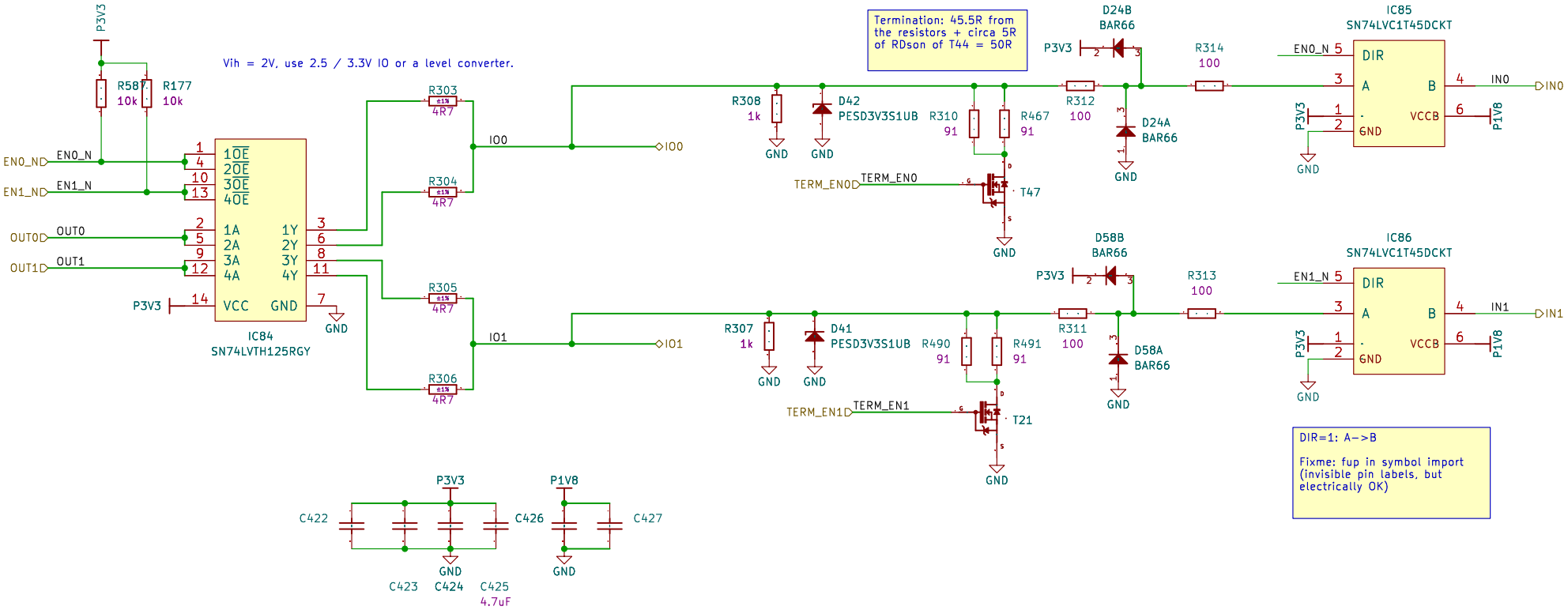
Sheet: /io_drivers_fp/bank1/io01/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 34/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

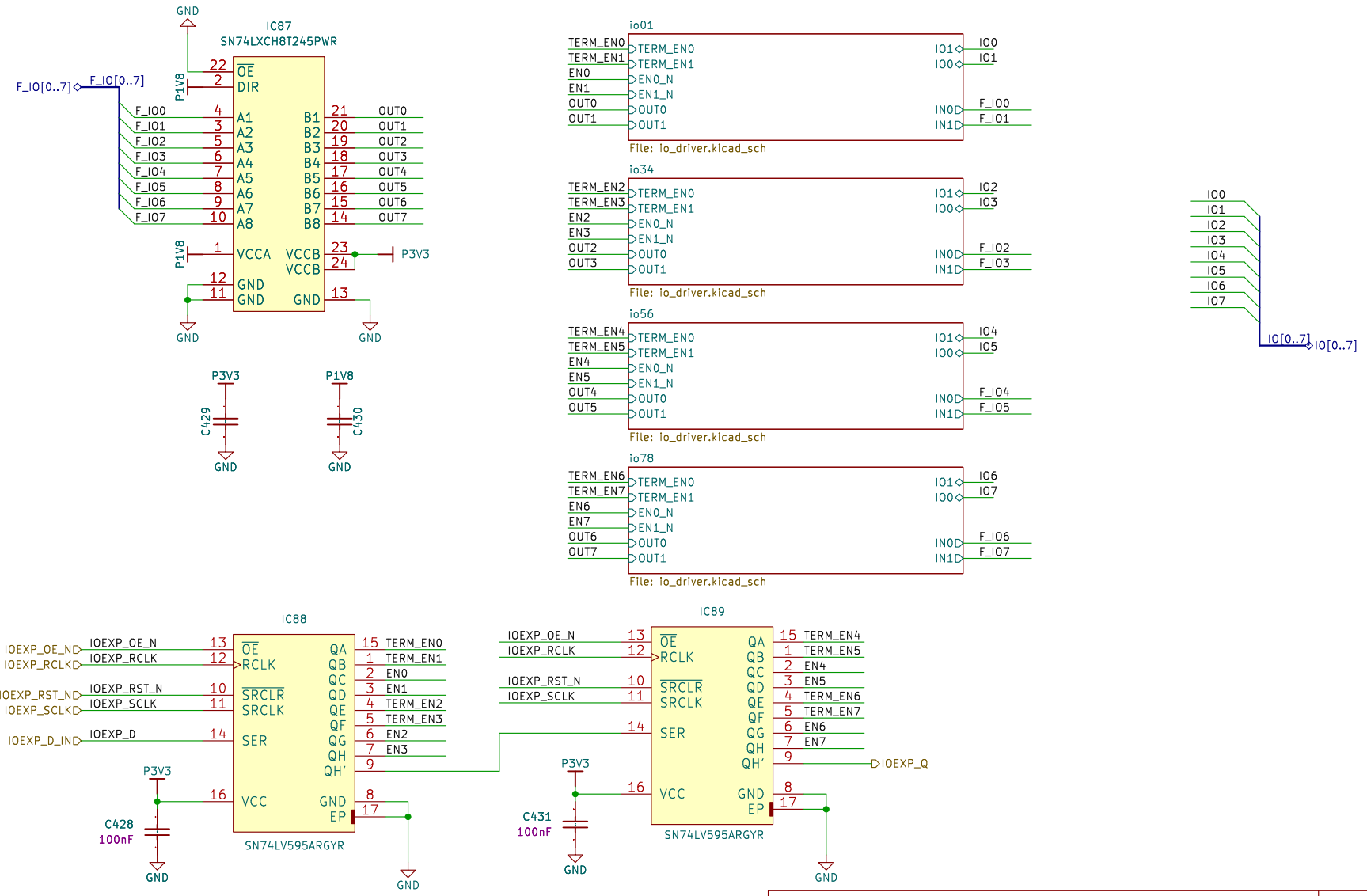
Sheet: /io_drivers_fp/bank1/io34/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 35/73

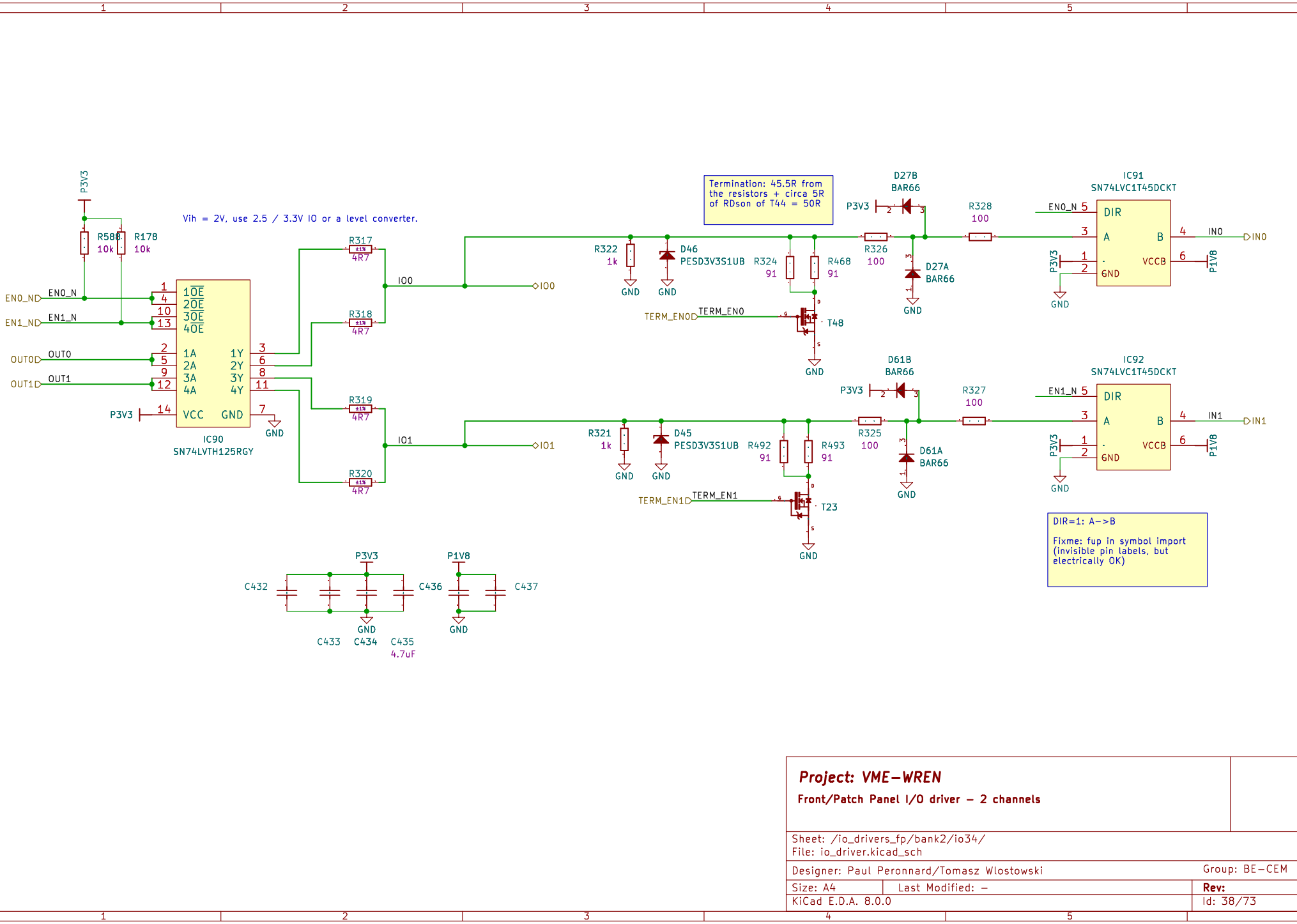


Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

Sheet: /io_drivers_fp/bank1/io56/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 36/73

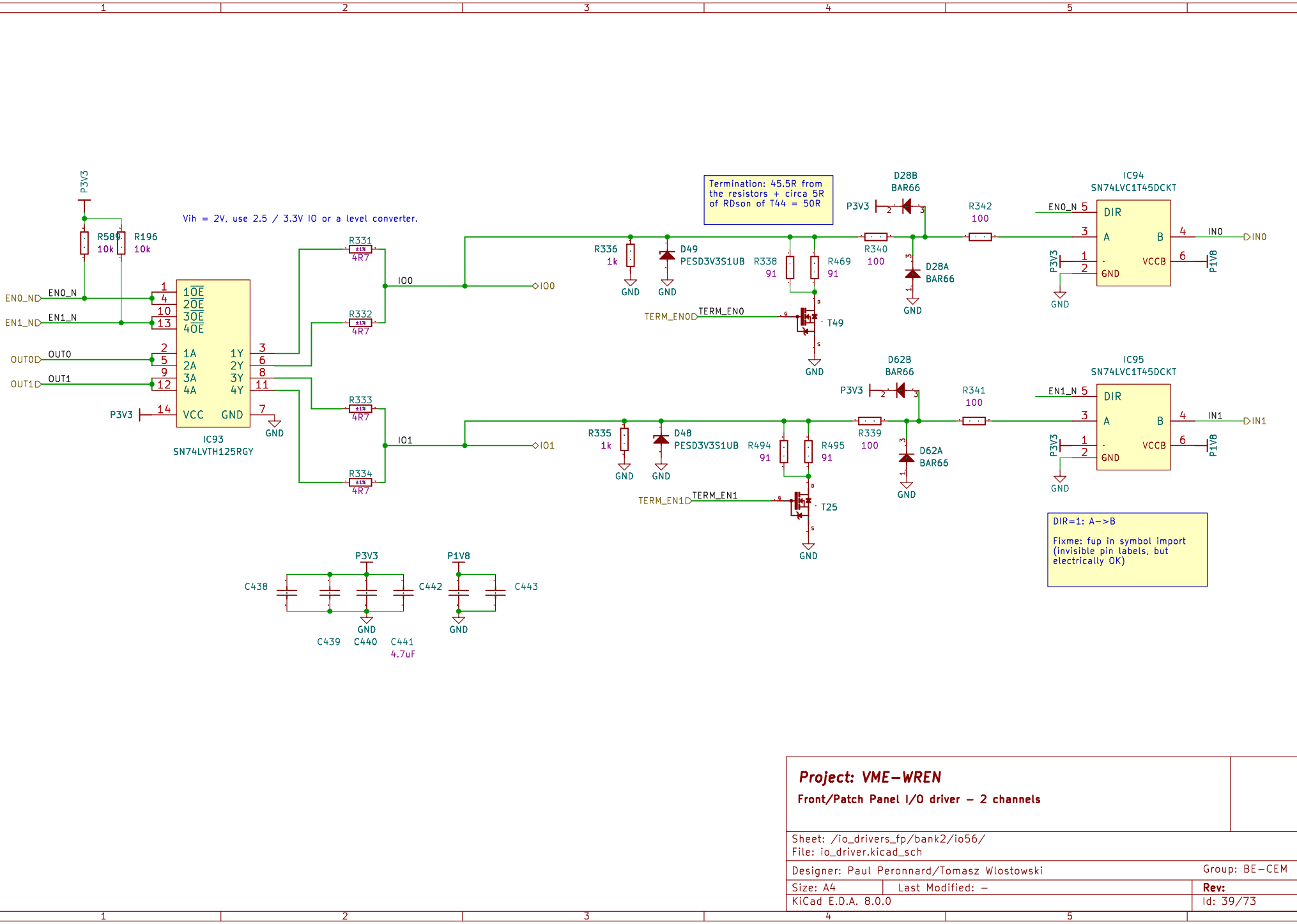

IC87
SN74LXCH8T245PWR
F_IO[0..7]
P1V8
P3V3
GND
C429
C430
io01
io34
io56
io78
File: io_driver.kicad_sch
IO[0..7]
IC88
IC89
SN74LV595ARGYR
IOEXP_OE_N
IOEXP_RCLK
IOEXP_RST_N
IOEXP_SCLK
IOEXP_D_IN
IOEXP_Q
C428
100nF
C431
100nF
Project: VME-WREN
Front/Patch Panel I/O driver - 8 channels
Sheet: /io_drivers_fp/bank2/
File: io_driver_8x.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A4
Last Modified: -
Rev:
KiCad E.D.A. 8.0.0
Id: 37/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

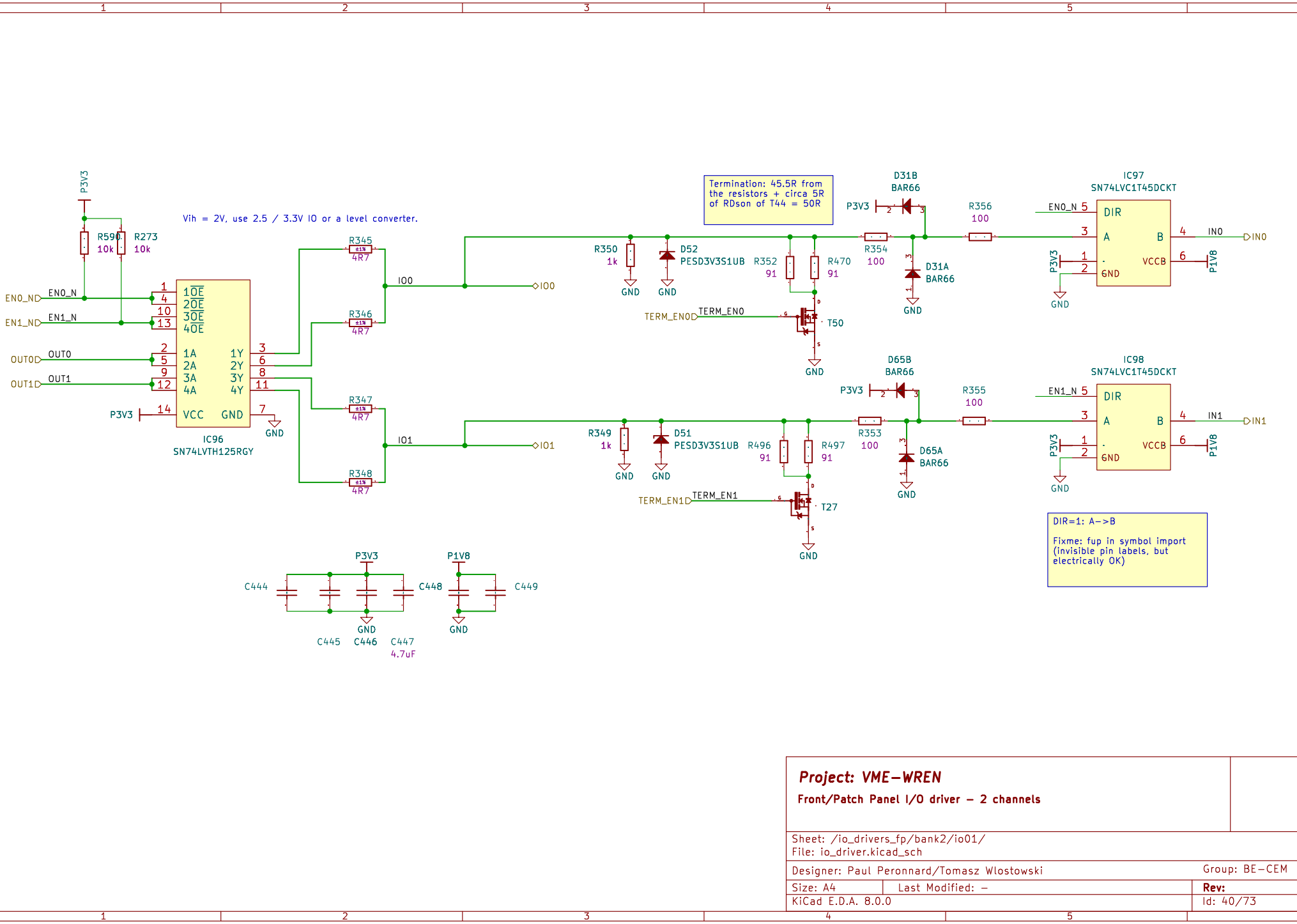
Sheet: /io_drivers_fp/bank2/io34/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 38/73

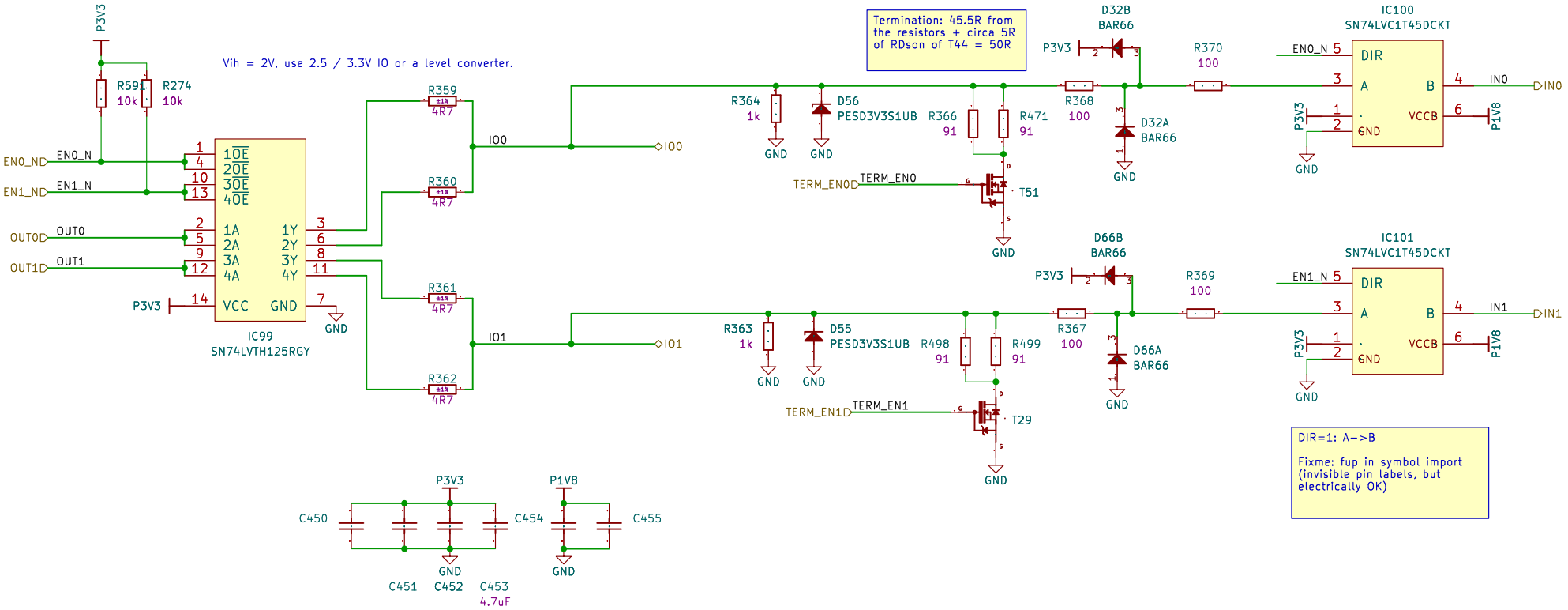


Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

Sheet: /io_drivers_fp/bank2/io56/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 39/73


Vih = 2V, use 2.5 / 3.3V IO or a level converter.
Termination: 45.5R from the resistors + circa 5R of RDson of T44 = 50R
DIR=1: A->B
Fixme: fup in symbol import (invisible pin labels, but electrically OK)
IC96
SN74LVTH125RGY
IC97
SN74LVC1T45DCKT
IC98
SN74LVC1T45DCKT
D52
PESD3V3S1UB
D51
PESD3V3S1UB
D31A
BAR66
D31B
BAR66
D65A
BAR66
D65B
BAR66
T50
T27
R590
10k
R273
10k
R345
4R7
R346
4R7
R347
4R7
R348
4R7
R350
1k
R349
1k
R352
91
R470
91
R496
91
R497
91
R354
100
R353
100
R356
100
R355
100
C444
C445
C446
C447
4.7uF
C448
C449
P3V3
P1V8
GND
IO0
IO1
EN0_N
EN1_N
OUT0
OUT1
TERM_EN0
TERM_EN1
IN0
IN1
Project: VME-WREN
Front/Patch Panel I/O driver - 2 channels
Sheet: /io_drivers_fp/bank2/io01/
File: io_driver.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A4
Last Modified: -
Rev:
KiCad E.D.A. 8.0.0
Id: 40/73



Project: VME-WREN

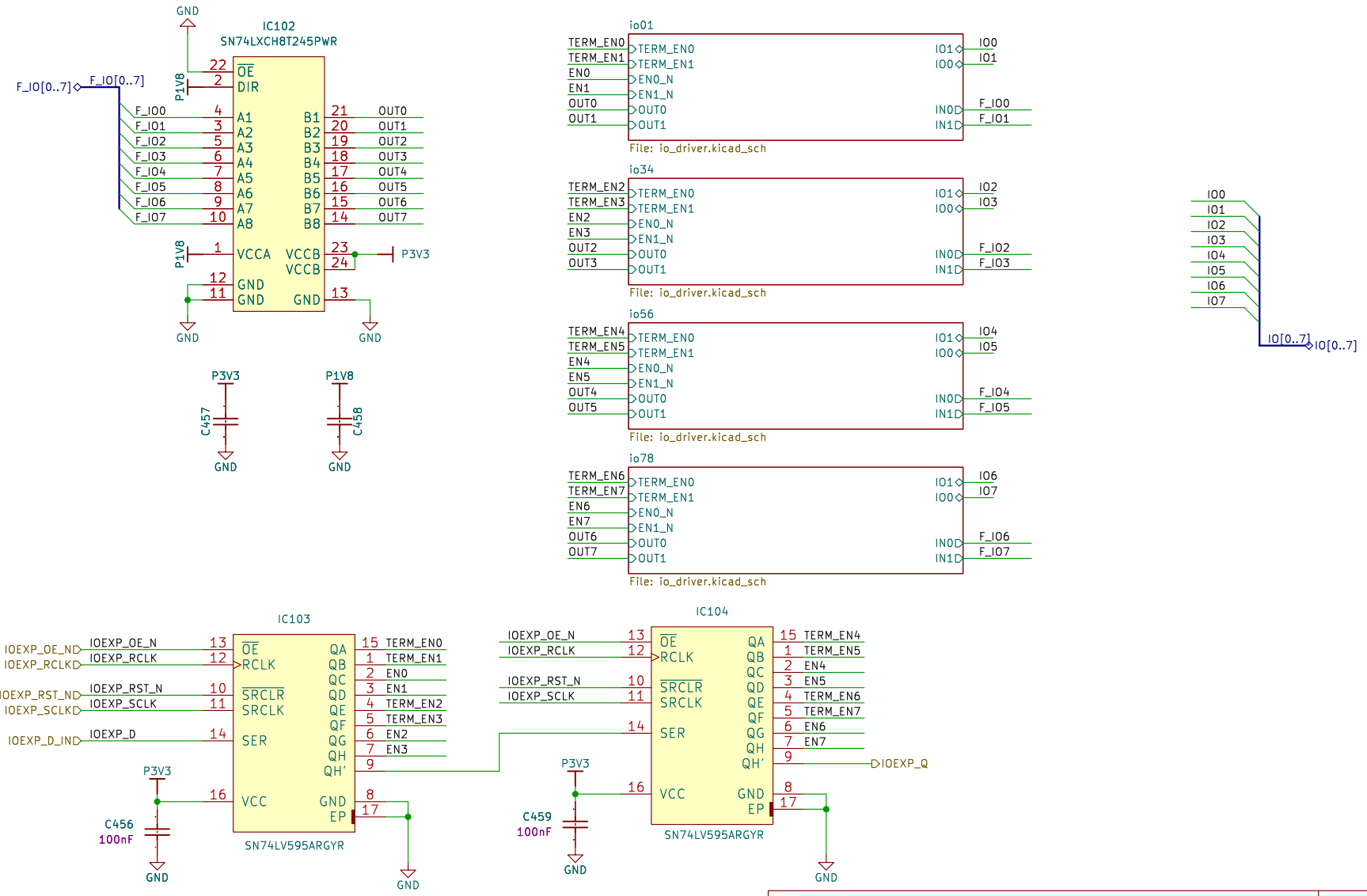
Front/Patch Panel I/O driver - 2 channels

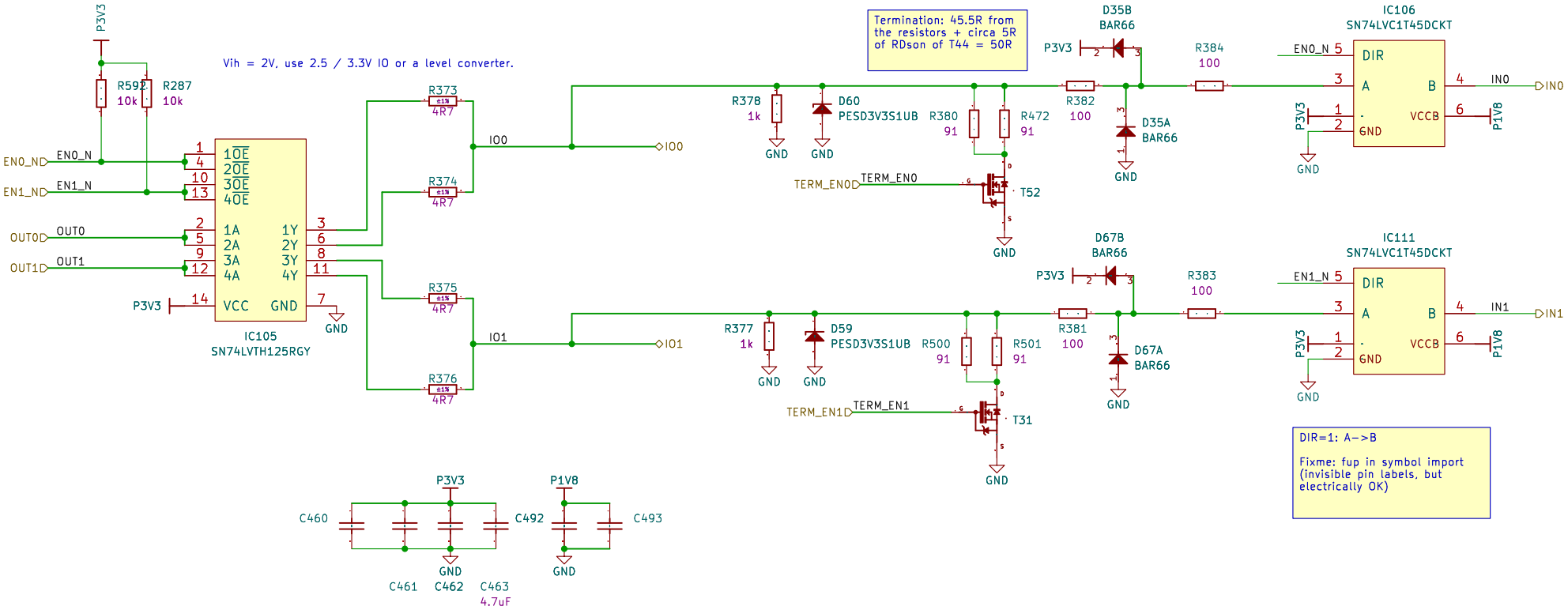
Sheet: /io_drivers_fp/bank2/io78/
File: io_driver.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

Size: A4 — Last Modified: - — **Rev:**

KiCad E.D.A. 8.0.0 — Id: 41/73

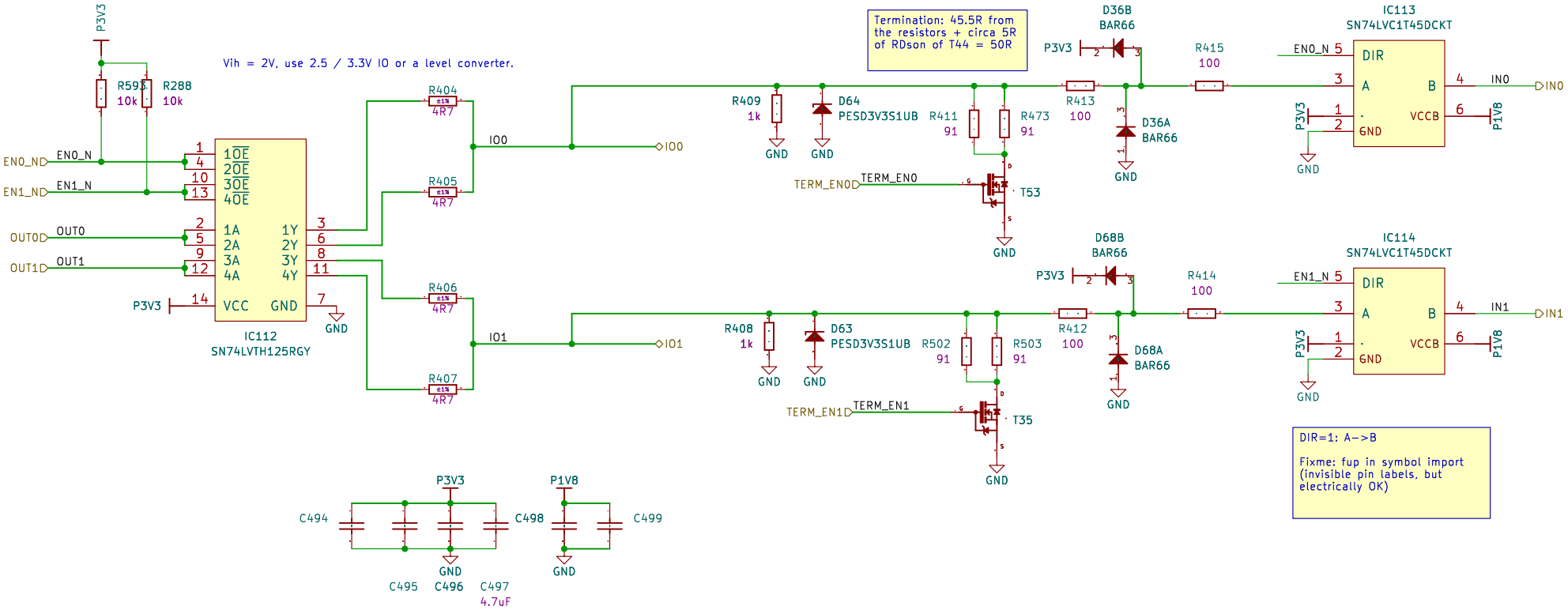

IC102
SN74LXCH8T245PWR
F_IO[0..7]
P1V8
P3V3
GND
C457
C458
io01
io34
io56
io78
File: io_driver.kicad_sch
IO[0..7]
IC103
IC104
SN74LV595ARGYR
IOEXP_OE_N
IOEXP_RCLK
IOEXP_RST_N
IOEXP_SCLK
IOEXP_D_IN
IOEXP_Q
C456
100nF
C459
100nF
Project: VME-WREN
Front/Patch Panel I/O driver - 8 channels
Sheet: /io_drivers_fp/bank3/
File: io_driver_8x.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A4
Last Modified: -
Rev:
KiCad E.D.A. 8.0.0
Id: 42/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

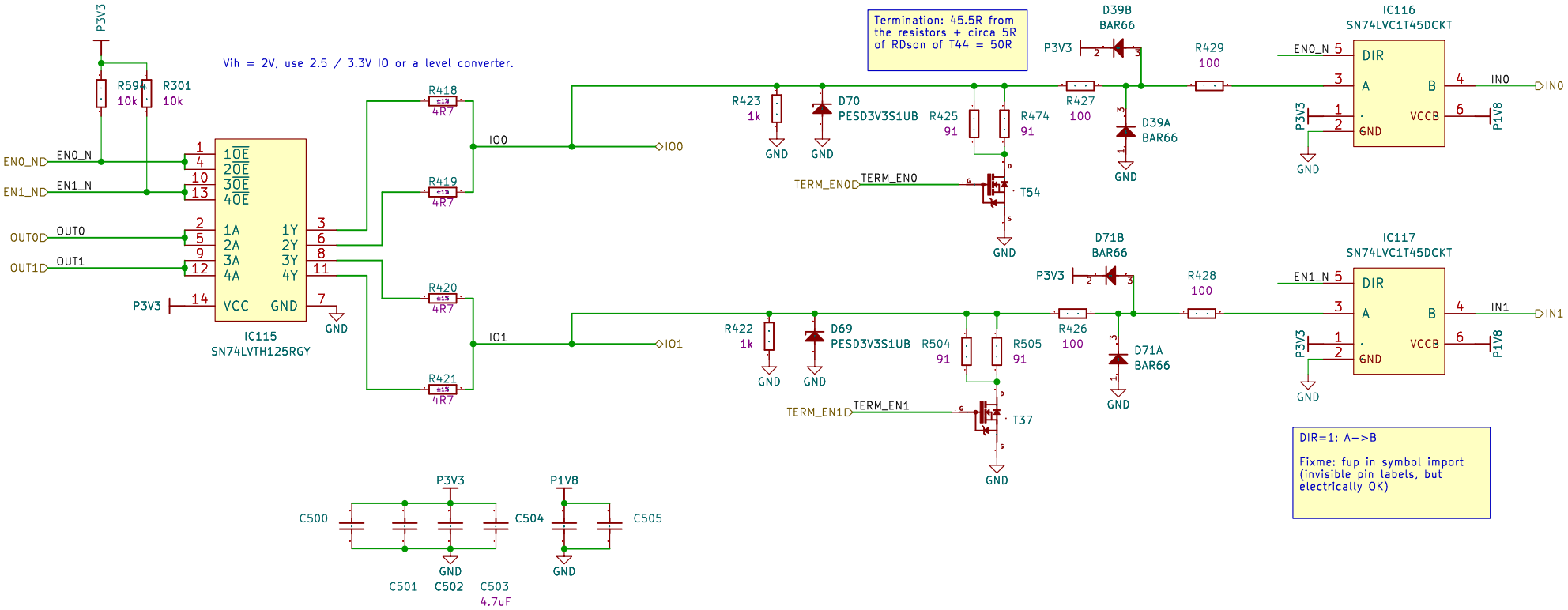
Sheet: /io_drivers_fp/bank3/io01/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 43/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

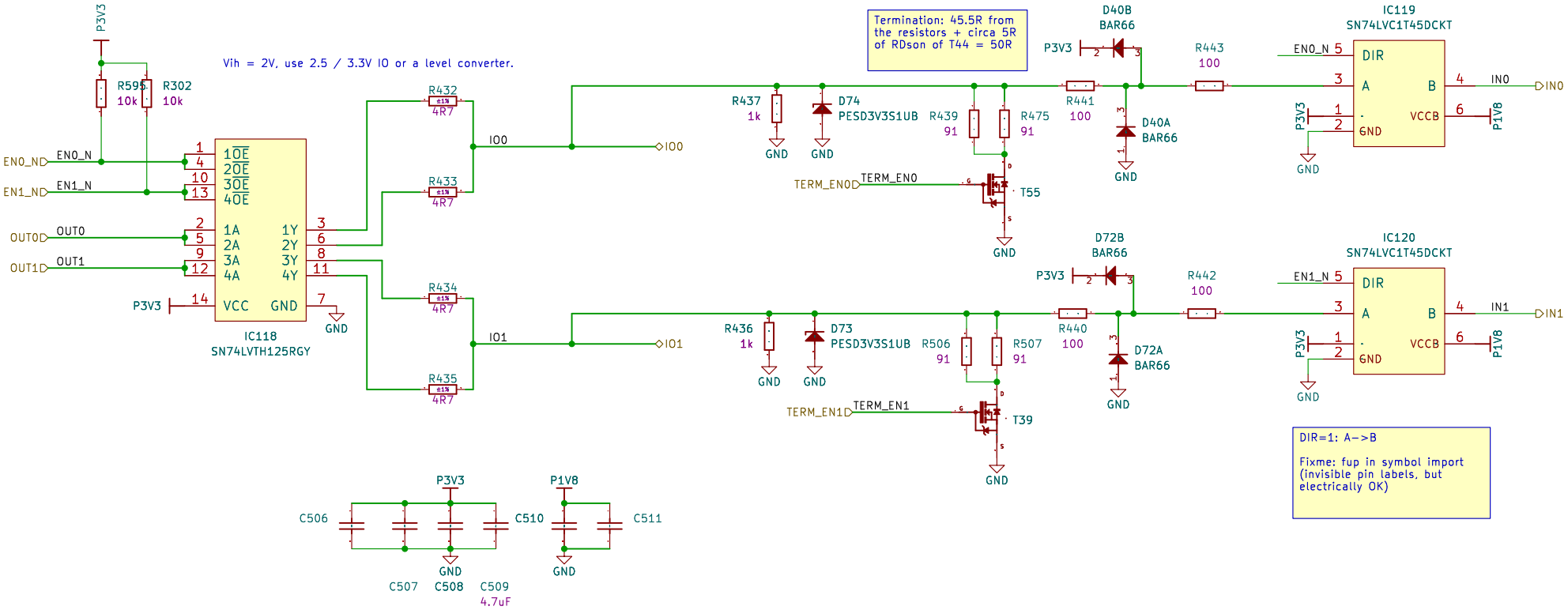
Sheet: /io_drivers_fp/bank3/io56/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 44/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

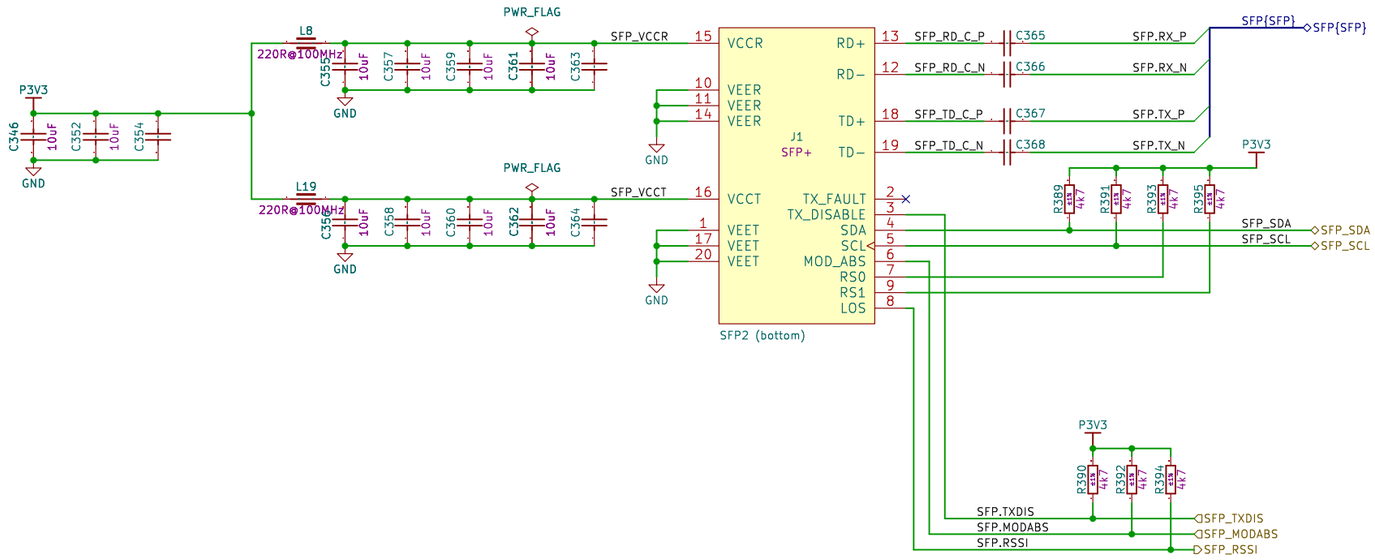
Sheet: /io_drivers_fp/bank3/io78/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 45/73



Project: VME-WREN

Front/Patch Panel I/O driver - 2 channels

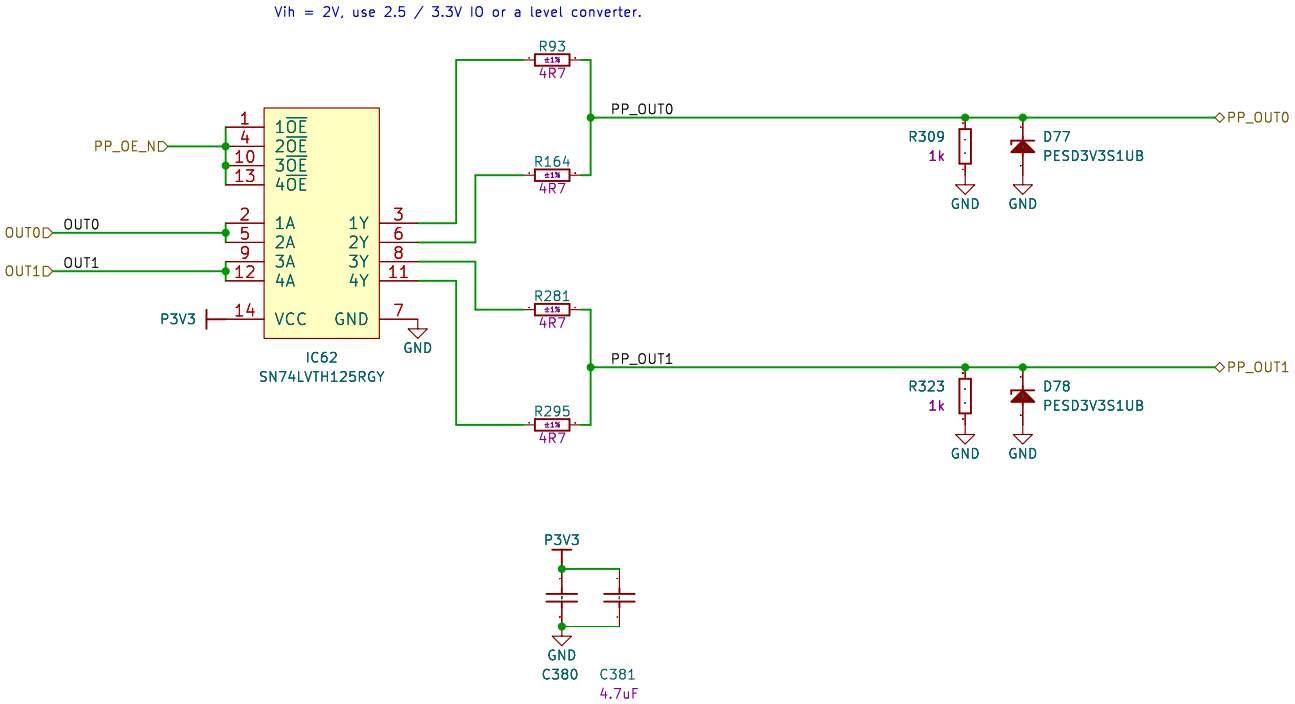
Sheet: /io_drivers_fp/bank3/io34/ File: io_driver.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 46/73



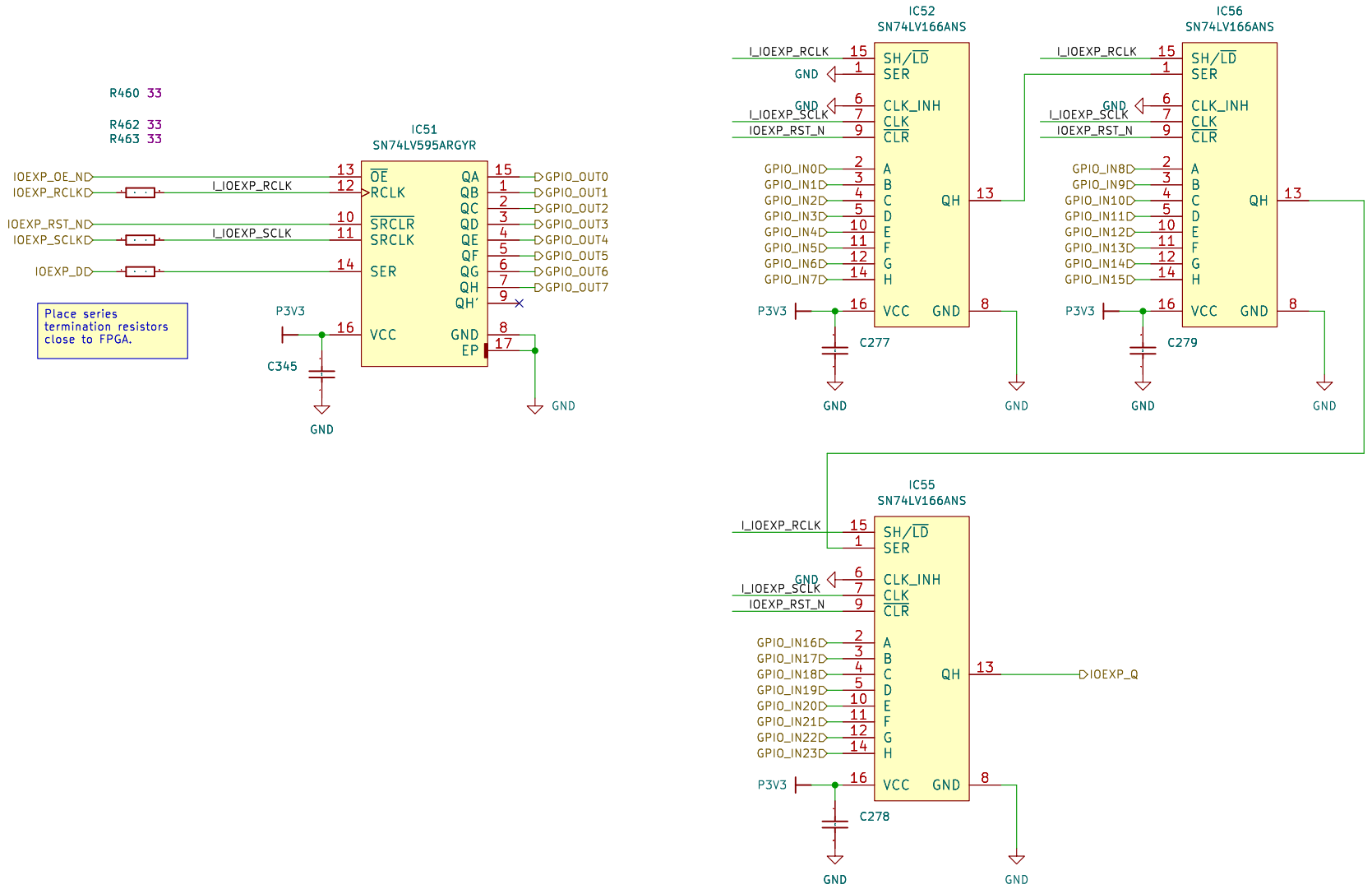
Project: VME−WREN

SFP+ Cage

Sheet: /SFP1/ File: sfp+.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE−CEM
Size: A3	Last Modified: −	**Rev: −**
KiCad E.D.A. 8.0.0		Id: 47/73



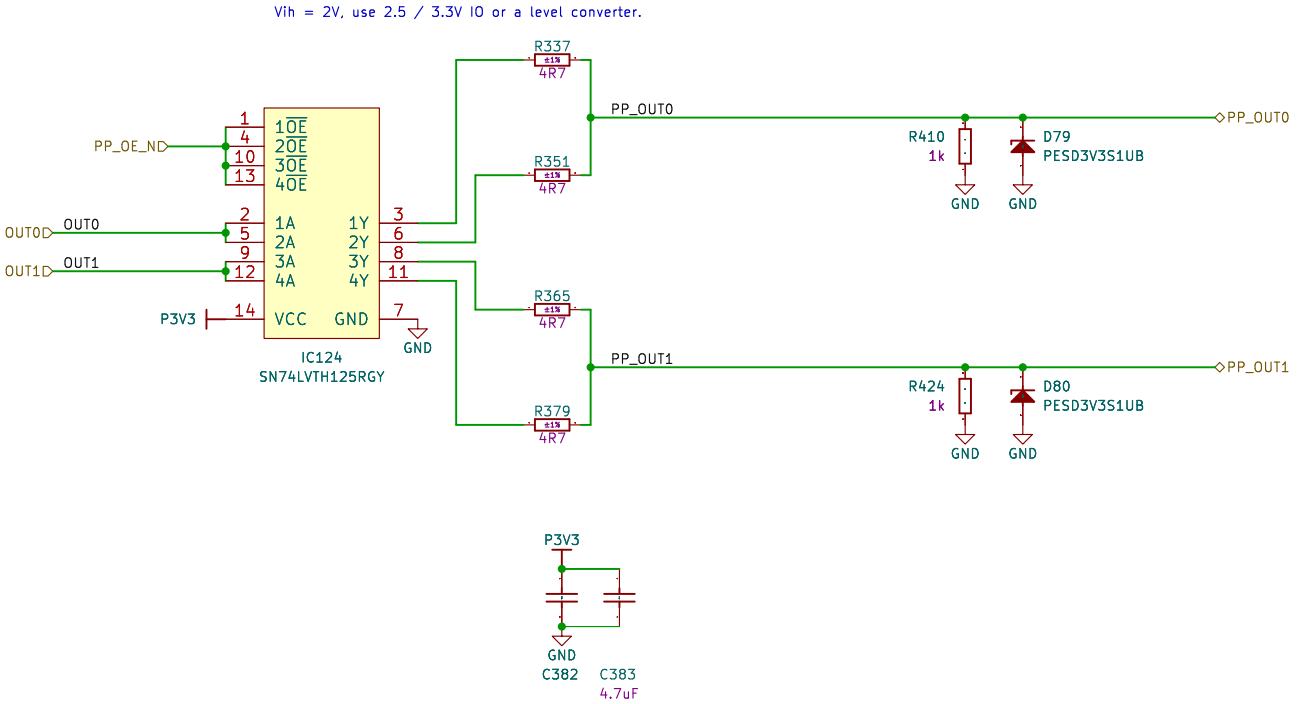
Project: VME-WREN	
Sheet: /io_drivers_pp/bank0/out01/ File: pp_driver_2x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0	Id: 48/73



Project: VME-WREN

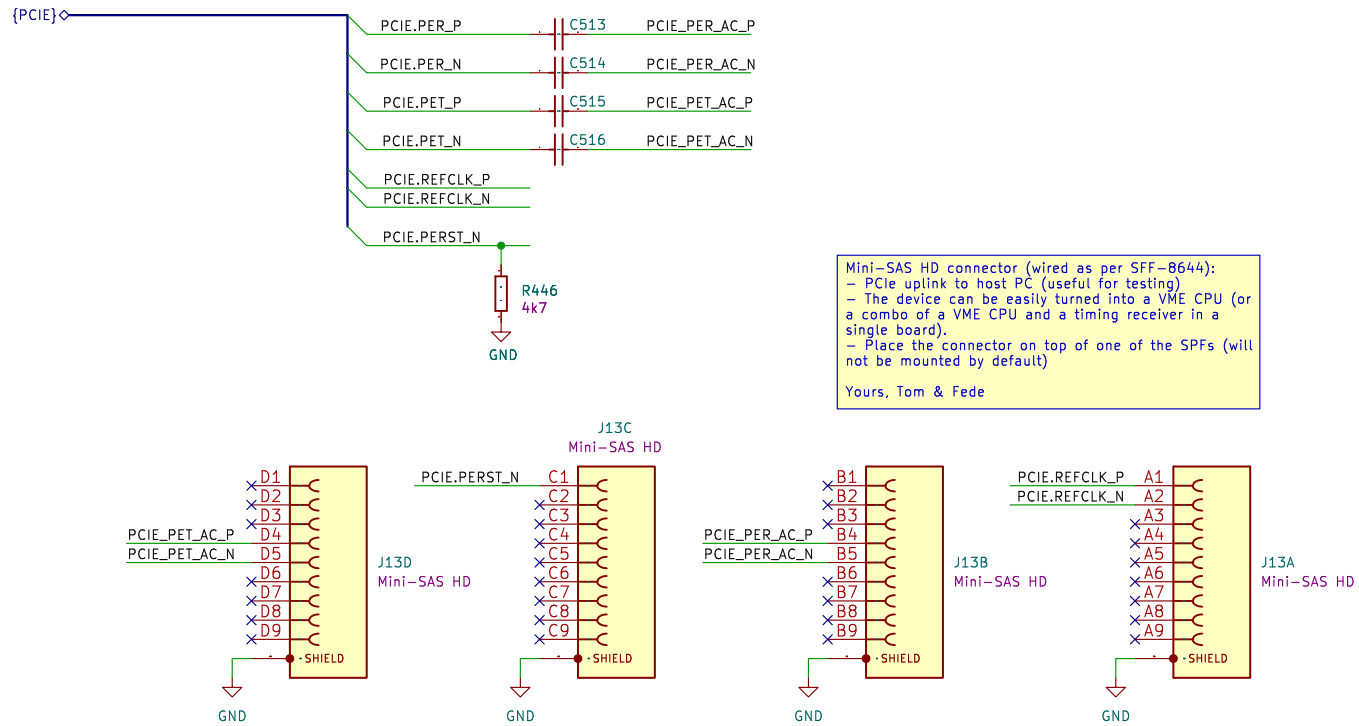
"Slow" GPIO pins

Sheet: /slow_gpio/ File: slow_gpio.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: –	**Rev:**
KiCad E.D.A. 8.0.0	Id: 49/73



Project: VME-WREN

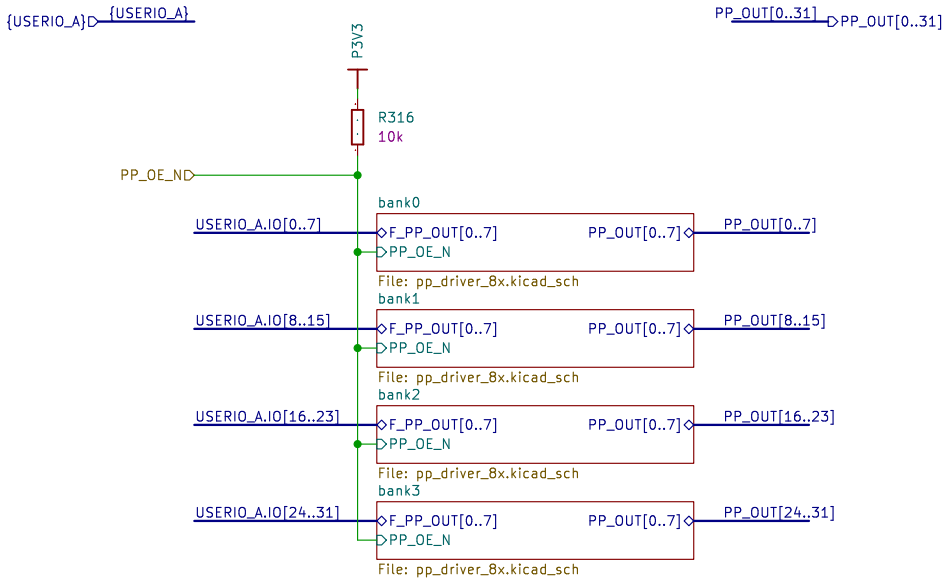
Sheet: /io_drivers_pp/bank0/out23/	
File: pp_driver_2x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: –	**Rev:**
KiCad E.D.A. 8.0.0	Id: 50/73



Project: VME-WREN

PCI Express Port (SFF-8466)

Sheet: /pcie_connector/ File: pcie_connector.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 51/73



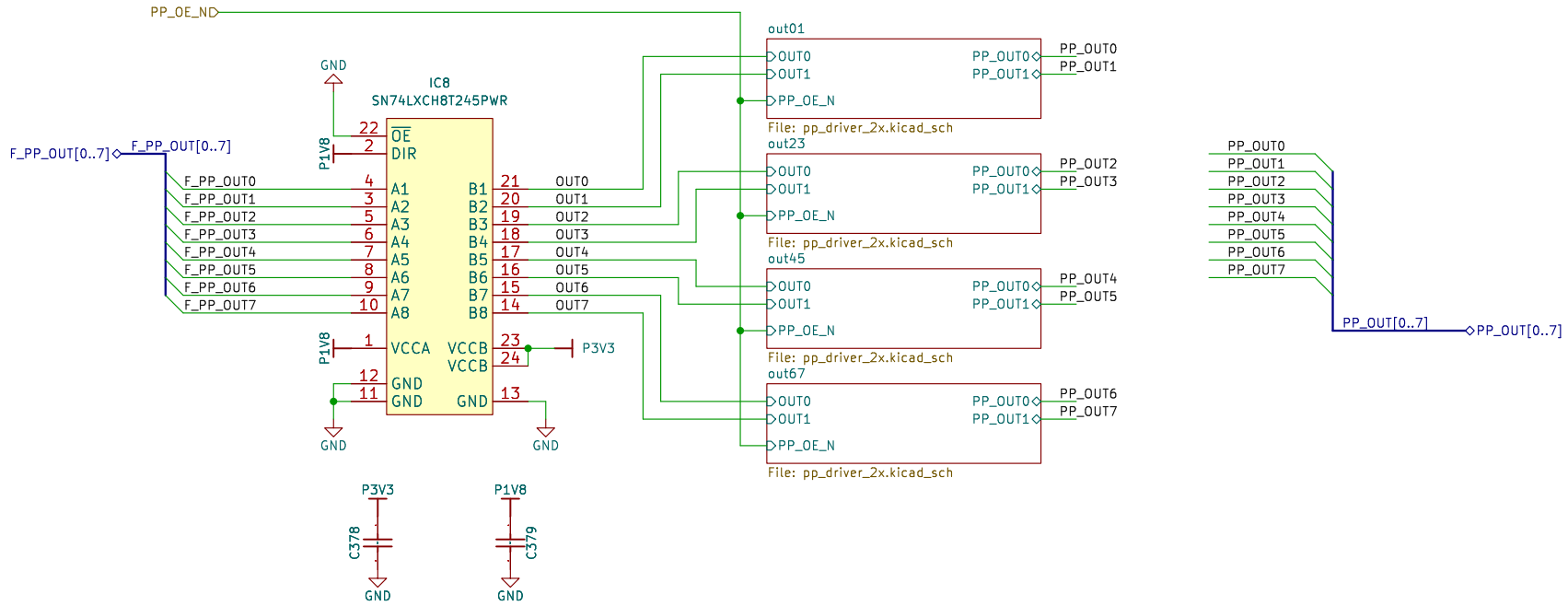
Project: VME-WREN

Sheet: /io_drivers_pp/
File: pp_driver_32x.kicad_sch

Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

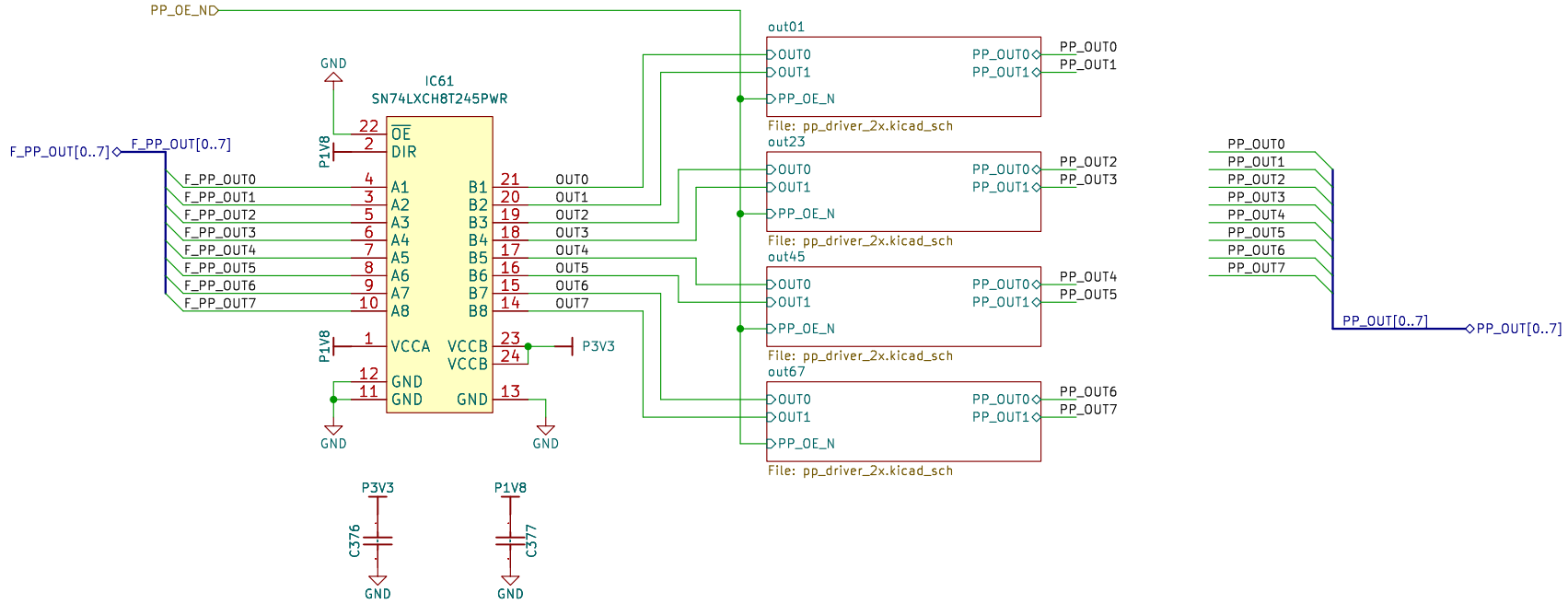
Size: A4 — Last Modified: – — **Rev:**

KiCad E.D.A. 8.0.0 — Id: 52/73



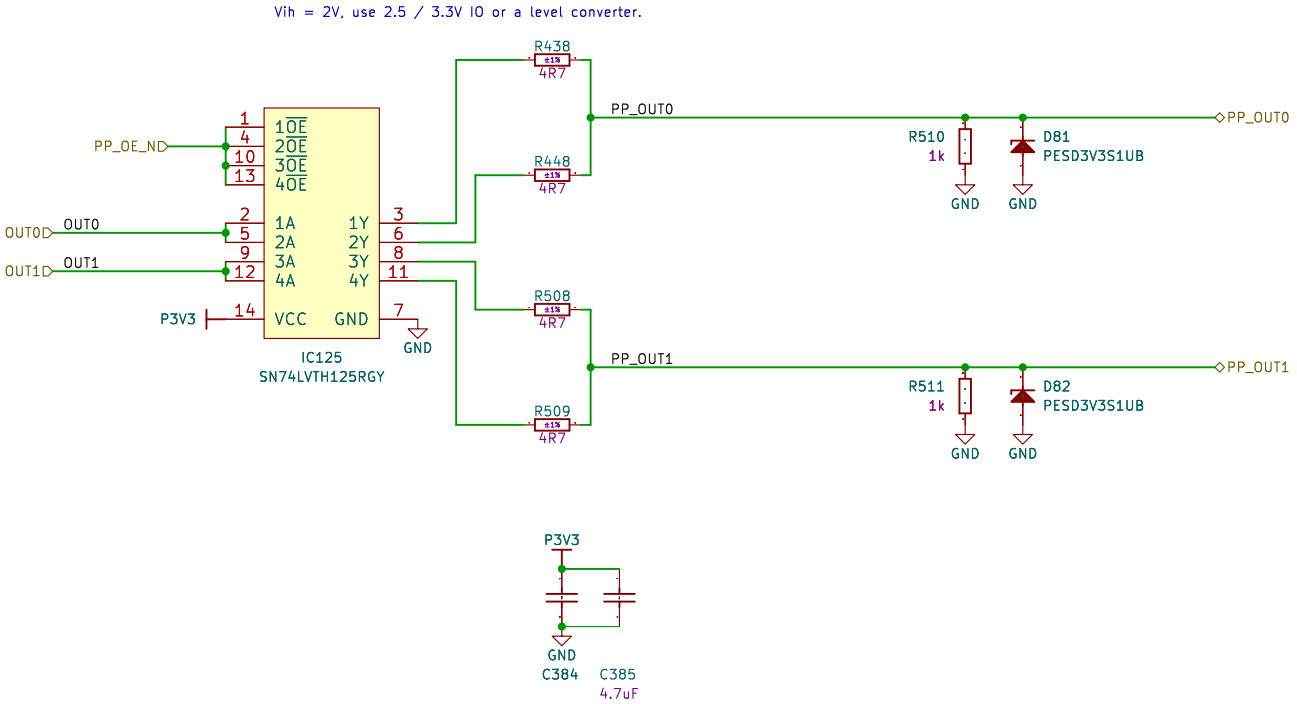
Project: VME-WREN

Sheet: /io_drivers_pp/bank1/ File: pp_driver_8x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 53/73

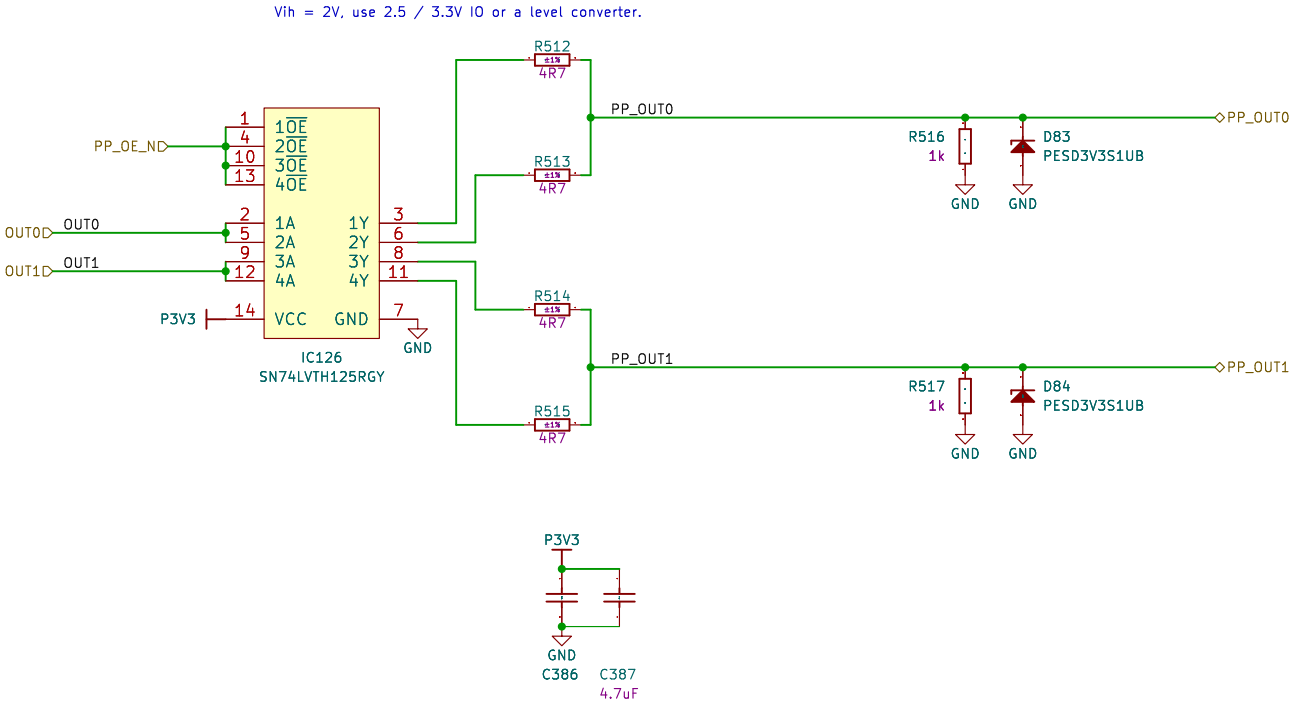


Project: VME-WREN

Sheet: /io_drivers_pp/bank0/ File: pp_driver_8x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 54/73



Project: VME-WREN	
Sheet: /io_drivers_pp/bank0/out45/ File: pp_driver_2x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0	Id: 55/73



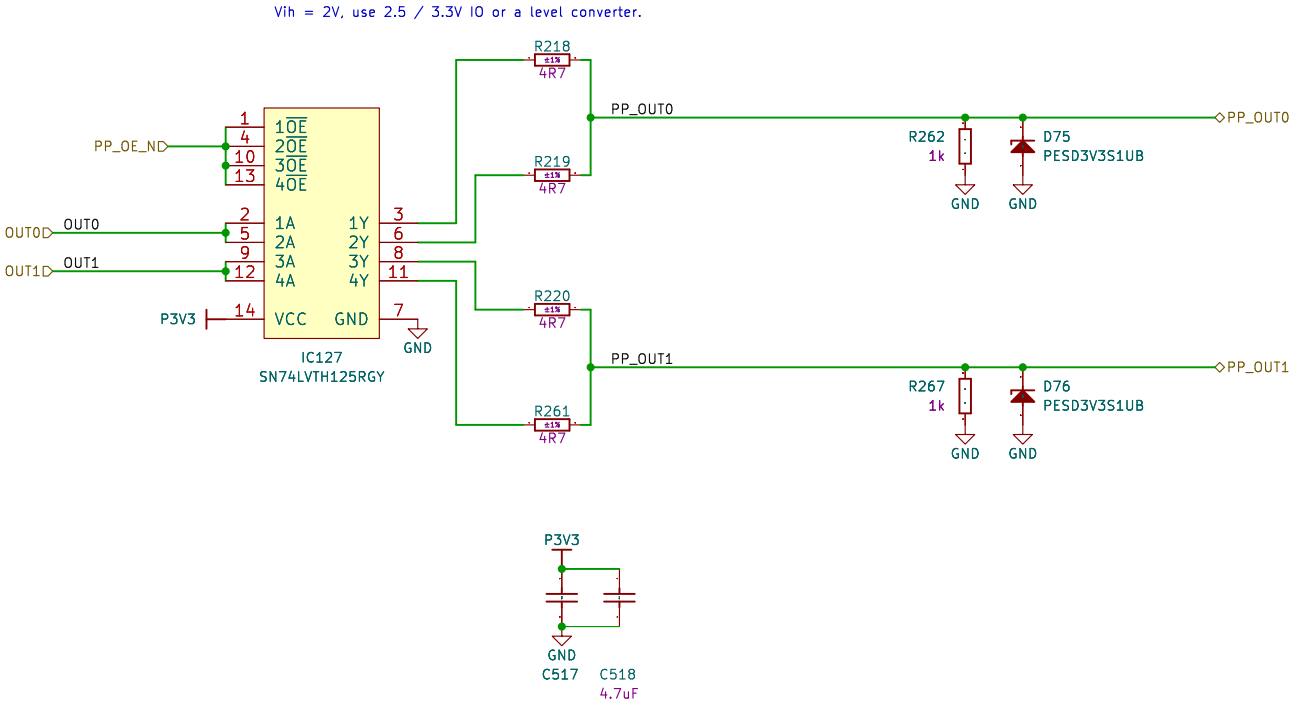
Project: VME-WREN

Sheet: /io_drivers_pp/bank0/out67/
File: pp_driver_2x.kicad_sch

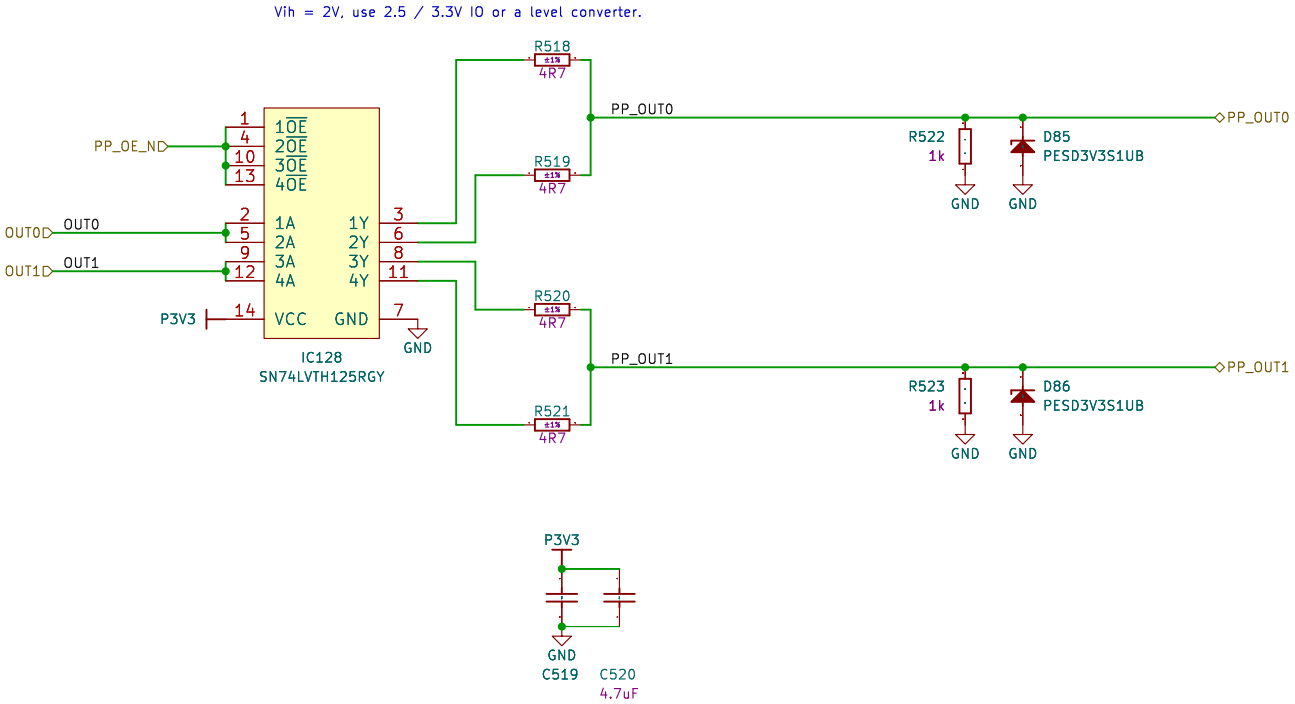
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM

Size: A4
Last Modified: -
Rev:

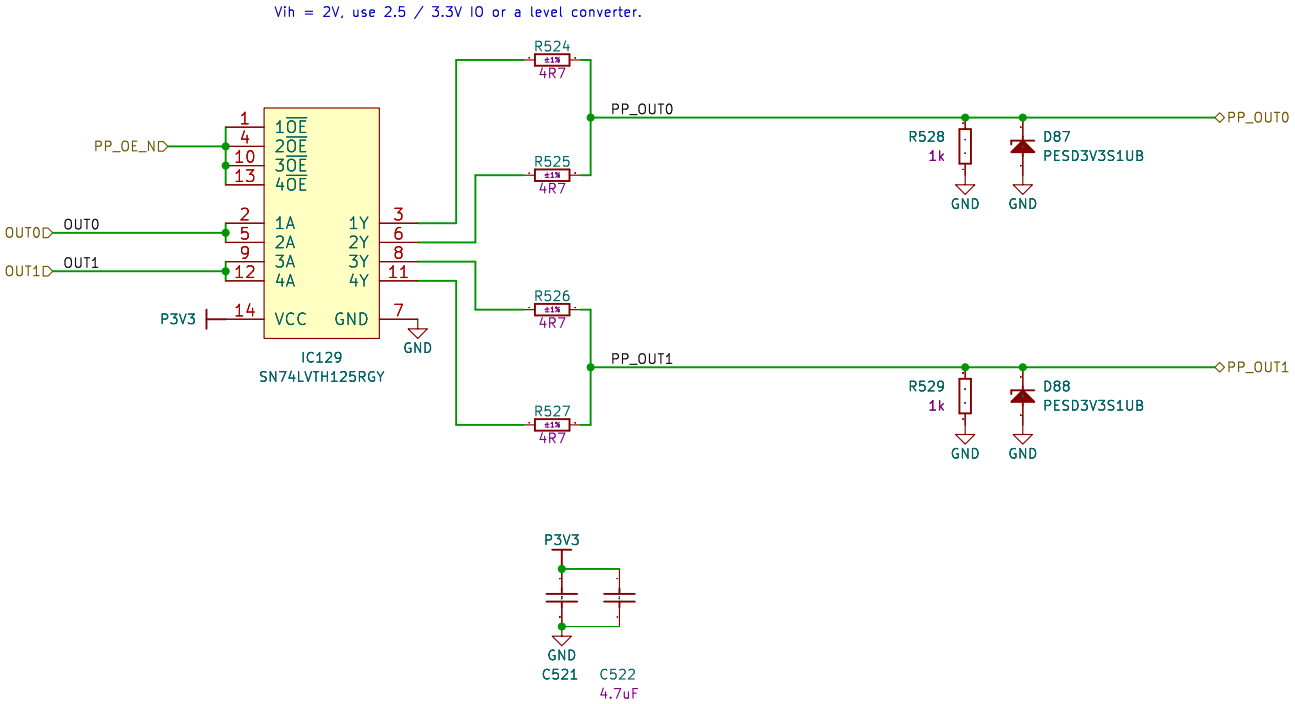
KiCad E.D.A. 8.0.0
Id: 56/73



Project: VME-WREN		
Sheet: /io_drivers_pp/bank1/out23/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 57/73



Project: VME-WREN		
Sheet: /io_drivers_pp/bank1/out45/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 58/73



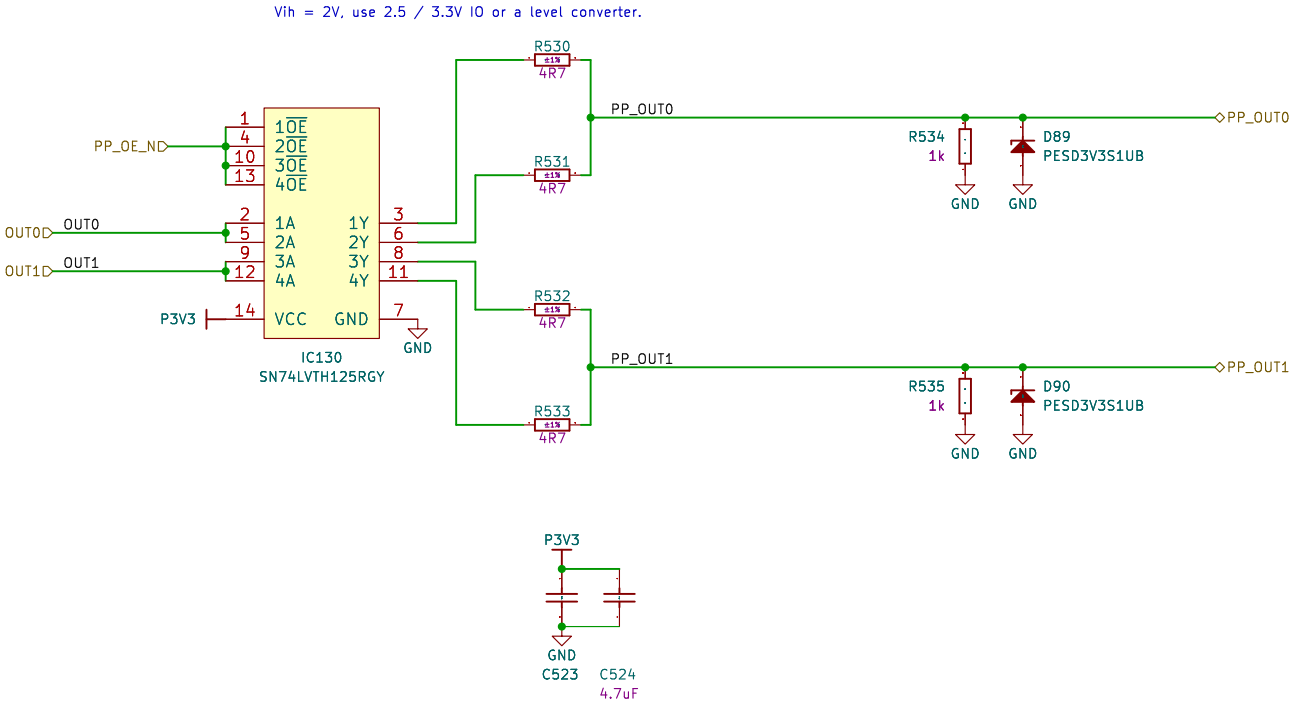
Project: VME-WREN

Sheet: /io_drivers_pp/bank1/out67/
File: pp_driver_2x.kicad_sch

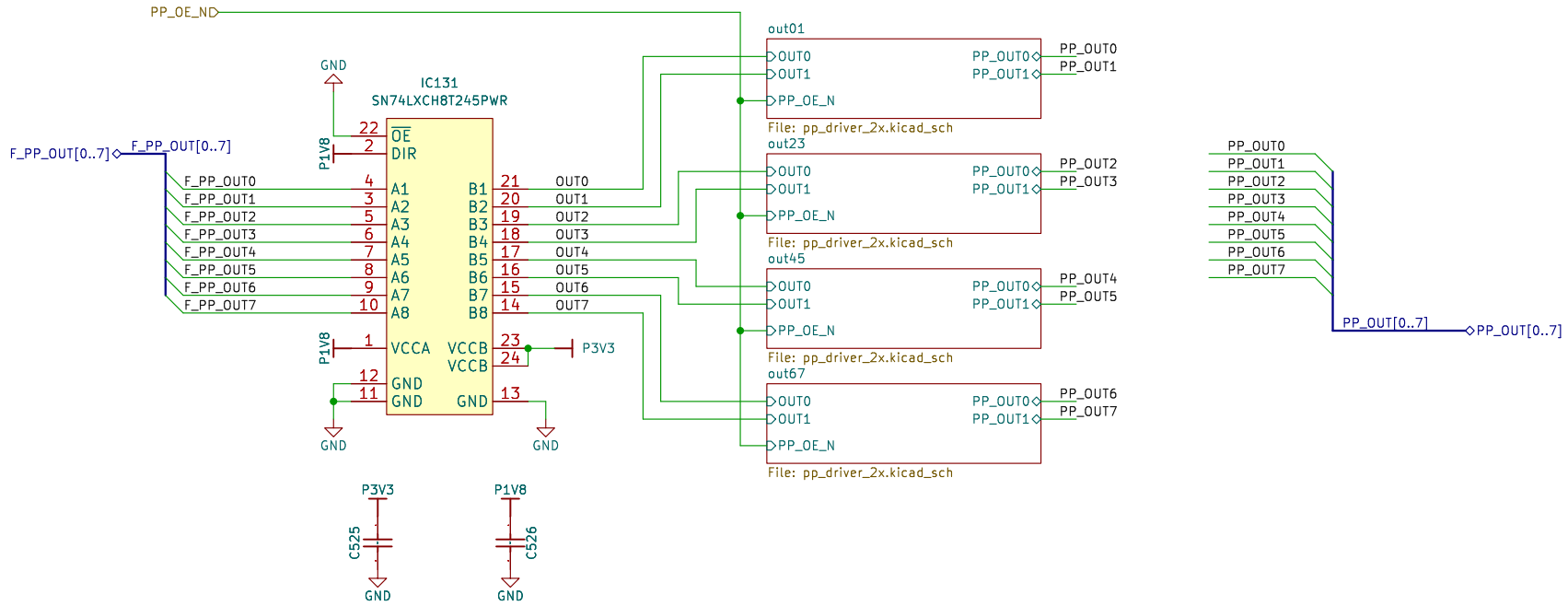
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM

Size: A4
Last Modified: -
Rev:

KiCad E.D.A. 8.0.0
Id: 59/73

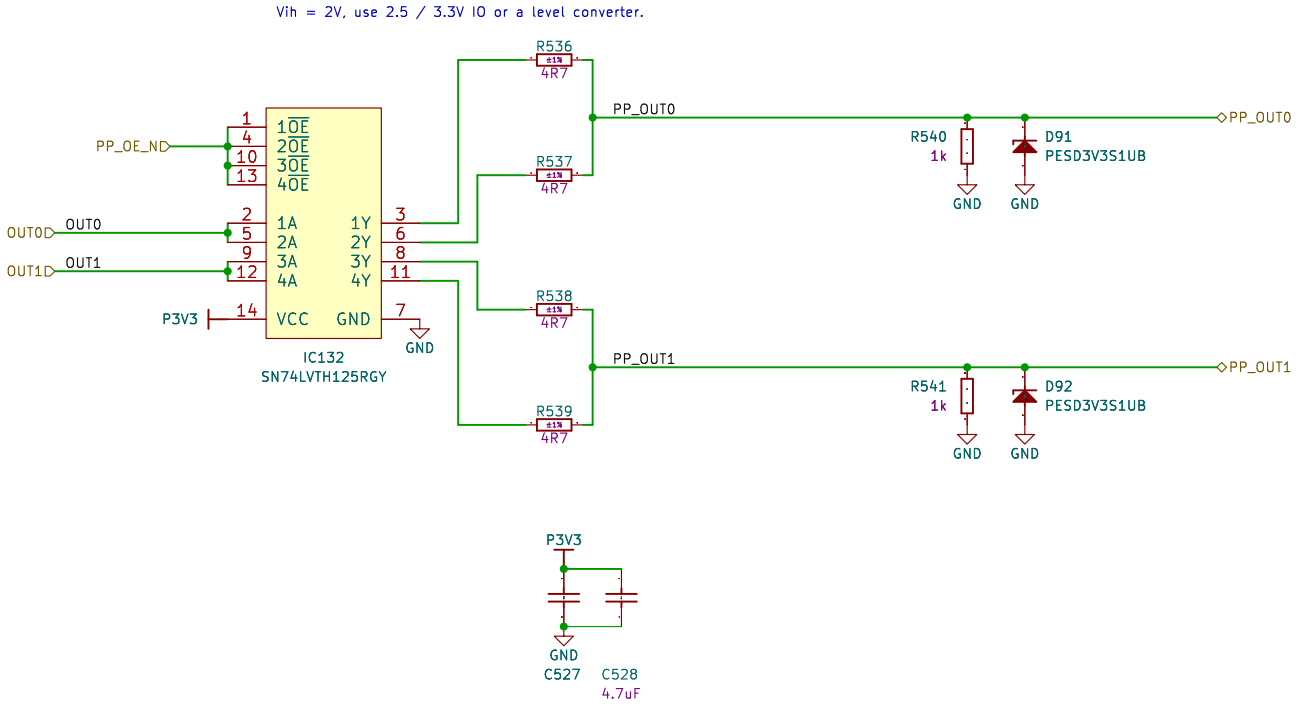


Project: VME-WREN		
Sheet: /io_drivers_pp/bank1/out01/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 60/73

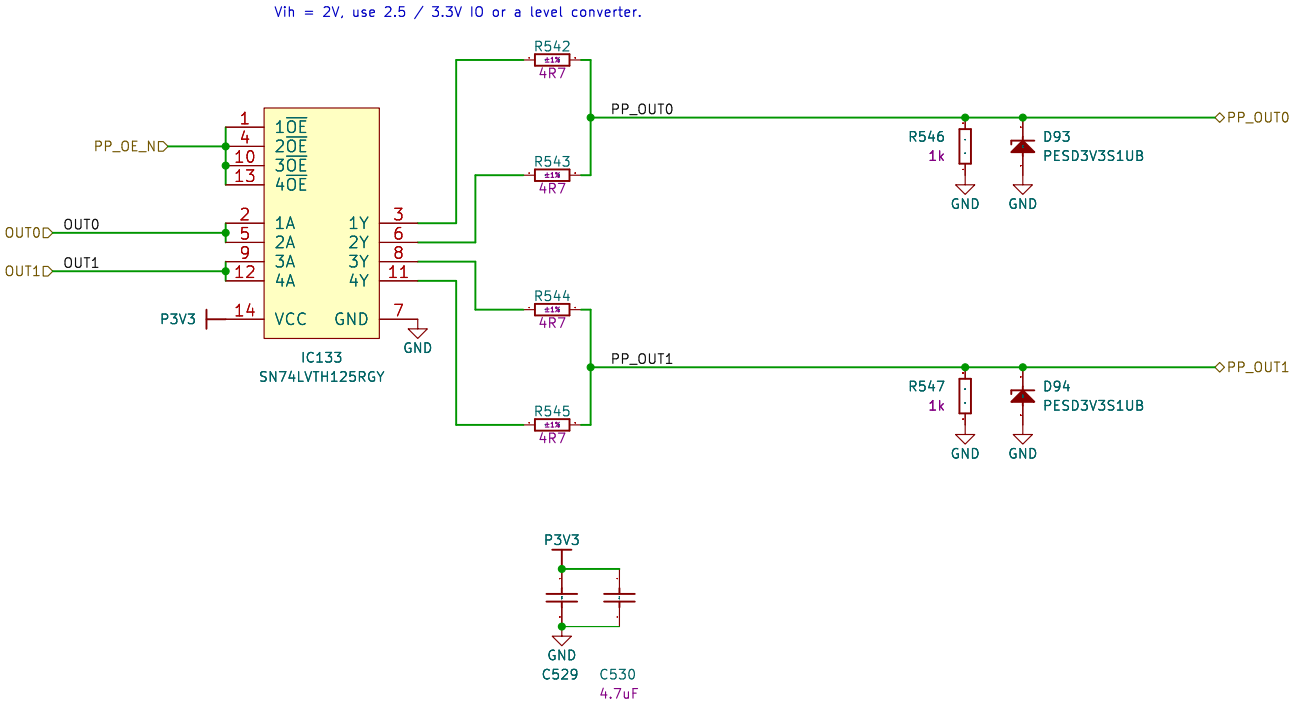


Project: VME-WREN

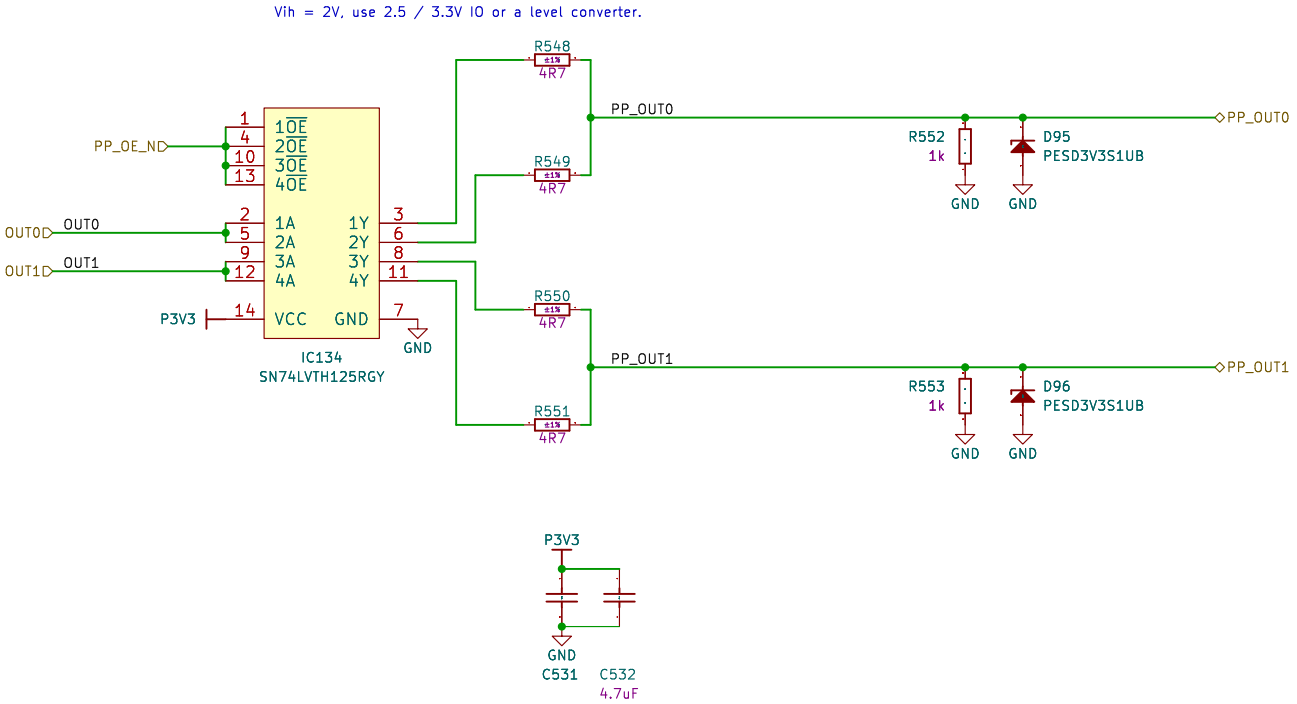
Sheet: /io_drivers_pp/bank2/ File: pp_driver_8x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0	Id: 61/73



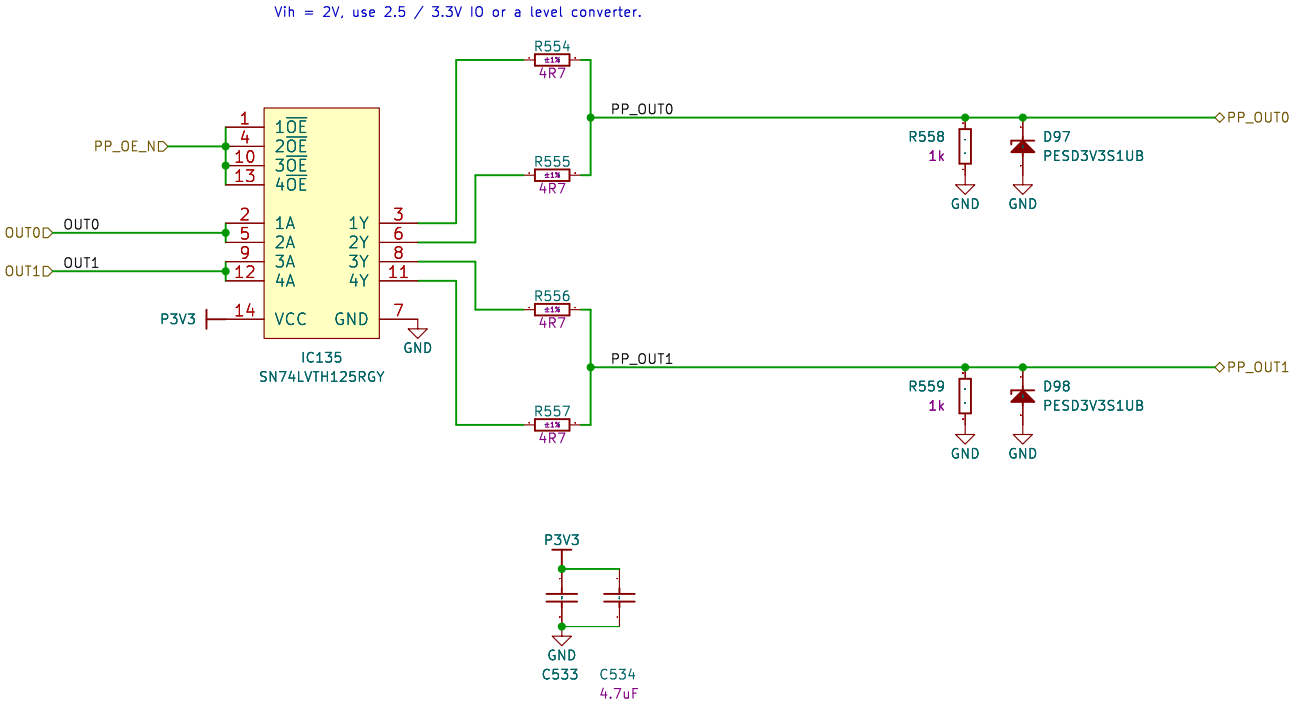
Project: VME-WREN		
Sheet: /io_drivers_pp/bank2/out23/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 62/73



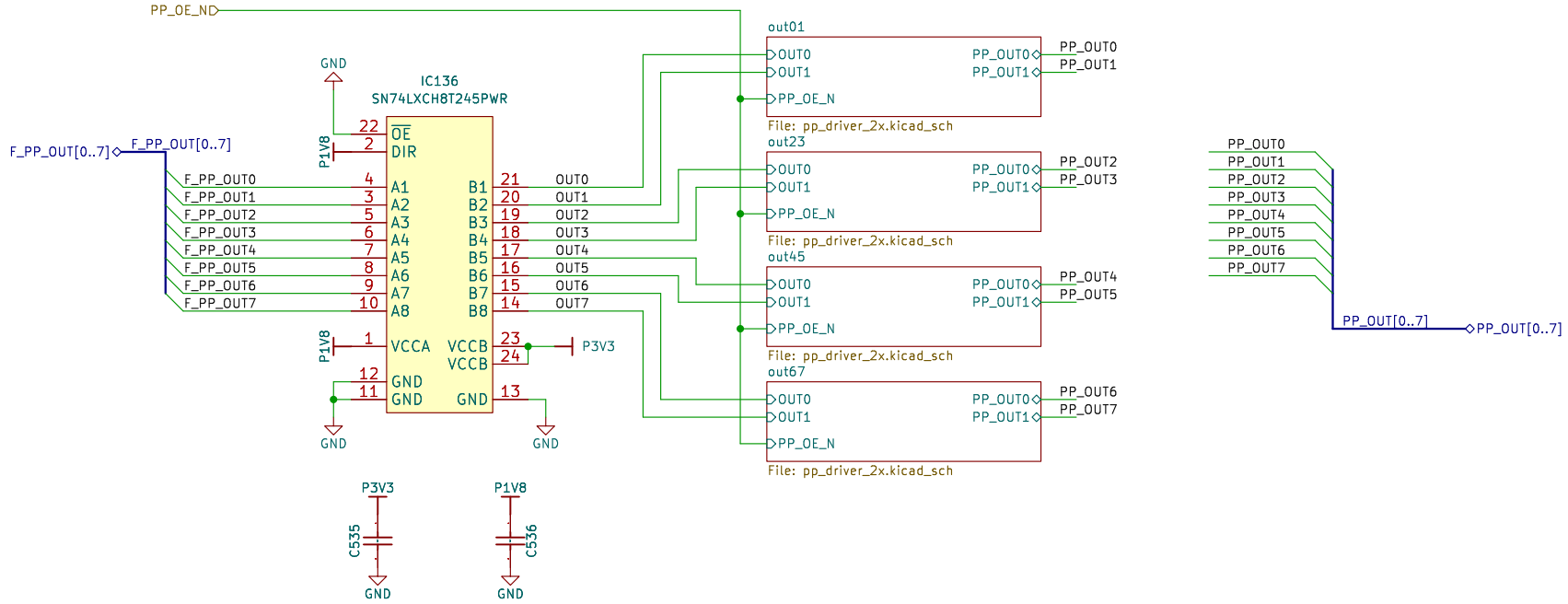
Project: VME-WREN		
Sheet: /io_drivers_pp/bank2/out01/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 63/73



Project: VME-WREN		
Sheet: /io_drivers_pp/bank2/out67/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 64/73

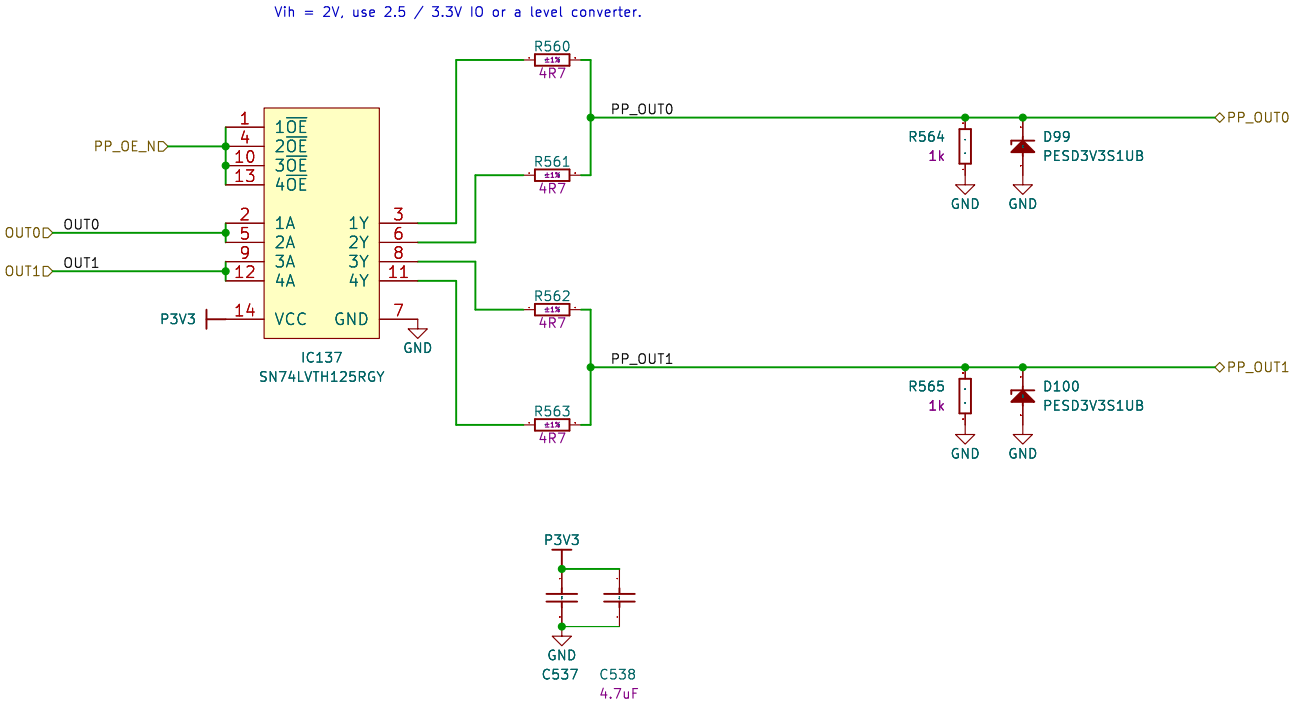


Project: VME-WREN		
Sheet: /io_drivers_pp/bank2/out45/ File: pp_driver_2x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 65/73

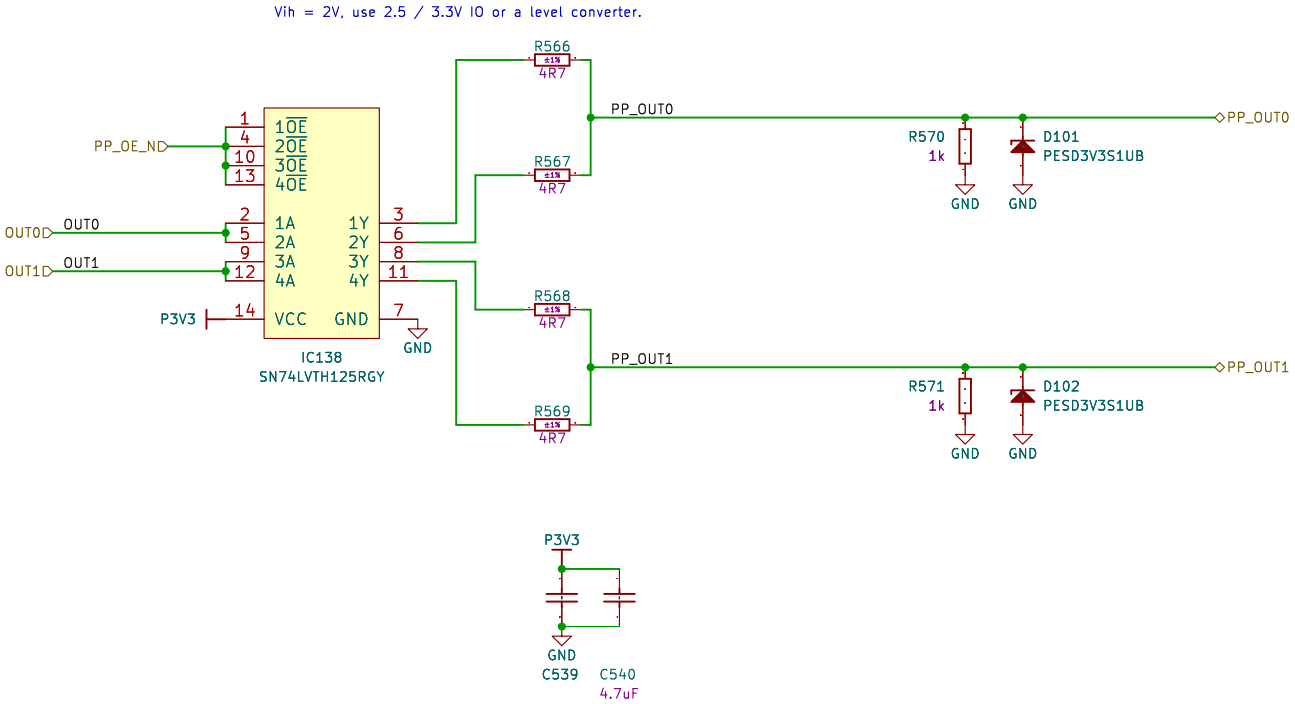


Project: VME-WREN

Sheet: /io_drivers_pp/bank3/ File: pp_driver_8x.kicad_sch		
Designer: Paul Peronnard/Tomasz Wlostowski		Group: BE-CEM
Size: A4	Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0		Id: 66/73



Project: VME-WREN	
Sheet: /io_drivers_pp/bank3/out67/ File: pp_driver_2x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0	Id: 67/73



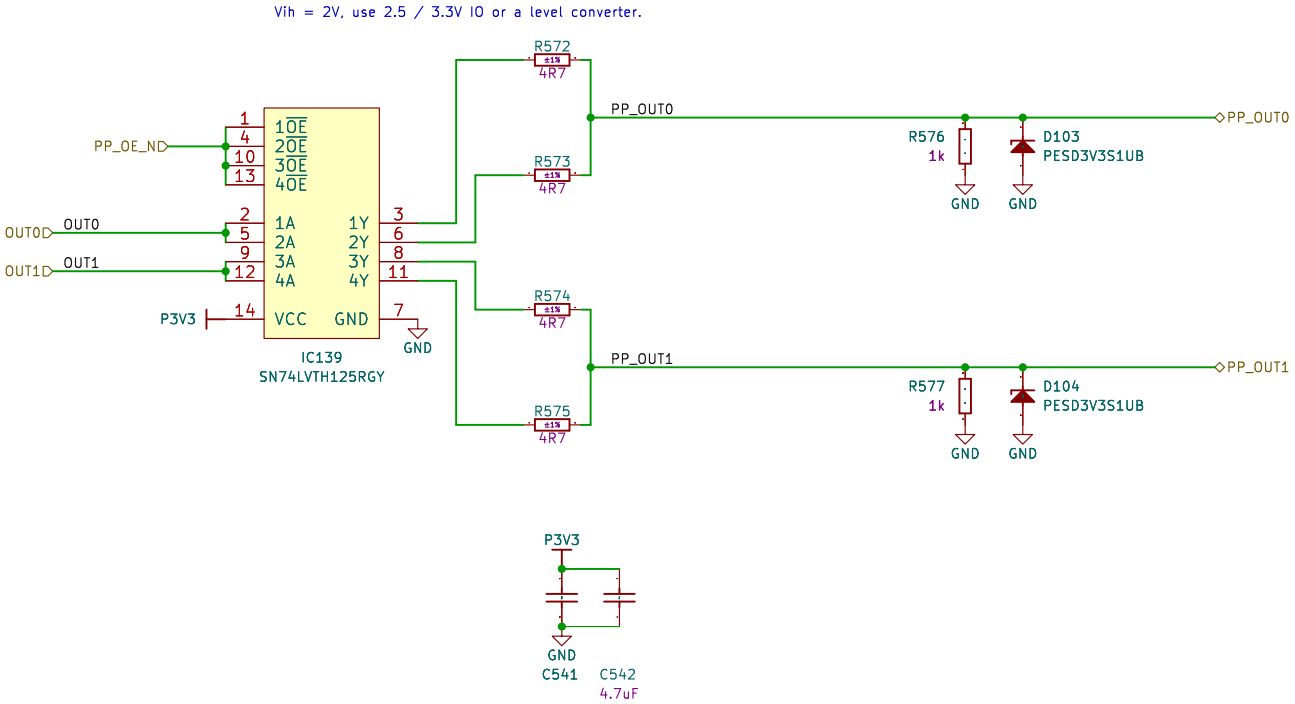
Project: VME-WREN

Sheet: /io_drivers_pp/bank3/out45/
File: pp_driver_2x.kicad_sch

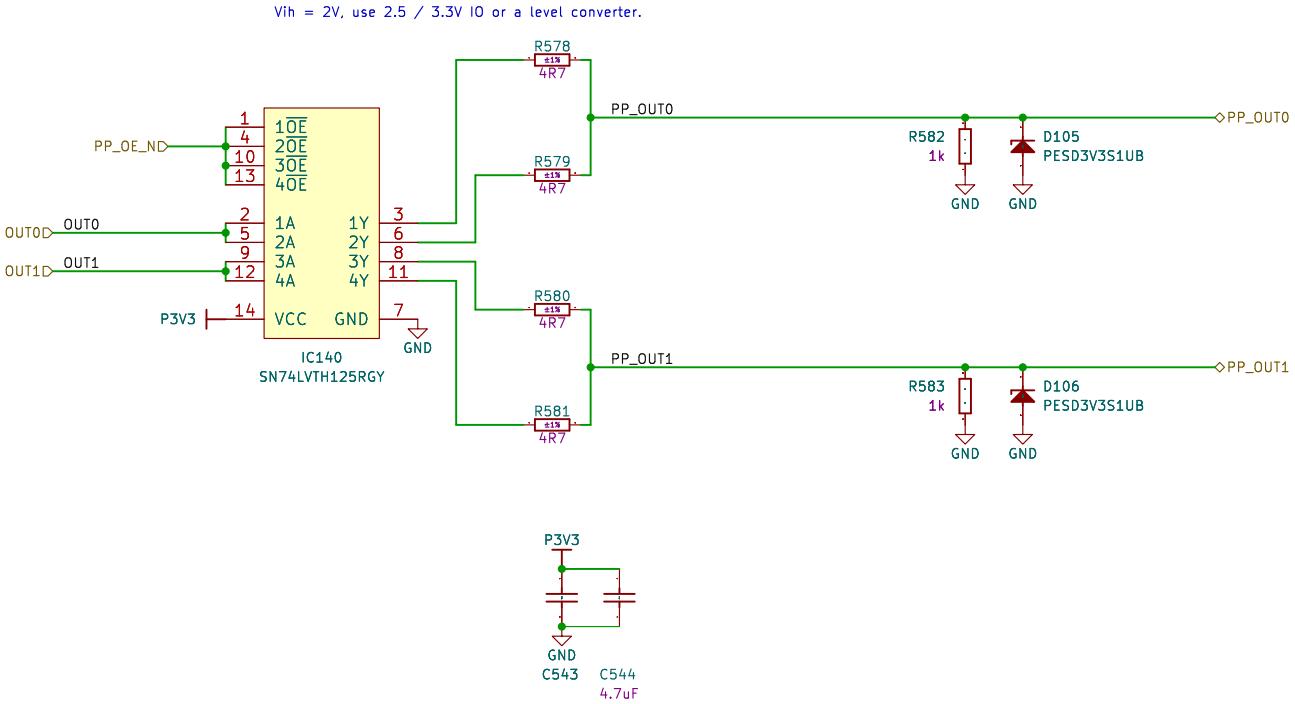
Designer: Paul Peronnard/Tomasz Wlostowski — Group: BE-CEM

Size: A4 — Last Modified: – — **Rev:**

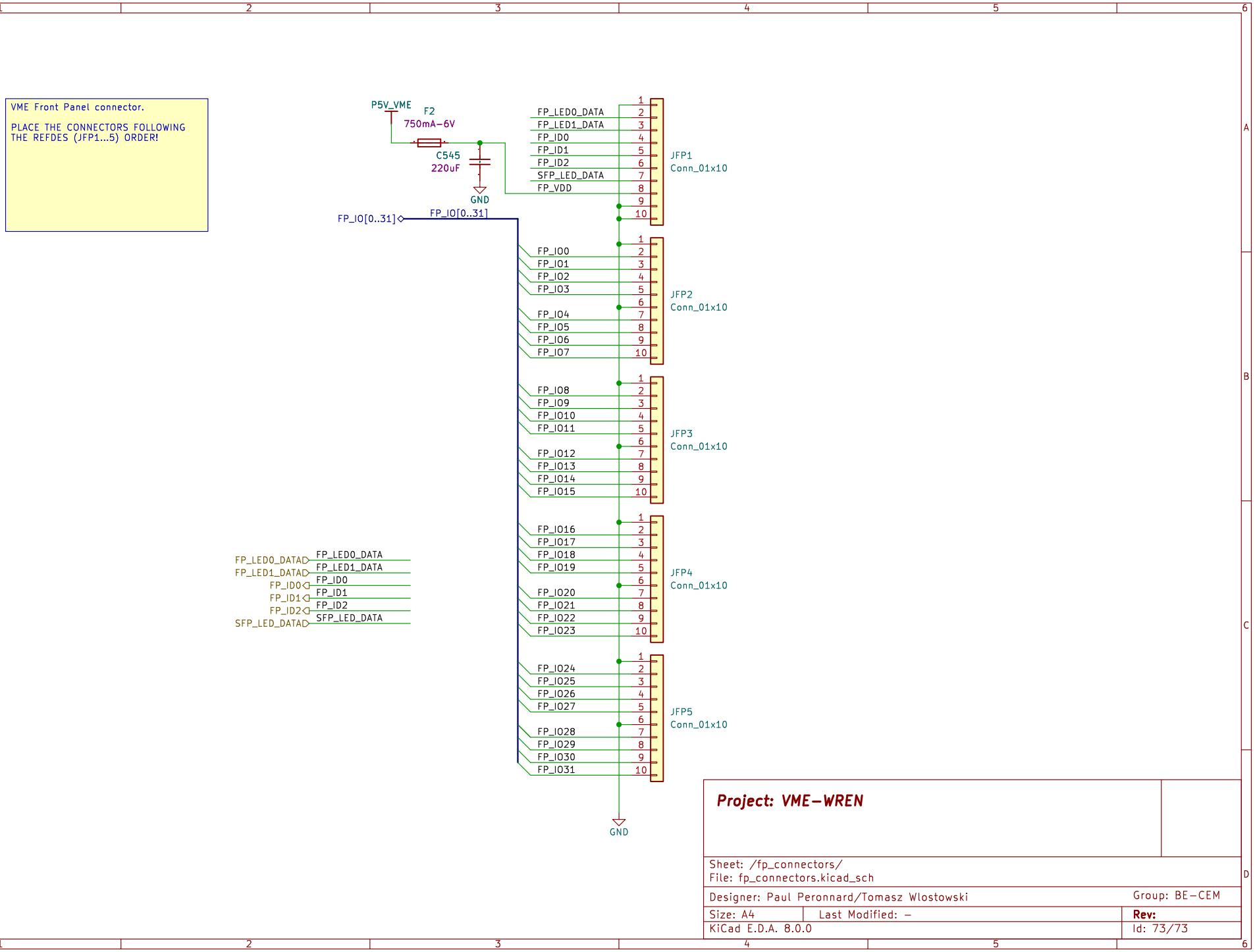
KiCad E.D.A. 8.0.0 — Id: 68/73



Project: VME-WREN	
Sheet: /io_drivers_pp/bank3/out01/ File: pp_driver_2x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: -	**Rev:**
KiCad E.D.A. 8.0.0	Id: 69/73



Project: VME-WREN	
Sheet: /io_drivers_pp/bank3/out23/ File: pp_driver_2x.kicad_sch	
Designer: Paul Peronnard/Tomasz Wlostowski	Group: BE-CEM
Size: A4 | Last Modified: –	**Rev:**
KiCad E.D.A. 8.0.0	Id: 70/73


VME Front Panel connector.
PLACE THE CONNECTORS FOLLOWING THE REFDES (JFP1...5) ORDER!
P5V_VME
F2
750mA-6V
C545
220uF
GND
FP_IO[0..31]
FP_IO[0..31]
FP_LED0_DATA
FP_LED1_DATA
FP_ID0
FP_ID1
FP_ID2
SFP_LED_DATA
FP_VDD
JFP1
Conn_01x10
FP_IO0
FP_IO1
FP_IO2
FP_IO3
FP_IO4
FP_IO5
FP_IO6
FP_IO7
JFP2
Conn_01x10
FP_IO8
FP_IO9
FP_IO10
FP_IO11
FP_IO12
FP_IO13
FP_IO14
FP_IO15
JFP3
Conn_01x10
FP_IO16
FP_IO17
FP_IO18
FP_IO19
FP_IO20
FP_IO21
FP_IO22
FP_IO23
JFP4
Conn_01x10
FP_IO24
FP_IO25
FP_IO26
FP_IO27
FP_IO28
FP_IO29
FP_IO30
FP_IO31
JFP5
Conn_01x10
GND
FP_LED0_DATA
FP_LED1_DATA
FP_ID0
FP_ID1
FP_ID2
SFP_LED_DATA
Project: VME-WREN
Sheet: /fp_connectors/
File: fp_connectors.kicad_sch
Designer: Paul Peronnard/Tomasz Wlostowski
Group: BE-CEM
Size: A4
Last Modified: -
Rev:
KiCad E.D.A. 8.0.0
Id: 73/73