ENCM 467 Better "All The Equations (NA)"

Tables

Sign Conventions:

Parameter	NMOS	PMOS
Substrate	P-Type	N-Type
ϕ_f	-	+
Q_{Bo}, Q_B	-	+
V_{SB}	+	-
γ	+	-
V_{Th}	+	-

MOS Regions

For nMOS, flip inequalities for pMOS
Triode: $V_{ds} > 0$ & $V_{gs} - V_{Th} > V_{ds}$
$I_d = k'_n \frac{w}{L}[(V_{gs} - V_{Th})V_{ds} - \frac{V_{ds}^2}{2}]$
Saturation: $V_{ds} > 0$ and $V_{ds} > V_{gs} - V_{Th}$
$I_d = \frac{k'_n}{2}\frac{w}{L}(V_{gs} - V_{Th})^2$

MOS Capacitances

$C_{sb} = C_j(L_s W + x_j W) + C_{jsw}(2L_s + W)$
$(L_s W + x_j W)$ is the Kang textbooks area definition, Pg. 110
$C_{jsw} = C'_{jsw} x_j$

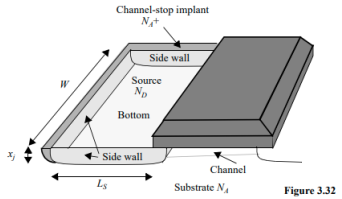


Figure 3.32

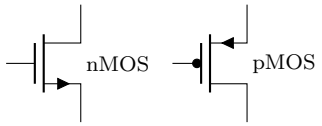
Pg. 112, Digital Integrated Circuits, Rabaey

Junction Capacitances:
$C_j = C_{jo} K_{eq}$
$K_{eq} = -\frac{\phi_o^m}{(V_2 - V_1)(1-m)}[(\phi_o - V_2)^{1-m} - (\phi_o - V_1)^{1-m}]$
Find ϕ_o in Diodes
Sidewall Capacitance
$C'_{jsw} = C_{josw} K_{eq(sw)}$
$C_{josw} = \sqrt{\frac{\epsilon_{si} q}{2} \frac{N_{a(sw)} N_d}{N_{a(sw)} + N_d} \frac{1}{\phi_{osw}}}$
$K_{eq(sw)} = -\frac{2\sqrt{\phi_{osw}}}{V_2 - V_1}(\sqrt{\phi_{osw} - V_2} - \sqrt{\phi_{osw} - V_1})$
$\phi_{osw} = \frac{kT}{q} ln(\frac{N_{a(sw)} N_d}{n_i^2})$
$V_{to(new)} = V_{to(n)} \pm \frac{q N_i}{C_{ox}}$ Where N_i is implanted carriers
NMOS: $+Acceptors, -Donors$
PMOS : $+Donors, -Acceptors$

Constants

$kT = 0.026eV$
$\frac{kT}{q} = \phi_T = V_T = 0.026V$
$k = 8.62 * 10^{-5} \frac{eV}{K}$ - Boltzmann's Constant
$q = 1.602 * 10^{-19} C$
$n_i = 1.45 * 10^{10} cm^{-3}$ - Intrinsic Conc. of Si at 300K
$\epsilon_o = 8.85 * 10^{-14} \frac{F}{cm}$
$\epsilon_{ox} = 3.9 * \epsilon_o \frac{F}{cm}$ - Permittivity of SiO_2
$\epsilon_{si} = 11.8 * \epsilon_o \frac{F}{cm}$ - Permittivity of Si
$\phi_{f(gate)} = 0.55V$
$\int \frac{dx}{x(ax+b)} = \frac{1}{b} ln(\frac{x}{ax+b})$

MOSFETs



$\phi_f = V_T ln(\frac{n_i}{N_a})$
$Q_B = \sqrt{2qN_a\epsilon_{si}|-2\phi_f + V_{SB}|}$
$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$
$V_{To} = \phi_{ms} - 2\phi_f - \frac{Q_{Bo}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$
$V_{Th} = V_{To} + \gamma(\sqrt{|-2\phi_f + V_{SB}|} - \sqrt{|2\phi_f|})$
$\gamma = \frac{\sqrt{2q\epsilon_{si}N_a}}{C_{ox}}$
$Q_{ox} = qN_{ox}$
$k'_n = \mu_n C_{ox}$
$k_n = \frac{W}{L} k'_n$
λ given: $I_{d,CLM} = I_d(1 + \lambda V_{ds})$
$g_m = g_{gs} = \frac{\partial i_d}{\partial V_{gs}}|_{V_{ds} \to const} = \frac{2I_d}{V_{gs} - V_{Th}}$
$g_{bs} = \frac{\partial i_d}{\partial V_{bs}} = g_{gs} \frac{\gamma}{2\sqrt{|-2\phi_f + V_{sb}|}} = \iota g_{gs}$
$g_{ds} = \lambda I_D$ (Saturation)
$I_D = g_{gs} V_{gs} + g_{bs} V_{bs} + \frac{V_{ds}}{r_{ds}}$
Unified Model:
$I_d = \mu C_{ox} \frac{w}{L}[(V_{gs} - V_{Th})V_{min} - \frac{V_{min}^2}{2}](1 + \lambda V_{ds})$
Where $V_{min} = min(V_{gs} - V_{th}, V_{ds}, V_{dsat})$

Diodes

$\phi_o = V_T ln(\frac{N_a N_d}{n_i^2})$
$I_d = I_s(e^{\frac{V_d}{nV_T}} - 1)$
$W_{dep} = \sqrt{\frac{2\epsilon_{si}(\phi_o - V_d)}{q}(\frac{1}{N_d} + \frac{1}{N_a})}$
$W_n = W_{dep} \frac{N_a}{N_d + N_a}$
$W_p = W_{dep} \frac{N_d}{N_d + N_a}$
$C_{jo} = \frac{\epsilon_{si} A}{W_{dep}}$
$C_j = C_{jo} \frac{1}{(1 - \frac{V_d}{\phi_o})^m}$
$C_d = \frac{(I_d + I_s)\tau_T}{V_T} \approx \frac{I_d \tau_T}{V_T}$
$C_d = C_{jo} \frac{1}{(1 - \frac{V_d}{\phi_o})^m} + \frac{\tau_T I_s}{V_T} e^{\frac{V_d}{n\phi_T}}$
$E_j = \sqrt{\frac{2q}{\epsilon_{si}} \frac{N_a N_d}{N_a + N_d}(\phi_o - V_d)}$
$Q_j = A_d \sqrt{2\epsilon_{si} q \frac{N_a N_d}{N_a + N_d}(\phi_o - V_d)}$

Short Channel Effects

$L < 0.25\mu m \to$ Short Channel
$\mu_{n(eff)} = \frac{\mu_{no}}{1 + \Theta E_x} = \frac{\mu_{no}}{1 + \frac{\Theta \epsilon_{ox}}{t_{ox}\epsilon_{si}}(V_{gs} - V(x))}$
$m = \frac{3t_{ox}}{W} + 1$
$E_{sat} = \frac{2v_{sat}}{\mu}$
$v = \frac{\mu_{eff} E}{1 + \frac{E}{E_{sat}}}$
$I_d = \frac{I_{d(LongChannel)}}{1 + \frac{V_{ds}}{E_{sat} L}}$
$I_{dsat} = \frac{I_{dsat(LongChannel)}}{1 + \frac{(V_{gs} - V_{th})}{E_{sat} L}}$
$I_{dsat} = \frac{W v_{sat} C_{ox}}{m}(V_{gs} - V_{th})$ Very Short Channel
$\frac{1}{V_{dsat}} = \frac{m}{V_{gs} - V_{th}} + \frac{1}{E_{sat} L}$

Short Channel Inverters

CMOS:
$G = -(g_{M1} + g_{M2})(R_{DS1} || R_{DS2})$
$g_m \approx k(V_{gs} - V_T)$
$R_{ds} \approx \frac{1}{\lambda I_d}$
$V_{th} = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{dd} - |V_{Tp}| + \frac{V_{DSATp}}{2})}{1 + r}$
$\approx \frac{rV_{dd}}{1+r}$
$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{E_{SATp} W_p}{E_{SATn} W_n}$
$\frac{k_p}{k_n} = \frac{V_{DSATn}(V_{th} - V_{Tn} - \frac{V_{DSATn}}{2})}{V_{DSATp}(V_{DD} - V_{Tn} - |V_{Tp}| + \frac{V_{DSATp}}{2})}$
$G \approx \frac{1+r}{(V_{th} - V_{Tn} - \frac{V_{DSATn}}{2})(\lambda_n - \lambda_p)}$
$NM_L = V_{th} - \frac{V_{dd} - V_{th}}{|G|}$
$NM_H = V_{dd} - V_{th}(1 + \frac{1}{|G|})$

Static Inverters

General:

V_{IL} & V_{IH} @ $\frac{dV_{out}}{dV_{in}} = -1$

$V_{OH} = V_{out}|_{V_{in}=V_{ss}}$

$V_{OL} = V_{out}|_{V_{in}=V_{dd}}$

$NM_L = |V_{IL} - V_{OL}|$

$NM_H = |V_{IH} - V_{OH}|$

$V_{th} \rightarrow V_{out} = V_{in}$

Pseudo NMOS

$k_r = k_n/k_p$

$V_{IL} = V_{TN} + \frac{V_{dd}-|V_{TP}|}{\sqrt{k_r^2+k_r}}$

$V_{IH} = V_{TN} + \frac{2(V_{dd}-|V_{TP}|)}{\sqrt{3k_r}}$

$V_{OL} = \frac{V_{dd}-V_{TN}}{\sqrt{3k_r}}$

$V_{OH} = V_{dd} - (V_{dd} - |V_{tp}|)(1 - \sqrt{\frac{k_r}{k_r+1}})$

Resistive Load NMOS Inverter:

$V_{OH} = V_{dd}$

$V_{OL} = V_{dd} - V_{TN} + \frac{1}{k_n R_L} - \sqrt{(V_{dd} - V_{TN} + \frac{1}{k_n R_L})^2 - \frac{2V_{dd}}{k_n R_L}}$

$\approx \frac{V_{dd}}{1+k_n R_L (V_{dd}-V_T)}$

$V_{IL} = V_{TN} + \frac{1}{k_n R_L}$

$V_{out}|_{V_{in}=V_{IL}} = V_{dd} - \frac{1}{2k_n R_L}$

$V_{IH} = V_{TN} + \sqrt{\frac{8V_{dd}}{3k_n R_L}} - \frac{1}{k_n R_L}$

$V_{out}|_{V_{in}=V_{IH}} = \sqrt{\frac{2V_{dd}}{3k_n R_L}}$

$V_{th} = V_{TN} - \frac{1}{k_n R_L}[1 - \sqrt{1 + 2k_n R_L (V_{dd} - V_{TN})}]$

$P_{DC(Avg)} = \frac{V_{dd}}{2} \frac{V_{dd}-V_{OL}}{R_L}$

CMOS Inverter:

$V_{th} = \frac{V_{Tn} + \sqrt{\frac{k_p}{k_n}}(V_{dd}-|V_{Tp}|)}{(1+\sqrt{\frac{k_p}{k_n}})}$

$\frac{k_p}{k_n} = (\frac{V_{th}-V_{Tn}}{V_{dd}-V_{th}-|V_{Tp}|})^2$

$V_{IL} = \frac{2V_{out}-|V_{Tp}|-V_{dd}+\frac{k_n}{k_p}V_{Tn}}{(1+\frac{k_n}{k_p})}$

$V_{IH} = \frac{V_{dd}-|V_{Tp}|+\frac{k_n}{k_p}(2V_{out}+V_{Tn})}{(1+\frac{k_n}{k_p})}$

Can approximate $Vo = V_{dd}$, or $V_o = 0$ for the above or find exact by substituting back into the $I_{d1} = I_{d2}$ equation.

Power in CMOS:

$P_{dyn} = C_L V_{dd}^2 f_{0\rightarrow1}$

$P_{sc} = t_{sc} V_{dd} i_{peak} f$

$t_{sc} = \frac{V_{dd}-2V_T}{V_{dd}}(\frac{t_r(f)}{0.8})$

$P_{TOTAL} = P_{DYN} + P_{SC} + P_{STATIC}$

Transient MOS Inverters

$R_n = \frac{1}{k_n(V_{dd}-V_{Tn})} = \frac{V_{ds}}{I_{ds}}$

$R_p = \frac{1}{k_p(V_{dd}-|V_{Tp}|)} = \frac{V_{sd}}{I_{sd}}$

$\tau \propto \frac{VC}{I} \propto RC$

$\tau_n = R_n C_L$ From ENEL 343

$\tau_p = R_p C_L$

$\tau_{PHL} = ln(2)\tau_n = \frac{0.69C_L}{k_n(V_{dd}-V_{tn})}$

$\tau_{PLH} = ln(2)\tau_p = \frac{0.69C_L}{k_p(V_{dd}-|V_{tp}|)}$

$t_p = \frac{1}{2}(\tau_{PHL} + \tau_{PLH})$

$t_r = 2.2\tau_p = \frac{2.2C_L}{k_p(V_{dd}-|V_{tp}|)}$ 10% to 90%

$t_f = 2.2\tau_n = \frac{2.2C_L}{k_n(V_{dd}-V_{tn})}$ 90% to 10%

$f_{max} = \frac{1}{t_r+t_f}$

$C_L = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_w + C_g$

Short Channel:

$R_{n,p} = \frac{3V_{dd}}{4I_{DSAT}}(1 - \frac{7}{9}\lambda V_{dd})$

$I_{DSAT} = kV_{DSAT}(V_{dd} - V_t - \frac{V_{DSAT}}{2})$

$\tau_{PHL} = \frac{0.52V_{dd}C_L}{I_{DSAT,n}}$

$\tau_{PLH} = \frac{0.52V_{dd}C_L}{I_{DSAT,p}}$

Inverter Chain Sizing

$f \rightarrow$ Device Size Increase per Inverter

$f = \sqrt[N]{\frac{C_L}{C_{g,1}}} = \sqrt[N]{F}$

$f_{opt} = 3.6$

$N_{opt} = \frac{ln(C_{out}/C_{in})}{ln(3.6)}$

$t_p = Nt_{po}(1 + \frac{\sqrt[N]{F}}{\gamma})$

Gate Chain Sizing

$g = \frac{C_{Gate}}{C_{Inverter}}$

$g_{NAND} = \frac{n+2}{3}$

$g_{NOR} = \frac{2n+1}{3}$

$g_{XOR2} = 4$

$g_{XOR3} = 12$

$g_{NOT} = 1$

$p = \frac{R_{gate}C_{d,gate}}{R_{inv}C_{d,inv}}$

$p_{Inverter} = 1$

$p_{NAND} = n$

$p_{NOR} = n$

$p_{XOR,XNOR} = n2^{n-1}$

$t_p = t_{po}(\sum_{j=1}^{N} p_j + \frac{N\sqrt[N]{H}}{\gamma})$

$b_i = \frac{C_{path}+C_{offpath}}{C_{path}}$ How many gates the output feeds into.

$G = g_1 g_2 g_3 ... g_n$ each g_i is only the specific gate passed through.

$B = b_1 b_2 b_3 ... b_n$

$H = GFB$

$h_{opt} = \sqrt[N]{H}$ N is how many rows of Gates.

$C_x = \frac{g_x C_{out} b_x}{h_{opt}}$, This is the Sizing of each Gate, and C_x for one gate is C_{out} for the one prior.

Sequential Logic

$T \geq t_{c-q} + t_{plogic} + t_{su}$

$t_{cdregister} + t_{cdlogic} \geq t_{hold}$

CMOS Logic Gates

N Input NOR:

$V_{th} = \frac{V_{dd}-|V_{tp}|+NV_{tn}\sqrt{k_n/k_p}}{1+N\sqrt{kn/kp}}$

N Input NAND:

$V_{th} = \frac{V_{dd}-|V_{tp}|+\frac{1}{N}V_{tn}\sqrt{k_n/k_p}}{1+\frac{1}{N}\sqrt{kn/kp}}$

Series MOS: $k_{n,p} = k_{n,p1}//k_{n,p2}$

Parallel MOS: $k_{n,p} = k_{n,p1} + k_{n,p2}$

$R_{eq} \propto \frac{\frac{1}{W}}{L}$

$R_{opt(PUN)} \propto \frac{L}{2W}$

$R_{opt(PDN)} \propto \frac{L}{W}$

$t_{elmore} = R_1C_1 + (R_1 + R_2)C_2 ... + (R_1 + R_2 + ... + R_n)C_n$