## PCI PCB DESIGN LAYOUT GUIDELINES

Careful attention must always be exercised when beginning the design and layout phase of any new printed circuit board. It is only through careful planning and the usage of good electrical design practices that long term product reliability may be achieved. Careful attention to layout issues of EMI, cross-talk and decoupling will avoid engineering prototype development problems and future production failures due to an "on the edge" design.

Designs incorporating PCI devices have specific printed circuit board layout requirements in order to comply with industry standard PCI local bus specifications. In addition to these requirements, AMCC's S5933/20 PCI controller also has specific requirements to ensure proper function and long life. This applications note is supplied by AMCC as factory recommended PCB design layout guidelines for printed circuit boards incorporating the S5933/20 PCI controller. The following sections detail important design areas concerning PCB design, power decoupling, ferrite beads and critical trace layout.

## PCB DESIGN

AMCC highly recommends the use of a four layer printed circuit board. This is due to the expected high trace density in most PCI designs incorporating PLCC and PQFP devices. Four layer designs significantly overcome ground noise problems associated with most two layer PCBs. Should a two layer design be implemented, leave as much copper on the PCB as possible for all power distribution traces. This is extremely important in ground traces to avoid ground loops and ground potential problems. Also utilize multiple feed-thrus for large traces. A 100 mil trace with a single 0.030 feed thru has it's current carrying capability significantly reduced due to the wall thickness of the via.

## DECOUPLING

The AMCC PCI controller is an application specific standard product (ASSP) utilizing CMOS technology. Although CMOS technology is commonly known for it's noise immunity properties, special consideration must still be given to electrical noise generated due to the high speed signals utilized in a PCI design.

The first design issue of concern is decoupling. By "decoupling", the designer provides a means to dissociate circuit functions from the power bus serving that circuit. This "means" is provided through the usage of decoupling capacitors, ferrite beads and proper printed circuit board trace layout. The lack of correct decoupling increases both radiated

and conducted emissions which increases electrical noise and susceptibility to circuit failure (i.e. erratic and intermittent circuit functions or "FLAKYNESS").

To reduce these problems, AMCC recommends PCI designs incorporate a low speed PCB decoupling capacitor. Select a 10uF (minimum) tantalum or metallized polycarbonate (not aluminum) capacitor for this purpose. Specify a low ESR type at a working voltage slightly above the circuit's operating voltage. Locate the capacitor no more than 300 mils from the PCB's power entry point as shown in figure 1. This point is likely the PCB edge fingers or a wire connector interfacing the PCB to the system power supply.
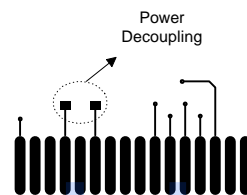


Figure 1

AMCC also recommends the use of one high speed 0.01uF decoupling capacitor per PCB IC package. Specify an X7R or BX type dielectric ceramic chip capacitor also rated slightly above required working voltage for this purpose. Locate each capacitor next to and on the same side of the PCB as each IC device. Locate capacitors no more than 150 mils from each IC package's ground pin. High speed decoupling for the S5933/20 PCI controller IC requires one 0.01uF per power and ground pin pair. IMPORTANT: Locate these capacitors on the same side of the PCB as the S5933 at a distance of less than 150 mils as shown in figure 2.
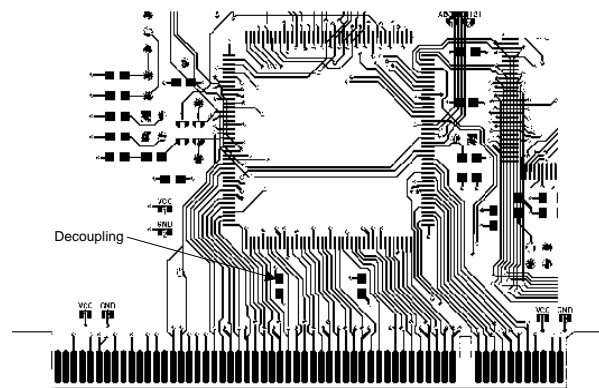


Figure 2

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# S5933/20 PCB Layout Guidelines
## Application Note

The use of the above capacitors will sufficiently decouple the Vcc and ground planes from high and low speed circuit functions. One last decoupling issue of concern involves any unused PCI edge connector power fingers. Industry PCI specifications provides for power sources of +3.3V and +5V within the PCI edge connector. PCI specifications require any unused power and V I/O pins on the PCI edge connector be decoupled to the ground plane with an average of 0.01uF. YES, ALL UNUSED POWER PINS INCLUDING THE 3.3V PINS!

## FERRITE BEADS

In many applications the requirement for ferrite beads to reduce high frequency noise is unnecessary once the above indicated board layout and by-pass practices have been followed. However, in some applications high frequency noise may persist. In these cases the addition of a ferrite bead to the input +V power entry point as shown in figure 1 may be necessary. The size and type of material used will vary depending on the particular design and electrical noise to be eliminated. Consult the bead manufacturer data books to determine the best fit. Expect to try a small selection of beads to achieve best results. Use a single pass thru or one turn to increase effectiveness of the bead. DO NOT series beads to increase impedance. Use a cracked air gap bead to reduce saturation effects as necessary.

## CRITICAL TRACE LAYOUT

AMCC's S5933/20 PCI devices are very powerful and flexible. They operate at clock and data bus speeds of up to 40 megahertz. PCI data bus transfer operations can occur in 30 nanoseconds with signal rise and fall times of 3 nanoseconds. At these speeds, signal traces look more like transmission lines where trace impedance becomes an important factor. Careful attention to trace lengths and routing will prevent impedance caused ringing and will preserve signal rise and fall times. As a last design issue, standard PCI specifications require the following design criteria be adhered to for all PCI bus controller devices.

1. Trace lengths for each 32 bit interface data signal from the S5933/20 to the PCI bus is limited to a maximum of 1.5 inches for all 32 bit cards.

2. The trace connecting the S5933/20 PCI clock signal (S5933 or S5920 pin 142) to the PCI bus connector must be 2.5 inches +/- .1 inches in length and can be routed to only one load. It may be necessary to "snake" this trace depending on the physical location of the PCI controller IC on the PCB to ensure this requirement is met. Ensure all corners of this trace are rounded. Do not use 90 degree sharp corners.

3. The unloaded impedance of a shared PCI signal trace on the expansion card must be held within a 60 to 100 ohm range. On a typical 4 layer glass epoxy PCB, maintaining a signal trace width of 20 to 30 mils will satisfy this requirement.

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