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CPE 410

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Project #1

For my project, I designed a 4-bit Binary Combinational Multiplier in VHDL. The theory behind the Combinational Multiplier is as follows:

Each output bit (S0-S7) represents a sum of partial products of the input bits. For example, to multiply two binary numbers, A \* B, it would be:

A3 A2  A1  A0

x B3 B2 B1 B0

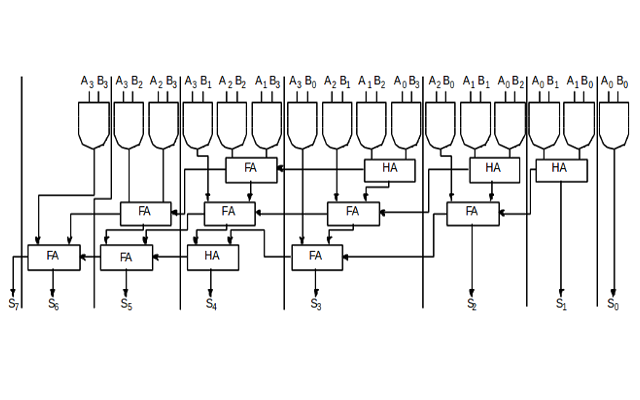
A3B A2B0  A1B0 A0B0

A3B1 A2B1 A1B1 A0B1

A3B2 A2B2 A1B2 A0B2

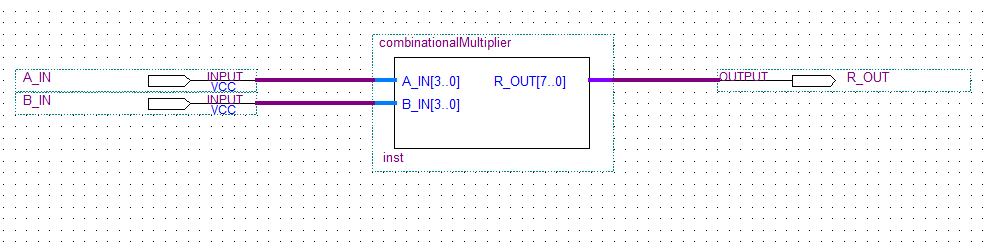
A3B3 A2B3 A1B3 A0B3

S7 S6 S5 S4 S3 S2 S1 S0



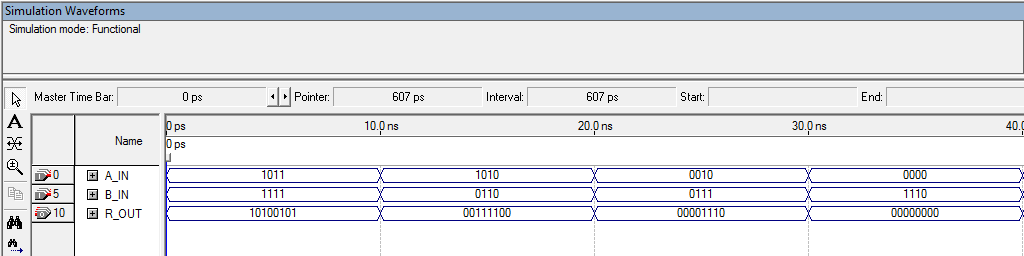
The output bits, S0-S7 can be minimized using a series of Half Adders, and Full Adders, in turn with AND gates, as seen below. (Image from <http://virtual-labs.ac.in/labs/cse10/images/cm.png>)

Using this information, I created VHDL Entities for both the Full and Half Adder. Then I created a VHDL file for the Combinational Multiplier and simulated it in Quartus. Below is the block diagram for my design.



It takes two 4-bit values as inputs, and outputs an 8bit value.

Finally, here are my simulation results for the design.



As you can see, I have demonstrated four different input combinations, all correctly displaying the value of A \* B.