

2021 Fall Computer Architecture

Homework 5

**Due Date: 12/28 (Tue) 23:59**

- You need to give an explanation about your answer or show how you derive it.
- Submit your answer sheet in **vertical A4 PDF** to NTU COOL.
- Name your file **[student\_id]\_hw5.pdf**.
- Due to coming final exam, **late submission won't be accepted**.

Unless specified otherwise, assume memory is byte addressable and 1 word is 4 bytes.

1. For a direct-mapped cache design with a 32-bit address, and with a valid bit and a dirty bit for each set, the following bits of the address are used to access the cache.

Tag	Index	Offset
31-10	9-4	3-0

- a. (5 points) What is the block size in bytes?
- b. (5 points) How many blocks does the cache have?
- c. (6 points) What is the total bits for this cache?
- d. (20 points) Beginning from power on, the following cache references are recorded.

	Address							
Hex	00	04	802	A66	4CFB	A65	188	3705

For each reference, list its tag, index, offset, and whether it is a hit or a miss, in the following format.

Address	Tag	Index	Offset	Hit/Miss
00	0x00	0x00	0x0	Miss
04				

(And so on...)

2. Assume that the main memory accesses take 70 ns and that 30% of all instructions access data memory. The following table shows data for the L1 cache attached to a processor P. Also assume that the L1 hit time determines the cycle time for P.

Cache	Miss Rate	Hit Time
L1	5.0%	0.60 ns

- (8 points) What is the AMAT (Average Memory Access Time) for P in cycles?
- (8 points) Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P? (When we say a “base CPI of 1.0”, we mean that an instruction completes in one cycle, unless either the instruction access or the data access causes a cache miss.)

For the next two problems, we will consider the addition of the L2 cache. The following table shows the data for the L2 cache attached to P. The L2 miss rate indicated is its local miss rate.

Cache	Miss Rate	Hit Time
L2	90.0%	5.0 ns

- (8 points) What is the AMAT for P with the addition of an L2 cache in cycles?
- (8 points) Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P with the addition of L2 caches?

3. The following table shows data for the page table of a system S. ( $1K = 2^{10}$ )

Virtual Address Size	Page Size	Page Table Entry Size
40 bits	16 KB	4 bytes

- (8 points) Given the parameters shown above, for a single-level page table, how many page table entries are needed for S?
- (8 points) Following the previous problem (a.), calculate the amount of memory required for the page tables for S running 3 processes.
- (8 points) Given the parameters shown above, for a two-level page table approach with up to 256 entries at the 1<sup>st</sup> level, what is the amount of memory required for a second-level table for S?
- (8 points) Following the previous problem (c.), for S running 3 processes that each utilizes half of virtual memory available, calculate the minimum amount of memory required for the second-level tables. (It is not necessarily all the page tables at the 2<sup>nd</sup> level are allocated.)