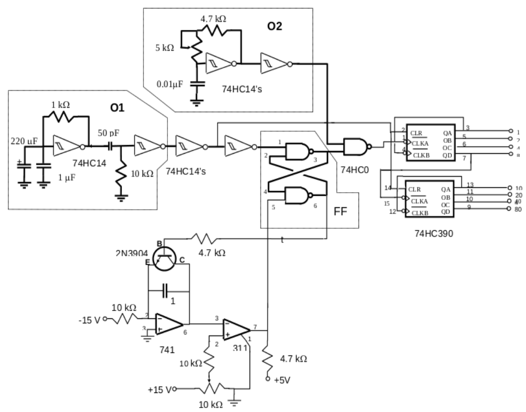
University of British Columbia

Construction and Analysis of an Analog to Digital Converter Implemented as a Voltmeter

PHYS – 219: Intermediate Experimental Physics



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Abstract

With the release of Fairchild Semiconductor's LM101operational amplifier in 1967, the modern op-amp has found wide application across industry. In this paper, we attempt to utilize an LM741 configured as a time sensitive ramp generator in combination with an LM311 compataror in an effort to convert an analog reference voltage to a binary coded decimal sequence. The addition of a rudimentary finite state machine and auxillary control logic allowed for capture of a rising reference voltage, within a defined time increment, resulting in the successfull conversion of voltage to BCD through a divide by100 BCD counter. The resultant configuration was implemented as a functional digital voltmeter.

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1.0 Introduction

An experimental test bench was assembled consisting of a +- 5,15VDC fixed power supply [1]. An Agilent HP34401A [2] multimeter was used to measure resistor values and reference voltages. Collection of the pre circuit / post circuit waveforms was performed by a DS1000E Rigol Oscilloscope [3] configured to allow for image capture to usb.

1.1 Theory

Exerpt from *Experiment #8 ANALOG TO DIGITAL CONVERTER*:

“The trigger generator (circuit “O1”) is the device which determines the frequency at which your d.c. input signal is sampled. Its short (negative go ing) output isused to: i) Clear the decade counter. But since the decade counter requires a positive reset (CLR) pulse, an additional digital inverter (which also feeds the TP1 test point) is incorporated between the circuit “01” and the decade counter.ii) “Sets” the control flip-flop (circuit “FF”) which in turn opens a gate to allow the clock pulses (from circuit “O2”) to pass to the decade counter. Since negative-goingsignals are required to “set” the FF, the necessary signal could have been obtained directly at the output of the “01” circuit. However, in order to be certain that no gated clock pulses can arrive at the decade counter before the counter has been cleared, a slight time delay is provided by using a further inverter following the TP1 testpoint. This inverter changes the short positiveoutput pulse at TP1 back to the short negative pulse required to “set” the FF.In addition, the control flip-flop opens the electronic (transistor) switch on the ramp generator to initiate the analogue-to-time conversion process. Once the ramp voltage reaches the level set by the d.c. input voltage, the negative transition at the output of the 311comparator “Resets” the flip-flop which in turncloses the gate at the output of the clock, thus preventing any more clock pulses from reaching the counter, and also closes the electronic (transistor) switch which in turn “shorts” the 1 µF integrating capacitor, thus terminating the production of the ramp and returning the output level of the integrating 741OpAmp to ground. At this instant, the 311comparator responds by changing its output to a Hi value. Since this whole process which occurs after the ramp voltage reaches the level set by the d.c. input level takes such a short time, the duration of the negative output pulse from the comparator is correspondingly short as well.” [0]

The following integrated circuits were used in construction of the Analog to Digital Converter, figure 0.

1. LM741 Operational Amplifier [4]

2. M74HC00A Quad 2-Input NAND Gate [5]

3. MM74HC14 Hex Inverting Schmitt Trigger [6]

4. 74HCT390 Dual Decade Ripple Counter [7]

5. LM311 Voltage Comparator [8]

6. 2N3904 NPN Transistor [9]

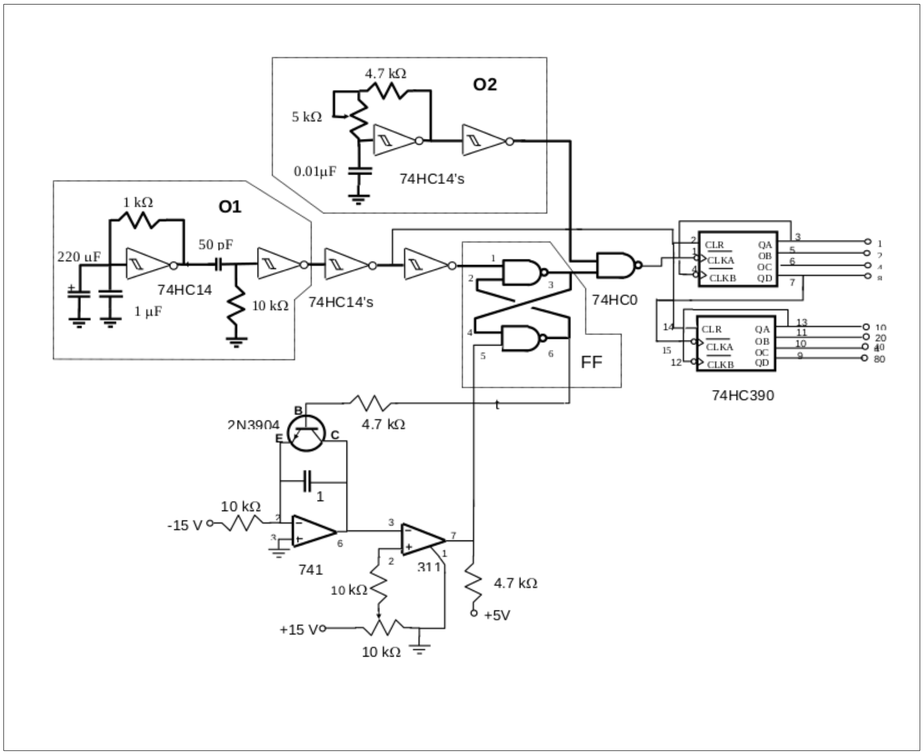
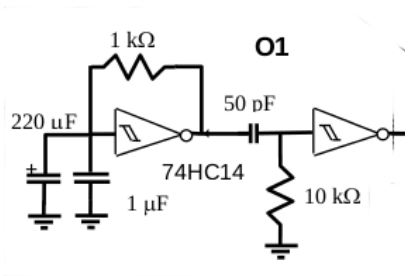


Figure 0 – Analog to Digital Converter

2.0 Analysis

2.1 kHz Square Wave Oscillator

The square wave oscillator was assembled as shown in figure 1, with particular characteristics presented in table 1.



Element	Value
1 k	1.0012k Ω
10 k	9.981k Ω
220 uF	Within 3%
1 uF	Within 3%
50 pF	Within 3%
Vcc	5.0065V DC
GND	0.0023V DC

Table 1 – Recorded values of oscillator circuit elements

Figure 1 – Square Wave Oscillator

Signal collection via the oscilloscope is presented in figure 2; with the generated RC wave displayed via channel 1 and the computed Vout square wave displayed via channel 2.

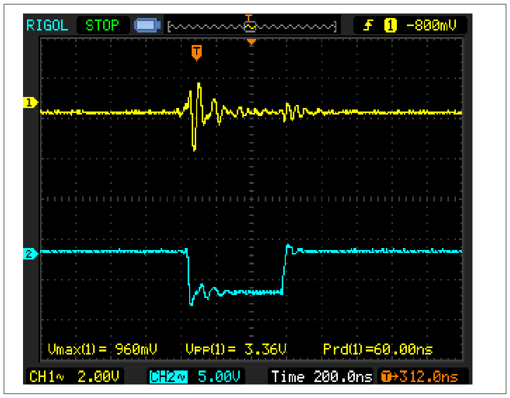
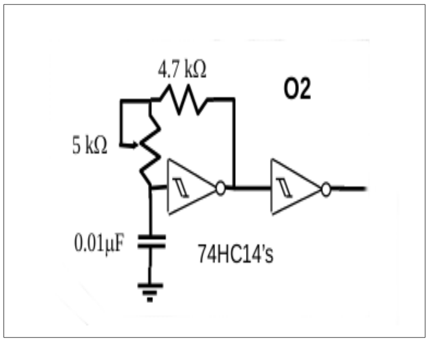


Figure 2 – Square Wave Oscillator I/O

2.2 Clock Pulse Generator

The clock pulse generator was assembled as shown in figure 3 with particular characteristics presented in table 2. The 5k potentiometer was adjusted to provide a 8.325 kHz square output.



Element	Value
4.7 k	4.7021 kΩ
5 k (10k used)	0.0024 kΩ to 10.0232 kΩ
0.01 uF	Within 3%
Vcc	5.0065 V DC
GND	0.0023 V DC
Output Freq.	8.325 kHz

Table 2 – Recorded values of clock pulse circuit elements

Figure 3 – Clock Pulse Generator

Signal collection via the oscilloscope is presented in figure 4; with the generated RC wave displayed via channel 1 and the computed Vout square wave displayed via channel 2. x10 zoom on falling edge presented for comparison.

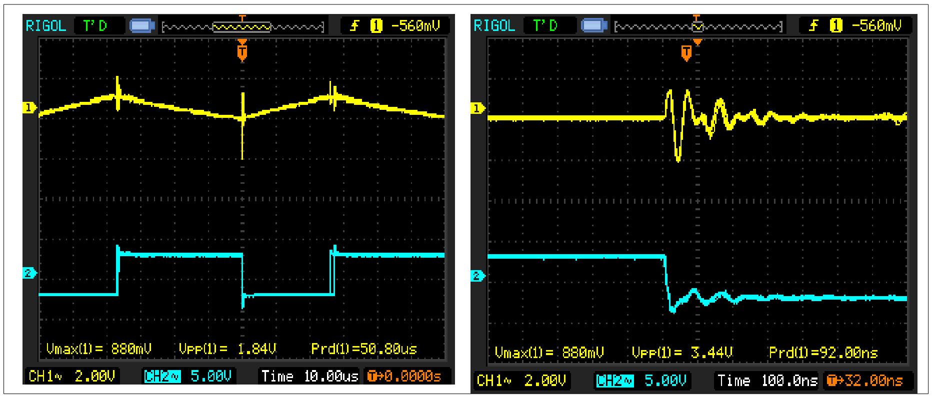


Figure 4 – Clock Pulse Generator I/O

2.3 Flip Flop

An SR flipflop was constructed using NAND gates enclosed in a single CMOS IC as shown in figure 5, with particular characteristics presented in table 3.

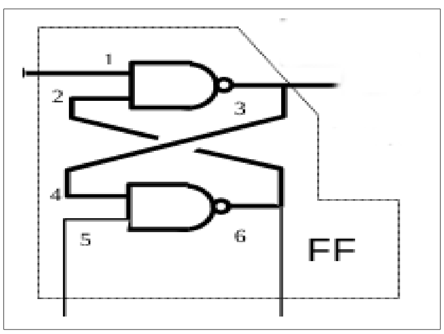


Figure 5 – SR Flipflop

Element	Value
Vcc	5.0065 V DC
GND	0.0023 V DC

Table 3 – Recorded values of SR flipflop circuit elements

Signal collection via the oscilloscope is presented in figure 6; with the square wave input signal displayed via channel 1 and flipflop output displayed via channel 2. x2 zoom on rising edge presented for comparison.

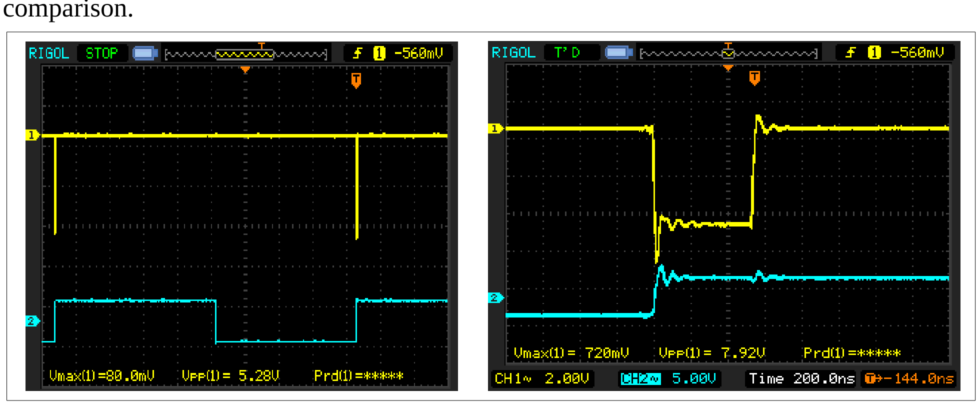
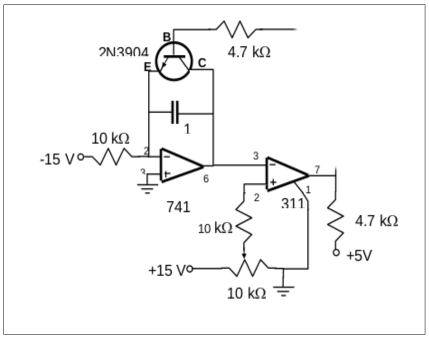


Figure 6 – SR Flipflop I/O

2.4 Analog to Time Converter

The analog to time converter was assembled as shown in figure 7, with particular characteristics presented in table 4.



Element	Value
4.7 k	4.63452k Ω
10 k – LM741	10.0432k Ω
10 k - LM311	10.0118k Ω
Vcc+	15.0026V DC
Vcc-	-15.0004V DC
0.01 uF	Within 3%
10 k	0.0019 kΩ to 10.1542 kΩ

Table 4 – Recorded values of analog to time converter circuit elements

Figure 7 – Analog to Time Converter

Signal collection via the oscilloscope is presented in figure 8; with the input displayed via channel 1 and the op amp, comparator, and full circuit segment displayed via channel 2 in figure 8, 9, 10 respectivley.

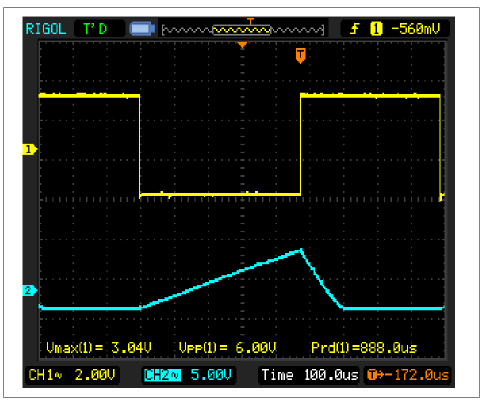


Figure 8 – Analog to Time Converter, resistor to op amp I/O.

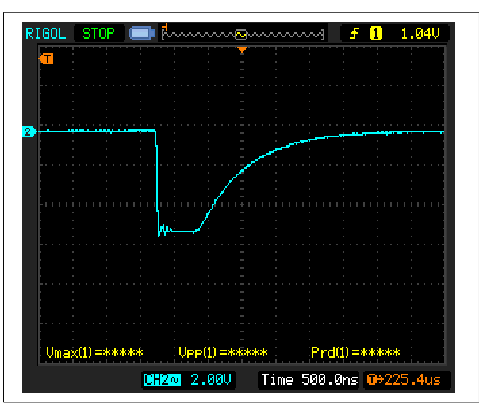


Figure 9 – Analog to Time Converter, comparator output.

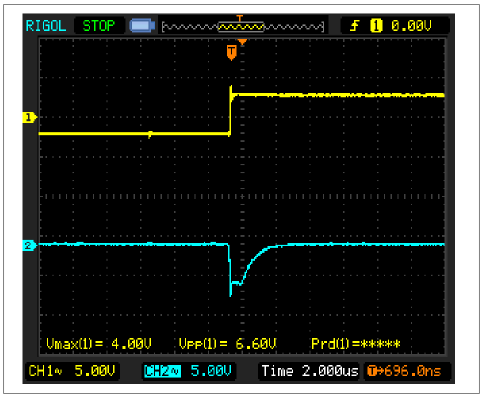


Figure 10 – Analog to Time Converter, resistor to comparator I/O

2.5 Divide by 100 BCD Counter

A divide by 100 BCD counter was constructed using a single 390 IC containing 2 x divide by 2 counters and 2 x divide by 5 counters as shown in figure 5, with particular characteristics presented in table 5. The outputs of the counter were connected to a 7 segment LCD base 10 display

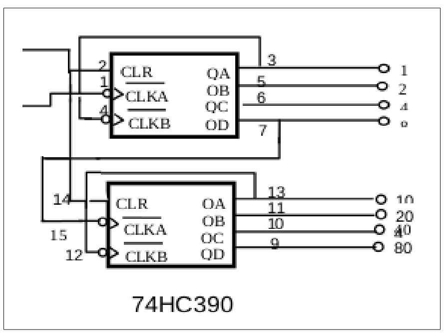


Figure 11 – Divide by 100 BCD Counter

Element	Value
Vcc	5.0065 V DC
GND	0.0023 V DC

Table 5 – Recorded values of divide by 100 BCD Counter circuit elements

Signal collection via the oscilloscope is presented in figure 12; with the input signal from the flip flop to 1CPo displayed via channel 1. Photograph of LED output with DMM comparison presented in figure 13.

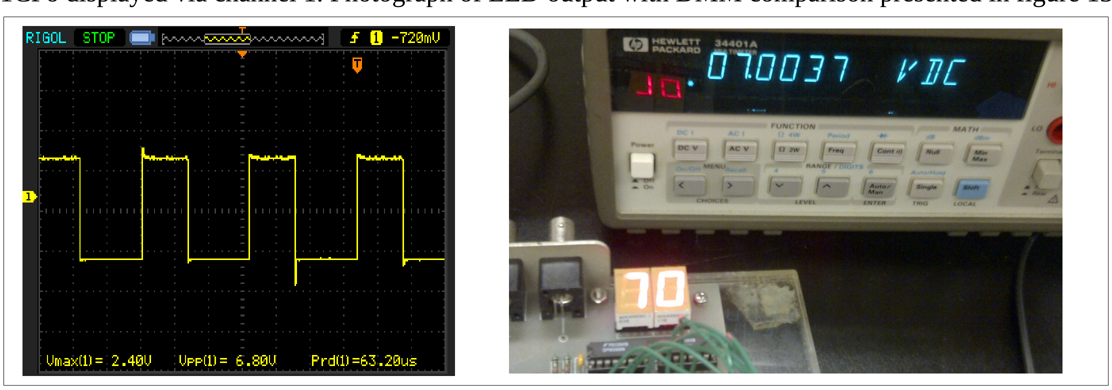


Figure 12 / 13 – Divide by 100 BCD Counter 1CPo I/O

3.0 Interpretation

The input analog voltage, to be converted to a digital signal for display by the LED segment, is adjusted via to 10k potentiometer in the analog to time converter. By adjusting the 5k potentiometer in subsection O2, clock pulse generator, the LED display can be synchronized to the DMM display providing 2 decimals of precision. A clock pulse frequency of 8.235 kHz allowed for 1:1 calibration of the LED diplayed voltage.

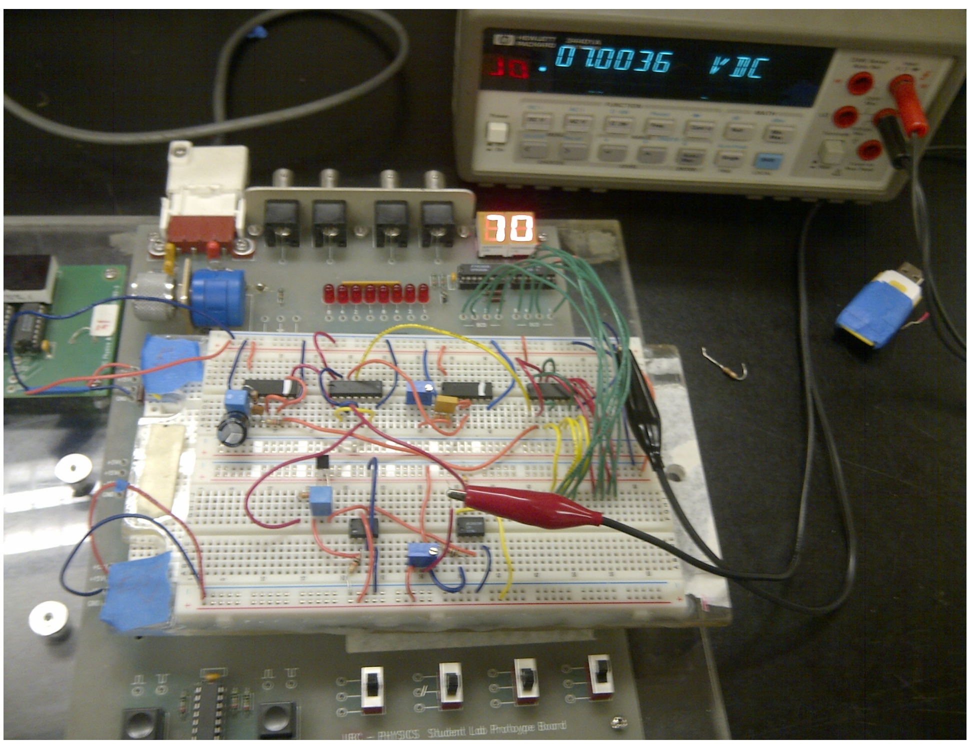
	DMM Voltage	LED Voltage
Minimum	.0025 DC	00
Mid Range	7.0037 DC	70
Maxmimum	10.0015 DC	99

Table 6 – Vin vs LED Results

4.0 Conclusion

Once assembled, the analog to digital converter performed as predicted. Precision by a factor of 10^-1, when compared to the HP DMM, was achieved after final adjustment to a clock pulse of 8.325 kHz. Adjustment of the input voltage maintained a linear relationship thoughout the entire measured range.

Further analysis of this design may consist of parallel divide by 100 counters, further increasing the circuits resolution as well as recalibrating the LED to display a percentage of the maximum input voltage. Such probing of extreme values would allow for determination of LM741 op amp roll off characteristics as well examinators of the LM311 comparator's limitations.



5.0 References

[0] Experiment #8 ANALOG TO DIGITAL CONVERTER, PHYS 219, Univeristy of British Columbia.

[1] Power Supply, Univeristy of British Columbia, specifications not availible.

[2] Agilent HP34401A Digital Multimeter. http://www.keysight.com

[3] Rigol Oscilloscope DS1000E. http://www.rigolna.com

[4] LM741 Operational Amplifier. http://www.ti.com/lit/ds/symlink/lm741.pdf

[5] M74HC00A Quad 2-Input NAND Gate. http://www.datasheetspdf.com/PDF/M74HC00/489292/1

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[7] 74HCT390 Dual Decade Ripple Counter
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[8] LM311 Voltage Comparator.
http://www.st.com/web/en/resource/technical/document/datasheet/CD00001072.pdf

[9] 2N3904 NPN Transistor. https://www.fairchildsemi.com/products/discretes/bipolar-transistors/small-signal-bjts/2N3904.html