1. Description

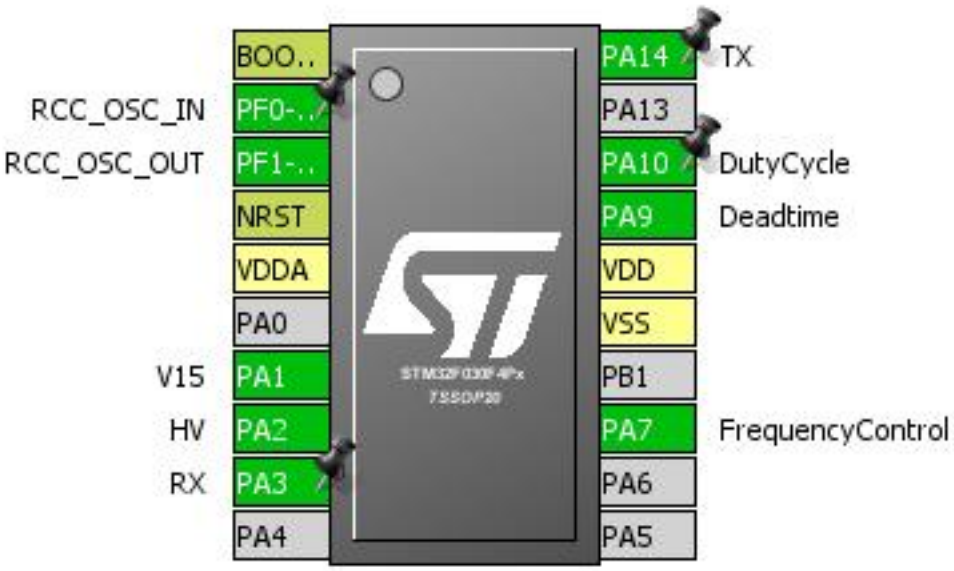
1.1. Project

Project Name	USG-Cube
Board Name	USG-Cube
Generated with:	STM32CubeMX 4.10.0
Date	09/23/2015

1.2. MCU

MCU Series	STM32F0
MCU Line	STM32F0x0 Value Line
MCU name	STM32F030F4Px
MCU Package	TSSOP20
MCU Pin number	20

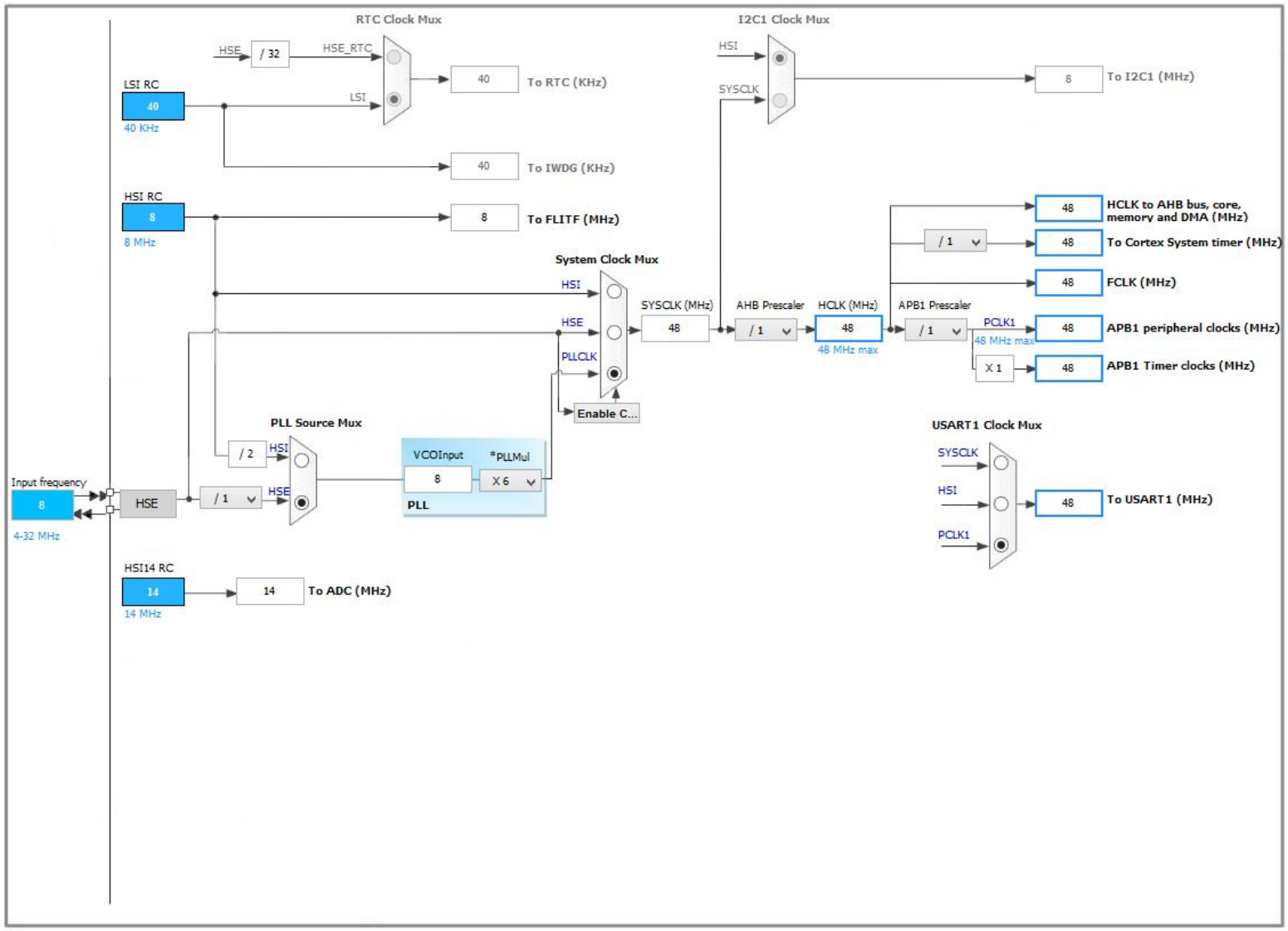
2. Pinout Configuration



3. Pins Configuration

Pin Number TSSOP20	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	BOOT0	Boot		
2	PF0-OSC_IN	I/O	RCC_OSC_IN	
3	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
4	NRST	Reset		
5	VDDA	Power		
7	PA1	I/O	ADC_IN1	V15
8	PA2	I/O	ADC_IN2	HV
9	PA3	I/O	USART1_RX	RX
13	PA7	I/O	TIM1_CH1N	FrequencyControl
15	VSS	Power		
16	VDD	Power		
17	PA9	I/O	TIM1_CH2	Deadtime
18	PA10	I/O	TIM1_CH3	DutyCycle
20	PA14	I/O	USART1_TX	TX

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC

mode: IN1

mode: IN2

mode: Temperature Sensor Channel

mode: Vrefint Channel

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Forward
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Low Power Auto Wait	Disabled
Low Power Auto Power Off	Disabled

ADC_Regular_ConversionMode:

Sampling Time	1.5 Cycles
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Disabled

Prefetch Buffer	Enabled
Data Cache	Disabled
Flash Latency(WS)	1 WS (2 CPU cycle)

RCC Parameters:

HSI14 Calibration Value	16

5.3. TIM1

mode: Clock Source

Channel1: PWM Generation CH1N

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1N:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CHN Polarity	High
CHN Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.4. USART1

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Is Inverted	Disable
RX Pin Active Level Is Inverted	Disable
Data Are Inverted	Disable
TX and RX Pins Are Swapped	Disable
Overrun Disable	Disable
DMA Disable on RX Error	Disable
MSB Is Sent First	Disable

*** User modified value**

5. Power Plugin report

5.1. Microcontroller Selection

Series	STM32F0
Line	STM32F0x0 Value Line
MCU	STM32F030F4Px
Datasheet	024849_Rev2

5.2. Parameter Selection

Temperature	25
Vdd	3.6

5.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self discharge	0.08 %/month
Nominal voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

5.4. Sequence

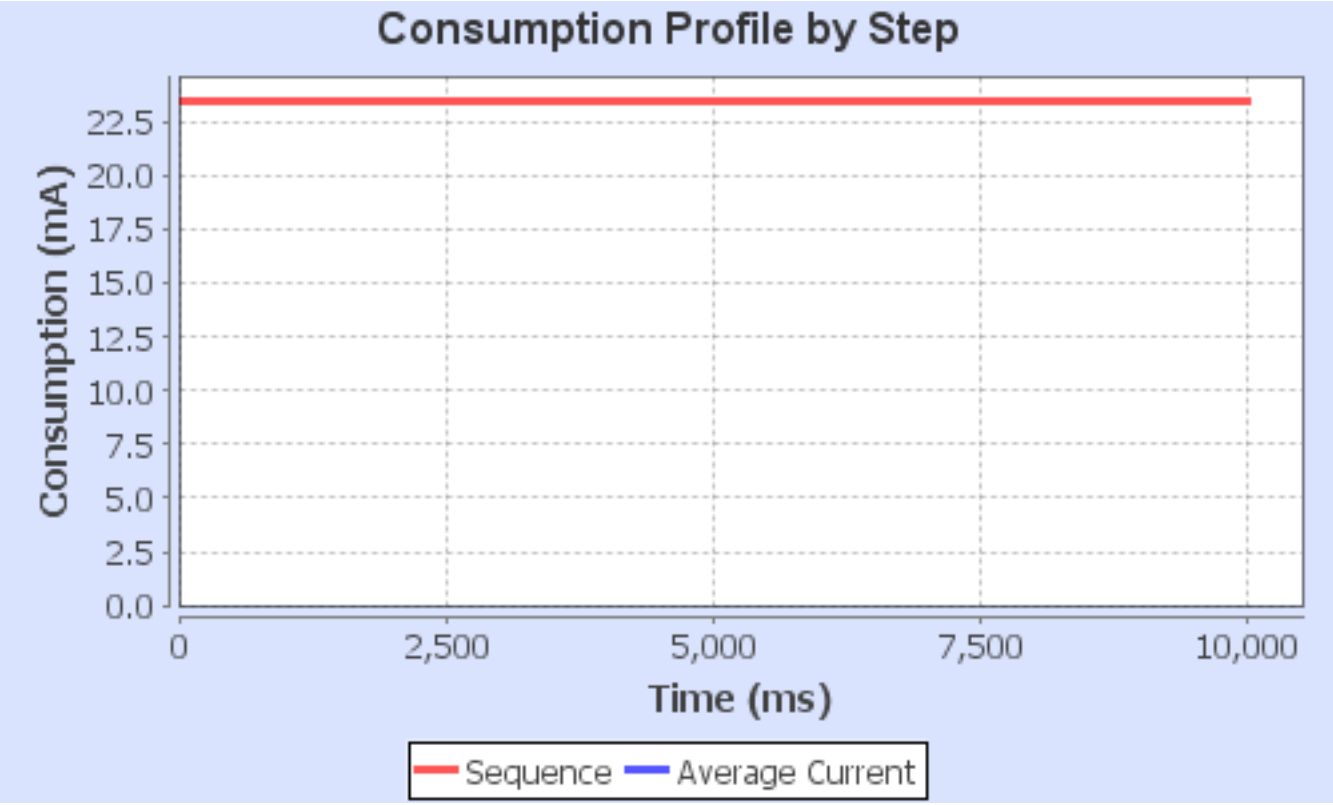
Step	STEP1
Mode	RUN
Range	No Scale
Fetch type	FLASH

Clock Config.	HSE PLL All IPs ON
Clock Source Freq.	8.0 MHz
CPU Freq.	48.0 MHz
Periph.	
Additional Cons.	0 mA
Average Current	23.46 mA
Duration	10 s
DMIPS	0.0

5.5. Results

Sequence time	10 s	Average current	23.46 mA
Battery Life	0	Average DMIPS	0.0 DMIPS

5.6. Chart



6. Software Project

6.1. Project Settings

Name	Value
Project Name	USG-Cube
Project Folder	D:\MPP-dev\USG-Cube
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F0 V1.3.0

6.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6.3. Toolchains Settings

Name	Value
Compiler Optimizations	Balanced Size/Speed