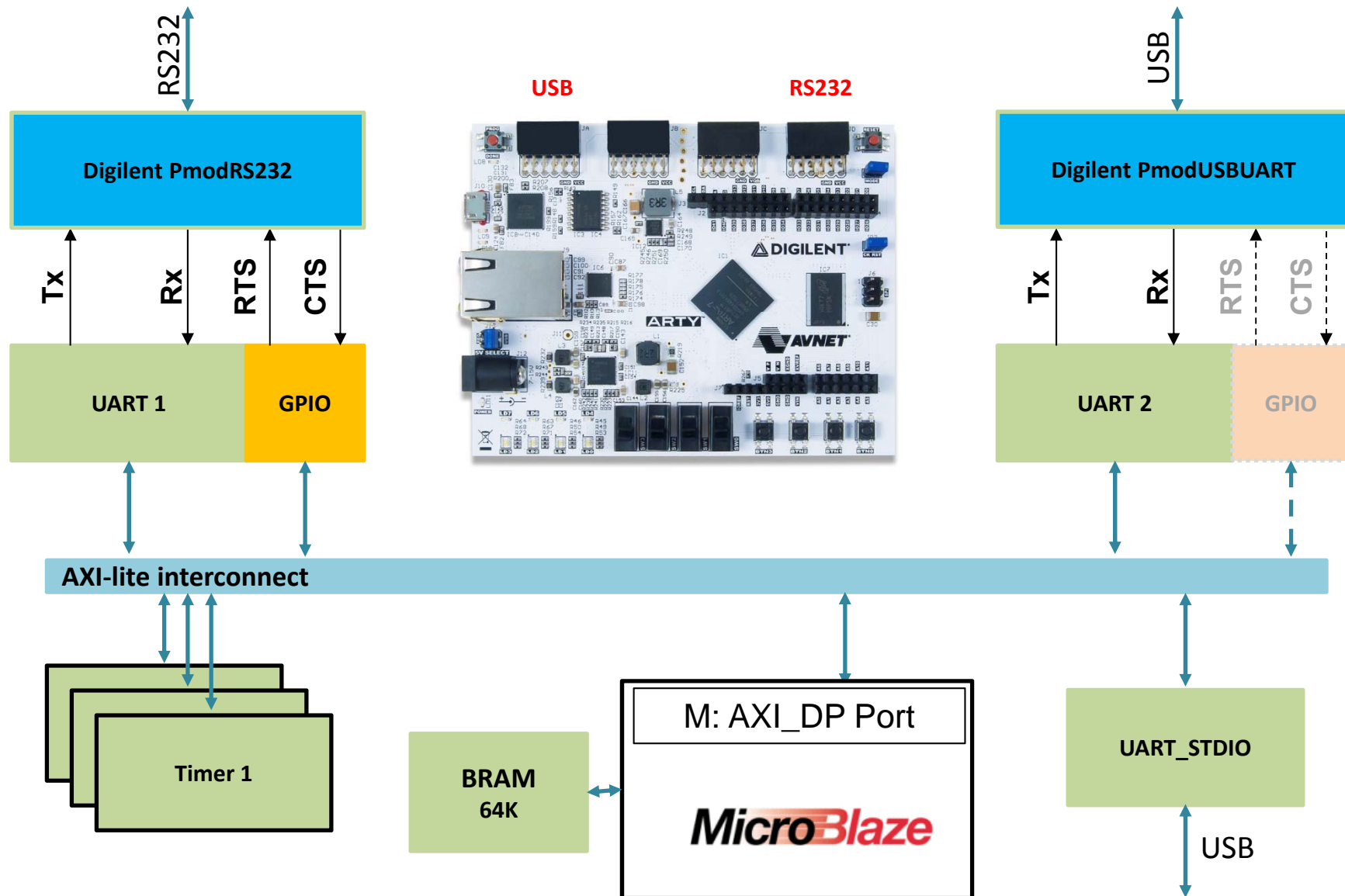


ARTY Architecture



UART Address Mapping and Characteristics

| Peripherals | AXI-Lite Base Address | Depth (Bytes) | BAUD RATE | Number of Data bits | Parity |
|-------------|-----------------------|---------------|-----------|---------------------|--------|
| UART 1 | 0x4000_0000 | 0x10000 | 9600 | 8 | None |
| UART1_FC* | 0x4001_0000 | 0x10000 | - | - | - |
| UART 2 | 0x4002_0000 | 0x10000 | 38400 | 8 | None |
| UART2_FC* | 0x4003_0000 | 0x10000 | - | - | - |
| UART_STDIO | 0x4060_0000 | 0x10000 | 9600 | 8 | None |

Implemented using GPIO IP core. RTS is connected in port 1 (Write only), CTS in port 2 (Read only).

More information:

http://www.xilinx.com/support/documentation/ip_documentation/axi_gpio/v2_0/pg144-axi-gpio.pdf

UART 1 and UART 2 Registers

| UART 1/2 | Data Size (bits) | Depth | Access Permission | Address Offset | Interconnect |
|-----------|------------------|-------|-------------------|----------------|--------------|
| RECV_FIFO | 32 | 16 | R | 0x00000000 | AXI lite |
| TRAN_FIFO | 32 | 16 | W | 0x00000004 | AXI lite |
| STAT_REG | 32 | 1 | R | 0x00000008 | AXI lite |
| CONT_REG | 32 | 1 | W | 0x0000000C | AXI lite |

More information in:

http://www.xilinx.com/support/documentation/ip_documentation/axi_uartlite/v2_0/pg142-axi-uartlite.pdf

Pin Locations (Pmod_USB_UART)

| UART 2 | ARTY PIN | PmodUSBUART Pin |
|--------|------------|-----------------|
| CTS | JA1 | 1 |
| Tx | JA2 | 2 |
| Rx | JA3 | 3 |
| RTS | JA4 | 4 |
| | GND | 5 |
| | VCC (3.3V) | 6 |

Digilent PmodUSBUART use the new signal assignment convention. More information in:
<https://digilentinc.com/Products/Detail.cfm?NavPath=2,401,928&Prod=PMOD-USB-UART>

Pin Locations (RS232_PMODs)

| UART 2 | Zedboard PIN | Pmod RS232 Pin |
|--------|--------------|----------------|
| CTS | JD1 | 1 |
| RTS | JD2 | 2 |
| Rx | JD3 | 3 |
| Tx | JD4 | 4 |
| | GND | 5 |
| | VCC (3.3V) | 6 |

Digilent Pmods RS232 use the old UART interface. More info in:

<https://digilentinc.com/Products/Detail.cfm?NavPath=2,401,463&Prod=PMOD-RS232>

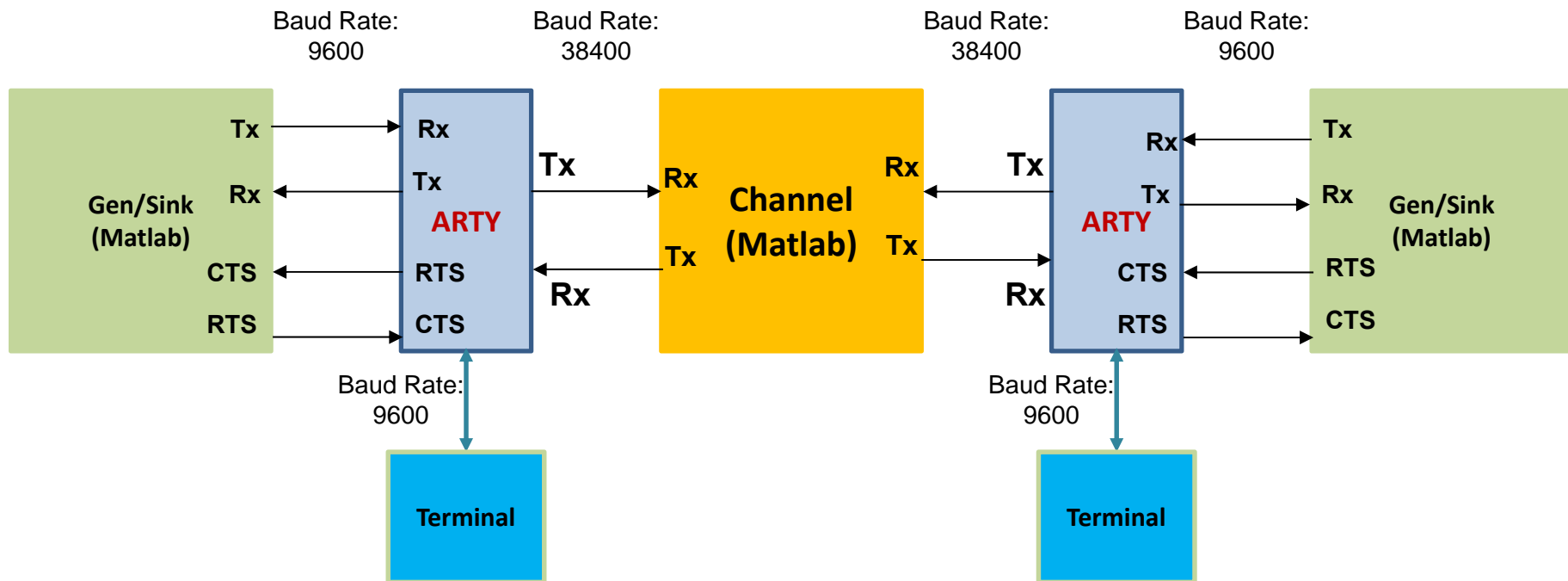
AXI Timers

| Peripherals | AXI-Lite Base Address | Depth (Bytes) | Input clock Frequency |
|-------------|-----------------------|---------------|-----------------------|
| Timer_0 | 0x41C0_0000 | 0x10000 | 100 MHz |
| Timer_1 | 0x41C1_0000 | 0x10000 | 100 MHz |
| Timer_2 | 0x41C2_0000 | 0x10000 | 100 MHz |

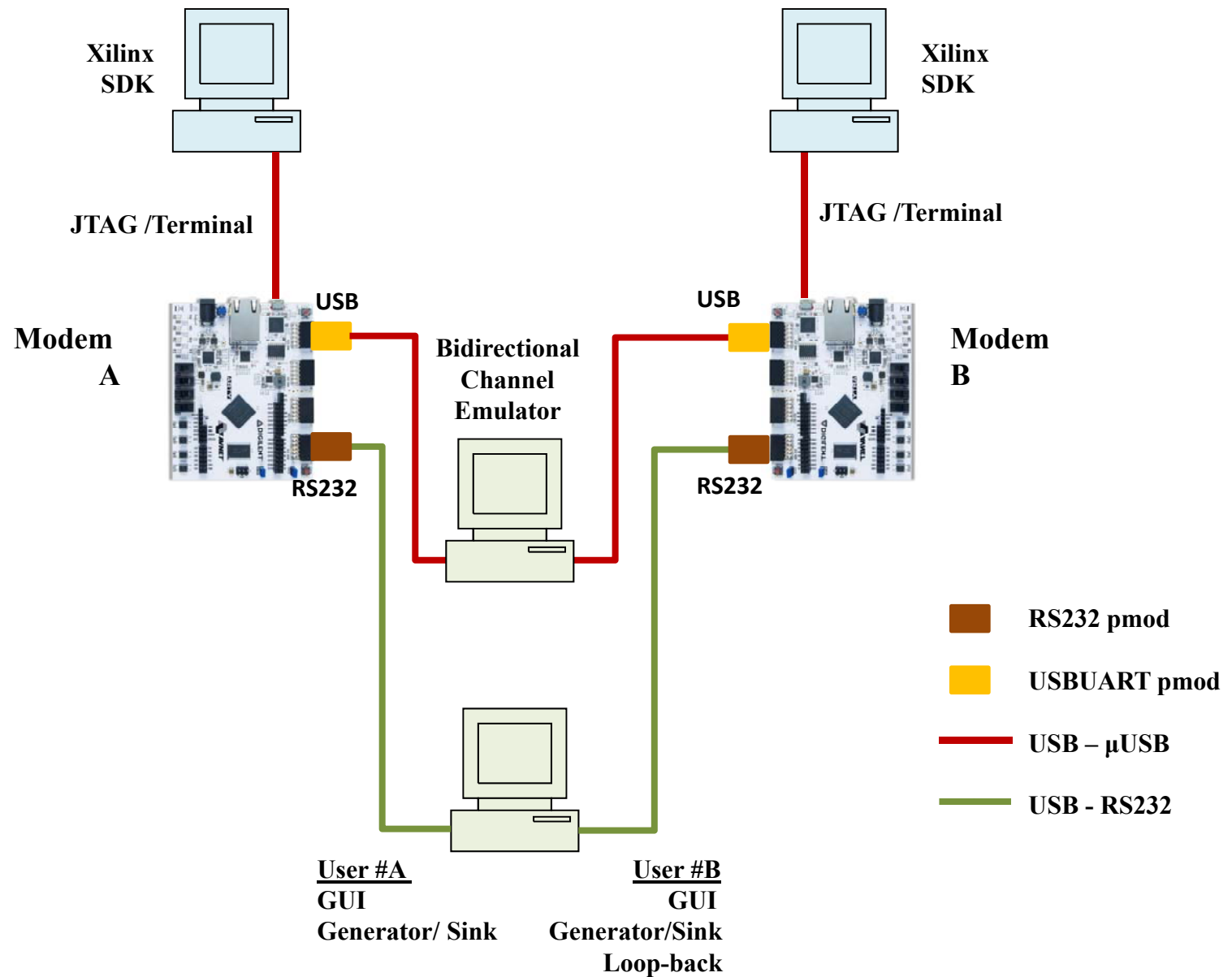
More information in:

http://www.xilinx.com/support/documentation/ip_documentation/axi_timer/v2_0/pg079-axi-timer.pdf

Reference Setup



Συνδεσμολογία



Additional Documentation

- [Digilent ARTY](https://reference.digilentinc.com/doku.php?id=arty)
<https://reference.digilentinc.com/doku.php?id=arty>
- [Xilinx SDK User Guide](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/SDK_Doc/index.html)
http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/SDK_Doc/index.html
- [MicroBlaze version 9.5](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/ug984-vivado-microblaze-ref.pdf)
http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_4/ug984-vivado-microblaze-ref.pdf
- [AXI Interrupt Controller version 4.1](http://www.xilinx.com/support/documentation/ip_documentation/axi_intc/v4_1/pg099-axi-intc.pdf)
http://www.xilinx.com/support/documentation/ip_documentation/axi_intc/v4_1/pg099-axi-intc.pdf
- [AXI UARTlite version 2.0](http://www.xilinx.com/support/documentation/ip_documentation/axi_uartlite/v2_0/pg142-axi-uartlite.pdf)
http://www.xilinx.com/support/documentation/ip_documentation/axi_uartlite/v2_0/pg142-axi-uartlite.pdf
- [AXI GPIO version 2.0](http://www.xilinx.com/support/documentation/ip_documentation/axi_gpio/v2_0/pg144-axi-gpio.pdf)
http://www.xilinx.com/support/documentation/ip_documentation/axi_gpio/v2_0/pg144-axi-gpio.pdf
- [AXI Timer version 2.0](http://www.xilinx.com/support/documentation/ip_documentation/axi_timer/v2_0/pg079-axi-timer.pdf)
http://www.xilinx.com/support/documentation/ip_documentation/axi_timer/v2_0/pg079-axi-timer.pdf