NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

EXAMINATION FOR

Semester 2 AY2008/9

CS2100 – COMPUTER ORGANISATION

April 2009 **Time allowed: 2 hours**

INSTRUCTIONS TO CANDIDATES

1. This examination paper consists of **SIXTEEN (16)** questions and comprises **NINE (9)** printed pages.
2. This is an **OPEN BOOK** examination.
3. Answer all questions.
4. Write your answers in the **ANSWER SCRIPT** provided.
5. Fill in your Matriculation Number with a pen, clearly on every page of your ANSWER SCRIPT.
6. You may use pencil to write your answers.
7. You are to submit only the ANSWER SCRIPT and no other document.

SECTION A (10 Multiple Choice Questions: 20 Marks)

Each question has one correct answer. Write your answer in the space provided in the ANSWER SCRIPT. Two marks are awarded for each correct answer and no penalty for wrong answer.

1. Given an unknown self-complementing code, **139** is represented as "0101 1100 0000" in that code. How is **608** represented?

   A. 1010 0011 1111
   B. 0000 1100 0101
   C. 0011 1010 1111
   D. 0011 1111 1010
   E. Impossible

2. Given the following two Boolean functions:

   $F(A,B,C) = \Sigma\, m(0, 2, 6)$
   $G(A,B,C) = \Sigma\, m(1, 2, 4, 6)$

   What is the Boolean function $\boldsymbol{H(A,B,C) = F(A,B,C) + G(A,B,C)}$?

   A. $H(A,B,C) = A' \cdot B' + C'$
   B. $H(A,B,C) = B \cdot C'$
   C. $H(A,B,C) = A' \cdot B' + B' \cdot C'$
   D. $H(A,B,C) = 0$
   E. None of the above

3. Giving the following assembly code in a stack architecture:

```
push @a0
push @a1
add
push @a2
mul
push @a3
add
pop @a4
```

   a0, a1, a2, a3, and a4 are associated with variables a, b, c, d, and e respectively. Which of the following C codes corresponds to the above assembly code? Note that multiplication (*) has a higher precedence than addition (+).

   A. `e = a + b * c + d;`
   B. `e = (a + b) * (c + d);`
   C. `e = (a + b) * c + d;`
   D. `e = a + b * (c + d);`
   E. None of the above

4. The table below shows three classes of instructions (*A*, *B*, *C* and *D*) and their respective CPI and number of instructions in a program.

Class	CPI	Number of instructions (million)
A	2	40
B	3	20
C	6	20

What is the average CPI of the program?

A. 2.67
B. 2.75
C. 2.90
D. 3.00
E. 3.25

5. Refer to question 4. If we choose to speed up one of the classes by a certain factor X, which of the following choices would enable us to get an overall speed-up of 1.1818?

(i) Class *A*, X = 2
(ii) Class *B*, X = 3
(iii) Class *C*, X = 3

A. (i) only
B. (ii) only
C. (iii) only
D. Either (i) or (ii) only
E. Either (ii) or (iii) only

6. Given the following MIPS code:

```
lw  $t0, 100($s0)
add $t2, $t0, $t1
```

On a 5-stage MIPS pipeline, how many cycles does it take to execute the code without forwarding? How about with forwarding?

A. Without forwarding: 7 cycles; with forwarding: 6 cycles
B. Without forwarding: 7 cycles; with forwarding: 5 cycles
C. Without forwarding: 8 cycles; with forwarding: 7 cycles
D. Without forwarding: 8 cycles; with forwarding: 6 cycles
E. None of the above

7. A machine has 16-bit instructions and 5-bit addresses. There are two classes of instructions: class *A* instructions have one address, while class *B* instructions have two addresses. Both classes exist and the encoding space for opcode is completely utilized. What is the minimum total number of instructions?

A. 2
B. 32
C. 33
D. 95
E. 96

8. Refer to question 7. What is the maximum total number of instructions?

A. 96
B. 1023
C. 2017
D. 2048
E. 2112

9. Which of the following is a valid MIPS instruction?

A. `sw $s3, $t0(12)`
B. `ori $t1, $t2, 0xCCCC0000`
C. `srl $s0, $s0, 8`
D. `subi $t3, $t2, 10`
E. None of the above

10. Which of the following types of cache has no conflict miss?

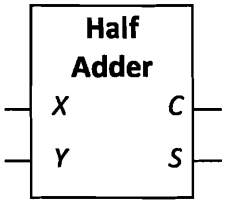
A. Direct-mapped
B. Two-way Set Associative
C. Four-way Set Associative
D. Fully Associative
E. None of the above

SECTION B (6 Questions: 80 Marks)

11. [8 marks] A **4-bit standard Gray-code to binary converter** takes a 4-bit standard Gray-code value *ABCD* as its input and generates its binary equivalent *WXYZ*.

    a. Create such a converter by using only half adders without any additional logic gates. The block diagram of a half adder is shown below. The half adder takes the inputs *X* and *Y* and produces the outputs *C* (carry) and *S* (sum). [6 marks]

    b. The half adder device consists of an AND gate and an XOR gate. Assuming that the propagation delay of a logic gate is *T*, what is the propagation delay of this converter? [2 marks]



12. [10 marks] The **84-2-1 code** is used to represent the ten decimal digits 0 – 9.

    a. Given a 4-bit input *ABCD* representing the 84-2-1 code, fill in the truth table in the answer script such that the output *F* is 1 if *ABCD* represents a value that is divisible by 4, and is 0 if the input value is not divisible by 4. [2 marks]

    b. What is the simplified SOP expression of *F*? [2 marks]

    c. Implement *F* using a single logic gate. [1 mark]

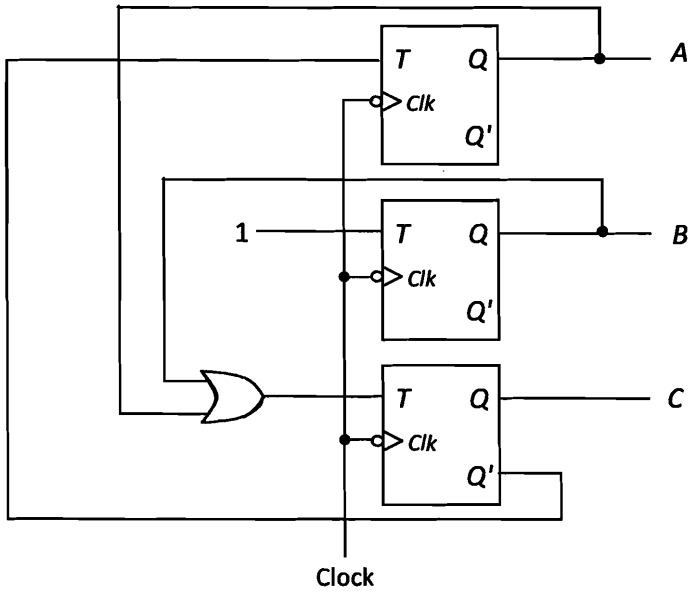
    d. Using a single 2×4 decoder without any logic gate, implement *F*. [2 marks]

    e. Using a single 8:1 multiplexer without any logic gate, implement *F*. You are allowed to use only logic constants 0 and 1 for the eight inputs. [3 marks]

13. [8 marks] The figure below shows a **sequential circuit** with three *T* flip-flops.

    a. Complete the state table. [6 marks]

    b. If the initial state is 000, what are the next 5 states of this circuit? [2 marks]



14. [20 marks]
Study the following MIPS code. The comment on each line includes the instruction number for ease of reference.

```
        addi $s0, $zero, 10      # I1
Loop:   lw   $t0, 0($s2)         # I2
        add  $t1, $t0, $t0       # I3
        add  $t1, $t1, $t0       # I4
        lw   $t2, 0($s3)         # I5
        add  $t4, $t1, $t2       # I6
        sw   $t4, 0($s3)         # I7
        addi $s2, $s2, 4         # I8
        addi $s3, $s3, 4         # I9
        addi $s0, $s0, -1        # I10
        beq  $s0, $zero, Done    # I11
        j    Loop                # I12
Done:
```

a. Associating **$s0** with the integer variable **i**, and **$s2** and **$s3** the base addresses of the 32-bit integer arrays **A** and **B** respectively, write a Java or C code that corresponds to the above MIPS code. [6 marks]

b. How many MIPS instructions are executed in the code? [2 marks]

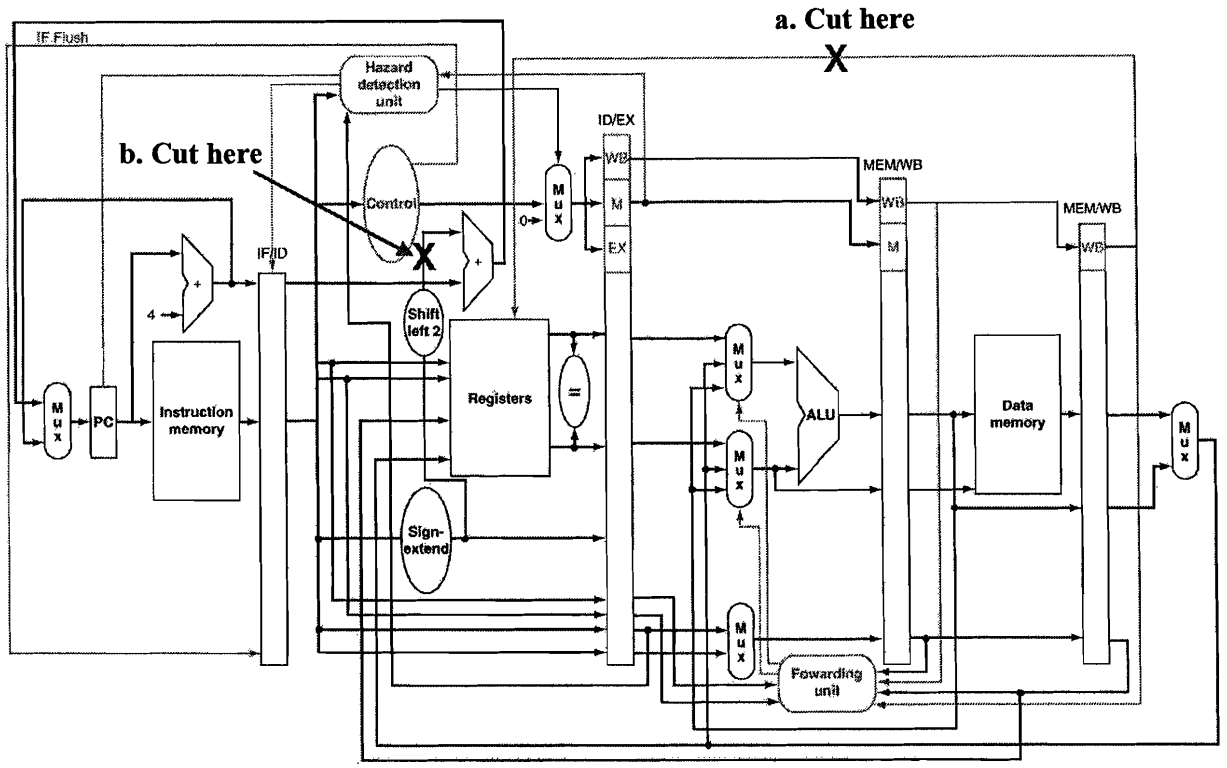
c. Assuming that the first instruction (I1) is at address 400 (in decimal), what is the immediate value (in decimal) in the **j** instruction (I12)? [2 marks]

d. Assuming a 5-stage MIPS pipeline with forwarding but no branch prediction (branch is resolved in the ID stage), list out all the data and control dependencies in the code that will cause delay in the pipeline, and the delay amount for each of the dependencies. You may refer to the instructions by their numbers (I1 to I12) in your answer. [4 marks]

e. Make a simple modification to the code so that it runs in fewer number of instructions. You do not need to write out the complete code; you only need to indicate the changes. [2 marks]

f. You have modified the code in part (e). Assuming a 5-stage MIPS pipeline with forwarding and branch prediction (branch is resolved in the ID stage and all branches are predicted non-taken), how many cycles of delay are incurred for branch misprediction in your modified code? How many cycles in total will it take to execute the modified code? [4 marks]

15. [16 marks]



For parts (a) and (b), refer to the MIPS datapath above.

Parts (a) and (b) are independent of each other.

a. Describe the negative consequence of cutting the line (a. Cut here). Write a short MIPS code that would fail if this line is cut. [3 marks]

b. Describe the negative consequence of cutting the line (b. Cut here). Write a short MIPS code that would fail if this line is cut. [3 marks]

c. Is it possible to design a test that would determine if there is a stuck-at-1 fault on each of the following two signals? If it is possible, write out the test and explain how your test works. If it is not possible, explain too. [4 marks]

   i. Bit 5 of instruction word
   ii. MemtoReg signal of control unit

For parts (d) to (f), refer to the following MIP instruction:

```
lw  $t0, 24($t1)
```

d. Write out the instruction in hexadecimal representation. [2 marks]

e. What are the values supplied to the "Read register 1" and "Read register 2" inputs of the register file? Are the values in the registers actually used? [2 marks]

f. What are the data input values of the ALU? [2 marks]

16. [18 marks]
A machine has word size of 8 bytes, a main memory of 64K bytes and a two-way set associative cache of 8 sets. The cache hence contains 16 blocks in total. Each block contains 2 words, or 16 bytes.

a. How many bits are there in the tag field, set index field, and byte offset field of the address? [3 marks]

b. [You may want to do both parts (b) and (c) together. Part (c) is on the next page.]

Given a sequence of read memory references as shown in the table below, where each memory reference is a byte address given in both decimal and hexadecimal forms, indicate whether the reference is a hit or a miss.

Assume that the cache is initially empty. If both blocks in a set are empty, fill in the left block first. If both blocks in a set are filled, replace the one that is least recently accessed, that is, apply the LRU policy for replacement. [7 marks]

Memory address		Hit or Miss?
(in decimal)	(in hexadecimal)	
211	0x00D3	Miss
464	0x01D0	
311	0x0137	
300	0x012C	
218	0x00DA	
292	0x0124	
319	0x013F	
722	0x02D2	

Fill in the table in the answer script.

16. (cont.)

c. Given the above sequence of read memory references, fill in the contents of the cache. If a particular block is to be replaced, cross out the content and fill in the new content.

Use the notation **M[*i*]** to denote the word starting at memory address *i*.

You may write the value in decimal or hexadecimal. If you write in hexadecimal, use the 0x prefix. [8 marks]

	Left block			Right block		
Index	Tag value	Word 0	Word 1	Tag value	Word 0	Word 1
0						
1						
2						
3						
4						
5						
6						
7						

Fill in the table in the answer script.