NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

EXAMINATION FOR

Semester 2 AY2007/8

CS2100 – COMPUTER ORGANISATION

May 2008 **Time allowed: 2 hours**

INSTRUCTIONS TO CANDIDATES

1. This examination paper consists of **TWENTY TWO (22)** questions and comprises **ELEVEN (11)** printed pages.
2. This is an **OPEN BOOK** examination.
3. Answer all questions.
4. Write your answers in the **ANSWER SCRIPT** provided.
5. Fill in your Matriculation Number with a pen, clearly on every page of your ANSWER SCRIPT.
6. You may use pencil to write your answers.
7. You are to submit only the ANSWER SCRIPT and no other document.

SECTION A (15 Multiple Choice Questions: 30 Marks)

Each question has one correct answer. Write your answer in the space provided in the ANSWER SCRIPT. Two marks are awarded for each correct answer and no penalty for wrong answer.

1. How many unique minterms does the following Boolean function contain?

$$F(A,B,C,D,E) = B \cdot D' \cdot E + A' \cdot C + A' \cdot B \cdot C \cdot D$$

A. 7
B. 10
C. 11
D. 12
E. 14

2. Given the following Boolean function:

$$F(A,B,C,D) = \Sigma\, m(0, 2, 8, 11) + d(3, 10, 15)$$

What is its complement function F' ?

A. $\Pi\, M(1, 4, 5, 6, 7, 9, 12, 13, 14)$
B. $\Pi\, M(1, 4, 5, 6, 7, 9, 12, 13, 14) \cdot d(3, 10, 15)$
C. $\Pi\, M(0, 2, 8, 11)$
D. $\Pi\, M(0, 2, 8, 11) \cdot d(3, 10, 15)$
E. None of the above

3. Which of the following expressions is equivalent to function F in question 2 above?

A. $B' \cdot (C + D')$
B. $B' \cdot (C' + D)$
C. $B' \cdot D' + C$
D. $B' \cdot (C' \cdot D' + C \cdot D)$
E. None of the above

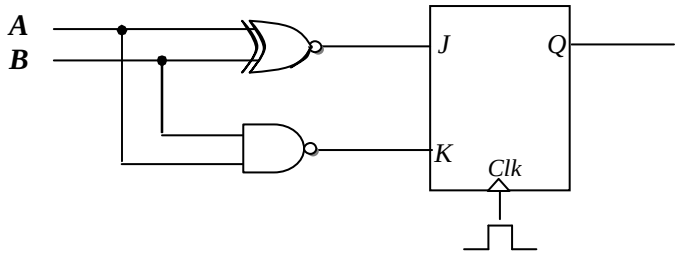
4. Which of the following is the software you used in some of your lab sessions?

   A. logicsim
   B. logisim
   C. logsim
   D. losim
   E. lsim

5. Assume a floating-point number scheme with 1-bit sign, 6-bit normalised mantissa, and 5-bit one's complement exponent. Which of the following is the closest representation for the decimal value **18.8**?

   A. 0 100101 11010
   B. 0 100110 11010
   C. 0 100101 00101
   D. 0 100110 00011
   E. 0 100110 00101

6. Which of the following sets of input values corresponds to a toggle command?



   A. $A = 0; B = 0$
   B. $A = 0; B = 1$
   C. $A = 1; B = 0$
   D. $A = 1; B = 1$
   E. None of the above.

7. Instruction set architecture is an interface between

   A. digital circuit and datapath control.
   B. application software and operating system.
   C. software and hardware organisation.
   D. compiler and programming language.
   E. memory and processor.

8. The total number of instructions executed in a program can be changed by

   A. changing the ISA of the processor.
   B. reducing the number of cycles needed to execute each instruction class in a program.
   C. increasing the clock rate of the processor.
   D. doubling the individual CPI of each instruction class executed in a program.
   E. None of the above.

9. Which of the following laws states that performance is limited to the non-speedup portion of a program?

   A. Moore's law
   B. DeMorgan's law
   C. Gustafson's law
   D. Amdahl's law
   E. Brooks' law

10. A certain machine has 16-bit instructions and 6-bit addresses. There are two classes of instructions: class *A* instructions have two addresses, while class *B* instructions have one address. All two classes exist and the encoding space for opcode is completely utilized. What is the minimum total number of instructions?

    A. 2
    B. 31
    C. 32
    D. 79
    E. 240

11. Refer to question 10 above. What is the maximum total number of instructions?

    A. 1040
    B. 961
    C. 960
    D. 241
    E. 240

12. Assuming a 5-stage MIPS pipeline, in what stage does the instruction **`add $t0, $t1, $t2`** perform the addition operation?

    A. IF
    B. ID
    C. EX
    D. MEM
    E. WB

13. Which pseudo-instruction corresponds to the following code?

```
slt $at, $t1, $t2
beq $at, $zero, L
```

    A. `blt $t1, $t2, L  # if ($t1 < $t2) goto L`
    B. `ble $t1, $t2, L  # if ($t1 <= $t2) goto L`
    C. `bgt $t1, $t2, L  # if ($t1 > $t2) goto L`
    D. `bge $t1, $t2, L  # if ($t1 >= $t2) goto L`
    E. None of the above

14. The five stages of a 5-stage pipeline take 2 ns, 3 ns, 1 ns, 4 ns, and 2 ns. If there are 100 instructions, what is the maximum speedup in the execution time of a pipeline implementation compared to a single-cycle implementation?

    A. 2.14
    B. 2.88
    C. 2.94
    D. 3.00
    E. 4.00

15. In a fully-associative cache with a 20-bit long tag field in the 32-bit address, which of the following statements is true?

    A. There are 2^{20} blocks in the cache.
    B. There are 2^{20} blocks in the memory.
    C. There are 2^{12} blocks in the cache.
    D. There are 2^{12} blocks in the memory.
    E. None of the above.

SECTION B (7 Questions: 70 Marks)

16. Given this code:

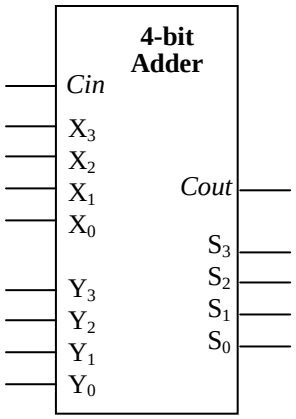
```
int n = 2147483640;
for (int i=1; i<=10; i++)
    n = n + 1;

System.out.println("n = " + n);
```

Given also that `int` type uses 32 bits, and that 2^{32} = 4294967296. What is the output of the above code? Explain your output. [5 marks]

17. Design a multiply-by-5 circuit using at most two 4-bit parallel adders. (A 4-bit parallel adder is shown below). The circuit takes in a 3-bit input *ABC* which has a value in the range [0, 5], and generates a 5-bit output *VWXYZ* that is 5 times the value of the input. No additional logic gate should be used to generate this 5-bit output.

The circuit also generates an output *E* (error), which is 1 if the input is invalid, or 0 otherwise. You are to use a single 2-input logic gate to implement *E*.

Draw the circuit, and briefly explain your solution in a sentence or two. [10 marks]



18. [12 marks]

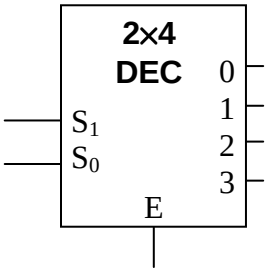
(a) The majority function *F(A,B,C,D)* generates 1 if among the inputs *A*, *B*, *C*, *D* there are more 1s than 0s. Otherwise, it generates 0. For example, if *ABCD* = 0010 or *ABCD* = 0101, then *F* = 0; if *ABCD* = 1101, then *F* = 1.

Give the simplified SOP expression for *F*. [4 marks]

(b) Given the following function:

$$G(A,B,C,D) = \Sigma\, m(2, 8)$$

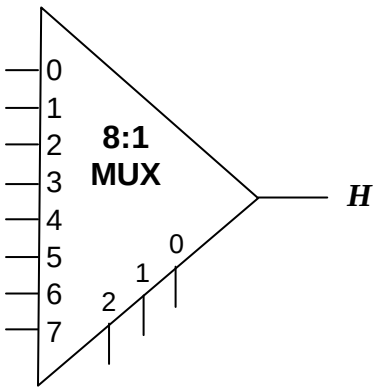
Implement this function using a single 2×4 decoder with one-enable (as shown below) and at most one 2-input logic gate. (Only partial credits will be given if you use an additional decoder or an additional gate.) [4 marks]



(c) Given the following function:

$$H(A,B,C,D) = \Sigma\, m(2, 5, 8, 10, 12, 13, 15)$$

Implement this function using a single 8:1 multiplexor (as shown below) with no additional logic gate. Complemented literals are not available. (Only partial credits will be given if you use complemented literals.) [4 marks]



19. [8 marks]
The table below shows two implementations M1 and M2 of the same instruction set, which consists of four classes of instructions (*A*, *B*, *C* and *D*), as well as the number of instructions executed in a certain program using the instruction set.

M1 has a clock rate of 2GHz. M2 has a clock rate of 2.5GHz.

Class	**CPI for M1**	**CPI for M2**	**Number of instructions**
A	1	2	80000000000
B	2	2	60000000000
C	2	3	40000000000
D	5	3	20000000000

(a) Calculate the average CPI for the program on M1, and on M2. [2 marks]

(b) Which machine is faster and by how much? Correct your answer to 3 decimal places. [2 marks]

(c) The makers of M2 want to reduce the CPI of one of the 4 classes of instructions by 1, to match the average CPI of the program on M1. Which class of instructions should be chosen? [2 marks]

(d) A new hardware for M1 can achieve a speedup of 2 for class-*A* insructions. What would be the overall speedup for the program on M1? Correct your answer to 3 decimal places. [2 marks]

20. [18 marks]
An array *A* contains a number of elements where each element is an integer occupying a word. The base address of *A* is stored in register **$s0**. The MIPS code below computes some result in register **$s1**.

```
      add  $t0, $zero, $zero  # I1
      addi $t1, $zero, 40     # I2
      add  $s1, $zero, $zero  # I3

Loop: add  $s2, $s0, $t0      # I4
      lw   $t2, 0($s2)        # I5
      andi $t3, $t2, 1        # I6
      bne  $t3, $zero, Here   # I7
      add  $s1, $s1, $t2      # I8

Here: addi $t0, $t0, 4        # I9
      bne  $t0, $t1, Loop     # I10
```

(a) What is the minimum and maximum number of instructions executed? [2 marks]

(b) If **$s1** is associated with the integer variable **sum**, write a Java or C code that corresponds to the above MIPS code. Explain what the code does in one sentence. [8 marks]

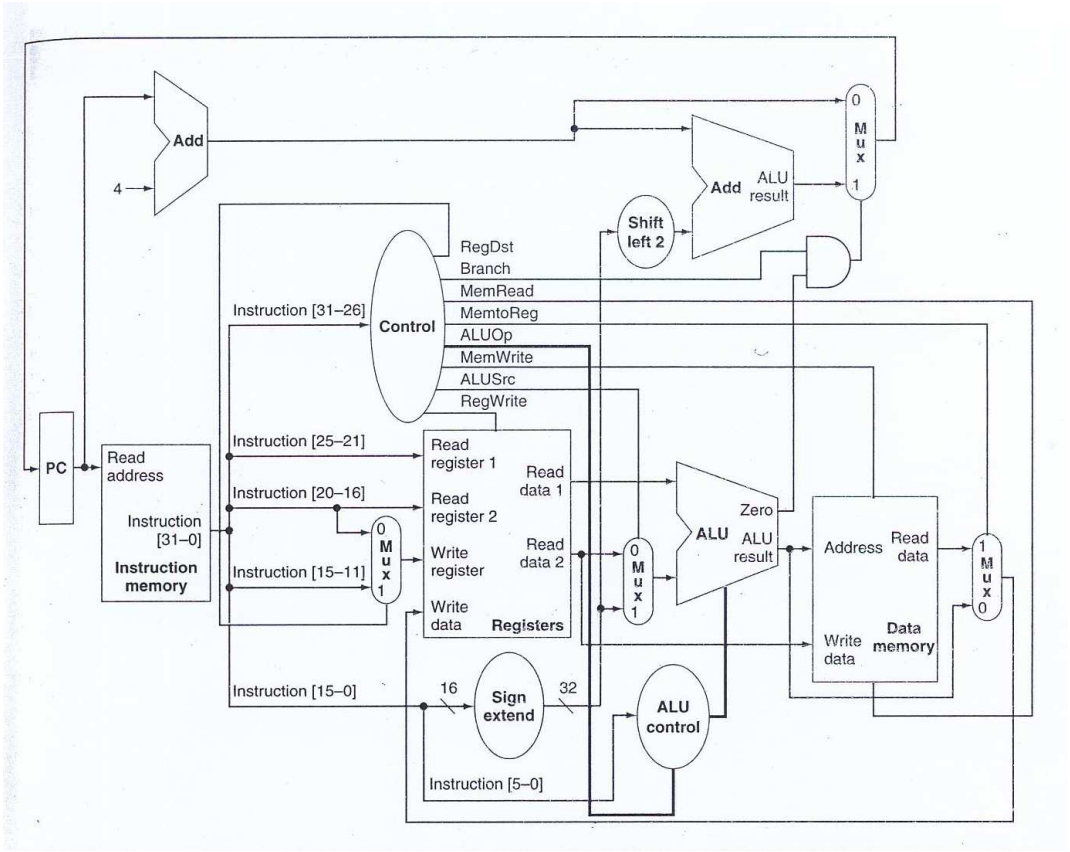
(c) For each of the two **bne** instructions in the code above, determine the value in the immediate field, and hence write out the binary representation of the instruction. Below are some essential information: [4 marks]

opcode for **bne** (in decimal) = 5
$zero = $0; $t0 = $8; $t1 = $9; $t3 = $11

(i) **bne $t3, $zero, Here**
(ii) **bne $t0, $t1, Loop**

(d) Assuming a 5-stage MIPS pipeline with forwarding but no branch prediction (branch is resolved in the ID stage), list out all the data and control dependencies in the code that will cause delay in the pipeline, and the delay amount for each of the dependencies. You may refer to the instructions by their numbers (I1 to I10) in your answer. [4 marks]

21. [7 marks]
We wish to add the **`sll`** (shift left logical) instruction to the single-cycle datapath as shown in the figure below.



(a) Add any necessary datapath(s) and control signal(s) to the figure in the answer script. [3 marks]

(b) The table below shows the truth table of the ALU control unit for some R-format instructions. Make the necessary changes to the entries for the **`add`** instruction, and fill in the entries for the **`sll`** instruction. [4 marks]

Instr	ALUOp		Funct Field						Operation
	ALUOp1	ALUOp0	F5	F4	F3	F2	F1	F0	
`add`	**1**	**X**	**X**	**X**	**0**	**0**	**0**	**0**	**0010**
`sub`	1	X	X	X	0	0	1	0	0110
`and`	1	X	X	X	0	1	0	0	0000
`or`	1	X	X	X	0	1	0	1	0001
`slt`	1	X	X	X	1	0	1	0	0111
`sll`									

Fill in the table in the answer script.

22. [10 marks]
A machine with a word size of 16 bits and address width of 32 bits has a direct-mapped cache with 16 blocks and a block size of 2 words.

(a) Given a sequence of memory references as shown below, where each reference is given as a byte address in both decimal and hexadecimal forms, indicate whether the reference is a hit (H) or a miss (M). Assume that the cache is initially empty. [5 marks]

Memory address		Hit (H) or Miss (M)?
(in decimal)	(in hexadecimal)	
4	4	M
92	5C	
7	7	
146	92	
30	1E	
95	5F	
176	B0	
93	5D	
145	91	
264	108	
6	6	

Fill in the table in the answer script.

(b) Given the above sequence of memory references, fill in the final contents of the cache. Use the notation M[*i*] to denote the word at memory address *i*. [5 marks]

Index	Tag value	Word 0	Word 1
0			
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			

Fill in the table in the answer script.

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