NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

TERM TEST #2
AY2012/3 Semester 2

CS2100 — COMPUTER ORGANISATION

13 April 2013 Time Allowed: **1 hour 15 minutes**

INSTRUCTIONS

1. This question paper contains **TEN (10)** questions and comprises **TEN(10)** printed pages.
2. The last three pages are for your reference and rough work. They contain the "datapath and control" diagram and empty timing charts.
3. An **Answer Sheet**, comprising **TWO (2)** printed page, is provided for you.
4. Answer **ALL** questions within the space provided on the **Answer Sheet**.
5. Maximum score is **30 marks**.
6. This is a **CLOSED BOOK** test. However, a handwritten single-sheet double-sided A4 cheat sheet is allowed.
7. Write legibly with a pen or pencil (at least 2B).
8. Calculators and computing devices such as laptops and PDAs are not allowed.
9. Submit only the **Answer Sheet** at the end of the test. You may keep the question paper.
10. Write your **MATRICULATION NUMBER** on the **Answer Sheet** using a **PEN**.

——— END OF INSTRUCTIONS ———

SECTION A (6 Multiple Choice Questions: 12 marks)

Each question has only one correct answer. Write your answer in the space provided on the **Answer Sheet**. Two marks are awarded for each correct answer and no penalty for wrong answer.

1. Suppose there are 20 memory load instructions in a program with 100 instructions and we reduce the cycles required for the load instruction by 50%. What is the speedup for this program?

   A. 1.2 (20% improvement)
   B. 1.5 (50% improvement)
   C. 1.1 (10% improvement)
   D. Not enough information for a definite answer
   E. None of the above

2. Given that the opcode for "addi" is $\mathbf{8_{16}}$. The instruction encoding (in hexadecimal) for "**`addi $2, $4, -3`**" is:

   A. **`0x20 82 00 03`**
   B. **`0x20 82 FF FD`**
   C. **`0x20 44 00 03`**
   D. **`0x20 44 FF FD`**
   E. None of the above

3. The pseudo-instruction "**`ble $s0, $s1, there`**" (branch-less-or-equal) can be translated to:

   A.
   ```
   slt $t0, $s0, $s1
   beq $t0, $zero, there
   ```

   B.
   ```
   slt $t0, $s0, $s1
   bne $t0, $zero, there
   ```

   C.
   ```
   slt $t0, $s1, $s0
   beq $t0, $zero, there
   ```

   D.
   ```
   slt $t0, $s1, $s0
   bne $t0, $zero, there
   ```

   E. None of the above

4. Given a **4-stage single cycle processor** with the following information:

	Stage 1	Stage 2	Stage 3	Stage 4
Time Needed	**2ns**	**1ns**	**3ns**	**2ns**

How much time is needed to execute 100 instructions on this processor?

A. 100ns
B. 200ns
C. 800ns
D. 1200ns
E. None of the above

5. This question uses the same information given in Q4. Suppose we change the processor to a pipeline design. Three pipeline latches are added, each with a delay of 1ns. What is the total time needed to execute 100 instructions on this new processor? You can assume the instructions are free of instruction dependencies (i.e. no hazards).

A. 309ns
B. 400ns
C. 412ns
D. 416ns
E. None of the above

6. Given the MIPS instruction "**`beq $7, $0, -10`**" at address 0x400040, where can we find the branch target in memory?

A. **`0x40 00 18`**
B. **`0x40 00 1C`**
C. **`0x40 00 30`**
D. **`0x40 00 31`**
E. None of the above

SECTION B (Bonus Question: 1 mark)

This is a bonus question. The mark of this question will be added only if the total mark scored is less than 30.

7. The lecturer loves to use strange analogies in the lecture, which of the following **is NOT used?**

   A. Uncle Soo rolls down the slopes while jogging.

   B. Lord of the rings.

   C. Falling in love with a computer.

   D. Ostrich sticking its head in the sand.

   E. Harry Potter.

SECTION C (Questions: 18 marks)

Write your answer in the space provided on the **Answer Sheet**. You do not need to show workings, unless otherwise stated.

8. Take a look at the following MIPS program and the memory content. **For simplicity, all values (memory address and content) are in decimal. [4 marks]**

```
#s1 is initialized to 0
#t0 is initialized to 112

loop:
      beq $t0, $zero, exit
      lw  $t1, 0($t0)
      add $s1, $s1, $t1
      lw  $t0, 4($t0)
      j   loop
exit:
```

Address	Content
100	120
104	132
108	128
112	108
116	124
120	116
124	104
128	100
132	136
136	112

Suppose we execute the code for **3 iterations**, answer the following:

(a) Give the value of register $s1 at the end of the 3rd iteration. **[2 marks]**

(b) If we want to terminate the loop at the 4th check of "beq", some memory contents need to be modified. Give the **address(es)** and the **modified content(s)** to achieve this. You should find the minimum changes required. **[2 marks]**

9. Suppose the following code is executed on a 5-stage MIPS pipeline processor. **[5 marks]**

`add $12, $15, $23`	`#i1`
`lw  $10, 24($12)`	`#i2`
`sub $7, $12, $10`	`#i3`
`add $9, $10, $23`	`#i4`
`or  $9, $3, $5`	`#i5`
`sw  $9, 24($12)`	`#i6`

(Note: Use the timing chart on page 10 to help.)

(a) Let us label the two forwarding paths as follows:

A. From EX/MEM pipeline latch to ALU unit

B. From MEM/WB pipeline latch to ALU unit

For each of the instructions, indicate which receiving instruction(s) it passes the result to, and via which forwarding path(s). For example:

	Forward to	Via
#i7	#i9	A

Indicates instruction #i7 uses forwarding path "(**A**) From EX/MEM to ALU unit" to pass result to instruction #i9**. Note that you need to get both parts correct to earn marks. [4 marks]**

(b) How many cycles are needed for the code if all forwarding paths in (a) are implemented? **[1 mark]**

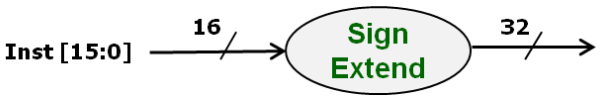
10. The I-format instructions in MIPS can expand the immediate field (16-bit) to a 32-bit value in two ways:

Expansion Type	Example Instructions	Expansion of the immediate field
Sign Extended	`addi $3, $7, 5` `addi $3, $7, -5`	0x00 05 ➔ 0x00 00 00 05 0xFF FB ➔ 0xFF FF FF FB
Zero Padded	`ori $3, $7, 0xFFFB`	0xFF FB ➔ 0x00 00 FF FB

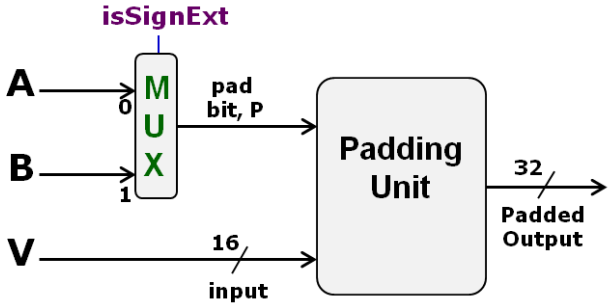
Essentially, the logical operations (andi, ori, xori) covered in this course expand the immediate by performing zero-padding instead of sign extension.

Suppose we want to extend the simple MIPS datapath and control design to handle the set of logical operations (andi, ori and xori). This question will deal with only the modification required to handle the two types of immediate field expansion.

Let us upgrade the original datapath element that handles the expansion from:



to



The "padding unit" takes in a 16-bit input value **V** and a 1-bit pad bit **P**, it will then output a 32-bit value by padding the most significant 16 bits with the pad bit **P** and the lower 16 bit with the input value **V**. A multiplexer is added to handle both types of expansion with the same design. The multiplexer uses the control signal "isSignExt" to either select the upper port (0) or the lower port (1). The control signal should be a "1" when sign extension is required, "0" when zero padding is needed. **[9 marks]**

(a) Give the 1-bit value for the upper and lower ports of the multiplexor. You can use any value readily available in the datapath. No additional logic gate or datapath element is allowed. **[2 marks]**

(b) Indicate an existing component that should handle the generation of the "isSignExt" signal. **[1 mark]**

~~~ Please turn over for part (C) ~~~

(c) Suppose the datapath elements have the following delay:

Inst-Mem / Data Mem	**Adder / *ALU Ctrl***	**MUX**	**ALU**	**Reg.File**	**Control**	**Left-shift / AND / Sign Ext / *Padding Unit***
200ps	30ps	10ps	60ps	100ps	70ps	20ps

(Please note the delay on the ALU Control Unit and the Padding Unit)

Which instruction(s) out of the list {**addi**, **beq**, **sw**} will require a **longer execution time compared to the original design? What is the additional duration required? [6 marks]**

(The complete datapath and control diagram is provided for your reference on page 9.)

——— END OF PAPER ———

This page is for your rough work.

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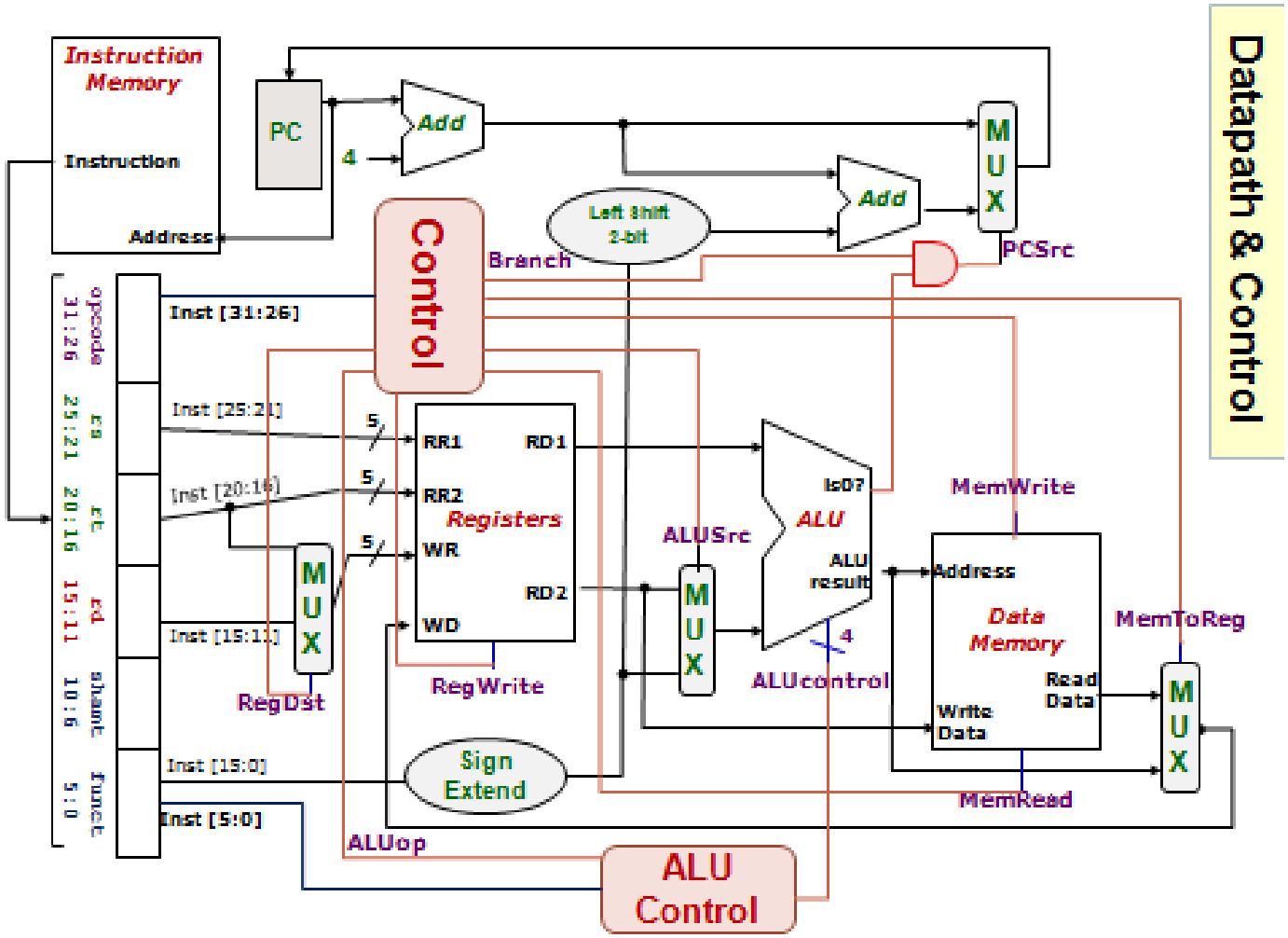

Inst-Mem / Data Mem	Adder / ALU Ctrl	MUX	ALU	Reg.File	Control	Left-shift / AND / Sign Ext / Padding Unit
200ps	30ps	10ps	60ps	100ps	70ps	20ps

This page is for your rough work.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
i1																			
i2																			
i3																			
i4																			
i5																			
i6																			

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
i1																			
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