NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

TERM TEST #2
AY2011/2 Semester 2

CS2100 — COMPUTER ORGANISATION

7 April 2012 Time Allowed: **1 hour 15 minutes**

INSTRUCTIONS

1. This question paper contains **ELEVEN (11)** questions and comprises **EIGHT (8)** printed pages. **TWO (2)** blank pages are included for your rough work.
2. An **Answer Sheet**, comprising **TWO (2)** printed page, is provided for you.
3. Answer **ALL** questions within the space provided on the **Answer Sheet**.
4. Maximum score is **30 marks**.
5. This is a **CLOSED BOOK** test. However, a handwritten single-sheet double-sided A4 cheat sheet is allowed.
6. Write legibly with a pen or pencil (at least 2B).
7. Calculators and computing devices such as laptops and PDAs are not allowed.
8. Submit only the **Answer Sheet** at the end of the test. You may keep the question paper.
9. Write your **MATRICULATION NUMBER** on the **Answer Sheet** using a **PEN**.

——— END OF INSTRUCTIONS ———

SECTION A (6 Multiple Choice Questions: 12 marks)

Each question has only one correct answer. Write your answer in the space provided on the **Answer Sheet**. Two marks are awarded for each correct answer and no penalty for wrong answer.

1. Suppose a binary executable executed on machine M with an **average CPI of 4.2**. If another machine N managed to improve the CPI for the load instruction **from 5 cycles to 4 cycles** as compared to machine M. What is the average CPI of the same executable on N if load instruction takes up 20% of total instruction count?

   A. Average CPI is 3.2
   B. Average CPI is 3.4
   C. Average CPI is 3.8
   D. Average CPI is 4.0
   E. None of the above

2. What is the best description of the behavior of the following MIPS code sequence?

```
lw   $t2, 4( $t0 )
sw   $t0, 4( $t2 )
```

   A. The instruction "**sw**" will cause an error.
   B. **4($t0)** and **4($t2)** refer to the same memory location.
   C. The location **4($t2)** will contain the value "**4**" afterwards.
   D. **$t2** and **$t0** refer to the same memory location.
   E. None of the above.

3. Given that the opcode/funct field of the MIPS instruction **xor** ("Exclusive-Or") is $\mathbf{0}_{16}$ and $\mathbf{26}_{16}$ What is the encoding of the following instruction?

```
xor $8, $4, $2
```

   A. 0x00040208
   B. 0x00428026
   C. 0x00824026
   D. 0x00209046
   E. None of the above

4. Given a MIPS code fragment with 10 non-control-flow instructions (i.e. Arithmetic and memory instructions only). If the code is executed with a 5-stage pipeline processor with no forwarding, what is the most accurate range of the total number of cycles needed?

   A. 14 cycles to 14 cycles (i.e. 14 cycles for all possible 10-instructions program)
   B. 10 cycles to 41 cycles
   C. 14 cycles to 32 cycles
   D. 14 cycles to 41 cycles
   E. None of the above

5. Which of the following statement(s) regarding the jump instruction in MIPS is/are TRUE?
   i. It is possible that a particular "**`j`**" instruction can **only** jump backward to instruction earlier in the code.
   ii. If the same "**`j`**" instruction is executed multiple times (e.g. in a loop), it is possible that different jump targets are specified.
   iii. If a "**`j`**" instruction fails to reach its target due to limitation of the immediate field, it is possible that we can construct a chain of multiple "**`j`**" instructions to reach the target.

   A. (i) only
   B. (i) and (iii) only
   C. (ii) and (iii) only
   D. (ii) only
   E. (i), (ii) and (iii)

6. Given two "**and**" instructions in MIPS with different operands, which of the following statement(s) is/are TRUE regarding the datapath and control?

   i. The control signals for the two instructions are exactly the same.
   ii. The input and output of the various datapath elements for the two instructions are exactly the same.
   iii. The latencies of the two instructions are exactly the same.

   A. (i) only
   B. (i) and (iii) only
   C. (ii) and (iii) only
   D. (ii) only
   E. (i), (ii) and (iii)

SECTION B (1 Bonus Question: 1 mark)

This is a bonus question. The mark of this question will be added only if the total mark scored is less than 30.

7. During the lecture on "Datapath and Control", the lecture associated characters from "The lord of the rings" to the various processor elements. Which of the following association is not the same as those presented in lecture?

   A. Saruman is like the Instruction Memory.

   B. Gandalf is like the ALU Unit.

   C. Aragorn is like the PC.

   D. Arwen is like the MUX(RegDst).

   E. The one-ring is like the main control unit.

SECTION C (4 Questions: 18 marks)

Write your answer in the space provided on the **Answer Sheet**. You do not need to show workings, unless otherwise stated.

8. **[3 marks]** This question uses the MIPS instruction subset: **add**, **sub**, **and**, **or**, **nor**, **beq**, **lw** and **sw** (the same instruction subset used to implement the basic MIPS processor in lecture). We would like to know whether partial information of the datapath and control signals can help to deduce the instruction(s) currently under execution. Give **all possible** instruction(s) from the given subset that can generate the following observed information. Missing or incorrect answers will be penalised. Each part is independent and should be considered on its own. Instruction with "X" (don't care) value for the particular case should be **left out**.

   (a) The "**RegWrite**" (Writing to register) signal is "0". **[1mark]**

   (b) The "**ALUControl**" signal is 0010 (Add). **[1mark]**

   (c) The "**A op B**" result of ALU unit is not utilized. **[1mark]**

9. [**6 marks**] Given the following MIPS program:

```
main:
      #Code to initialize $s0, $s1, $s2 not shown
      #$s2 is initialized to zero
      lui $t0, 0x8000
      ori $t0, $t0, 0x0000
      addi $t1, $zero, 31
      addi $t2, $zero, 0

loop: and $t3, $t0, $s1
      beq $t3, $zero, next
      sll $t2, $s0, $t1     #$t1 specifies the shift amount
      add $s2, $s2, $t2

next: addi $t1, $t1, -1
      srl $t0, $t0, 1
      bne $t0, $zero, loop

end:
```

   (a) What is the value of $s2 at the end of code, if $s0 is 3 and $s1 is 1023? **[2 marks]**

   (b) Suppose that $s0 and $s1 are unsigned integers and all operations in the code do not cause overflow (i.e. the result is well defined and fit in a register). Express the relationship of $s0, $s1 and $s2 in the simplest mathematical expression. **[2 marks]**

   (c) Suppose there is a **single MIPS** instruction that implements the exact same operation as in (b) and takes **C** cycles to execute. We want to know when to use the program above to save some cycles. If every instruction in the program above takes 1 cycle to execute, how large should **C** be in order for the program above to be more cost-effective? Express **C** as an inequality, i.e. **C** > **someNumber**. **[2 marks]**

10. **[6 marks]** This question assumes a 5-stage MIPS pipeline processor as covered in the course. We will look into the problem associated with RAW data hazards in this question. The following information in the pipeline registers is used:

ID/EXE
O1: Value of Opr1 **O2**: Value of Opr2

EXE/MEM
RES: Result of ALU unit

MEM/WB
RES: Result of ALU unit

For ease of expression, you can write **`[PipelineRegister].[ValueName]`** to indicate a certain information. For example, **`[ID/EXE].O1`** is the value of operand 1 stored in the **`ID/EXE`** pipeline register.

(a) Let us tackle the problem of RAW hazard for instructions that are 1 instruction apart:

```
# X is followed by Y in program
X: op r1, r2, r3    # ([r2] op [r3]) is stored in (r1)
Y: op r4, r5, r6    # ([r5] op [r6]) is stored in (r4)
```

Express the idea of RAW hazard and data forwarding using high level C-like if-else statement. For example:

```
if (r2 == r5) then
    ID/EXE.O1 = [r5]
```

means if the register numbers "**`r2`**" and "**`r5`**" are the same, then we replace the Operand 1 value stored in the ID/EXE register with content of "**`r5`**" (i.e. forwarding). The **`r1`**, **`r2`**, …, **`rX`** are variables referring the real register number used. Also, note that this is just an example on the notation, it may not make sense semantically.

For simplicity, you can express the problem concerned **with the first source operand of Y only** (i.e. "r5" in the example above), as the problem/solution with second source operand is very similar. **[2 marks]**

(b) Now, the problem of RAW hazard for instructions that are 2 instructions apart:

```
X: op r1, r2, r3        # ([r2] op [r3]) is stored in (r1)
Y: <some instruction>
Z: op r7, r8, r9        # ([r8] op [r9]) is stored in (r7)
```

Express the idea of RAW hazard and data forwarding using high level if-else statement. Again, you can express only for first operand of Z (i.e. "r8"). **[2 marks]**

(c) There are times where the problems of (a) and (b) occur **at the same time**, for example in the code below:

```
X:  add  $2, $3, $5      #produces $2
Y:  sub  $2, $2, $7      #uses and produces $2
Z:  add  $9, $2, $13     #uses $2
```

Using instruction Z as the point of reference, there are 2 data hazards according to (a) and (b), i.e. X→Z, Y→Z.

[2 marks] Give the simplest expression, such that:

- The first source operand ("$2" in the example) of instruction **Z** will receive the correctly forwarded results. You can safely ignore other dependencies (e.g. the X→Y in the example above).
- All three cases of data hazards should be considered. i.e. (X→Z) only, (Y→Z) only, both (X→Z) and (Y→Z).

Please use the same notation as in (a) and (b):

```
X: op r1, r2, r3
Y: op r4, r5, r6
Z: op r7, r8, r9
```

11. **[3 marks]** This question is on processor performance. The answers can be in ratio form (X/Y) without simplification.

(a) Amadahl's law can be applied to the pipeline processor with a simple extension. If an instruction causes no stall in the pipeline, it can be approximated as having a speedup of N times (N is number of pipeline stages). If an instruction causes X cycle of stall, then it can be approximated to have a speedup of (N-X) times.

Let us consider the MIPS 5-stage pipeline processor. If 50% of instructions causes data hazards, and 20% of these are memory load instruction. What is the speedup of the pipeline processor if there are no forwarding paths? You can ignore the pipeline startup cost in this question. **[2 marks]**

(b) Given the same values in (b), what is the speedup of the pipeline processor if forwarding paths are implemented? **[1 mark]**

——— END OF PAPER ———

(2 blank pages are provided for your rough work)

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