NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING

TERM TEST #1
AY2013/2014 Semester 2

CS2100 — COMPUTER ORGANISATION

8 March 2014 Time Allowed: **1 hour 15 minutes**

INSTRUCTIONS

1. This question paper contains **ELEVEN (11)** questions (excluding the bonus question) and comprises **EIGHT (8)** printed pages.
2. The last two pages are for your rough work. They contain blank truth tables, K-maps and state table for your use.
3. An **Answer Sheet**, comprising **TWO (2)** printed page, is provided for you.
4. Write your **Name**, **Matriculation Number** and **Tutorial Group Number** on the Answer Sheet with a **PEN**.
5. You may write your answers in pencil (at least 2B).
6. Answer **ALL** questions within the space provided on the Answer Sheet.
7. Submit only the Answer Sheet at the end of the test. You may keep the question paper.
8. Maximum score is **30 marks**.
9. This is a **CLOSED BOOK** test. However, a single-sheet double-sided handwritten A4 reference sheet is allowed.
10. Calculators and computing devices such as laptops and PDAs are not allowed.

——— END OF INSTRUCTIONS ———

Bonus question:

0. The is the bonus question which is worth 1 mark. The mark of this question will only be added if the total mark scored is less than 30.

On the Answer Sheet you will find one of the above 4 figures. Write the name of the figure, making sure that your spelling is correct. Optionally, you may also fill in the speech bubble what you want to say to the setter and grader of this paper. ☺

Note the following acronyms used in this paper:

- **SOP**: Sum-of-Products
- **POS**: Product-of-Sums

Questions 1 – 5: Each multiple-choice-question has only <u>one</u> correct answer. Write your answers in the boxes on the **Answer Sheet**. Two marks are awarded for each correct answer and no penalty for wrong answer.

1. Which of the following statements is INCORRECT?

   A. If an integer is expressed the same way in sign-and-magnitude form, 1s complement form, and 2s complement form, then the integer must be positive.

   B. Given any self-complementing decimal code scheme, if we know the codes for the number 283, then we can deduce the codes for 671.

   C. An SOP expression may also be a POS expression.

   D. It is not possible to implement a 4-variable Boolean function using a single 8:1 multiplexer.

   E. The sum (or) of two distinct maxterms of a Boolean function is always 1 (true).

2. What is the simplified SOP expression for the following Boolean expression?

$$(B + A \cdot B \cdot C \cdot D' \cdot E) \cdot (C \cdot D' \cdot F + C \cdot D \cdot F + C' \cdot F) + B' \cdot G \cdot H + F \cdot G \cdot H$$

   A. $B' + F$

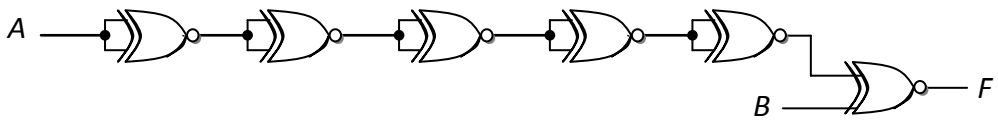
   B. $B \cdot F + B' \cdot G \cdot H$

   C. $B \cdot F + B' \cdot G \cdot H + F \cdot G \cdot H$

   D. $B \cdot F + G \cdot H + F \cdot G \cdot H$

   E. None of the above

3. Given the following circuit, what is the output ***F***?

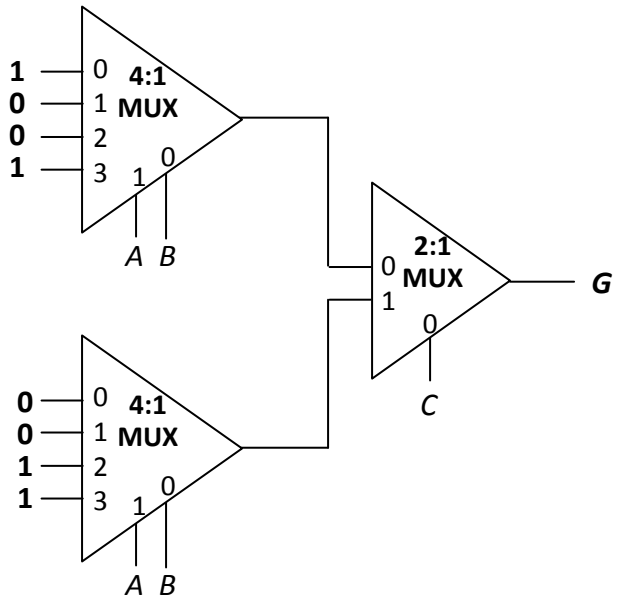


A. 0
B. 1
C. *A*
D. *B*
E. None of the above

4. The Boolean function ***F*** is given below:

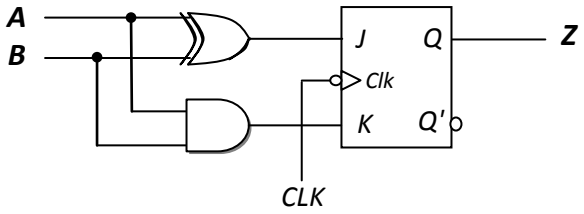
$F(A,B,C) = \Sigma m(0, 3, 6, 7)$

Compare the output ***G*(*A*,*B*,*C*)** of the circuit below with ***F***. Which of the following statements is correct?

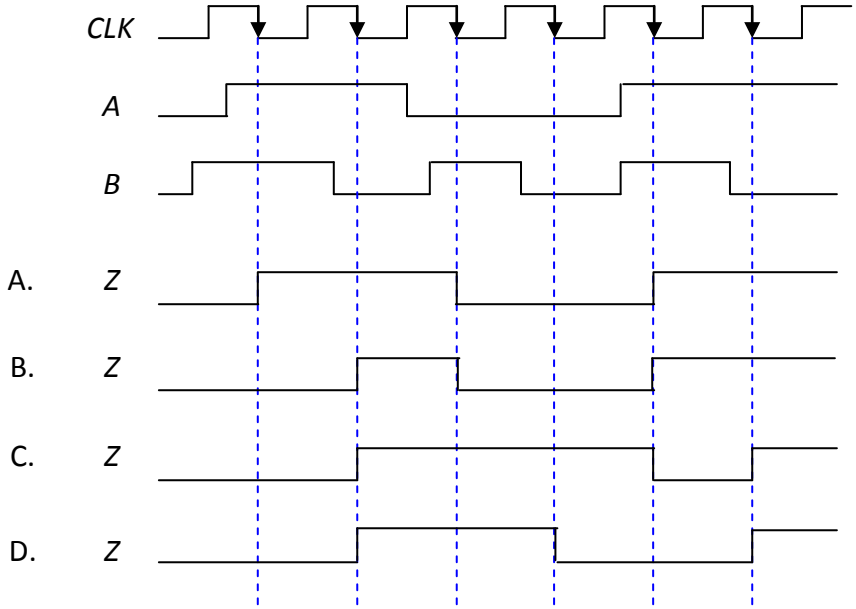


A. *F* and *G* are identical.
B. The values of *F* and *G* differ only at *ABC* = 001, 010, 100 or 101.
C. The values of *F* and *G* differ only at *ABC* = 000, 011, 110 or 111.
D. The values of *F* and *G* differ only at *ABC* = 010 or 100.
E. The values of *F* and *G* differ only at *ABC* = 011 or 101.

5. Given the following sequential circuit:



Which of the following timing diagrams for ***Z*** is correct?



E. None of the above.

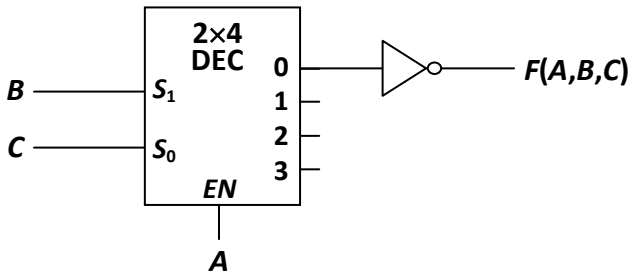
Questions 6 – 11: Write your answer in the space provided on the **Answer Sheet**. You do not need to show workings, unless otherwise stated.

6. Given the following hexadecimal representation in IEEE 754 single-precision floating-point number system:

   4 1 8 6 0 0 0 0

   Fill in the first 20 bits of the representation and write out the decimal value it represents. [3 marks]

7. Study the logic circuit below, which consists of a 2×4 decoder with 1-enable and active-high outputs, and an inverter.



   (a) Write out the simplified SOP expression for ***F***. [1 mark]

   (b) Implement ***F*(*A*,*B*,*C*)** using a single **2×4 decoder** with **0-enable** and **active-low outputs** without any logic gate. Complemented literals are not available**.** [2 marks]

8. Given the following Boolean function:

   $$F(A,B,C) = \Pi M(1, 4)$$

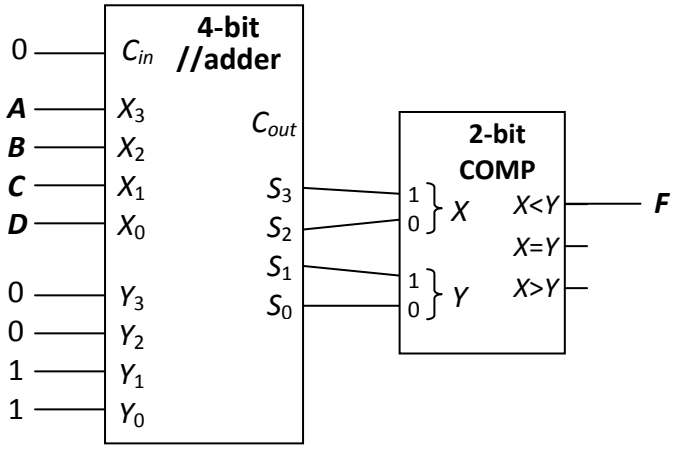
   Implement *F* using a single **4:1 multiplexer** without any additional logic gate. You may assume that constants 0 and 1 are available, but not complemented literals. [2 marks]

9. The following table shows a **4-to-2 priority encoder** with inputs *A*, *B*, *C*, *D* and outputs *P* and *Q*. 'X' represents don't-care value.

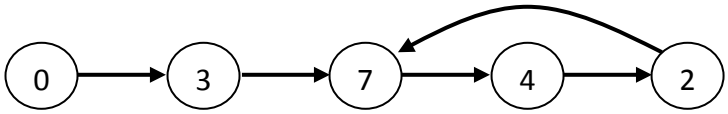
A	*B*	*C*	*D*	*P*	*Q*
0	0	0	0	X	X
X	X	X	1	1	1
X	1	X	0	0	1
X	0	1	0	1	0
1	0	0	0	0	0

   Write out the simplified SOP expressions for ***P(A,B,C,D)*** and ***Q(A,B,C,D)***. [2 marks]

10. The following circuit consists of a 4-bit parallel adder and a 2-bit magnitude comparator. The circuit takes a 4-bit unsigned binary number *ABCD* as input. Write the simplified SOP expression and simplified POS expression for ***F***. If there are more than one simplified SOP expression or POS expression, you need only write one. [4 marks]



11. The state diagram of a sequential circuit is shown below, with state values shown in decimal. The binary values *ABC* of the states are represented by variables *A*, *B*, and *C*.



Implement the above circuit using *T* flip-flop for *A*, and *JK* flip-flops for *B* and *C*, with the fewest number of additional logic gates. (No restriction on the type of logic gates.)

(a) Write the simplest expressions (need not be SOP expressions) for the flip-flop inputs *TA*, *JB*, *KB*, *JC* and *KC*. If there are alternatives, choose the one that uses the fewest number of gates. No restriction on the type of logic gates, but all gates, except for inverters, should have a fan-in of 2. [5 marks]

(b) How many additional logic gates besides the flip-flops does your implementation need to use? [1 mark]

——— END OF PAPER ———

(Blank truth tables, K-maps and state table are provided in the next two pages.)

This page is for your rough work.

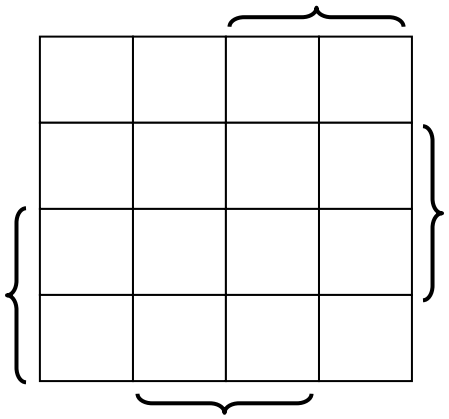
A	*B*	*C*	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

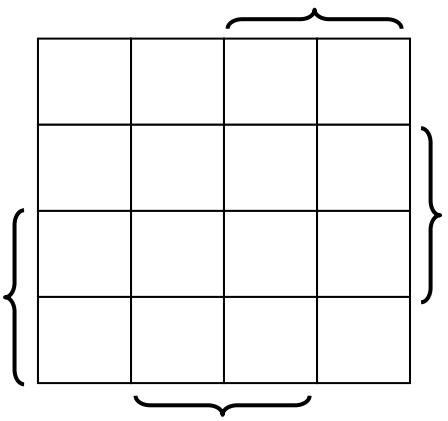
A	*B*	*C*	
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

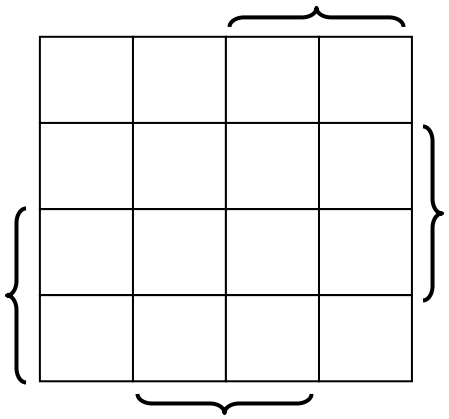
A	*B*	*C*	*D*	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

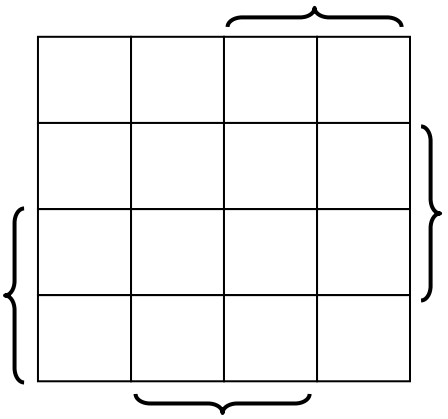
A	*B*	*C*	*D*	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

This page is for your rough work.









Present state			Next state							
A	***B***	***C***	A^+	B^+	C^+					