ARCHITECTURE AND ORGANIZATION

Vo Hieu Nghia

1. Altera NIOS II

It employs a 5 or 6-stage pipeline to achieve maximum DMIPS/MHz. The table below gives us the information about the number of stages of Nios II Processor cores

Table 5–1. Nios II Processor Cores (Part 1 of 2)

Feature		Core		
		Nios II/e	**Nios II/s**	**Nios II/f**
Objective		Minimal core size	Small core size	Fast execution speed
Performance	DMIPS/MHz *(1)*	0.15	0.74	1.16
	Max. DMIPS *(2)*	31	127	218
	Max. f_{MAX} *(2)*	200 MHz	165 MHz	185 MHz
Area		< 700 LEs; < 350 ALMs	< 1400 LEs; < 700 ALMs	< 1800 LEs; < 900 ALMs
Pipeline		1 Stage	5 Stages	6 Stages
External Address Space		2 Gbytes	2 GBytes	2 GBytes

For example ,the stages of Nios II/f core :

Table 5–4. Implementation Pipeline Stages for Nios II/f Core

Stage Letter	Stage Name
F	Fetch
D	Decode
E	Execute
M	Memory
A	Align
W	Writeback

It has multi-cycle instructions, Avalon-MM instruction master port read accesses, Avalon-MM data master port read/write accesses, and data dependencies on long latency instructions.

All instructions take one or more cycles to execute. Some instructions have other penalties associated with their execution. Late result instructions have two cycles placed between them and an instruction that uses their result. Instructions that flush the pipeline cause up to three instructions after them to be cancelled. This creates a three-cycle penalty and an execution time of four cycles. Instructions that require Avalon-MM transfers are stalled until any required Avalon-MM transfers (up to one write and one read) are completed.

5. ARM Cortex – A9

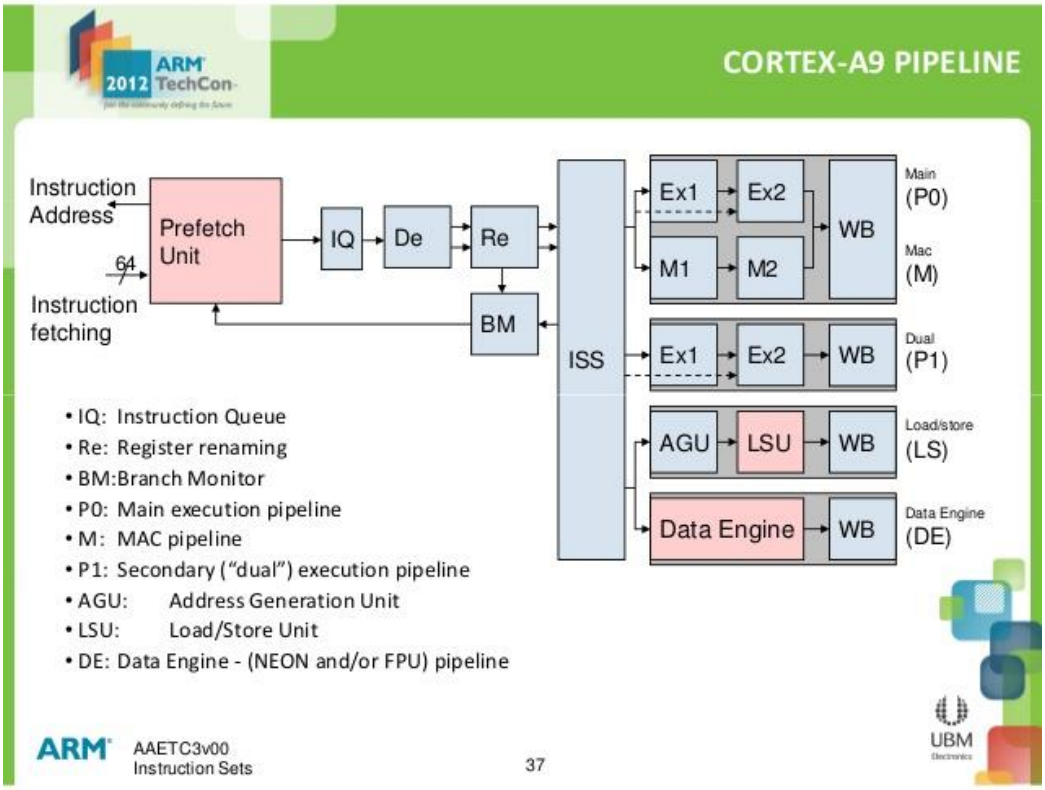

Figure 1 : Arm Cortex A9

Arm Cortex A9 pipeline is superscalar, which can fletch and dispatch two instructions per clock cycle but it performs only one pipeline per stage. It has full implementation of the ARM architecture v7-A instruction set, on an efficient 8-stage pipeline. Common instructions take 9 cycles, while complex instructions take up to 11 cycles. Supports dispatch of 4 instructions and completion of 7 instruction per clock cycle.

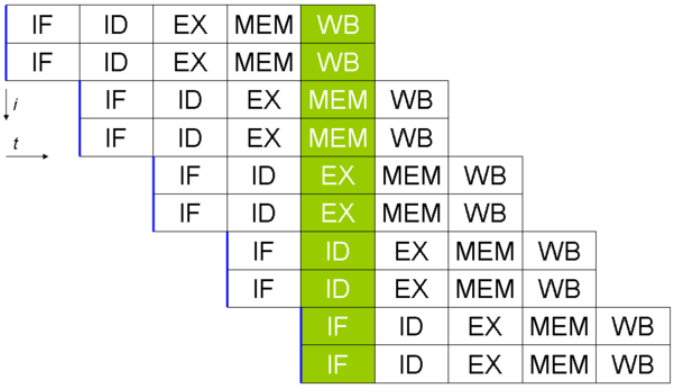

Figure 2: Superscalar processor

Reference

1. http://www.slideshare.net/AnhDungNGUYEN3/arm-aae-intrustion-set

2. http://rtcgroup.com/arm/2007/presentations/174%20-%20Details%20of%20a%20New%20Cortex%20Processor%20Revealed%20Cortex-A9.pdf

3. https://en.wikipedia.org/wiki/Superscalar_processor

4. http://www.eecg.toronto.edu/~moshovos/ECE243-2009/n2cpu_nii5v1.pdf