Von Neumann and Harvard architectures

This document will analyze the architecture of the microprocessor. The processors, which are chosen to be examined are Intel Itanium/Itanium 2 and Nios II Processor. Below is the block diagram of the processors :

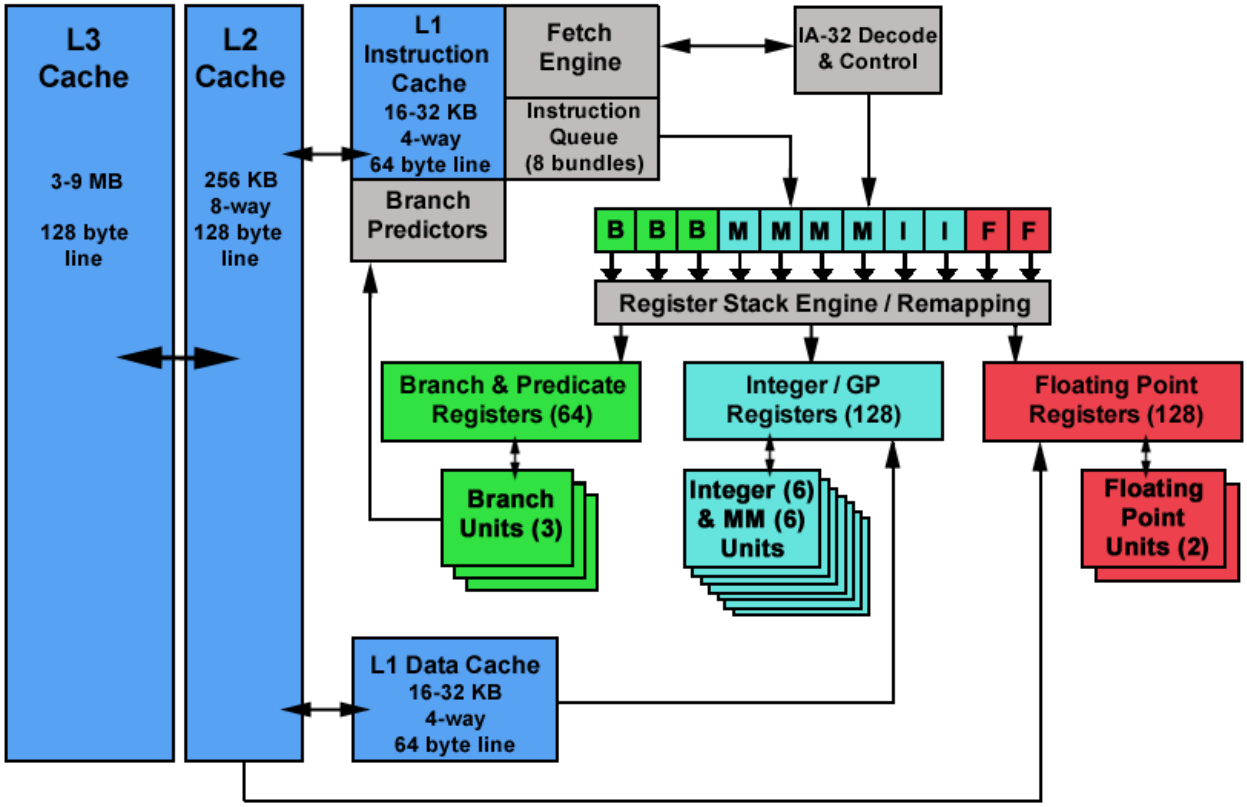

Figure 1: Intel Itanium / Itanium 2 Block diagram (Blaise Barney,2009)

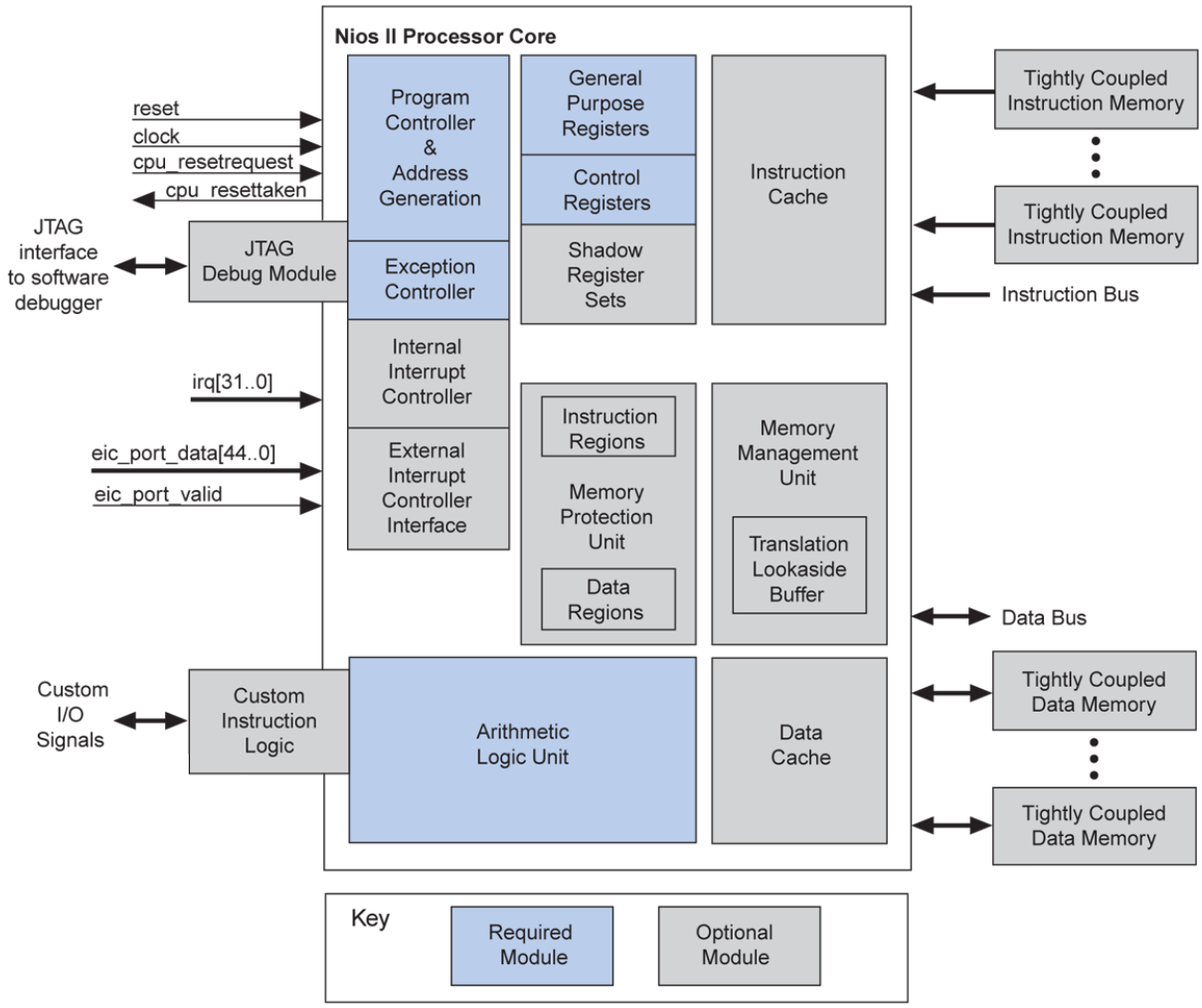

Figure 2: Nios II Processor core block diagram (Altera corporation, 2011)

Itanium is the 64 bits Intel microprocessors, which is usually used for servers. Nios II is a 32 bits processor can be found form Digital Signal Processing to system control. In the bock diagram (Figure 1 &2), it can be recognized that they both have separate caches for program and data. Therefore, the data and program can be accessed parallel, which is closer to the Harvard architecture style. However, instead of using separate memory like in Harvard architecture, it uses caches to get the instructions and a data parallel. In conclusion, they both use the modified Harvard architecture, which combines all the best parts of both architecture type.

Reference

1. Blaise Barney,2009, https://computing.llnl.gov/tutorials/linux_clusters/thunder.html
2. Altera corporation, 2011, https://www.altera.com/zh_CN/pdfs/literature/hb/nios2/n2cpu_nii51002.pdf