PIPE LINE ASSIGNMENT

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Ex1:

A processor has a data path that is made up of modules with latencies of 2, 3, 4, 7, 3, 2 and 4 ns !

1. Case 1: Join adjacent modules together to have minimum stages: 2, 7, 7, 5, 4
   Maximum clock frequency : 1/7*10^-9 = 143 MHz
   Number of pipeline stages : 5
   Execution time for a single instruction = 5 * 7 = 35 ns
2. Case 2 : 7ns split into 3 & 4 ns 2, 3, 4, 3, 4, 3, 2, 4
3. Maximum clock frequency 2 : 1/4*10^-9 = 250 MHz
   Execution time 2 : 8*4 = 32 ns
   Number of pipeline stages 2 : 8
4. Add 1 ns overhead to each stage in the pipeline
   Case1 : 3, 8, 8, 6, 5
   Execution time : 5*8 = 40 ns
   Number of pipeline stages : 5
   Maximum clock frequency 2 = 1/8*10^-9 = 125 MHz
   Case2: 3, 4, 5, 4, 5, 4, 3, 5
   Execution time : 5*8 = 40 ns
   Number of pipeline stages : 8
   Maximum clock frequency 2 = 1/5*10^-9 = 200 MHz
   ⇨ The overhead makes the maximum clock frequency reduced in both cases.

Ex2:

⇨ Processor a):

Number of cycle to complete the instructions:

Case 1: 5 + (15 – 1) = 19

Case 2: 5 + (30 – 1) = 34

Case 3: 5 + (100 – 1) = 104

CPI :

Case 1: CPI = 19 / 15 = 1,27

Case 2: CPI = 34 / 30 = 1,13

Case 3: CPI = 104 / 100 = 1,04

⇨ Processor b):

Number of cycle to complete the instructions:

Case 1: 9 + (15 – 1) = 23

Case 2: 9 + (30 – 1) = 38

Case 3: 9 + (100 – 1) = 108

CPI :

Case 1: CPI = 23 / 15 = 1,53

Case 2: CPI = 38 / 30 = 1,27

Case 3: CPI = 108 / 100 = 1,08

- ⇨ Processor c):

Number of cycle to complete the instructions:

Case 1: 21 + (15 – 1) = 35

Case 2: 21 + (30 – 1) = 50

Case 3: 21 + (100 – 1) = 120

CPI :

Case 1: CPI = 35 / 15 = 2,33

Case 2: CPI = 50 / 30 = 1,67

Case 3: CPI = 120 / 100 = 1,2

- ⇨ The higher number of stages and the lower number of the instruction, the higher CPI will be. In contrary, the lower number of stages and the higher number of the instruction, the lower CPI will be