Project 3 Report

The purpose of this project was to simulate an out of order execution processor and determine the optimal configuration given 4 different programs. The parameters to vary were the following:

- Number of ALU function units
- Number of MUL function units
- Number of LSU function units
- Reservation Stations per function unit
- Number of physical registers
- Fetch width

As expected, increasing most of these resources improved the main measure of performance, Instructions per Cycle (IPC). This can be seen as the average IPC is plotted vs each of the parameters for each trace below. Every possible configuration was run to generate the plots.

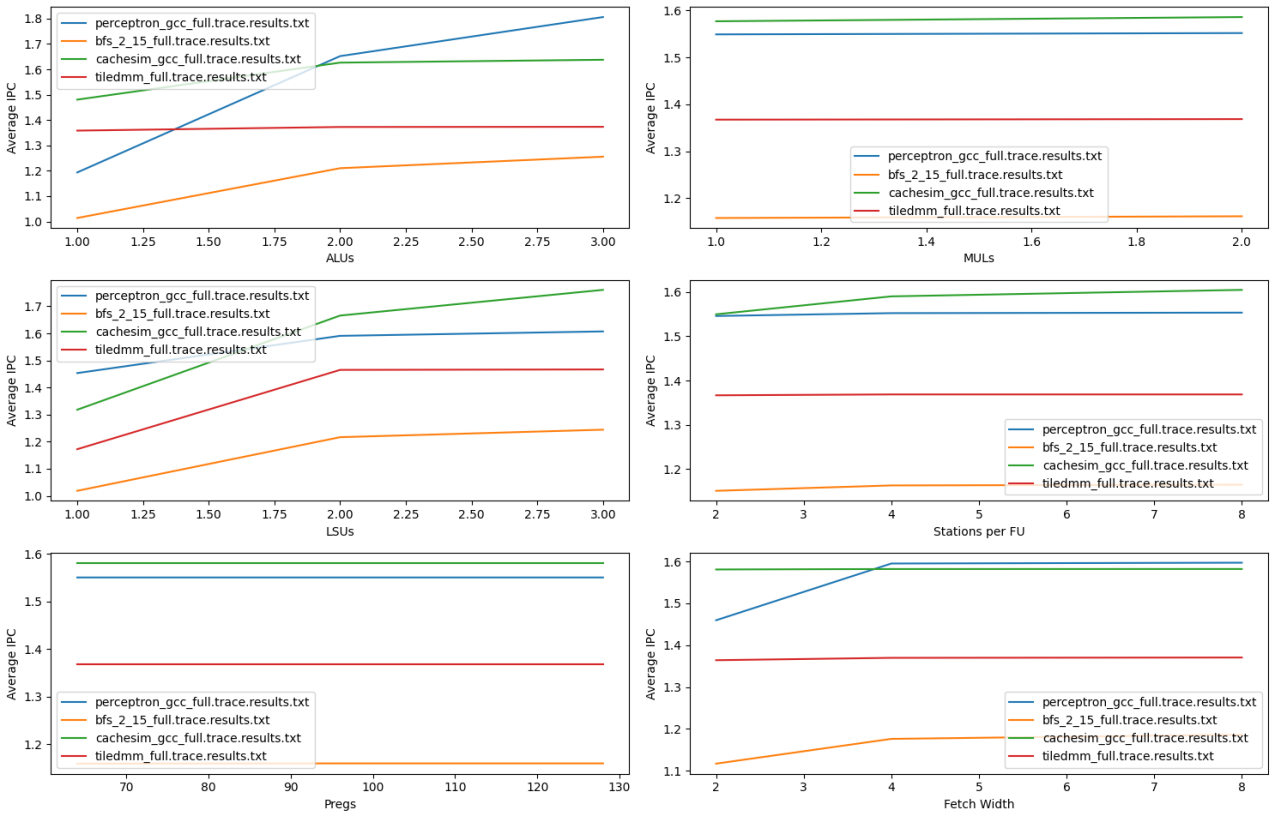

Figure 1. Each parameter plotted against average IPC for each trace.

Some of the parameters made less of an impact compared to the others. Increasing the number of physical registers and MUL units seems to not affect the performance by much at all. This may be because the stalls due to pregs does not happen very often, so incrementing this parameter only helps marginally. Another parameter that has a little effect on the performance is the MUL function unit. This is probably because many programs have a small amount of multiplies when compared to other instructions, so it is rarely the bottleneck of the program.

To chose the optimal configuration for each trace the knee in each of the curves was considered to pick a balance between performance and resource utilization. If there was still a good amount of performance to be gained after the knee, then that parameter was subjectively increased.

Optimal Configurations for Each Trace:

perceptron_gcc:

3 ALUs, 1 MULs, 2 LSUs, 2 Stations per FU, 64 Physical Registers, 4 Fetch Width

bfs_2_15:

3 ALUs, 1 MULs, 3 LSUs, 4 Stations per FU, 64 Physical Registers, 4 Fetch Width

cachesim_gcc:

2 ALUs, 1 MULs, 3 LSUs, 4 Stations per FU, 64 Physical Registers, 2 Fetch Width

tiledmm:

1 ALUs, 1 MULs, 2 LSUs, 2 Stations per FU, 64 Physical Registers, 2 Fetch Width