Final Project Report

-Analog Integrated Circuits, Spring 2024-

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1. DC Characteristics of MOSFETS

Understanding that the DC characteristics of the MOSFETS could be affected by channel length L and channel finger width, both parameters were fixed for all future simulations. Since longer channel length means less impact of channel length modulation, L was set as 400nm, and ch annel finger width was set as default 1um. This meant aspect ratios of only multiples of 2.5. The number of fingers for this section was set as 1, hence channel width W as 1um.

The testbench for simulating the DC character istics is shown below in Figure 1. VDD was set as 1.8V, VSS as 0V, and the gate voltage IN was initially swept from 0 to 1.8V to observe the Id vs. Vgs characteristics.

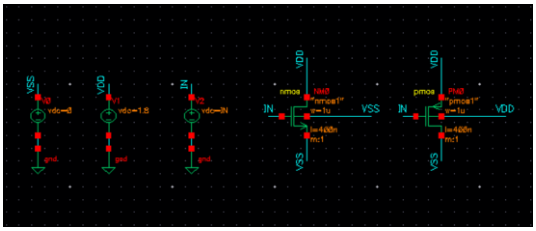


Figure 1. Testbench for DC characteristics.

The Id vs. Vgs, gm vs. Vgs characteristics for NMOS were derived as Figure 2.

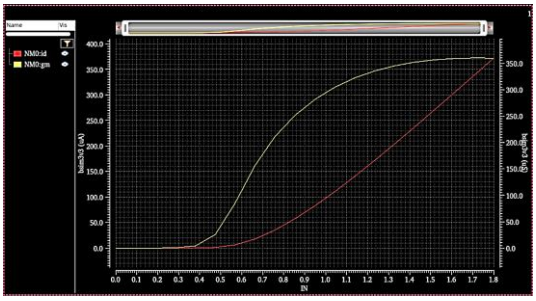


Figure 2. Id vs. Vgs, gm vs. Vgs characteristics for NMOS.

The dcOpInfo suggested that Vth was 494mV. gm is the slope of an Id vs. Vgs curve, and ideally (if the MOSFET follows the square law) should be linear for Vgs higher than Vth. However, it is evident from Figure 2 that this is not the case. Furthermore, gm has a relatively high value at the suggested Vth (when it should be ideally zero). Considering these non-idealities, parametric analysis of 20 points was done for Vgs range of 0.5 to 0.75V, where the gm curve was seemingly linear. The results were copied to Excel, and quad ratic regression analysis was done. The derived 2nd order polynomial was as follows, where x was Vgs, and y was Id. R^2 was 1.

$$y = 10^{-3}\,(0.357x^2 - 0.319x + 0.073)$$

$$= \frac{1}{2}K_n'\left(\frac{W}{L}\right)(x - V_{th,n})^2$$

Using the first two terms in the equation, Kn' was derived as 286uA/V^2, Vth,n as 0.45V.

The Id vs. Vgs, gm vs. Vgs characteristics for PMOS were derived as Figure 3.

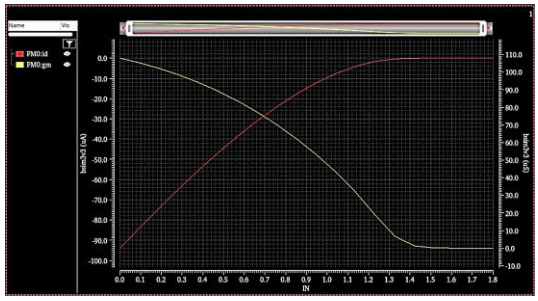


Figure 3. Id vs. Vgs, gm vs. Vgs characteristics for PMOS.

The dcOpInfo suggested that Vth was 459mV. Following the same logic as above, parametric analysis of 20 points was done for Vgs range of 1.1 to 1.34V where gm was linear, and the anal ysis result is shown below. R^2 was 1.

$$y = 10^{-3}\,(-0.068x^2 + 0.187x - 0.128)$$

$$= -\frac{1}{2}K_p'\left(\frac{W}{L}\right)(1.8 - x - V_{th,p})^2$$

Using the first two terms, K_p' was derived as 54uA/ V^2, Vth,p as 0.43V.

For derivation of lambda of NMOS, IN, hence Vgs was fixed as 0.6V, and parametric analysis of 50 points was done for Vds range of 0 to 1.8V by setting VDD as the variable. The Id vs. Vds chara cteristic was derived as Figure 4.

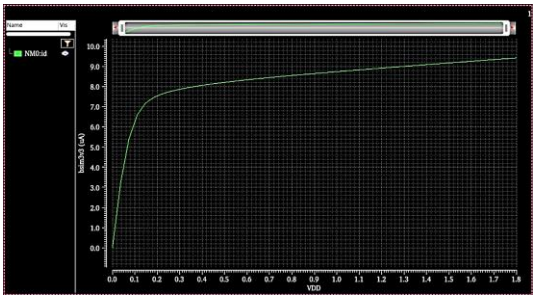


Figure 4. Id vs. Vds characteristic for NMOS.

The linear region in the curve, approximately from 1.2 to 1.8V was fitted by linear regression analysis of Excel. The result was as follows. y was Id, x was Vds. R^2 was 1.

$$y = 10^{-5}(0.084x + 0.791)$$

$$= \alpha(1 + \lambda x)$$

Ideally, λ_n must be the slope divided by the y intercross value, which was derived as 0.106/V.

For lambda of PMOS, IN was fixed as 1.2V, and parametric analysis of 50 points was done for Vds range of 0 to 1.8V by setting VSS as the variable. Figure 5 shows the Id vs. Vds characteristic.

The following result identicates the fitted linear region from 0 to 1V, with R^2 of 0.997. λ_p was derived as 0.085/V.

$$y = 10^{-5}(0.019x + 0.223)$$

It is worth noting that the calculated DC characteristics may not be accurate, which is quite evident from the discrepancy with the values that the dcOpInfo provides. However, the calculated values specifically fit the square model well. Hence, they make future hand calculations

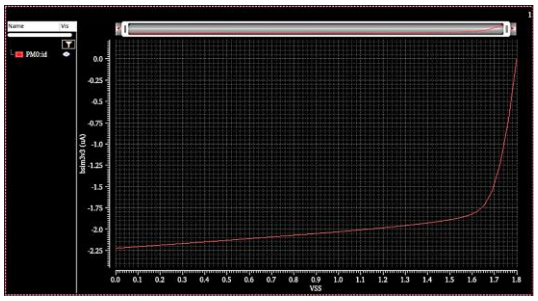


Figure 5. Id vs. Vds characteristic for PMOS.

regarding the MOSFET sizing more reliable.

2. Calculation of MOSFET & Cap Sizes

Using the DC characteristics derived in the previous section, hand calculation was performed to determine the aspect ratios of the transistors, size of the compensation capacitor, and the ideal current source (DC current bias). The process was nearly identical to the PPT. As mentioned before, the aspect ratios were calculated and rounded up to the closest integer multiple of 2.5.

For a phase margin of more than 60 degrees, the following inequality holds, assuming that the second stage RHP zero is higher than 10GB.

$$C_C > 0.22C_L = 2.2p$$

C_c was set as a relaxed 3pF. Next, to satisfy the slew rate (SR), the following inequality holds.

$$SR = \frac{I_5}{C_c} > 10^7 \rightarrow I_5 > 30u$$

I_5 was set as 40uA. Next, S_3 was calculated using the maximum ICMR and square law.

$$S_4 = S_3$$

$$= \frac{I_5}{K_{3,p}'(V_{DD} - V_{in,max} - V_{th3,p} + V_{th1,n})^2}$$

$$= \frac{40u}{(54u)\cdot(1.8 - 1.7 - 0.43 + 0.45)^2} \approx 52.5$$

gm_1 was derived as below, setting desired GB as twice the specification limit. The following step shows calculation of S_1.

$$g_{m1} = GB \cdot C_c = (2 \cdot 10^7 \cdot 2\pi) \cdot (3 \cdot 10^{-12})$$

$$\approx 377uS$$

$$S_1 = S_2 = \frac{g_{m2}^2}{K'_{2,n} I_5} = \frac{(377u)^2}{286u \cdot 40u} \approx 12.5$$

S_5 was calculated using the minimum ICMR and square law, as shown below.

$$V_{DS5} = V_{in,min} - V_{SS} - \sqrt{\frac{I_5}{K'_{1,n} S_1}} - V_{th1,n}$$

$$= 0.9 - \sqrt{\frac{40u}{(286u) \cdot (12.5)}} - 0.45 \approx 0.344$$

$$S_5 = \frac{2I_5}{K'_{5,n} V_{DS}^2} = \frac{2 \cdot 40u}{(286u) \cdot (0.344)^2} \approx 2.5$$

For the desired phase margin of 60 degrees, we could calculate gm_6 and S_6. The multiplication constant was set as 8 rather than 10 to satisfy the power dissipation specification later.

$$g_{m6} > 8g_{m1} = 3016uS, g_{m3} = \sqrt{2K'_{3,p} S_3 I_3}$$

$$= \sqrt{2(54u) \cdot (52.5) \cdot (20u)} \approx 336uS$$

$$S_6 = S_4 \frac{g_{m6}}{g_{m3}} = 52.5 \cdot \frac{3016u}{336u} \approx 472.5$$

I_6 could be calculated accordingly.

$$I_6 = \frac{g_{m6}}{2K'_{6,p} S_6} = \frac{(3016u)^2}{2 \cdot (54u) \cdot (472.5)} \approx 178uA$$

Theoretical power dissipation ignoring DC current bias was 392uW, and 474uW including the bias. Hence, both were under 0.5mW, meeting the specification. S_7 was derived next.

$$S_7 = \frac{I_6}{I_5} S_5 = \frac{178u}{40u} \cdot 2.5 \approx 12.5$$

Finally, the theoretical DC gain was calculated.

$$A_v = \frac{2g_{m2} g_{m6}}{I_5(\lambda_{2,n} + \lambda_{3,p}) I_6(\lambda_{6,p} + \lambda_{7,n})}$$

$$= \frac{2(377u)(3016u)}{(40u)(0.106 + 0.085)(178u)(0.085 + 0.106)}$$

$$\approx 8755 \gg 60dB$$

According to the hand calculations, all design specifications were satisfied using the calculated sizings. The testbench and simulation results under these specified sizings are analyzed in the next section.

3. Testbenches & Simulation Results

Figures 6, 7 show the opamp schematic and the DC/AC simulation testbench, respectively. The common mode input (CMI) voltage was set as a variable VCM for DC simulation, and differential input was given by 500m, -500mV, respectively, for AC simulation. Using DC simulation, the o utput voltage range and power dissipation for the ICMR were verified. Using AC simulation, the DC gain, gain bandwidth product, and phase margin for the ICMR were verified.

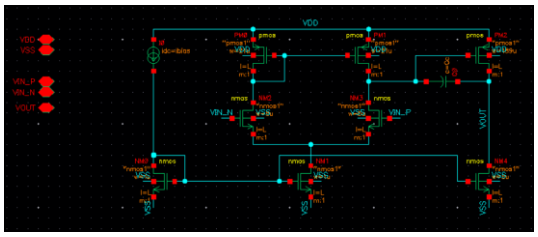


Figure 6. Opamp design schematic.

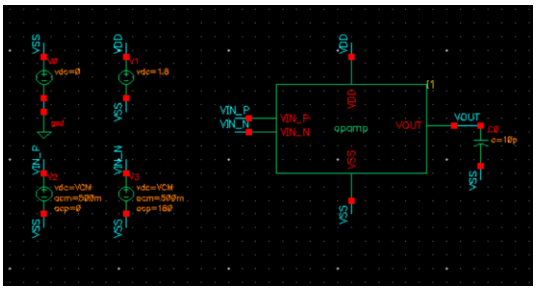


Figure 7. Testbench for DC/AC simulations.

Before verifying the specifications, it was intuitive to do comparative anaylsis between the simulated DC characteristics and the previous hand calculations. General values were compared when ICM voltage was 1.3V, although the values would change over the ICMR. The comparison is organized in the table below.

The values imply that the currents were simulated similarly as calculated, and that the gm

Characteristics	Hand calculated	Simulated
gm_1, gm_2	377uS	305uS
gm_3, gm_4	336uS	276uS
gm_6	3016uS	2679uS
I_5	40uA	39.217uA
I_6	178uA	193uA

values, although not identical, had similar tendencie. For example, gm_6 was about 8 times gm_2, and gm_3 slightly smaller than gm_2. A thorough comparitive analysis between the sim ulation results and the design specifications are shown below.

1) Verification of DC specifications

a) Output voltage range

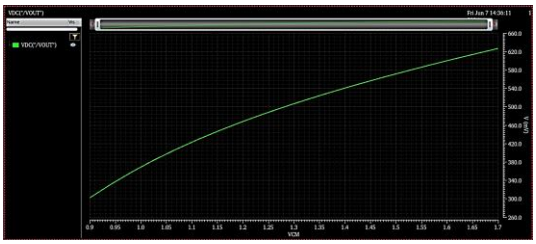


Figure 8. Simulated output voltage range for ICMR.

Parametric analysis of 10 points was done for the ICMR. Output voltage was measured as Figure 8. The minimum was 0.302V when ICM voltage was 0.9V, and the maximum was 0.627V of 1.7V ICM voltage, with all other points in bet ween. Hence, the DC output voltage range spec tification (0.2 to 1.6V) was satisfied.

b) Power dissipation

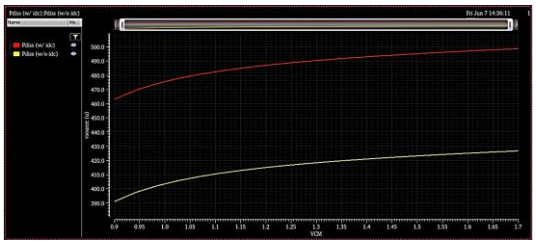


Figure 9. Simulated power dissipation for ICMR.

Power dissipation was measured and calculated as Figure 9. If the DC current bias is considered, power dissipation should be VDD times the total current flowing out of VDD. If the bias is neglected (as was permitted), then power diss ipation is VDD times the total current subtracted by the bias. (When bias was considered, the power dissipation ranged from 0.463m to 0.498m W. Hence, even considering bias power diss ipation, design specifications were satisfied.) Neglecting bias, total power dissipation had a maximum of 0.427mW at 1.7V. This value was close to the calculated power dissipation, 0.39 2mW, and comfortably meets specification.

2) Verification of AC specifications

The design specifications were verified for ICM voltages with intervals of 0.1V.

a) DC gain

Figure 10 shows all magnitude responses sweeping the ICMR. Since AC simulation was not possible for 0Hz, the 1KHz gain was treated as the DC gain. It is worth noting that since gain typically increases as frequency decreases, it is sufficient to verify the 1KHz gain. Figure 11 shows the 1KHz gain vs. ICMR plotted in MAT LAB. For all voltages, the gain was larger than 60dB, with minimum of 60.931dB at 0.9V. Thus, the DC gain specification was satisfied.

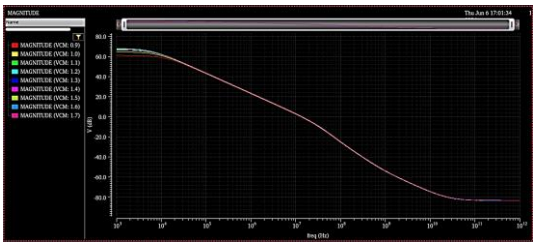


Figure 10. Simulated magnitude response for ICMR.

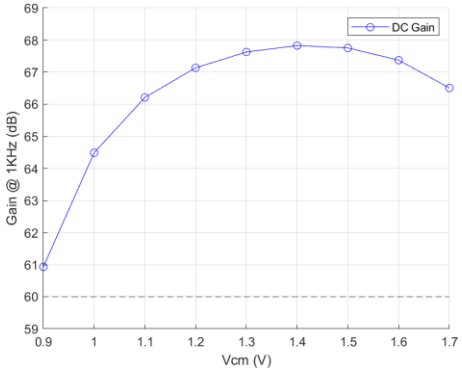


Figure 11. 1KHz gain vs. ICMR plot.

b) Phase margin (PM)

All phase responses sweeping the ICMR are shown in Figure 12. Like Figure 11, the response does not alter much with the ICMR, which is preferred for consistency.

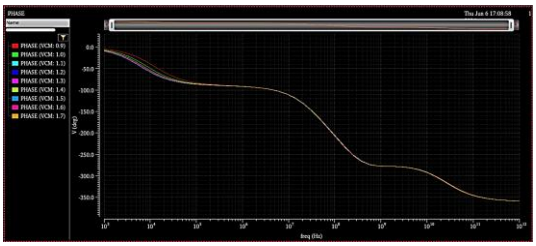


Figure 12. Simulated phase response for ICMR.

To calculate PM, unity gain bandwidth (UGB) was measured using a marker, and the corr esponding phase was compared with -180 deg rees. The derived PM values are shown in Figure 13 as “PM measured”. Spectre also provides a PM function, and the according values are shown as “PM function”.

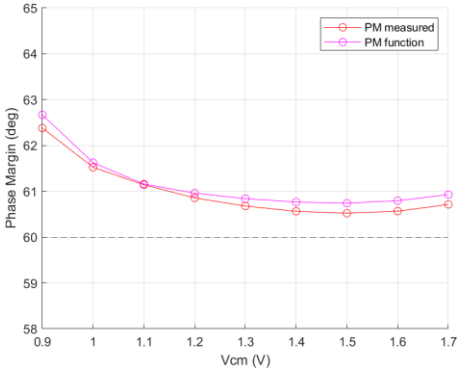


Figure 13. PM vs. ICMR plot.

The two graphs have nearly identical values, and for all the ICMR, PM is well above 60 degrees, with minimum being 60.522 degrees at 1.5V. This meets the specification as well as previous assum ptions during the hand calculations.

c) Gain bandwidth product (GB)

There were several techniques to measure and calculate GB. One simple but unprecise way was to assume that UGB equals GB. The measured UGBs from the magnitude response are shown in Figure 14 as “UGB measured”. UGBs obtained by using the UGB function in Spectre are shown as “UGB function”. The more accurate results calculated by multiplying the measured 1KHz gain and measured 3dB bandwidth of the mag nitude reponse are shown as “GBP measured”. It is worth noting that since the reference DC gain is not actually the DC but the 1KHz gain, the resulting GBs are sufficient to check the spec ifications but are not precise. Spectre provides a GB function, whose results are shown as “GBP function”.

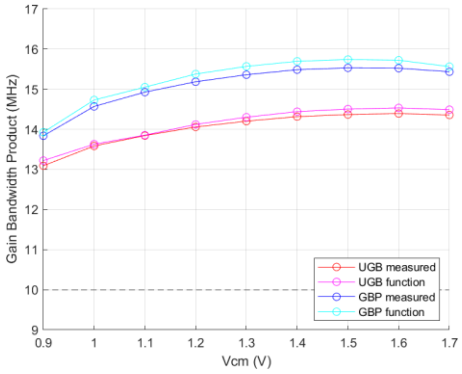


Figure 14. GB vs. ICMR plot.

For all techniques, GB was higher than 10MHz for all the ICMR. Maximum GB was obtained for 1.5V, with a measured GB of 15.498MHz. Rec alling that GB was assumed to be around twice as large as the design specification, this is a tolerable result. Hence, the design specification for GB was met with ease.

3) Verification of Transient specifications

The slew rate (SR) refers to the maximum rate of change of a signal, which shows a nonlinear tendency for large input signal variations. To verify the SR specification, transient analysis was performed, under the testbench shown in Figure 15. The negative input and output nodes were tied together to create feedback, and positive input step size was altered to observe change.

To observe positive SR, input voltage was intially set as 0.9V and was raised to 1.0 to 1.7V with intervals of 0.1V, with a rise time of 10ps. For negative SR, input voltage was set as 1.7V and was lowered to 1.6 to 0.9V, with an identical

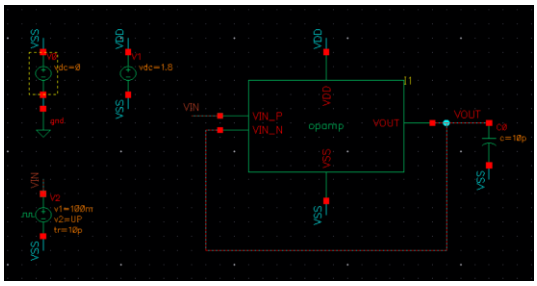


Figure 15. Testbench for Transient simulations.

fall time of 10ps. The rising and falling voltage values were set as such considering the ICMR. The rising and falling transient output voltage are shown in Figure 16, respectively.

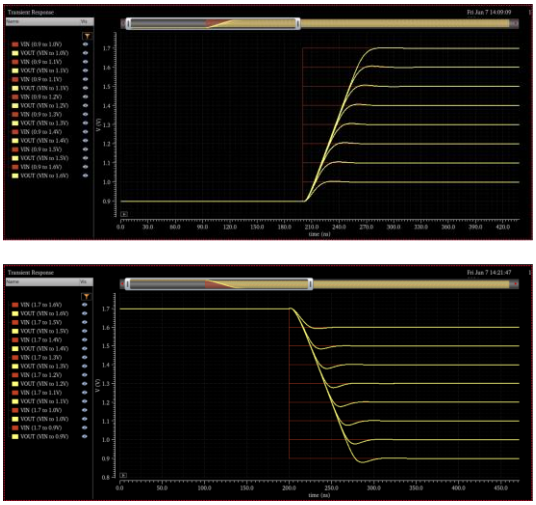


Figure 16. Simulated SR for ICMR. (Rising, Falling)

Voltage change rate saturates, as predicted, according to Figure 16. The measured positive SR using distance key was approximately 12.766 MV/s, or 12.766V/us. The measured negative SR was approximately 12.110MV/s, or 12.110V/us. These values are well over 10V/us, and hence meets the design spectification. In conclusion, **the designed opamp satisfies all design spec ifications. This design was submitted to etl.**

4. Design Revision for Improvements

Once again, the designed opamp already meets all necessary design specifications. However, it is important to note that the DC gain and PM in AC simulations did not have a comfortable breathing room from the limit. On the other hand, output voltage range, GB, power dissipation, and SR easily met the specifications. Therefore, these could be leveraged to increase DC gain and PM.

First, to increase PM, C_c could be increased. This, however, decreases SR, if I_5 is maintained. GB also decreases due to the increase of C_c if gm_1 were to be maintained. However, as mentioned, SR and GB were well over the specification limit, hence allowing manipulation of C_c.

As for the DC gain, increasing I_6 or decreasing I_5, while maintaining gm_2 would increase gain. Understanding that I_5 must be fixed to keep other values the same, we turn our attention to incr easing I_6. I_6 can be increased by increasing the aspect ratio of S_6. However, it should be noted that according to previous hand calculations, the gain is also inversely proportional to I_6. Hence, thorough analysis of simulations results would only be able to tell if increasing S_6 actually increased the DC gain. One important fact is that increasing current increases total power diss ipation of the opamp. Therefore, S_6 should be increased with caution in order not to unsatisfy previously satisfied specifications.

For the simulations in this section, C_c was set as 3.2pF (0.2pF increase from previous design), and S_6 was set as 500 (27.5 increase from previous design). The theory was that minimum DC gain and minimum PM will increase, but increase in total power dissipation, as well as a decrease in SR and GB would occur.

1) Verification of DC specifications

a) Output voltage range

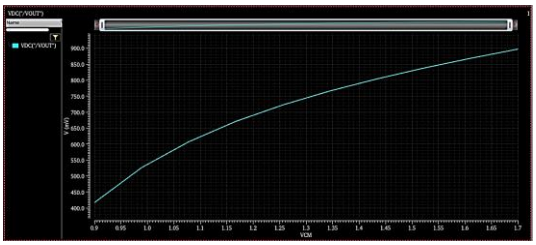


Figure 17. Newly simulated output voltage range.

Output voltage range was measured as Figure 17. The minimum was 0.417V, and the maximum was 0.897V. Therefore, the DC output voltage range is much more relaxed than the previous design for the ICMR.

b) Power dissipation

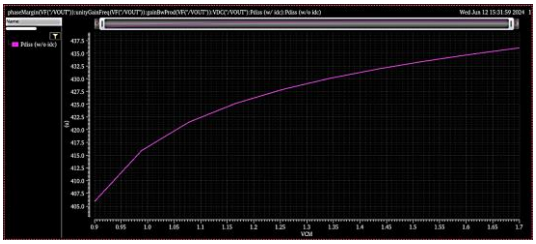


Figure 18. Newly simulated power dissipation.

Power dissipation was measured and calculated as Figure 18. Power dissipation neglecting bias was only plotted, with the minimum being 0.406 mW, and the maximum being 0.436mW. The power dissipation was higher than the previous minimum of 0.392mW. However, the range still satisfies the limit of less than 0.5mW.

2) Verification of AC specifications

a) DC gain

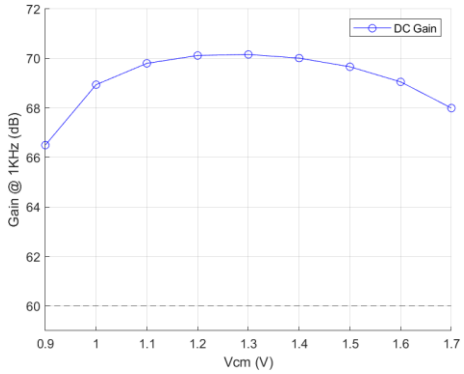


Figure 19. 1KHz gain vs. ICMR plot for new design.

Figure 19 shows the 1KHz gain vs. ICMR plotted in MATLAB. The minimum DC gain was 66.5dB at 0.9V. Comparing this to the previous minimum 60.931dB at 0.9V, it is clear that the minimum DC gain has increased by >5dB.

b) Phase margin (PM)

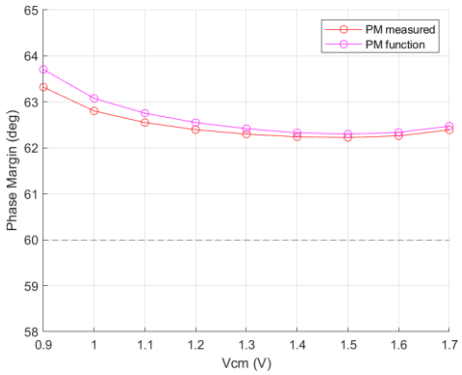


Figure 20. PM vs. ICMR plot for new design.

Figure 20 shows "PM measured", and "PM function" PM of the new design. The minimum measured PM was 62.301 degrees at 1.5V. Comparing this to the previous 60.522 degrees, an increase of >1.5 degrees was achieved.

c) Gain bandwidth product (GB)

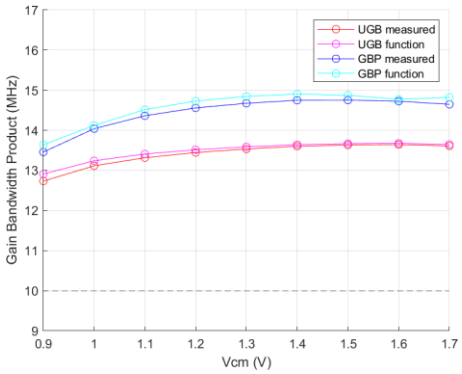
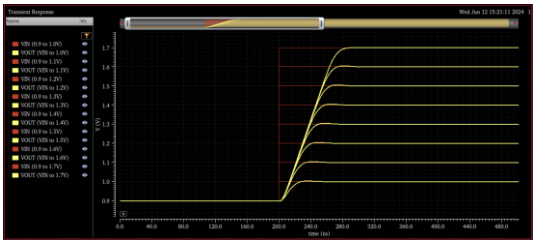


Figure 21. GB vs. ICMR plot for new design.

Figure 21 shows "UGB measured", "UGB fun ction", "GB measured", "GB function" GB for the new design for the ICMR. All plots are higher than the threshold 10MHz, but the maximum measured GB was 14.822MHz, rougly 0.8MHz lower than the previous maximum GB.

3) Verification of Transient specifications



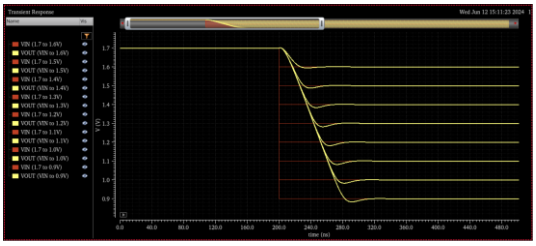


Figure 22. Newly simulated SR for ICMR. (Rising, Falling)

The SR was measured under the same conditions as in the previous design. The positive SR was measured as 11.841V/us, and the ne gative SR was measured as 11.335V/us. These va lues, compared to the previous 12.766V/us and 12.110V/us, indicate a slower transient change.

To summarize, the new opamp design was intended to increase overall and minimum DC gain and PM. While the two goals were met, an increase in total power dissipation, as well as a decrease in GB and SR were observed. Hence, it was understood that many factors are intertwined, and tradeoffs exist for every benefit. Also, note that increasing S_6, as well as increasing C_c would lead to a larger area consumption.

5. Conclusion

An opamp satisfying the given specifications was designed in this project. Before hand calculations, the DC characteristics of the MOSFET were measured and calculated. With the information, hand calculation was done to determine the transistor and capacitor sizing, as well as the DC bias current value. Comparative analysis of the DC, AC, and Transient simulation results showed that all design specifications were met. To relax tight conditions, a few parameters (namely S_6 and C_c) were tweaked and simulated once again. This led to improved DC gain and PM, as well as many tradeoffs.

We again note that although the new design has better overall performance, the power dissipation is larger, and SR is smaller. Generally speaking, power dissipation and speed are two very crucial constaints in real life applications. Hence, **we ultimately chose the previous design as our final design**, emphasizing that the previous design also satisfied all design specifications. The final transistor and capacitor sizing, as well as DC bias current are summarized below (all device numbers are according to the project file, which is different from the actual schematic numbers).

Device	(L,W)	Cap (C)	Current (I)
M1, M2	400nm, 5um		
M3, M4	400nm, 21um		
M5	400nm, 1um		
M6	400nm, 189um		
M7	400nm, 5um		
Cc		3pF	
Idc (Bias)			40uA