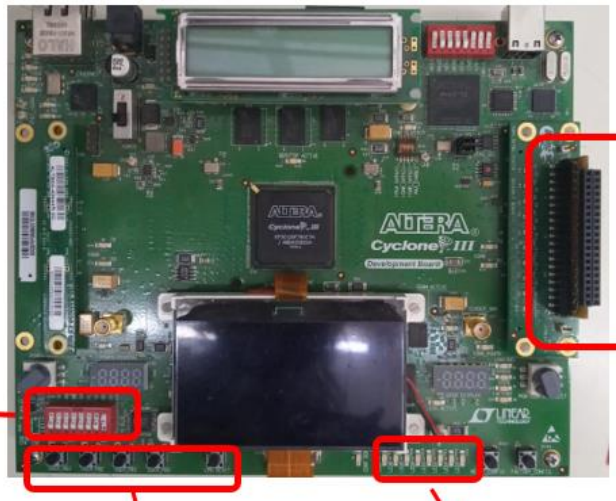
Pines de CYCLONE 3 ALTERA, información de: Cyclone III 3C120 Development Board Reference Manual (archivo rm_cycloneiii_dev_kit_host_board.pdf)

Clock 50MHz	AH15
Clock 125MHz	A14



X	X
G24	H23
G25	H24

sw7	sw6	sw5	sw4	sw3	sw2	sw1	sw0
AF25	AB15	G20	AD14	AC19	AG23	AO18	AC14

LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0
AF19	AG19	AC17	AE15	AD19	AF18	AE20	AD15

S1	S2	S3	S4	S5
AA12	AH3	AC12	AD7	T21

Table 2–27. LED Reference Number, Schematic Signal Name, and Cyclone III Device Pin Number

LED Board Reference	Description	I/O Standard	Schematic Signal Name	Cyclone III Device Pin Number
D26	User-defined LED	1.8 V	USER_LED7	AF19
D27	User-defined LED	1.8 V	USER_LED6	AG19
D28	User-defined LED	1.8 V	USER_LED5	AC17
D29	User-defined LED	1.8 V	USER_LED4	AE15
D30	User-defined LED	1.8 V	USER_LED3	AD19
D31	User-defined LED	1.8 V	USER_LED2	AF18
D32	User-defined LED	1.8 V	USER_LED1	AE20
D33	User-defined LED	1.8 V	USER_LED0	AD15

Table 2–28 lists the general user-defined LED component reference and manufacturing information.

Table 2–48. HSMC Port B Interface Signal Name, Description, and Type (Part 1 of 4)

Board Reference	Description	I/O Standard	Schematic Signal Name	Cyclone III Device Pin Number
J9 pin 33	Management serial data	2.5 V	HSMB_SDA	H26
J9 pin 34	Management serial clock	2.5 V	HSMB_SCL	H25
J9 pin 35	JTAG clock signal	2.5 V	FPGA_JTAG_TCK	P5
J9 pin 36	JTAG mode select signal	2.5 V	FPGA_JTAG_TMS	P8
J9 pin 39	Dedicated CMOS clock out	2.5 V	HSMB_CLK_OUT0	J22
J9 pin 40	Dedicated CMOS clock in	2.5 V	HSMB_CLK_IN0	A15
J9 pin 41	Dedicated CMOS I/O bit 0	2.5 V	HSMB_D0	G24
J9 pin 42	Dedicated CMOS I/O bit 1	2.5 V	HSMB_D1	H23
J9 pin 43	Dedicated CMOS I/O bit 2	2.5 V	HSMB_D2	G25
J9 pin 44	Dedicated CMOS I/O bit 3	2.5 V	HSMB_D3	H24
J9 pin 47	LVDS TX 0p or CMOS I/O data bit 4	LVDS or 2.5 V	HSMB_TX_D_P0	J25
J9 pin 48	LVDS RX 0p or CMOS I/O data bit 5	LVDS or 2.5 V	HSMB_RX_D_P0	F27