Metode si Tehnici de Programare in High Performance Computing

AAC/IALA Master Module

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Acknowledgements

- The material in this course has been compiled by me from various (cited) authoritative sources:
  - Applied Parallel Programming – UIUC, Spring 2020
  - High-Performance Scientific Computing – University of Washington, Spring 2019
  - Parallel Bootcamp – UC Berkeley, 2010-2014
  - Introduction to High-Performance Scientific Computing – Victor Eijkhout, 2015
  - Computational Science and Engineering – MIT, 2020
  - Trends in High Performance Computing – Horst Simon LBNL@UC Berkeley, 2009-2012

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Master@CS Feedback

- Speaking & presenting skills in English
- Team work experience is vital
- Working on big SW projects is important
- Improvements required:
  - **Hard** rules & deadlines
  - Periodic evaluation of **individual** effort
  - Learn during the whole year (3 week session)
  - Individual oral exam

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Grading@HPSC

- Project work – 5/6 points
  - Similar to APP & PP:
    - 3/coding, 1/documentation, 1/presentation, *1/bonus*
  - Topics from subjects related to the HPSC
  - Teams of 2-3 people – independent grading
  - Subject can also be done in the "research" hours – at the end a paper/presentation should emerge
- Oral exam – 5 points (1 activity)
  - 5-10 minutes / person
  - 2-3 subjects from the lecture
  - Can be **replaced** by holding a talk during the semester on a topic agreed with me in advance (iff > 75% attendance in class)
  - Activity during lectures – 1 point
    - Presence in class for the lectures is compulsory but does not insure the point – you have to (try to) participate actively

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Deadlines

- Choosing the Project:
  - Soft-deadline 23.03
  - Hard-deadline 30.03
- Project Status
  - Agreed at the lab by each team
- Project Submission
  - The **ONLY** Deadline: 25.05
  - Project Presentations on 25.05

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Project Work Roadmap

- One page project description (pdf + gitlab) due 23/**30**.03
  - **Introduction:** A one paragraph description of the significance of the application.
  - **Description:** A one to two paragraph brief description of what the application really does
  - **Objective:** A sentence on what I would like to accomplish with the team on the application – we have to agree on this at the lab.
  - **Background :** Outline the technical skills (type of Math, Physics, Chemistry, etc) that one needs to understand and work on the application.
  - **Resources:** A list of web and traditional resources that students can draw for technical background, general information and building blocks. Give URL or github/-lab links. Only use our gitlab.cs.pub.ro.
  - **Contact Information:** Name, e-mail, group and master program the team members are part of.
- The labs until then are dedicated to presentation of project ideas by you and me and used to recruit teammates

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What Will You Get from this Lecture

- A working knowledge of the numerical methods used in standard software packages from HPSC
- Improve the ability to participate in program development of HPSC projects
- Ability to use prototyping in modeling scientific phenomena
- Among the topics being covered:
  - Differential equations, numerical methods, analysis of scientific data, solving equations and optimization problems, scientific visualization

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Lecture Strategy

- Concentrate on the basics, with simple motivating examples
- Get enough hands-on experience to be comfortable experimenting further and learning much more on your own
- Learn what's out there to help select what's best for your needs
- Teach as many things as possible "by example" as we go along

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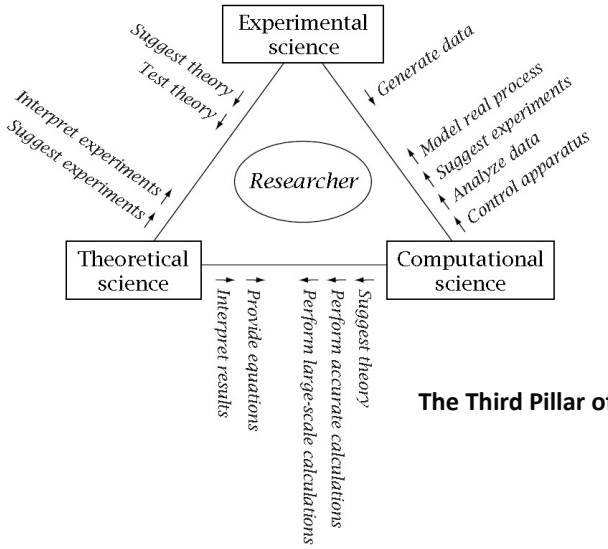
Scientific Research



The Third Pillar of Science

Table of Contents (subject to update)

- Motivation & Trends in HPC
- Mathematical Modeling
- Numerical Methods used in HPSC
  - Systems of Differential Equations: ODEs & PDEs $m\frac{d^2x(t)}{dt^2} = F(x(t)),$
  - Automatic Differentiation
  - Solving Optimization Problems $\min_{x\in\mathbb{R}} f(x) = e^{-x} + x^2$
  - Solving Nonlinear Equations $f(x) = -e^{-x} + 2x = 0$
  - Basic Linear Algebra, Eigenvalues and Eigenvectors
  - Chaotic systems
- HPSC Program Development/Enhancement: from Prototype to Production
- Visualization, Profiling, Performance Analysis & Optimization, Testing, Correctness

Trends in High Performance Computing 2010 – 2020+

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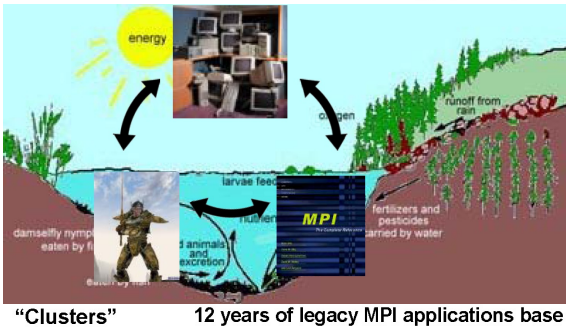
- Computing is changing more rapidly than ever before, and scientists have the unprecedented opportunity to change computing directions

Commercial Off The Shelf technology (COTS)

Supercomputing Ecosystem 200x



"Clusters" 12 years of legacy MPI applications base

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Traditional Sources of Performance Improvement are Flat-Lining

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- **New Constraints**
  - 15 years of *exponential* clock rate growth has ended
- **Moore's Law reinterpreted:**
  - How do we use all of those transistors to keep performance increasing at historical rates?
  - Industry Response: #cores per chip doubles every 18 months *instead* of clock frequency!

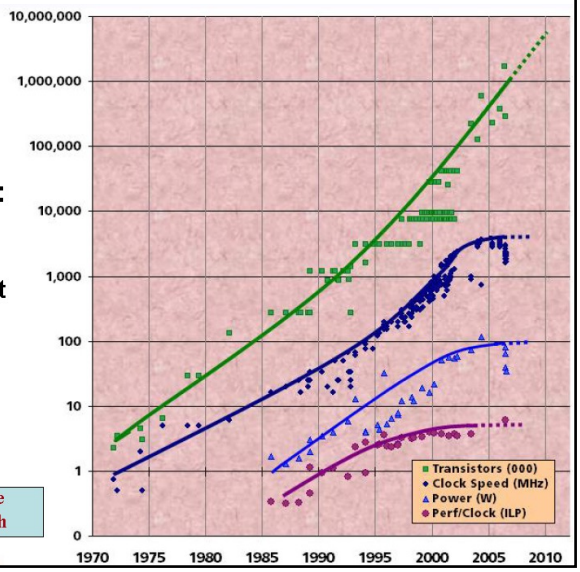

Figure courtesy of Kunle Olukotun, Lance Hammond, Herb Sutter, and Burton Smith

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Supercomputing Ecosystem 20xx

Commercial Off The Shelf technology (COTS)

PCs and desktop systems are no longer the economic driver.

Architecture and programming model are about to change

"Clusters"

years of legacy MPI applications base

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Breaking the 1PFlop Barrier

- 1,026 Tflop/s on LINPACK reported on June 9, 2008
- 6,948 dual core Opteron + 12,960 cell BE
- 80 TByte of memory
- IBM built, installed at LANL

Roadrunner

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Cray XT5@ORNL

Jaguar	Total	XT5	XT4
Peak Performance	1,645	1,382	263
AMD Opteron Cores	**181,504**	**150,176**	**31,328**
System Memory (TB)	**362**	**300**	**62**
Disk Bandwidth (GB/s)	**284**	**240**	**44**
Disk Space (TB)	**10,750**	**10,000**	**750**
Interconnect Bandwidth (TB/s)	**532**	**374**	**157**

The systems will be combined after acceptance of the new XT5 upgrade. Each system will be linked to the file system through 4x-DDR Infiniband

U.S. DEPARTMENT OF ENERGY
Office of Science

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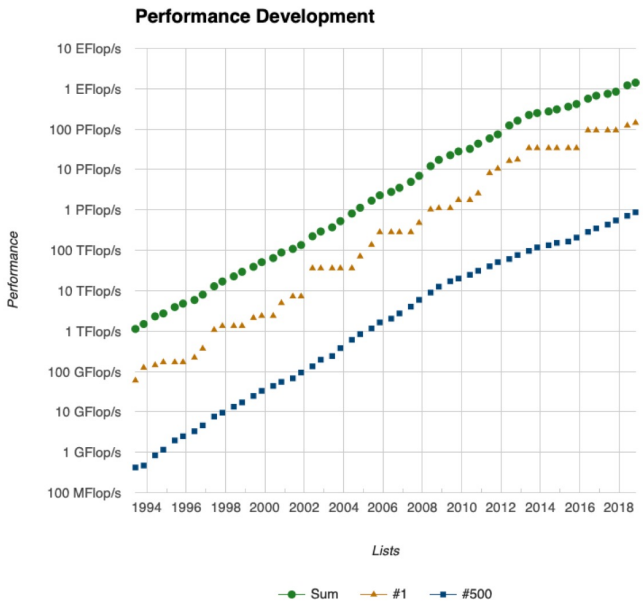

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Moore's Law "Reloaded"

- Number of cores per chip will double every two years
- Clock speed will not increase (possibly decrease)
- Need to deal with systems with millions of concurrent threads
- Need to deal with inter-chip parallelism as well as intra-chip parallelism

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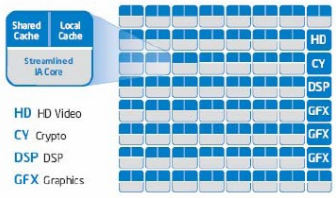
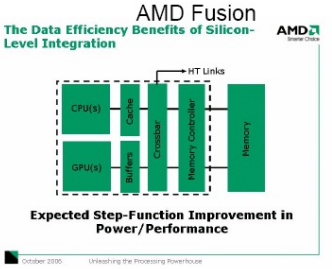
Industry presentations show changing trends in processors

Intel's Microprocessor Research Lab



AMD Fusion



Intel's Visual Computing Group - Larabee

nVidia G80 - 2006

Taken from publicly available information

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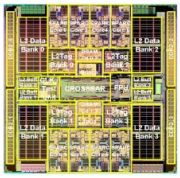
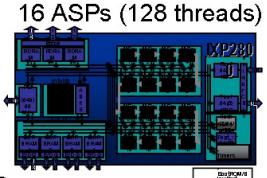
Multicore comes in a wide variety

- Multiple parallel general-purpose processors (GPPs)
- Multiple application-specific processors (ASPs)

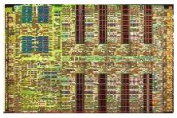


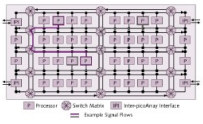
Sun Niagara
8 GPP cores (32 threads)

Intel Network Processor
1 GPP Core
16 ASPs (128 threads)

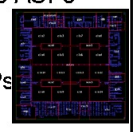


IBM Cell
1 GPP (2 threads)
8 ASPs





Picochip DSP
1 GPP core
248 ASPs



Cisco CRS-1
188 Tensilica GPPs

Intel 4004 (1971):
4-bit processor,
2312 transistors,
~100 KIPS,
10 micron PMOS,
11 mm² chip

1000s of processor cores per die

"The Processor is the new Transistor" [Rowen]

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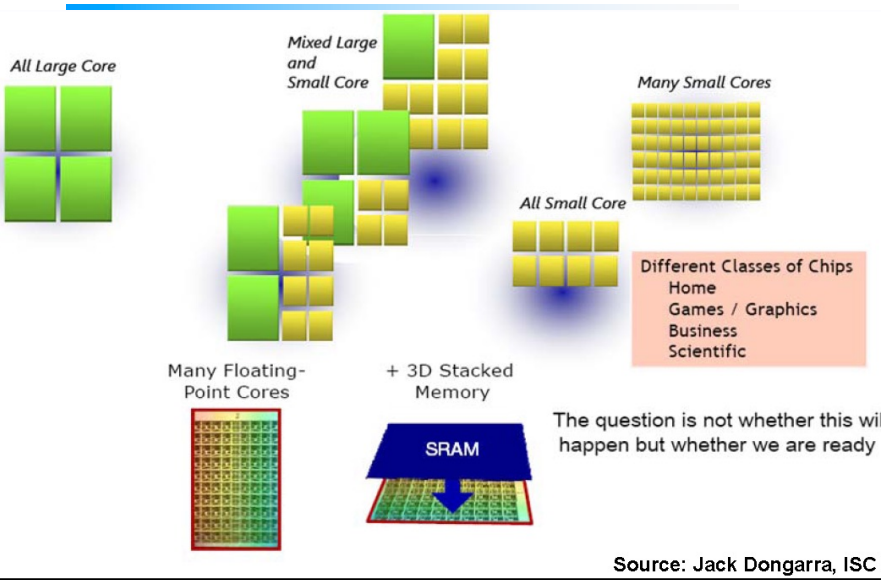
What's next?



Source: Jack Dongarra, ISC 2008

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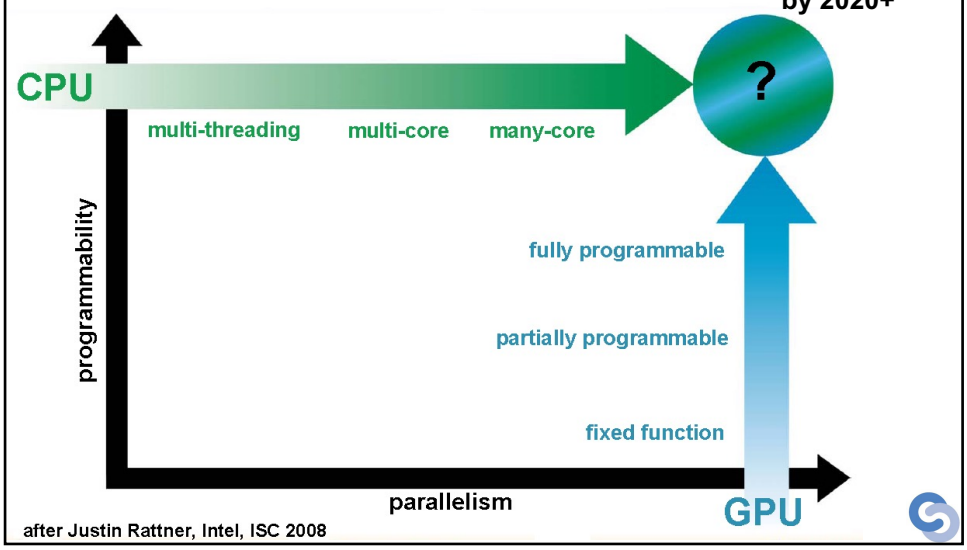
A Likely Trajectory: Collision or Convergence?



Trends for the next five years

- After a period of rapid architectural change we will likely settle on a future standard processor architecture
- A good bet:
  - Intel will continue to be a market leader
  - AMD will be the challenger in the CPU space
  - NVidia will lead in the accelerator space
- The impact of this disruptive change on software and systems architecture is not clear yet