

Observations:

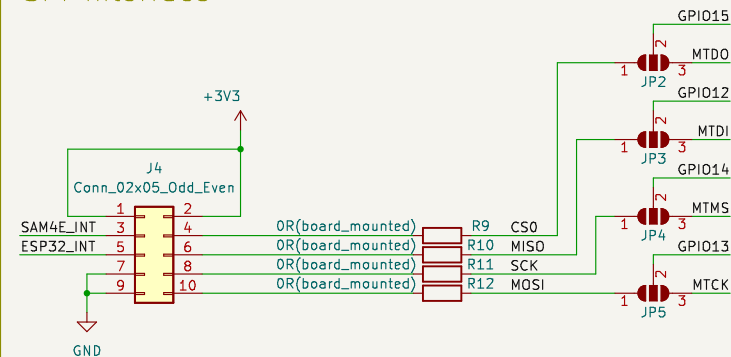
| Voltage supervisor added to safely shut down ESP32 when the power supply feeds less than 2.7V to the source pin.

Auto-program (Boot & Enable) is made available via UART interface to flash ESP32.

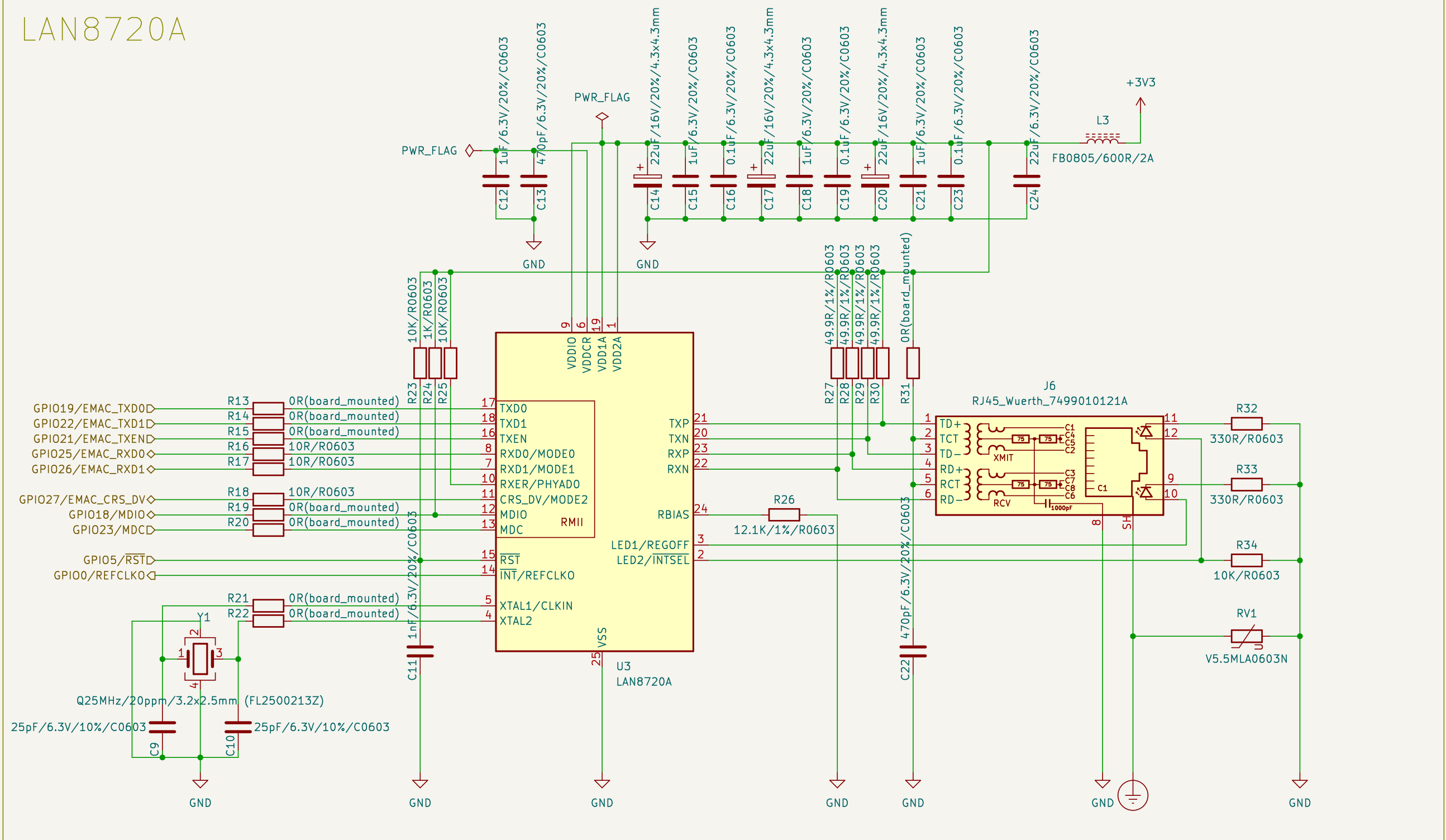
DTR	RTS	->	EN	100
1	1		1	1
0	0		1	1
1	0		0	1
0	1		1	0

The 00hm resistor may be removed in order to isolate the JTAG port from this system reset signal. Other 00hm resistors are present for debug purposes.

SPI interface and JTAG debug interface share the same 4 pins for communication. The hardware must be configured accordingly for each module to be accessed.



LAN8720A



Author: Nicolae-Andrei Vasile

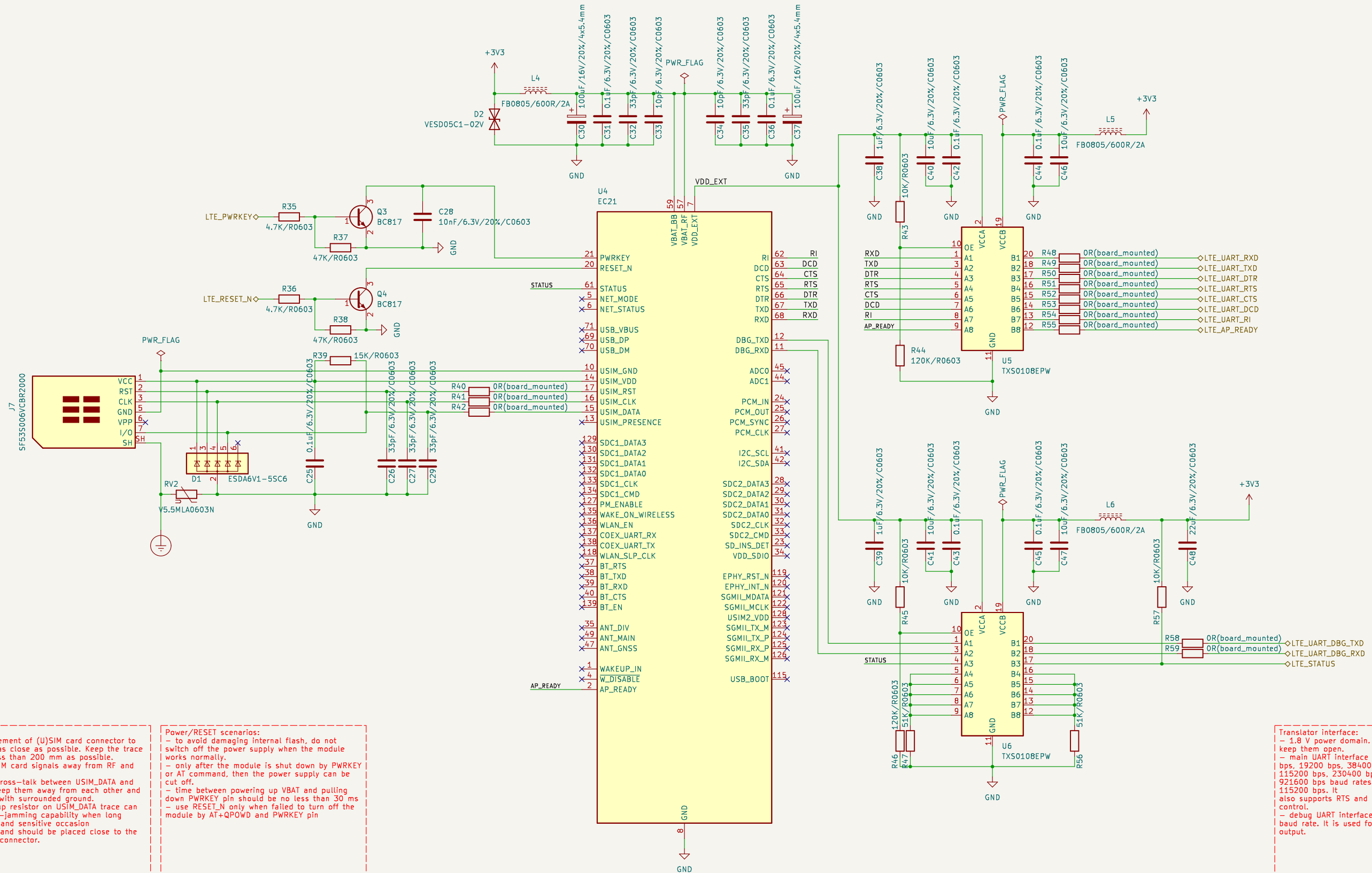
Sheet: /LAN8720A/
File: LAN8720A.kicad_sch

Title: ESP32

Size: A4 Date: 2023-12-22
KiCad E.D.A. kicad 7.0.9-7.0.9-ubuntu20.04.1

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LTE Cat-1 Quectel EC21



- (U)SIM card: keep placement of (U)SIM card connector to the module as close as possible. Keep the trace length as less than 200 mm as possible.
- keep (U)SIM card signals away from RF and VBAT traces.
- to avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- the pull-up resistor on USIM_DATA trace can improve anti-jamming capability when long layout trace and sensitive occasion are applied, and should be placed close to the (U)SIM card connector.

- Power/RESET scenarios:
 - to avoid damaging internal flash, do not switch off the power supply when the module works normally.
 - only after the module is shut down by PWRKEY or AT command, then the power supply can be cut off.
 - time between powering up VBAT and pulling down PWRKEY pin should be no less than 30 ms
 - use RESET_N only when failed to turn off the module by AT+QPOWD and PWRKEY pin

- Translator interface:
 - 1.8 V power domain. If UART pins are unused, keep them open.
 - main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps and 921600 bps baud rates, and the default is 115200 bps. It also supports RTS and CTS hardware flow control.
 - debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.

Author: Nicolae–Andrei Vasile

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