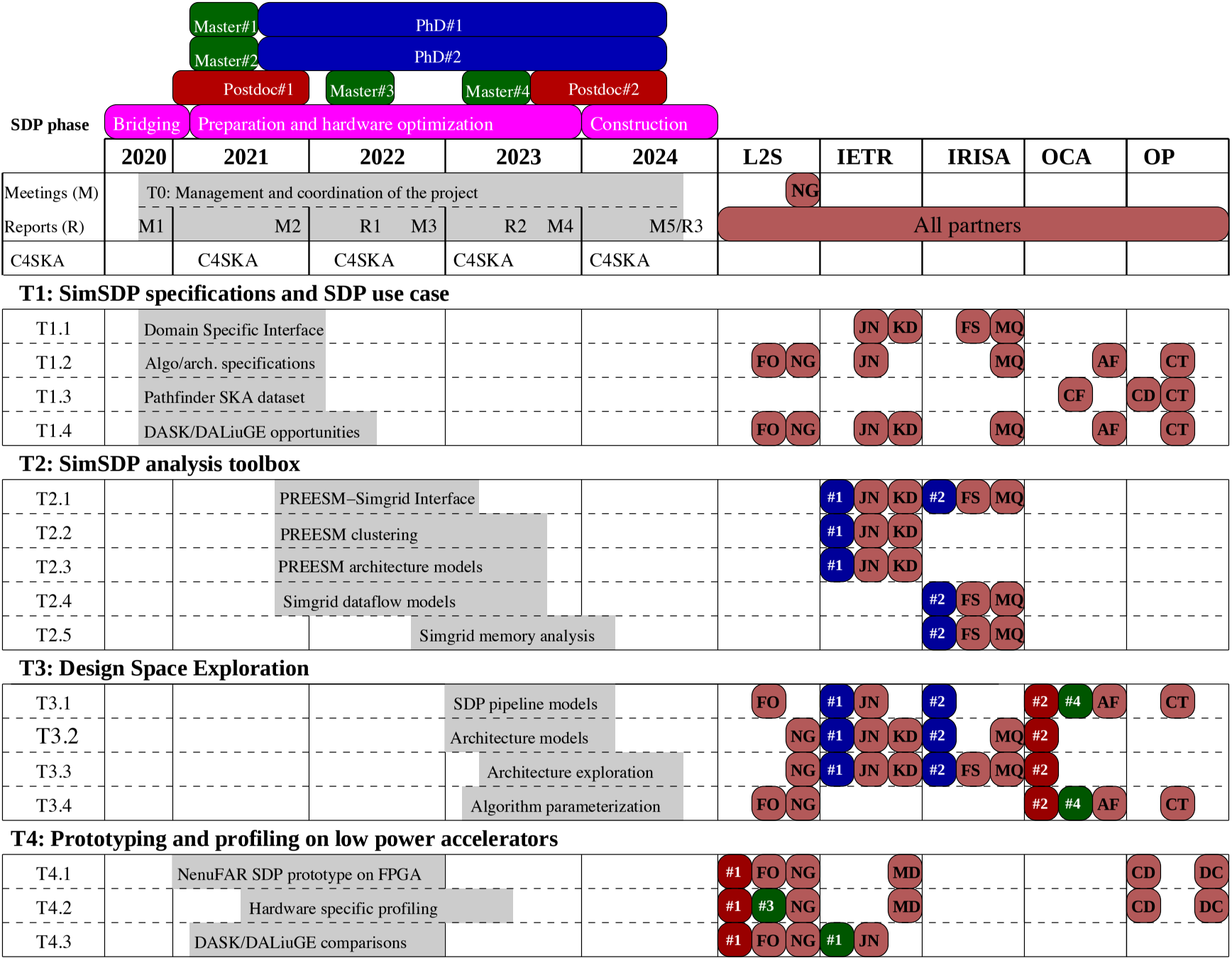
Master#1
PhD#1
Master#2
PhD#2
Postdoc#1
Master#3
Master#4
Postdoc#2
SDP phase
Bridging
Preparation and hardware optimization
Construction
2020
2021
2022
2023
2024
L2S
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IRISA
OCA
OP
Meetings (M)
T0: Management and coordination of the project
NG
Reports (R)
M1
M2
R1
M3
R2
M4
M5/R3
All partners
C4SKA
C4SKA
C4SKA
C4SKA
C4SKA
T1: SimSDP specifications and SDP use case
T1.1
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T1.2
Algo/arch. specifications
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JN
MQ
AF
CT
T1.3
Pathfinder SKA dataset
CF
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T1.4
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T2: SimSDP analysis toolbox
T2.1
PREESM–Simgrid Interface
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#2
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T2.2
PREESM clustering
#1
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PREESM architecture models
#1
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#2
FS
MQ
T2.5
Simgrid memory analysis
#2
FS
MQ
T3: Design Space Exploration
T3.1
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JN
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#2
#4
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T3.2
Architecture models
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KD
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MQ
#2
T3.3
Architecture exploration
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#1
JN
KD
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#2
T3.4
Algorithm parameterization
FO
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#4
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T4: Prototyping and profiling on low power accelerators
T4.1
NenuFAR SDP prototype on FPGA
#1
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NG
MD
CD
DC
T4.2
Hardware specific profiling
#1
#3
NG
MD
CD
DC
T4.3
DASK/DALiuGE comparisons
#1
FO
NG
#1
JN