Typical stages in digital signal processing

A/D Conversion

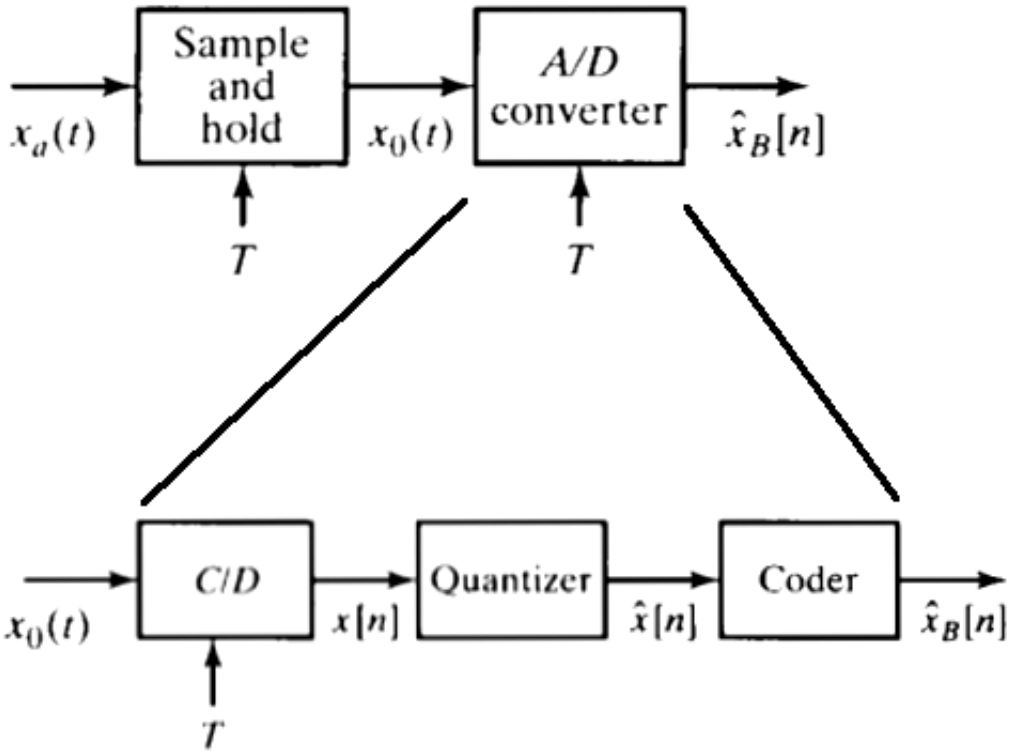
Dr. Ing. Rodrigo Gonzalez

rodralez@frm.utn.edu.ar
rodrigo.gonzalez@ingenieria.uncuyo.edu.ar

Summary

A/D Conversion Stages

- The A/D converter is a physical device that converts a voltage or current amplitude at its input into a binary code representing a quantized amplitude value closest to the amplitude of the input.
- The sample-and-hold stage can be a **zero-order-hold**.



Quantizer

- Uniformly spaced quantizer, function $Q(x)$.
- The number of quantization levels will be a power of two (2^B).
- Precision of quantizer, $\Delta = \frac{\text{full voltage range}}{2^{\text{word lenght}}} = \frac{2V_p}{2^B}$. $[mV]$

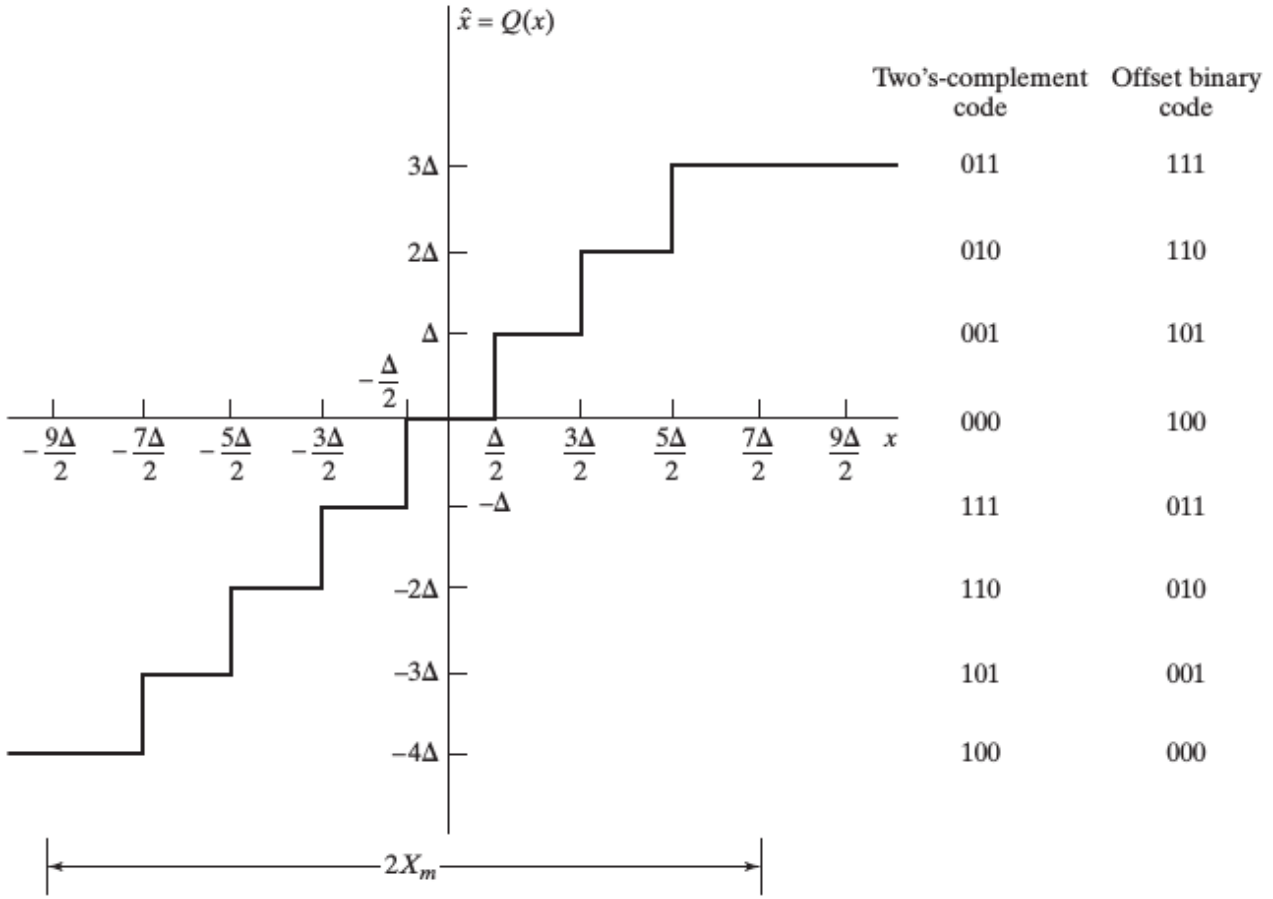


Figure 4.54 Typical quantizer for A/D conversion.

Quantizer Error example

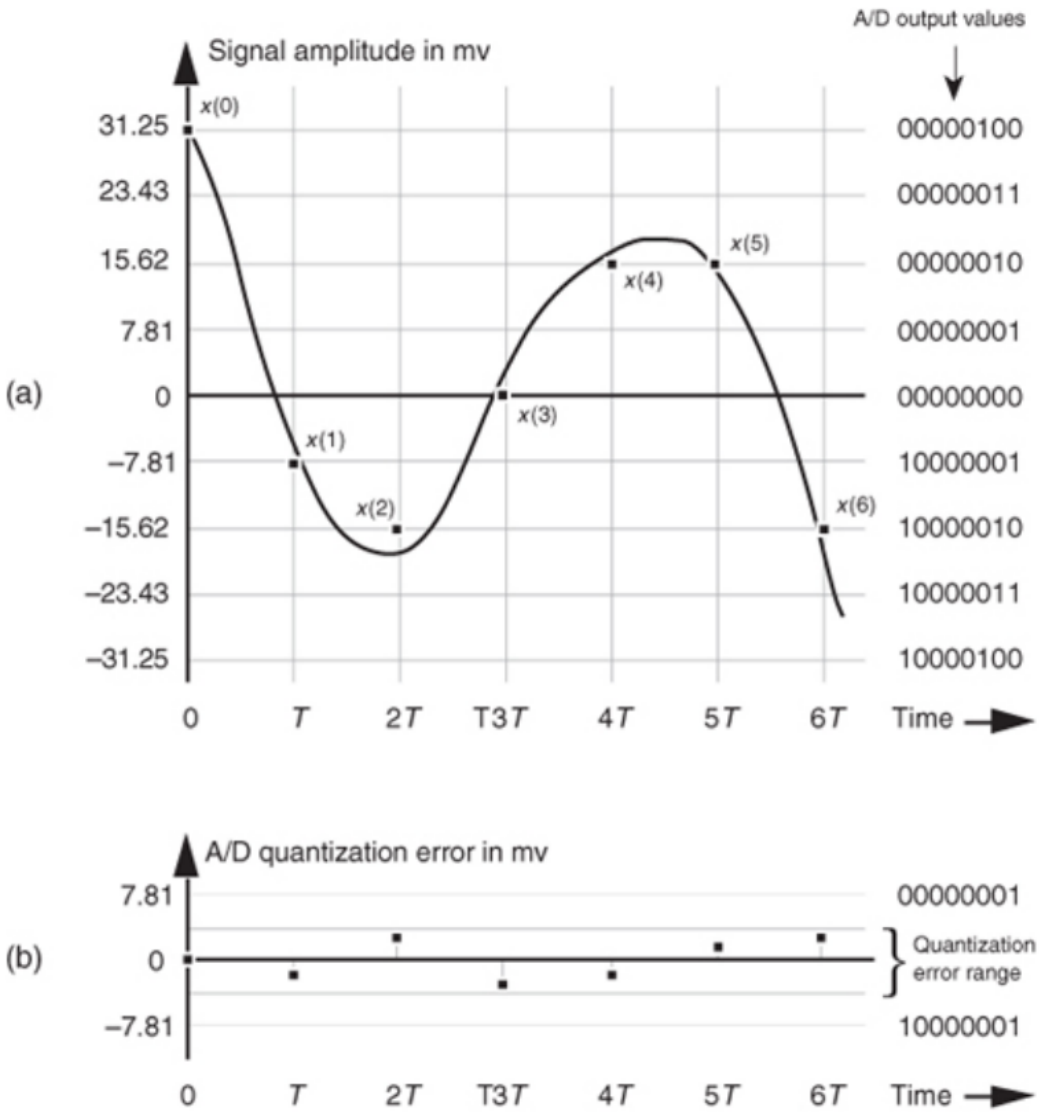


Figure: 12.1 [2]

Quantizer Error example, II

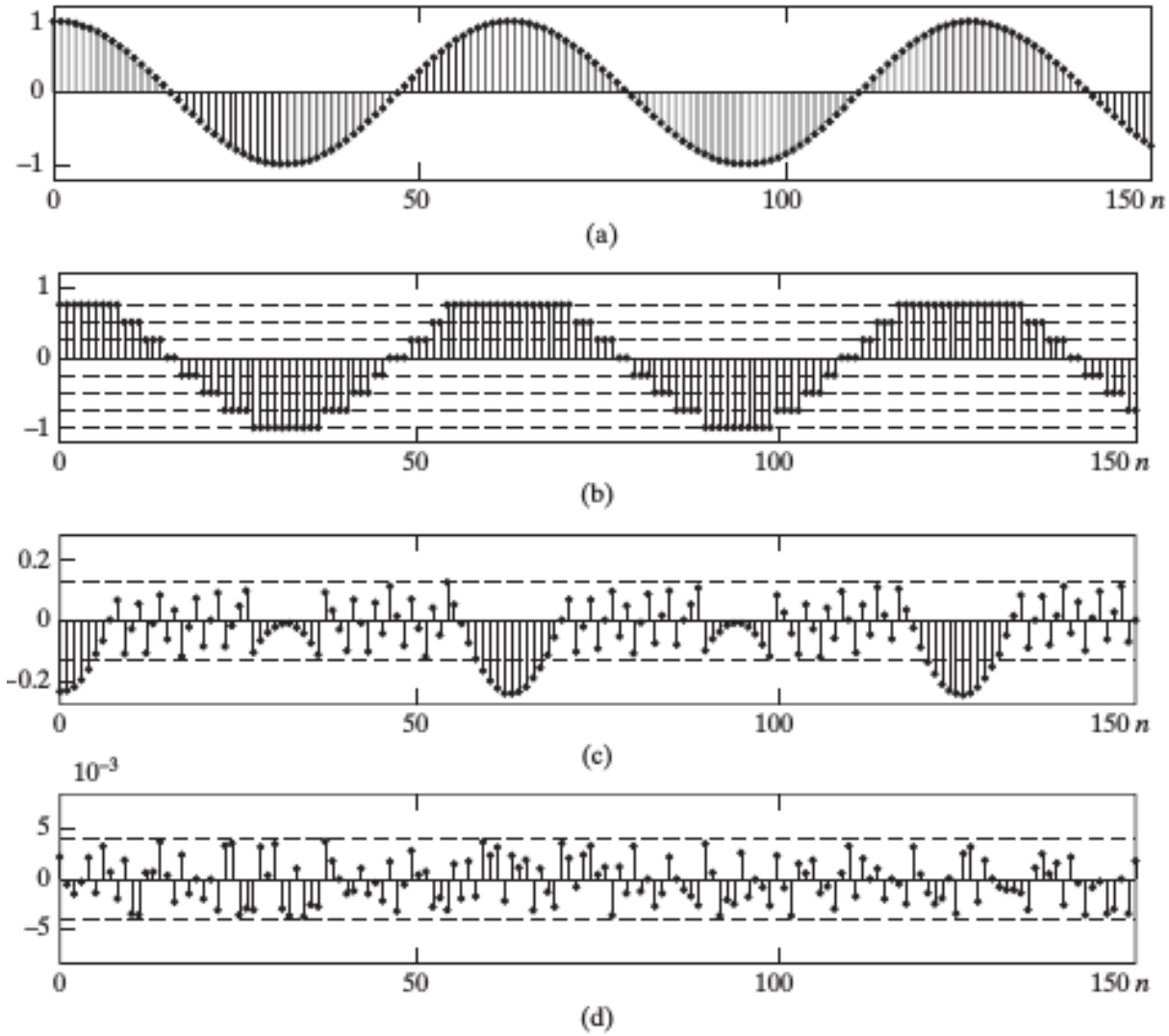


Figure 4.57 (*continued*) (b) Quantized samples of the cosine waveform in part (a) with a 3-bit quantizer. (c) Quantization error sequence for 3-bit quantization of the signal in (a). (d) Quantization error sequence for 8-bit quantization of the signal in (a).

Quantizer Error model

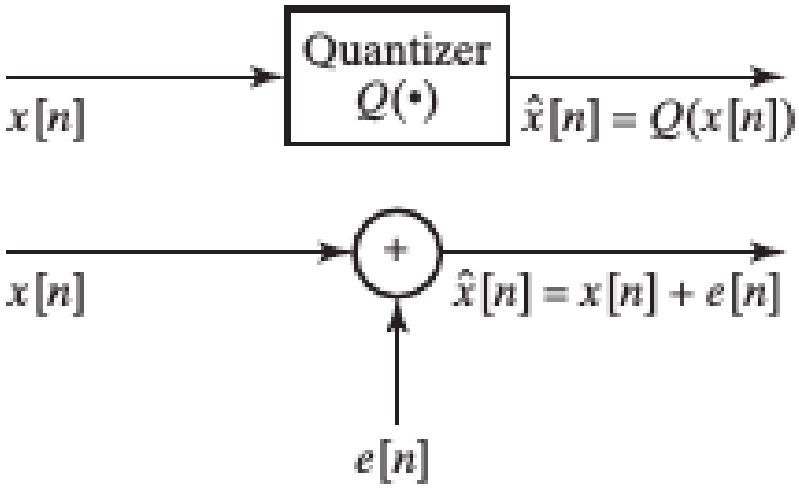


Figure 4.56 Additive noise model for quantizer.

ADC Signal-to-Noise relationship

The precision of the quantizer is given by [2]:

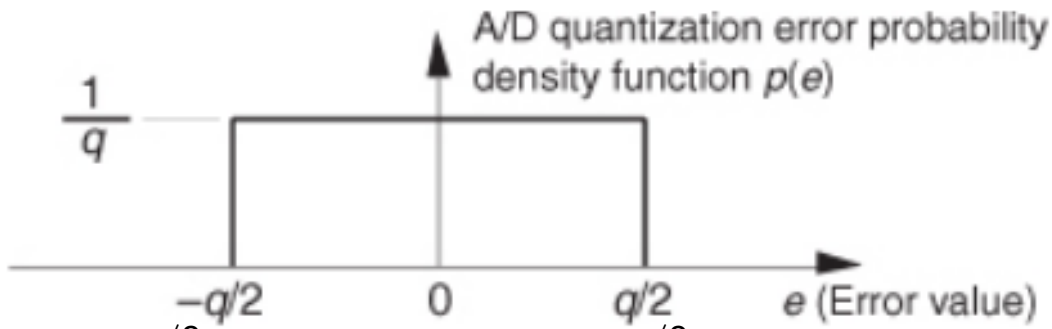
$$\Delta = q = \frac{\text{full voltage range}}{2^{\text{word lenght}}} = \frac{2V_p}{2^B} \,. \quad [mV] \tag{1}$$

- $SNR = (P_{signal})/(P_{noise})$ relates two powers.
- Since q is defined as a random variable, its power cannot be represented explicitly.
- A statistical version of SNR is used,

$$SNR_{ADC} = 10 \cdot \log_{10} \left(\frac{\text{input signal variance}}{\text{A/D quantization noise variance}} \right) \,, \quad [\text{dB}] \tag{2}$$

$$= 10 \cdot \log_{10} \left(\frac{\sigma^2_{signal}}{\sigma^2_{ADC}} \right) \,. \tag{3}$$

ADC Signal-to-Noise relationship, II



$$\sigma^2_{ADC} = \int_{-q/2}^{q/2} (e-\mu)^2 p(e)de = \int_{-q/2}^{q/2} e^2 p(e)de = \frac{1}{q}\int_{-q/2}^{q/2} e^2 de = \frac{q^2}{12}\,, \tag{4}$$

$$\sigma^2_{ADC} = \left(\frac{2V_p}{2^B}\right)^2 \cdot \frac{1}{12} = \boxed{\frac{V_p^2}{3\cdot 2^{2B}}}\,, \tag{5}$$

$$\text{Load Factor,}\quad LF = \frac{rms_{signal}}{V_p} = \frac{\sigma_{signal}}{V_p} \implies \sigma^2_{signal} = \boxed{LF^2 \cdot V_p^2}\,, \tag{6}$$

$$SNR_{ADC} = 10\cdot\log_{10}\left(\frac{\sigma^2_{signal}}{\sigma^2_{ADC}}\right)\,,$$

$$= 10\cdot\log_{10}\left[\left(LF^2\cdot V_p^2\right)\cdot\frac{3\cdot 2^{2B}}{V_p^2}\right] = 10\cdot\log_{10}\left[\left(LF^2\cdot 3\cdot 2^{2B}\right)\right]\,, \tag{7}$$

$$= 10\cdot\left[\log_{10}(LF^2) + \log_{10}(3) + 2\log_{10}(2)\cdot B\right]\,, \tag{8}$$

$$= 20\cdot\log_{10}(LF) + 4.77 + 6.02\cdot B\,. \quad \text{[dB]} \tag{9}$$

ADC Signal-to-Noise relationship considerations

$$SNR_{ADC} = 20 \cdot \log_{10}(LF) + 4.77 + 6.02 \cdot B\,, \quad \text{[dB]}$$
$$= 20 \cdot \log_{10}\left(\frac{rms_{signal}}{V_p}\right) + 4.77 + 6.02 \cdot B\,. \quad \text{[dB]}$$

Considerations about LF:

- Ideally, if $rms_{signal} >> V_p$, SNR_{ADC} **increases**, but this will produce a severe distortion in the sampling signal (saturation).
- On the other hand, if $rms_{signal} << V_p$, SNR_{ADC} **decreases**.

Considerations about B (numbers of bits):

- SNR_{ADC} increases 6 dB by each bit in ADC's quantizer.
- So, the more bits the better, isn't it?

Other sources of error should be taken into account:

- It was considered that ADC's $V_{MAX} = V_p$.
- The proposed model for tje probability density function of $e[n]$ may not be uniform.
- Therefore, SNR_{ADC} from Eq. 9 should be **decreased by 3 or 6 dB**.

ADC Signal-to-Noise relationship for a sinusoidal signal

For a sinusoidal signal, $rms_{signal} = V_p/\sqrt{2}$.

$$SNR_{ADC} = 20 \cdot \log_{10}\left(\frac{rms_{signal}}{V_p}\right) + 4.77 + 6.02 \cdot B\,, \tag{10}$$

$$= 20 \cdot \log_{10}\left(\frac{V_p/\sqrt{2}}{V_p}\right) + 4.77 + 6.02 \cdot B\,. \tag{11}$$

Thus, the maximum SNR_{ADC} is,

$$SNR_{ADC} = 20 \cdot \log_{10}\left(1/\sqrt{2}\right) + 4.77 + 6.02 \cdot B\,, \tag{12}$$

$$= -3.01 + 4.77 + 6.02 \cdot B\,, \tag{13}$$

$$= 1.76 + 6.02 \cdot B\,. \quad \text{[dB]} \tag{14}$$

ADC resolution for a particular signal

Consider the following example:

- The SNR for an audio output amplifier is 110 dB.
- A 24-bits ADC is chosen to sample the output amplifier (professional audio).
- The amplifier is excited by an input sinusoidal signal.

$$SNR_{ADC} = 1.76 + 6.02 \cdot 24 - 3 = 143.24 \text{ dB}\,.$$

- How many bits are used to measure noise? $(143 - 110)/6 \simeq 5.5$ bits!.
- In a control loop, picking a bad ADC resolution could lead to a catastrophic scenario.
- What happens if $B = 10$ bits? $SNR_{ADC} = 61.96$ dB, $(110 - 61.96)/6 \simeq 8$ extra bits are needed!.

Summary: the number of bits B in an ADC must provide $SNR_{ADC} \geqslant SNR_{signal}$.

- Rule of thumb: the ADC resolution should be choose in order to provide 6 dB (1 bit) above the SNR of the signal to be sample.
- Additional bits (noisy bits) can be eliminated by right shifting.

  In C: `adc_read >>= 5`.

Bibliography

1. Alan V. Oppenheim and Ronald W. Schafer. *Discrete-time signal processing, 3rd Ed.* Prentice Hall. 2010. Section 4.8.
2. Richard G. Lyons. *Understanding Digital Signal Processing, 3rd Ed.* Prentice Hill. 2010. Section 12.3.1.
3. Paolo Prandoni and Martin Vetterli. Signal processing for communications. Taylor and Francis Group, LLC. 2008. Section 9.6.