

Maurizio Valle
Paolo Gastaldo
Ernesto Limiti *Editors*

Proceedings of SIE 2024

55th Annual Meeting of the Italian
Electronics Society

Series Editors

Leopoldo Angrisani, *Department of Electrical and Information Technologies Engineering, University of Napoli Federico II, Napoli, Italy*

Marco Arteaga, *Departament de Control y Robótica, Universidad Nacional Autónoma de México, Coyoacán, Mexico*

Samarjit Chakraborty, *Fakultät für Elektrotechnik und Informationstechnik, TU München, Munich, Germany*
Shanben Chen, *School of Materials Science and Engineering, Shanghai Jiao Tong University, Shanghai, China*

Tan Kay Chen, *Department of Electrical and Computer Engineering, National University of Singapore, Singapore, Singapore*

Rüdiger Dillmann, *University of Karlsruhe (TH) IAIM, Karlsruhe, Germany*

Haibin Duan, *Beijing University of Aeronautics and Astronautics, Beijing, China*

Gianluigi Ferrari, *Dipartimento di Ingegneria dell'Informazione, Sede Scientifica Università degli Studi di Parma, Parma, Italy*

Manuel Ferre, *Centre for Automation and Robotics CAR (UPM-CSIC), Universidad Politécnica de Madrid, Madrid, Spain*

Sandra Hirche, *Department of Electrical Engineering and Information Science, Technische Universität München, Munich, Germany*

Faryar Jabbari, *Department of Mechanical and Aerospace Engineering, University of California, Irvine, USA*

Limin Jia, *State Key Laboratory of Rail Traffic Control and Safety, Beijing Jiaotong University, Beijing, China*

Janusz Kacprzyk, *Intelligent Systems Laboratory, Systems Research Institute, Polish Academy of Sciences, Warsaw, Poland*

Alaa Khamis, *Department of Mechatronics Engineering, German University in Egypt El Tagamo El Khames, New Cairo City, Egypt*

Torsten Kroeger, *Intrinsic Innovation, Mountain View, USA*

Yong Li, *College of Electrical and Information Engineering, Hunan University, Changsha, China*

Qilian Liang, *Department of Electrical Engineering, University of Texas at Arlington, Arlington, USA*

Ferran Martín, *Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Bellaterra, Spain*

Tan Cher Ming, *College of Engineering, Nanyang Technological University, Singapore, Singapore*

Wolfgang Minker, *Institute of Information Technology, University of Ulm, Ulm, Germany*

Pradeep Misra, *Department of Electrical Engineering, Wright State University, Dayton, USA*

Subhas Mukhopadhyay, *School of Engineering, Macquarie University, Sydney, NSW, Australia*

Cun-Zheng Ning, *Department of Electrical Engineering, Arizona State University, Tempe, AZ, USA*

Toyoaki Nishida, *Department of Intelligence Science and Technology, Kyoto University, Kyoto, Japan*

Luca Oneto, *Department of Informatics, Bioengineering, Robotics and Systems Engineering, University of Genova, Genova, Italy*

Bijaya Ketan Panigrahi, *Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India*

Federica Puccetti, *Department di Ingegneria, Università degli Studi Roma Tre, Rome, Italy*

Yong Qin, *State Key Laboratory of Rail Traffic Control and Safety, Beijing Jiaotong University, Beijing, China*

Gan Woon Seng, *School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, Singapore*

Joachim Speidel, *Institute of Telecommunications, University of Stuttgart, Stuttgart, Germany*

Germano Veiga, *FEUP Campus, INESC Porto, Porto, Portugal*

Haitao Wu, *Academy of Opto-electronics, Chinese Academy of Sciences, Beijing, China*

Walter Zamboni, *Department of Computer Engineering, Electrical Engineering and Applied Mathematics, DIEM—Università degli studi di Salerno, Fisciano, Italy*

Kay Chen Tan, *Department of Computing, Hong Kong Polytechnic University, Hong Kong, Hong Kong*

The book series *Lecture Notes in Electrical Engineering* (LNEE) publishes the latest developments in Electrical Engineering—quickly, informally and in high quality. While original research reported in proceedings and monographs has traditionally formed the core of LNEE, we also encourage authors to submit books devoted to supporting student education and professional training in the various fields and applications areas of electrical engineering. The series cover classical and emerging topics concerning:

- Communication Engineering, Information Theory and Networks
- Electronics Engineering and Microelectronics
- Signal, Image and Speech Processing
- Wireless and Mobile Communication
- Circuits and Systems
- Energy Systems, Power Electronics and Electrical Machines
- Electro-optical Engineering
- Instrumentation Engineering
- Avionics Engineering
- Control Systems
- Internet-of-Things and Cybersecurity
- Biomedical Devices, MEMS and NEMS

For general information about this book series, comments or suggestions, please contact leontina.dicecco@springer.com.

To submit a proposal or request further information, please contact the Publishing Editor in your country:

China

Jasmine Dou, Editor (jasmine.dou@springer.com)

India, Japan, Rest of Asia

Swati Meherishi, Editorial Director (Swati.Meherishi@springer.com)

Southeast Asia, Australia, New Zealand

Ramesh Nath Premnath, Editor (ramesh.premnath@springernature.com)

USA, Canada

Michael Luby, Senior Editor (michael.luby@springer.com)

All other Countries

Leontina Di Cecco, Senior Editor (leontina.dicecco@springer.com)

**** This series is indexed by EI Compendex and Scopus databases. ****

Maurizio Valle · Paolo Gastaldo · Ernesto Limiti
Editors

Proceedings of SIE 2024

55th Annual Meeting of the Italian Electronics Society



Springer

Editors

Maurizio Valle
DITEN
University of Genoa
Genoa, Italy

Paolo Gastaldo
DITEN
University of Genoa
Genoa, Italy

Ernesto Limiti
DIE
University of Rome Tor Vergata
Rome, Italy

ISSN 1876-1100 ISSN 1876-1119 (electronic)

Lecture Notes in Electrical Engineering

ISBN 978-3-031-71517-4 ISBN 978-3-031-71518-1 (eBook)

<https://doi.org/10.1007/978-3-031-71518-1>

© The Editor(s) (if applicable) and The Author(s), under exclusive license
to Springer Nature Switzerland AG 2025

This work is subject to copyright. All rights are solely and exclusively licensed by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, expressed or implied, with respect to the material contained herein or for any errors or omissions that may have been made. The publisher remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

This Springer imprint is published by the registered company Springer Nature Switzerland AG
The registered company address is: Gewerbestrasse 11, 6330 Cham, Switzerland

If disposing of this product, please recycle the paper.

Preface

This book collects the original papers presented at the 55th Annual Meeting of the Italian Electronics Society (Società Italiana di Elettronica - SIE), held in Genova, Italy, on June 26–28, 2024. The Italian Electronics Society is a non-profit association aiming at promoting and developing training, research, and technology transfer activities in the field of Electronics conducted by its members and affiliated institutions.

The SIE-2024 Annual Meeting program included invited talks given by experts in fields of interest for the Italian Electronics community, oral sessions, round tables, and exhibitions by companies with on-site demonstrations of instrumentation, devices, and systems.

The conference received a total of 65 original contributions in the following 7 areas:

- Area 1 – Integrated Circuits and Systems
- Area 2 – Micro- and Nano-Electronic Devices
- Area 3 – Microwave Electronics
- Area 4 – Sensors, Microsystems, and Instrumentation
- Area 5 – Optoelectronics and Photonics
- Area 6 – Power Electronics
- Area 7 – Electronic Systems and Applications

Works submitted to the conference underwent a peer-review process, with each paper evaluated by at least two experts selected by the conference committee. After comprehensive verification of technical content and plagiarism, we ended up with 61 papers published in the proceedings.

Contributions in Area 1 focus on the design of advanced functional blocks for analog and digital ASICs, covering topics such as neural networks, fault mitigation techniques, and Physical Unclonable Function (PUF) architectures. Contributions in Area 2 include works dealing with Raman micro-thermometer for self-heating analysis, semi-analytical model for the potential profile in the semiconductor channel of two-dimensional Dirac-source FETs, and simulation framework for hole spin qubits. Contributions in Area 3 target the design of a new generation of low-noise amplifiers, power dividers, and power amplifiers. Contributions in Area 4 focus both on the design and applications of sensing systems; the addressed topics include biosensors for both antibody and antigen detection, human activity recognition by head-worn devices, and an ASIC for the front-end charge readout to be implemented in the Lunar Electromagnetic Monitor in X-rays. Contributions in Area 5 cover topics such as the integration of CMOS analog electronics into a standard Silicon Photonics platform, the characterization of a pixeded plasmonic metasurface as Surface-Enhanced InfraRed Absorption (SEIRA) spectroscopy platform, and the development of a Lab-on-Fiber self-heating platform for accurate monitoring of volumetric water content in soil. Contributions in Area 6 include an investigation on the thermal, electrical, and mechanical behavior of new prepackage embedding technologies for wide band gap power devices, the design of quasi-planar trench (QPT) power MOSFET, an analysis of the limitations of the double-sided cooled (DSC), which is a

state-of-the-art solution for manufacturing power modules technology. Contributions in Area 7 target topics such as architectures for full-digital tunable True Random Number Generators, enabling tiny machine learning on ultra-low-power microcontroller units, and the integration of photoplethysmographic (PPG) sensors into smart glasses.

These proceedings are a quite comprehensive overview of the current research activities in which members of the SIE are involved. Besides the relevance of the scientific contents that will certainly attract the attention of researchers active in many research fields, even outside the boundaries of the discipline, we expect these proceedings to act as a catalyst for favoring the development of international collaborations.

The scientific value of a conference can only be as good as the contributions by the authors participating in it. Therefore, we would like to thank all the authors who have contributed with original works and with enjoyable presentations.

Finally, we would like to thank the several sponsoring companies that have contributed both with their financial support and with their presence in dedicated spaces and sessions. Sponsors have notably included: large semiconductor companies, small and medium-sized high-tech companies whose focus is the development of electronic devices and systems, and companies for which electronics represent an enabling technology. This in turn proves that the awareness on the fundamental role of electronics in industry in general is increasing.

July 2024

Organization

General Chairs

Ernesto Limiti
Paolo Gastaldo
Maurizio Valle

Technical Program Committee

Andrea Bonfanti
Domenico Caputo
Antonio D'Alessandro
Simona Donati Guerrieri
David Esseni
Massimo Ruo Roch
Giorgio Spiazzi

Local Organizing Committee

Orazio Aiello
Christian Gianoglio
Edoardo Ragusa
Chiara Micheli
Silvia Ferrari
Filippo Parisi

Sponsors



www.leonardo.com



www.nxp.com



www.st.com



www.infineon.com



www.idvgroup.com



www.marvell.com



www.synopsys.com



www.3brain.com



www.aeit.it



www.icos-semiconductors.eu



www.alldata.it



www.analog.com



www.canovatech.com



www.inventvm.com



www.skytechnologies.it

x Organization



www.ansaldoenergia.com



www.rf-microwave.com



www.gruppofos.it

Contents

Integrated Circuits and Systems

On-Chip Analog Neural Network for Edge Computing in Radiation Detectors	3
<i>Susanna Di Giacomo, Michele Ronchi, Mattia Amadori, Marco Carminati, Giacomo Borghi, and Carlo Fiorini</i>	
A High-Voltage LDO Voltage Regulator Featuring Enhanced Transient Response and Reduced Area	12
<i>Jacopo Serra and Franco Fiori</i>	
A Low-Cost Fault Tolerance Technique for Microcontroller-Class RISC-V Processors	21
<i>Riccardo Tedeschi, Alessandro Nadalini, Filippo Grillotti, Fabio De Ambroggi, Elio Guidetti, Luca Benini, and Davide Rossi</i>	
Exploiting the Latched Ring Oscillator Cell as a Compact PUF Architecture on FPGA	29
<i>Riccardo Della Sala and Giuseppe Scotti</i>	
Low Power Design of Approximate Adders Based on Inexact Full Adder	35
<i>Ali Ibrahim, Fatima Bzeih, Oussama Srour, Zeinab Hijazi, and Orazio Aiello</i>	
0.7 V, 215 nW Tunable Universal Gm-C Filter	41
<i>Ali Namdari, Orazio Aiello, and Daniele D. Caviglia</i>	
Operating Principles and Power Consumption of DB-OTAs	48
<i>Paolo Faustini, Andrea Rosa, Luigi Colalongo, and Anna Richelli</i>	

Micro- and Nano-Electronic Devices

Semi-analytical Model for the Estimation of the Subthreshold Swing in Dirac-Source FETs	61
<i>Tommaso Ugolini, Giorgio Baccarani, and Elena Gnani</i>	
Anomalous I-V Characteristics of 4H-SiC p-i-n Diode at Cryogenic Temperature	71
<i>Nicola Rinaldi, Luigi Di Benedetto, Gian Domenico Licciardo, Rosalba Liguori, and Alfredo Rubino</i>	

Rutile TiO ₂ Nanoparticles as Raman Micro-thermometer for Self-heating Analysis	77
<i>Francesca Zarotti, Ernesto Limiti, and Andrea Reale</i>	
Simulation Framework for Hole Spin Qubits	85
<i>Lorenzo Raschi and Antonio Gnudi</i>	
Effect of Phase Noise in Superconducting Qubit Control	94
<i>Agata Barsotti, Gregorio Prociassi, Carola Ciaramelletti, Paolo Marconcini, Leonardo Guidoni, Simone Paganelli, and Massimo Macucci</i>	
Microwave Electronics	
Advanced Interconnect Solutions for Millimetre-Wave Low-Noise Amplifiers	105
<i>Patrick Ettore Longhi, Walter Ciccognani, Sergio Colangeli, Peiman Parand, Antonio Serino, and Ernesto Limiti</i>	
A Wideband L-band Integrated Low Noise Amplifier	113
<i>Sergio Colangeli, Patrick E. Longhi, Walter Ciccognani, and Ernesto Limiti</i>	
A Filtering Single-Ended-to-Balanced Power Divider with Enhanced Ultra-Wideband Suppression	121
<i>Leidan Pan, Yongle Wu, Weimin Wang, Anna Piacibello, and Vittorio Camarchia</i>	
Challenges of 9-dB Back-Off Doherty Power Amplifiers with 20% Fractional Bandwidth	132
<i>Zhifan Zhang, Anna Piacibello, and Vittorio Camarchia</i>	
Low-Cost Calibrated Microwave Radiometers for Solar Observation: From Education to Science	142
<i>Giacomo Schiavolini, Giulio Brancali, Ethan Bernardini, Giulia Orecchini, Valentina Palazzi, Camille C. A. Westerhof, Timo S. Prinz, Martin Hübner, Sebastian Lange, Maurizio Burla, and Federico Alimenti</i>	

Sensors Microsystems and Instrumentation

Resistorless Current-Mode Schmitt Trigger for Single-Event Detection in Photomultipliers Front-Ends	163
<i>Davide Colaiuda, Alfiero Leoni, Gianluca Barile, Vincenzo Stornelli, and Giuseppe Ferri</i>	
The Front-End Charge Readout IC for the LEM-X Mission Concept	170
<i>Filippo Mele, Marco Grassi, Irisa Dedolli, Piero Malcovati, Riccardo Campana, Ettore Del Monte, Yuri Evangelista, Marco Feroci, and Giuseppe Bertuccio</i>	
Sensor-Based Monitoring of Physical Activity for Glucose Management in Diabetic Patients: A Review	177
<i>Sara Campanella and Lorenzo Palma</i>	
Analysis of Non-linearity Sources in Piezoresistive Gyroscopic Systems	189
<i>Gabriele Laita, Andrea Buffoli, and Giacomo Langfelder</i>	
Effect of Intrinsic Layer Thickness on the Performances of Amorphous Silicon P-I-N Junction	199
<i>Nicola Lovecchio, Silvia Casaliniuovo, Augusto Nascetti, Giampiero de Cesare, and Domenico Caputo</i>	
Role of Feedthrough Capacitance in Mode-Split MEMS Gyroscope Bias-Instability	205
<i>Luca Pileri and Giacomo Langfelder</i>	
Efficient Human Activity Recognition: Machine Learning at the Sensor Level	213
<i>Arianna De Vecchi, Alice Scandelli, Federica Bossi, Benedetta Caterina Casadei, Hazem Hesham Yousef Shalby, Marco Boschi, and Federica Villa</i>	
Bio-reconfigurable Impedance-Based Platform for Multiplexing Diagnostic	221
<i>Arianna Adelaide Maurina, Cainã de Oliveira Figares, Francesco Damin, Chiara Capelli, Laura Sola, Marcella Chiari, Francesco Zanetto, Giorgio Ferrari, and Marco Sampietro</i>	
Architectural Modeling and Experimental Characterization of a SPAD-Based Imager Developed for Fast-Quantum Ghost Imaging Applications	228
<i>Enrico Manuzzato, Massimo Gandola, Matteo Perenzoni, Leonardo Gasparini, and Roberto Passerone</i>	

Pilot Study: Experimental Analysis of PVDF Sensors Response to Slippage	238
<i>Razan Khalifeh, Christian Gianoglio, Yahya Abbass, and Maurizio Valle</i>	
Stability and Functionalization of Carbon Nanotube Electrolyte-Gated Field-Effect Transistors	244
<i>Anna Tagliaferri, Bajramshahe Shkodra, Martina Aurora Costa Angeli, Moritz Ploner, Mattia Petrelli, Antonio Altana, Pietro Iba, Paolo Lugli, and Luisa Petti</i>	
Stress Transmission in a Soft Electronic Skin with Viscoelastic Properties	251
<i>Chiara Micheli, Giovanni Berselli, and Lucia Seminara</i>	
FPGA Implementation of a Convolutional Recurrent Neural Network for Real-Time Sensor Data Processing	258
<i>Riccardo Testa, Mohamad Yaacoub, Christian Gianoglio, and Maurizio Valle</i>	
Electrical Characterization of Red Blood Cells with a Nanoelectrode Array Sensor	266
<i>Mariano José Guillén, Jacopo Nicolini, Daniele Goldoni, Rossana Madrid, and Luca Selmi</i>	
The Safety Monitoring System for the SND@LHC Experiment at CERN	274
<i>Francesco Fienga, Vincenzo Romano Marrazzo, Michele Riccio, Antonia Di Crescenzo, Giovanni De Lellis, Salvatore Buontempo, Andrea Irace, and Giovanni Breglio</i>	
Optoelectronics and Photonics	
Experimentally Validated Model of the Optoelectronic and Photonic Section of the Interferometric Fiber-Optic Gyroscope	285
<i>Teresa Natale and Francesco Dell'Olio</i>	
A Novel Lab-on-Fiber Platform for Soil Water Content Monitoring	292
<i>G. M. Berruti, M. Leone, P. Vaiano, G. V. Persiano, M. Consales, and A. Cusano</i>	
Integrating CMOS Analog Electronics in Silicon Photonics	301
<i>Francesco Zanetto, Monica Crico, Samuele De Gaetano, Giorgio Ferrari, and Marco Sampietro</i>	
Detection of Selected IR Signatures Through SEIRA Sensing Platform	308
<i>Valentina Di Meo, Alessio Crescitelli, Massimo Moccia, Emanuela Iaccarino, Annamaria Sandomenico, Vincenzo Galdi, Menotti Ruvo, Ivo Rendina, and Emanuela Esposito</i>	

Optoelectronic Characterization of Nano-Diamond/crystalline Silicon Heterostructures	316
<i>Arpana Singh, Marinus Kunst, Diana Sannino, Vito Speranza, Vincenzo Carrano, and Heinz-Christoph Neitzert</i>	
Real-Time Reconfiguration of Free-Space Optical Receivers by Means of Fully Integrated CMOS Controller	322
<i>Emanuele Sacchi, Francesco Zanetto, Francesco Morichetti, Andrea Melloni, Marco Sampietro, and Giorgio Ferrari</i>	
A Plethysmographic Sensor Based on FBG Embedded in a Soft Silicone Patch	328
<i>Mariaconsiglia Cuomo, Elena De Vita, Vincenzo Romano Marrazzo, Giovanni Breglio, Agostino Iadicicco, and Stefania Campopiano</i>	
Fiber Optic Probes Exploiting Localized Surface Plasmon Resonance for Chemical Detection	335
<i>Amin Moslemi, Lucia Sansone, Flavio Esposito, Stefania Campopiano, Michele Giordano, and Agostino Iadicicco</i>	
True Time Delay System Using Phase Change Materials	341
<i>Rahuldas Kutteeri, Martino De Carlo, Francesco De Leonardi, Richard A. Soref, and Vittorio M. N. Passaro</i>	
Power Electronics	
Model-Based Design and AI for Monitoring Systems in Automotive Power Electronics	351
<i>Pierpaolo Dini, Sergio Saponara, Giovanni Basso, and Claudio Romano</i>	
In-Depth Analysis of the Electrical Ruggedness of Double-Sided Cooled Power Modules	362
<i>Antonio Pio Catalano, Ciro Scognamillo, and Vincenzo d'Alessandro</i>	
Out-of-SOA Performance of 3.3 kV SiC MOSFETs: Comparison Between Planar and Quasi-Planar Trench	369
<i>C. Scognamillo, A. Borghese, K. Melnyk, I. Nistor, V. d'Alessandro, M. Boccarossa, V. Terracciano, M. Riccio, A. P. Catalano, G. Breglio, N. Lophitis, M. Antoniou, M. Rahimo, A. Irace, and L. Maresca</i>	
An Ultra-Fast Overcurrent Protection Circuit Based on SMD Shunt Resistors for Wide Band-Gap Devices	375
<i>Emanuele Martano, Giovanni Busatto, Annunziata Sanseverino, Simone Palazzo, and Francesco Velardi</i>	

Performance Analysis of a Custom DC-DC Buck Converter for Smart Plug Applications in Nanogrids	382
<i>Danilo Santoro, Armel Asongu Nkembi, Paolo Cova, and Nicola Delmonte</i>	
Modeling and Optimization of 1.2 kV SiC-Based Pre-package Power Module in Half-Bridge Arrangement Using Finite Element Analysis	390
<i>Saimir Frroku, Ankit Bhushan Sharma, Till Huesgen, Andrea Irace, and Giovanni A. Salvatore</i>	
Electronic Systems and Applications	
Supporting in-Sensor Computing with Hardware-Aware Neural Architecture Search	407
<i>Andrea Mattia Garavagno, Edoardo Ragusa, Rodolfo Zunino, Antonio Frisoli, and Paolo Gastaldo</i>	
Enhancing Vibration Inspection via Compressed Sensing Based on Embedded Phase Change Memories	413
<i>Federica Zonzini, Francesco Zavalloni, Daniele Martinelli, Alessio Antolini, Eleonora Franchi Scarselli, Marco Pasotti, and Luca De Marchi</i>	
Towards Energy-Efficient Smart Sensing Nodes for Automatic Structural Health Monitoring	422
<i>Edoardo Ragusa, Federica Zonzini, Paolo Gastaldo, Rodolfo Zunino, and Luca De Marchi</i>	
A Multi-parameter Sensing Device for Vital Signs Monitoring	429
<i>Chiara Botrugno, Elisabetta Leogrande, Teresa Natale, and Francesco Dell'Olio</i>	
A Front-End Board for Modular Ultrasound Open Scanners	435
<i>F. Lagonigro, A. Vignoli, V. Meacci, P. Verdi, P. Tortoli, A. Ramalli, and E. Boni</i>	
Miniaturized Low-Power Head-Mounted PPG Board	441
<i>Alice Scandelli, Ilaria Crupi, Andrea Giudici, Pietro Bartoli, Arianna De Vecchi, Giacomo Gervasoni, Diana Trojaniello, and Federica Villa</i>	

A Modular Portable Current Stimulator for Electrical Stimulation of Excitable Tissues	448
<i>Riccardo Collu, Stefano Lai, Antonello Mascia, Roberto Paolini, Elena Ferrazzano, Loredana Zollo, Piero Cosseddu, and Massimo Barbaro</i>	
Investigating Cutaneous Mechanoreceptors for Neuromorphic Tactile Texture Classification	456
<i>Haydar Al Haj Ali, Yahya Abbass, Christian Gianoglio, and Maurizio Valle</i>	
On-Edge 1-D Convolutional Neural Network for Hand-Gesture Classification	462
<i>Daniella Shebly, Haydar Al Haj Ali, Mohamad Yaacoub, Hussein Chibli, Maurizio Valle, and christian Gianoglio</i>	
TinyML Acceleration with MAX78000	468
<i>Ali Dabbous, Luca Lazzaroni, Francesco Bellotti, Sara Muñoz Presentación, Alessandro Pighetti, and Riccardo Berta</i>	
Classification of Skiing Techniques on Embedded System	475
<i>Matteo Fresta, Francesco Bellotti, Alessio Capello, Marianna Cossu, Luca Forneris, and Riccardo Berta</i>	
Enhancing μNAS for 1D CNNs on Microcontrollers	481
<i>Alessio Capello, Riccardo Berta, Hadi Ballout, Matteo Fresta, Vafali Soltanmuradov, and Francesco Bellotti</i>	
Digital Low-Complexity Entropy Estimator Based on the Direct Assessment of Average Shannon Entropy	487
<i>Tommaso Addabbo, Ada Fort, Filippo Spinelli, and Valerio Vignoli</i>	
Author Index	493

Integrated Circuits and Systems



On-Chip Analog Neural Network for Edge Computing in Radiation Detectors

Susanna Di Giacomo^{1,2(✉)}, Michele Ronchi^{1,2}, Mattia Amadori^{1,2},
Marco Carminati^{1,2}, Giacomo Borghi^{1,2}, and Carlo Fiorini^{1,2}

¹ Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano,
Milan 20133, Italy
susanna.digiacomo@polimi.it

² Istituto Nazionale di Fisica Nucleare (INFN), Sez. di Milano, Milan 20133, Italy

Abstract. This work presents an analog on-chip neural network for embedded processing of gamma rays in radiation detectors, featuring 64 inputs, two 20-neurons hidden layers, and two outputs. Leveraging in-sensor processing of analog signals coming from photodetectors permits to reduce the amount of data to transmit and digitize, as well as eliminating the need of FPGAs for signal processing, allowing for an easier scale up of complex multichannel systems. Fabricated in a 0.35 μm CMOS process node, this first prototype chip demonstrates an energy efficiency of 46.8 GOP/J. Its functionality is showcased through the localization of X and Y coordinates of gamma photons interacting in a scintillator crystal readout by a planar array of silicon photomultipliers (SiPMs), in the field of medical imaging applications based on emission tomography (such as PET and SPECT). The neural network's weight reconfigurability broadens its applicability beyond gamma-ray detection, making it suitable for other edge-computing applications requiring a feedforward neural network architecture.

Keywords: Analog neural network · capacitive crossbar array · radiation detectors · in-memory computing

1 Introduction

Embedding signal processing into the front-end of detectors is a prominent solution for managing the rising volume of data and complexity of computations, which are the major bottlenecks in conventional digital systems based on von Neumann architecture. [1].

In this paper we present the realization of an ASIC called ANNA [2], that is an analog implementation of a neural network (NN) performing the multiply-and-accumulate (MAC) operations in charge domain through a programmable capacitive crossbar array. As shown in Fig. 1, this ASIC was designed targeting a specific application in nuclear medical imaging, that is the estimation of scintillation coordinates of gamma rays in a Gamma Camera used for emission

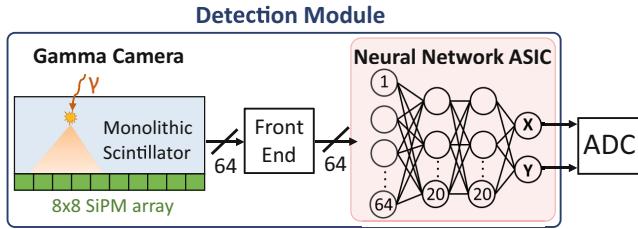


Fig. 1. The analog neural network ASIC is intended to be inserted in the detection module of a Gamma Camera for edge processing of the photodetectors output signals for positioning of the scintillation event.

tomography (PET and SPECT), taking as inputs the output signals from the photodetectors (in our case Silicon PhotoMultipliers, SiPMs), thus eliminating the need to digitize them and converting only the final outputs. However, the neural network's weight are reprogrammable, therefore its applicability could be extended in a large variety of sensing contexts where a feedforward neural network can be exploited for computations.

2 ASIC Concept and Implementation

2.1 Electrical Neuron Operation

Figure 2 shows the analogy between a neural network layer and its analog implementation as a crossbar array of programmable capacitors. The fundamental operations needed to perform a neural network inference are the MAC operations, which in the proposed circuit are executed in analog (charge) domain by simply exploiting charge-voltage capacitor law $Q = CV$ for multiplications and Kirchhoff's laws for summations.

The electrical neuron MAC operation is articulated in two consecutive phases. In the first phase, by closing switches S_1 and S_2 , the input voltage values on each row are sampled into capacitors with adjustable values $C_{i,j}$. Next, in the second phase in which switches S_3 and S_4 are closed and S_1 and S_2 are open, the weighted charges, resulting from multiplication of input voltages and capacitors, are added together vertically using charge integrator's virtual ground. If a negative weight has to be implemented, the weighting capacitor is flipped by closing switches S_2 and S_5 during integration phase, resulting in a subtraction of charges from the integrator. The integrator converts the total charge into the output voltage (neuron's output) through the feedback capacitor C_F , which will be the input of neurons in the following layer. The non-linear activation function is intrinsic in the integrator rectifying response, clipping the output voltage between the two power supplies. With N being the total number of inputs, the j^{th} integrator output is equal to $V_{out,j} = \sum_{i=1}^N V_{in,i}(C_{i,j}/C_F)$, which is a weighted sum of the inputs.

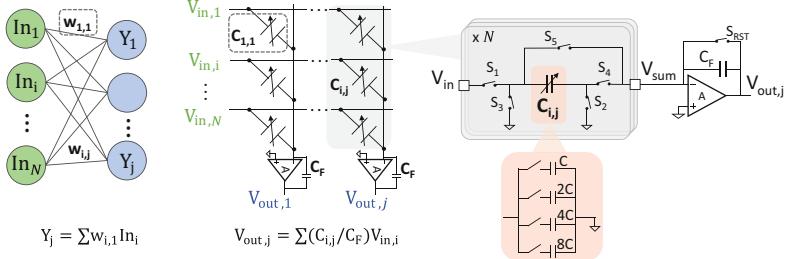


Fig. 2. A neural network layer and its analog implementation with a programmable capacitive crossbar array. A detailed schematic of a neuron with all its inputs connected and the implementation of weight as switched capacitors is shown on the right.

The weight is obtained with a bank of 15 capacitors scaled as power of 2, selectively connected in parallel by digitally-controlled switches. This allows to implement weights with a resolution of 4 bits, plus an additional bit for the sign, resulting in 5-bit precision weights.

To reduce charging energy, a technique based on redistribution of charge has been adopted. This requires the addition of two more phases during MAC computation. In this approach, the input voltage is sampled solely on the LSB capacitor C whose value is of 100 fF, thus reducing the energy by a factor of at maximum 15. Subsequently, by employing two intermediate phases, the stored charge is distributed among the $15C$ capacitors of the bank and, to obtain the desired weight, certain capacitors are disconnected prior to summation phase, and only the ones corresponding to the weight are connected to integrator's virtual ground.

2.2 Neural Network Architecture and Training

We have selected a NN with 64 input nodes, two hidden layers of 20 neurons each and two output neurons for inference of X and Y interaction coordinates. Training and test datasets were obtained from Monte Carlo simulations (ANTS2 [3]) of a PET detector based on a 51 mm × 51 mm × 10 mm LYSO scintillator read out by an 8 × 8 array of SiPMs.

The NN weights are defined offline through a Quantization Aware Training (QAT) approach done in Matlab, in which weights are discretized to 5 bits (4 + 1 for the sign) during learning phase, to minimize the effect of quantization error on NN performance. The impact of the discretization of weights was studied and the number of 5 bits resulted as an optimal compromise between achievable accuracy, neuron complexity and occupied silicon surface.

Before inference operations, weights are loaded to the chip by means of SPI communication and stored on local write-only SRAM cells. The neural network has 1762 weights, and 8.81 Kbit of SRAMs are required to implement them. Although the NN architecture is fixed, SRAM cells can be reprogrammed as needed, enabling the use of different sets of weights and making the on-chip NN

adaptable for different applications. To our knowledge, this is the first study to implement an analog neural network for position sensitivity purposes in the field of nuclear medical imaging.

2.3 Impact of Non-idealities

Parasitisms. We carefully identified the most critical circuit non-idealities (such as integrator offsets, parasitic capacitances, injected charges) and build an analytical model of the electrical neuron that includes them. The training was performed with this model to ensure good matching between software NN and on-chip NN predictions, and to make the network robust to the effect of circuital inaccuracies. To build the most accurate model possible, it was fitted over thousands of experimental measurements of the electrical neurons, obtained by measuring all 42 integrators output for different combinations of inputs and weights. The acquired data was used to estimate the model parameters representing the circuit non-idealities. The bestfitted parameters at which the model converged are all reasonable values and very close to the ones that could be derived from post-layout estimations. The model error, evaluated as the difference between model predictions of integrator outputs and measured outputs, is of $0.01 \text{ mV} \pm 222 \text{ mV}$, confirming the reliability of the model in resembling the ASIC behaviour.

Electronic Noise. The amount of noise at integrator output due to both kT/C noise of switches and integrator electronic noise was quantified from transient noise simulations, and introduced during software NN inference to study its effect on positioning performance. The propagation of the kT/C noise to the integrator output resulted equal to 3.077 mV_{rms} , considering the worst case with all capacitors and all 64 inputs connected. The contribution due to integrator electronics noise only resulted equal to 0.340 mV_{rms} . The combined contribution of these two noise sources, calculated as the square root of the sum of squares of the individual noise sources, is equal to 3.095 mV_{rms} . To study the impact of noise to the network positioning performance, we carried out Matlab simulations in which we performed several inferences of the neural network for the same input pattern, adding at each neuron a noise value taken from a Gaussian distribution with standard deviation of 5 mV, to emulate (with safety margins) the presence of noise at the integrators output. We then evaluated the performance of the network as the standard deviation of the predicted coordinates, which resulted equal to 0.11 mm (0.26 mm FWHM), however much smaller than the target spatial resolution of 1.5 mm FWHM for PET applications. These results allow us to consider negligible the effect of electronic noise to the network performance, emphasizing the ability to maintain performance even when small changes or noise are introduced in the data.

Capacitor Mismatch. The impact of binary-scaled capacitors mismatches on integrator output was simulated via a Monte Carlo simulation in Cadence,

involving one integrator and the 64 capacitor blocks connected to it (corresponding to a neuron of the first layer). This analysis reproduces the short-distance capacitor variation $\sigma(\Delta C/C)$ (which is $0.039\% \pm 0.003\%$ for a 100 fF capacitor as reported in the capacitor matching curves of the foundry documentation), producing a standard deviation at integrator output of only $58.3 \mu V_{rms}$. To estimate the long-distance variation along a column of the crossbar array, we performed measurements of an integrator of the first layer (whose connected 64 capacitor blocks are distributed along a 4.5-mm long column), in which only one capacitor bank $C_{i,j}$ at a time was active and charged with an input. Specifically, one weight out of 64 was set individually and swept from -1.5 pF to 1.5 pF with steps of 100 fF, and charged with an input voltage (the other 63 weights were set to 0 fF). This measurement was repeated for each capacitor block in the column. We were therefore able to measure the integrator output corresponding to the product between one input and one weight, for different weight values and different location along the column. All measured integrator outputs resulted to be practically equal for the same input/weight combinations, with a standard deviation of $4.2 mV_{rms}$, averaged among all tested weights and capacitor blocks. This value is comparable to the one obtained from transient noise simulations and, as demonstrated in the previous subsection, it was found to have a negligible impact to the performance of the neural network.

3 ANNA ASIC Experimental Characterization

3.1 Measurement Setup

The ASIC is fabricated in $0.35 \mu \text{m}$ CMOS process and occupies an area of 24 mm^2 . Figure 3 shows the measurement setup developed for the laboratory experimental characterization of the prototype ASIC. The printed circuit boards (PCBs) system comprises three interconnected boards: i) the Carrier Board, which accommodates the ASIC, allowing its communication with the outside world, ii) the Mother Board manages the power supply connections and serves as a platform for the other boards facilitating communication among the various system components, iii) the microcontroller board, hosting the STM32-L476RG microcontroller ([4]), for ASIC programming, inputs delivery and output data sampling. Neurons output can also be acquired with an oscilloscope. Besides X and Y coordinates, all internal neurons output can be measured thanks to an on-chip multiplexer and buffer, useful for debug purposes and integrators characterization and offset measurements. A custom graphical user interface (GUI) developed in Matlab manages and facilitates the communication among computer, microcontroller and ASIC, allowing to perform various types of measurements according to the settings chosen in the GUI panel.

3.2 Results

Experimental measurements of the on-chip neural network were carried out to test its prediction accuracy. To perform an inference, a given set of 64 analog

voltages is fed to the ASIC inputs, derived from simulated data of SiPM signals corresponding to an event with known position of interaction. The output voltages of the last two integrators, corresponding to the X and Y interaction coordinates are measured, and an example is reported in Fig. 4(a). The steady-state values of the waveforms are then converted in millimeters values within the range ± 25 mm for position reconstruction. The ASIC was tested on a grid of 121 simulated points uniformly distributed in a $50\text{ mm} \times 50\text{ mm}$ crystal surface. Figure 4(b) shows some of the points reconstructed along the diagonal. The bias, calculated as the displacement between position reconstructed by the ASIC network and the real event position, is averaged among all 121 tested points and resulted equal to 3.9 mm. The mean bias is of 2.8 mm when points distributed along the edge of the crystal are not considered, since estimating the interaction position for gamma rays at the edge is typically more challenging due to truncation and reflections of the scintillation light distribution (*edge effect*, [5]). The bias error of the software (Matlab) NN, on the same 121 test points, is of 2.3 mm. The residual error between model and chip NN can be attributed to electronic circuit non-idealities that are difficult to represent analytically and therefore deteriorates the expected performance.

We also tested the precision of the ASIC network. To do this, the same input has been delivered to the ASIC 100 times, and in Fig. 5 are shown the reconstructed 2D points (left) and their distribution along X directions (right). The measured standard deviations are of 4.4 mV and 4.1 mV for the X and Y coordinates, respectively, which converted in millimeters correspond to 0.074 mm and 0.067 mm, resulting in a 2D FWHM of 0.166 mm, i.e. about 10% if we consider a target spatial resolution better than 1.5 mm FWHM for PET applications. The average 2D FWHM considering all 121 tested points is of 0.175 mm.

The measured average power consumption needed for an inference amounted to $\sim 16.8\text{ mW}$, corresponding to an energy consumption of 76 nJ, at the maximum operating frequency of 10 MHz. The energy efficiency is of 46.8 GOP/J (giga operations per Joule). From post-layout simulations, we were able to estimate the energy consumption of individual circuit components involved during

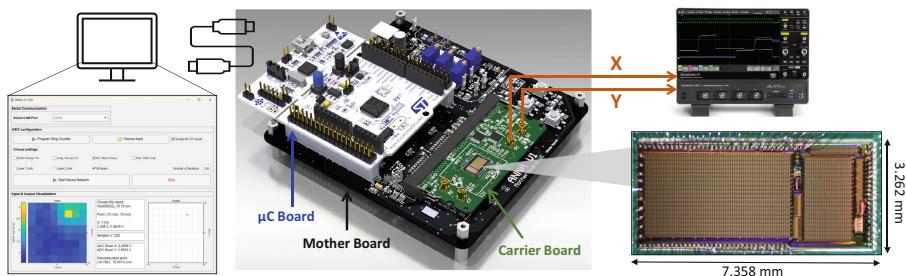


Fig. 3. Setup for ANNA ASIC experimental characterization.

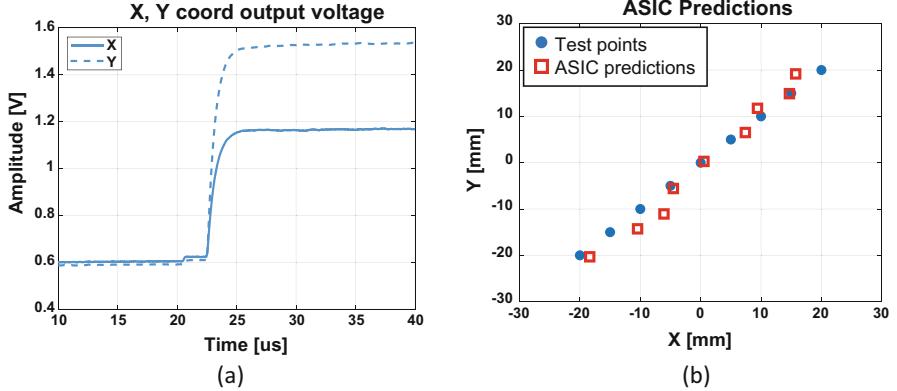


Fig. 4. (a) Example of the two measured output voltages representing the X, Y predicted coordinates. The steady-state values of these waveform are converted in millimeters values within the range ± 25 mm. (b) ASIC predictions of some test points lying along the diagonal of the crystal surface.

NN inference. The dominant contributions are three and given by: 1) ring counters, which are the shift registers used to synchronize all switching activities; 2) switches of the capacitor banks, driven by long, tightly packed digital nets (there are 1762 capacitor banks for a total of 17,620 switches); 3) integrators, that are however powered on only when needed for energy saving. These components represent a bottleneck in terms of power consumption, and will be carefully addressed and improved in the future version of the ASIC.

The main features and performance of the presented ASIC are summarized in Table 1, reporting also a comparison with a few single-chip digital and analog accelerators.

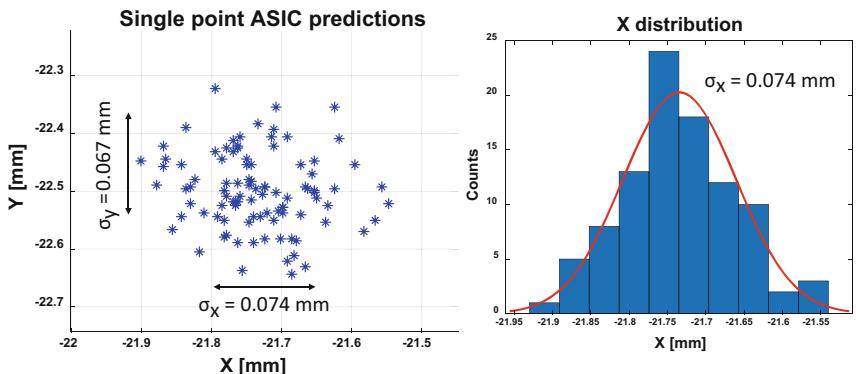


Fig. 5. Standard deviation of the measured X and Y coordinates of a single point, obtained from 100 inferences of the same input.

Table 1. Performance comparison with digital and analog accelerators.

	Eyeriss [6]	EIE [7]	Nat. El. 2019 [8]	This Work
Technology	65 nm	45 nm	180 nm	350 nm
Digital/Analog	Digital	Digital	Analog (Resistive)	Analog (Capacitive)
Area [mm ²]	16	63.8	61.4	24
Input/Weight Precision	16/16-bit	4/4-bit	4/6-bit	Analog/5-bit
Power [W]	0.278	0.590	0.306	0.017
Throughput [GOP/s]	23.1	102	57.5	0.792
Energy Efficiency [GOP/J]	83.1	172.8	187	46.8

4 Discussion and Conclusions

The presented ASIC is a first proof-of-concept prototype of an analog neural network integrated circuit and this gives reason to the choice of a conservative technology ($0.35\text{ }\mu\text{m}$ CMOS), beyond the fact that it is compatible with available analog front-end circuits and has a lower cost compared to more recent and more scaled processes. The LSB capacitance C is chosen of 100 fF, and the total capacitance of each capacitor bank is of 1.5 pF. All capacitors are realised with a polysilicon-insulator-polysilicon process, designed with interconnected squared LSB capacitors and laid out with a common centroid method to reduce mismatches. We are aware that 100 fF is not the smallest available capacitance for this technology, but we decided to opt for this value since it resulted the best compromise among occupied area, energy required to charge the capacitors, capacitor mismatch and effect of kT/C noise. This first prototype has the aim to demonstrate the feasibility of the analog implementation of a feedforward neural network where weights and computations are performed by crossbar arrays of switched capacitors. The network is intended to be used for gamma event positioning, without the need for photodetectors signal ADC conversion.

The ASIC network performance are promising: even though the accuracy is still not good enough for the target application, the achievable precision (spatial resolution) of 0.175 mm FWHM is satisfying to meet the requirements of PET imaging. These results are encouraging and there is still room for improvements by addressing all issues encountered in this first prototype.

Transitioning to a more scaled technology is envisaged to enhance energy efficiency, since this will allow to build a larger network (increasing the number of parallel MAC operations, thus the throughput), to reduce latency and decrease power dissipation through a reduction in LSB capacitance value and power supply voltage scaling. A revision of the crossbar array with the scope of handling all the limitations and criticalities found in the presented prototype is foreseen for a new version of the ASIC. However, these inaccuracies are systematic and can be included in the model during training, making the neural network robust to small variations in data and helping it to learn general features and patterns.

References

1. Mannocci, P., et al.: In-memory computing with emerging memory devices: status and outlook. *APL Mach. Learn.* **1**(1) (2023)
2. Di Giacomo, S., et al.: Implementing an integrated neural network for real-time position reconstruction in emission tomography with monolithic scintillators. *IEEE Trans. Rad. Plasma Med. Sci.* (2024)
3. Morozov, A., et al.: ANTS2 package: simulation and experimental data processing for Anger camera type detectors. *J. Inst.* **11**(04), P04022 (2016)
4. STMicroelectronics. <https://www.st.com/en/evaluation-tools/nucleo-l476rg.html#overview>
5. Decuyper, M., et al.: Artificial neural networks for positioning of gamma interactions in monolithic PET detectors. *Phys. Med. Biol.* **66**(7), 075001 (2021)
6. Chen, Y., et al.: Eyeriss: an energy-efficient reconfigurable accelerator for deep convolutional neural networks. *IEEE J. Solid-State Circ.* **52**(1), 127–138 (2016)
7. Han, S., et al.: EIE: efficient inference engine on compressed deep neural network. *ACM SIGARCH Comp. Arch. News* **44**(3), 243–254 (2016)
8. Cai, F., et al.: A fully integrated reprogrammable memristor-CMOS system for efficient multiply-accumulate operations. *Nat. Electron.* **2**(7), 290–299 (2019)



A High-Voltage LDO Voltage Regulator Featuring Enhanced Transient Response and Reduced Area

Jacopo Serra^(✉) and Franco Fiori

Politecnico di Torino, Torino, Italy

{jacopo.serra,franco.fiori}@polito.it

Abstract. This paper introduces a high-voltage output-capacitorless voltage regulator designed for fast transient response to supply switching loads digital blocks directly from the high-voltage power rail. The proposed solution based on the current buffer Miller compensation, achieves a load current transient response of about 1.6ns and reduces silicon area by a factor of 2.25 compared to a high-voltage Flipped Voltage Follower-based topology.

Keywords: Analog ICs · OCL-LDO voltage regulator · FVF · advanced frequency compensation

1 Introduction

Low dropout (LDOs) voltage regulators are extensively used in the Power Management Integrated Circuits (PMICs) of System-on-Chips (SoCs) to supply the building blocks with a clean, stable and accurate voltage [1].

In a conventional LDO, such as the one shown in Fig. 1a, the slow-loop comprising the Error Amplifier (EA), the output transistor (MP) and the resistive voltage divider provides the regulated output voltage starting from a reference voltage (V_{REF}). An off-chip capacitor (C_{L-off}), in the μF range, is used both to stabilize the voltage regulator and to reduce the output voltage ripple due to fast load current variations. Such a capacitor increases the number of pins and introduces stray inductances (L_p) that worsen the load transient response at the point-of-load. Aiming to eliminate the off-chip components, output-capacitorless LDOs (OCL-LDOs) have been developed in the last decades [2].

Referring to the OCL-LDO in Fig. 1b, the on-chip capacitor (C_L) is several orders of magnitude smaller than (C_{L-off}). Therefore, its transient performance mainly relies on the capability of the voltage regulator to sense the output voltage variation and quickly adjust the source-gate voltage of the transistor MP [3]. Usually, the unit gain frequency of such voltage regulators is extended using sophisticated compensation networks [4,7], which introduce fast-loops featuring larger bandwidth [5], and/or implementing undershoot/overshoot detection circuits that drive the output transistor quickly [6].

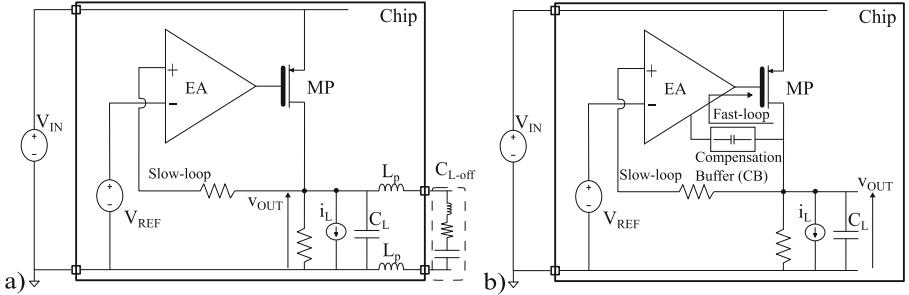


Fig. 1. a) Conventional LDO voltage regulator with off-chip load capacitor and parasitics. b) Output-capacitorless LDO with fast-loop to enhance the transient performance.

The aforementioned architectures focus on minimizing the load capacitance while providing fast response time under low power budget. However, to the authors' knowledge, none of the fast transient solutions available in the open literature can handle input-voltage larger than a few Volts. Indeed, a high input-voltage LDO would allow for a further reduction in the number of pins by powering both the low-voltage digital core and the output-power stage of the SoC with the same supply voltage.

Wanting to fill this gap, a high-voltage OCL-LDO voltage regulator that exploits the current buffer Miller compensation (CBMC) approach featuring transient performance comparable to that of low-voltage OCL-LDO regulators and reduced silicon area is proposed.

The paper is organized as follow. Section 2 presents the pros and cons of high-voltage swing OCL-LDOs for the test case of a Flipped Voltage Follower OCL-LDO and analyses the proposed architecture. Simulation results are provided in Sect. 3 and concluding remarks are drawn in Sect. 4.

2 Circuit Implementation

As highlighted in the introduction, OCL-LDO voltage regulators allow one to save silicon area while preserving excellent transient performance. To achieve this result, OCL-LDOs are typically implemented as multi-loop systems in which a slow-loop ensures the accurate DC regulation, while the fast-loop immediately drives the power device in case of load current variations. Common implementations include the Flipped Voltage Follower(FVF) topology or Advanced Miller compensation-based architectures. In this Section, we first review a reference FVF-based solution, highlighting the critical issues in designing a fast transient high-voltage regulators based on this topology. Then, the proposed current buffer Miller compensated OCL-LDO is presented and compared with the reference one in terms of silicon area reduction.

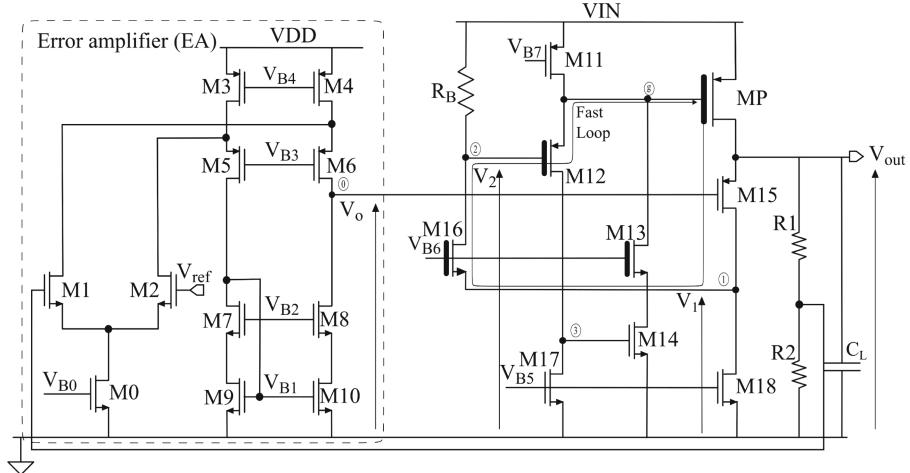


Fig. 2. Schematic of the OCL-LDO based on the cascaded Flipped Voltage Follower topology with Super Source Follower buffer derived by [6]. High-voltage device highlighted with thicker gate line.

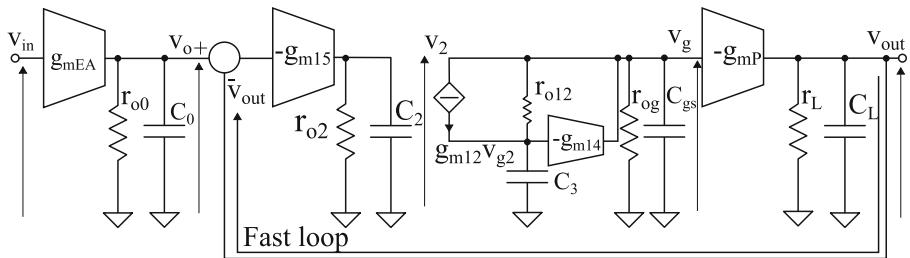


Fig. 3. Small-signal equivalent circuit for the OCL-LDO in Fig. 2.

2.1 High-Voltage FVF-Based Voltage Regulator

The FVF is a widely adopted low-voltage architecture for the realization of OCL-LDOs voltage regulators. A high-voltage variant of the topology proposed in [6], shown in Fig. 2, is used as reference architecture for the following analyses. In this solution, the fast-loop consists of: (1) a FVF (M₁₅-M₁₆) with folded cascode stage to sense the output voltage and (2) a Super Source Follower (SSF) buffer (M₁₂-M₁₄) to quickly discharge the input capacitance of the transistor MP. Indeed, since the transient performance of an OCL-LDO relies on the fast-loop bandwidth, the SSF low output impedance allows to move toward high frequencies the non dominant pole associated with MP.

The small-signal model for the circuit of Fig. 2 is shown in Fig. 3. g_{mEA} represents the transconductance of the error amplifier, g_{mP} the transconductance of the power transistor, while r_{oi} and C_i are the lumped resistance and capacitance

at the i -th node. The open-loop transfer function of the fast-loop is

$$T = \frac{v_{\text{out}}}{v_{\text{out}} - v_o} \approx \frac{v_2}{v_{\text{out}} - v_o} \frac{v_g}{v_2} \frac{v_{\text{out}}}{v_g}, \quad (1)$$

where Eqs. (2), (3) and (4) are the transfer functions of the cascoded FVF, the SSF and the power transistor.

$$\frac{v_2}{v_{\text{out}} - v_o} \approx \frac{g_{m15} r_{o2}}{1 + s r_{o2} C_2} \approx \frac{g_{m15} R_B}{1 + s R_B C_2} \quad (2)$$

$$\frac{v_g}{v_2} \approx \frac{1}{s^2 \frac{C_{gs} C_3}{g_{m12} g_{m14}} + s \frac{C_{gs} + g_{m12} r_{o12} C_3}{r_{o12} g_{m12} g_{m14}} + 1} \quad (3)$$

$$\frac{v_{\text{out}}}{v_g} = -\frac{g_{mp} r_L}{1 + s r_L C_L} \quad (4)$$

The phase margin is given by

$$\phi_m \approx 90^\circ - \tan^{-1} \left(\frac{UGF}{Q \omega_o [1 - (UGF/\omega_o)^2]} \right) \quad (5)$$

where ω_o is the characteristic frequency of the SSF complex poles, Q is their quality factor and UGF represents the loop unity-gain frequency. Wanting to keep a phase margin above 60° one can choose $\omega_o \approx 2UGF$ and $Q \approx \sqrt{2}$. Furthermore, assuming that (1) models a dominant pole system, the load capacitor should be:

$$C_L \geq 2g_{mp} g_{m15} R_B \sqrt{\frac{C_{gs} C_3}{g_{m12} g_{m14}}}. \quad (6)$$

Equation highlights the tradeoff between area and power consumption in the FVF-based solution, in which the requirement for quiescent current sets a lower bound on R_B , thereby limiting the on-chip capacitance reduction.

3 Proposed High-Voltage CBMC Voltage Regulator

The proposed solution is shown in Fig. 4. It is based on a conventional LDO voltage regulator comprising of an high-voltage output transistor (MP) feeding the load. The output is loaded by the capacitor C_L , i.e. the load capacitance or an additional one placed intentionally to make the circuit stable. The slow-frequency regulation loop is composed of the resistive voltage divider (R_1, R_2) and the error amplifier (EA) which in turn drives the gain stage comprising of the transistors M1-M5. The Compensation buffer (CB), implemented by the transistors M9-M11 and the compensation capacitor C_m , sets a low impedance path for the high-frequency components making the voltage regulator stable, thus enhancing its transient performance. Besides the output transistor (MP) only two high-voltage transistors are needed, M4 and M7 respectively. All the others, including the compensation capacitor, are low voltage components, therefore they are much

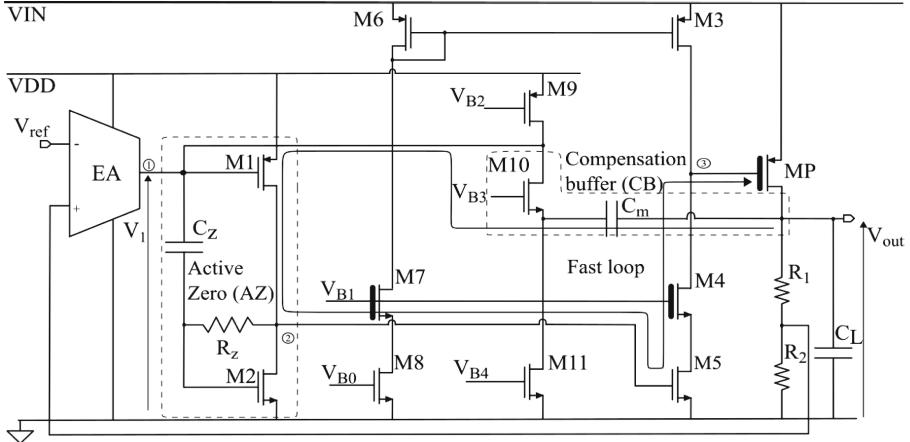


Fig. 4. Schematic view of the CBMC OCL-LDO comprising high-voltage devices.

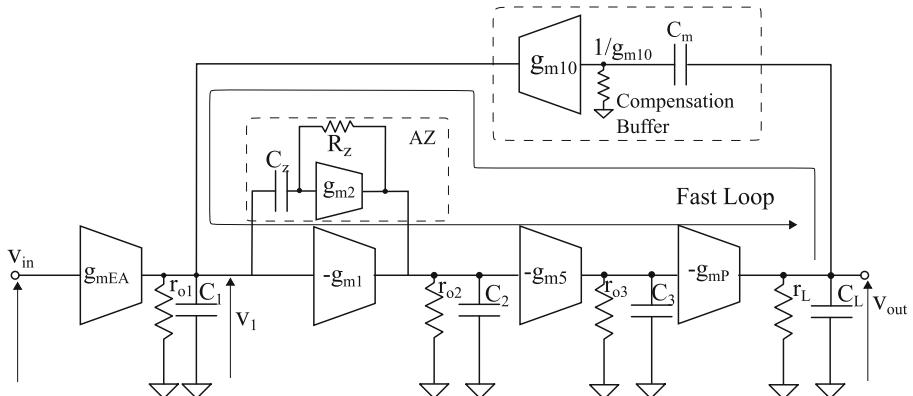


Fig. 5. Small-signal equivalent circuit for the CBMC OCL-LDO.

faster, and they need much less silicon area than their high-voltage counterpart. Furthermore, it should be noted that the EA, a part of the circuit used to drive MP and the compensation circuit are supplied through a low voltage rail (V_{DD}), which takes energy from a pre-regulator (not shown in Fig. 4).

Figure 5 shows the small-signal equivalent of the circuit in Fig. 4, r_{oi} and C_i represent the lumped resistance and the parasitic capacitance at the i-th node. The open loop transfer function of the proposed solution can be written as

$$T = \frac{v_{out}}{v_{in}} \approx A_\infty \frac{\left(\frac{C_m/C_1}{1+s(C_m/g_{m10})} \right) H}{\left(\frac{C_m/C_1}{1+s(C_m/g_{m10})} \right) H + 1}, \quad (7)$$

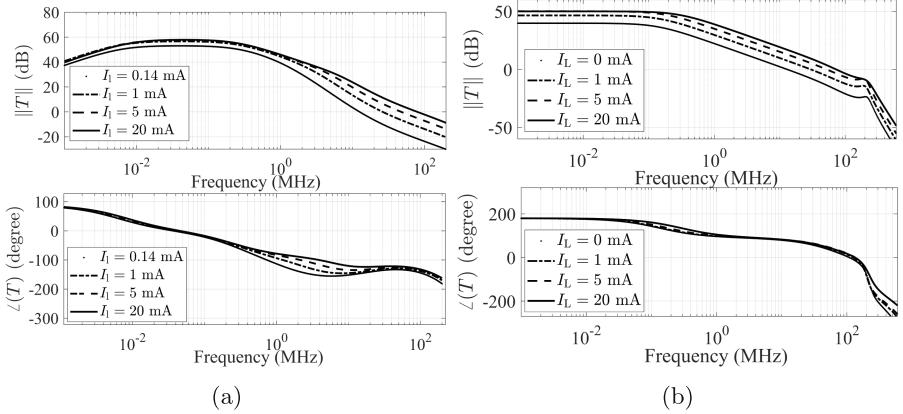


Fig. 6. Simulated open-loop transfer function for the fast-loop (a) CBMC with $C_L = 80 \text{ pF}$ and (b) FVF with $C_L = 180 \text{ pF}$. Load current ranging from I_L^{\min} to 20 mA.

where A_∞ is the ideal closed-loop gain (8), H is the transfer function v_{out}/v_1 (9) and C_1 is the parasitic capacitance seen from the EA output node.

$$A_\infty = \frac{g_{\text{mEA}}}{1/g_{\text{m}10} + 1/sC_{\text{m}}} \quad (8)$$

$$H = \frac{v_{\text{out}}}{v_1} \approx -\frac{g_{\text{m}1}g_{\text{m}5}g_{\text{mP}}r_{\text{o}3}r_{\text{L}}}{g_{\text{m}2}} \frac{1 + s \frac{(g_{\text{m}1} + g_{\text{m}2})R_{\text{Z}}C_{\text{z}}}{g_{\text{m}1}}}{s^2 \frac{R_{\text{Z}}C_{\text{z}}C_2}{g_{\text{m}2}} + s \frac{C_{\text{z}}}{g_{\text{m}2}} + 1} \frac{1}{1 + sr_{\text{o}3}C_3} \frac{1}{1 + sr_{\text{L}}C_{\text{L}}} \quad (9)$$

Provided that the pole introduced by the Compensation Buffer at $g_{\text{m}10}/C_{\text{m}}$ lies at a much higher frequency than the UGF, the CBMC boosts the fast loop UGF by a factor of C_{m}/C_1 w.r.t the standard Miller compensation. Moreover, to ensure the voltage regulator stability in all load conditions, an Active Zero (AZ) circuit was introduced to partially compensate the output pole at $1/(r_{\text{L}}C_{\text{L}})$ thereby boosting the phase around the UGF [5].

As highlighted in [3], improving the loop bandwidth enhances the transient performance of the voltage regulator by reducing the response time (t_r). Ensuring the stability of the voltage regulator, a reduction in t_r , for a given current step and a specified ΔV_{out} requirement allows for a reduction of C_{L} . Given that the capacitance C_{L} represents a significant fraction of the silicon area, the result of an advanced compensation is a substantial reduction of the silicon area.

4 Simulation Results

The proposed high-voltage OCL-LDO was designed and simulated, referring to a $0.35 \mu\text{m}$ High Voltage (HV) CMOS technology [10], to meet the specifications listed in Table 1. In the design, the fast-loop bandwidth and the output capacitance (C_{L}) were optimized to limit the output voltage droop to 330 mV (10%

Table 1. Specification designed OCL-LDOs

Parameter	Value	Parameter	Value
V_{IN}^{MAX}	24V	V_{do}	1V
V_{OUT}	3.3V	I_L^{max}	20 mA
V_{DD}	3.3V	Tech.	0.35 μ m

of V_{out}). To compare the CBMC OCL-LDO with a reference architecture, the FVF-based voltage regulator in Fig. 2 was also designed to meet the same design specifications.

Figure 6a shows the magnitude and phase of the fast-loop gain for the proposed LDO, achieving a UGF of 81 MHz with a corresponding phase margin of 52.5°. Furthermore, it should be noted that the maximum bandwidth and phase margin occur at the maximum load current I_L^{max} . This ensures the shortest response time without oscillations in the worst case scenario of a load current variation from I_L^{min} to I_L^{max} . Analyzing the results of the FVF-based solution (Fig. 6b), at the maximum load current, the fast-loop achieves a UGF of 70.3 MHz and a phase margin of 35°. In accordance with the Eq. (5), the worst-case phase margin occurs at the maximum load current, potentially leading to oscillations during the response time. Despite both architectures showing comparable bandwidth, the CBMC solution requires a load capacitance (C_L) of merely 80 pF compared to $C_L = 180$ pF for the FVF, resulting in an estimated silicon area reduction by a factor of 2.25.

Such a high bandwidth enhances the transient performance of the regulators as shown in Fig. 7. Indeed, for a load current step ranging from 0.14 mA to 20 mA, the output voltage droop remains below 10% of V_{out} for both the CBMC and the FVF LDO. In previous works [4,5], when the response time approaches the edge time, t_r is estimated as in (10), where ΔV_{out} is the voltage droop at t_r . Substituting the results of Fig. 7 in (10) the FVF-based LDO has $t_r = 2.4$ ns while the proposed CBMC OCL-LDO presents $t_r = 1.6$ ns.

$$t_r = \sqrt{\frac{2C_L \Delta V_{out} T_{edge}}{\Delta I_L}} \quad (10)$$

Therefore, while both topologies have comparable performance in terms of frequency behavior and response time, the CBMC-based architecture outperforms the conventional FVF-based architecture in reducing the load capacitance. Additionally, the CBMC OCL-LDO shows a response time lower than that of the most recent high-voltage LDOs [8,9] comparable to the of state-of-the-art low-voltage OCL-LDOs [4,5].

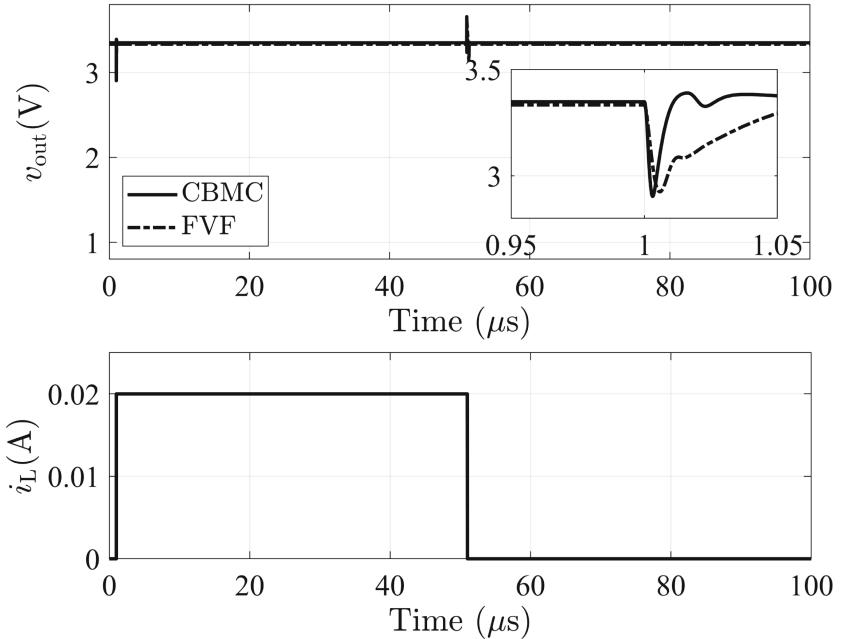


Fig. 7. Simulated load transient response, load current ranging from 0.14 mA and 20 mA, with $T_{\text{edge}} = 1\text{ns}$, $V_{\text{IN}} = 9\text{V}$ and $V_{\text{IN}} = 3.3\text{V}$.

5 Conclusion

In this paper, an OCL-LDO designed for load current fast transient response and suitable for high-voltage applications has been presented. It exploits the current buffer Miller compensation scheme, which make possible the design of the fast feedback loop using a low-voltage CMOS technology. The CBMC OCL-LDO was designed and its features compared with those of a FVF-based reference architecture. The investigation highlighted that the silicon area occupied by the proposed voltage regulator is 2.25 times smaller than that needed by the FVF-based topology.

References

1. Guo, J., Leung, K.N.: A 6- μW chip-area-efficient output-capacitorless LDO in 90-nm CMOS technology. *IEEE J. Solid-State Circ.* **45**(9), 1896–1905 (2010)
2. Chyan, T.Y., et al.: Evaluation and perspective of analog low-dropout voltage regulators: a review. *IEEE Access* **10**, 114469–114489 (2022)
3. Rincon-Mora, G.A., Allen, P.E.: A low-voltage, low quiescent current, low drop-out regulator. *IEEE J. Solid-State Circ.* **33**(1), 36–44 (1998)
4. Bu, S., Guo, J., Leung, K.N.: A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth $\gtrsim 100$ MHz in 130-nm CMOS. *IEEE Trans. Power Electron.* **33**(4), 3232–3246 (2018)

5. Bu, S., Leung, K.N., Lu, Y., Guo, J., Zheng, Y.: A fully integrated low-dropout regulator with differentiator-based active zero compensation. *IEEE Trans. Circ. Syst. I* **65**(10), 3578–3591 (2018)
6. Liu, N., Johnson, B., Nadig, V., Chen, D.: A transient-enhanced fully-integrated LDO regulator for SoC application. In: 2018 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1–5. IEEE, Florence (2018)
7. Liu, N., Chen, D.: A transient-enhanced output-capacitorless LDO with fast local loop and overshoot detection. *IEEE Trans. Circ. Syst. I* **67**(10), 3422–3432 (2020)
8. Maity, A., Patra, A.: A single-stage low-dropout regulator with a wide dynamic range for generic applications. *IEEE Trans. VLSI Syst.* **24**, 1–11 (2015)
9. Wei, X., Liu, W., Zhang, Z., Yu, Z.: A wide input voltage range LDO with fast transient response. In: 2023 6th International Conference on Electronics Technology (ICET), pp. 114–119. IEEE, Chengdu (2023)
10. AMS 0.35 um HV-CMOS 50 V. <https://ams-osram.com/technology/full-service-foundry/technology-portfolio>



A Low-Cost Fault Tolerance Technique for Microcontroller-Class RISC-V Processors

Riccardo Tedeschi¹✉, Alessandro Nadalini¹, Filippo Grillotti³,
Fabio De Ambroggi³, Elio Guidetti³, Luca Benini^{1,2}, and Davide Rossi¹

¹ DEI, University of Bologna, Bologna, Italy

{riccardo.tedeschi6,alessandro.nadalini3,davide.rossi}@unibo.it

² IIS Lab, ETH Zurich, Zürich, Switzerland

lbenini@iis.ee.ethz.ch

³ STMicroelectronics, Milan, Italy

{filippo.grillotti,fabio.deambroggi,elio.guidetti}@st.com

Abstract. Reliable Cyber-Physical Systems (CPSs) must ensure their functionality according to the criticality level of their application, even under Single Event Transients (SETs) and Single Event Upsets (SEUs) caused by ionizing radiations. Dual (DCLS) and Triple Core Lock-step (TCLS) are typical radiation-hardening techniques for processors based on spatial redundancy. However, these approaches can be costly when embedding computing platforms into dependable systems with constrained area and budget requirements. We propose a low-cost fault mitigation technique targeted at SETs called Temporal Lockstep (TL), which combines temporal redundancy and minimal spatial repetition to reduce the area overhead with respect to state-of-the-art solutions. TL was implemented on the open-source Ibex core and synthesized in GF 22 nm technology. The area overhead ranges from 53% to 77%, significantly lower than the over 100% and 200% seen in DCLS and TCLS, respectively. Fault injection simulations show an 82.8% reduction in faulty execution outcomes thanks to Temporal Lockstep.

Keywords: Fault Tolerance · Fault Mitigation · RISC-V · Temporal Lockstep

1 Introduction

Cyber-physical systems (CPSs) encompass the range of applications where computation and physical processes are deeply integrated to obtain a physically aware computational system. CPSs must be able to perform real-time sensing, processing, communication, and actuation reliably even in harsh environments and with limited resources due to the embedded nature of these platforms [5].

Radiation-induced faults are one of the primary vulnerabilities in modern integrated circuits, especially in the case of Single Event Effects (SEEs) [4].

© The Author(s), under exclusive license to Springer Nature Switzerland AG 2025
M. Valle et al. (Eds.): SIE 2024, LNEE 1263, pp. 21–28, 2025.

https://doi.org/10.1007/978-3-031-71518-1_3

While these phenomena were originally a concern only for aerospace applications, Single Event Transients (SETs) and Single Event Upsets (SEUs) are becoming increasingly relevant at the ground level, such as in the automotive field, due to the scaling of technology [16]. The components that perform the processing and decision-making in CPSs must be designed to withstand these faults reliably, using multiple Radiation-Hardening (RH) techniques targeted at different layers of abstraction during the design flow [11]. In processor design, Dual-Core Lockstep (DCLS) and Triple-Core Lockstep (TCLS) techniques are typically used to achieve significant fault tolerance through Modular Redundancy (MR), accepting increased area and power consumption as a trade off [18].

When speed is not the primary goal, Temporal Redundancy (TR) and hardware reuse can be leveraged as an alternative to curtail spacial redundancy cost, which is a significant concern in many applications. We propose Temporal Lockstep (TL), a fault mitigation technique oriented to low area overhead, which exploits hardware-level instruction duplication to protect the data path of the core by repeating successive instructions, while spatial redundancy is limited to the combinational part of the vulnerable portions of the control path. The area overhead obtained is limited between 53% and 77%, as opposed to more than 100% and 200% for DCLS and TCLS, respectively. This area reduction is obtained as a tradeoff with increased energy consumption. Fault injection simulations show an 82.8% reduction in faulty execution outcomes thanks to Temporal Lockstep.

2 Related Work

In a microprocessor, it is essential to protect both memory storage and the control and data paths [11]. Related works employing different hardening techniques are summarized in Table 1.

Triple-Core Lockstep (TCLS) and Dual-Core (DCLS) leverage Modular Redundancy (MR) since they respectively replicate the whole core two or three times to run the same task concurrently and to compare the outputs on a cycle-per-cycle base [18]. TCLS is capable of error correction due to its majority vote mechanism, while DCLS is limited to error detection, and restoring the execution is usually done by rolling back to a previous checkpoint. TCLS and DCLS trade off significant area overhead with fault tolerance both for sequential and combinational elements. However, the performance is not penalized during regular execution since it happens in parallel due to spatial replication. When errors occur, the performance penalty is limited to the recovery mechanism, requiring the cores to be reset or rolled back to a previous checkpoint (DCLS) or rolled forward by loading the correct majority-voted state (TCLS). In addition, these techniques can be easily applied to Commercial-Off-The-Shelf (COTS) components. In [8], three COTS Cortex-R5 cores with minimal additional modifications are grouped and wrapped inside a rad-hard TCLS assist unit, which orchestrates the spatially redundant execution and contains voters, error detection, and synchronization logic. CEVERO [15] employs two RISC-V Ibex cores configured

Table 1. Comparison of related works in term of ISA, hardening techniques, and overhead

Work	ISA	RH technique	Overhead	
			Area	Perf.
ARM TCLS	ARM	TCLS	High	Low
CEVERO	RISC-V	DCLS	Medium	Low
Kasap et al.	ARM, MicroBlaze	Hybrid DCLS/TCLS	High	Low
ARM DCLS	ARM	DCLS	Medium	Low
Rogenmoser et al.	RISC-V	Hybrid MR	Low ¹	Configurable
SHAKTI-F	RISC-V	ECC, DMR, TR	Low	High
DuckCore	RISC-V	ECC	Low	Low
Hardisc	RISC-V	DMR/TMR, ECC	Medium	Low
Klessydra-ft03	RISC-V	Buffered TMR (TR)	Medium ²	High
Temporal Lockstep	RISC-V	Instr. duplication (TR), TMR	Low	High

¹ Compared to the unmodified cluster of cores

² Overhead in an FPGA implementation over the single-threaded version

for DCLS and an additional module that contains the comparison logic and a copy of the Register File and the Program Counter, which are updated every time an instruction results in a successful match between the outputs of the two cores. This backup is used to roll back the cores in case of a mismatch. In [9], a hybrid DCLS/TCLS approach is proposed leveraging the All-Programmable System-on-Chip (APSoC) Xilinx Zynq-7000 by combining two ARM Cortex-A9 processor with a soft MicroBlaze core implemented in the programmable logic.

Multi-core processors and clustered cores open the possibility of configurable DCLS and TCLS by grouping the available cores in a lockstep execution at runtime to mitigate the area overhead by trading off performance for robustness only on safety-critical applications. The ARM Cortex-R embedded processors [7] implements this concept: while on normal operations, the two available cores can be used independently, in safety-critical tasks, they can be coupled by sharing the same Tightly Coupled Memories, caches, and peripheral ports. In [14], a cluster of cores is dynamically grouped or ungrouped to prioritize reliability through lockstepping or performance via parallelization.

To avoid full core replication, pipeline-level protection techniques can be used to selectively protect only a subset of vulnerable elements with different strategies. Information redundancy is commonly utilized by encoding stored bits with Error Correcting Codes (ECC) to enhance the resilience of sequential elements. This approach incurs additional costs due to the need for increased storage elements and additional encoding and decoding blocks [17]. Dual (DMR) or Triple (TMR) Modular Redundancy is employed to safeguard both sequential and combinational logic through complete replication of functional blocks at various levels to achieve spatial redundancy [11]. SHAKTI-F [6] uses ECC-protected pipeline registers and a DMR scheme for the ALU. Moreover, Temporal Redundancy is featured since any mismatch in the ALU operations results in

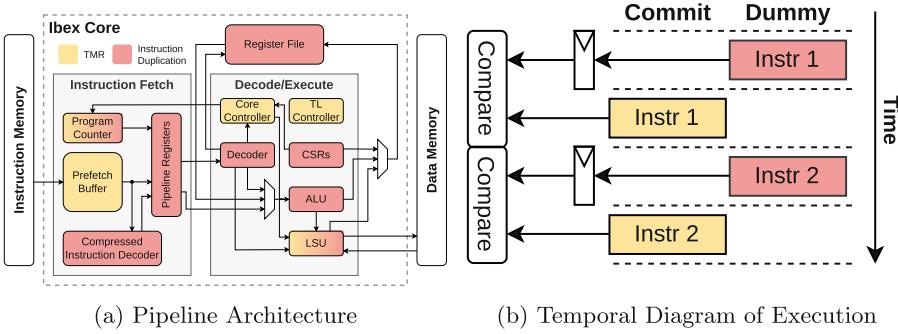


Fig. 1. Temporal Lockstep Methodology

its re-computation. Similarly, DuckCore [10] uses ECC-protected pipeline registers and instruction rollback after a mismatch is detected. Hardisc [13] proposes an in-pipeline protection scheme leveraging selective DMR and TMR of the different stages based on the observation that fault detection is sufficient until the core issues a data request, while fault masking is needed subsequently to ensure the safe completion of the initiated transaction. In addition, the RF is ECC-protected, and the integrity of the CSRs is ensured through TMR.

When speed is not the primary goal, temporal redundancy, and hardware reuse can be leveraged as an alternative to reduce area consumption further. Klessydra-ft03 [1] is based on an Interleaved Multi-Threading (IMT) core, where three threads are available by triplicating state-holding elements (PC, RF, and CSRs) to accommodate the thread states and the combinational logic is time-multiplexed. Thus, redundancy is achieved using the three available threads to execute the same program and inserting majority voting after the triplicated elements. Temporal Lockstep tries to minimize the area overhead by exploiting instruction duplication to protect the data path, limiting TMR only to the control portions otherwise not covered by temporal redundancy. No prior assumption about the underlying architecture is needed, unlike the Klessydra-ft03, which targets an IMT processor.

3 Methodology

The open-source RISC-V microcontroller core Ibex [3] was used as a testbed for the proposed technique. The vulnerable elements that constitute the internal state of the core are the Register File (RF), the Control and Status Registers (CSRs), and the Program Counter (PC). Figure 1b illustrates the execution scheme in Temporal Lockstep. Instructions are replicated and divided into “dummy” and “commit” flows within the hardware without the compiler’s knowledge. An instruction can safely modify the core status or the main memory only when two consecutive executions match; otherwise, the system inhibits any write operation, flushes the pipeline, and retries the faulty instruction. Moreover, instruction duplication can be toggled via software to reduce the execution

time overhead by protecting only critical portions of the code. Instruction repetition enhances the data path's ability to detect and recover transient faults in combinational logic of the datapath. This prevents errors from corrupting the core's state, minimizing the occurrence of Single Event Upsets (SEUs). It requires minimal additional logic, namely sequential components for storing temporary results and checkers for comparing repeated instruction outcomes. Where needed, the protection against random bit flips happening directly into storage elements must be addressed with orthogonal techniques, such as circuit-level redundancy or ECC-protected sequential components.

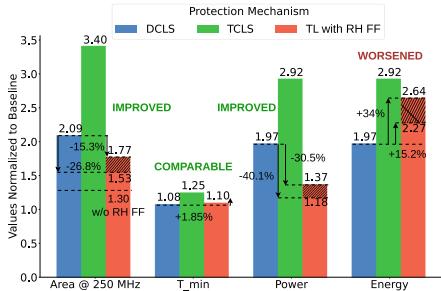
Triple Modular Redundancy (TMR) is exclusively applied to protect the vulnerable control combinational logic in the main core controller and those in the prefetch buffer, the Load Store Unit (LSU), and the controller managing TL since their state is generally modified independently from the execution of the current instruction. As an example, the main controller Finite State Machine (FSM) updates its internal state each cycle and handles events that happen concurrently with the normal execution flow, such as external interrupts or debug requests.

The core's overall pipeline structure is illustrated in Fig. 1a, indicating each module's protection mechanism. Yellow blocks are protected through TMR, red blocks are protected by instruction duplication, and mixed-color blocks take advantage of both techniques. Namely, the LSU controller is protected via TMR, and repeated memory operations cover the remaining logic. The sequential PC update logic uses TMR, while the branch/jump targets are checked via instruction duplication.

4 Results

The proposed design was synthesized using Globalfoundries' 22 nm technology in topographical mode at the worst timing corner with a reference frequency of 250 MHz. Figure 2a displays the Power, Performance, and Area (PPA) estimations for TL, DCLS, and TCLS normalized to the values of the baseline version of Ibex, and a direct comparison with DCLS is highlighted. DCLS is an optional feature in Ibex, and the TCLS implementation is custom-developed. For a balanced comparison, the TL values include a multiplication of the sequential area that has to be protected against bitflips by a factor ranging between $\times 2$ and $\times 3$, depicted as the shaded area, when Rad Hard registers are considered [12].

The results show that the area overhead for TL is 30%, accounting for the registers used to store dummy results, the checkers needed to compare dummy and commit values, the recovery logic, and TMR applied to controllers. The area overhead increases to a range between 53% and 77% when RH registers are factored in by multiplying the vulnerable sequential area (RF, selected CSRs, controllers state holding registers) by a factor of $\times 2$ or $\times 3$, respectively. Thus, Temporal Redundancy with limited use of TMR compares favorably with DCLS or TCLS, which suffer respectively an increase greater than 100% and 200% due to complete Spatial Redundancy. The effect on the critical path was assessed



(a) Normalized PPA Analysis

Outcome	Base	TL		DCLS	TCLS
		TR	TMR		
Wrong Result	7.13	1.09		0.00	0.00
Hang ³	3.45	0.73		1.82	0.13
Detected	N.A.	7.58	4.28	18.70	
Corrected	N.A.			- ⁴	13.00
No Effect	89.42	86.32		79.48	86.87

(b) % of fault injection outcomes

Fig. 2. PPA and Fault Simulation results. (³A watchdog is required.)

⁴The correction mechanisms depends on the implementation)

by calculating the degradation in the minimum achievable clock period. TL is comparable but greater than DCLS because of the internal use of TMR, which adds a majority voter to the critical path for each protected block instead of a single voter on the core outputs. This degradation is accentuated in Ibex because of the limited pipelining. Power and energy calculations were based on a reference scenario where a single CoreMark iteration runs at 50 MHz. TL incurs a lower power increase than DCLS and TCLS due to the reduced area, but the execution time doubles due to instruction duplication, and energy consumption increases consequently. Thus, a tradeoff is highlighted between area reduction and increased energy consumption. However, repeating instructions at the hardware level is more energy-efficient than a software-only approach, where the overhead in execution time can increase by a factor of $\times 3\text{--}4$ [2].

A fault injection setup was devised to cause a SET-like fault in a combinational node during an RTL simulation. Given the list of all possible targets, a victim is chosen randomly, and its value is flipped in a random moment for one cycle between two consecutive negative edges of the clock to guarantee the presence of a positive edge. After a fault has been injected, the execution is compared on a cycle-per-cycle basis with the previously computed waveforms of a correct simulation to determine if the fault has corrupted the core state. Suppose it was filtered temporally, i.e. the victim register did not sample its input on the active clock edge. In that case, the routine continues to pick nets and flip their value periodically until corruption occurs. Otherwise, the outcome of the computation is checked for corruption. A matrix multiplication kernel was used as the target application to evaluate the protection offered by TL and compare it with DCLS and TCLS. Figure 2b reports the simulation outcomes from the baseline core and the protection mechanisms mentioned above. In the table, red indicates a problematic outcome, while green signifies an accepted one. In particular:

- Wrong Result: the computation ended with the wrong result
- Hang: the core reached an unrecoverable internal state, and a reset is needed (e.g. via a watchdog)

- Detected: the injected fault was detected
- Corrected: the injected fault was corrected
- No Effect: the fault did not produce any visible effect on the application

In Temporal Lockstep, the problematic outcomes are reduced from the unmodified core baseline value of 10.58% to 1.82%. The remaining ones, particularly those leading to wrong results, can be traced back to faults impacting TMR voters or unprotected segments of control paths not covered explicitly by TMR. The latter situation occurs in the small glue logic placed between different modules or for input signals coming from outside the core and shared by the replicated modules via TMR, thus generating a common mode fault. In DCLS and TCLS, no wrong results are expected due to the checker monitoring core-level outputs unless the failure affects the checker itself. The higher incidence of core hangs in DCLS compared to TCLS can be explained by the fact that the latter can carry out error correction even when one of the cores is irrecoverable by resetting it to the state chosen by the majority vote, contrary to the former that can solely perform error detection.

5 Conclusion

We have presented Temporal Lockstep, a fault tolerance technique to reduce the area overhead to protect a core against SETs by leveraging temporal redundancy via instruction duplication at the hardware level. An instruction can only update the core status or the main memory when two consecutive executions match. Otherwise, a fast recovery is executed by flushing the pipeline and repeating the affected instruction. The control path of the core is protected using TMR. The area overhead is estimated between 53% and 77%, including radiation-hardened registers for sequential elements vulnerable to SEUs, as opposed to more than 100% and 200% in DCLS and TCLS, respectively. We highlighted a tradeoff between reduced area occupation and increased energy consumption due to the doubled number of instructions, which places Temporal Lockstep between DCLS and TCLS in this regard. Lastly, fault injection simulations at an RTL level show a reduction by 82.8% of problematic outcomes from the unmodified core baseline value of 10.58% to 1.82%.

Acknowledgement. This work was supported by the National Centre for HPC, Big Data and Quantum Computing – HPC (CN00000013).

References

1. Barbirotta, M., Cheikh, A., Mastrandrea, A., Menichelli, F., Olivieri, M.: Design and evaluation of buffered triple modular redundancy in interleaved-multi-threading processors. *IEEE Access* **10**, 126074–126088 (2022)
2. Bohman, M., James, B., Wirthlin, M.J., Quinn, H., Goeders, J.: Microcontroller compiler-assisted software fault tolerance. *IEEE Trans. Nucl. Sci.* **66**(1), 223–232 (2019)

3. Davide Schiavone, P., et al.: Slow and steady wins the race? a comparison of ultra-low-power risc-v cores for internet-of-things applications. In: 2017 27th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS), pp. 1–8 (2017)
4. Gaillard, R.: Single Event Effects: Mechanisms and Classification, pp. 27–54. Springer US, Boston (2011)
5. Gunes, V., Peter, S., Givargis, T., Vahid, F.: A survey on concepts, applications, and challenges in cyber-physical systems. *KSII Trans. Internet Inf. Syst.* **8**(12), 4242–4268 (2014)
6. Gupta, S., Gala, N., Madhusudan, G.S., Kamakoti, V.: Shakti-f: a fault tolerant microprocessor architecture. In: 2015 IEEE 24th Asian Test Symposium (ATS), pp. 163–168 (2015)
7. Iturbe, X., Venu, B., Ozer, E.: Soft error vulnerability assessment of the real-time safety-related arm cortex-r5 cpu. In: 2016 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 91–96 (2016)
8. Iturbe, X., Venu, B., Ozer, E., Poupat, J.L., Gimenez, G., Zurek, H.U.: The arm triple core lock-step (tcls) processor. *ACM Trans. Comput. Syst.* **36**(3) (2019)
9. Kasap, S., Wächter, E.W., Zhai, X., Ehsan, S., McDonald-Maier, K.D.: Novel lockstep-based approach with roll-back and roll-forward recovery to mitigate radiation-induced soft errors. In: 2020 IEEE Nordic Circuits and Systems Conference (NorCAS), pp. 1–7 (2020)
10. Li, J., Zhang, S., Bao, C.: Duckcore: a fault-tolerant processor core architecture based on the risc-v isa. *Electronics* **11**(1) (2022)
11. Li, T., Ambrose, J.A., Ragel, R., Parameswaran, S.: Processor design for soft errors: challenges and state of the art. *ACM Comput. Surv.* **49**(3) (2016)
12. Lin, Y., Zwolinski, M., Halak, B.: A low-cost radiation hardened flip-flop. In: 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE), pp. 1–6 (2014)
13. Mach, J., Kohútka, L., Číčák, P.: In-pipeline processor protection against soft errors. *J. Low Power Electron. Appl.* **13**(2) (2023)
14. Rogenmoser, M., Tortorella, Y., Rossi, D., Conti, F., Benini, L.: Hybrid modular redundancy: exploring modular redundancy approaches in risc-v multi-core computing clusters for reliable processing in space. *ACM Trans. Cyber-Phys. Syst.* (2023). <https://doi.org/10.1145/3635161>
15. Silva, I., do Espírito Santo, O., do Nascimento, D., de Souza, S.X.: Cevero: A soft-error hardened soc for aerospace applications. In: Anais Estendidos do X Simpósio Brasileiro de Engenharia de Sistemas Computacionais, pp. 121–126. SBC, Porto Alegre (2020)
16. Tang, D., He, C., Li, Y., Zang, H., Xiong, C., Zhang, J.: Soft error reliability in advanced CMOS technologies-trends and challenges. *Sci. China Technol. Sci.* **57**(9), 1846–1857 (2014)
17. Velazco, R., Franco, F.J.: Single event effects on digital integrated circuits: origins and mitigation techniques. In: 2007 IEEE International Symposium on Industrial Electronics, pp. 3322–3327 (2007)
18. Wächter, E.W., Kasap, S., Zhai, X., Ehsan, S., McDonald-Maier, K.: Survey of lockstep based mitigation techniques for soft errors in embedded systems. In: 2019 11th Computer Science and Electronic Engineering (CEEC), pp. 124–127 (2019)



Exploiting the Latched Ring Oscillator Cell as a Compact PUF Architecture on FPGA

Riccardo Della Sala^(✉) and Giuseppe Scotti

Sapienza, University of Rome, 00184 Rome, RM, Italy
{riccardo.dellasala,giuseppe.scotti}@uniroma1.it

Abstract. In this study, the latched ring oscillator, previously employed as an entropy source in a True Random Number Generator, is exploited as Physical Unclonable Functions to derive keys. The LRO cell aims to minimize hardware usage on FPGA, particularly with respect to those architecture which exploits ring oscillators. An LRO-based PUF is implemented on an Artix-7 FPGA, occupying only 0.25 Slice/bit, representing cutting-edge efficiency. Evaluation on 16 Artix-7 FPGAs confirms the approach's effectiveness, achieving a Uniqueness of 48.63%, nominal Reliability of 95.11%, and 0–1 bias of 46.82%.

Keywords: Physical Unclonable Functions · Key Generation · Hardware Security · Cryptography

1 Introduction

In recent years, the field of computer science has increasingly focused on hardware security, driven by the growing efficiency of hardware attacks and tampering techniques [1–4]. Cryptographic algorithms, while robust, often depend on secret keys stored in device memories, making them susceptible to various forms of physical attacks, including micro-probing, focused ion beam techniques, glitch attacks, and side-channel attacks [5–7].

To mitigate these threats, researchers have developed innovative methods for securely storing secret keys. PUFs, in particular, have emerged as a secure alternative for storing cryptographic keys by generating unique outputs based on the intrinsic physical properties of a device, exploiting silicon variability to produce a unique “fingerprint” that serves as a cryptographic key. This approach eliminates the need for traditional non-volatile memory storage, enhancing security by dynamically generating keys [8, 9].

To effectively address the rising importance of hardware security in the context of contemporary computing, it is crucial to consider the vulnerabilities and countermeasures associated with physical device security. Modern technological advancements have facilitated seamless integration of smart devices into daily life, allowing for extensive data exchange across various sectors, including government, healthcare, and finance. While cryptographic algorithms serve to protect

data integrity and confidentiality, it is increasingly evident that the security of the hardware itself must also be fortified to defend against sophisticated physical attacks such as laser cutting and focused ion beam tampering [10–12].

Given the escalating threat landscape, innovative approaches to secure storage and authentication mechanisms are imperative. One promising solution is the deployment of Physical Unclonable Functions (PUFs). PUFs leverage inherent variations in semiconductor manufacturing processes to generate unique, hardware-specific responses that are difficult to replicate, thereby enhancing security in a cost-effective manner. Nevertheless, the performance of PUFs can be affected by environmental factors such as temperature fluctuations and supply voltage variations, necessitating a delicate balance between uniqueness and reliability within a compact design [10, 12–14].

Another fundamental cryptographic component is the True Random Number Generator (TRNG), which produces random bitstreams by harnessing unpredictable physical phenomena. TRNGs are vital for generating secure cryptographic keys and ensuring the randomness required for various security applications [15–17].

Both PUFs and TRNGs have found extensive application in Application-Specific Integrated Circuits (ASICs) and Field Programmable Gate Arrays (FPGAs). Current research trends favor their development on FPGA platforms due to their reconfigurability and cost-effectiveness [10, 18].

1.1 State-of-the-Art of Physical Unclonable Functions

Several FPGA-compatible solutions for PUF integration have been explored. SRAM-based PUFs, for example, offer compactness and superior uniqueness due to the inherent asymmetries in metastable cells, outperforming traditional ring oscillator (RO) based implementations in terms of space efficiency and performance consistency. The Butterfly PUF, utilizing a cross-coupled latch pair, requires meticulous routing to ensure optimal operation, particularly in managing the precharge and clear operations symmetrically. On the other hand, RO-based PUFs exhibit exceptional reliability under varying environmental conditions. Other designs, such as the NAND latch PUF [13] and the Pico-PUF [10, 14], provide alternatives with different trade-offs in terms of reliability and resource usage. The Transient Effect Ring Oscillator (TERO) PUF, which relies on transient frequency mismatches between two nominally identical oscillators, necessitates additional hardware for bit extraction and stability assurance [19, 20]. Advances in enhancing the reliability of metastability-based PUFs have been proposed, emphasizing novel excitation sequences to achieve stable responses [12, 21–23].

FPGA-based TRNG solutions also abound, typically relying on physical phenomena like jitter accumulation [15] or coherent sampling. RO configurations, which are common in TRNGs, require precise delay balancing to meet National Institute of Standards and Technology (NIST) compliance standards. High-throughput RO-based TRNGs incorporate techniques like frequency modulation and Multi-Stage Feedback Ring Oscillators (MSFRO) [24]. Lightweight

architectures aim to minimize resource usage, though they may compromise the quality of the bitstream, necessitating post-processing or feedback mechanisms to ensure randomness [15].

Integrating PUFs and TRNGs on the same chip presents a powerful strategy to bolster hardware security in cryptographic applications. However, achieving a unified, reconfigurable PUF+TRNG architecture on FPGA platforms entails navigating trade-offs between statistical properties, complexity, resource utilization, and power consumption. An RO-based PUF+TRNG solution compatible with FPGA platforms has been documented in [25], where oscillation frequencies are compared for PUF key derivation, and XORed RO outputs are used for random bitstream extraction. The proposed architecture repurposes conventional RO PUFs as TRNGs, demonstrating a novel approach to reconfigurable entropy sources.

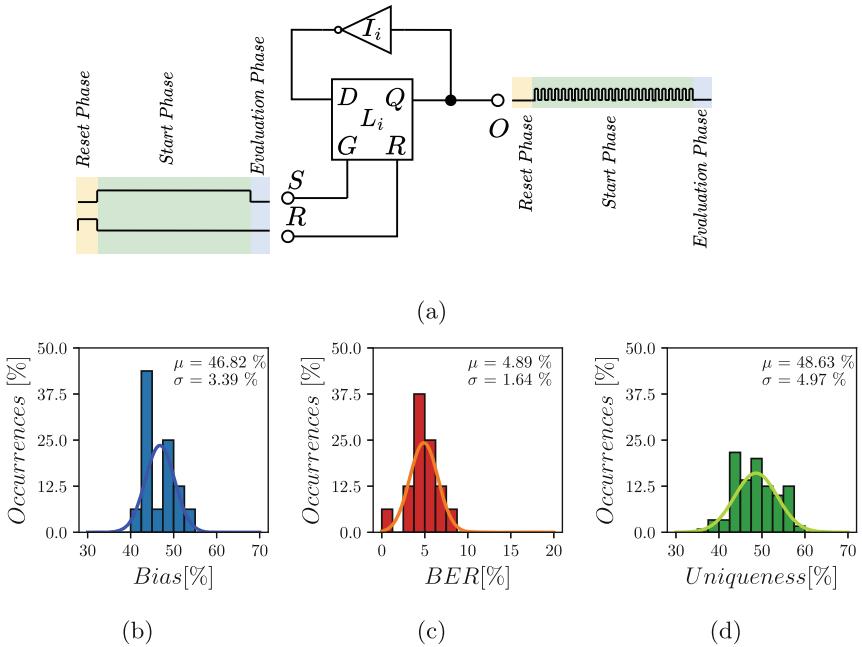


Fig. 1. Scheme of the proposed LRO cell a), bias b), Bit Error Rate (BER) c) and Uniqueness d) of the proposed LRO PUF.

1.2 Figures of Merits

The primary metrics for PUF evaluation are Reliability, ideally at 100%, indicating the stability of bits under varied environmental conditions; Uniqueness, ideally at 50%, showing the differentiation between keys generated by the same

PUF across different devices. Additionally, key bias reflects the proportion of 0s or 1s in the key. In FPGA-based PUF assessment, resource consumption per bit, typically measured by Slices [21], is a critical factor.

2 Proposed Architecture

The LRO cell, depicted in Fig. 1a, comprises an inverter and a latch. Two control signals, S and R, are employed to stimulate the architecture effectively. The excitation sequence is delineated into three primary phases:

- Reset Phase: During this phase, the R signal is high, and the S signal is low. The latch is opaque in this state, enforcing its output to 0. Utilizing the inverting function of the inverter, the D input of the latch is set to 1, preventing oscillation at the output node Q.
- Start Phase: Here, the R signal transitions low, while the S signal remains high for N clock cycles. With the S signal governing the gate terminal, the latch becomes transparent, enabling the circuit to act as a ring oscillator for N clock cycles.
- Evaluation Phase: The R signal persists low, and the S signal transitions low as well, rendering the latch opaque and sampling the output Q of the ring oscillator. This yields a state that can be 0, 1, or during the low-to-high (high-to-low) transition.

The PUF response is acquired through comparing the oscillation frequencies of multiple nominally identical LRO cells.

For the FPGA implementation of the LRO Cell, the AMD series-7 devices were chosen as the target platform. Using a lookup table (LUT) and a flip-flop configured as a latch, the LRO cell was instantiated. Each Slice accommodated 4 LUTs and 4 latches, enabling the incorporation of 4 LRO cells within each Slice. Additionally, as each Configurable Logic Block (CLB) comprises two Slices, a total of 8 LRO cells were integrated into each CLB. The oscillation frequencies of LRO cells within each CLB are very similar, allowing for the extraction of 8 bits from each CLB by comparing their frequencies.

The performance evaluation of the proposed PUF+TRNG architecture involved 16 identical Artix-7 FPGAs (xc7a100t-2e). Key performance metrics for the 128-bit LRO PUF across the 16 FPGA boards are summarized in Fig. 1. Figure 1b shows the PUF bias, Fig. 1c presents the nominal bit error rate (BER), and Fig. 1d displays Uniqueness results. On average, Bias is 46.82% (ideal: 50%), BER averages 4.89% (ideal: 0%), and the Uniqueness distribution averages 48.63% (ideal: 50%). These findings demonstrate the effectiveness of the proposed approach. Furthermore, the Bias and Uniqueness results suggest that the selected routing strategy and PUF response extraction method effectively address FPGA implementation challenges.

A comparison with state-of-the-art is depicted in Table 1. As it can be observed, the proposed work is 2 \times more compact than state-of-the-art and results in comparable performance with respect to Reliability and Uniqueness.

Table 1. Comparison Table

	Platform	Slice/bit	Uniqueness	Reliability
[10]	Artix-7	1	48.05	99.30
[13]	Spartan-6	2	49.24	99.18
[14]	Spartan-6	1	49.93	93.96
[12]	Artix-7	0.5	49.50	98.62
This Work	Artix-7	0.25	48.63	95.11

3 Conclusion

This work introduces a compact PUF design utilizing LRO cells. Implemented on an Artix-7 FPGA, experimental evaluation across 16 boards confirms its efficacy, demonstrating a $2\times$ reduction in size compared to state-of-the-art, while maintaining comparable levels of Uniqueness and Reliability.

References

1. Sklavos, N., Chaves, R., Di Natale, G., Regazzoni, F. (eds.): *Hardware Security and Trust*. Springer, Cham (2017). <https://doi.org/10.1007/978-3-319-44318-8>
2. Jin, Y.: Introduction to hardware security. *Electronics* **4**, 763–784 (2015)
3. Potlapally, N.: Hardware security in practice: challenges and opportunities. In: 2011 IEEE International Symposium on Hardware-Oriented Security and Trust, pp. 05–06. IEEE (2011)
4. Majzoobi, M., Koushanfar, F., Potkonjak, M.: Testing techniques for hardware security. In: 2008 IEEE International Test Conference, pp. 28–30. IEEE (2008)
5. Hu, W., Chang, C.H., Sengupta, A., Bhunia, S., Kastner, R., Li, H.: An overview of hardware security and trust: threats, countermeasures, and design tools. *IEEE Trans. Comput.-Aided Des. Integrat. Circ. Syst.* **40**(6), 1010–1038 (2020)
6. Gennaro, R., Lysyanskaya, A., Malkin, T., Micali, S., Rabin, T.: Algorithmic tamper-proof (ATP) security: theoretical foundations for security against hardware tampering. In: Naor, M. (ed.) *TCC 2004*. LNCS, vol. 2951, pp. 258–277. Springer, Heidelberg (2004). https://doi.org/10.1007/978-3-540-24638-1_15
7. Spreitzer, R., Moonsamy, V., Korak, T., Mangard, S.: Systematic Classification of Side-Channel Attacks: A Case Study for Mobile Devices. *IEEE Commun. Surv. Tutorials* **20**, 465–488 (2017)
8. Della Sala, R., Bellizia, D., Centurelli, F., Scotti, G.: A monostable physically unclonable function based on improved RCCMs with 0–1.56% native bit instability at 0.6–1.2 V and 0–75 °C. *Electronics* **12**, 755 (2023)
9. Della Sala, R., Centurelli, F., Scotti, G., Tommasino, P., Trifiletti, A.: A differential-to-single-ended converter based on enhanced body-driven current mirrors targeting ultra-low-voltage OTAs. *Electronics* **11**(23), 3838 (2022)
10. Gu, C., Chang, C.-H., Liu, W., Hanley, N., Miskelly, J., O’Neill, M.: A large-scale comprehensive evaluation of single-slice ring oscillator and PicoPUF bit cells on 28-nm Xilinx FPGAs. *J. Cryptogr. Eng.* **11**, 227–238 (2021)

11. Sala, R.D., Scotti, G.: The DD-cell: a double side entropic source exploitable as PUF and TRNG. In: 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), pp. 12–15. IEEE (2022)
12. Della Sala, R., Scotti, G.: A novel FPGA implementation of the NAND-PUF with minimal resource usage and high reliability. *Cryptography* **7**(2), 18 (2023)
13. Habib, B., Kaps, J.-P., Gaj, K.: Efficient SR-latch PUF. In: Sano, K., Soudris, D., Hübner, M., Diniz, P.C. (eds.) ARC 2015. LNCS, vol. 9040, pp. 205–216. Springer, Cham (2015). https://doi.org/10.1007/978-3-319-16214-0_17
14. Gu, C., O'Neill, M.: Ultra-compact and robust FPGA-based PUF identification generator. In: 2015 IEEE International Symposium on Circuits and Systems (ISCAS), pp. 934–937. IEEE (2015)
15. Sala, R.D., Bellizia, D., Scotti, G.: A novel ultra-compact FPGA-compatible TRNG architecture exploiting latched ring oscillators. *IEEE Trans. Circuits Syst. II* **69**, 1672–1676 (2021)
16. Sala, R.D., Scotti, G.: On enhancing the throughput of the latched ring oscillator TRNG on FPGA. In: Applications in Electronics Pervading Industry, Environment and Society, pp. 277–283. Springer, Cham (2024)
17. Sala, R.D., Bellizia, D., Scotti, G.: High-throughput FPGA-compatible TRNG architecture exploiting multistimuli metastable cells. *IEEE Trans. Circ. Syst. I* **69**, 4886–4897 (2022)
18. Sala, R.D., Bellizia, D., Centurelli, F., Scotti, G., Trifiletti, A.: Exploiting body-driven feedbacks in physical unclonable functions for ultra low voltage, ultra low power applications: a 0.3 V weak-PUF. *IEEE Trans. Circ. Syst. I*, 1 (2024)
19. Bossuet, L., Ngo, X.T., Cherif, Z., Fischer, V.: A PUF based on a transient effect ring oscillator and insensitive to locking phenomenon. *IEEE Trans. Emerging Top. Comput.* **2**, 30–36 (2013)
20. Sala, R.D., Scotti, G.: Exploiting the DD-cell as an ultra-compact entropy source for an FPGA-based re-configurable PUF-TRNG architecture. *IEEE Access* **11**, 86178–86195 (2023)
21. Della Sala, R., Bellizia, D., Scotti, G.: A novel ultra-compact FPGA PUF: the DD-PUF. *Cryptography* **5**, 23 (2021)
22. Della Sala, R., Scotti, G.: The DD-cell: a double side entropic source exploitable as PUF and TRNG. In: 2022 17th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), pp. 353–356. IEEE (2022)
23. Sala, R.D., Bellizia, D., Scotti, G.: A lightweight FPGA compatible weak-PUF primitive based on XOR gates. *IEEE Trans. Circuits Syst. II* **69**, 2972–2976 (2022)
24. Cui, J., et al.: Design of true random number generator based on multi-stage feedback ring oscillator. *IEEE Trans. Circuits Syst. II* **69**, 1752–1756 (2021)
25. Wang, Y., et al.: A reconfigurable PUF structure with dual working modes based on entropy separation model. *Microelectron. J.* **124**, 105445 (2022)



Low Power Design of Approximate Adders Based on Inexact Full Adder

Ali Ibrahim¹(✉), Fatima Bzeih¹, Oussama Srour¹, Zeinab Hijazi¹, and Orazio Aiello²

¹ Department of Electrical and Electronics Engineering, Lebanese International University, Beirut, Lebanon

ali.ibrahim@liu.edu.lb

² Department of Electrical, Electronic, Telecommunication Engineering, and Naval Architecture DITEN, University of Genoa, Genoa, Italy

Abstract. This paper presents the design of a low-power logic gate approximate adder based on an inexact full adder. Simulation results show that the proposed adder improves the accuracy over approximate adders by 27% in terms of mean square error (MSE) while achieving a power reduction of 8% demonstrated by synthesis. Moreover, when compared to the exact adder, the proposed circuit achieves a power reduction of up to 40% in the case of a 16-bit adder with 14 approximated bits.

Keywords: Low Power Design · Logic Gate Architectures · Approximate Computing · Inexact Adders · VLSI circuits

1 Introduction

Designing low power circuits has become one of the top design priorities in a wide range of electronic systems, particularly for self-powered smart sensing systems for Internet of Things and Wearable devices [1]. The growing need for higher computing power is pushing towards the development of ultra-low power strategies and methods. Seeking to enhance energy efficiency, hardware designers are employing optimization techniques at various levels ranging from system to gate and transistor levels. Approximate computing is an efficient method for boosting efficiency across the computing stack by using the natural fault resiliency of many application domains. By measuring and tuning the accuracy, considered to be the quality of results, the approximate computing method enables significant reduction in the area and power consumption of VLSI circuits. Many error-resilient applications such as machine learning, digital signal processing, and computer vision are computationally intensive as they require a significant number of adder units in their hardware architectures. Aside from their high presence in complex computing architectures, adders are also the main building blocks for many other arithmetic operations. Hence, improving the efficiency of adder blocks may significantly affect such operations. A low power approximate reduced precision redundancy scheme for unsigned integer arithmetic computation is proposed in [2]. Instead of replicating the entire module multiple times, authors proposed the use of inexact copies to reduce the

redundancy overhead maintaining the ability of correcting large errors. Zhou et. al. Have increased the accuracy of approximate adders at the cost of low extra complexity [3]. Authors proposed an enhancement to four different types of approximate adders and presented an improvement in computational precision at the cost of minor increase in area and energy. A comparative study with analysis for static approximate adders considered suitable for both FPGA and ASIC type implementations is provided in [4]. Various static approximate adder architectures have been highlighted and evaluated in terms peak signal to noise ratio and structural similarity index targeting digital image processing application. In [5], approximate parallel prefix adders have been proposed by employing the approximation in the prefix operators. Results have shown that the proposed adder overcomes similar state of the art solution when energy-quality and area-quality have been compared. Authors in [6] proposed the design of approximate adders and multipliers for majority logic. Designed circuits have been evaluated in terms of error, delay, and gate complexity showing superior performance When compared to similar state of the art methods. An approximate majority logic based multibit adders and multipliers is proposed in [7]. Several implementation metrics have been employed to evaluate the proposed designs such as costs, error, and layouts showing significant improvement over previous similar designs.

In this work, we propose the design of an approximate adder based on inexact full adder architecture. Results demonstrate that the proposed adder provides comparable results in terms of accuracy while overcoming similar state-of-the-art solutions in terms of power consumption.

2 Approximate Adder Gate Level Design

The proposed architecture of the gate level approximate adder based on inexact full adder is illustrated in Fig. 1. The core design of the proposed inexact full adder divides the circuit into two main parts: the most significant bits (MSB) part and the least significant bits (LSB) part. The LSB part employs Lower Part Or Adder (LOA) [2] while the MSB one incorporates an inexact full adder aiming to further reduce the circuit complexity. The approximation is made in the carry-out (c_{out}) component by replacing the majority function among a , b , and c_{in} usually used to compute the carry by an OR gate considering as input only a and b . This approximation assumes that both ‘ a ’ and ‘ b ’ has the most significant influence on the overall circuit behavior. The carry-out (c_{out}) value is calculated using $c_{out} = a \text{ or } b$. This doesn’t involve any carry propagation through the intermediate stages; however, it assumes that the carry-in signal (C_{in}) has already been precomputed and is ready to be used in the calculations like in carry-look-ahead adder (CLA). Thus, the combination of the MSB and LSB parts serves to merge the two components effectively. As a result, the sum of the final bit in the LSB section is linked to the carry-in of the least significant bit within the MSB part. This is shown in Fig. 2 where $C_{in(k)}$ from the MSB section equals to the $S(k-1)$ for the LSB part.

3 Implementation and Results

The proposed circuit has been implemented using VHDL hardware description language on Cadence. Xcelium and Genus tools have been used for simulation and synthesis respectively. Table 1, Table 2, and Table 3 report the obtained implementation results of the proposed circuit for 8-bit, 16-bit, and 32-bit architectures respectively. For the approximate adder error calculation, the following metrics are employed as they are the most common in the literature: mean relative error (MRE), mean error distance (MED), normalized mean error distance (NMED), and mean squared error (MSE). The MRE is defined by the following formula: $MRE = \frac{\sum_{i=0}^N \frac{Error}{ExactResult}}{N} \times 100$, where N is the number of samples. On the other hand, the MED is calculated by the sum of the error over the number of samples $MED = \frac{\sum Error}{N}$, and the NMED is defined as $NMED = \frac{MED}{K}$, where k represents the number of bits. Finally, the following equation defines the mean square error MSE $= \frac{1}{N} \sum_{i=0}^N (Error)^2$. It is clearly shown from the reported tables how the area and power consumption are reduced with the increase of the number of approximated bits (NAB) at the cost of a quality degradation in the presented error metrics. This extensive simulation may lead to the selection of a trade-off between quality and performance depending on the error resiliency of the target application. Furthermore, Table reports the results providing a comparison of the quality of results represented by the mean square error (MSE) versus the power consumption among the proposed architecture and similar state of the art solutions. Although the highlighted architectures present implementations using different technologies, the proposed architecture is considered to be the worst-case scenario since it uses 180 nm technology while the others are using 90 nm [3] and 28 nm [2].

Table 1. Proposed 8-bit adder performance metrics

NAB	MRE	MED	NMED	MSE	Log (MSE)	Power (μW)	Area
0	-2.656	-0.992	-0.124	1.969	0.294	43.954	1316.534
2	-2.525	-0.250	-0.031	4.438	0.647	41.050	1224.955
4	-1.934	-0.750	-0.094	25.50	1.406	37.536	1117.641
6	1.086	-1.250	-0.156	218.5	2.339	34.022	1010.328
8	22.342	30	3.750	2506.5	3.399	31.312	925.739

Fig. 2 Shows the power consumption reduction with the variation of NAB. Without any approximated bit (NAB = 0), the proposed approximate adder provides around 20% of power reduction when compared to the exact adder. Moreover, it achieves up to 40% power reduction when the NAB = 14 bits.

Table 2. Proposed 16-bit adder performance metrics

NAB	MRE	MED	NMED	MSE	Log (MSE)	Power (μW)	Area
0	-0.019	0	0	1.999	0.301	93.196	2895.414
2	-0.020	-0.25	-0.016	4.499	0.653	90.292	2803.835
4	-0.022	-0.75	-0.047	26.496	1.423	86.780	2696.521
6	-0.014	-1.25	-0.078	234.438	2.370	83.269	2589.208
8	0.033	-1.75	-0.109	2985.5	3.475	79.752	2481.895
10	0.233	-2.25	-0.141	44698.5	4.650	76.235	2374.581
12	0	0	0	0	-	72.723	2267.268
14	0	0	0	0	-	69.211	2159.955

Table 3. Proposed 32-bit adder performance metrics

NAB	MRE	MED	NMED	MSE	Log (MSE)	Power (μW)	Area
0	-0.007	-1	-0.031	1.999	0.301	179.711	5321.965
4	-0.008	-1.75	-0.055	26.499	1.423	173.293	5123.072
8	0.009	-2.727	-0.085	2987.31	3.475	166.265	4908.445
12	0.342	3.460	0.108	699270	5.844	159.236	4693.818
16	6.425	2408.88	75.277	1.846×10^8	8,266	152.208	4479.192
20	49.999	50000	1562.5	6.666×10^9	9.823	141.632	4154.597
24	24.985	24995.9	781.121	1.666×10^9	9.221	138.151	4094.938
28	24.985	24995.9	781.121	1.666×10^9	9.221	131.122	3835.312
32	24.985	24995.9	781.121	1.666×10^9	9.221	124.896	3643.410

4 Conclusions and Future Perspectives

This paper presented the implementation and analysis of a proposed approximate adder based on inexact full adder architecture. Functional simulations have been done at RTL level and demonstrated the effectiveness of the proposed architecture by achieving comparable results in terms of accuracy when compared to similar state of the art solutions. Moreover, the circuit achieved a reduction of up to 40% in power consumption with

Table 4. MSE vs Power consumption for different 16-bit adder architectures. Number of approximation bits (NAB) = 8.

Reference	Technology	MSE	Power (mW)
Convention [2]	28 nm	226.04	2.771
ITDMR [2]	28 nm	263.61	2.240
ARPR [2]	28 nm	247.97	2,200
ESA [3]	90 nm	32640	0.187
EESA [3]	90 nm	24440	0.189
LOA [3]	90 nm	4096	0.086
Proposed	180 nm	2985.5	0.079

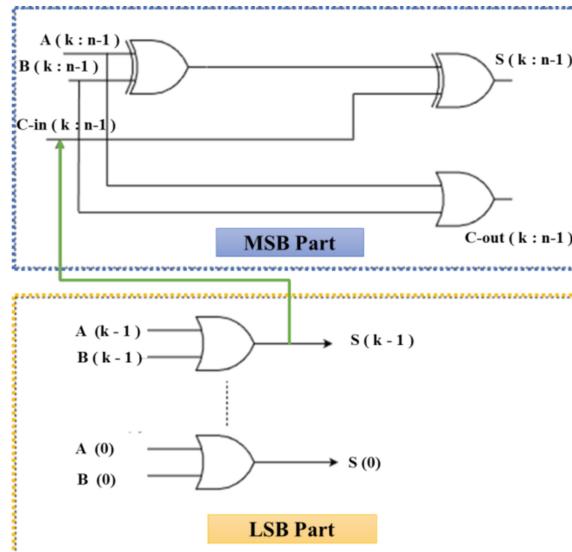


Fig. 1. Gate level architecture of the approximate adder based on inexact full adder.

respect to exact adder when synthesized on X-FAB 180 nm technology. Future work will consist of integrating the proposed circuit in the Coordinate Rotational Digital Computer

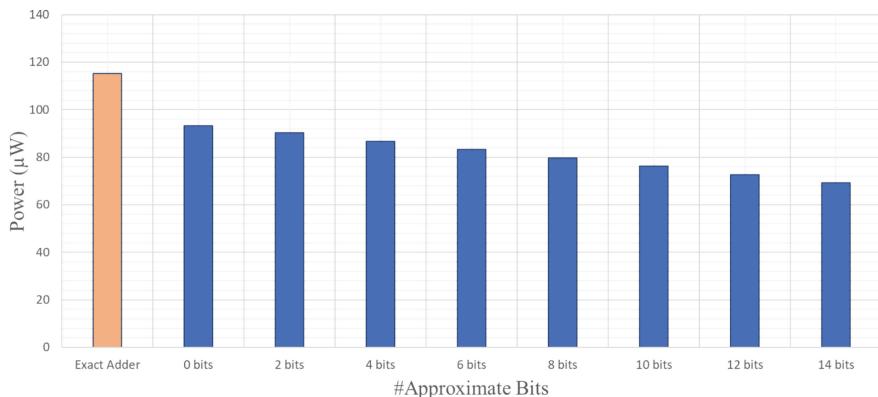


Fig. 2. The bar plot of the power consumption variation of the proposed approximate adder with the variation of the number of approximated bits and with respect to the exact adder.

(CORDIC) circuit used as squarer in the Izhikevich neuron architecture targeting a low power spiking neural network integrated circuit (Table 4).

Acknowledgement. This project has received funding from the European Union’s Horizon Europe research and innovation programme under the Marie Skłodowska-Curie grant agreement No 101086359.

References

1. M. Osta et. al, “Approximate Multipliers Based on Inexact Adders for Energy Efficient Data Processing,” 2017 New Generation of CAS (NGCAS), Genova, Italy, 2017
2. Chen, K., et al.: Low-Power Approximate RPR Scheme for Unsigned Integer Arithmetic Computation. IEEE Open J. Nanotechnol. **3**, 36–44 (2022)
3. Y. Zhou, J. Lin and Z. wang, “Increasing the Accuracy of Approximate Adders with Very Low Extra Complexity,” 2018 IEEE 18th International Conference on Communication Technology (ICCT), Chongqing, China, 2018
4. B., Padmanabhan et. al. 2021. “Gate-Level Static Approximate Adders: A Comparative Analysis” Electronics 10, no. 23: 2917
5. Perri, S., Spagnolo, F., Frustaci, F., Corsonello, P.: Accuracy Improved Low-Energy Multi-Bit Approximate Adders in QCA. IEEE Trans. Circuits Syst. II Express Briefs **68**(11), 3456–3460 (2021). <https://doi.org/10.1109/TCSII.2021.3077669>
6. M. M. A. d. Rosa, G. Paim, P. Ü. L. d. Costa, E. A. C. d. Costa, R. I. Soares and S. Bampi, “AxPPA: Approximate Parallel Prefix Adders,” in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 31, no. 1, pp. 17–28, Jan. 2023, <https://doi.org/10.1109/TVLSI.2022.3218021>
7. Z. Chu, C. Shang, T. Zhang, Y. Xia, L. Wang and W. Liu, “Efficient Design of Majority-Logic-Based Approximate Arithmetic Circuits,” in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 12, pp. 1827–1839, Dec. 2022, <https://doi.org/10.1109/TVLSI.2022.3210252>



0.7 V, 215 nW Tunable Universal Gm-C Filter

Ali Namdari^(✉), Orazio Aiello, and Daniele D. Caviglia

DITEN, University of Genova, Genoa, Italy
ali.namdari@edu.unige.it

Abstract. In this paper, an ultra-low-power, inverter-based, universal Gm-C filter is proposed. The proposed filter benefits from the orthogonal tunability of center frequency (f_0) and quality factor (Q) and is designed using 180 nm TSMC technology node parameters. To significantly reduce the proposed filter's power consumption, all transistors are biased in the subthreshold region at a 0.7 V supply voltage. Additionally, the quality factor and center frequency of the proposed filter are varied by the variations of the capacitance parameters. The power consumption for the proposed Gm-C filter is 215 nW at the center frequency of 4.5 kHz.

Keywords: Low-power · Inverter · Gm-C · Universal filter · CMOS · Tunability

1 Introduction

In the past few years, Gm-C filters have become widely used in a variety of applications, including communication systems, signal processing, implantable biomedical devices, and portable electronic systems [1–3]. The use of analog filters, due to their different frequency responses, such as low-pass (LP), high-pass (HP), band-reject (BR), all-pass (AP), and band-pass (BP) is common in a wide range of applications. Therefore, the design of a universal filter in which all the filtering responses (LP, HP, BR, AP, and BP) can be generated is reported in [1–3]. Considering that analog circuits use both current and voltage signals, multi-mode analog filters, can be generated in different modes of operation like voltage mode (VM), current mode (CM), transconductance mode (TCM), and trans resistance mode (TRM) [1–3]. Furthermore, the adjustability of the filter's performance (center frequency f_0 , quality factor Q) over a wide range is crucial in the design of high-performance universal Gm-C filters [4–9].

2 The Proposed Tunable Gm-C Filter

The tunable, universal Gm-C filter is depicted in Fig. 1(a). In Fig. 1(a), I_{in1} , I_{in2} , I_{in3} , and V_{in1} , V_{in2} , and V_{in3} represent input current and voltage signals, while I_{out} and V_{out} signify the output current and voltage signals of the proposed filter. The inverter-based gm block used in the proposed filter is shown in Fig. 1(b) in which g_{mN} and g_{mP} are negative and positive output voltage gm blocks. As shown in Fig. 1(b), to have a proper output voltage biasing, the Common-mode Feedback (CMFB) circuit is added

to the inverter circuit design. The filter equations for the overall transfer function, are as follows:

$$V_{\text{OUT(VM)}} = \frac{S^3 V_{\text{in}3} + \frac{g_{\text{mP}}}{C_3} S^2 V_{\text{in}2} + \frac{g_{\text{mP}}^2}{C_2 C_1} S V_{\text{in}1}}{D(s)} \quad (1)$$

$$I_{\text{OUT(TCM)}} = \frac{g_{\text{mP}} \left[S^3 V_{\text{in}3} + \frac{g_{\text{mP}}}{C_3} S^2 V_{\text{in}2} + \frac{g_{\text{mP}}^2}{C_2 C_1} S V_{\text{in}1} \right]}{D(s)} \quad (2)$$

$$I_{\text{OUT(CM)}} = \frac{S^3 I_{\text{in}3} + \frac{g_{\text{mP}}}{C_3} S^2 I_{\text{in}2} + \frac{g_{\text{mP}}^2}{C_2 C_1} S I_{\text{in}1}}{D(s)} \quad (3)$$

$$V_{\text{OUT(TRM)}} = \frac{S^3 I_{\text{in}3} + \frac{g_{\text{mP}}}{C_3} S^2 I_{\text{in}2} + \frac{g_{\text{mP}}^2}{C_2 C_1} S I_{\text{in}1}}{g_{\text{mP}} D(s)} \quad (4)$$

$$D(s) = S^3 + \frac{g_{\text{mN}}}{C_3} S^2 + \frac{g_{\text{mN}} g_{\text{mP}}}{C_2 C_1} S \quad (5)$$

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{g_{\text{mN}} g_{\text{mP}}}{C_2 C_1}} \quad (6)$$

$$Q = \frac{C_3}{g_{\text{mN}}} \sqrt{\frac{g_{\text{mN}} g_{\text{mP}}}{C_2 C_1}} \quad (7)$$

The variation filtering functions for the proposed filter are summarized in Table 1. As shown in Table 1, the different filtering functions (LP, HP, BP, BR, and AP) are obtained in all modes of operations.

Table 1. Different filtering function for the proposed filter.

Filtering Function	Input for Current and Trans-resistance Modes	Input for Voltage and Trans-conductance Modes
LP	$I_{\text{in}1}$	$V_{\text{in}1}$
HP	$I_{\text{in}3}$	$V_{\text{in}3}$
BP	$I_{\text{in}2}$	$V_{\text{in}2}$
BR	$I_{\text{in}1} = I_{\text{in}3}$	$V_{\text{in}1} = V_{\text{in}3}$
AP	$I_{\text{in}1} = I_{\text{in}2} = I_{\text{in}3}$	$V_{\text{in}1} = V_{\text{in}2} = V_{\text{in}3}$

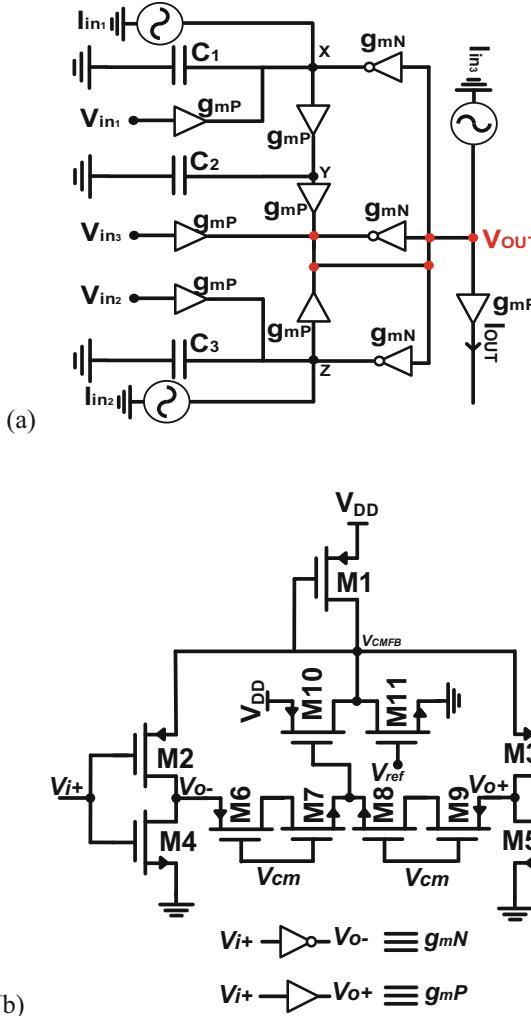


Fig. 1. Schematic of the proposed Gm-C filter: (a) Tunable Gm-C filter (b) Proposed gm block.

3 Simulation Results

The proposed inverter-based gm block is biased at 0.7 V supply voltage while its transistors are biased in the sub-threshold region resulting in low power consumption. The simulation results for the Gm-C filter in all modes of operations are illustrated in Fig. 2. The proposed Gm-C filter can adjust the quality factor and center frequency parameters as depicted in Fig. 3. It is evident from Fig. 3(a) that the quality factor's performance varies with changes in the C_3 values. Similarly, the center frequency of the proposed filter varies with adjustments in capacitance values (C_1, C_2, C_3) as illustrated in Fig. 3(b).

Table 2 summarizes the variations in quality factor (C_3 variations) and center frequency (capacitance variations) for the proposed filter.

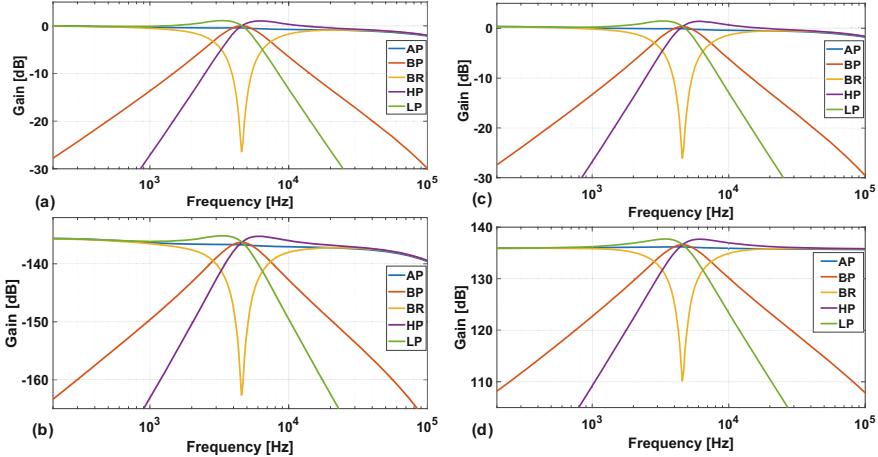


Fig. 2. Simulation results for the Gm-C filter (a): Voltage-mode filter (b): Trans-conductance mode filter (c): Current-mode filter (d): Trans-resistance mode filter.

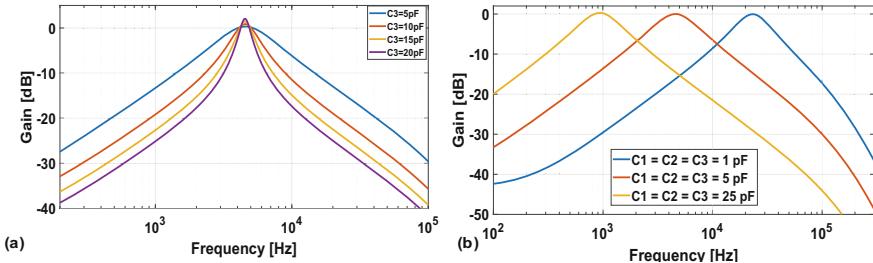


Fig. 3. The tunability simulation results for the proposed filter; (a) Quality factor, (b) Center frequency.

4 Comparison with the Other Reported Designs

The comparison of the proposed filter with the other reported designs are summarized in Table 3. As shown from Table 3, The proposed filter's power consumption is a considerably lower than that of [4, 6, 8] while is higher in comparison to [5, 7, 9]. The proposed filter has the ability to adjust the wider frequency range for the center frequency than other reported designs. The proposed filter is a universal filter which is able to generate in all modes of operation while in [4, 5, 7] the modes operating is only voltage. Furthermore, the universal multi-mode filters are reported in [6, 8, 9] while they have ability to adjust the center frequency, but their center frequency range are lower in comparison to the proposed filter. It is worth mentioning that the power consumption of the proposed filter is stable when its center frequency is adjusted by capacitance variations, while the tunability of all other reported designs consume a higher power consumption due to the current biasing variations. To better comparison of the proposed filter in low power design with other reported circuits shown in Table 3, the Figure-of-Merit (FOM) parameter is defined as follows, where P is the power consumption, f is the center frequency,

Table 2. Quality factor and center frequency variations.

$C_1 = C_2 = 5 \text{ pF}, C_3 = \text{pF}$	Quality Factor
5	1
10	2
15	3
20	4
Capacitance Variations	Frequency range
$C_1 = C_2 = C_3 = 1 \text{ pF}$	25 kHz
$C_1 = C_2 = C_3 = 5 \text{ pF}$	4.5 kHz
$C_1 = C_2 = C_3 = 25 \text{ pF}$	950 Hz
$C_1 = C_2 = C_3 = 1 \text{ pF}$	200 Hz

N is the filter's order, and DR is the dynamic range of the filter.

$$\text{FOM} = \frac{P}{f \cdot N \cdot DR} \quad (8)$$

Due to the fact that the supply voltage of the proposed filter is higher in comparison to all reported design, the proposed filter has a significantly lower FOM value than all reported circuits shown in Table 3 which confirms that the proposed filter has a better performance in low-power and low-voltage applications.

Table 3. Comparison table.

Parameters	[4]	[5]	[6]	[7]	[8]	[9]	T.W
Supply voltage [V]	0.5	0.5	0.5	0.5	0.5	0.5	0.7
Universal	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Multi-mode	Voltage	Voltage	Yes	Voltage	Yes	Yes	Yes
Filter order	2	2	2	2	2	2	2
Center frequency [kHz]	0.254	0.01	0.323	0.153	0.211	0.114	4.5
Frequency tuning [Hz]	66–501	5.9–21.6	162–1330	62.3–595.6	28–211	58.8–840	200–25000
Tuning rang [X]	7.6	3.66	8.2	9.56	7.53	14.28	125
THD [%]	0.62	1	0.8	0.33	1	1	1
Dynamic range [dB]	49.7	63	53.2	50	58.23	53.2	40
Noise [μ Vrms]	116	45	108	220	130	208	72
Power consumption [nW]	616	53.3	646	37	281	58	215
FOM [10^{-12} W · Hz $^{-1}$ · dB $^{-1}$]	3.96	1.88	2.187	2.41	0.816	0.566	0.24

5 Conclusion

In this paper, an inverter-based, universal Gm-C filter using 180 nm TSMC technology node is presented which can properly generate all the filtering responses in all modes of operation. Furthermore, the transistors of the proposed filter bias in the sub-threshold region, which effectively decreases the power consumption, while the proposed filter benefits from the orthogonal tunability of the center frequency (f_0) and quality (Q) parameters. The power consumption of the proposed filter at the frequency of 4.5 kHz is 215 nW which justifies its ultra-low-power performance.

References

1. Namdari, A., Dolatshahi, M.: A new ultra low-power, universal OTA-C filter in subthreshold region using bulk-drive technique. *Int. J. Electron. Commun. (AEÜ)* **82**(12), 458–466 (2017)
2. Namdari, A., Dolatshahi, M.: Design of a low-voltage and low-power, reconfigurable universal OTA-C filter. *Analog Integr. Circuits Signal Process.* **111**(2), 169–188 (2022)
3. Namdari, A., Dolatshahi, M., Aghababaei, M.: A new ultra low-power high-order universal OTA-C filter based on CMOS double-inverters in the subthreshold region. *Circuits Syst., Signal Processing J.* **42**, 6379–6398 (2023)

4. Khateb, F., Kumngern, M., Kulej, T., Biolek, D: 0.5 V Differential Difference Transconductance Amplifier and Its Application in Voltage-Mode Universal Filter. *IEEE Trans. Access.* 10, 43209–43220 (2022).
5. Jaikla, W., Khateb, F., Kumngern, M., Kulej, T., Ranjan, R-K., Suwanjan, P: 0.5 V Fully Differential Universal Filter Based on Multiple Input OTAs. *IEEE Trans. Access.* 8, 187832 –187839 (2020)
6. Kulej, T., Kumngern, M., Khateb, F., Arbet, D: 0.5 V Versatile Voltage- and Transconductance-Mode Analog Filter Using Differential Difference Transconductance Amplifier. *Sensors.* 23, 1–16 (2023).
7. Khateb, F., Kumngern, M., Kulej, T., Akbari, M., Stopjakova, V: 0.5 V, nW-Range Universal Filter Based on Multiple-Input Transconductor for Biosignals Processing. *Sensors.* 22, 1–13 (2022).
8. Khateb, F., Kumngern, M., Kulej, T: 0.5-V 281-nW Versatile Mixed-Mode Filter Using Multiple-Input/Output Differential Difference Transconductance Amplifiers. *Sensors.* 24, 1–18 (2023).
9. Khateb, F., Kumngern, M., Kulej, T: 58-nW 0.5-V mixed-mode universal filter using multiple-input multiple-output OTAs. *IEEE Trans. Access.* 11, 130345–130357 (2023)



Operating Principles and Power Consumption of DB-OTAs

Paolo Faustini^(✉), Andrea Rosa, Luigi Colalongo, and Anna Richelli

Università degli Studi di Brescia, DII, 25123 Brescia, Italy

paolettafaustini@unibs.it

<https://www.unibs.it/it>

Abstract. This paper presents an analysis of digitally based analog amplifiers (DB-OTAs). The operating principle and the main mathematical relations of digitally based differential amplifiers are discussed along with an explanation of its operating regions and of the corresponding power consumption.

Keywords: digitally based amplifiers · ultra low power · CMOS integrated circuits

1 Introduction

Technology scaling favors digital circuits thanks to their high speed and low power dissipation. In this context, there is an increasing trend of radically rethinking analog functions in digital terms using only digital circuits. In [1] a differential amplifier, composed of only logic gates, was proposed. It has several appealing features, such as low power consumption, small area, easy design, and fast prototyping. It is an interesting approach, and a deep understanding of the possible topologies, designs, features, and limits is important for analog-background designers, who habitually use different design methodologies. This paper is focused on the understanding of the DB-OTA from both a circuital and mathematical standpoints, with particular emphasis on its power consumption which is one of its main appealing features. In Sect. 2, the operating principles, the transistors operating conditions, and the main mathematical relations required to design the DB-OTA are devised. In Sect. 3, the full design of the amplifier in 180 nm CMOS standard is shown, along with a comprehensive explanation of the operating regions and power consumption. In Sect. 4, some conclusions are drawn.

2 Operating Principle of the DB-OTA

The output of the digital buffers ($OUT+$, $OUT-$) is high (H) when the input voltages v_{i+} , v_{i-} are larger than the threshold voltage (V_M) and low (L) when

are lower than V_M . The CMFB (green box) adjusts the CM voltage v_{CM} : hence, $(OUT+, OUT-)$ are related to the differential voltage $v_D = v_{i+} - v_{i-}$. A detailed description of the DB-OTA, along with the basic mathematical relations, are reported in [1]. Here we recall: $v_{CM} = (v_{i+} + v_{i-})/2$, $v_{i\pm} = v_{CM} \pm v_D/2$ and, using a balanced resistor network, $v'_{i\pm} = (v_{i\pm} + v_{CM})/2$. Since the logic gates

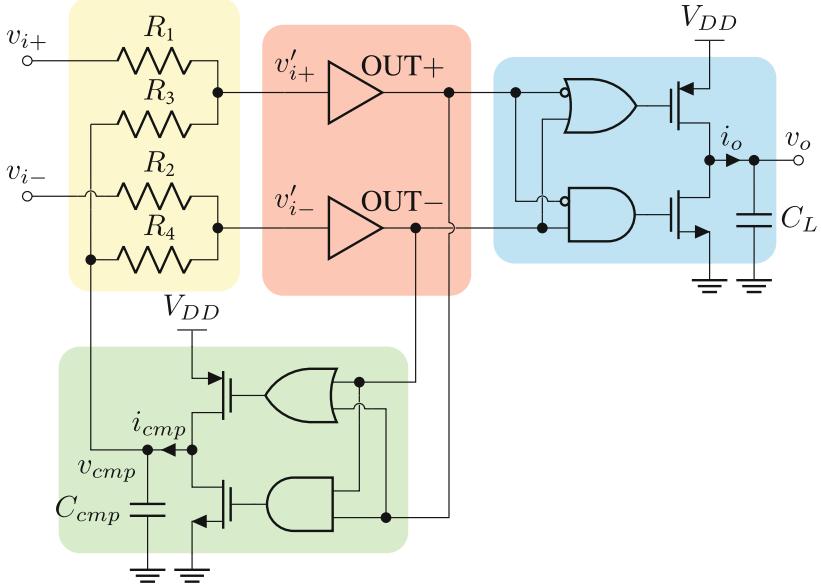


Fig. 1. Digitally based amplifier [1], resistor network (yellow box), digital buffers (pink box), output stage (blue box), CMFB (green box). $R_1 = R_2 = R_3 = R_4 = R$.

are assumed to switch much faster than the input signals of the DB-OTA, the output and CMFB voltages v_o e v_{cmp} are well approximated by the following first order differential equations:

$$\frac{dv_o(t)}{dt} = \frac{i_o(t)}{C_L}, \quad \frac{dv_{cmp}(t)}{dt} = \frac{i_{cmp}(t)}{C_{cmp}} \quad (1)$$

where $i_o(t) = \{ i_o^{pmos} \text{ if } [v'_{i+}(t_1) > V_M] \wedge [v'_{i-}(t_1) < V_M], -i_o^{nmos} \text{ if } [v'_{i+}(t_1) < V_M] \wedge [v'_{i-}(t_1) > V_M], 0 \text{ elsewhere } \}$, $i_{cmp} = \{ i_{cmp}^{pmos} \text{ if } [v'_{i+}(t_2) < V_M] \wedge [v'_{i-}(t_2) < V_M], -i_{cmp}^{nmos} \text{ if } [v'_{i+}(t_2) > V_M] \wedge [v'_{i-}(t_2) > V_M], 0 \text{ elsewhere } \}$, $t_1 = t - t_{D,o}$, $t_2 = t - t_{D,cmp}$ and $t_{D,o}$ and $t_{D,cmp}$ represent the propagation time through the logic gates. Furthermore, for the sake of simplicity, the logic gates are assumed ideal with the same propagation time $t_D = t_{D,o} = t_{D,cmp}$, and $i_o^{pmos} = i_o^{nmos} = I_o$, $i_{cmp}^{pmos} = i_{cmp}^{nmos} = I_{cmp}$ constant and not depending on v_o and v_{cmp} . Under those assumptions, in the following, the two possible operating conditions $v_D = 0$ and $v_D \neq 0$, will be discussed.

The waveforms are shown in Fig. 2 in the case of $v_D = 0$. When $v_D = 0$, $OUT+$, $OUT-$ are the same, the output inverter is in high impedance, v_o is constant and the load capacitor C_L holds its charge. Nevertheless, the compensation voltage v_{cmp} oscillates, in fact:

- At $t = 0$ both v'_{i+} and v'_{i-} cross V_M , and $OUT+$, $OUT-$ switch from L to H. It takes a certain amount of time t_D for the signal to propagate through the CMFB.
- Before t_D , although $OUT+$, $OUT-$ are high, the CM compensation inverter has not yet changed its state, and C_{cmp} is still charging with I_{cmp} as when $t = 0$.
- At $t = t_D$, the CMFB changes its state: the pull-down switches on, and the capacitor C_{cmp} is discharged with a constant current $-I_{cmp}$.
- From t_D to $2t_D$, while C_{cmp} is discharging, both v'_{i+} and v'_{i-} fall below the threshold V_M .
- At $2t_D$, $OUT+$, $OUT-$ switch from H to L;
- Before $3t_D$ the CM compensation inverter has not yet changed its state and C_{cmp} is still discharging.
- At $3t_D$ the CM compensation inverter changes state, the pull-up switches on, and the capacitor C_{cmp} is charged with the current I_{cmp} .
- This cycle is repeated every $T_{cmp} = 4t_D$.

Hence, the delay introduced by the compensation network t_D induces a triangular wave oscillation on v_{cmp} of period $4t_D$ and peak-to-peak amplitude $v_{cmp,pp} = 2t_D I_{cmp}/C_{cmp}$.

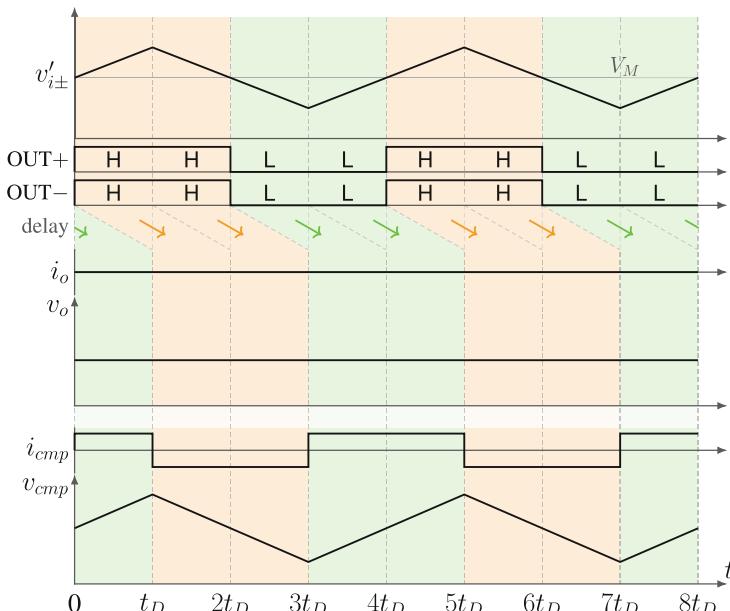


Fig. 2. Waveforms of the DB-OTA at $v_D = 0$, i.e. $v'_{i+} = v'_{i-}$.

In Fig. 3, the waveforms when $v_D > 0$ are shown, similar considerations hold when $v_D < 0$.

- The differential voltage v_D corresponds to a small mismatch between v'_{i+} and v'_{i-} that, in turn, causes v'_{i-} to cross the threshold voltage V_M with a small delay Δt_C ; during Δt_C , the differential voltage is positive, $v'_{i+} > v'_{i-}$, and the outputs ($OUT+$, $OUT-$) = (1, 0). After $2t_D$, it is v'_{i+} , that crosses the threshold voltage V_M with a small delay Δt_C respect to v'_{i-} .
- v_{cmp} is a triangular wave with the same period $T_{cmp} = 4t_D$, as in Fig. 2 but, during the interval Δt_C , the voltage is clamped since the buffer is in the high impedance region.
- During the interval Δt_C , the output buffer charges C_L and v_o steps up of $I_o \Delta t_C / C_L$.
- The charge on C_L is incremented by $I_o \Delta t_C$, twice every $T_{cmp} = 4t_D$.

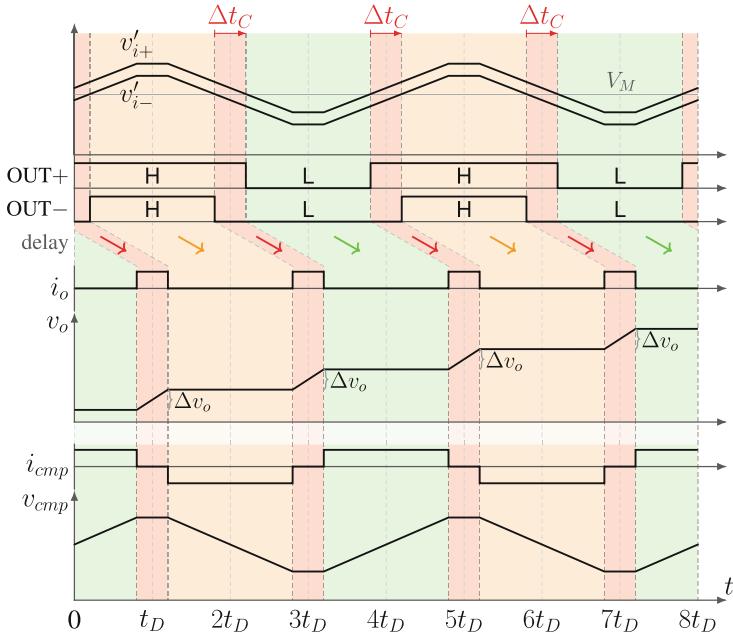


Fig. 3. Waveforms of the DB-OTA at $v_D > 0$, i.e. $v'_{i+} > v'_{i-}$.

In other words, the DB-OTA operates a double conversion from voltage to time and back from time to voltage again. The first conversion is v_D to Δt_C , thanks to the oscillation on v_{cmp} . Indeed, the mismatch on v'_{i+} and v'_{i-} is converted into a delay Δt_C , i.e. a time. Then, the output buffer converts the delay Δt_C

back into a voltage $\Delta v_o = I_o \Delta t_C / C_L$. The voltage gain of the DB-OTA in the frequency domain, assuming only the capacitive load C_L , reads:

$$A_D(f) = \frac{G_D(f)}{j2\pi f C_L} = \frac{\alpha}{j2\pi f 2t_D} e^{-j2\pi f t_D} \quad (2)$$

where $\alpha = I_o / C_L$,

$$G_D(f) = \frac{I_o(f)}{V_D(f)} \approx \frac{I_o}{2t_D} \frac{C_{cmp}}{I_{cmp}} e^{-j2\pi f t_D} \quad (3)$$

and $e^{-j2\pi f t_D}$ is the phase shift due to the propagation delay t_D . Furthermore, when $f \ll f_c/2$, Eq. (2) can be simplified as $A_D(f) \approx \alpha / (j2\pi f 2t_D)$. Thus, the transfer function is equivalent to an integrator with a unity gain frequency of $f_u = \alpha / (4\pi t_D)$. Digitally based analog amplifier can be used, almost as conventional analog amplifiers, in feedback loops. Nevertheless, the classical assumptions of infinite input impedance ($Z_i \rightarrow \infty$) and negligible output impedance ($Z_o \rightarrow 0$) are not properly verified. The transfer function can be approximated as:

$$G(f) = \frac{V_o(f)}{V_i(f)} = \frac{1/\beta}{1 + j2\pi f / (\beta f_u)} \quad (4)$$

where β is the gain of the feedback network set by the resistors' ratio. In other words, the DB-OTA operates as a first order system.

3 Design and Simulations of the DB-OTA

Digitally based amplifier discussed in the previous section has been designed in the standard 180 nm UMC (United Microelectronic Corporation) CMOS process and extensively simulated in different operating conditions. It is worth noting that the final schematic is slightly modified with respect to the base circuit of Fig. 1 to equalize the propagation time of $OUT+$ and $OUT-$. The circuit is extremely simple, composed only of resistors and logic gates. The supply voltage is standard for this technology (1.8 V) at the aim of investigate the DB-OTA in normal operating conditions. Several simulations worked out at lower supply voltages show that the DB-OTA operates correctly at supply as low as 400 mV. The capacitive load is assumed of 10 pF. It is a fair value to account for typical operating conditions of the DB-OTA i.e. the parasitic effects of the pad, of the bonding, of the package, or of the subcircuits connected as load. A buffer should be included if the DB-OTA is connected to a bulky load. The DB-OTA can hardly be simulated by means of the classical small-signal AC analysis tools since the core of its operating principle is digital and is related to the oscillation of v_{cmp} . Time-expensive transient analysis are required to design and characterize the amplifier. The DB-OTA has been simulated in two different configurations: open loop as a comparator, and closed loop as a feedback amplifier.

Open Loop. The amplifier is operated as a comparator. In the simulations, to generate a modulated differential voltage v_D that emphasizes all the different operating regions of the amplifier, we used two input sinusoidal signals v_{i+} and v_{i-} of amplitude V_{DD} with different frequencies: v_{i+} 10 kHz, v_{i-} 30 kHz. The transient simulation time is 100 μ s. The waveforms of the most relevant voltages of the internal nodes are shown in Fig. 4: the bottom x-axis represents the simulation time, the top x-axis the operating regions, the y-axis the voltages at the nodes. In Fig. 5, one can see that the DB-OTA has five distinct behaviors that we call operating regions 1–5:

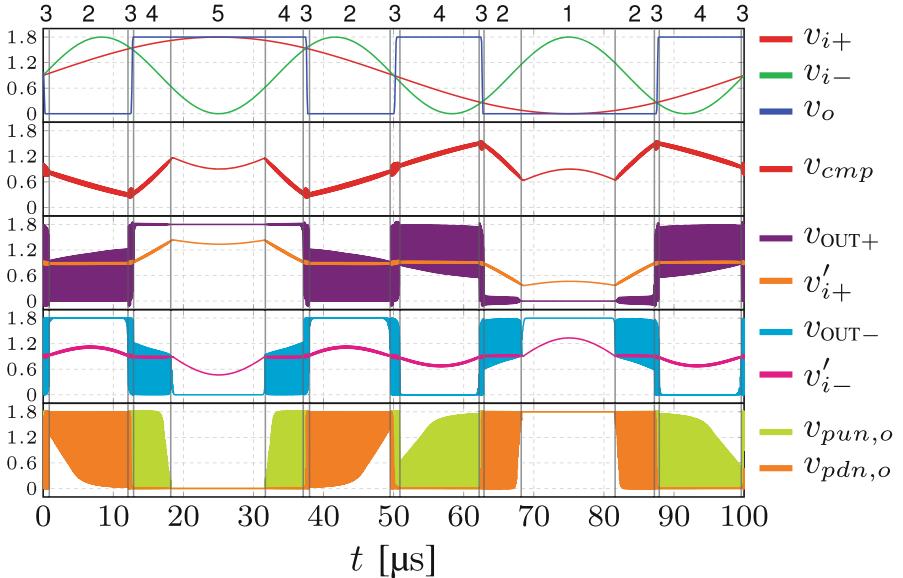


Fig. 4. Open loop: input/output waveforms and intermediate node voltages

- In the regions 1 and 5, the differential voltage v_D is large, $v_{i\pm}$ are well separated and opposite with respect to the logic threshold V_M . In these regions the output voltage saturates to V_{DD} or 0, the common-mode compensation network is not active and only the pull-up or the pull-down of the output inverter turns on. In Fig. 4, $v_{pun,o}$, $v_{pd़n,o}$ are the gate voltages of the pull-up and pull-down respectively. In Fig. 6, the regions 1 and 5 are limited by the equations $|v'_{i+}| < V_M$ and $|v'_{i-}| > V_M$:

$$v'_{i+} = \frac{v_{i+} R_3 + v_{cmp} R_1}{R_1 + R_3} \quad (5)$$

$$v'_{i-} = \frac{v_{i-} R_4 + v_{cmp} R_2}{R_2 + R_4} \quad (6)$$

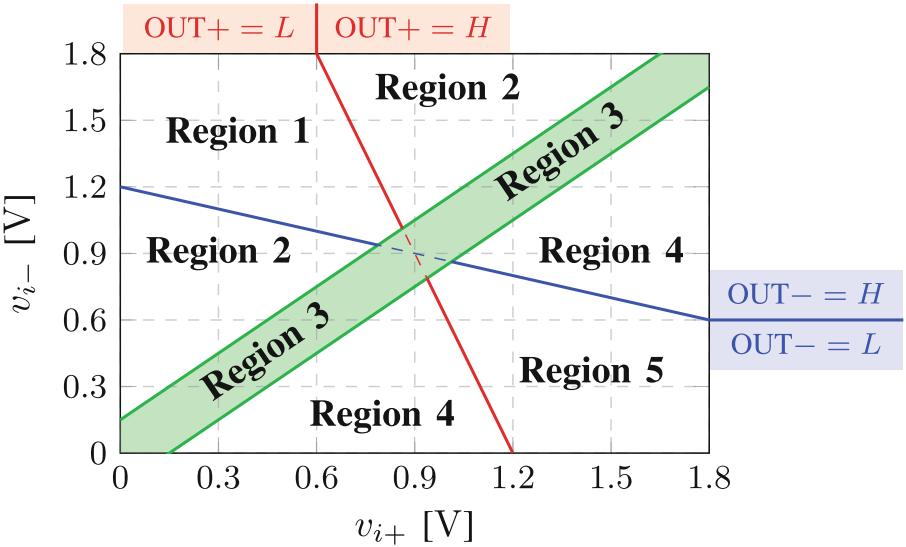


Fig. 5. Open loop: operating regions vs. $v_{i\pm}$

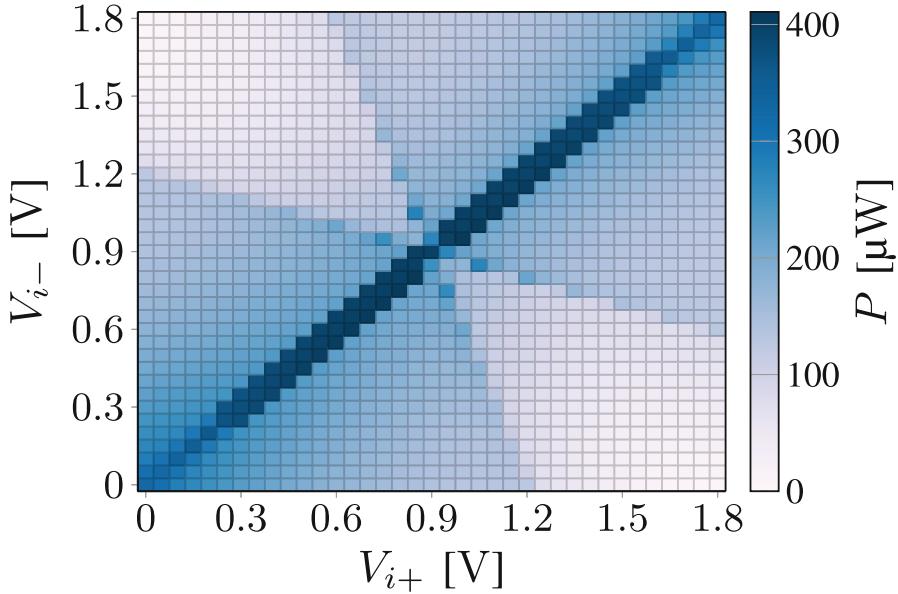


Fig. 6. Open loop: power consumption vs. $v_{i\pm}$

Furthermore, since the CMFB is not active $v_{cmp} = v_{CM}$, i.e. $(v_{i+} + v_{i-})/2$, the regions 1 and 5 reads:

$$v'_{i+} = \frac{v_{i+} + v_{CM}}{2} = \frac{3}{4} v_{i+} + \frac{1}{4} v_{i-} \quad (7)$$

$$v'_{i-} = \frac{v_{i-} + v_{CM}}{2} = \frac{1}{4}v_{i+} + \frac{3}{4}v_{i-} \quad (8)$$

- In the region 3, the differential voltage v_D is small enough to activate the CMFB. The compensation voltage v_{cmp} oscillates and the digital outputs $OUT+$ and $OUT-$ commute between L and H. Both the pull-up and the pull-down of the output inverter are active: if v_D is positive, v_o steps up, if v_D is negative, v_o steps down. This region is defined by the condition $\Delta t_C < t_D$ i.e. $v_D < I_{cmp}/C_{cmp} t_D$
- In the regions 2 and 4, the differential voltage v_D is small, but not as small as in the region 3. In the region 2 $v_D < 0$, $OUT+$ holds the low logic state, while $OUT-$ quickly commutes from H to L due to the CMFB. The pull-down of the output stage switches on. In the region 4 $v_D > 0$, $OUT-$ holds the low logic state, while $OUT+$ quickly commutes from H to L due to the CMFB. The pull-up of the output stage switches on. Hence, the pull-up or the pull-down switches on, but are not always active as in region 1 and 5.

The power consumption of the DB-OTA is mostly dynamic and is due to the switching of the gates (P_{gates}), to the charging and discharging of C_{cmp} (P_{cmp}) and C_L (P_o). It strongly depends on the operating regions of the amplifier as shown in Fig. 6: the dissipated power, as a function of the differential voltage, is represented as a shade of blue from light (lower power consumption) to dark (higher power consumption). The x- and the y-axis are the input voltages $v_{i\pm}$, ranging from 0 to V_{DD} in steps of 50 mV. It is worth adding, that the simulations are worked out at 1.8 V (standard for this technology): if the voltage supply is reduced, the power consumption gets remarkably smaller, [2-6]. This is due both to the dependence of the dynamic power on V_{DD} and to the reduction of the switching frequencies of the CMFB and of the output stage. In the regions 1 and 5, the power dissipation is lower than in the region 2, 3, 4, since the common mode compensation network is always switched off, only the pull-up or pull-down is conducting, and the output voltage saturates to V_{DD} or 0. In the regions 2 and 4 the power dissipation is higher since the CMFB is active. Finally in the region 3 the power consumption reaches its maximum since the differential voltage is small and v_{cmp} oscillates continuously.

Closed Loop. The DB-OTA can be used in feedback connection as an analog amplifier. In the simulations of the closed loop connection a sinusoidal rail-to-rail input signal of 20 kHz is applied to the non-inverting input v_{i+} . The simulation time is 100 μ s. The Fast Fourier Transform (FFT) of the buffer connection with unitary loop gain (G) is 0.992, the phase delay (φ) 0.08°, and a total harmonic distortion (THD) 0.23%. Figure 7 show that, when the DB-OTA is used as a buffer, the differential voltage v_D is very small and always operates in the region 3. Hence, despite the rather good overall performances, the power consumption reaches its maximum.

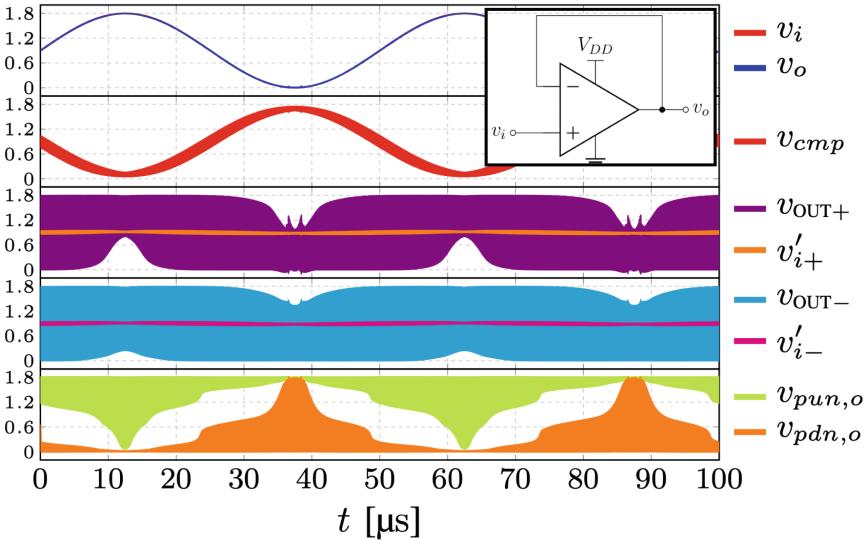


Fig. 7. Buffer: input/output waveforms and internal node voltages

4 Conclusions

Digitally based analog amplifier has been designed and investigated along with its main mathematical relations. We have shown that the amplifier can operate in 5 different regions and that the power consumption peaks when v_D is small. Several simulations have been worked out both in the open and closed loop configuration. The simulations show that the amplifier represents a really attractive approach for the signal conditioning of the integrated circuits with advantages on power consumption and ease of design. The amplifier is better suited for low to medium frequency input signals with rather large amplitude. Nevertheless, it represents a very appealing architecture when the area on chip and the power dissipation are of paramount importance.

References

1. Crovetti, P.S.: A digital-based analog differential circuit. *IEEE TCAS-I*. **60**(12), 3107–3116 (2013). <https://doi.org/10.1109/TCSI.2013.2255671>
2. Toledo, P., Crovetti, P., Aiello, O., Alioto, M.: Fully digital rail-to-rail OTA with sub-1000- μm^2 area, 250-mV minimum supply, and nW power at 150-pF Load in 180 nm. *IEEE Solid-State Circ. Lett.* **3**, 474–477 (2020)
3. Toledo, P., Crovetti, P., Aiello, O., Alioto, M.: Design of digital OTAs with operation down to 0.3 V and nW power for direct harvesting. *IEEE Trans. Circ. Syst. I: Regular Papers* **68**(9), 3693–3706 (2021)
4. Toledo, P., Crovetti, P., Klimach, H., Bampi, S., Aiello, O., Alioto, M.: A 300 mV-supply, sub-nW-power digital-based operational transconductance amplifier. *IEEE Trans. Circ. Syst. II Express Briefs* **68**(9), 3073–3077 (2021)

5. Richelli, A., Faustini, P., Rosa, A., Colalongo, L.: An investigation of the operating principles and power consumption of digital-based analog amplifiers. *J. Low Power Electron. Appl.* **13**, 51 (2023). <https://doi.org/10.3390/jlpea13030051>
6. Toledo, P., Crovetti, P.S., Klimach, H.D., Musolino, F., Bampi, S.: Low-voltage, low-area, nW-Power CMOS digital-based biosignal amplifier. *IEEE Access* **10**, 44106–44115 (2022)

Micro- and Nano-Electronic Devices



Semi-analytical Model for the Estimation of the Subthreshold Swing in Dirac-Source FETs

Tommaso Ugolini^(✉), Giorgio Baccarani, and Elena Gnani

ARCES and DEI, University of Bologna, Viale Risorgimento 2, 40136 Bologna, Italy
tommaso.ugolini2@unibo.it

Abstract. A 2D analytical model for the potential profile in the semiconductor channel of two-dimensional (2D) Dirac-Source (DS) FETs is worked out and compared with a rigorous numerical solution of Poisson's equation. This analytical solution holds validity in weak inversion and enables a precise assessment of the subthreshold swing (SS) under the constraint of ballistic transport. When the device is biased in strong inversion, instead, a semi-empirical approach is worked out, which accounts for the correct potential in the middle of the channel and at the source and drain boundaries. Extensive comparisons between the analytical model and numerical results are carried out on the resulting conduction-band profiles, device characteristics and subthreshold swings. Different device geometries (gate length and oxide thickness) and morphologies (gate dielectric) are widely evaluated. This study confirms the effectiveness of DS-FETs as high-efficiency electronic switches, showing a minimum SS well below 60 mV/dec and a reasonable on-state current.

Keywords: Dirac-source field-effect transistor (DS-FET) · Potential profile · Analytical model

1 Introduction

The need to lower power consumption in integrated circuits requires a scaling down of the supply voltage. This goal can only be achieved with no performance penalty of logic gates by lowering the subthreshold swing (SS) of the transistor turn-on characteristics. Several approaches have been suggested in the last decade to achieve this goal, but none of them has proved to be competitive with the leading-edge CMOS technology.

One of the most promising device concepts recently proposed in the literature to overcome the 60 mV/dec limit is the 2D DS-FET [1–4] (see, Fig. 1). This transistor leverages the Dirac cone in the density of states of graphene to filter out high-energy electrons injected into the channel, leading to a reduced effective injected carrier temperature and to a subthreshold swing well below 60 mV/dec. At the same time, the on-state current is not severely affected by low-transmission tunneling probability as for band-to-band tunneling FETs.

In this work we develop a 2D semi-analytical solution of the Poisson equation within the channel of the 2D transistor. This solution allows us to understand the

impact of geometrical and morphological parameters on the device electrostatics, which directly impacts carrier transport. The knowledge of band profiles is necessary to extract the transmission probability required to compute the current under the assumption of ballistic transport. The device characteristics are then computed and SS is calculated for different channel lengths and gate-insulating materials.

Extensive comparisons are presented of the conduction band profiles, turn-on characteristics and subthreshold swings provided by the analytical model and by numerical results for different insulating materials, gate-oxide thicknesses and gate lengths. The obtained results confirm that an SS smaller than 60 mV/dec over three orders of magnitude in current can be achieved with a suitable device design.

2 Poisson's Equation in the 2DSC Channel

We consider a 2D transistor with a monolayer MoS₂ as a channel material. The limited thickness of the two-dimensional semiconductor layer makes it reasonable to approximate the charge distribution in the channel with a delta-function. Consequently, Poisson's equation simplifies to the Laplace equation within the oxide region

$$\frac{\partial^2 \phi}{\partial x^2} + \frac{\partial^2 \phi}{\partial z^2} = 0 \quad (1)$$

with $\phi(x, z)$ the electrostatic potential. The vertical coordinate x originates from the channel and extends towards the gate, while z represents the direction of the current flux and is defined within the interval $\{0, L_g\}$. The device is assumed to be uniform in the y direction. When solving Eq. (1), the charge appears just as a non-homogeneous Neumann boundary condition.

In weak inversion, the boundary conditions can be defined as

$$\Phi(t_{\text{ox}}, z) = 0 \quad (2a)$$

$$\Phi(x, 0) = (\phi_{c1} - \phi_g)(1 - x/t_{\text{ox}}) \quad (2b)$$

$$\Phi(x, L_g) = (\phi_{c2} - \phi_g)(1 - x/t_{\text{ox}}) \quad (2c)$$

$$\left. \frac{\partial \Phi}{\partial x} \right|_{x=0} \simeq 0 \quad (2d)$$

where $\Phi(x, z) = \phi(x, z) - \phi_g$, $\phi_g = V_{\text{GS}} - V_{\text{FB}}$ is the effective gate potential, and $\phi_{c1,2}$ are the potentials at the source and drain ends of the channel, respectively. Conditions (2b), (2c) are justified by the typical device form factor, where the gate oxide is usually much thinner than the gate length, i.e., $t_{\text{ox}} \ll L_g$. The potential is thus assumed to vary linearly along the left and right edges [5].

Equation (1) can be addressed by separation of the variables, namely, by setting $\Phi(x, z) = \alpha(x)\beta(z)$. The Laplace equation then becomes

$$\frac{1}{\alpha} \frac{\partial^2 \alpha}{\partial x^2} + \frac{1}{\beta} \frac{\partial^2 \beta}{\partial z^2} = 0 . \quad (3)$$

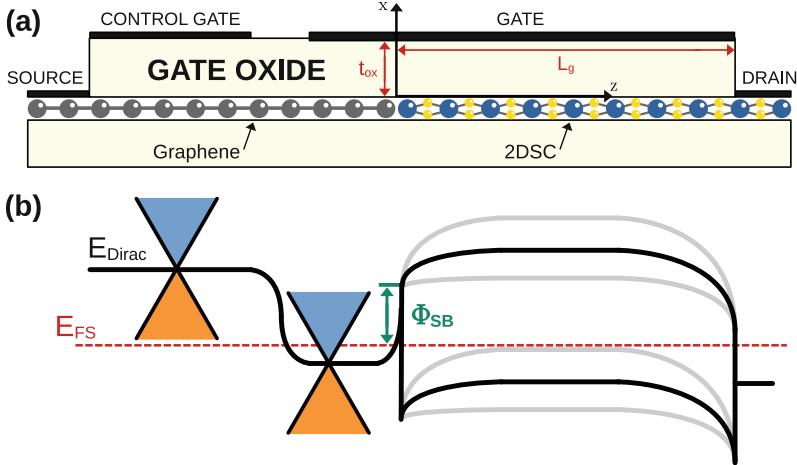


Fig. 1. (a) Device structure. The control gate electrode is used to properly align in energy the Dirac cone of graphene so to maximize the filtering effect. (b) Schematic band diagram showing the density of states of graphene and the conduction and valence bands of the semiconductor. The n-doped graphene region is used to lower the channel barrier with respect to the source Fermi level. ϕ_{SB} is the barrier height at the heterojunction.

The above relation contains two terms, one dependent only on x and the other dependent only on z , both of them constant and opposite in sign. Hence, we can find independent solutions of the kind

$$\alpha_n(x) = C_n \sin(k_n x) + D_n \cos(k_n x), \quad (4a)$$

$$\beta_n(z) = A_n \sinh(k_n z) + B_n \cosh(k_n z). \quad (4b)$$

Having set $k_n = \alpha_n/t_{\text{ox}}$, the Fourier series representation of (2b), (2c) can be expressed as

$$\Phi(x, 0) = (\phi_{c1} - \phi_g) \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{\cos(\alpha_n x/t_{\text{ox}})}{(1+2n)^2} \quad (5a)$$

$$\Phi(x, L_g) = (\phi_{c2} - \phi_g) \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{\cos(\alpha_n x/t_{\text{ox}})}{(1+2n)^2} \quad (5b)$$

where $\alpha_n = (1+2n)\pi/2$. From the above conditions, the solution is found to be

$$\begin{aligned} \Phi(x, z) &= (\phi_{c1} - \phi_g) \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{\cos(\alpha_n x/t_{\text{ox}})}{(1+2n)^2} \frac{\sinh(\alpha_n(L_g - z)/t_{\text{ox}})}{\sinh(\alpha_n L_g/t_{\text{ox}})} \\ &\quad + (\phi_{c2} - \phi_g) \frac{8}{\pi^2} \sum_{n=0}^{\infty} \frac{\cos(\alpha_n x/t_{\text{ox}})}{(1+2n)^2} \frac{\sinh(\alpha_n z/t_{\text{ox}})}{\sinh(\alpha_n L_g/t_{\text{ox}})}. \end{aligned} \quad (6)$$

The above relation satisfies the boundary conditions (5a) and (5b). In fact, when $z = 0$, the second term vanishes, while the ratio of hyperbolic sines in the first term becomes equal to 1. Besides, when $z = L_g$, the first term vanishes and the ratio of the hyperbolic sines in the second term becomes equal to 1. Therefore, Eq. (6) reduces to the boundary conditions (5) for $z = 0$ and $z = L_g$, respectively.

Equation (6) can be conveniently rewritten in the following form

$$\Phi(x, z) = \sum_{n=0}^{\infty} \left(A_n \frac{\sinh(\alpha_n(L_g - z)/t_{\text{ox}})}{\sinh(\alpha_n L_g/t_{\text{ox}})} + B_n \frac{\sinh(\alpha_n z/t_{\text{ox}})}{\sinh(\alpha_n L_g/t_{\text{ox}})} \right) \cos(\alpha_n x/t_{\text{ox}}) \quad (7)$$

having defined

$$A_n = \frac{8}{\pi^2} \frac{\phi_{c1} - \phi_g}{(1 + 2n)^2} \quad B_n = \frac{8}{\pi^2} \frac{\phi_{c2} - \phi_g}{(1 + 2n)^2} . \quad (8)$$

The derivative of Φ with respect to x thus becomes

$$\frac{\partial \Phi}{\partial x} = -\frac{1}{t_{\text{ox}}} \sum_{n=0}^{\infty} \phi_{cn}(z) \alpha_n \sin(\alpha_n x/t_{\text{ox}}) \quad (9)$$

having defined

$$\phi_{cn}(z) = A_n \frac{\sinh(\alpha_n(L_g - z)/t_{\text{ox}})}{\sinh(\alpha_n L_g/t_{\text{ox}})} + B_n \frac{\sinh(\alpha_n z/t_{\text{ox}})}{\sinh(\alpha_n L_g/t_{\text{ox}})} . \quad (10)$$

Equation (9) clearly vanishes for $x = 0$, in accordance with condition (2d). Finally, the potential in the channel of infinitesimal thickness can be expressed as

$$\phi_c(z) = \phi_g + \Phi(0, z) = \phi_g + \sum_{n=0}^{\infty} \phi_{cn}(z) . \quad (11)$$

Importance must be given to the fact that, when the charge per unit area in the channel becomes relevant, condition (2d) is no longer fulfilled. Thus, it is essential to replace it with the more realistic one:

$$\varepsilon_{ox} \frac{\partial \phi}{\partial x} \Big|_{x=0} = -Q_n(z) = qN_{2D} \ln \left\{ 1 + \exp \left(\frac{q[\phi_c(z) - \phi_N]}{k_B T} \right) \right\} \quad (12)$$

where $Q_n(z)$ is the charge density per unit surface, ϕ_N is the Fermi pseudopotential for electrons and N_{2D} is the effective density of states of a two-dimensional gas

$$N_{2D} = g_c \frac{2(2\pi m^* k_B T)}{h^2} = g_c \frac{m^* k_B T}{\pi \hbar^2} . \quad (13)$$

In the above relation, g_c is the number of minima in the conduction band of the 2DSC. For long channel transistors is possible to identify an analytical one-dimensional solution. This one, in turn, would be valid everywhere except in the

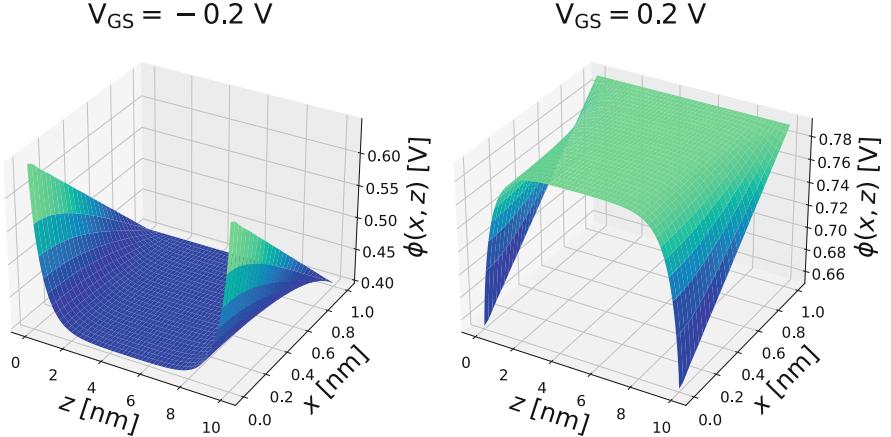


Fig. 2. Two-dimensional representation of the equilibrium potential profile at two different gate voltages, namely $V_{GS} = -0.2$ V (left plot) and $V_{GS} = 0.2$ V (right plot). $\phi_{SB} = 0.25$ eV and $E_c - E_{FS} = 0.3$ eV at $V_{GS} = 0$ V are assumed. The device under consideration has $L_g = 10$ nm and $t_{ox} = 1$ nm. As noticeable, all boundary conditions (2) are satisfied.

proximity of source and drain contacts. To proceed, if it is $\ddot{\phi}_z \ll \ddot{\phi}_x$, the solution to the one-dimensional Laplace equation is

$$\phi(x, z) = \phi_c(z) + [\phi_g - \phi_c(z)] \frac{x}{t_{ox}} . \quad (14)$$

The consideration of (12) and (14) leads to the following relation

$$\phi_g - \phi_c = q \frac{N_{2D}}{C_{ox}} \ln \left[1 + \exp \left(\frac{q(\phi_c - \phi_N)}{k_B T} \right) \right] \quad (15)$$

which reduces to

$$\phi_g - \phi_c = q \frac{N_{2D}}{2C_{ox}} \left\{ \ln \left[1 + \exp \left(\frac{q(\phi_c - \phi_{FS})}{k_B T} \right) \right] + \ln \left[1 + \exp \left(\frac{q(\phi_c - \phi_{FD})}{k_B T} \right) \right] \right\} \quad (16)$$

in case of ballistic transport. Equation (16) accounts for the fact that electrons with positive velocity are only those coming from the source, and the ones with negative velocity are only those coming from the drain. Note that we have chosen $\phi_{FS} = \phi_N(0)$. By replacing ϕ_c with the saturation value of the electric potential at mid-channel $\phi_{cm}^{(LC)}$ in Eq. (16), we can extract by an iterative procedure $\phi_{cm}^{(LC)}$, whose value holds in strong as well as in weak inversion.

The electric potential $\phi_c(z)$ then becomes

$$\phi_c(z) = \phi_{cm}^{(LC)} + \sum_{n=0}^{\infty} \phi_{cn}(z) \quad (17)$$

where the coefficients A_n and B_n in Eq. (10) are now defined as

$$A_n = \frac{8}{\pi^2} \frac{\phi_{c1} - \phi_{cm}^{(LC)}}{(1 + 2n)^2} \quad B_n = \frac{8}{\pi^2} \frac{\phi_{c2} - \phi_{cm}^{(LC)}}{(1 + 2n)^2}. \quad (18)$$

Figure 2 shows two potential profiles calculated using the above relations. In addition, please note that (17) is a very general solution, which holds both in subthreshold and in strong-inversion.

The boundary conditions (2b), (2c) indicate that we assume Schottky contacts at the source and drain ends of the channel. In fact, ϕ_{c2} is a constant for an assigned drain voltage. On the other hand it may be worth pointing out that, if the DS-FET is considered as a whole (including the heterojunction region between graphene and the 2DSC), ϕ_{c1} should depend on the voltage applied to the gate contact. Nevertheless, this investigation is beyond the scope of the present paper. We therefore evaluate the impact of different barrier heights at the heterojunction as was previously done in Refs. [3,4]. From now on, the conduction band at the beginning of the channel $E_c(0)$ is considered as a parameter fixing the height of the Gr-2DSC barrier $\phi_{SB} = E_c(0) - E_{FS}$.

To conclude, we emphasise that the approach used here can be simply extended to double-gate FETs by considering a doubled amount of charge in (12) for an assigned gate voltage.

3 Current Calculation

In the ballistic limit, the current in a DS-FET is given by the Landauer equation [3]

$$I \simeq \frac{2q}{h} \int_{E_{cm}}^{\infty} M_{Gr}(E) T(E) [f(E - E_{FS}) - f(E - E_{FD})] dE, \quad (19)$$

where E_{cm} is the minimum value of the conduction band edge in the semiconductor channel, $M_{Gr}(E)$ is the number of modes in graphene [3], $T(E)$ the tunneling probability, and $f(E - E_{FS,D})$ the charge distribution function at the source and drain contacts. In Eq. (19) graphene is considered through its number of conducting channels $M_{Gr}(E) = W 2|E - E_{Dirac}|/\pi\hbar v_F$, which is lower than that of the 2DSC in the relevant energy range, while the semiconductor acts as an adjustable energy barrier.

In our implementation, the term $T(E)$ contains only the transmission probability at the Gr-2DSC heterojunction, while the tunneling probability at the Gr-Gr junction is considered equal to 1 (this assumption is justified by the Klein tunneling effect [6]). $T(E)$ is then computed using the WKB method, with the band profiles coming from Eq. (17).

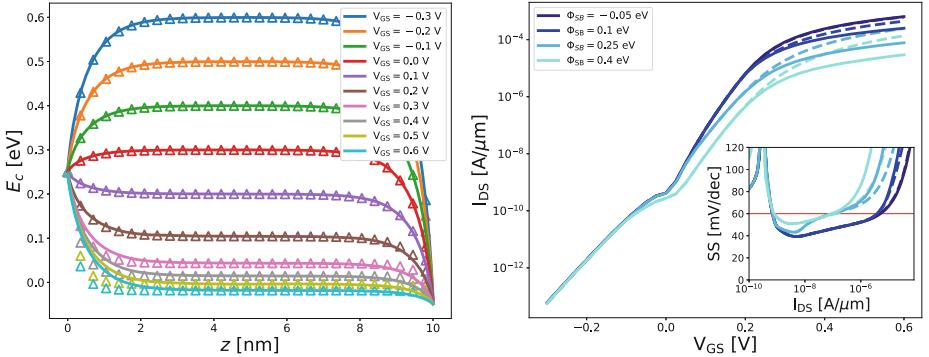


Fig. 3. Conduction band profiles in the **Fig. 4.** Current characteristics and SS for lateral direction z at different gate voltages V_{GS} , with $V_{DS} = 0.3$ V and $\phi_{SB} = 0.25$ eV. Solid lines: I_{DS} with bands of the analytical model. Symbols: analytical model eq. (17). Dashed lines: numerical solution. The device under consideration is 10 nm long, with a 1-nm layer of SiO₂ gate oxide. Numerical results show steeper profiles in the proximity of contacts than analytical ones. As expected from fig. 3, the tunneling probability is larger for steeper profiles (numerical case), resulting in higher saturation current values.

some barrier heights ϕ_{SB} with $V_{DS} = 0.3$ V. Solid lines: I_{DS} with bands of the numerical solution. The device under consideration is 10 nm long, with a 1-nm layer of SiO₂ gate oxide. As expected from fig. 3, the tunneling probability is larger for steeper profiles (numerical case), resulting in higher saturation current values.

4 Results

In our simulations we have considered molybdenum disulfide (MoS₂) as the semiconductor monolayer, whose main parameters are reported in [3]. Furthermore, the Dirac point in the graphene region underlying the control gate (p-doped) is fixed at $E_{\text{Dirac}} = 0.3$ eV, resulting in a leakage current slightly below $10^{-9} \text{ A}/\mu\text{m}$ at $V_{GS} = 0$ V. References are taken so as to guarantee the alignment of the conduction band of the 2DSC with the Dirac energy of the p-Gr region when a zero gate voltage is applied, i.e. $E_{\text{cm}} - E_{\text{FS}} = E_{\text{Dirac}}$ at $V_{GS} = 0$ V.

Figure 3 shows the conduction band profiles E_c in the MoS₂ channel of a silicon-dioxide insulated DS-FET, for some values of the gate voltage V_{GS} . The SiO₂ thickness $t_{\text{ox}} = 1$ nm and the semiconductor channel length $L_g = 10$ nm. Here, curves from the semi-analytical model (solid lines) are compared with those coming from a rigorous numerical solution of the Poisson equation (symbols). In the subthreshold regime ($V_{GS} < 0.2$ V) the profiles coincide, confirming the validity of the model. On the other hand, under strong-inversion conditions, we incur in some discrepancies between the two solutions in proximity of the contacts, where the presence of charge cannot be neglected.

Next, we compute the current and the SS from the aforementioned profiles. Results are reported in Fig. 4. As expected, the device characteristics start differing when the inversion regime is approached. More specifically, for the same Schottky barrier height ϕ_{SB} , the ON-state current computed from the analytical

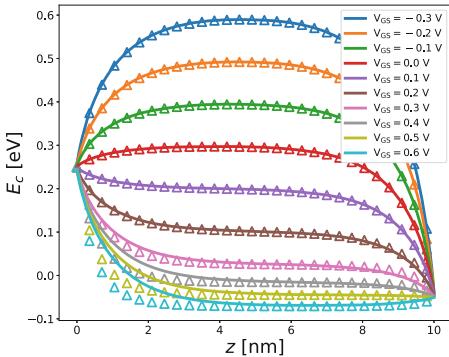


Fig. 5. Conduction band profiles in the lateral direction z at different gate voltages with $V_{DS} = 0.3$ V and $\phi_{SB} = 0.25$ eV. Solid lines: analytical model. Symbols: numerical solution. The device under consideration is 10 nm long, with a HfO₂ gate insulator having a thickness $t_{ox} = 1.8$ nm. This device operates closer to the onset of short-channel effects, but the band profiles coincide in subthreshold, while differing slightly in strong inversion, in the region between the source contact and mid-channel.

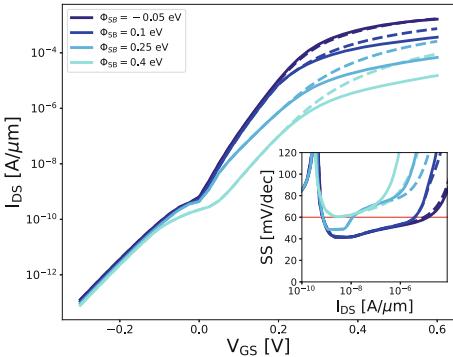


Fig. 6. Current characteristics and SS for some barrier heights ϕ_{SB} with $V_{DS} = 0.3$ V. Solid lines: I_{DS} with analytical band profiles from eq. (17). Dashed lines: I_{DS} with bands from the numerical solution. The device under consideration is 10 nm long, with a HfO₂ gate insulator having a thickness $t_{ox} = 1.8$ nm. The current curves are not severely influenced by the increased short-channel effect, but SS is slightly degraded, especially at the highest barrier heights, due to the thicker HfO₂ insulator.

profiles (solid curves) turns out to be lower than that obtained from numerically evaluated profiles (dashed curves). This happens due to the increased tunneling probability resulting from the numerical profiles, in view of the sharper transition of the conduction band edge next to the contacts. As is visible from the inset, the difference in current also affects SS in strong inversion.

Subsequently, in order to investigate the impact of high-k dielectrics as gate oxides, we changed the gate insulator from SiO₂ to HfO₂ while reducing the EOT to 0.32 nm, i.e. $t_{ox} \simeq 1.8$ nm. Resulting band profiles are visible in Fig. 5. The curves are smoother in this case. This is attributable to a larger fringing field due to the increased physical thickness of HfO₂ ~ 1.8 times higher than that of SiO₂ [7]. However, we would like to emphasize that the two simulation approaches give the same results in subthreshold and are very similar in the inversion regime. As in the previous cases, we then compute the current and SS (Fig. 6). From the inset we can notice that an SS lower than 60 mV/dec can still be reached. This confirms high-k dielectrics as a valuable alternative to SiO₂.

Finally, we considered a reduced semiconductor channel length of 5 nm (Figs. 7 and 8). In this configuration there is a higher leakage current attributable to source-to-drain tunneling. However, despite the minimal channel length, performance is not significantly degraded.

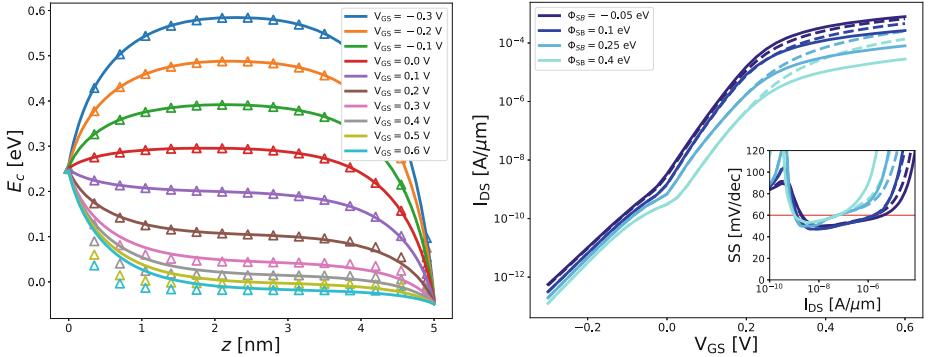


Fig. 7. Conduction band profiles in the lateral direction z at different gate voltages V_{GS} with $V_{DS} = 0.3$ V and $\phi_{SB} = 0.25$ eV. Solid lines: analytical model. Symbols: numerical solution. The device under consideration is 5 nm long, with a 1-nm of SiO₂ gate oxide. This device operates at the onset of short-channel effects, but the band profiles coincide in subthreshold, while differing somewhat in strong inversion, in the mid-channel.

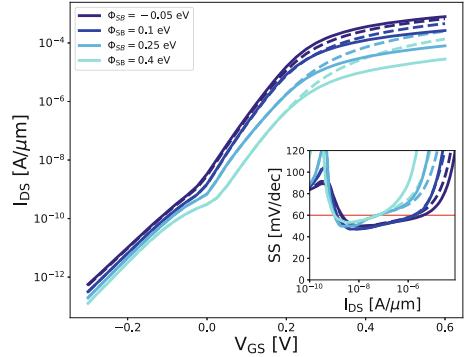


Fig. 8. Current characteristics and SS for some barrier heights ϕ_{SB} with $V_{DS} = 0.3$ V. Solid lines: I_{DS} computed with bands from the analytical model Eq. (17). Dashed lines: I_{DS} with bands computed from the numerical solution. The device under consideration is 5 nm long, with a 1-nm layer of SiO₂ gate oxide. A shortened channel length causes source-to-drain tunneling, resulting in an increased current in the OFF state and a degraded SS.

To conclude we observe that the use of high-k dielectrics can introduce short-channel effects in the same manner as a reduction of the channel length would do. Indeed, as we could have noticed from the analytical model in weak inversion (Eq. 6), where the gate oxide dielectric constant ϵ_{ox} does not appear, the change in the gate dielectric is taken into account through the resulting modification in the transistor geometric parameters.

5 Conclusions

In this work we propose an analytical 2D solution of Laplace equation within the oxide of SOI DS-FETs. The model is rigorous under weak inversion conditions, but fails to predict the appropriate potential value within the channel in strong inversion. In order to account for the quasi-saturation of the surface potential in the latter condition, a semi-empirical approach is pursued based on the computation of the surface potential for a long-channel FET under the gradual-profile approximation. The resulting semi-empirical model turns out to be correct at mid-channel and at the contacts, but exhibits some discrepancies with respect to numerical simulation results within the transition regions between mid-channel and the contacts.

The device turn-on characteristics are then computed for different device geometries (gate length and oxide thickness) and morphologies (low-k and high-

k dielectrics) and the corresponding subthreshold swings are extracted. This work confirms that an SS smaller than 60 mV/dec can be sustained over three orders of magnitude of drain current for a well-designed DS-FET. One major conclusion is that, so long as the device operates in weak inversion, the oxide permittivity plays no role, while its physical thickness does. Therefore, the use of high-k dielectrics with an increased oxide thickness degrades short-channel effects and increases SS. High-k dielectrics can only improve the ON-state current at given gate and drain voltages so long as their physical thickness is not much increased with respect to that of SiO₂.

Acknowledgements. This research was supported by the Horizon Europe programme, Attoswitch project (GA 101135571, www.attoswitch.eu).

References

1. Qiu, C., et al.: Dirac-source field-effect transistors as energy-efficient, high-performance electronic switches. *Science* **361**(6400), 387–392 (2018). <https://doi.org/10.1126/science.aap9195>
2. Liu, F., et al.: Dirac electrons at the source: breaking the 60-mV/decade switching limit. *IEEE Trans. Electron Devices* **65**(7), 2736–2743 (2018). <https://doi.org/10.1109/TED.2018.2836387>
3. Wu, P., Appenzeller, J.: Design considerations for 2-D dirac-source FETs-part I: basic operation and device parameters. *IEEE Trans. Electron Devices* **69**(8), 4674–4680 (2022). <https://doi.org/10.1109/TED.2022.3181544>
4. Wu, P., Appenzeller, J.: Design considerations for 2-D dirac-source FETs-part II: nonidealities and benchmarking. *IEEE Trans. Electron Devices* **69**(8), 4681–4685 (2022). <https://doi.org/10.1109/TED.2022.3181537>
5. Liang, X., Taur, Y.: A 2-D analytical solution for SCEs in DG MOSFETs. *IEEE Trans. Electron Devices* **51**(9), 1385–1391 (2004). <https://doi.org/10.1109/TED.2004.832707>
6. Katsnelson, M.I., et al.: Chiral tunnelling and the Klein paradox in graphene. *Nat. Phys.* **2**(9), 620–625 (2006). <https://doi.org/10.1038/nphys384>
7. Gnani, E., et al.: Effects of high- κ (HfO₂) gate dielectrics in double-gate and cylindrical-nanowire FETs scaled to the ultimate technology nodes. *IEEE Trans. Nanotechnol.* **6**(1), 90–96 (2007). <https://doi.org/10.1109/TNANO.2006.888547>



Anomalous I-V Characteristics of 4H-SiC p-i-n Diode at Cryogenic Temperature

Nicola Rinaldi^(✉), Luigi Di Benedetto, Gian Domenico Licciardo, Rosalba Liguori, and Alfredo Rubino

Department of Industrial Engineering, University of Salerno,
Via Giovanni Paolo II 132, 84084 Fisciano, Italy
{nrinaldi,lidibenedetto,gdlicciardo,rliuguori,arubino}@unisa.it

Abstract. A vertical 4H-SiC p-i-n diode fabricated by Aluminum implantation is characterized in the cryogenic temperature range, i.e. lower than 123K. An anomalous characteristic is shown under current bias conditions and it can limit its use in fields of applications, like temperature sensing. To investigate the thermo-electrical behaviour, Deep Level Transient Spectroscopy (DLTS) analysis has been performed and an electron trap at 97 meV below the minimum edge of the conduction band with a capture cross section of $1.14 \cdot 10^{-13} \text{ cm}^2$ and a hole trap at 375 meV from valence band with a capture cross section of $4.4 \cdot 10^{-13} \text{ cm}^2$ have been found. We suppose that the anomalous behaviour of the I-V characteristics can be ascribed to the hole traps.

Keywords: 4H polytype Silicon Carbide · Cryogenic Devices · DLTS.

1 Introduction

Nowadays, 4H-polytype Silicon Carbide technology is an enough mature technology and related commercial devices are available [1]. Although they are primarily used in power electronics, its radiation hardness [2,3] and high electric field [4] can extend its use to other application fields, like aerospace, interfacing electronics for quantum computing [5] or temperature sensing [6,7], in which cryogenic temperature are required ($T < 123K$). However, because Aluminum ion, Al^+ , implantation is the only technology to make selective p-type regions, the ion damage recovering process is still an issue [8,9].

In this study, we report the I-V characteristics of p-i-n diodes fabricated by Al^+ implantation in n-type drift epi-layer. The diode is biased at a forced current $I_D \in [10^{-7}, 10^{-4}]A$ and in the temperature range from 33.9K to 79.3K it shows a no-continue curves, making it unusable as a standard device. To understand this phenomenon, a DLTS analysis has been performed and a minority carrier emission process found, despite a 0V filling pulse, V_P , has been applied. We suppose that the holes deep trap can be ascribed to the anomalous behaviour of the I-V characteristic.

2 Experimental

Measurements have been performed on an ion-implanted 4H-SiC p-i-n diode with an Al^+ doping concentration of $5 \cdot 10^{19} \text{ cm}^{-3}$ in a n-type drift epi-layer with a $1.5 \cdot 10^{15} \text{ cm}^{-3}$ donor concentration. A Janesis Research 10K closed cycle refrigerator system and an Agilent HP4155B Semiconductor Parameter Analyzer have been used to perform I-V measurements. Moreover, DLTS measurements have been done with a BOONTON 7200 Capacitance meter among the temperature range $T \in [33; 300]K$.

During DLTS measurements, a reverse and filling voltages, respectively, $V_{BIAS} = -2V$ and $V_P = 0V$ are applied to the sample with a constant filling time, t_P of $15ms$. In Fig. 1.a) the waveform of the bias voltage is reported. During the filling pulse, the depletion region reduces causing an increase of capacitance, Fig. 1.b-II), respect to its steady-state value, Fig. 1.b-I). If there are deep levels at an energy level below the Fermi Level, they will be filled.

After the filling pulse, the reverse bias is returned to its quiescent level, causing an increase of depletion region. However, since some of the deep level traps in the depletion region are now filled, the charge density in the depletion region is less than it was before the filling pulse, therefore the depletion region is slightly wider and the capacitance is lower Fig. 1.b-III). Since the filled traps in the depletion region are above the Fermi level, they now emit carriers causing the increase of the charge density in the depletion region with the consequent reduction of the width in Space Charge Region. Hence, the capacitance of the junction, Fig. 1.b-IV), [10], increases.

Once that the capacitance transients have been recorded, they can be analyzed through boxcar method [11]. The capacitance value is recorded at two fixed time $C(t_1)$, $C(t_2)$, Fig. 1.c), and then subtracted among them, δC , at each scan temperature. The value of δC depends on the trap parameter as follows, in case of n-type doped semiconductor:

$$\delta C = \frac{n_T(0)}{2N_D} C_0 e^{\frac{t_2-t_1}{\tau_e}} \quad (1)$$

where C_0 is the steady-state capacitance value, $n_T(0)$ is the trap density at the beginning of the emission process and N_D is the net doping donor concentration.

Plotting each difference, δC , as function of the temperature, the DLTS spectrum is built. Repeating this process with different ratio window, t_2/t_1 , different spectra with δC maximum at different temperature results, each of them related to a maximum emission time constant, $\tau_{e,max}$:

$$\tau_{e,max} = \frac{t_2 - t_1}{\ln(t_2/t_1)} \quad (2)$$

Collecting the emission time constant, τ_e , related to each δC maximum, an Arrhenius plot can be drawn through the following relation:

$$\tau_e T^2 = \frac{e^{\left(\frac{\Delta E_T}{k_B T}\right)}}{\gamma_N \sigma_N} \quad (3)$$

where $\Delta E_T = E_C - E_T$, k_B is the Boltzmann constant, $\gamma_N = (v_{th}/T^{1/2})(N_C/T^{3/2})$, with v_{th} electron thermal velocity. In case of hole traps, $\Delta E_T = E_T - E_V$, whereas γ_N , N_C and σ_N , are changed with γ_P , N_V and σ_P , respectively.

Then, the trap activation energy, ΔE_T , and trap capture cross section, σ_n , are obtained, respectively, from the slope and intercept of the Arrhenius plot.

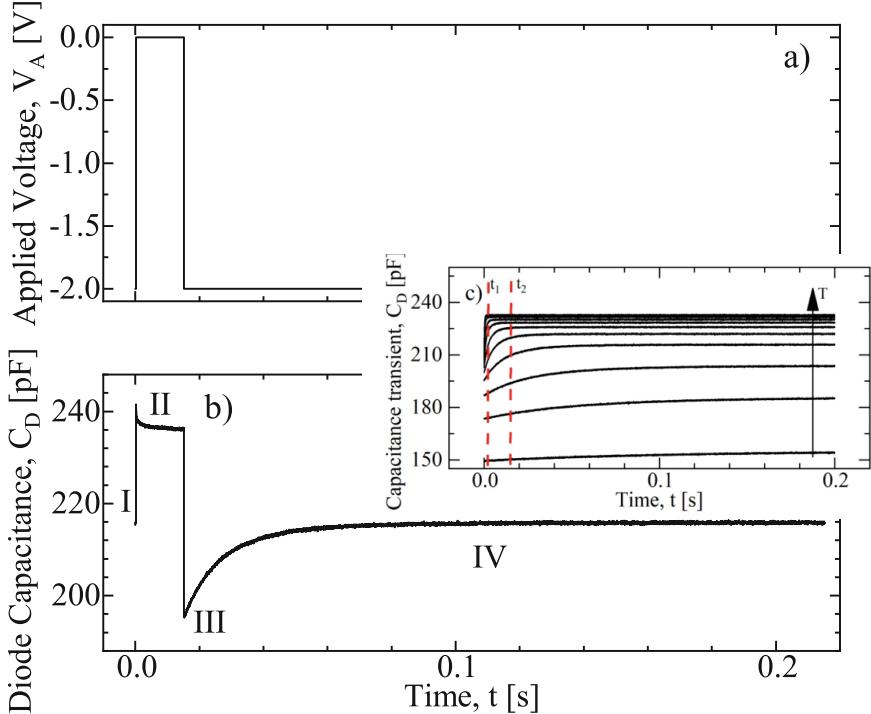


Fig. 1. a)Applied voltage pulse during DLTS measurements .b) Diode capacitance behaviour when majority carrier traps are captured and emitted. c) Diode Capacitance transient, during emission process, recorded at different temperature to perform boxcar method.

3 Results

I-V characteristics show an anomalous behaviour when a forward constant current, $I_D \in [4 \cdot 10^{-7}; 10^{-4}]$, biases the diode in the temperature range $T \in [33.9; 79.3]K$ (see Fig. 2). It can be observed that the characteristics have a negative slope with a discontinuity in some bias voltage making irregular the curves. To investigate it, DLTS has been performed to identify a possible defect

in the band-gap and two energy trap levels are found, as shown in Fig. 2a)-b), whose electrical parameters are in Table 1. The first one, i.e. Level 1, is a majority carrier trap with an activation energy of $E_C - E_T = 97$ meV and it is ascribed to nitrogen dopant freeze out in n-type drift epi-layer [12], whereas a second signal, named Level 2, has an inverted behaviour. Although a 0V filling pulse is applied, it can be associated to a minority carrier trap with an activation energy of $E_T + E_V = 375$ meV, as also reported in [12]. The hole energy level can be ascribed to the anomalous behaviour of IV curves: the minority carriers are injected through the junction and captured by LEVEL2 traps, which are filled, and, as consequence, a high voltage drop is achieved. However, numerical analysis are required to validate this hypothesis (Fig. 3).

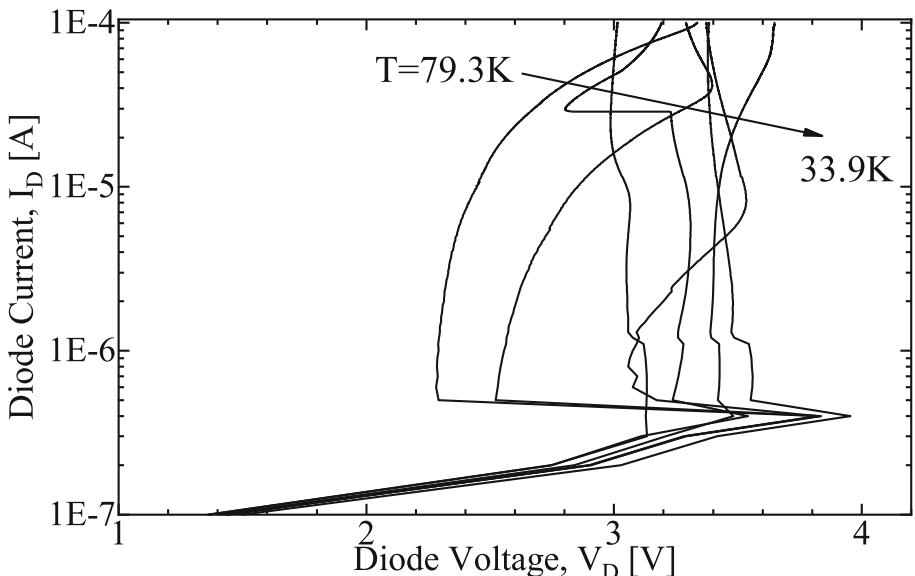


Fig. 2. Experimental I-V characteristic of the Al^+ implanted 4H-SiC p-i-n diode biased with a current, $I_D \in [10^{-7}, 10^{-4}] A$, in the temperature range $T \in [33.9; 79.3] K$.

Table 1. Energy levels extracted from DLTS signal.

Level	N_T/N_D	$\Delta E_T [eV]$	$\sigma [cm^2]$
1	0.185	$E_C - E_T = 97.09 \cdot 10^{-3}$	$1.14 \cdot 10^{-13}$
2	0.024	$E_T + E_V = 375.4 \cdot 10^{-3}$	$4.4 \cdot 10^{-13}$

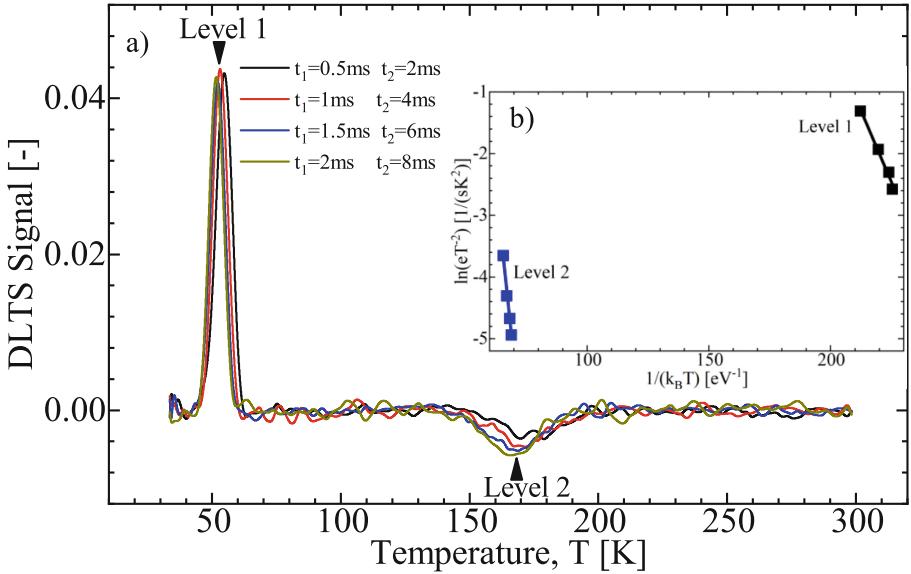


Fig. 3. a) DLTS Signal obtained with boxcar method, $t_2/t_1 = 4$, with $V_{BIAS} = -2\text{ V}$ and a 15 ms filling pulse, $V_p = 0\text{ V}$, in the temperature range, $T \in [33; 300]\text{ K}$. b) In the inset Arrhenius plot obtained through Eq. 3, where $e = 1/\tau_e$.

4 Conclusions

No-continue I-V curves of an Al^+ implanted 4H-SiC vertical p-i-n diode is shown in $T \in [33.9; 79.3]\text{ K}$ when a forward constant current is applied, and a capture-emission process caused by a minority carrier trap, found at an energy level of $E_T + E_V = 375\text{ meV}$ through DLTS measurements, can be ascribed to this behaviour.

References

1. Kimoto, T.: Fundamentals, commercialization, and future challenges of sic power devices. In: 2023 IEEE International Meeting for Future of Electron Devices, Kansai (IMFEDK), pp. 1–4. IEEE (2023)
2. Lebedev, A.A., Kozlovski, V.V., Davydovskaya, K.S., Levinshtein, M.E.: Radiation hardness of silicon carbide upon high-temperature electron and proton irradiation. Materials **14**(17), 4976 (2021)
3. Lebedev, A.A., et al.: Radiation hardness of silicon carbide. In: Materials Science Forum, vol. 433, pp. 957–960. Trans Tech Publ (2003)
4. Kimoto, T., Cooper, J.A.: Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications. John Wiley & Sons, Hoboken (2014)
5. van Dijk, J.P., Charbon, E., Sebastian, F.: The electronic interface for quantum processors. Microprocess. Microsyst. **66**, 90–101 (2019)

6. Matthus, C.D., et al.: Feasibility of 4h-sic pin diode for sensitive temperature measurements between 20.5 k and 802 k. *IEEE Sens. J.* **19**(8), 2871–2878 (2019)
7. Rao, S., Pangallo, G., Di Benedetto, L., Rubino, A., Licciardo, G.D., Della Corte, F.G.: A v2o5/4h-sic schottky diode-based ptat sensor operating in a wide range of bias currents. *Sens. Actu. A* **269**, 171–174 (2018)
8. Nipoti, R., Ayedh, H.M., Svensson, B.G.: Defects related to electrical doping of 4h-sic by ion implantation. *Mater. Sci. Semicond. Process.* **78**, 13–21 (2018)
9. Nipoti, R., Di Benedetto, L., Albonetti, C., Bellone, S.: Al+ implanted anode for 4h-sic pin diodes. *ECS Trans.* **50**(3), 391 (2013)
10. Lang, D.: Deep-level transient spectroscopy: a new method to characterize traps in semiconductors. *J. Appl. Phys.* **45**(7), 3023–3032 (1974)
11. Schroder, D.K.: Semiconductor Material and Device Characterization. John Wiley & Sons, Hoboken (2015)
12. Ayedh, H.M., Puzzanghera, M., Svensson, B.G., Nipoti, R.: Dlts study on al+ ion implanted and 1950° c annealed pin 4h-sic vertical diodes. In: Materials Science Forum, vol. 897, pp. 279–282. Trans Tech Publ (2017)



Rutile TiO₂ Nanoparticles as Raman Micro-thermometer for Self-heating Analysis

Francesca Zarotti^(✉), Ernesto Limiti, and Andrea Reale

University of Rome “Tor Vergata”, Electronic Engineering Department, Via del Politecnico 1,
00133 Rome, Italy

francesca.zarotti@uniroma2.it

Abstract. In microelectrical systems, improving device performance and shrinking feature sizes make thermal design crucial. HPA based devices concentrate very high dissipation power in the sub-micron region, causing localized high channel temperatures. This study investigates rutile TiO₂ microparticles as thermal probes for precise temperature mapping on semiconductor surfaces, focusing on silicon. Utilizing micro-Raman spectroscopy, we calibrate temperature responses across various substrates, revealing distinct behaviors influenced by volumetric ratios and proximity to heat sources. The scaling of Raman shifts with applied power highlights complex thermal dynamics critical for optimizing device performance and reliability. TiO₂ microparticles demonstrate effectiveness in overcoming traditional thermometry method limitations, offering sub-micrometer spatial resolution and accurate temperature estimation. This study provides valuable insights into sub-micrometer thermal analysis, guiding advancements in microelectronic and microelectromechanical systems, particularly in managing localized high temperatures in GaN-based devices and improving device lifetime estimation.

Keywords: thermal characterization · Raman spectroscopy · micro-Raman thermometers

1 Introduction

In the rapidly advancing fields of microelectrical and microelectromechanical systems, the significance of thermal design and management has reached unprecedented levels. With device performance continually improving and feature sizes steadily decreasing, the ability to manage heat dissipation has become a critical factor influencing the overall functionality and reliability of micro devices. As heat dissipation remains a limiting factor, there is a growing need for innovative approaches to understand heat transfer on a microscopic level. Traditional thermometry methods, such as infrared (IR) emission and contact-mode techniques, fall short due to their inherent limitations in spatial resolution and potential for distorted measurements. For example, the spatial resolution of IR-emission based methods is diffraction-limited to approximately 10 μm [1], and while contact-mode techniques offer higher spatial resolution (around 20 nm), they suffer from local heat transfer distortions and limited temporal resolution [2]. To address these

challenges, new high-resolution thermometry techniques like micro-Raman and thermoreflectance thermometry have been developed, boasting spatial resolutions down to 0.5 μm. Micro-Raman thermometry, in particular, leverages the temperature-dependent changes in Raman spectra, providing detailed temperature distribution images through raster scanning of a laser. This technique has been effectively applied across various domains, including microelectromechanical systems, microelectronic devices and optoelectronic systems. Materials such as silicon, gallium nitride (GaN), gallium arsenide (GaAs), and graphene have been investigated using micro-Raman thermometry [3, 4]. However, despite its advantages, micro-Raman thermometry is limited to specific materials like semiconductors and insulators. Metals, with their low phonon energies, present challenges in distinguishing Raman scattered light from the excitation source, and temperature measurements can be distorted by thermally induced strain.

To overcome these material limitations, microparticles with strong and temperature-sensitive Raman signals, such as TiO₂, offer a promising solution [5, 6]. These microparticles can be used to map temperatures at different device locations or monitor particle temperature *in situ*, providing a valuable tool for experiments involving catalytic reactions on nanoparticles or microcalorimetry measurements.

This paper presents an innovative implementation of micro-Raman thermometry using rutile TiO₂ microparticles deposited on Si devices, enabling significantly higher spatial resolution than most current techniques. Unlike traditional methods, this approach is not restricted by substrate materials, as the Raman scattering from the microparticles provides the temperature data. We delved into the fundamental mechanisms of micro-Raman thermometry and detail the experimental setup, sample preparation, calibration, and spectral analysis for rutile TiO₂ microparticles.

These findings offer valuable insights into heat transfer and thermal gradients within and across materials at micrometer scale, providing a benchmark for thermal simulations. This method is particularly applicable for thermal analysis in GaN-based HEMT devices [7], enhancing the understanding and management of thermal dynamics in advanced semiconductor applications.

2 Methods

As a proof of concept, we prepared two different devices acting as passive loads by creating ohmic contacts on an n-type, heavily doped Si (100) wafer chip mounted on glass microslide substrates. 100 nm silver contacts were evaporated onto the Si substrates after removing the native SiO₂ in the contact region. We used 300 nm light-scattering TiO₂ nanoparticles deposited on top of the Si as thermal probes to evaluate the surface temperature of the semiconductor. The TiO₂ particles, dispersed in ethanol at a concentration of 25.4 mg/ml, were spin-coated onto the Si sample by applying 100 μl of the solution at 5000 rpm for 30 s. The distribution of TiO₂ nanoparticle agglomerates (microparticles, mp_s) was observed using a TESCAN MIRA SEM, acquiring images at 10 keV beam energy with an EDX detector (model 30 Xplore, Oxford Instruments). Images and maps are shown in Fig. 1.

Raman measurements were performed using a Horiba LabRAM ARAMIS confocal microscope equipped with a 50x LWD objective and a 532 nm wavelength laser. The

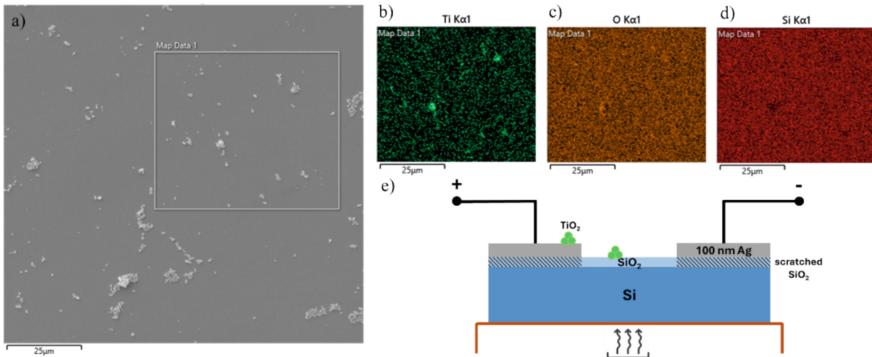


Fig. 1. a) SEM image of glass/ITO/TiO₂ nanoparticles agglomerates together with EDX maps for b) Ti, c) O and d) Si from the glass. e) Sketch of the Si device and agglomerates of TiO₂ nanoparticles on top of Si surface and Ag contact.

temperature was controlled using a Julabo temperature controlled stage with Peltier cell, ensuring precise thermal conditions during the experiments.

3 Results and Discussion

After having determined the useful concentration and right size of nanoparticles agglomerates, we calibrate the samples by the use of Raman spectroscopy. The organization of an agglomerate of TiO₂ nanoparticles spin-coated on glass/ITO is shown by a SEM image in Fig. 2a). In Fig. 2b) and c), typical Raman spectra from Si and from rutile TiO₂ nanoparticles on top of Si sample are reported. Raman active lattice vibrations of Si (520 cm⁻¹) and of rutile TiO₂, B_{1g} (145 cm⁻¹), E_g (445 cm⁻¹), and A_{1g} (610 cm⁻¹) are present [8].

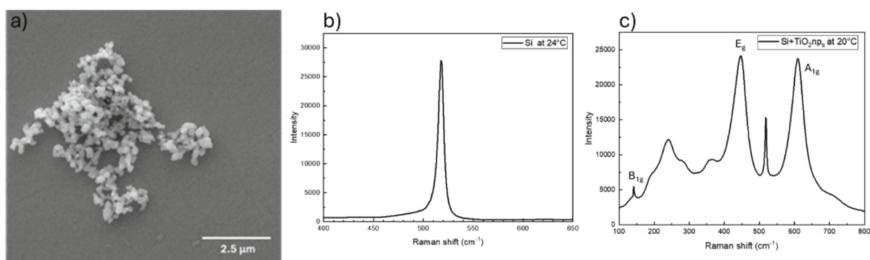


Fig. 2. a) SEM image of glass/ITO/TiO₂ nanoparticles agglomerate. Raman spectra from b) Si and from c) Si and rutile phase of TiO₂ mp_s.

The calibration involved testing at various temperatures: 20 °C, 40 °C, 60 °C, and 80 °C. Figure 3 illustrates the Raman spectra for (a) and (b) TiO₂ mp_s on the Si surface, and (c) TiO₂ mp_s on top of Ag contacts at these different investigated temperatures.

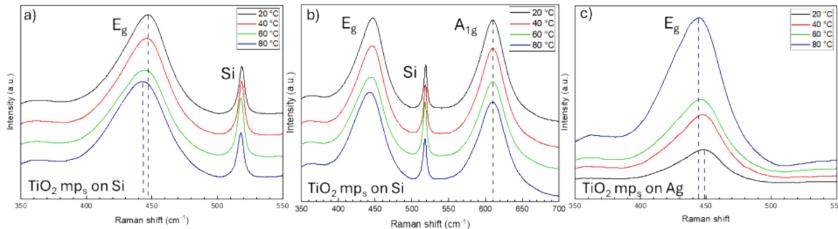


Fig. 3. a) Raman shift due to the variation of temperature of E_g band of rutile $\text{TiO}_2 \text{ mp}_s$ together with Si Raman peak and b) comparison between Raman shift of E_g band and A_{1g} band of rutile $\text{TiO}_2 \text{ mp}_s$. c) Raman shift of E_g band of rutile $\text{TiO}_2 \text{ mp}_s$ on top of Ag contact surface.

As it is explained in reference [8] E_g mode around 445 cm^{-1} was of the asymmetric bending of the O – Ti – O bonds in the {001} plane, caused by the opposite moving of the O atoms across the O – Ti – O bond. The A_{1g} mode around 610 cm^{-1} was characterized by the symmetric stretching of the O – Ti – O bonds in the {110} plane, caused by the opposite moving of the O atoms in the adjacent O – Ti – O bonds. Since the agglomerate develops in z-direction, perpendicular to the Si surface, increasing the temperature, a major contribution from vibrational mode along this out of plane direction instead from in-plane is expected. For this reason we decided to calibrate the material from E_g TiO_2 Raman peak.

We also leveraged mapping techniques to obtain precise information on the behavior of the TiO_2 Raman thermometer as a function of temperature on both Si and Ag surfaces. By using these maps, we could not only identify the peaks related to the specific TiO_2 probes but also measure signals from the substrate. In Fig. 4 a), spectra collected at 40°C are presented for a $10 \times 10 \mu\text{m}^2$ area on the Si surface with a step size of $1 \mu\text{m}$, totaling 100 points. The analysis of intensity variations for the two major peaks from rutile TiO_2 —b) E_g and c) A_{1g} bands—is shown, along with the intensity ratio between the E_g peak of TiO_2 and the Si substrate peak. This ratio highlights the position of the TiO_2 agglomerates, where the TiO_2 signal is more intense than that from the Si substrate.

Figure 5 presents a similar map for a TiO_2 agglomerate on the Ag contact surface. Notably, in this region, the signal from the substrate is absent, as it is fully covered by the background signal from the Ag. This mapping approach ensures accurate temperature measurement and characterization of TiO_2 nanoparticles on different substrates, enhancing our understanding of the Raman thermometer's performance.

Figure 6 displays the calibration curves along with their linear fits for a) Si and b) $\text{TiO}_2 \text{ mp}_s$ on both Si and Ag surfaces. The variation in the linear coefficients of the three curves can be attributed to the volumetric ratio between Si and $\text{TiO}_2 \text{ mp}_s$ and the distance from the heat source. Specifically, the absolute value of the linear coefficient increases from Si to $\text{TiO}_2 \text{ mp}_s$ due to the smaller volume of $\text{TiO}_2 \text{ mp}_s$ involved in the heating process. The difference in the linear behavior of the Raman shift for the E_g TiO_2 band on Si compared to Ag is primarily due to the increased distance from the heat source. This indicates that the $\text{TiO}_2 \text{ mp}_s$ on Ag are less affected by the direct heating, resulting in a different thermal response compared to those on the Si substrate.

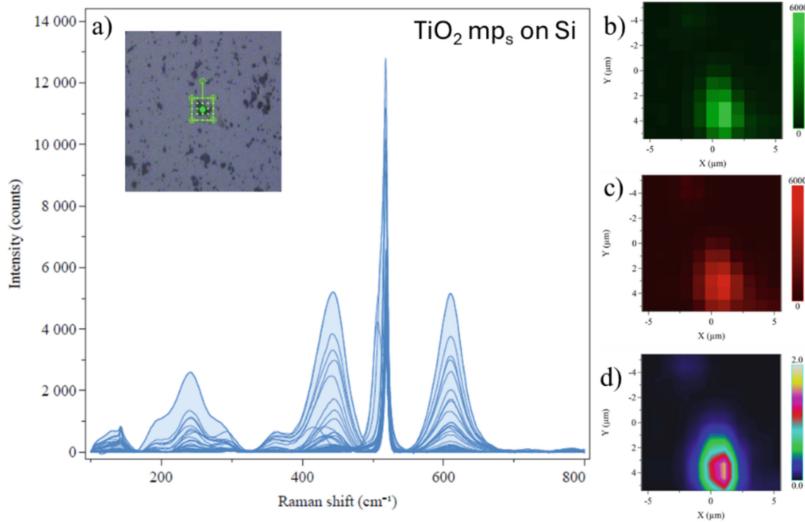


Fig. 4. a) Collection of Raman spectra measured at T = 40 °C on the Si surface on the TiO₂ agglomerate enclosed in the 10 × 10 μm² map, showed in the inset. Maps of the peaks intensity of b) Eg band and of c) A_{1g} band of rutile TiO₂ mps are displayed on the left side. d) Map of the intensity ratio between Si and Eg band of TiO₂ mps.

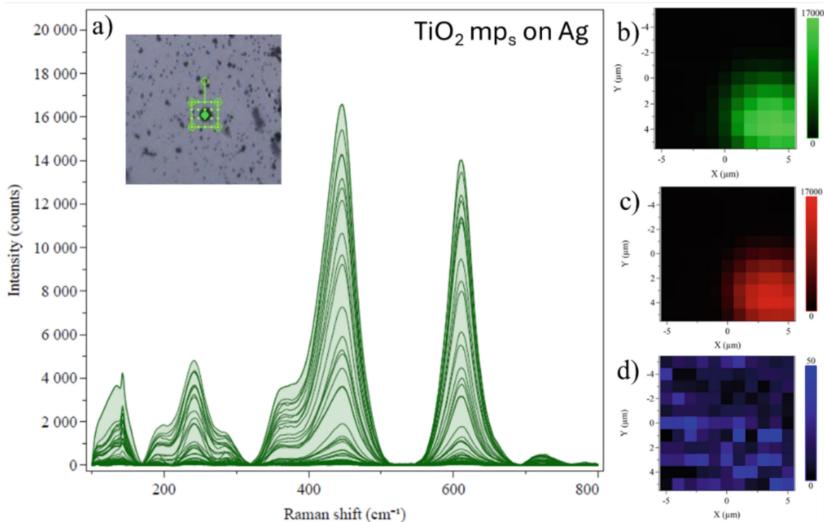


Fig. 5. a) Collection of Raman spectra measured at T = 60 °C on the Ag contact of the TiO₂ agglomerate enclosed in the 10 × 10 μm² map, showed in the inset. Maps of the peaks intensity of b) Eg band, c) A_{1g} band rutile TiO₂ mps and d) Si peak are displayed on the left side.

For both devices, we used the obtained calibration curves to estimate the reached temperature during the dissipation process at various applied power levels. The results

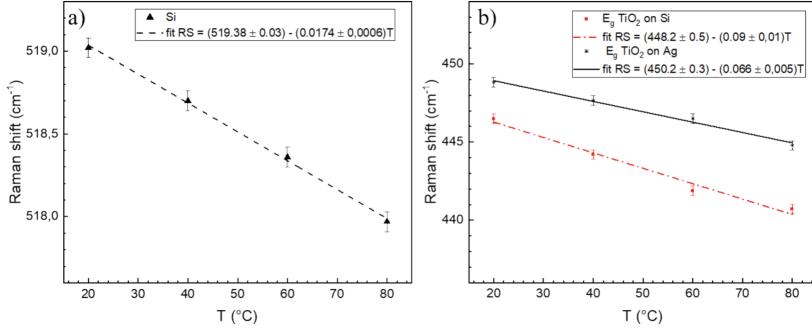


Fig. 6. a) Calibration curve of Si peak and of b) E_g band of TiO₂ mp_s on Si surface (red points) and on Ag contact (black points).

are shown in Fig. 7 for a) the Si signal and b) the E_g band from the TiO₂ mp_s. It can be noted that the Raman shift does not scale linearly with power. Interestingly, the resistance between the Ag contacts decreased after the Raman measurements during dissipation. This is likely due to structural reorganization and changes in electrical resistance beneath the Ag contact region, where the Si surface was scratched to ensure current flow through the device. This circumstance also affects the signal measurements from the TiO₂ mp_s on the Si surface. During the dissipation process, power is applied through the contact on top of the Si surface while the heat source is maintained at 20 °C. As the applied power increases, the current flow is enhanced, but the efficiency of heat extraction at the surface remains relatively low. This explains the higher estimated temperatures of TiO₂ mp_s on Si (~154 °C) and on Ag (~170 °C, not shown) compared to that of Si (~142 °C) at the highest applied power level.

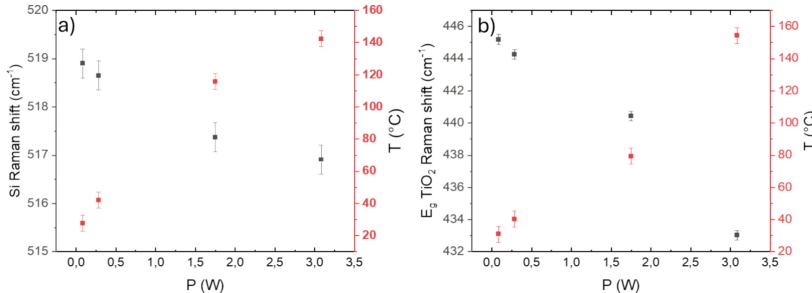


Fig. 7. The Raman shift (black points) together with the estimated temperature (red points) of a) the Si peak and of b) the E_g band of TiO₂ mp_s on Si, as a function of applied dissipation power.

Figure 8 a), b), and f) show SEM images of a GaN HEMT device with spin-coated rutile TiO₂ mp_s. Unlike the Si surface, this GaN HEMT surface has regions of varying depths where the TiO₂ microparticles can form larger agglomerates. One technique to overcome this difficulty is spray-coating the microparticles for a more uniform distribution. Figures 8 c), d), and e) present maps of the sample's key elements: Au for the

metallization, and Ti and O from the microparticles deposited on the device. A close-up of the active region of the channel confirms the presence of g) the Au gate finger, h) Ga from the GaN-based layers, and i) Ti from the microparticles on the left side of the image. This detailed elemental mapping underscores the precise positioning and interaction of the TiO₂ mp_s with the GaN HEMT device, providing valuable insights for thermal analysis and device optimization.

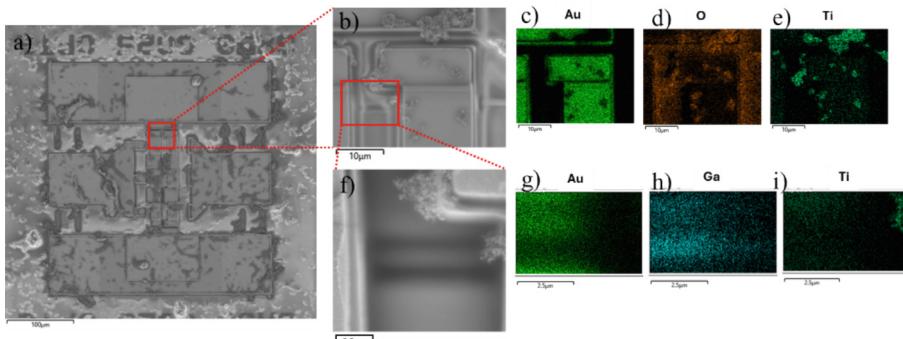


Fig. 8. a) 100 μm image of GaN based HEMT device. b) Zoom on the “channel” region and relative EDX maps for c) Au, d) Ti and e) O elements. f) Further zoom on the active region of “channel” and EDX maps for g) Au, h) Ga and i) Ti elements.

4 Conclusions

This study successfully employed rutile TiO₂ mp_s as thermal probes to assess temperature distribution on semiconductor surfaces, particularly silicon. Calibration with Raman spectroscopy at various temperatures revealed distinct linear behaviors on silicon and silver surfaces, due to differences in volumetric ratios and distances from heat sources. The calibration curves allowed precise temperature estimation during power dissipation, uncovering non-linear Raman shift scaling with applied power and highlighting complex thermal dynamics. This approach validated TiO₂ mp_s as effective thermal probes and provided valuable data for optimizing thermal management in semiconductor devices. Our findings support future research on improved deposition techniques and alternative nanoparticle materials. Upcoming work will explore using nanoparticles of various materials, selected for size and deposition technique compatibility, to apply onto GaN HEMT devices. This approach aims to enable temperature monitoring across different components of the device using a single probe type, enhancing the efficiency and accuracy of thermal management strategies.

Acknowledgements. The authors would like to thank the SEXTET project “design of sustainable, affordable, and energy-efficient communication systems for extreme environments” in the framework of RESTART – RESearch and innovation on future Telecommunications systems and networks, to make Italy more smART (CUP: E83C22004640001) funded by European Union through the NextGenerationEU program.

References

1. Sarua, A., et al.: Integrated micro-Raman/infrared thermography probe for monitoring of self-heating in AlGaN/GaN transistor structures. *IEEE Trans. Electron Devices* **53**(10), 2438–2447 (2006)
2. Gucmann, F., et al.: Scanning thermal microscopy for accurate nanoscale device thermography. *Nano Today* **39**, 101206 (2021)
3. Lundt, N., et al. (2013) “High spatial resolution Raman thermometry analysis of TiO₂ microparticles. *Rev. Sci. Instrum.* **84** (10)
4. Kuball, M., et al.: A review of Raman thermography for electronic and opto-electronic device measurement with submicron spatial and nanosecond temporal resolution. *IEEE Trans. Device Mater. Reliab.* **16**(4), 667–684 (2016)
5. Brocero, G., et al.: Measurement of self-heating temperature in AlGaN/GaN HEMTs by using cerium oxide micro-Raman thermometers. *IEEE Trans. Electron Devices* **66**(10), 4156–4163 (2019)
6. Strenaer, R., et al.: Self-heating temperature measurement in AlInN/GaN HEMTs by using CeO₂ and TiO₂ micro-Raman thermometers. *Microelectron. Reliab.* **138**, 114693 (2022)
7. Hoo Teo, K., et al. (2021) “Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects.” *J. Appl. Phys.* **130**(16)
8. Zhang, Y., et al.: Asymmetric lattice vibrational characteristics of rutile TiO₂ as revealed by laser power dependent Raman spectroscopy. *J. Phys. Chem. C* **117**(45), 24015–24022 (2013)



Simulation Framework for Hole Spin Qubits

Lorenzo Raschi^(✉) and Antonio Gnudi^{ID}

University of Bologna, ARCES/DEI, Viale Risorgimento 2, 40136 Bologna, Italy
lorenzo.raschi4@unibo.it

Abstract. A framework for the simulation of hole spin qubits based on COMSOL Multiphysics is presented. The tool solves the coupled Poisson and Schrödinger equations in the four-bands $\mathbf{k} \cdot \mathbf{p}$ Hamiltonian including the effects of a static magnetic field \mathbf{B} . The gyromagnetic matrix g and its derivative g' with respect to the gate voltage are calculated from the wavefunctions at zero magnetic field. The matrices g and g' allow for the computation of the Rabi frequency as a function of the magnetic field to first order in the magnetic field and in the gate voltage. Results for a qubit hosted in a silicon nanowire fabricated in SOI technology are presented. Solutions for different gate geometries are compared.

Keywords: Spin-Qubit · Quantum Computing · Quantum-CAD · Luttinger-Kohn Hamiltonian

1 Introduction

Among the various technological platforms that are currently investigated as possible candidates for the implementation of large-scale multi-qubit quantum computers, spin qubits in silicon quantum dots (QDs) are one of the most attractive solutions. Long spin lifetimes can indeed be achieved in isotopically purified silicon. Silicon is also a natural platform for the co-integration of quantum devices with classical electronics [1]. More specifically, hole spin qubits are more attractive than their electron counterparts because hole spin can be coupled with the orbital motion more easily than electron spin, thus opening the way to all-electrical spin manipulation [2].

On the modeling side, the availability of a Quantum-CAD (QCAD) framework is a highly desirable goal to assist device designers and explore new solutions, with a very similar role to well-established TCAD tools in nanoelectronics.

In this paper we present a QCAD tool based on COMSOL Multiphysics [3] for the analysis of hole spin qubits hosted in semiconductor quantum dots, which calculates in a self-consistent way the electrostatic potential profile and the energy levels of a hole in a QD in the presence of a static magnetic field. The gyromagnetic matrix is also calculated, which fully characterizes the behavior of the qubit and allows for the calculation of the Rabi frequency as a function of the magnetic field orientation [4].

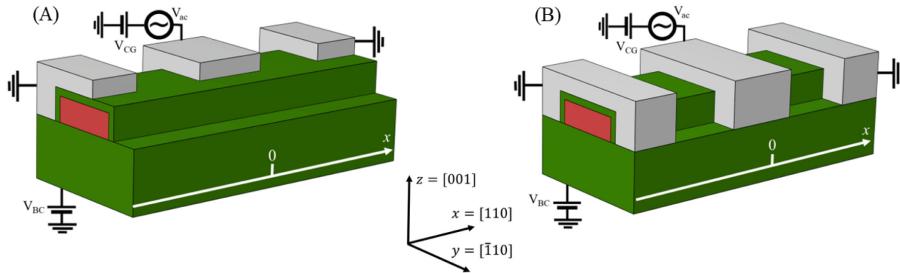


Fig. 1. Simulated structures with two different gate geometries. Color code: red for Si, green for SiO₂, grey for metal gates. In both structures the Si nanowire cross section is 10 nm × 30 nm, the bottom oxide thickness 25 nm, the central gate length 30 nm, the lateral gates length 20 nm, the gate spacing 30 nm, the thin SiO₂ layer thickness 3 nm. The structures are covered by a passivating SiO₂ layer (not shown). In structure A the gates overlap 20 nm out of 30 nm of the nanowire. The x axis is parallel to the longitudinal nanowire axis. The crystallographic orientation is illustrated in the inset.

2 Simulated Structures

Figure 1 shows the geometry of the two simulated structures (see the caption for details). They are essentially based on an SOI technology, where a [110]-oriented Si nanowire embedded in an SiO₂ layer hosts the qubit. Three metal gates are used to form a potential trap for a hole under the central gate. The latter is biased at voltage V_{CG} , with a radiofrequency (RF) modulation of amplitude V_{ac} to manipulate the qubit state. The lateral gates are biased at fixed zero voltage. A bottom contact at voltage V_{BC} replaces the doped Si substrate. Each device is covered by a passivating SiO₂ layer, which has been removed from the figure for clarity. The two devices differ because in case A the gates partially overlap the nanowire, as opposed to case B where the gates completely surround the nanowire.

3 The Mathematical Model

The four-bands $\mathbf{k}\cdot\mathbf{p}$ Luttinger-Kohn (LK) Hamiltonian [5, 6] for the valence band is assumed in this paper for the calculation of the hole eigenstates. Appendix A reports all definitions and equations. In essence, the model captures the dynamics of the heavy-hole (HH) and light-hole (LH) components of the wavefunction. Schrödinger equation has the form of an eigensystem of four PDEs in the four unknown components of the wavefunction envelope. The Hamiltonian is discretized on a finite difference mesh. Zero wavefunction is imposed at the Si/insulator interfaces (i.e., no penetration of the wavefunction in the insulators is assumed).

Rabi frequency can be computed either with a direct approach culminating in Eq. (13) of Appendix B, or by exploiting the g -matrix formalism outlined in Appendix C, closely following the theory presented in [4]. The advantage of the g -matrix approach consists in the fact that the eigenvalue problem needs not to be solved for each magnetic field orientation, as opposed to the direct method.

Table 1. Heavy-holes (HH, $J_z = \pm \frac{3}{2}$, components 1 and 4) and light-holes (LH, $J_z = \pm \frac{1}{2}$, components 2 and 3) weights of the squared ground-state envelopes of both devices at $\mathbf{B} = \mathbf{0}$ T, $V_{BC} = -0.14$ V and $V_{CG} = -0.1$ V. The HH character of the ground-state is evident.

	HH	LH
Device A	97%	3%
Device B	96%	4%

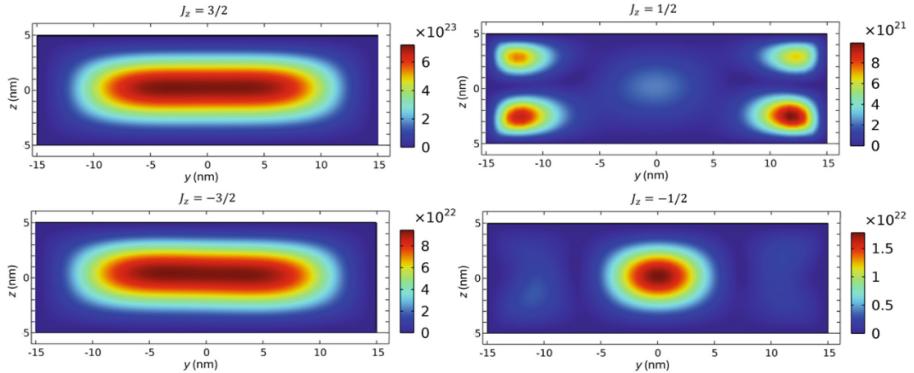


Fig. 2. Squared HH ($J_z = \pm \frac{3}{2}$) and LH ($J_z = \pm \frac{1}{2}$) envelopes of the ground-state doublet on the (y,z) plane at $x = 0$ (see Fig. 1) for structure B at $V_{CG} = -0.1$ V and $V_{BC} = 0$ V. The HH components are more than one order of magnitude larger than the LH components.

4 Results

4.1 Zero Field Results

The results presented in this Section are obtained with $\mathbf{B} = \mathbf{0}$ T. With no magnetic field each energy eigenvalue is double degenerate due to symmetry reasons, forming the so called Kramers doublet. The calculated energy gap between the ground and the first excited doublet at $V_{CG} = -0.1$ V and $V_{BC} = 0$ V is $\Delta E_A = 4.03$ meV in case A and $\Delta E_B = 1.6$ meV in case B.

In both cases the states forming the ground doublet have a dominant HH character. The total HH ($(\frac{3}{2}, \pm \frac{3}{2})$) and LH ($(\frac{3}{2}, \pm \frac{1}{2})$) weights of the squared ground-state envelopes for both structures are reported in Table 1. As an example, the square of the four components of the ground states on the (y,z) plane at $x = 0$ (i.e. just under the central gate, see Fig. 1) of structure B are reported in Fig. 2.

The main difference between device A and B is that in the former, due to the partial overlap of the central gate with the nanowire, it is possible to move the trapped hole along the y -direction under the central gate by acting on voltages V_{CG} and V_{BC} , thus introducing an additional degree of freedom to adjust the qubit performance. This is

illustrated in Fig. 3, which shows the isoprobability surfaces of the ground-state wavefunction of structure A at $V_{CG} = -0.1$ V for three different V_{BC} values. In general

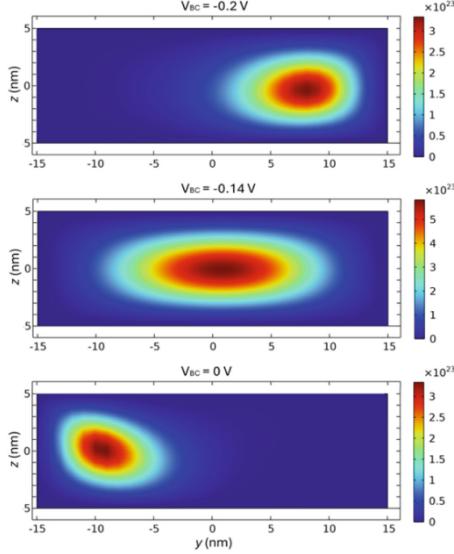


Fig. 3. Isoprobability surfaces of the ground-state hole wavefunction of structure A at three different V_{BC} values and $V_{CG} = -0.1 \text{ V}$ in the (y, z) symmetry plane at $x = 0$ (see Fig. 1). Note that at $V_{BC} = -0.14 \text{ V}$ the hole wavefunction is almost symmetric.

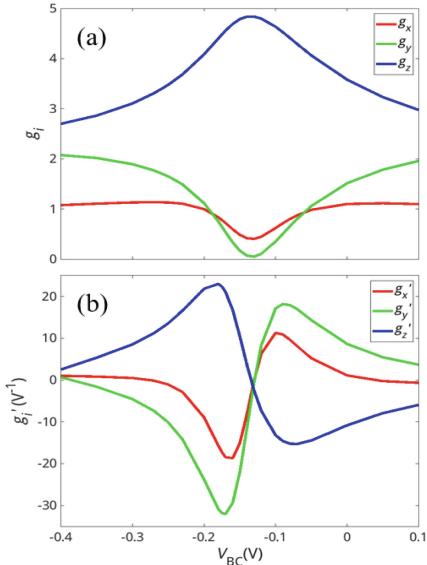


Fig. 4. (a) Principal g factors g_x , g_y , g_z of structure A and (b) their derivatives with respect to V_{CG} as a function of V_{BC} at $V_{CG} = -0.1 \text{ V}$. At the nearly symmetric point with $V_{BC} = -0.14 \text{ V}$, $g_i' \simeq 0$.

the hole remains closer to the contact at the lower voltage, i.e. mostly under the central gate for $V_{BC} = 0$ V and in the opposite corner for $V_{BC} = -0.2$ V. An almost symmetric condition is obtained at $V_{BC} = -0.14$ V. All this translates into a peculiar shape of the Rabi frequency vs. V_{BC} curve, as shown next.

Following the procedure illustrated in Appendix C, the g -matrix is computed together with its derivative g' with respect to V_{CG} . The latter is obtained through the repeated calculation of $g(V_{CG})$ for $V_{CG} = V_0$ and $V_{CG} = V_0 \pm \Delta V$. The principal g -factors (see Appendix C) are plotted in Fig. 4(a) for device A as a function of V_{BC} for $V_{CG} = -0.1$ V. As expected from the strong HH character of the wavefunction envelopes, g_z appears to be the largest g -factor. The same transformation that diagonalizes g is then applied onto g' . It turns out that the resulting derivative matrix is almost diagonal. The diagonal elements of g' for structure A are plotted in Fig. 4(b). It can be observed that, at the nearly symmetric point with $V_{BC} = -0.14$ V, $g_i' \simeq 0$.

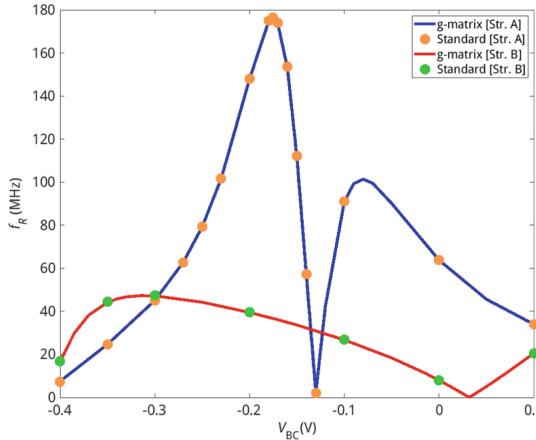


Fig. 5. Rabi frequency vs. V_{BC} for $\mathbf{B} = (0, 1, 1)/\sqrt{2}$ T and $V_{ac} = 1$ mV at $V_{CG} = -0.1$ V. The results obtained with the g -matrix approach (solid lines) are compared with the standard procedure (circles) for both structures. The plot shows excellent agreement. As expected, Rabi frequency is almost zero at $V_{BC} = -0.14$ V in case A. The peak value in case A is much larger than in case B.

4.2 Rabi Frequency Results

Figure 5 shows the plot of the Rabi frequency as a function of V_{BC} for both structures, with $V_{CG} = -0.1$ V, $\mathbf{B} = (0, 1, 1)/\sqrt{2}$ T and $V_{ac} = 1$ mV. The results obtained with the g -matrix formalism (17) are compared with the standard procedure (13). The very good agreement between the two approaches demonstrates that for the applied value of B the device operates in linear regime. As expected, Rabi frequency is almost zero at $V_{BC} = -0.14$ V in case A, due to the particular shape of g_i' . It can be also observed that the peak value in case A is much larger than in case B, suggesting the possibility of an optimization of the gate shape.

5 Conclusions

A framework for the simulation of hole spin qubits based on COMSOL Multiphysics is presented, allowing for the numerical characterization of the device. It can be used as a CAD tool for the analysis of qubit characteristics such as the sensitivities to geometrical parameters, material defects and process variations. Results have been presented for silicon, but the tool can handle other types of semiconductors, e.g. Ge/SiGe.

Appendix A: Hamiltonian Model

The hole states are obtained by diagonalizing the four-bands $\mathbf{k} \cdot \mathbf{p}$ Luttinger-Kohn (LK) Hamiltonian [5, 6] for the valence band. The HH and LH components of the wavefunction are mapped onto the $J_z = \pm \frac{3}{2}$ and $J_z = \pm \frac{1}{2}$ components of a $J = \frac{3}{2}$ total angular momentum, respectively. The total Hamiltonian reads

$$H = H_K + H_Z + V_t(V_{CG}, \mathbf{r}) \quad (1)$$

where H_K is the kinetic term, H_Z the Zeeman term and $V_t(V_{CG}, \mathbf{r})$ the potential energy, which is a function of position and depends on the voltage V_{CG} applied to the central gate. The potential profile is obtained through the solution of Poisson equation.

In the $\{|\frac{3}{2}, \frac{3}{2}\rangle, |\frac{3}{2}, \frac{1}{2}\rangle, |\frac{3}{2}, -\frac{1}{2}\rangle, |\frac{3}{2}, -\frac{3}{2}\rangle\}$ basis set, the H_K component of the Hamiltonian reads [6]

$$H_K = - \begin{bmatrix} P+Q & -S & R & 0 \\ -S^\dagger & P-Q & 0 & R \\ R^\dagger & 0 & P-Q & S \\ 0 & R^\dagger & S^\dagger & P+Q \end{bmatrix} \quad (2)$$

where

$$P = \frac{\hbar^2}{2m_0} \gamma_1 (k_x^2 + k_y^2 + k_z^2) \quad (3)$$

$$Q = \frac{\hbar^2}{2m_0} \gamma_2 (k_x^2 + k_y^2 - 2k_z^2) \quad (4)$$

$$R = \frac{\hbar^2}{2m_0} \sqrt{3} \left[-\gamma_3 (k_x^2 - k_y^2) + 2i\gamma_2 \{k_x, k_y\} \right] \quad (5)$$

$$S = \frac{\hbar^2}{2m_0} 2\sqrt{3} \gamma_3 [\{k_x - ik_y, k_z\}] \quad (6)$$

with $\{A, B\} = \frac{1}{2}(AB + BA)$. Here $\mathbf{k} = (k_x, k_y, k_z)$ is the wavevector, m_0 the free electron mass and $\gamma_1, \gamma_2, \gamma_3$ the Luttinger parameters that characterize the valence band. The reference system axes are defined in Fig. 1. Notice that the x -axis, that is the longitudinal nanowire axis, corresponds to the [110] crystal orientation.

At finite magnetic field \mathbf{B} , the HH and LH components are also mixed by the Zeeman Hamiltonian H_Z

$$H_Z = 2\mu_B(\kappa\mathbf{B} \bullet \mathbf{J} + q\mathbf{B} \bullet \mathbf{J}^3) \quad (7)$$

where μ_B is the Bohr magneton, $\mathbf{J} = (J_x, J_y, J_z)$ is the spin $\frac{3}{2}$ operator, $\mathbf{J}^3 = (J_x^3, J_y^3, J_z^3)$ and κ, q are the isotropic and cubic Zeeman parameters. The \mathbf{J} matrices consistent with the basis set of (1) read:

$$J_x = \frac{1}{2} \begin{bmatrix} 0 & \sqrt{3} & 0 & 0 \\ \sqrt{3} & 0 & 2 & 0 \\ 0 & 2 & 0 & \sqrt{3} \\ 0 & 0 & \sqrt{3} & 0 \end{bmatrix} \quad (8)$$

$$J_y = \frac{i}{2} \begin{bmatrix} 0 & -\sqrt{3} & 0 & 0 \\ \sqrt{3} & 0 & -2 & 0 \\ 0 & 2 & 0 & -\sqrt{3} \\ 0 & 0 & \sqrt{3} & 0 \end{bmatrix} \quad (9)$$

$$J_z = \frac{1}{2} \begin{bmatrix} 3 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & -3 \end{bmatrix} \quad (10)$$

The action of the magnetic field on the orbital motion of the hole is described by the substitution $\mathbf{k} \rightarrow -i\nabla + e\mathbf{A}/\hbar$, where \mathbf{A} is the vector potential. By choosing the Landau gauge $\nabla \bullet \mathbf{A} = 0$ for constant magnetic field \mathbf{B} the vector potential reads:

$$\mathbf{A} = -(yB_z, zB_x, xB_y). \quad (11)$$

It should be noticed that \mathbf{B} enters the Hamiltonian through both the Zeeman term H_Z and the kinetic term H_K via the \mathbf{k} operator.

Appendix B: Direct Calculation of the Rabi Frequency

This Appendix and the following one closely follow the theory outlined in [4]. Consider a QD in a homogeneous and static magnetic field \mathbf{B} . Assume the central gate voltage $V_{CG}(t) = V_0 + V_{ac}\sin(2\pi ft + \varphi)$, with V_0 the reference bias voltage. The Hamiltonian can then be expressed as

$$H(V_{CG}, \mathbf{B}) = H_0(V_{CG}) - \mathbf{B} \bullet \mathbf{M}_1 + \mathcal{O}(B^2), \quad (12)$$

where $\mathbf{M}_1 = (M_{1,x} M_{1,y} M_{1,z})$ is a vector composed of three matrices $M_{1,k} = -\left.\frac{\partial H}{\partial B_k}\right|_{\mathbf{B}=0}$ and is assumed to be independent of V_{CG} . We label $|1\rangle, |0\rangle$ the lowest-energy eigenstates of $H(V_0, \mathbf{B})$. The corresponding eigenenergies are E_1 and E_0 , respectively. At $\mathbf{B} = 0$ the two states are degenerate (Kramers doublet). Degeneracy is broken with the application

of the finite static magnetic field: the two eigenenergies are split by the Zeeman energy $\Delta E = E_1 - E_0 = g^* \mu_B B$, where g^* is the effective gyromagnetic factor that may depend on the orientation of \mathbf{B} . The RF modulation of the voltage $V_{CG}(t)$ at resonance ($hf = \Delta E$) produces coherent oscillations between states $|0\rangle$ and $|1\rangle$ with Rabi frequency

$$f_R = \frac{e}{\hbar} V_{ac} |\langle 1 | D_1 | 0 \rangle|, \quad (13)$$

where $D_1(\mathbf{r}) = \left. \frac{\partial V_t(V_{CG}, \mathbf{r})}{\partial V_{CG}} \right|_{V_{CG}=V_0}$ is the derivative of the potential energy $V_t(V_{CG}, \mathbf{r})$ with respect to the gate voltage V_{CG} .

Appendix C: Rabi Frequency in the g-matrix Formalism

Recalling the $H(V_{CG}, \mathbf{B})$ expression (12), we can also expand the \mathbf{B} -independent term $H_0(V_{CG})$ in powers of $\delta V = V_{CG} - V_0$

$$H_0(V_{CG}) = H_0(V_0) + (\delta V) D_1 + \mathcal{O}(\delta V^2), \quad (14)$$

and we call $|\uparrow\downarrow\rangle, |\downarrow\uparrow\rangle$ the degenerate Kramers doublet eigenstates of $H_0(V_0)$. To first order in \mathbf{B} and V_{ac} , an effective two-states Hamiltonian can be derived having the form

$$H_{eff}(V_{CG}, \mathbf{B}) = \frac{1}{2} \mu_B \boldsymbol{\sigma} \bullet g(V_{CG}) \mathbf{B}, \quad (15)$$

where $\boldsymbol{\sigma}$ is the vector formed of the Pauli matrices and g is a real 3×3 matrix called gyromagnetic matrix. For $V_{CG} = V_0$ the g -matrix can be expressed as

$$g(V_0) = -\frac{2}{\mu_B} \begin{bmatrix} Re\langle \downarrow \downarrow | M_{1,x} | \uparrow \uparrow \rangle & Re\langle \downarrow \downarrow | M_{1,y} | \uparrow \uparrow \rangle & Re\langle \downarrow \downarrow | M_{1,z} | \uparrow \uparrow \rangle \\ Im\langle \downarrow \downarrow | M_{1,x} | \uparrow \uparrow \rangle & Im\langle \downarrow \downarrow | M_{1,y} | \uparrow \uparrow \rangle & Im\langle \downarrow \downarrow | M_{1,z} | \uparrow \uparrow \rangle \\ \langle \uparrow \uparrow | M_{1,x} | \uparrow \uparrow \rangle & \langle \uparrow \uparrow | M_{1,y} | \uparrow \uparrow \rangle & \langle \uparrow \uparrow | M_{1,z} | \uparrow \uparrow \rangle \end{bmatrix}, \quad (16)$$

where g depends on V_0 through the states $|\uparrow\downarrow\rangle, |\downarrow\uparrow\rangle$. The g -matrix can be factorized in the form (singular value decomposition) $g = U g_d V^T$, where U and V are 3×3 unitary matrices and $g_d = \text{diag}(g_x, g_y, g_z)$ is a diagonal matrix, with g_x, g_y and g_z the principal g -factors.

By considering the derivative of g with respect to the gate voltage at $V_{CG} = V_0$, $g'(V_0) = \left. \frac{\partial g(V_{CG})}{\partial V_{CG}} \right|_{V_{CG}=V_0}$, one can express the Rabi frequency as

$$f_R = \frac{\mu_B B V_{ac}}{2\hbar|g(V_0)\mathbf{b}|} |[g(V_0)\mathbf{b}] \times [g'(V_0)\mathbf{b}]|, \quad (17)$$

where $\mathbf{b} = \mathbf{B}/B$. The knowledge of $g(V_0)$ and $g'(V_0)$ is therefore sufficient to compute the Rabi frequency for any magnetic field direction. This procedure is correct to first order in \mathbf{B} and V_{ac} .

References

1. Burkard, G., Ladd, T.D., Nichol, J.M., Pan, A., Petta, J.R.: Rev. Mod. Phys. **95**, 025003 (2023)
2. Fang, Y., Philippopolous, P., Culcer, D., Coish, W.A., Chesi, S.: Mater. Quantum Technol. **3**, 012003 (2023)
3. COMSOL Multiphysics, <https://www.comsol.com/>
4. Venitucci, B., Bourdet, L., Pouzada, D., Niquet, Y.-M.: Phys. Rev. B **98**, 155319 (2018)
5. Lew Yan Voon, L.C., Willatzen, M.: The $k\cdot p$ Method. Springer, Berlin (2009)
6. Martinez, B., Abadillo-Uriel, J.C., Rodríguez-Mena, E.A., Niquet, Y.-M.: Phys. Rev. B **106**, 235426 (2022)



Effect of Phase Noise in Superconducting Qubit Control

Agata Barsotti¹(✉), Gregorio Prociassi¹, Carola Ciaramelletti²,
Paolo Marconcini¹, Leonardo Guidoni³, Simone Paganelli³,
and Massimo Macucci¹

¹ Dipartimento di Ingegneria dell'Informazione, Università di Pisa, via Caruso 16,
56122 Pisa, Italy

agata.barsotti@phd.unipi.it

² Dipartimento di Ingegneria e Scienze dell'Informazione e Matematica, Università
dell'Aquila, via Vetoio, 67010 Coppito-L'Aquila, Italy

³ Dipartimento di Scienze Fisiche e Chimiche, Università dell'Aquila, via Vetoio,
67010 Coppito-L'Aquila, Italy

Abstract. Quantum computer operations, called quantum gates, include qubit rotations, entanglement operations, and measurements, each of which is essential for the implementation of advanced quantum algorithms. However, the effect of phase noise in control operations has not yet been extensively studied. We present a practical phase noise model for performing simulations with control signals affected by phase noise as close as possible to that obtained from a real system.

Keywords: phase noise · control · superconducting qubit

1 Introduction

Quantum computers represent a revolution in the field of computing because of the potentially increased computational capacity that can be achieved due to the quantum mechanical principles on which they are based. The basic unit of information is the qubit (or “quantum bit”), which, unlike a classical bit which can be in one of two states, can exist in a superposition of its two “basis” states, the fundamental state $|0\rangle$ and the excited state $|1\rangle$.

The state of a qubit $|\psi\rangle$ can be represented on the Bloch sphere as:

$$|\psi\rangle = \cos\left(\frac{\theta}{2}\right)|0\rangle + e^{i\varphi} \sin\left(\frac{\theta}{2}\right)|1\rangle, \quad (1)$$

where θ and φ are the polar and the azimuthal angles, respectively.

1.1 Qubit Control

The control of qubits requires the generation of precise radio frequency (RF) pulses that can perform rotations of the qubit state, which can be coherently controlled using microwave signals close to the qubit resonance frequency.

In general, a drive signal can be represented with the expression

$$s(t) = \Re\{f(t)e^{i(2\pi\nu t + \phi)}\} \quad (2)$$

where $f(t)$ is the envelope, ν is the carrier frequency and ϕ is the phase. Drive pulses are designed to perform logical operations on qubits, and their duration, amplitude and phase determine the type of operation performed.

In this paper, we focus on the generation of $N \pi$ -pulses affected by phase noise that would implement N NOT non-ideal gates. Here, rectangular pulses with a duration of 50 ns, an amplitude of about 0.5 a.u., and a carrier frequency of 6 GHz are used. A π -pulse forces a 180° rotation around a specific axis of the Bloch sphere, in our case the X-axis, and thus leading to an inversion of the state of the qubit, see Fig. 1(a). In case the π -pulse is affected by phase noise and the qubit is initialized in the fundamental state $|0\rangle$, the final state will not be $|1\rangle$, but a different state, due to unwanted rotations around the X, Y, and Z axes, see Fig. 1(b). Phase noise has been directly applied to the pulse envelope components, which is equivalent to applying it to the carrier phase.

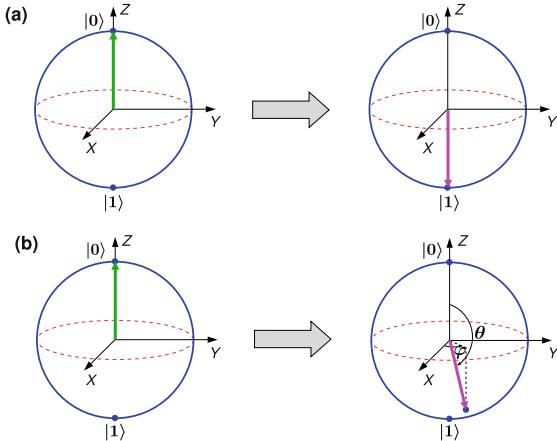


Fig. 1. Representation on the Bloch sphere of the state evolution due to (a) an ideal π -pulse and (b) a π -pulse affected by phase noise.

1.2 Phase Noise

Phase noise $\Phi(t)$ is a random fluctuation affecting the phase of the periodic carrier signal $v(t) = V_0 \cos(\omega_0 t + \Phi(t))$, and is the major non-ideality appearing in the generation of the control and readout pulses. Due to this phenomenon, the signal energy spreads into sidebands of the center frequency (corresponding to the long-term average frequency). Since the signals generated by every electronic oscillator are affected by phase noise, the spectrum of a “real” sine wave is never a

single line, but has a finite width. The phase noise level is a fundamental quality parameter of any signal-generating circuit and it is particularly important in communication systems and in superconducting qubit control systems, for which phase accuracy is critical for proper system operation (Ref. [1]).

The Hamiltonian analysis performed in Ref. [2] provides a first assessments of the effect of control-signal non-idealities on qubit coherence and error rates. Such a study, along with a more general analysis of non idealities due to qubit controllers (Ref. [3]), has raised the attention on the relevance that phase noise may have on the fidelity of qubit operations. These analyses assess the effect of control-signal non idealities on qubit coherence and on error rates, allowing to establish signal quality parameters that are relevant to achieve assigned fidelity figures. It turns out that, in order to increment the coherence times, the containment of phase noise in control signals can be of paramount importance.

2 Phase Noise Modeling

Realizations of the phase noise process with the desired power spectral density (PSD) are generated in the discrete-time domain as shown in Fig. 2 by filtering a white noise process through a Linear and Time Invariant (LTI) system.

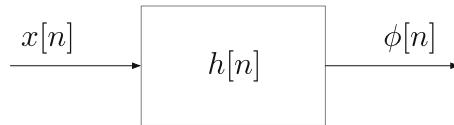


Fig. 2. Discrete-time LTI filter.

In fact, given the LTI filter with impulse response $h[n]$, it is well known (see, e.g., Ref. [4]) that the PSD $S_\phi(\omega)$ of the output process is given by:

$$S_\phi(\omega) = S_x(\omega) |H(e^{i\omega})|^2 \quad (3)$$

where $H(e^{i\omega})$ is the frequency response of the filter. If $x[n]$ is a white noise process with normalized variance $\sigma_x^2 = 1$, Eq. (3) becomes:

$$S_\phi(\omega) = |H(e^{i\omega})|^2, \quad (4)$$

whose inversion gives a simple way for synthesizing a random process with given PSD. In other words, in order to generate a random process with PSD $S_\phi(\omega)$ it is sufficient to synthesize the *coloring* filter $h[n]$ (or, equivalently, its system function $H(z)$), so that its amplitude response is:

$$|H(e^{i\omega})| = \sqrt{S_\phi(\omega)} \quad (5)$$

Generalized Linear Phase (GLP) FIR filters are a convenient class of LTI systems to implement according to given spectral requirements. Their frequency response is given by:

$$H(e^{i\omega}) = A(\omega)e^{i\phi_0 - i\omega M/2}, \quad (6)$$

where $A(\omega)$ is the (real-valued) amplitude function, M is the (integer) filter order, and ϕ_0 is equal to 0 or $\pi/2$. Depending on the evenness value of M and the initial phase ϕ_0 , GLP filters can be classified into types I, II, III, and IV. There exist many techniques to design GLP FIR filters that approximate a desired frequency response. The *windowing* technique is very simple to implement and it consists of setting the desired frequency response as:

$$H_D(e^{i\omega}) = A_D(\omega)e^{i\phi_0 - i\omega M/2}, \quad (7)$$

computing the ideal (IIR) impulse response $h_d[n]$:

$$h_D[n] = \frac{1}{2\pi} \int_{-\pi}^{\pi} H_D(e^{i\omega}) e^{i\omega n} d\omega \quad (8)$$

and multiplying (*windowing*) $h_d[n]$ by the finite length window $w[n]$ of length $M + 1$:

$$h[n] = h_D[n]w[n] = \begin{cases} h_D[n]w[n] & 0 \leq n \leq M \\ 0 & \text{otherwise} \end{cases} \quad (9)$$

Note that when $w[n]$ is the rectangular window, the technique minimizes the mean square error:

$$\epsilon^2 = \frac{1}{2\pi} \int_{-\pi}^{\pi} |H_D(e^{i\omega}) - H(e^{i\omega})|^2 d\omega \quad (10)$$

Therefore, in order to generate a random process with the desired PSD $S(w)$, it is sufficient to set $A_d(w) = \sqrt{S(w)}$ in Eq. 7, select the type and the order of the filter and the window sequence to obtain the impulse response $h[n]$ of the coloring filter from Eq. (9).

2.1 Sample Rate Conversion

Discrete time processing of analog signals assumes to select a sampling period F_s which satisfies the Nyquist relation. In the above described procedure, to generate a 500 MHz band-limited phase noise signal $\phi[n]$ it is sufficient to set the sample rate to $F_s = 1$ GHz. However, in our study the random noise is used to modulate a carrier with higher analog frequency ν . Discrete time processing of the modulated signal requires a higher sample rate, which, in turn, calls for resampling of the sequence $h[n]$. Given that the new sampling rate is higher than the original one, one can observe that this is always possible by reconstructing the analog signal through DAC conversion and then resampling. However, the same result can be conveniently obtained in the discrete time domain. In particular, if the new sampling rate F'_s is an integer multiple of F_s (i.e., $F'_s = I F_s$), sampling

rate conversion can be obtained according to the scheme of Fig. 3, in which the impulse response $h[n]$ is first *upsampled* by a factor I^1 and then filtered by a low-pass filter with cutoff frequency π/I .

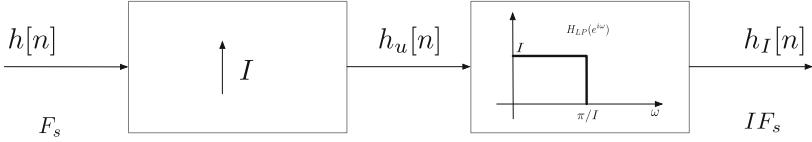


Fig. 3. Sampling Rate Increase of a Factor I in the Discrete-Time Domain

2.2 $1/f$ -Like Phase Noise

We generated base-band random noise by assuming the sampling period of 1 ns, corresponding to a sampling rate of $F_s = 1$ GHz. In order to approximate a $1/f$ -like PSD while keeping the length of the impulse response of the coloring filter at reasonable values, we chose:

$$S(\omega) = \frac{1}{\omega + \omega_0} \quad (11)$$

and we set $A_d(\omega) = \sqrt{1/(\omega + \omega_0)}$ in Eq. (7) accordingly. In addition, given the shape of $S(\omega)$, we selected $\phi_0 = 0$ and even order M (type I filter) in Eq. (7) as well as the rectangular window in Eq. (9).

We first generated a random sequence $x[n]$ of uncorrelated values with a Gaussian amplitude distribution, using the method due to von Neumann [5,6]. As a result of their uncorrelation, a white spectrum is obtained.

The sequence $x[n]$ was then processed by the coloring filter $h[n]$ in which we selected $\omega_0 = 2\pi f_0/F_s$ to have an analog PSD cutoff frequency of 159 KHz after digital to analog conversion.

This output sequence $\phi[n]$ (see Fig. 4b) represents the random phase of the drive signal that we use in our quantum calculations; in particular, $\phi[n]$ is used as direct input for the Qiskit-Dynamics simulations.

In order to verify the result of the modulation of a carrier with the generated base-band noise, we have first interpolated $\phi[n]$ with a shorter time step ($T_s = 83.3333$ ps), suitable for the discretization of the modulated signal (with a carrier

¹ Numerical upsampling of the sequence $h[n]$ by an integer factor I is simply obtained by inserting $I - 1$ zeros between any two samples of $h[n]$, namely

$$h_u[n] = \begin{cases} h[n/I] & n = 0, \pm I, \pm 2I, \dots \\ 0 & \text{otherwise} \end{cases}$$

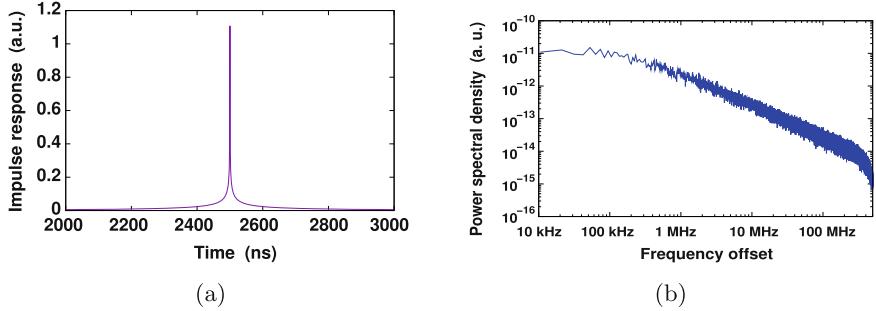


Fig. 4. (a) Impulse response of a FIR filter in order to obtain noise with $1/f$ spectra
(b) Power spectral density of baseband generated phase noise

at 4 GHz). We have then computed the Fast Fourier Transform (FFT) [7] of the resulting signal ($\cos(2\pi\nu nT_s + \phi[n])$), verifying the presence of sidebands around the carrier with a shape consistent with the spectrum of the generated phase noise. From the spectrum obtained with the FFT, we evaluate the phase noise amplitudes in values in dBc/Hz (dB carrier per Hz, i.e. the ratio in dB of the noise power within a bandwidth of 1 Hz around the considered offset from the carrier to the carrier power), to be compared with the values from measurements on actual frequency synthesizers (Fig. 5).

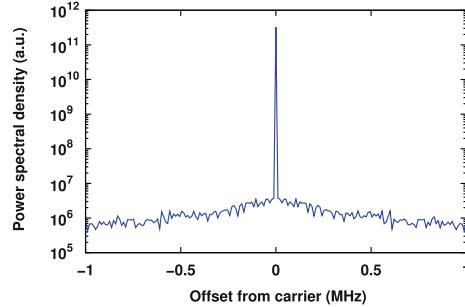


Fig. 5. Power spectral density of a carrier affected by phase noise with a corner frequency of 159 kHz

3 Qiskit-Dynamics Simulations

We performed simulations with Qiskit-Dynamics, which allows us to simulate the time evolution of the qubit state using the Schrödinger equation. In the simulations, we set the initial state of the qubit to $|0\rangle$ and tune the pulse amplitude for a sequence of N ideal rectangular pulses implementing N cascaded NOT

gates, in order to achieve a fidelity as close to the ideal value as possible in the absence of phase noise. The phase noise values obtained from our noise model are applied to the real and imaginary components of the rectangular pulses and then we simulate the qubit evolution, evaluating the fidelity of the resulting states.

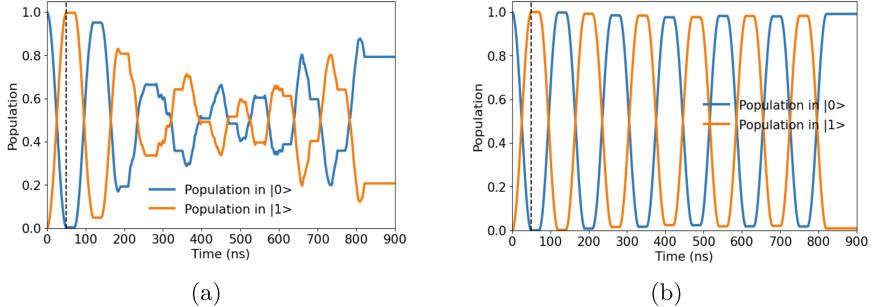


Fig. 6. Time evolution of the qubit population during the 12 applied pulses affected by phase noise with $1/f$ spectrum a corner frequency of 159 kHz and equal to -72.6 dBc/Hz in (a) and to -84.6 dBc/Hz in (b) at a 100 kHz offset.

We have performed simulations for a phase noise with a $1/f$ spectrum, a 159 kHz corner frequency, and with amplitudes of -72.60 dBc/Hz and -84.60 dBc/Hz at a 100 kHz offset. For a single applied pulse, the fidelity is not significantly degraded, being 99.36% and 99.64%, while for 12 pulses, fidelities of 79.29% (Fig. 6a) and 99.11% (Fig. 6b) are obtained, respectively.

4 Conclusions

We have set up a numerical simulation for the analysis of the effect of phase noise on the fidelity of superconducting qubits. In particular, we have synthesized phase noise realizations with controlled amplitude and spectral characteristics. Initial tests performed with Qiskit-Dynamics with the application of rectangular control pulses affected by phase noise have shown, assuming a $1/f$ spectrum down to 159 kHz, that, as long as the noise is below about -70 dBc/Hz at 100 kHz, the effect on the fidelity after a single pulse is substantially negligible. A significant loss of fidelity is observed instead over a series of 12 pulses. However, if the noise is below -90 dBc/Hz, fidelity is maintained at relatively high values even after 12 pulses. Future work will include considering different types of pulses, a $1/f$ noise spectrum with a lower corner frequency (which will require a larger number of noise samples), and more general phase noise spectra, such as those measured on actual qubit control instrumentation.

Acknowledgements. This work was partially supported by the Italian Ministry of the University and Research (MUR) in the framework of the CrossLab and the FoReLab

projects (Departments of Excellence). Financial support is also acknowledged from the European Union, Next-GenerationEU, National Recovery and Resilience Plan (NRRP), Mission 4 Component 2 Investment N. 1.4, CUP N. I53C22000690001, through the National Centre for HPC, Big Data and Quantum Computing (“Spoke 10: Quantum Computing”). This work was supported also by the U.S. Department of Energy, Office of Science, National Quantum Information Science Research Centers, Superconducting Quantum Materials and Systems Center (SQMS) under Contract No. DEAC02-07CH11359 and by Qub-IT, a project funded by the Italian Institute of Nuclear Physics (INFN) within the Technological and Interdisciplinary Research Commission (CSN5).

References

1. Rubiola, E.: Phase Noise and Frequency Stability in Oscillators. Cambridge University Press, Cambridge (2008)
2. Ball, H., Oliver, W., Biercuk, M.: The role of master clock stability in quantum information processing. *npj Quant. Inf.* **2**, 16033 (2016). <https://doi.org/10.1038/npjqi.2016.33>
3. Dijk, J.P., et al.: Impact of classical control electronics on qubit fidelity. *Phys. Rev. Appl.* **12**, 044054 (2019). <https://doi.org/10.1103/PhysRevApplied.12.044054>
4. Manolakis, D.G., Ingle, V.K.: Applied Digital Signal Processing: Theory and Practice. Cambridge University Press, Cambridge (2011)
5. Von Neumann, J.: Various techniques used in connection with random digits. In: National Bureau of Standards Applied Mathematics Series, No. 12, p. 36, U.S. Government, Printing Office, Washington, D.C. (1951)
6. Knuth, D.: The Art of Computer Programming: Volume 2: Seminumerical Algorithms, p. 122. Addison Wesley, Upper Saddle River (1998)
7. Press, W.H., Teukolsky, S.A., Vetterling, W.T., Flannery, B.P.: Numerical Recipes: The Art of Scientific Computing. Cambridge University Press, Cambridge (2007)

Microwave Electronics



Advanced Interconnect Solutions for Millimetre-Wave Low-Noise Amplifiers

Patrick Ettore Longhi^(✉), Walter Cicognani, Sergio Colangeli,
Peiman Parand, Antonio Serino, and Ernesto Limiti

Department of Electronic Engineering, University of Roma Tor Vergata, Rome, Italy
longhi@ing.uniroma2.it

Abstract. Advanced integrated interconnect solutions are proposed in this paper targeting Low-noise amplifiers (LNA) operating at 100 GHz and above. A demonstrator GaAs LNA assembled on PCB is designed and tested showing more than 20 dB gain and typically 5–6 dB Noise Figure in 92–114 GHz, accounting also for the losses of the vertical RF interconnects (hot vias). The RF vertical interconnect design challenges are described.

Keywords: Low-Noise Amplifiers · GaAs · RF interconnect · MMIC · W band

1 Introduction

The recent introduction of 5G cellular communication systems has enabled high data rate links, up to 10 Gbps. To cope with this explosive growth in data traffic, mobile network operators will need to expand their cellular network infrastructures. This outstanding demand for data links requires the use of millimeter-wave frequencies to support wireless links for different applications and use cases; in particular, E band (71–76 and 81–86 GHz) is going to be exploited for gigabit-per-second Point to Point (PtP) wireless communications over links with hop distances of up to a few kilometers, such as those suitable for backhaul infrastructures. However the significant increase in backhaul capacity, as needed to enable an effective 5G network deployment, also requires a move to wider bandwidth solutions. The constant pressure to improve performance levels results in a need for more spectrum, and a more efficient use of it in microwave backhaul and fixed-service systems. The use of frequency bands is governed by regulatory recommendations on channel arrangements. Beyond 100 GHz, part of the spectrum has been recently allocated by ITU-R for fixed service systems, in the 92–114.25 GHz and 130–174.8 GHz ranges, commonly referred to as the W- and D-band, respectively. Therefore, an enormous amount of additional bandwidth becomes available. W band offers 17.9 GHz of available spectrum (92 to

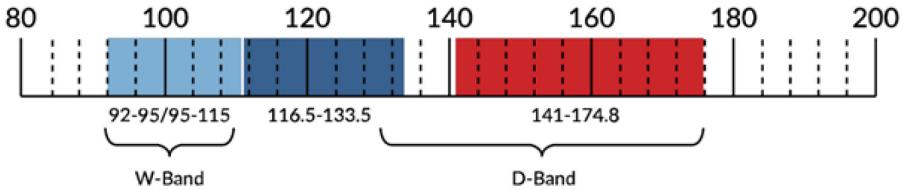


Fig. 1. Allocated spectrum (in GHz) for Point-to-Point radio links at W- and D-band.

114 GHz), while D-band hosts a total of 31.7 GHz (130 to 175 GHz), as graphically depicted in Fig. 1.

The key challenge for the industry becomes to develop and supply technology cost-effective solutions with high performance in terms of transmitted power, linearity, noise figure, bandwidth, operating frequency range, and last but not least packaging cost. Focusing on the latter aspect, to lower the costs and allow full integration of a complete radio-system, GaAs MMIC components at E band were traditionally assembled directly onto printed wire boards (PWB) with a technology called Direct-Chip-Attach (DCA) or Chip-on-Board (COB). If multiple chips are involved, the solution is also known as Multi-chip Module (MCM) or System-in-Package (SiP). Chips can be assembled on the PWB using the conventional wire-bonding, by adopting suitable parasitic compensation design techniques to mitigate the unavoidable performance degradation effects. The associated packaging design and manufacturing technologies include solder joint integrity inspection, testing, rework, thermal management, mechanical characterization, chip encapsulation and reliability assessment. Research here described at W band relies on new technologies that provide increased performance and higher levels of integration of components such as Low-Noise Amplifiers (LNAs). To lower the cost of the radio equipment and allow the full integration of the front-end in a complete SIP solution, it is desirable to integrate this component into packages with a suitable assembling technology which is able to deliver repeatable performance while introducing a reduced degradation due to interconnections and integration. The best design solutions are investigated to shift to higher frequencies and develop a chip-to-substrate interconnection technology with unprecedented performance and packaging results. Consequently, the effect of RF wire bonds is either accounted for by design [7] or needs to be replaced with less inductive and radiative components. Through-substrate hot-vias are one possibility, since their inductance and attenuation is less than that of a wire-bond. This topic is gaining interest in the scientific community [1–5, 13, 17] as designers try to cope with wire bond inductance in millimeter-wave designs.

2 Chip-on-Board Design

The MMIC LNA design goals are: full telecom W band operation (92–115 GHz), 20 dB gain, minimizing noise figure within the technology's inherent limits and

direct connection to the bottom layer Printed Circuit Board (PCB) using a kind of through-substrate RF interconnection from now on referred to as Hot Via (HV). Given this last constraint, we opted for a new GaAs process (PP10–20) recently made available from WIN semiconductors commercial foundry [16].

The first step consists in defining the stack-up used for the MMIC-to-PCB interconnect. The stack-up is shown in Fig. 2. The bottom layer (PCB) is a 4-mil thick substrate having $\epsilon_r = 3.11$ and 0.004 loss tangent. The propagation over the PCB is in coplanar Waveguide with Ground (CPWG) to reduce the effect of substrate losses due to the rather high loss tangent. The top layer is the 2-mil thick GaAs MMIC in WIN's PP10–20 technology.



Fig. 2. PCB and MMIC cross-section stack-up.

2.1 Selected MMIC Technology

The circuit is fabricated on 150 mm GaAs wafers using the WIN Semiconductors PP10–20 pHEMT platform. The core of this technology is a 160 GHz f_T , 0.1 μm -gate D-mode transistor and is qualified for 4 V operation. This technology offers two interconnect metals with air bridge crossovers, monolithic PN diodes for on-chip ESD protection, precision thin film resistors, MIM capacitors, through-wafer vias for low-inductance ground connections and can be manufactured with through-chip RF transitions. This latter feature (through-chip RF transitions) is the key-enabler for this design.

2.2 Interconnect Design

The design of the interconnect circuit to compensate the inductive effect of the HV is rather critical. Different pad sizes (red rectangle in Fig. 3) are evaluated to improve the return loss in the operating bandwidth. The black ellipse represents the HV while the light blue area is the central conductor of the CPWG on PCB designed to obtain 50 Ω characteristic impedance. The width of the central conductor is 190 μm while the gap is 100 μm . The solution to optimize the transition's return loss at W band is a square patch having 160- μm side. The rather thin microstrip line (in red in the picture) is designed to provide 50 Ω characteristic impedance on the 2-mil thick GaAs substrate, and its width is fixed to 35 μm . The typical return loss in the operating bandwidth is 16 dB while the insertion loss of the structure depicted in Fig. 3 is 0.8 dB. The estimated loss of

the HV transition is 0.4–0.5 dB, coherently with data in [4,14], while the rest is losses due to propagation on the PCB and MMIC.

The bottom side of the MMIC is shown in Fig. 4. The RF conductor is isolated from the metallic ground through a 80 μm wide isolated ring. The same interconnect technology is used to provide bias functionality; in this latter case no EM study is performed due to the DC nature of the provided signal.

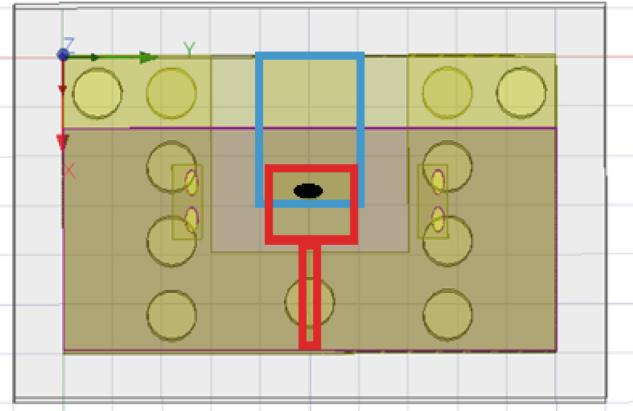


Fig. 3. Hot via transition geometrical study in 3D EM environment (ANSYS HFSS student version).

2.3 MMIC LNA Design

The MMIC LNA is designed exploiting a 4-stage topology to reach the prescribed 20-dB gain level [6,9,12]. Source inductive degeneration is applied on the first three stages to ease the difficult trade-off between signal and noise match [8, 10, 11] over the rather broad operating bandwidth. Optimum noise performance is assured by selecting an input termination that minimizes noise measure [8, 15]. The final stage is with the source directly grounded to provide additional gain and improve linearity performance. The selected transistors are $2 \times 25 \mu\text{m}$ devices biased at 10 mA drain current and +2 V drain-to-source voltage. Series capacitors are inserted acting as DC-block components while providing also RF matching functionality. The MMIC micro-photograph is shown in Fig. 5 where the HV interconnect is highlighted in the red inset at the RF input (left side). The same HV technology is applied to provide drain and gate bias voltages from the top and bottom pads.

3 Chip-on-Board Test

The DUT (LNA & PCB) shown in Fig. 6 is characterized in the nominal bias conditions. Red dashed lines are provided to identify the reference planes for

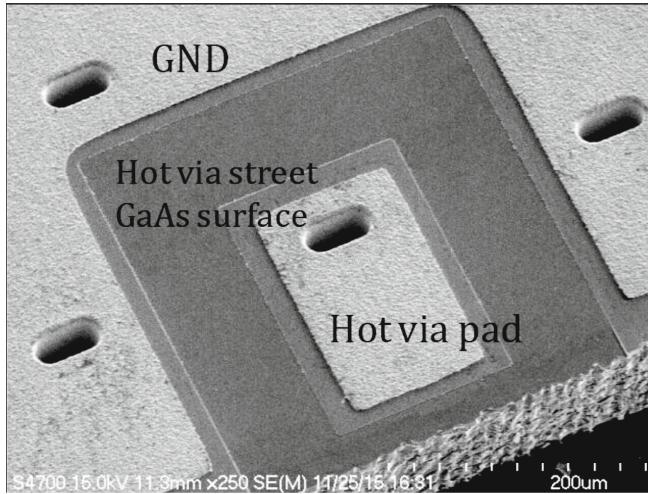


Fig. 4. Hot via bottom layer view.

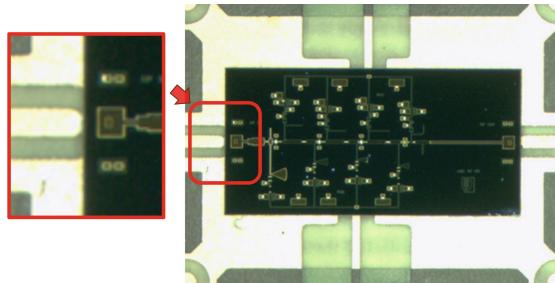


Fig. 5. W band LNA MMIC assembled on PCB with hot-via vertical RF interconnects. A zoom of the hot-via interconnect is provided in the inset. MMIC size is 4 mm × 2 mm.

linear and noise characterization. The effect of the CPWG lines are not de-embedded in the characterized data at the moment. Gain and return loss are in good agreement between measured data (solid lines) and simulations (dotted lines). The gain is greater than 20 dB and the return loss is typically 12 dB from 90 to 115 GHz, as seen in Fig. 7 (left).

Preliminary NF characterization, Fig. 7 (right), shows a typical value of 5.5 up to 105 GHz and around 6–7 dB from 105 to 110 GHz. This NF value is interesting considering the 0.5 dB losses introduced by the transition that are not usually accounted for in a pure-MMIC solution and more than 1 dB loss of the rather long coplanar wave transmission line on the input side of the PCB.

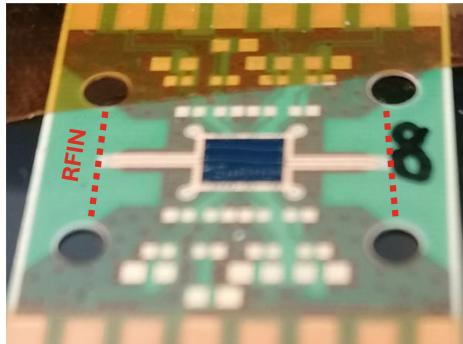


Fig. 6. DUT: W band LNA MMIC assembled on PCB with hot-via vertical RF interconnects. Red dashed lines are provided to identify the reference planes used for linear and noise characterization.

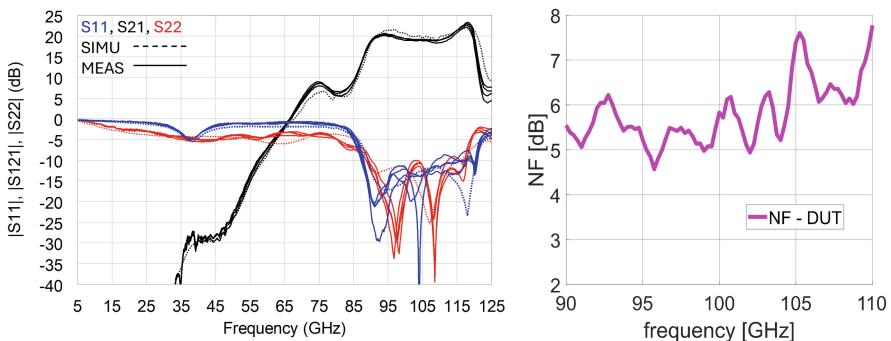


Fig. 7. W band LNA MMIC assembled on PCB linear characterization (left) and NF data (right). Design bandwidth is 92–115 GHz.

4 Conclusions

Design solutions and technological consideration of a Low-Noise Amplifier using Hot Via interconnects at W band is provided in this paper. The DUT's measured gain is 20 dB and its NF is 5–6 dB. The MMIC is realized in WIN's PP10–20 technology.

Acknowledgment. The Authors wish to thank Dr. David Danzilio and the Customer Engineering Department at WIN Semiconductors Corp. for granting access to PP10–20 technology within the “mm wave for select universities” programme.

References

- Alleaume, P., Toussain, C., Auvinet, C., Domnesque, D., Quentin, P., Camiade, M.: Millimetre-wave hot-via interconnect-based gaas chip-set for automotive radar

- and security sensors. In: 2008 European Microwave Integrated Circuit Conference, pp. 52–55 (2008). <https://doi.org/10.1109/EMICC.2008.4772226>
- 2. Bessemoulin, A.: Design data for hot-via interconnects in chip scale packaged mmics up to 110 ghz. In: 34th European Microwave Conference, 2004, vol. 1, pp. 97–100 (2004)
 - 3. Bessemoulin, A., Gaessler, C., Gruenenpuett, C., Reig, B.: Hot-via interconnects: a step toward surface mount chip scale packaged mmics up to 110 ghz. In: IEEE Compound Semiconductor Integrated Circuit Symposium, 2004, pp. 237–240 (2004). <https://doi.org/10.1109/CSICS.2004.1392548>
 - 4. Bessemoulin, A., Maréchal, L., Stieglauer, H., Poilvert, P., Auxemery, P., Viaud, J.: Demonstration of reproducible millimeter-wave smt chip scale package using hot-via mmics and plastic bga encapsulation. In: 2021 51st European Microwave Conference (EuMC), pp. 6–9 (2022). <https://doi.org/10.23919/EuMC50147.2022.9784210>
 - 5. Bessemoulin, A., Rodriguez, M.C., Mahon, S.J., Parker, A.E., Heimlich, M.C.: Soldered hot-via e-band and w-band power amplifier mmics for millimeter-wave chip scale packaging. In: 2016 IEEE MTT-S International Microwave Symposium (IMS), pp. 1–4 (2016). <https://doi.org/10.1109/MWSYM.2016.7540025>
 - 6. Cicognani, W., Giannini, F., Limiti, E., Longhi, P.E.: Full w-band high-gain lna in mhemp mmic technology. In: 2008 European Microwave Integrated Circuit Conference, pp. 314–317 (2008). <https://doi.org/10.1109/EMICC.2008.4772292>
 - 7. Cicognani, W., Longhi, P.E., Colangeli, S., Limiti, E., IEEE, S.M.: Q/v band lna for satellite on-board space applications using a 70 nanometers gaas mhemp commercial technology. *Microw. Opt. Technol. Lett.* **60**(9), 2185–2190 (2018). <https://doi.org/10.1002/mop.31317>
 - 8. Colangeli, S., Longhi, P.E., Cicognani, W., Limiti, E.: On the optimum noise-gain locus of two-ports. *IEEE Trans. Microw. Theory Tech.* **67**(6), 2284–2290 (2019). <https://doi.org/10.1109/TMTT.2019.2910066>
 - 9. Karkkainen, M., et al.: Coplanar 94 ghz metamorphic hemt low noise amplifiers. In: 2006 IEEE Compound Semiconductor Integrated Circuit Symposium, pp. 29–32 (2006). <https://doi.org/10.1109/CSICS.2006.319911>
 - 10. Lehmann, R., Heston, D.: X-band monolithic series feedback lna. *IEEE Trans. Microw. Theory Tech.* **33**(12), 1560–1566 (1985). <https://doi.org/10.1109/TMTT.1985.1133257>
 - 11. Longhi, P.E., Pace, L., Colangeli, S., Cicognani, W., Limiti, E.: Novel design charts for optimum source degeneration tradeoff in conjugately matched multistage low-noise amplifiers. *IEEE Trans. Microw. Theory Tech.* **69**(5), 2531–2540 (2021). <https://doi.org/10.1109/TMTT.2021.3068285>
 - 12. Longhi, P.E., et al.: Modelling, design, and characterization challenges of a gallium arsenide high-linearity low-noise amplifier with gain control at w-band. In: 2023 18th European Microwave Integrated Circuits Conference (EuMIC), pp. 378–381 (2023). <https://doi.org/10.23919/EuMIC58042.2023.10289083>
 - 13. Mahon, J.C., Clark, M., Katzin, P.: A surface mount 45 to 90 ghz low noise amplifier using novel hot-via interconnection. In: 2018 IEEE/MTT-S International Microwave Symposium - IMS, pp. 293–296 (2018). <https://doi.org/10.1109/MWSYM.2018.8439302>
 - 14. Milner, L.E., Mehta, S.G., Hall, L.T., Mahon, S.J., Chakraborty, S., Heimlich, M.C.: Optimised hot-via transition with 20 db return loss for mmic packaging from dc to 110 ghz. In: 2021 51st European Microwave Conference (EuMC), pp. 14–17 (2022). <https://doi.org/10.23919/EuMC50147.2022.9784265>

15. Poole, C., Grammenos, R.: Correct equations for minimum noise measure of a microwave transistor amplifier. *IEEE Trans. Microw. Theory Tech.* **70**(2), 1361–1366 (2022). <https://doi.org/10.1109/TMTT.2021.3129496>
16. Serino, A., et al.: Fet characterization and modeling targeting low-noise w-band applications. In: 2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), pp. 1–4 (2023). <https://doi.org/10.1109/INMMIC57329.2023.10321768>
17. Wu, W.C., et al.: 60 ghz broadband ms-to-cpw hot-via flip chip interconnects. *IEEE Microwave Wirel. Compon. Lett.* **17**(11), 784–786 (2007). <https://doi.org/10.1109/LMWC.2007.908053>



A Wideband L-band Integrated Low Noise Amplifier

Sergio Colangeli^(✉), Patrick E. Longhi, Walter Ciccognani, and Ernesto Limiti

University of Roma Tor Vergata, Department of Electronics, Rome, Italy
colangeli@ing.uniroma2.it

Abstract. Collecting accurate Earth surface data is crucial for climatology and weather modelling, especially in cold regions. However, recent missions have revealed Radio Frequency Interference (RFI) challenges within the protected L-Band, necessitating robust payloads capable of operating amidst strong RFIs. This study proposes an L-band packaged low-noise amplifier (LNA) designed to maintain performance across the 0.4 GHz–2 GHz band, using a GaN-on-SiC HEMT process. The LNA design employs a cascode architecture and achieves a small-signal gain of 20.7 ± 0.18 dB with a worst-case noise figure of 0.9 dB. To enhance survivability, an integrated limiter is added ahead of the LNA, forming a compact chain with promising performance for radiometric measurements in challenging RF environments. Chip size is $3 \times 2 \text{ mm}^2$.

Keywords: GaN-on-Sic · L band · LNA · MMIC · high survivability

1 Introduction

The importance of Earth's surface data for understanding climatology and improving weather models, especially in cold regions, cannot be overstated. Retrieving such data requires low frequency RF payloads, like radiometers in the L-band range. However, recent missions have revealed significant Radio Frequency Interference (RFI) issues within the protected L-band, necessitating the development of payloads with wider bandwidths capable of operating in the presence of strong RFIs without failure. This calls for an L-band packaged low-noise amplifier (LNA) with improved signal handling capabilities to maintain performance across the 0.4 GHz–2 GHz band, ensuring accurate radiometric measurements despite RFI contamination.

An extensive review of the state of the art in the open literature [1–12], evidenced a predominance of GaN-based technologies in this area. With particular reference to the adopted topologies, the majority of these works present variations of the cascode architecture with resistive feedback. However, alternative solutions are also present, and in particular common-source [1, 2, 4, 10–12] and distributed amplifier [3]. Accordingly, a comparison of candidate technologies made available by European and worldwide foundries was carried out, ending up in the selection of United Monolithic Semiconductors (UMS)'s GaN-on-SiC HEMT process with 150-nm gate length (commercial

name GH15). Also, three possible design solutions were compared, namely, broadband dissipative matching [13], distributed or chain-of-distributed-stages architecture [14, 15], and cascode architecture, the last of which was eventually chosen for the actual design. The key design goals are high survivability and low noise figure over the whole 0.4 GHz–2 GHz band, while minimizing power consumption.

2 Design of the LNA and of an Ancillary Limiter

The adopted 150 nm GaN-on-SiC HEMT process is featured by a typical cutoff frequency (f_T) in excess of 35 GHz and has an optimal transistor drain-source voltage (V_{DS}) of 20 V. The designed LNA consists of two $8 \times 100 \mu\text{m}$ transistors in cascode topology. Either stage is operated at a gate-source bias of $V_{GS} = -2.7$ V, a drain-source voltage of $V_{DS} = +9.3$ V and a drain current of 70 mA. The amplifier requires a supply $V_{DD} = +20$ V and a bias $V_{GG} = -4$ V, from which the two gate voltages are derived internally through resistive dividers. The nominal power consumption of the LNA is $P_{DC} = 1.4$ W.

It is worth noting that V_{GG} and ground pads are placed along the North side of the chip, but a V_{DD} pad is missing. In fact, the V_{DD} voltage is supplied through the output RF port. This is a consequence of one of the main difficulties faced in the design, i.e., the lack of DC-block capacitors sufficiently large to exhibit a low impedance at the lower end of the bandwidth but simultaneously associated with negligible parasitics. Thus, they were not integrated in the LNA but left as external components. As for the output, a DC-feed inductor is also required. On the one hand, the input DC block is not strictly required (depending on the preceding elements in the complete chain); on the other hand, the external output bias-T does not impact noise figure significantly due to its position. Finally, it is to consider that this solution posed some constraints on the possible topologies of the output matching network, which was required to pass the supply voltage.

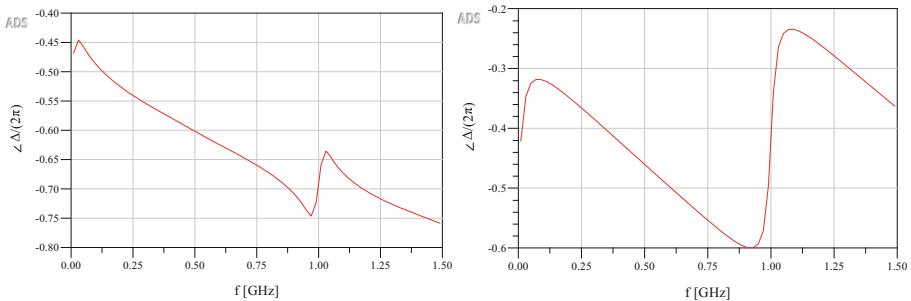


Fig. 1. Normalized phases of the sub-factors Δ_i , as defined in [17], for the large-signal stability test of the LNA at $P_{av} = 10$ dBm, $f_{LS} = 1$ GHz. Left: Δ_1 . Right: Δ_2 .

By virtue of the adopted cascode topology, no DC blocks were required between the two stages; a virtual-ground capacitor was inserted in correspondence with the gate of the second-stage transistor, but its value did not prove as critical. As a further deviation

from an ideal common-gate stage, a small resistor was added in series to the gate to solve a stability problem, namely, the lack of inherent stability, evidenced by the Ohtomo test [16].

After stabilization, the large-signal stability of the LNA was investigated through the method presented in [17]. As an example, Fig. 1 shows the normalized phases of the sub-factors Δ_i computed for the two active devices, when the LNA is operated nominally and driven by an available input power $P_{av} = 10$ dBm at frequency $f_{LS} = 1$ GHz. The phases indicate no encirclements of the origin and, therefore, stability, provided that the two active devices are inherently stable under the given large-signal regime. It is interesting to note that, as opposed to the typical case of 2-port active sub-blocks, in this situation both active devices are considered as 3-port sub-blocks: this is necessary for the common-gate stage, but the same representation was adopted for the common-source stage mainly for ease of implementation.

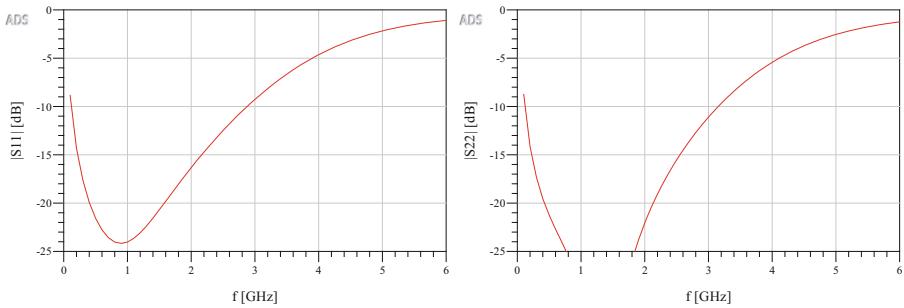


Fig. 2. Simulated matching of the limiter. Left: $|S_{11}|$. Right: $|S_{22}|$.

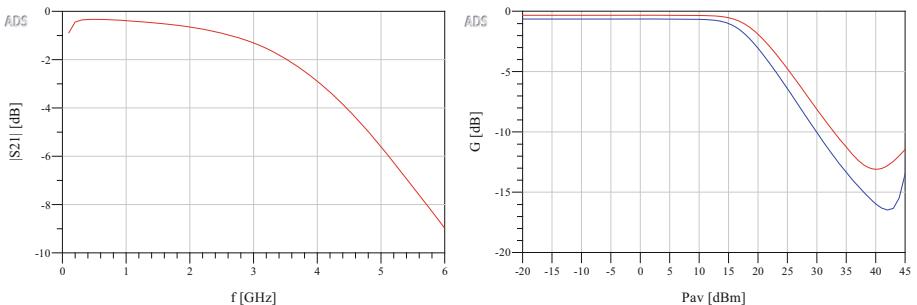


Fig. 3. Simulated loss of the limiter. Left: small-signal loss over frequency. Right: large-signal loss over input available power, at lower frequency (0.4 GHz) and upper frequency (2.0 GHz).

Based on electromagnetic (EM) simulations in ADS Momentum, the LNA as described so far achieves across the whole bandwidth (0.4 GHz–2 GHz) a small-signal gain of 20.65 ± 0.15 dB, input and output return losses better than 12 dB and 13 dB, respectively, and a worst-case noise figure of 0.9 dB. As to survivability, an extensive investigation was conducted, analyzing the critical breaking parameters of the active

and passive components. First of all, it was observed that, under large excitations, the drain current was prone to exceed the associated maximum ratings: to correct for this, a series resistor (17Ω) was added in series between drain of the common-source transistor and the source of the common-gate transistor. No way was found, on the other hand, to solve at LNA the problem of very negative instantaneous voltages across the gate-source junction of the first stage, which set to 27 dBm (worst case at the upper frequency) the maximum allowable input driving level.

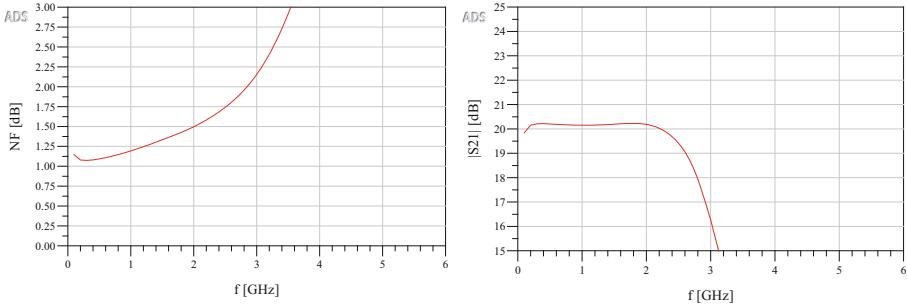


Fig. 4. Simulated noise figure and small-signal gain of the broadband LNA, including the limiter. Left: NF . Right: $|S_{21}|$.

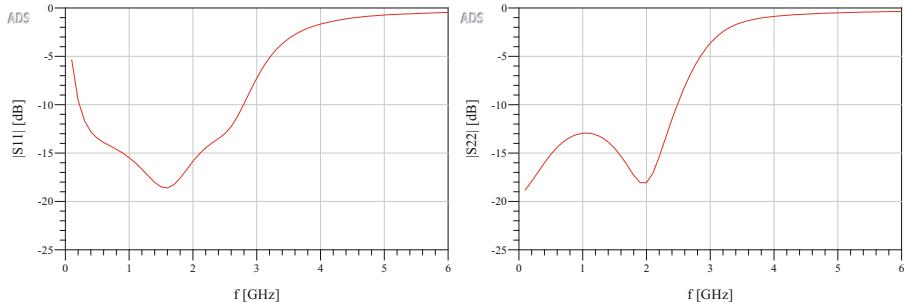


Fig. 5. Simulated matching of the broadband LNA, including the limiter. Left: $|S_{11}|$. Right: $|S_{22}|$.

Thus, to improve survivability further, it was deemed necessary to add an integrated limiter ahead of the LNA. This is based on large shunt switch transistors and a detector [18], plus additional components for matching, a DC block (in this case unavoidable), stabilization of the limiter-LNA chain. A bias voltage $V_{GG} = -4$ V, i.e., the same as for the LNA, is required. The simulated return losses of the limiter, which can be deduced from Fig. 2, are better than 16 dB at the input and 19.5 dB at the output. The insertion loss, on the other hand, is reported in Fig. 3 both at small- and large-signal. As can be seen, the worst-case insertion loss is 0.65 dB at 2 GHz in linear regime; the limiting regime starts at approximately 15 dBm (actually, this is the 1-dB compression power) and is well behaved up to at least 40 dBm.

The chain of limiter and LNA occupies an area of $3 \times 2 \text{ mm}^2$. For better versatility in the measurement phase, the two circuits can be probed separately, but alternatively

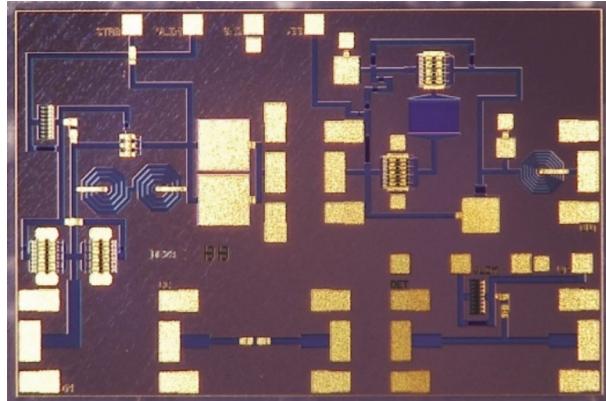


Fig. 6. Micro-photo of a realized sample. Left: limiter. Top right: LNA. Bottom: test structures.

they can be connected by means of an additional bonding wire. As shown in Fig. 4 and Fig. 5, the chain exhibits a small-signal gain of 20.2 ± 0.1 dB, input and output return losses better than 13 dB, and a noise figure better than 1.5 dB. The simulated maximum input driving level, however, is 39 dBm. The chip, photographed in Fig. 6, has been recently fabricated and is in the process of being characterized.

Table 1 summarizes the literature survey carried out at the beginning of the project and frames the results of the present work in it. Notice that for the referenced works the reported figures of merit are based on measurements, whereas for this work only simulations are available at the moment. Also, two lines are reported for the simulations of the LNA alone and those of the whole chain, respectively, when the relevant values are different.

Table 1. L-band LNA literature survey. Values relevant to this work are simulated.

Ref	BW [GHz]	G [dB]	NF [dB]	Size [mm ²]	PDC [W]	Technology	OP1dB [dBm]	ORL [dB]	IRL [dB]
1	0.2–8	20	0.8	1.7 × 1.7	6	AlGaN/GaN	32.8–33.2	12	9.1
2	0.3–3	22	1.7	1 × 1	2.2	AlGaN/GaN	NA	12	1
3	0.6–6	10	4.0	3 × 3.4	5	GaN HEMT	26	15	15
4	1–6	14	3	NA	14	GaN HEMT	NA	9.5	2.4
5	0.1–2	9	1.8	1.35 × 1.35	0.9	AlGaN/GaN	NA	7.1	8.9
6	2–4.5	17	2.9	2.25 × 2.25	0.2	AlGaN/GaN - SiC	NA	10	9.2
7	0.3–4	18	1.2	2.7 × 1.8	1	AlGaN/GaN - SiC	25	15	10
8	0.3–4	18	1.5	2.7 × 1.8	1	AlGaN/GaN	25	15	10
9	1–3	31	0.8	70 × 40	1.2	GaN HEMT	29.5	12	12
10	1.7–2.3	15	2.0	60 × 35	16	AlGaN/GaN	35	10	10
11	1.2–1.6	30	2.9	43 × 41	1	GaAs	33	18.2	10.8
12	1.7–2	17	1.07	0.325	0.562	GaAs pHEMT	27.5	10	10
This work	0.4–2	20.5	0.9	1.4 × 1.1	1.4	GaN HEMT	21	12	13.5
		20	1.5	3 × 2			20.5	13	13

3 Conclusion

In this contribution, the design of a robust L-band LNA for collecting Earth surface data in the presence of RFI, as in climatology and weather modelling applications, has been presented. Although the LNA, based on a 0.15-μm GaN HEMT technology, is expected to survive available input power levels up to 27 dBm, an input limiter has also been designed to increase that value up to almost 40 dBm. The simulated noise figure of the LNA is as low as 0.9 dB in the whole design bandwidth of 0.4–2 GHz (deteriorating to 1.5 dB in the presence of the limiter), accompanied by an exceptionally flat gain of 20.5 dB and good return losses. The power consumption is comparatively quite low for the technology, namely, 1.4 W, and the output power at 1-dB gain compression exceeds 20 dBm. Measurements on the recently fabricated dice are under way and will be published in a future contribution.

Acknowledgement. This work was funded by the European Space Agency in the framework of the project “Wideband L-band Integrated Low Noise Amplifier” (ESA ITT AO 11525).

References

1. Kobayashi, K.W., Chen, Y., Smorchkova, I., Tsai, R., Wojtowicz, M., Oki, A.: A 2 Watt, Sub-dB Noise Figure GaN MMIC LNA-PA Amplifier with Multi-octave Bandwidth from 0.2–8 GHz. In: 2007 IEEE/MTT-S International Microwave Symposium, pp. 619–622. IEEE, Honolulu, HI, USA (2007)
2. Piotrowicz, S., et al.: Broadband AlGaN/GaN high power amplifiers, robust LNAs, and power switches in L-Band. In: 2009 European Microwave Integrated Circuits Conference (EuMIC), pp. 431–434. IEEE, Rome, Italy (2009)
3. Yamaguchi, Y., Kaho, T., Kawashima, M., Shiba, H., Nakagawa, T.: A wideband GaN low noise amplifier for a frequency sensing system. In: 2014 Asia-Pacific Microwave Conference, pp. 420–422. IEEE, Sendai, Japan (2014)
4. Bassal, A.M., Jarndal, A.H.: GaN low noise amplifier design for WiMax applications. In: 2016 16th Mediterranean Microwave Symposium (MMS), pp. 1–4. IEEE, Abu Dhabi, United Arab Emirates (2016)
5. Zafar, S., Osmanoglu, S., Cankaya, B., Kashif, A., Ozbay, E.: GaN-on-SiC LNA for UHF and L-Band. In: 2019 European Microwave Conference in Central Europe (EuMCE), pp. 95–98. IEEE, Prague, Czech Republic (2019)
6. Kao, H.L., et al.: Design of an S-band 0.35 μm AlGaN/GaN LNA using cascode topology. In: 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), pp. 250–253. IEEE, Karlovy Vary, Czech Republic (2013)
7. Shih, S.-E., et al.: Design and Analysis of Ultra Wideband GaN Dual-Gate HEMT Low-Noise Amplifiers. In: IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 12, pp. 3270–3277 (2009)
8. Shih, S.E., et al.: Broadband GaN Dual-Gate HEMT Low Noise Amplifier. In: 2007 IEEE Compound Semiconductor Integrated Circuits Symposium, pp. 1–4. IEEE, Portland, OR, USA (2007)
9. Chehrenegar, P., Abbasi, M., Grahn, J., Andersson, K.: Highly linear 1–3 GHz GaN HEMT low-noise amplifier. In: 2012 IEEE/MTT-S International Microwave Symposium Digest, pp. 1–3. IEEE, Montreal, QC, Canada (2012)
10. Andrei, C., Liero, A., Lossy, R., Heinrich, W., Rudolph, M.: Highly linear broadband GaN-based low-noise amplifier. In: German Microwave Conference Digest of Papers, pp. 36–38. IEEE, Berlin, Germany (2010)
11. Bajpai, N., Pampori, A., Maity, P., Shah, M., Das, A., Chauhan, Y.S.: A Low Noise Power Amplifier MMIC to Mitigate Co-Site Interference in 5G Front End Modules. In: IEEE Access, vol. 9, pp. 124900–124909 (2021)
12. Pramod, K.B., Kumaraswamy, H.V., Praveen, K.B.: The design and simulation of radio frequency narrow band low noise amplifiers with input, output, intermediate matching. In: 2013 International Conference on Informatics, Electronics and Vision (ICIEV), pp. 1–7. IEEE, Dhaka, Bangladesh (2013).
13. Ciccognani, W., Colangeli, S., Longhi, P.E., Serino, A., Giofrè, R., Pace, L., Limiti, E.: Broadband Amplifier Design Technique by Dissipative Matching Networks. In: IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 1, pp. 148–160 (2021)
14. Colangeli, S., Bentini, A., Ciccognani, W., Limiti, E., Nanni, A.: GaN-based robust low-noise amplifiers. In: IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 10, pp. 3238–3248 (2013)
15. Limiti, E., Colangeli, S., Bentini, A., Ciccognani, W.: Robust GaN MMIC chipset for T/R module front-end integration. In: International Journal of Microwave and Optical Technology, vol. 9, no. 1, pp. 6–12 (2014)

16. Ohtomo, M.: Stability analysis and numerical simulation of multidevice amplifiers. In: IEEE Transactions on Microwave Theory and Techniques, vol. 41, no. 6, pp. 983–991 (1993)
17. Colangeli, S., Pantoli, L., Cicognani, W., Longhi, P.E., Leuzzi, G., Limiti, E.: Partitioned Ohtomo Stability Test for Efficient Analysis of Large-Signal Solutions. In: IEEE Access, vol. 12, pp. 52227–52236 (2024)
18. Provost, Z.O., Caillé, L., Camiade, M., Olivier, M., Leclerc, D., Tolant, C., Stanislawiak, M.: High Robustness S-Band GaN Based LNA. In: 14th European Microwave Integrated Circuits Conference (EuMIC), pp. 243–246. IEEE, Utrecht, The Netherlands (2019)



A Filtering Single-Ended-to-Balanced Power Divider with Enhanced Ultra-Wideband Suppression

Leidan Pan¹ , Yongle Wu¹ , Weimin Wang² , Anna Piacibello³ , and Vittorio Camarchia³

¹ School of Integrated Circuits, Beijing University of Posts and Telecommunications,
Beijing 100876, China

panleidan601@gmail.com

² School of Electronic Engineering, Beijing University of Posts and Telecommunications,
Beijing 100876, China
wangwm@bupt.edu.cn

³ Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Turin, Italy
{anna.piacibello,vittorio.camarchia}@polito.it

Abstract. In this paper, a four-parallel-coupled line is applied for the design of a novel filtering single-ended-to-balanced power divider. To facilitate the even- and odd-mode analysis of the symmetric structure, the proposed four-parallel-coupled line is split into two parallel coupled lines, and the closed-form design equations at f_0 are given. Moreover, the coupled lines and open-circuited stubs between the four-parallel-coupled line and balanced output ports can realize performances of high-selectivity filtering and enhanced ultra-wideband common-/differential-mode suppression. By regulating two impedances of the OC stubs, three prototypes with different filtering bandwidths are designed and simulated. Among them, the circuit with the high-selectivity is fabricated and measured. Measurements agree well with simulations and ideal results, which verifies the validity of the theoretical derivations and circuit feasibility.

Keywords: Common-mode · Differential-mode · enhanced ultra-wideband suppression · four-parallel-coupled line · high-selectivity filtering · power divider · single-ended-to-balanced

1 Introduction

As one of the most essential components in microwave and radio frequency (RF) systems, various kinds of power dividers (PDs) are widely used in many wireless communication circuits such as mixers, power amplifiers, multichannel communication networks, and phased array radars, etc. Therefore, the investigation of multi-functional and high-performance PDs has always been one of the top priorities in the field of microwave and RF front ends. As a typical type of PDs, the related researches on the Wilkinson-type PD [1] are very extensive. Coupled lines (CLs) are commonly used to realize the

dual frequency band, filtering function, and multi-way outputs of the Wilkinson PD [2–5]. Moreover, the multifunctional reconfigurable filtering PDs in [6] and [7] are also achieved by integrating the CL with varactor diodes.

In addition to the traditional single-ended-to-single-ended (SETSE) structures mentioned above, PDs can also be classified as balanced-to-single-ended (BTSE) PDs, balanced-to-balanced (BTB) PDs, and single-ended-to-balanced (SETB) PDs according to different types of input and output ports. Compared with the traditional SETSE devices, circuits using the topology of balanced ports are more complex to design, but they can significantly reduce the common-mode (CM) noises, inherent electromagnetic (EM) radiation interference caused by the multifrequency operating modes, and enhance the efficiency of systems as well [13]. Several SETB PD are proposed based on microstrip lines [8–10], the double-sided microstrip-to-slotline structure [11], the defected ground structure [12], CLs [13, 14], and the three-parallel-coupled line [15]. However, few researches show advantages of simple structure, outstanding filtering performance, and enhanced wideband CM/DM isolation.

In this paper, a planar filtering SETB PD with enhanced ultra-wideband CM and DM suppression utilizing the four-parallel-coupled (FPC) line is designed, which can be equivalent to a complex system composed of the Wilkinson PD, bandpass filters, and two baluns, as presented in Fig. 1. Advantages of the proposed SETB PD can be summarized as follows. 1) Planar and compact structure with the in-phase characteristic and an equal power division. 2) All five ports are well matched and the closed-form design formulas are derived. 3) High-selectivity filtering performance from SE input port to two balanced output ports. 4) Adjustable filtering bandwidth which is only related to two characteristic impedances of OC stubs. 5) Enhanced ultra-wideband isolation and suppression under the CM/DM excitations of two balanced output ports. 6) Deep and wideband mode-conversion (MC) suppression.

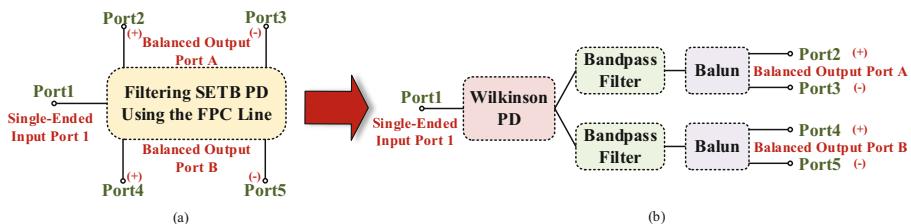


Fig. 1. (a) The proposed filtering FPC-line SETB PD and (b) its equivalent circuit systems.

2 Circuit Theory and Analysis at Center Frequency

2.1 Circuit Analytical Procedures

As depicted in Fig. 2, due to the inherent symmetrical structure of the proposed SETB PD along the horizontal direction, the method of even- and odd-mode analysis can be applied. The generalized even- and odd-mode analytical method is introduced in [16], and the two-step analytical procedure can be adopted as follows.

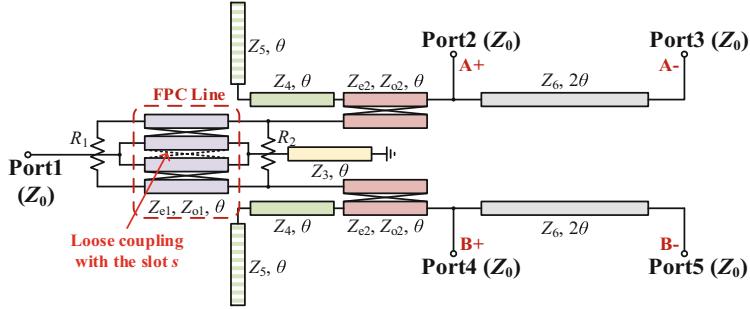


Fig. 2. Circuit schematic of the proposed filtering SETB PD using the FPC line.

Step 1. Assuming that the input P1 is well matched, then a symmetric $2n = 4$ network (P2-P5) can be obtained, which has even- and odd-mode scattering matrices expressed as

$$\begin{cases} S^o = \begin{bmatrix} S_{22}^o & S_{23}^o \\ S_{32}^o & S_{33}^o \end{bmatrix} = -\frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \\ S^e = \begin{bmatrix} S_{22}^e & S_{23}^e \\ S_{32}^e & S_{33}^e \end{bmatrix} = -\frac{1}{2} \begin{bmatrix} 1 & 1 \\ 1 & 1 \end{bmatrix} \end{cases}. \quad (1)$$

Step 2. Ensuring that the input P1 can be perfectly matched when the output ports P2-P5 are all well matched, which means

$$S_{11} = 0. \quad (2)$$

2.2 Specific Theoretical Analysis of the SETB PD Model

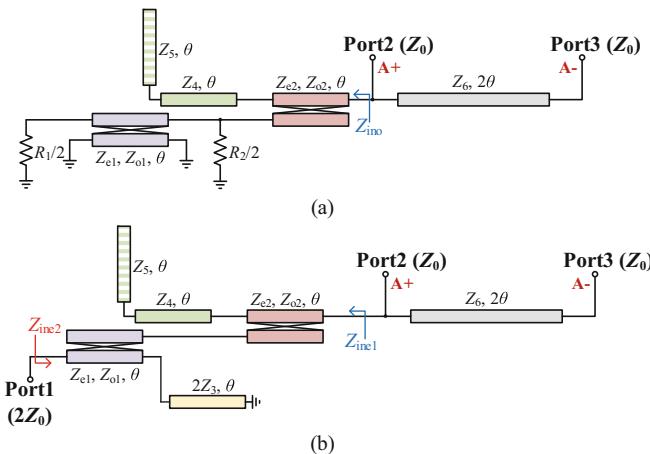


Fig. 3. Model of the split-FPC-line based SETB PD under (a) odd-mode. (b) even-mode.

The proposed filtering SETB PD configuration is composed of an FPC line, two CLs, several TL stubs, and two isolated resistors, as displayed in Fig. 2. The termination impedances of five ports are all Z_0 . Referring to the method in [17], to simplify the theory analysis, the FPC line is split into two parallel CLs temporarily due to the assumed loose coupling, and the effect of the slot s between the two parallel CLs is discussed in the subsequent section. In this section, the even-/odd-mode models of the proposed SETB PD are discussed, and their characteristic impedances of the CLs are Z_{ei}/Z_{oi} ($i = 1, 2$), respectively. The electrical length θ is assigned as 90° at f_0 .

Odd-Mode Analysis. The odd-mode circuit of the split-FPC-line based SETB PD is displayed in Fig. 3(a). According to the analysis theory of CLs in [18], the input impedance of the filtering CL can be calculated as

$$Z_{\text{ino}} = \frac{(Z_{e2} - Z_{o2})^2 [16Z_{e1}^2 Z_{o1}^2 + R_1 R_2 (Z_{e1} + Z_{o1})^2]}{32R_2 Z_{e1}^2 Z_{o1}^2}. \quad (3)$$

According to the network cascade theory and the matrix conversion relationship, the odd-mode S -parameters matrix between port 2 and port 3 can be obtained as

$$\begin{bmatrix} S_{22}^o & S_{23}^o \\ S_{32}^o & S_{33}^o \end{bmatrix} = \begin{bmatrix} \frac{Z_0}{2Z_{\text{ino}} - Z_0} & \frac{2Z_{\text{ino}}}{Z_0 - 2Z_{\text{ino}}} \\ \frac{2Z_{\text{ino}}}{Z_0 - 2Z_{\text{ino}}} & \frac{Z_0}{2Z_{\text{ino}} - Z_0} \end{bmatrix}. \quad (4)$$

Finally, by combining Eqs. (1), (3), and (4), the relationship between the CL impedances and the isolation resistors of the SETB PD should be

$$\frac{(Z_{e2} - Z_{o2})^2 [16Z_{e1}^2 Z_{o1}^2 + R_1 R_2 (Z_{e1} + Z_{o1})^2]}{16R_2 Z_{e1}^2 Z_{o1}^2} = Z_0. \quad (5)$$

Even-Mode Analysis. As shown in Fig. 3(b), the termination impedance of port 1 is $2Z_0$ under the even-mode excitation. Therefore, the analytical procedure should be divided into two parts.

Analysis when port 1 is well matched. The even-mode input impedance of the filtering CL viewed from right to left can be obtained by using the analysis theory of CLs in [18] as

$$Z_{\text{ine1}} = \frac{2Z_0(Z_{e2} - Z_{o2})^2}{(Z_{e1} - Z_{o1})^2}. \quad (6)$$

Similarly, the even-mode S -parameters matrix between port 2 to port 3 is

$$\begin{bmatrix} S_{22}^e & S_{23}^e \\ S_{32}^e & S_{33}^e \end{bmatrix} = \begin{bmatrix} \frac{Z_0}{2Z_{\text{ine1}} - Z_0} & \frac{2Z_{\text{ine1}}}{Z_0 - 2Z_{\text{ine1}}} \\ \frac{2Z_{\text{ine1}}}{Z_0 - 2Z_{\text{ine1}}} & \frac{Z_0}{2Z_{\text{ine1}} - Z_0} \end{bmatrix}. \quad (7)$$

Finally, by combining Eqs. (1), (6), and (7), the relationship between the two CL impedances should meet the condition of

$$\frac{Z_{e2} - Z_{o2}}{Z_{e1} - Z_{o1}} = \frac{1}{2}. \quad (8)$$

Analysis when port 2–5 are all well matched. It is noteworthy that port 1 is shorted under the odd-mode excitation, so the analysis of port 1 matching condition only needs to consider the even-mode excitation, namely

$$S_{11} = S_{11}^e = 0. \quad (9)$$

According to the input impedance equation of the TL, the even-mode input impedance of port 1 viewed from left to right can be obtained as

$$Z_{\text{ine}2} = \frac{Z_0(Z_{e1} - Z_{o1})^2}{2(Z_{e2} - Z_{o2})^2} = 2Z_0. \quad (10)$$

It is obvious that the value of $Z_{\text{ine}2}$ satisfies the impedance matching condition of port 1 under the even-mode excitation automatically, so the Eq. (9) is valid.

3 Circuit Design Discussion

3.1 Full-Circuit Simulation

According to the even- and odd-mode theoretical analysis at $f_0 = 3.5$ GHz in Sect. 2, as long as the parameters in the SETB PD meet limiting conditions of (5) and (8), the circuit is realizable in practical with arbitrary selected TL impedances of Z_3 , Z_4 , Z_5 , and Z_6 . Within the feasibility of the fabrication technology, parameters of the full circuit are selected and calculated as $Z_{e1} = 117 \Omega$, $Z_{o1} = 46 \Omega$, $Z_{e2} = 92 \Omega$, $Z_{o2} = 56.5 \Omega$, $R_1 = 240 \Omega$, $R_2 = 39 \Omega$, $Z_3 = 54 \Omega$, $Z_4 = 58 \Omega$, $Z_5 = 44 \Omega$, $Z_6 = 20 \Omega$, and $\theta = 90^\circ$.

Ideal results of the split-FPC-line based SETB PD are plotted in Fig. 4, which shows advantages of high-selectivity filtering function and ultra-wideband DM isolation (The subscript c, d, and s indicates the CM, DM, and the SE port, respectively). The 6-dB bandwidth of the power division from the SE port to two balanced ports $|S_{dsA1}|$ ($|S_{dsB1}|$) is 20.0%. The 15-dB bandwidths of the SE port return loss $|S_{ss11}|$ and the balanced port DM signals isolation $|S_{ddAA}|$ is 8.6% and 10.3%, respectively. Moreover, the proposed SETB PD also shows superiorities of enhanced ultra-wideband MC and CM noise suppression, as shown in Fig. 4(b).

The frequencies of transmission zeros (TZs) are shown in (11). It can be seen that impedances Z_4 and Z_5 determine the frequencies of TZ2 and TZ3, and the values of f_{z2} and f_{z3} affect the bandwidth of the circuit directly. Since impedance $Z_4 = 58 \Omega$ and $Z_5 = 44 \Omega$, the values f_{z2} and f_{z3} are calculated as 1.60 and 5.40 GHz, respectively, which are consistent with the simulations shown in Fig. 4(a).

$$f_{z1} = 0, f_{z2} = \frac{2f_0}{\pi} \arctan \sqrt{\frac{Z_5}{Z_4}}, f_{z3} = 2f_0 - \frac{2f_0}{\pi} \arctan \sqrt{\frac{Z_5}{Z_4}}, f_{z4} = 2f_0. \quad (11)$$

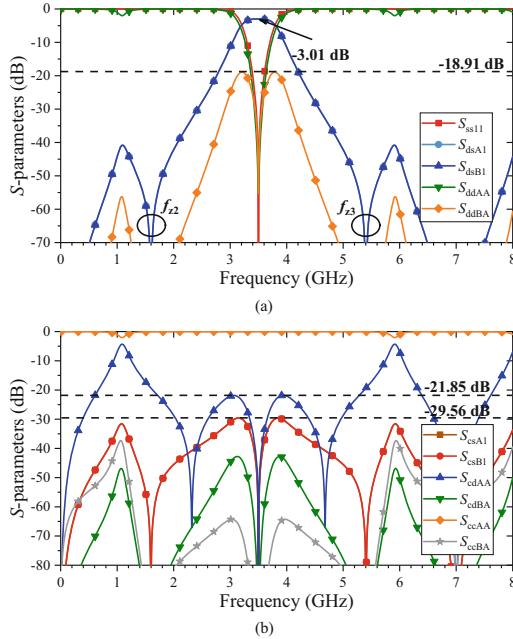


Fig. 4. Ideal results of the split-FPC-line based SETB PD.

3.2 Slot s of the FPC Line

For simplification of the previous calculations and theoretical analysis, the FPC line is split into two CLs and the coupling caused by slot s between two CLs is ignored. It is worth mentioning that the values of slots between two adjacent lines in the FPC line are all equal to s . In Fig. 5, the FPC line structure is compared with the equivalent split-FPC-line structure. It is obvious that the simulations show little differences between two cases, which also validates that a loose coupling exists between two adjacent CLs in the FPC line. Therefore, to minimize the size and simplify the structure of the circuit as much as possible, the simulation and fabrication of the SETB PD are all carried out according to the FPC line structure in the subsequent analysis and discussion.

3.3 Circuit Analysis with Different Parameters

As discussed previously, the impedances variation of the TLs has no effect to the performance of the proposed circuit at f_0 . However, the influences of their variation cannot be ignored within the whole band range.

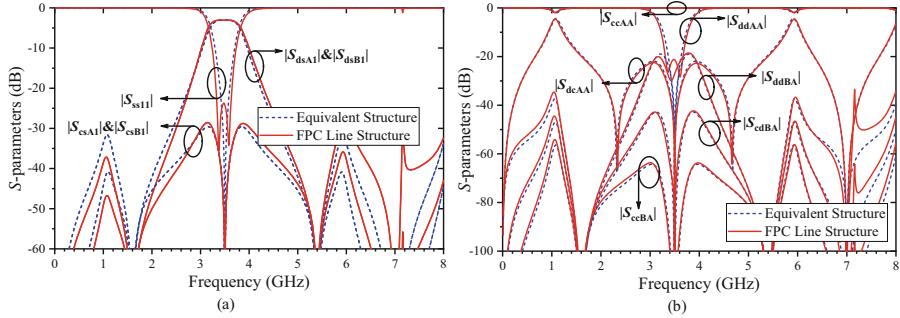


Fig. 5. Simulation comparison of the split-FPC-line structure and the FPC line structure.

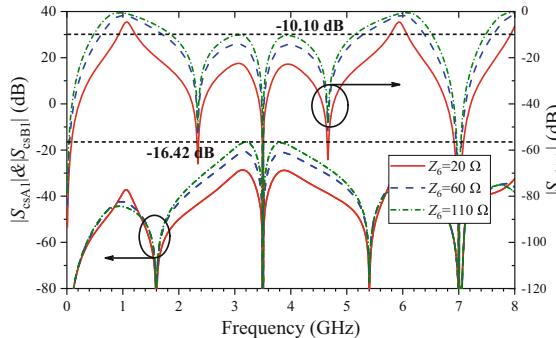


Fig. 6. Simulated S -parameters of the FPC-line based SETB PD with different value of Z_6 for $|S_{csA1}|$, $|S_{csB1}|$, and $|S_{cdAA}|$.

The simulated S -parameters of the FPC-line based SETB PD with different values of Z_6 are illustrated in Fig. 6. The varying of Z_6 has a great influence on the CM noises and MC suppression performances. As the Z_6 decreases from 110Ω to 20Ω , the MC suppression $|S_{cdAA}|$ increases from 10 dB to about 25 dB , meanwhile, the CM noise suppression $|S_{csA1}|$ ($|S_{csB1}|$) also improves from about 16 dB to 30 dB . Apparently, the circuit shows a better performance with a smaller Z_6 within the allowable value range of the fabrication. Moreover, it is also noteworthy that the loss of the SETB PD can increase undesirably with large values of isolated resistors. Therefore, R_1 and R_2 should be set as small as possible within the appropriate range.

As calculated in (11), impedances Z_4 and Z_5 determine the frequencies of TZ2 and TZ3, which affect the bandwidth of the circuit directly, as depicted in Fig. 7 with Design I to III. Circuit parameters of the three designs are listed in Table 1. The value of Z_3 should be adjusted slightly for a better performance of simulated S -parameters. The width, slot, and length of the FPC line are represented as w , s , and l , respectively. All structures are implemented on the 0.762-mm Rogers RO4350B substrate with $\epsilon_r = 3.66$ and $\tan\delta = 0.0037$.

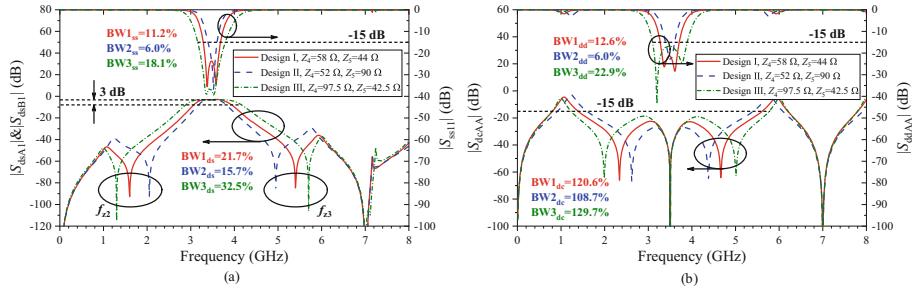


Fig. 7. Simulated S-parameters of the proposed SETB PD with different values of Z_4 and Z_5 .

Table 1. Circuit Parameters of Fig. 7

	Dimensions (mm)			Impedances and Resistors (Ω)							
	w	s	l	Z_{e2}	Z_{o2}	Z_3	Z_4	Z_5	Z_6	R_1	R_2
Design I	0.54	0.20	13.19	99.7	57.9	54	58	44	20	240	39
Design II	0.56	0.22	13.09	101.7	60.2	56	52	90			
Design III	0.48	0.16	12.93	105.7	56.4	49.9	97.5	42.5			

3.4 Design Procedure

Based on the analysis and discussion mentioned above, the complete design procedure of the proposed SETB PD using the FPC line is summarized as follows.

Step 1. Specify the operating center frequency f_0 of the SETB PD.

Step 2. Simplify the FPC line into two parallel CLs. According to (5) and (8), determine and calculate values of two isolated resistors and the even-/odd-mode impedances of CLs in the circuit.

Step 3. Following the analysis and discussion of Fig. 6, select the appropriate value of Z_6 for a better performance of the SETB PD.

Step 4. Based on the relationship in (11), determine the required bandwidth of the circuit and calculate the values of f_{z2}, f_{z3}, Z_4 , and Z_5 . Adjust the impedance Z_3 slightly according to the simulated results.

Step 5. Construct the FPC line equivalent to the two parallel CLs, keeping the width s of the slot between two adjacent lines equal.

Step 6. Choose the substrate for the prototype implementation, convert the electrical quantities into physical dimensions and optimize if necessary.

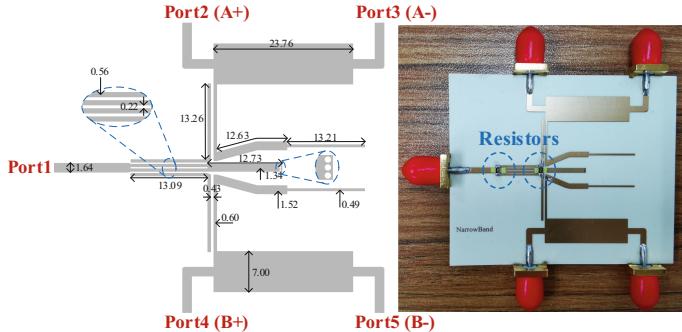


Fig. 8. Layout and photograph of the SETB PD with marked physical dimensions (unit: mm).

4 Experiments and Discussion

For a further verification, the proposed SETB PD with the high-selectivity filtering function (Design II) is implemented, measured, and demonstrated. The ideal model results and schematic simulations are all performed on Advanced Design System (ADS) software, while the measurements are accomplished on the vector network analyzer (VNA) of ROHDE&SCHWARZ ZVA67. Since the VNA is a four-port instrument while the measured SETB PDs have five ports, a $50\text{-}\Omega$ load is needed to connect with the no-load port during the measurement. The layout and photograph of the fabricated prototype is presented in Fig. 8 with marked physical dimensions. Ideal results, schematic simulations, and measurements can be seen in Fig. 9.

In Fig. 9(a), the measured DM isolation $|S_{ddAA}|$ ($|S_{ddBB}|$) has a 6.6% 10-dB bandwidth. The DM suppression level $|S_{ddAB}|$ ($|S_{ddBA}|$) is higher than 14.9 dB in the whole frequency range $0\text{--}2.3f_0$. As shown in Fig. 9(b), the measured $|S_{ccAB}|$ ($|S_{ccBA}|$) shows enhanced ultra-wideband performance of more than 30 dB suppression from 0 to 5.7 GHz ($0\text{--}1.63f_0$), and the CM noise suppression between the SE and balanced ports $|S_{csA1}|$ ($|S_{csB1}|$) has a 121.7% 20-dB bandwidth. In Fig. 9(c), the $|S_{dcAA}|$ ($|S_{dcBB}|$) shows a 112.9% 15-dB bandwidth and the $|S_{dcAB}|$ ($|S_{dcBA}|$) shows a suppression greater than 20 dB in the whole band within $0\text{--}2.3f_0$.

Finally, the comparisons between simulations and measurements of the SE port isolation, the power dividing, and the phase difference are illustrated in Fig. 9(d). The frequency deviations of $|S_{dsA1}|$ ($|S_{dsB1}|$) and the variation of $\angle(S_{dsA1}/S_{dsB1})$ at TZs can be due to the discontinuities of CLs, the different phase velocities of even- and odd-mode of CLs, the inaccuracy of fabrication, and the reasonable measurement errors. The 15-dB bandwidth of the SE port isolation $|S_{ss11}|$ is about 6.1% and the 6-dB bandwidth of $|S_{dsA1}|$ ($|S_{dsB1}|$) is about 12.9%. The filtering transition bandwidths of $|S_{dsA1}|$ ($|S_{dsB1}|$) from -6 dB to -20 dB are 0.29 and 0.21 GHz at low and high frequencies, respectively, which shows the high-selectivity performance of the SETB PD. Moreover, the $|S_{dsA1}|$ ($|S_{dsB1}|$) is -4.26 dB (-4.56 dB) at f_0 and the minimum power loss is 1.36 dB at 3.49 GHz. The in-band fluctuation of the phase difference $\angle(S_{dsA1}/S_{dsB1})$ is $0^\circ \pm 2^\circ$.

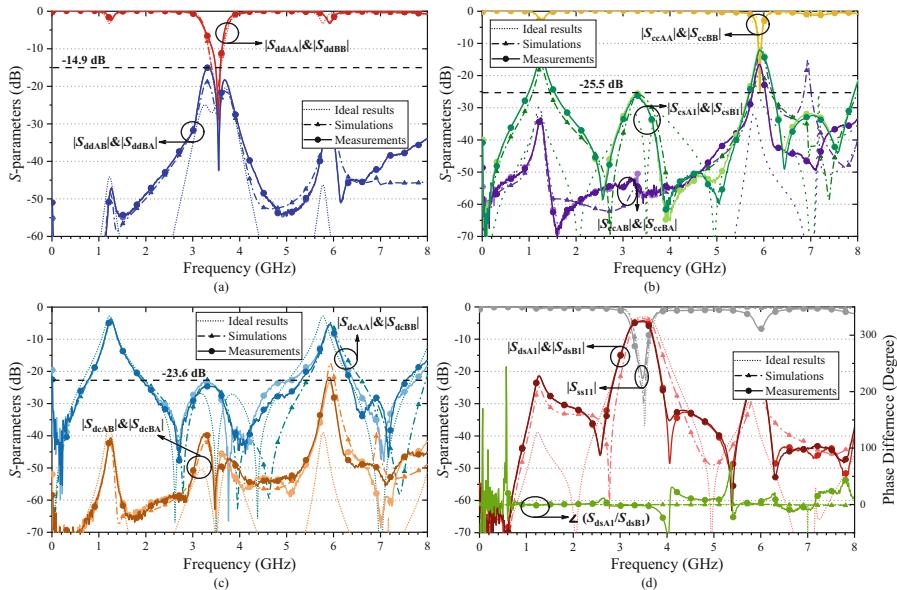


Fig. 9. Ideal results, simulations, and measurements of the SETB PD.

5 Conclusion

In this paper, a high-selectivity filtering SETB PD with enhanced ultra-wideband CM/DM isolation and suppression using the FPC line has been proposed. The closed-form equations, theory analysis, and complete design procedure have also been provided. By adjusting two impedances of the OC stubs, three designs with different bandwidths have been simulated. Moreover, ideal results, schematic simulations, and measurements of the prototype with the high-selectivity filtering function have been given and discussed thoroughly. The enhanced efficiency and the capability of reducing CM noises and the EM interference allow the proposed structure to be widely used in feeding arrays, high-selectivity microwave/RF systems, and multichannel communication networks.

References

1. Gómez-García, R., et al.: Single/Multi-band Wilkinson-type power dividers with embedded transversal filtering sections and application to channelized filters. *IEEE Trans. Circuits Syst. I, Reg. Papers.* **62**(6), 1518–1527 (2015)
2. Wu, Y., Liu, Y., Xue, Q.: An analytical approach for a novel coupled-line dual-band Wilkinson power divider. *IEEE Trans. Microw. Theory Techn.* **59**(2), 286–294 (2011)
3. Sajadi, A., Sheikhi, A., Abdipour, A.: Analysis, simulation, and implementation of dual-band filtering power divider based on terminated coupled lines. *IEEE Trans. Circuit Syst. II, Exp. Briefs.* **67**(11), 2487–2491 (2020)
4. Zhao, X., Song, K., Zhu, Y., Fan, Y.: Wideband four-way filtering power divider with isolation performance using three parallel-coupled lines. *IEEE Microw. Wireless Compon. Lett.* **27**(9), 800–802 (2017)

5. Yu, X., Sun, S.: A novel wideband filtering power divider with embedding three-line coupled structures. *IEEE Access* **6**, 41280–41290 (2018)
6. Zhang, G., Liu, S., Chen, W., Zhang, Z., Yang, J.: Design method for compact multifunctional reconfigurable filtering power divider on a new tunable three-port multi-mode topology. *IEEE Trans. Circuits Syst. I, Reg. Papers.* **67**(12), 4580–4592 (2020)
7. Xu, J.-X., Huang, M., Zhan, W.-L., Zhang, X.Y.: Reconfigurable filtering power divider with arbitrary operating channels based on external quality factor control. *IEEE Trans. Circuits Syst. I, Reg. Papers.* **69**(11), 4395–4403 (2022)
8. Yu, Y., Sun, L.: A design of single-ended to differential-ended power divider for X band application. *Microw. Opt. Technol. Lett.* **57**(11), 2669–2673 (2015)
9. Feng, W., et al.: Single-ended-to-balanced filtering power dividers with wideband common-mode suppression. *IEEE Trans. Microw. Theory Techn.* **66**(12), 5531–5542 (2018)
10. Wu, Y., Zhuang, Z., Kong, M., Jiao, L., Liu, Y., Kishk, A.A.: Wideband filtering unbalanced-to-balanced independent impedance-transforming power divider with arbitrary power ratio. *IEEE Trans. Microw. Theory Techn.* **66**(10), 4482–4496 (2018)
11. Zhu, H., Qin, P.-Y., Guo, Y.J.: Single-ended-to-balanced power divider with extended common-mode suppression and its application to differential 2×4 butler matrices. *IEEE Trans. Microw. Theory Techn.* **68**(4), 1510–1519 (2020)
12. Zhu, Y., et al.: Wideband single-ended-to-balanced power divider with intrinsic common-mode suppression. *IEEE Microw. Wireless Compon. Lett.* **30**(4), 379–382 (2020)
13. Muralidharan, S., et al.: A compact low loss single-ended to two-way differential power divider/combiner. *IEEE Microw. Wireless Compon. Lett.* **25**(2), 103–105 (2015)
14. Zhang, W., et al.: Novel planar compact coupled-line single-ended-to-balanced power divider. *IEEE Trans. Microw. Theory Techn.* **65**(8), 2953–2963 (2017)
15. Li, S., Tang, W., Wang, J., Wang, X., Yang, J.: A new dual-band single-ended-to-balanced filtering power divider. *Int. J. RF Microw. Comput. Aided Eng.* **30**(6) (2020)
16. Roberg, M., Campbell, C.: A novel even & odd-mode symmetric circuit decomposition method. In: Proc. IEEE Compound Semicond. Integr. Circuit Symp. (CSICS), Monterey, CA, USA, pp. 1–4 (2013)
17. Pan, L., Wu, Y., Wang, W., Zheng, Y., Liu, Y.: A symmetrical broadband tight-coupled directional coupler with high directivity using three-folded-coupled lines. *IEEE Trans. Circuit Syst. II, Exp. Briefs.* **69**(9), 3744–3748 (2022)
18. Zhang, B., Wu, Y., Liu, Y.: Wideband single-ended and differential bandpass filters based on terminated coupled line structures. *IEEE Trans. Microw. Theory Techn.* **65**(3), 761–774 (2017)



Challenges of 9-dB Back-Off Doherty Power Amplifiers with 20% Fractional Bandwidth

Zhifan Zhang^(✉), Anna Piacibello, and Vittorio Camarchia

Department of Electronics and Telecommunications, Politecnico di Torino,
Turin, Italy

{zhifan.zhang,anna.piacibello,vittorio.camarchia}@polito.it

Abstract. This paper addresses the critical weakness of the conventional Doherty Power Amplifier when targeting wideband and deep back-off operation. A load modulation network with a good trade-off between complexity and performance enhancement is proposed for broadband operation around 9-dB back-off. As an initial assessment, its effectiveness in enhancing the performance in broadband operation has been proven using linear simulations.

Keywords: Deep back-off · Doherty power amplifier · sub-6 GHz

1 Introduction

With the rapid growth of wireless communication systems, a sharp rise in data traffic poses significant challenges on implementation of radio frequency (RF) power amplifiers (PAs) in wireless transmitters. Among these, the efficiency versus linearity trade-off has become key to the development of the technologies as well as the architectures, especially due to the increasingly high Peak-to-Average Power Ratio (PAPR) and wide instantaneous bandwidth of the adopted modulations [1–4]. Furthermore, in some applications the thermal aspects [5–7] often severely constrain the achievable performance.

The Doherty Power Amplifier (DPA) has become a trendy option in 5G scenario due to its flexible circuit structure, reliable performance and most important property of providing high efficiency at significant output power back-off (OBO) level [8–12] compared to non-load modulated PAs such as class-AB [13–15] and harmonically tuned [16–19] PAs.

However, the conventional DPA struggles to fully meet the requirement outlined in 5G scenario due to its bandwidth limitations and 6-dB OBO efficiency enhancement. This work studies some of the possible topologies of the load modulation network (LMN) for a 9-dB DPA targeting relatively broadband ($\approx 20\%$) operation below 6 GHz.

2 Definition of the Simulation Setup

In this preliminary study, a set of linear simulations based on the assumed optimum load at the drain current generator plane of the DPA configuration was used to initially estimate the achievable bandwidth of conventional and proposed LMN. As Fig. 1(a) shows, the output of the Main and Auxiliary amplifiers are initially modelled as ideal current generators synchronously controlled by the respective input voltages.

In a 9-dB OBO DPA configuration, the Auxiliary generator is initially off, until the Main amplifier current I_M reaches $\gamma I_{M,\max}$, where $I_{M,\max}$ is the maximum Main drain current and $\gamma = 1/3$. This refers to a 9.6-dB input back-off power level, which is typically compatible with an OBO level around 9 dB due to the unavoidable gain compression at saturation in GaN PAs. Moreover, under the assumption that both devices operate at the same drain voltage supply, the ratio of the Auxiliary and Main active peripheries scales like the ratio of the maximum drain currents: $\beta = I_A/I_M = 2$.

The drain current profiles I_M and I_A of the Main and Auxiliary amplifiers are expressed by (1), (2) [20] and plotted in Fig. 1(b).

$$I_M = x I_{M,\max}, \quad \text{for } 0 \leq x \leq 1. \quad (1)$$

$$I_A = \begin{cases} 0 & \text{for } 0 \leq x < \gamma \\ I_{M,\max} \cdot \beta \cdot \frac{x-\gamma}{1-\gamma}, & \text{for } \gamma \leq x \leq 1. \end{cases} \quad (2)$$

$$\text{where } x = \frac{v_{\text{in}}}{v_{\text{in},\max}} = \sqrt{\frac{P_{\text{in}}}{P_{\text{in},\max}}}. \quad (3)$$

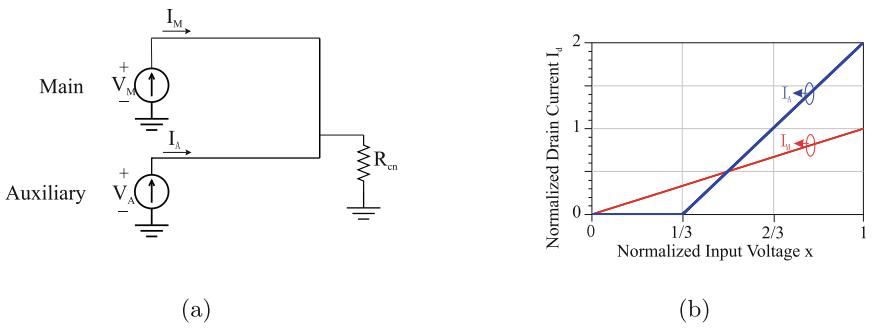


Fig. 1. (a) DPA configuration and (b) drain current profiles of the Main and Auxiliary amplifier in 9-dB OBO DPAs.

3 Preliminary Study of LMN in a GaN 9-dB OBO DPA

Considering the parameters of a typical GaN technology [21] suited for application up to X band, i.e., $V_{DD} = 28$ V and a power density of 4 W/mm, for a design aimed at delivering around 75 W of saturated power, the resulting optimum loads are $R_{opt,M} = 16\Omega$ and $R_{opt,A} = 8\Omega$ assuming the same supply voltage is adopted for both. The LMN is required to present $3R_{opt,M}$ to the Main amplifier at the 9-dB OBO power level, $R_{opt,M}$ and $R_{opt,A}$ to the current plane of the Main and the Auxiliary ones at saturation.

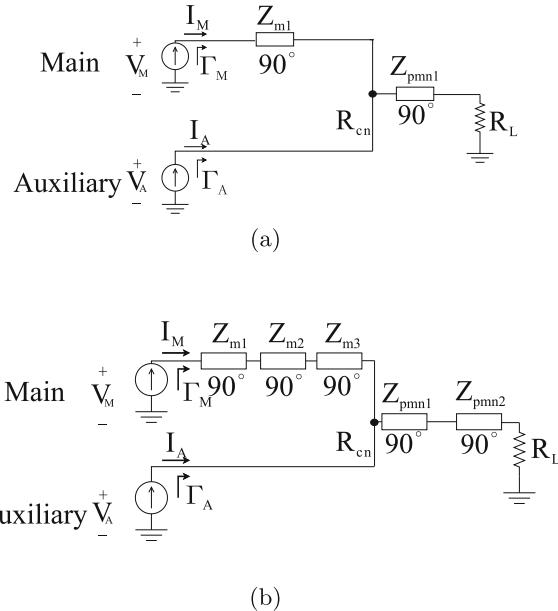


Fig. 2. Block diagrams of (a) conventional and (b) proposed DPA.

A conventional DPA architecture, made of two quarter-wavelength transmission lines (QWTs) with characteristic impedance Z_{m1} and Z_{pmn1} acting as inverter and post-matching, is shown in Fig. 2(a). Typically, the single QWT tends to narrow the bandwidth over which the optimal load modulation occurs. Thus, an alternative broadband LMN, shown in Fig. 2(b), is proposed to improve the DPA performance. The common node is connected through a three-section QWT-constructed impedance inverter to the Main, and a two-section QWT PMN is adopted to match the common node load R_{cn} to 50Ω . This topology has additional degrees of freedom, which allows optimizing the loads at OBO and at saturation with different trade-offs.

3.1 Static Transistor Model

Assuming that the parasitic effects of the devices are negligible, or can be ideally cancelled over the target band, the ideal current generators can fully model the devices' outputs to initially evaluate the effectiveness of the modified LMN.

The conventional and proposed LMNs are implemented with the circuit parameters provided in Table 1, and the corresponding results are illustrated in Fig. 3. The circuit parameters for the conventional combiner can either be obtained analytically by solving the equations reported in (4) at center frequency, or optimized numerically to trade-off the matching condition at OBO and saturation, thus allowing to cover a wider bandwidth.

It is worth mentioning that the resulting characteristic impedances are rather low in all cases, but are especially critical for the proposed LMN. This may hinder its implementation in some specific technology, and in any case calls for careful layout planning and electromagnetic simulation of the passive networks as well as the transition between them and the terminals of the transistors. In case the resulting impedance levels were too low, the options are either to constrain them by accepting a worse bandwidth matching trade-off or to consider lumped implementation of the QWTs. These considerations are however difficult to treat in a general analysis due to the high number of variants.

Table 1. Circuit parameters for the combiners of Fig. 2

Circuit		Z_{m1}	Z_{m2}	Z_{m3}	Z_{pmn1}	Z_{pmn2}	Unit
Figure 2(a)	analytical	16	—	—	16	—	Ω
	optimized	23	—	—	20	—	Ω
Figure 2(b)	optimized	27	9	6	12	34	Ω

$$R_{\text{opt,M}} = \frac{{Z_{m1}}^2}{R_{\text{cn}}} ; R_{\text{cn}} = \frac{{Z_{pmn1}}^2}{R_L}. \quad (4)$$

Figure 3(a) compares the performance that can be obtained by the conventional LMN, in terms of load synthesized at the current generator planes and corresponding efficiency. The dashed lines refer to the analytical solution exact at f_0 , whereas the solid lines to the numerically optimized one.

In both cases, the load modulation line at f_0 is well located at the real axis in the Smith chart with the synthesized loads at OBO and saturation, reaching the optimum value. Conversely, at frequencies that deviate from f_0 , ranging from 0.9 f_0 to 1.1 f_0 , the load modulation trajectories are symmetrically distributed across the inductive and capacitive region along the centered real axis. The Auxiliary load at saturation and the Main load at OBO remain approximately close to the optimum impedance, despite the load at saturation of the Main

deviates significantly from the optimal load target as the frequency shifts from f_0 .

At the critical power level, the Auxiliary load maintains a relatively stable matching over a 20% fractional bandwidth, while the Main load at OBO remains below -10 dB across a 15% bandwidth but deteriorates when it comes to a 20% one. Even if the loading condition at saturation is less constant and remains below -10 dB only in a 10% fractional bandwidth, the efficiency in this ideal case can be still optimized to remain over 60% at both OBO and saturation over a 20% fractional bandwidth. In this first evaluation the bandwidth is estimated by an approximate method that does not account for voltage clipping.

Figure 3(b) illustrates how the proposed LMN is capable to synthesize the net-like load modulation curves, offering the potential to achieve a trade-off for optimal matching at either OBO or saturation of the Main over the bandwidth. The simulation results demonstrate that the proposed LMN achieves a trade-off for improved matching at Main saturation across the bandwidth, while maintaining good matching for other loading condition with a margin over a 20% fractional bandwidth. Consequently, it shows a 75% saturation efficiency over the band, meanwhile still maintaining over 60% OBO efficiency. Compared to conventional LMNs, this topology improves the overall performance and offers greater flexibility in achieving design objectives. This enables the DPA to operate efficiently in the 9-dB OBO and saturation regions.

3.2 Effect of Transistors' Parasitics

In practice, parasitic effects are hardly ever completely negligible in current applications and should therefore be taken into consideration.

Since the proposed analysis should hold for a typical GaN/SiC technology, the parasitic parameters of the Main and Auxiliary amplifiers are assumed to be modelled by a shunt-C and series-L network with values per unit gate width of 0.35 pF/mm and 3 pH/mm, respectively, which are assumed to scale linearly with the device periphery W .

For a design focusing on achieving 75 W saturated power, the scaled parasitic capacitance are estimated as $C_{\text{out},M} = 2$ pF, $L_{\text{out},M} = 15$ pH and $C_{\text{out},A} = 4$ pF, $L_{\text{out},A} = 30$ pH [22]. In this case, a simple L-section network cascaded at the output of the Main and Auxiliary amplifiers, as presented in Fig. 4, is introduced to compensate for the parasitic effects over target band [23].

Consequently, the conventional and proposed LMNs topologies incorporate an additional compensation network illustrated in Fig. 4 to synthesize the desired load modulation across the bandwidth. The characteristic impedance of each transmission line is re-optimized numerically together with the circuit parameters of the parasitic compensation networks, to achieve the best matching conditions for both Main and Auxiliary simultaneously over a 20% fractional bandwidth. The resulting circuit parameters are summarized in Table 2 and in Table 3.

The performance of the modified LMNs are depicted in Fig. 5. For the re-optimized conventional LMN, the Main matching condition at saturation improved to -15 dB across a 15% fractional bandwidth. However, it degrades

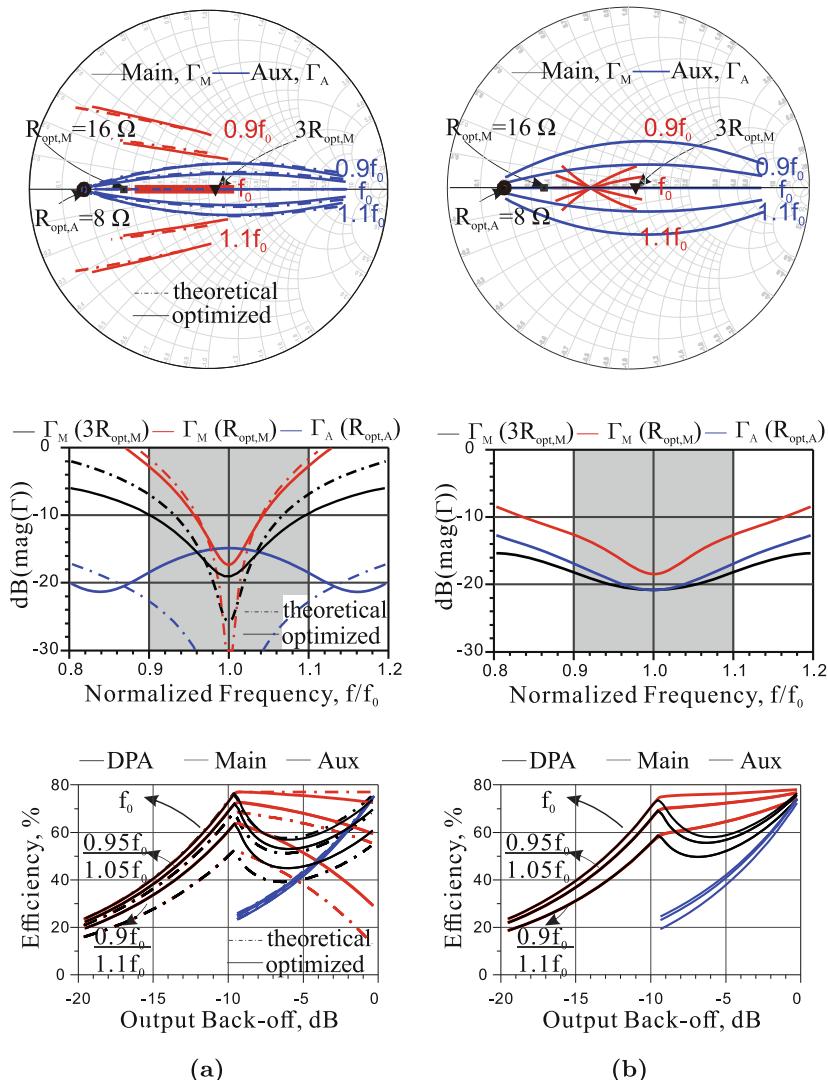


Fig. 3. Performance of the combiners of Fig. 2(a) and Fig. 2(b), in terms of synthesized loads and corresponding efficiency.

Table 2. Circuit parameters for the parasitic compensation networks of Fig. 4

Circuit	Z, θ_{cM0}	Z, θ_{cM1}	Z, θ_{cA0}	Z, θ_{cA1}	Unit
Figure 4(a)	58, 8	48, 18	5, 1	82, 6	$\Omega, {}^\circ$
Figure 4(b)	79, 1	90, 13	20, 1	90, 7	$\Omega, {}^\circ$

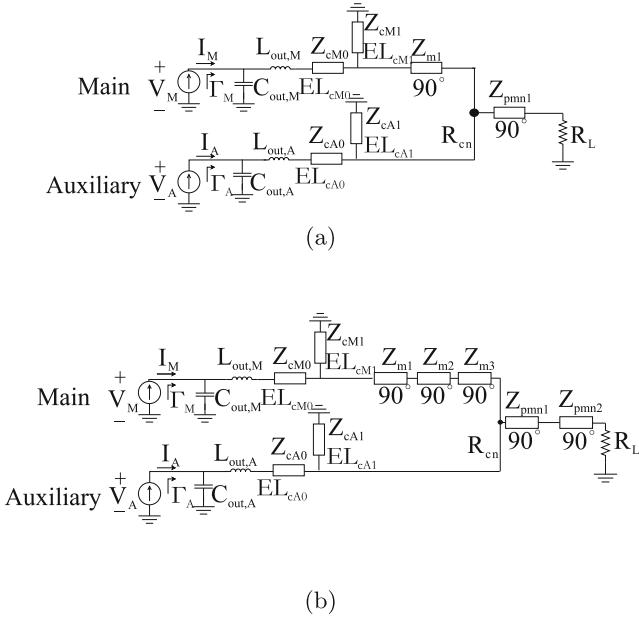


Fig. 4. Block diagrams of (a) conventional and (b) proposed DPA incorporating with a L-section compensator.

Table 3. Circuit parameters for the combiners of Fig. 4

Circuit	Z_{m1}	Z_{m2}	Z_{m3}	Z_{pmn1}	Z_{pmn2}	Unit
Figure 4(a)	19	—	—	24	—	Ω
Figure 4(b)	31	13	6	10	35	Ω

the matching condition of Main at OBO and Auxiliary at saturation respectively. As a result, the saturation efficiency deteriorates over band.

Conversely, the proposed LMN after optimization is able to maintain -15 dB matching referring to all the desired load across a 20% fractional bandwidth. Moreover, the matching at the center frequency improved towards -30 dB with the assistance of the compensation network. As a consequence, it leads to the performance enhancement over band. Overall, the performance considering the impact of parasitic effects closely aligns with the ideal case, demonstrating the effectiveness of the proposed LMN.

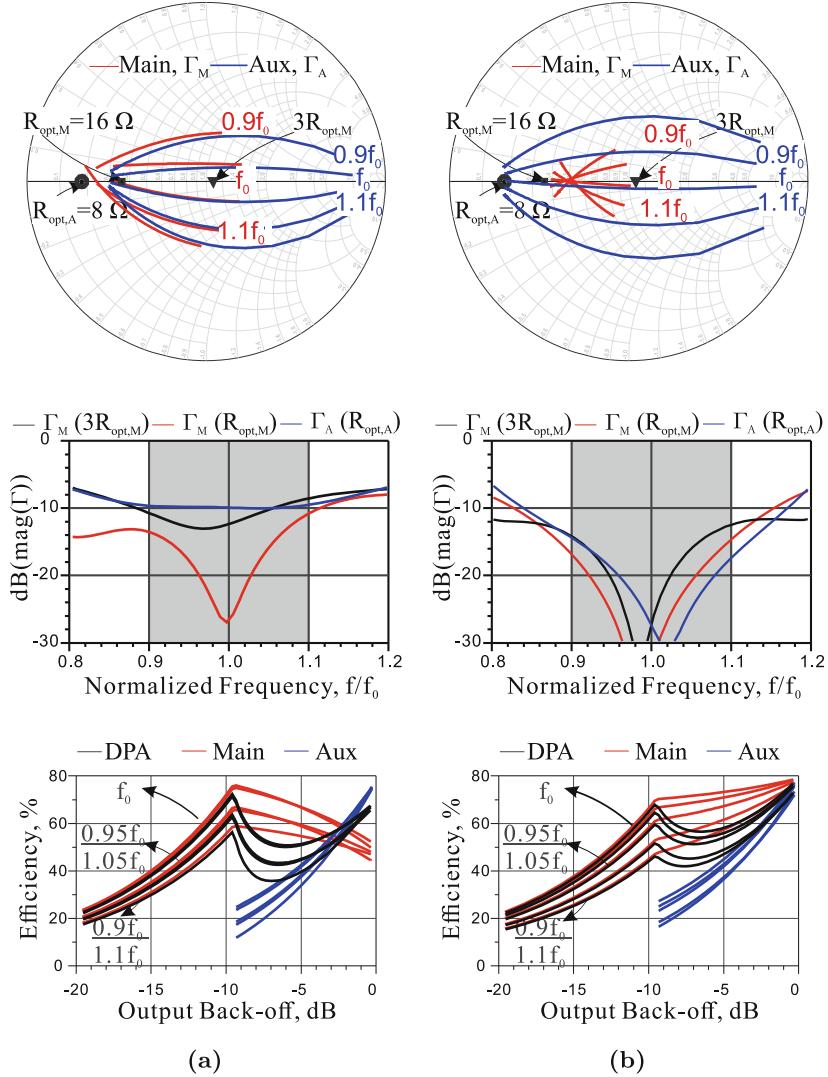


Fig. 5. Performance of the combiners of Fig. 4(a) and Fig. 4(b), in terms of synthesized load and corresponding efficiency.

4 Conclusion

This paper has discussed some of the challenges existing in the implementation of wideband DPAs for deep OBO operation, such as the presence of transistor parasitic effects to be compensated (which strongly depends on technology) and the feasibility of the QWT dimensions, and has proposed a load modulation network to enhance the bandwidth of a Doherty PA for 9-dB OBO. In fact, the

targeted loads lead to rather low values for $Z_{m2,3}$, which pose a challenge for the DPA layout. Consequently, a MMIC implementation is impractical due to the wide transmission lines required, not prone to bending and fitting a compact layout. Conversely, a PCB implementation of the combiner which avoids bends is feasible. If packaged transistors are adopted, the achievable bandwidth has to be reconsidered including the parasitic effects caused by the packaging. A promising alternative for sub-6-GHz operation is a PCB-based design using bare dies, which only needs to embed the effect of short bondwires in the combiner QWTs.

References

1. Piacibello, A., et al.: High-gain and high-linearity MMIC GaN Doherty power amplifier with 3-GHz bandwidth for Ka-band satellite communications. *IEEE Microw. Wirel. Technol. Lett.* **34**(6), 765–768 (2024)
2. Giofrè, R., et al.: A design approach to maximize the efficiency vs. linearity trade-off in fixed and modulated load GaN power amplifiers. *IEEE Access* **6**, 9247–9255 (2018)
3. Zhao, S., et al.: Linearity improved Doherty power amplifier using non-foster circuits. *IEEE Access* **7**, 40109–40113 (2019)
4. Sharma Nitesh, R., et al.: A 700 MHz to 2.5 GHz cascode GaAs power amplifier for multi-band pico-cell achieving 20 dB Gain, 40 dBm to 45 dBm OIP3 and 66% peak PAE. *IEEE Access* **6**, 818–829 (2018)
5. Wang, Y., Naylor, R.: Challenges in designing 5 GHz 802.11ac WiFi power amplifiers. In: 2014 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications, Newport Beach, CA, USA, pp. 16–18 (2014)
6. Ramella, C., et al.: Thermal-aware GaN/Si MMIC design for space applications. In: 2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), Tel-Aviv, Israel, pp. 1–6 (2019)
7. Costanzo, F., et al.: A derating-rules compliant Ka-band GaN-on-Si power amplifier designed for highly reliable satellite applications. In: 2021 16th European Microwave Integrated Circuits Conference. London, United Kingdom, pp. 253–256 (2022)
8. Nikandish, G., et al.: Breaking the bandwidth limit: a review of broadband Doherty power amplifier design for 5G. *IEEE Microw. Mag.* **21**(4), 57–75 (2020)
9. Fang, X.-H., et al.: Modified Doherty amplifier with extended bandwidth and back-off power range using optimized peak combining current ratio. *IEEE Trans. Microw. Theory Techn.* **66**(12), 5347–5357 (2018)
10. Chen, S., et al.: A bandwidth enhanced Doherty power amplifier with a compact output combiner. *IEEE Microw. Wirel. Compon. Lett.* **26**(6), 434–436 (2016)
11. Piacibello, A., et al.: 3-way Doherty power amplifiers: design guidelines and MMIC implementation at 28 GHz. *IEEE Trans. Microw. Theory Tech.* **71**(5), 2016–2028 (2022)
12. Pitt, A., et al.: A broadband asymmetrical Doherty power amplifier with optimized continuous mode harmonic impedances. *IEEE J. Microw.* **3**(4), 1120–1133 (2023)
13. Iqbal, M., Piacibello, A.: A 5 W class-AB power amplifier based on a GaN HEMT for LTE communication band. In: 2016 16th Mediterranean Microwave Symposium (MMS), Abu Dhabi, United Arab Emirates, pp. 1–4 (2016)

14. Alqadami, A.S.M., et al.: A 5 W high efficiency class AB power amplifier for LTE base station application. In: 2017 28th Irish Signals and Systems Conference, Killarney, Ireland, pp. 1–5 (2017)
15. Gadallah, A., et al.: A high efficiency 3–7 GHz class AB CMOS power amplifier for WBAN applications. In: 2015 IEEE International Symposium on Radio-Frequency Integration Technology, Sendai, Japan, pp. 163–165 (2015)
16. Piacibello, A., Zhang, Z., Camarchia, V.: Continuous inverse class-F GaN power amplifier with 70% efficiency over 1.4–2 GHz bandwidth. In: 2023 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications, Las Vegas, NV, USA, pp. 10–12 (2023)
17. Duan, Y.-W., et al.: Low-voltage continuous class-F wideband power amplifier. *IEEE Microw. Wirel. Technol. Lett.* **34**(6), 639–642 (2024)
18. Sharma, T., et al.: Generalized continuous class-F harmonic tuned power amplifiers. *IEEE Microw. Wirel. Compon. Lett.* **26**(3), 213–215 (2016)
19. Chu, C., et al.: High-efficiency class-iF-1 power amplifier with enhanced linearity. *IEEE Trans. Microw. Theory Tech.* **71**(5), 1977–1989 (2023)
20. Ghione, G., Pirola, M.: *Microwave Electronics*. Cambridge University Press, 2018 Forum (2002)
21. Camarchia, V., et al.: Fabrication and nonlinear characterization of GaN HEMTs on SiC and sapphire for high-power applications. *Int. J. RF Microwave Comput.-Aided Eng.* **16**, 70–80 (2006)
22. Stillmaker, A., et al.: Scaling equations for the accurate prediction of CMOS device performance from 180 nm to 7 nm. *IEEE Trans. Microw. Theory Tech.* **58**, 74–81 (2017)
23. Rubio, J.M., et al.: Design of an 87% fractional bandwidth Doherty power amplifier supported by a simplified bandwidth estimation method. *IEEE Trans. Microw. Theory Tech.* **66**(3), 1319–1327 (2018)



Low-Cost Calibrated Microwave Radiometers for Solar Observation: From Education to Science

Giacomo Schiavolini¹, Giulio Brancalì¹, Ethan Bernardini¹, Giulia Orecchini¹,
Valentina Palazzi¹, Camille C. A. Westerhof², Timo S. Prinz²,
Martin Hübner², Sebastian Lange², Maurizio Burla²,
and Federico Alimenti¹(✉)

¹ Dipartimento d'Ingegneria, Università degli Studi di Perugia, via G. Duranti 93,
06125 Perugia, Italy

federico.alimenti@unipg.it

² Technische Universität Berlin, Fachgebiet Hochfrequenztechnik-Photonik
Einsteinufer 25, 10587 Berlin, Germany

burla@tu-berlin.de

Abstract. Low-cost microwave radiometers can be built using a low-noise downconverter for satellite TV reception and a software-defined radio. Errors due to system gain and noise temperature drift can be corrected using motorized black body and noise injection. Successful solar observations have been made with such a radiometer mounted on a 75 cm offset parabolic dish. A joint educational project between the University of Perugia and the Technical University of Berlin is launched on this topic to give students the opportunity to practice with microwave systems, antennas, electronics and data processing.

Keywords: Microwave radiometers · electronic noise · solar observation

1 Introduction

The observation of the Sun in the microwave and mm-wave bands is a very active research field because, at these frequencies, it is possible to investigate complex physical mechanisms that characterize our star. Since the use of large radio telescopes is not always possible (the Sun is a very intense source), and the working time of these instruments is distributed among different experiments, researchers have decided to equip themselves with smaller instruments specifically designed for solar observations. In particular 2.5-m radio telescopes working up to 100 GHz have recently been proposed [9].

In this context, it would be desirable to complement the scientific data with solar brightness temperature measurements obtained with full-disk radiometers, i.e. instruments without imaging capability [21]. A network of these radiometers, distributed around the world, is needed to provide a time-on-target measurement

24 h a day, 365 days a year. Consequently, the ideal instrument should be simple and inexpensive so that it can be easily replicated. The apparatus should be equipped with a calibration circuit and, possibly, with two channels at different frequencies to determine the spectral index. The design and the first experimental validation of a radiometer with these features is described in the present study.

This paper introduces the basics of radio astronomy, microwave radiometry and related electronics, as well as the use of software defined radios as instrument backend units, which is quite novel. Indeed, in the last decade, SDRs have been integrated with microwave radiometers to improve reconfigurability [15] and miniaturization, which are important issues in small satellites [6], Cubesats [14] and unmanned aircraft systems [5].

To demonstrate the feasibility of the idea, one of the less expensive SDR devices available on the market (i.e., an 8-bit SDR belonging to the RTL family) is chosen as a case study and experimentally characterized. This SDR has a software programmable gain between 20 and 50 dB, a noise figure of 7.5 dB at 1 GHz and a dynamic range of about 40 dB. The radio can be tuned between 64 and 1766 MHz with a signal bandwidth up to 3.2 MHz, performances that allow its use as an intermediate frequency receiver in radiometric applications.

2 The Students Project

A joint educational project between the University of Perugia and the Technical University of Berlin is launched to give students the opportunity to engage in the hands-on task of building an amateur radio telescope. The educational goal is to learn the basics of microwave radiometry, microwave electronics, antennas, the nature of emission and motion of astronomical objects, and to solve mechanical problems such as antenna construction, mounting and tracking. Many amateur radio astronomical projects have been proposed, and their descriptions are available in great detail in a number of books or web sites. However, not many of the described approaches offer the possibility to obtain calibrated measurement data. Instead, the ambition of this specific project is to realize a calibrated instrument, i.e. able to measure the brightness temperature of the observed celestial bodies, mainly the Sun and the Moon.

The present paper is written for the benefit of readers who want to start similar activities and, especially, is dedicated to the students involved in the project.

3 Theory

Celestial bodies such as the Sun, the Moon and radio sources emit electromagnetic radiation. These hot objects radiate like black bodies, and produce a white-noise spectrum at microwave and millimeter-wave frequencies. The Sun and the Moon, in particular, are quite strong radio astronomical sources, so they can be easily detected even with small radio telescopes. Purpose of this section is to

recall the theoretical basis that allows, under some simplifying assumptions, to predict the noise level picked up by the radio telescope antenna.

3.1 Antenna Noise Temperature

The antenna noise temperature is the physical quantity measured by microwave radiometers. Such a temperature depends on the scene observed by the antenna and can be evaluated according to [7, p. 144] as:

$$T_A = \frac{A_e}{\lambda^2} \iint P_n(\rho, \varphi) T_B^{obs}(\rho, \varphi) d\Omega \quad (1)$$

where λ is the signal wavelength, A_e is the effective area of the antenna, P_n is the normalized (power) radiation pattern, and T_B^{obs} is the brightness temperature of the observed radio source. The variables ρ and φ are used to describe the spatial variations of the above functions. In the case of a celestial body such as the Sun or Moon, it is particularly convenient to define ρ as the angular coordinate along the radius of the celestial body, and φ as the angular coordinate around the axis between the antenna and the celestial body. In the case of the Sun, this spherical coordinate system is shown in Fig. 1.

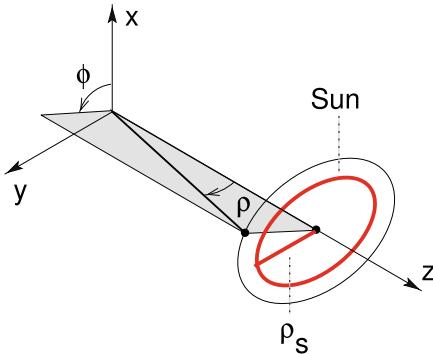


Fig. 1. Spherical coordinate system used to define the brightness temperature distribution over the solar disk (or a celestial body). The antenna is pointed at the center of the Sun. The solar radius ρ_s is equal to about 16 arcmin. The solid angle of the Sun Ω_s is defined as the cone of angular aperture ρ_s .

The antenna soild angle Ω_A is defined as:

$$\Omega_A = \iint P_n(\rho, \varphi) d\Omega \quad (2)$$

with the elementary solid angle $d\Omega$ given (in spherical coordinates) by:

$$d\Omega = \sin \rho d\rho d\varphi \simeq \rho d\rho d\varphi \quad (3)$$

The small-angle approximation is well verified for all celestial bodies since $\rho \leq \rho_S \ll 1$ (for the Sun $\rho_S \simeq 16$ arcmin which is 4.65×10^{-3} radians). It is worth noting here that the antenna theorem relates the antenna solid angle, the effective area and the wavelength squared, [10], [7, p. 144]:

$$\frac{A_e}{\lambda^2} = \frac{1}{\Omega_A} \quad (4)$$

Finally it is observed that, for most practical cases (dish antennas), Ω_A can be related to the half-power beamwidth (HPBW) $2\rho_H$ as follows:

$$\Omega_A = \kappa \pi \rho_H^2 \quad (5)$$

κ being a constant of the antenna. Note that the HPBW is twice ρ_H .

From now on we will limit our discussion to the Sun, but the same formulation applies without modification to all celestial bodies. In order to evaluate the above integral in Eq. (1), some assumptions are necessary. First, the brightness temperature of the Sun is assumed to be uniform over the solar disk:

$$T_B^{sun}(\rho, \varphi) = \begin{cases} T_S & 0 \leq \rho \leq \rho_S \\ 0 & \text{elsewhere} \end{cases} \quad (6)$$

where T_S is the average brightness temperature of the Sun. Second, since the measurements are made from Earth, both the atmospheric transmittance (τ_a) and the radio temperature of the sky (T_{sky}) must be taken into account to model the observed object:

$$T_B^{obs}(\rho, \varphi) = \tau_a T_B^{sun}(\rho, \varphi) + T_{sky} \quad (7)$$

At this point it is interesting to note that if the half-power beamwidth of the antenna is greater than the diameter of the Sun, the Sun can be assimilated to a point-like source (assuming the antenna is pointed at the center of the Sun), while the sky is an extended source. This is the case for inexpensive microwave radiometers with small antennas. Furthermore, we observe that τ_a and T_{sky} depend on the antenna elevation above ground, although this is not explicitly stated in (7). Inserting (7), (6) into (1) and using (4) one gets:

$$T_A = \frac{\tau_a}{\Omega_A} \iint_{\Omega_s} P_n(\rho, \varphi) T_B^{sun}(\rho, \varphi) d\Omega + T_{sky} \underbrace{\frac{1}{\Omega_A} \iint d\Omega}_1 \quad (8)$$

An estimate of the antenna noise temperature can thus be obtained by evaluating the first integral over the solid angle of the Sun Ω_s :

$$T_A \simeq \frac{\tau_a}{\Omega_A} \int_0^{2\pi} d\varphi \int_0^{\rho_S} T_S \underbrace{P_n(\rho, \varphi)}_{\approx 1} \rho d\rho + T_{sky} \quad (9)$$

where $P_n(\rho, \varphi) \simeq 1$ since this study assumes an antenna with $\Omega_A \gg \Omega_s$. As previously said we are considering small antennas whose beam is much larger than the solar radius (full disk radiometers). Performing the above calculations:

$$T_A \simeq \tau_a \frac{\pi \rho_S^2}{\Omega_A} T_S + T_{sky} = \frac{\tau_a}{\kappa} \frac{\rho_S^2}{\rho_H^2} T_S + T_{sky} \quad (10)$$

where (5) is finally used to express Ω_A in terms of the half-power beamwidth. In the above relationship the term ρ_S^2/ρ_H^2 is known as the filling factor and justifies the dilution of T_S across the antenna beam.

The previous formulation assumes an ideal antenna with unit efficiency, i.e. with $\eta_A = 1$. Substituting η_A in (10), we get the effective antenna noise temperature T'_A , i.e. the quantity that is measured by the microwave radiometer:

$$T'_A = \eta_A T_A + (1 - \eta_A) T_{amb} \quad (11)$$

In this equation, T_{amb} is the ambient temperature. The last term represents the thermal noise generation associated with the antenna ohmic losses. The final result is obtained by combining (10) and (11):

$$T'_A \simeq \eta_A \frac{\tau_a}{\kappa} \frac{\rho_S^2}{\rho_H^2} T_S + \underbrace{T_{sky} + (1 - \eta_A) T_{amb}}_{T'_{sky}} \quad (12)$$

with T'_{sky} being the apparent sky temperature. In the following of the paper it will be shown that the apparent temperature can be easily determined from measurements, and that it can be used to estimate the antenna efficiency.

3.2 Gaussian Antennas

Aperture antennas used in radio astronomy can often be approximated as Gaussian beam focusing elements. Using such an approximation it is possible to estimate the antenna solid angle and thus the parameter κ . According to [7, p. 136] the normalized radiation pattern of a gaussian beam focusing element is:

$$P_n(\rho) = \exp \left(-2 \frac{\rho^2}{\rho_0^2} \right) \quad (13)$$

where ρ_0 is the far-field divergence angle and the Gaussian beam radiation pattern, being axially symmetric, is a function of the angle ρ only. Evaluation of Ω_A with (2) gives:

$$\Omega_A = \pi \frac{\rho_0^2}{2} \quad (14)$$

The relationship between ρ_0 and ρ_H (half-power angle) is obtained from (13):

$$\rho_0 = \sqrt{\frac{2}{\ln 2}} \rho_H \quad (15)$$

and, as a result, we can express Ω_A in terms of ρ_H :

$$\Omega_A = \pi \underbrace{\frac{1}{\ln 2}}_{\kappa} \rho_H^2 \quad (16)$$

In conclusion, comparing (5) with (16) we have found that, for a Gaussian beam, $\kappa = 1/\ln 2 \simeq 1.443$.

3.3 Brightness Temperature of the Quiet Sun

The brightness temperature of the quiet Sun averaged over the whole solar disk has been studied by many radio astronomers in the last decades, [12, 21]. In particular the following empirical relationship (based on more than three decades of observations) is reported in [12]:

$$\log(T_S) = a + b \log(f_0) \quad (17)$$

where \log is the base 10 logarithm, f_0 is the observation frequency in Hz, and the constants $a = 6.43$ and $b = -0.236$ represent the 1-Hz temperature extrapolation and the spectral index respectively. The above linear fit (in log scale) is valid in the range 10–100 GHz. In our case the observation frequency is 12.6 GHz and a quiet Sun brightness temperature $T_S \simeq 11000$ K is calculated.

4 Material and Methods

As seen in the previous section, the microwave noise emitted from the Sun is captured by the radio telescope and produces a certain noisy signal at the antenna output. Such a noise can be accounted for assigning the effective noise temperature T'_A to the radiation resistance of the antenna, and is measured by a microwave radiometer. As a consequence, from the radiometer's point of view, the antenna appears as a matched resistor that emitting thermal noise at an equivalent physical temperature T'_A . A total power radiometer consists of a microwave receiver followed by a true rms power detector. Since the input noise level is very low, a significant amount of gain should be provided by the receiver to make the output signal compatible with the power detector range. Assuming a perfect power matching between the antenna and the receiver, the available noise power N_o at the detector input (or at the front-end output) is given by:

$$N_o = k_B (T'_A + T_{rx}) B_{rx} G_{rx} \quad (18)$$

where G_{rx} , T_{rx} , and B_{rx} are the available receiver power gain, equivalent noise temperature, and bandwidth, respectively, and $k_B = 1.38^{-23}$ J/K is the Boltzmann constant. In a superheterodyne architecture, B_{rx} is determined by the IF filter. The inverse (18) is the basic (total power) radiometer equation:

$$T'_A = \underbrace{\frac{1}{k_B B_{rx} G_{rx}}}_{\alpha} N_o - \underbrace{T_{rx}}_{\beta} = \alpha N_o - \beta \quad (19)$$

Such an equation states that there is a linear relationship between the measured output noise power N_o and the antenna noise temperature T'_A . The radiometer scale factor α and the offset β should ideally be constants determined by some a priori calibration. In practice, this is not true because receiver gain and noise temperature can change significantly as a function of the physical temperature of the receiver electronics. The drifts of α and β are the main source of systematic errors, and to correct them a periodic calibration of the radiometer is necessary. In general, since two instrument parameters are unknown, two independent measurements are required. This is usually done by pointing the antenna toward two black bodies of known physical temperatures $T_{bb}^{(1)}$, $T_{bb}^{(2)}$ and using (19) to set a linear system of equations:

$$\begin{cases} N_o^{(1)} \alpha - \beta = T_{bb}^{(1)} \\ N_o^{(2)} \alpha - \beta = T_{bb}^{(2)} \end{cases} \quad (20)$$

which can be solved for α and β . This approach requires some instrument engineering (e.g., a movable black body), which will be discussed below, along with other calibration methods (noise injection).

Another methodological aspect to consider is that N_o results from the measurement of a noisy signal. This leads to the fluctuation of its value and thus to the fluctuation of the estimate of T'_A . The standard deviation of such a quantity is known as the radiometer resolution ΔT and represents the minimum temperature variation that can be measured by the instrument. Hersman and Poe [8] demonstrated the following relationship for a total power radiometer:

$$\Delta T = (T'_A + T_{rx}) \sqrt{\frac{1}{\tau B_{rx}} + \left(\frac{\Delta G}{G_{rx}}\right)^2} \quad (21)$$

where τ is the integration time, while the $\Delta G/G_{rx}$ term accounts for the total receiver gain drift and fluctuations that occur during the integration time. A low standard deviation ΔT thus implies maximizing the τB_{rx} product and minimizing the $\Delta G/G_{rx}$ gain fluctuations.

Figure 2 shows the microwave radiometer architecture considered in this study. The system is based on satellite TV low noise frontend [16]. An input signal in the 11.6–12.70 GHz band is converted to an IF signal between 0.95 and 2.05 GHz. These devices have a typical gain of 54 dB with a noise figure of less than 0.8 dB. Two polarizations and different input frequency bands can be selected electronically in the more advanced units. The average price of these devices is about \$20, so low-cost instruments are feasible.

The basic configuration uses an analog backend. This consists of an IF amplifier, a ceramic bandpass filter, a Schottky diode square-law power detector, an integrator, and a video amplifier. The signal is acquired by a 10-bit ADC and sent to a computer. A more advanced configuration uses a software defined radio (SDR) to perform IF amplification, bandwidth selection, and power detection. The latter is achieved by processing the sampled In-phase and Quadrature (I/Q) signal components in real time.

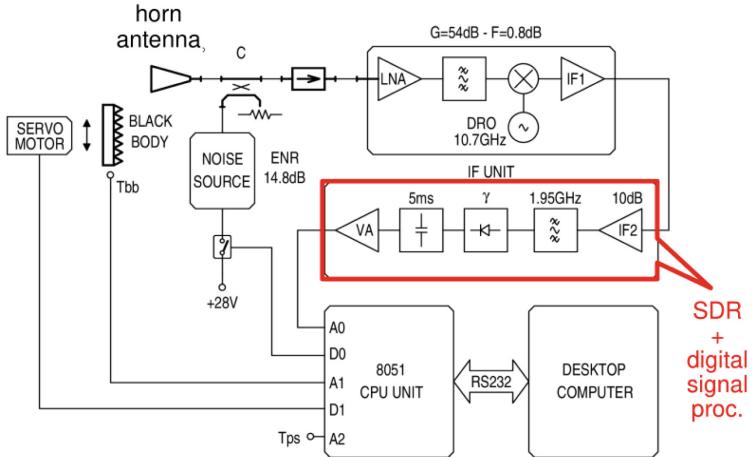


Fig. 2. Block diagram of the low-cost microwave radiometer used in the solar experiments. The classical architecture is based on analog IF amplification, detection and integration stages to process the received signal (analog backend). A software defined radio can replace the IF unit with several advantages (SDR backend).

In this paper, the SDR radiometer is proposed as the main solution. This approach is in fact quite new and offers several advantages, as described in the rest of the paper. From this point of view, we want to show that an SDR can be used to measure microwave noise with good accuracy. However, the radiometer with analog backend is a mature instrument, so it will be adopted to make a first Sun observation and to validate the model summarized by Eq. (12).

4.1 Radiometer with SDR Backend

In the previous section it has been described a novel microwave radiometer concept based on a low-noise downconverter for satellite TV reception and a software-defined radio. The latter works as an IF stage, performing amplification, filtering and power detection functions [17].

The SDR approach has many advantages. First, it simplifies the design of the instrument, since it is based on high-level components already available on the market. Second, the IF frequency can be tuned digitally within the output bandwidth of the downconverter (0.95 to 2.05 GHz), which is very important for eliminating interference from TV satellites. Finally, two channels can be processed simultaneously, allowing the spectral index to be determined. Such a parameter is of great interest to radio astronomers.

This study is based on the SDR shown in Fig. 3 (top panel). Although high-performance SDRs are now available on the market (see, for example, the Adalm Pluto family from Analog Devices), our interest is in the performance that can be achieved with low-cost devices. In particular, we focused on RTL-SDR using the Rafael R820T RF tuner and the Realtek RTL2832U demodulator [19]. The RF

interface consists of a reconfigurable integrated superheterodyne architecture. The front-end can be programmed to acquire signals between 64 and 1766 MHz with a maximum gain of 50 dB that can be set by software. A Low-Noise Amplifier (LNA) is used as the first stage and this ensures a typical noise figure of 3.5 dB at 500 MHz. The input reflection coefficient S_{11} is about -10 dB at 1000 MHz in a 50Ω environment. The received signal is then filtered and frequency shifted before sampling and acquisition. Two 8-bit Analog-to-Digital Converters (ADCs) are used for this purpose, giving a dynamic range (with fixed RF gain) of about 40 dB. Due to the complex sampling (in-phase and quadrature signal components) it is possible to acquire the signal bandwidth up to the sampling rate. This can go up to 3.2 Mb/s and is software controlled. The ADCs and all the devices required for digital signal processing and communication via the USB interface are integrated in the Realtek RTL2832U chip.

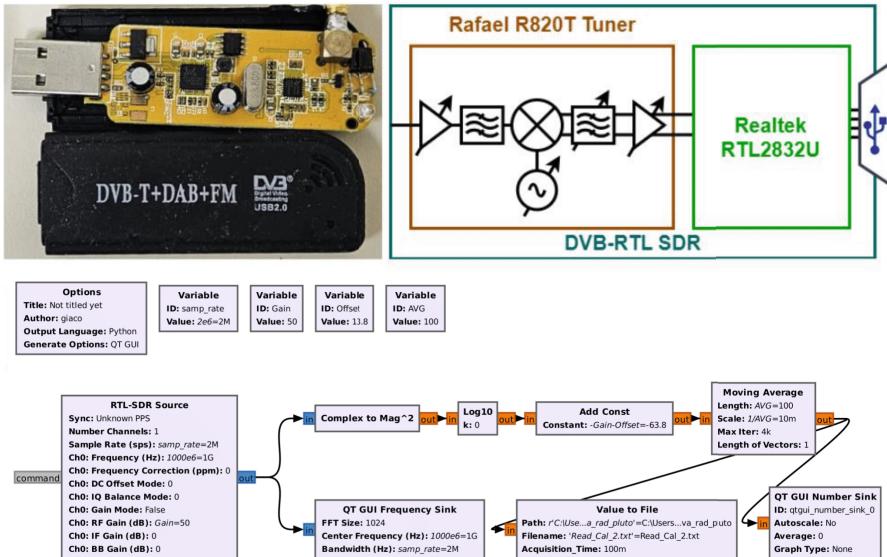


Fig. 3. RTL-SDR that can be used as radiometer backend. Hardware (top left), block diagram (top right) and GNURadio software (bottom).

To configure the radio and extract the desired data, a diagram-based GNU-Radio script was implemented. In this program, as a first step, we configure the SDR with the RTL-SDR source block. Then, the instantaneous power $p(\ell)$ at the SDR output is evaluated, in the discrete time domain, as the square magnitude of the complex signal. Using the in-phase $i(\ell)$ and quadrature $q(\ell)$ signal components:

$$p(\ell) = i^2(\ell) + q^2(\ell) \quad (22)$$

where ℓ is the discrete time, so the continuous time is given by $t = \ell \Delta t$ with sampling period Δt . Such a value is finally integrated over time, as required by

the processing of microwave radiometer data:

$$\bar{p}(\ell) = \frac{1}{L_\tau} \sum_{\ell=1}^{L_\tau-1} p(\ell) \quad (23)$$

In this expression the integration time τ is given by $\tau = L_\tau \Delta t$.

To use the SDR in microwave noise measurements it is important to relate the power P_o at the SDR output with the input power P_i . This can be done with the following model:

$$P_o = G_{sdr} (P_i + k_B F_{sdr} T_0 B_{sdr}) \quad (24)$$

where G_{sdr} is the total SDR gain (which can be set by software), F_{sdr} is the SDR noise figure, and $T_0 = 290$ K is the IEEE standard temperature for noise¹. Observe that the SDR bandwidth B_{sdr} determines the bandwidth of the whole system (low-noise downconverter + SDR) since it is the narrow one. As a result we can assume $B_{rx} = B_{sdr}$ in Eq. (18).

4.2 Radiometer with Analog Backend

A breadboard of the microwave radiometer with analog backend is depicted in Fig. 4 (left panel). Although a complete account of such an instrument can be found in [2] and [18], a brief description of the adopted electronic circuits is also given here for the reader's convenience.

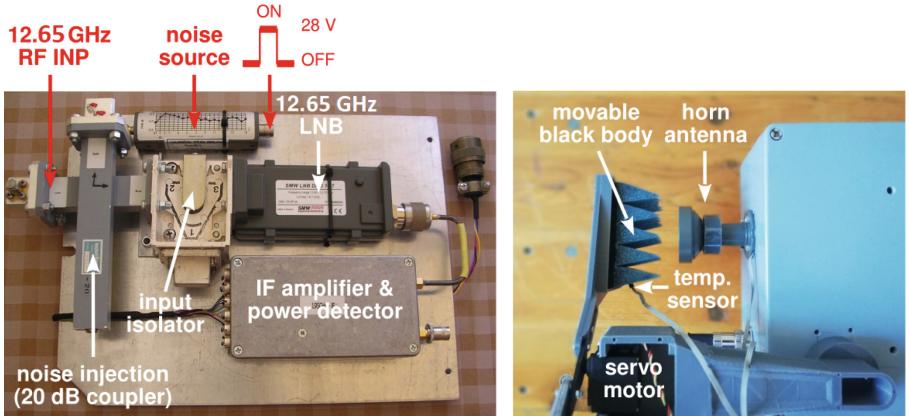


Fig. 4. Breadboard of the 12.65 GHz radiometer equipped with the analog backend.

A downconverter from Swedish Microwave was used to implement a superheterodyne receiver. The downconverter is characterized by a 0.8 dB noise figure,

¹ G_{sdr} and F_{sdr} are frequency dependent, so they should be determined (with an appropriate calibration procedure) at the frequency at which the SDR is tuned.

a 54 dB RF gain, and a gain drift with temperature of less than 0.1 dB/K. The local oscillator is an integrated 10.7 GHz dielectric resonator oscillator (DRO) with -75 dBc/Hz phase noise at 1 kHz offset from the carrier and excellent stability over temperature. Thus, an input RF signal between 11.65 GHz and 12.75 GHz is downconverted to an output IF signal between 0.95 GHz and 2.05 GHz. The image frequencies (8.65 GHz to 9.75 GHz) are rejected by more than 50 dB by a bandpass filter integrated into the downconverter. The LNB input port is a standard WR75 rectangular waveguide.

The analog IF chain is a custom design to match the characteristics of the downconverter. It consists of an input bias tee to power the downconverter, a fixed 10 dB attenuator to set a 50Ω input impedance of the IF chain, a two-stage monolithic amplifier to provide IF gain, a digital attenuator to fine tune the system gain, and a 1.95 GHz ceramic bandpass filter to define the radiometer IF bandwidth. The filter bandwidth is 100 MHz. All of these components are integrated on a single PCB fabricated by an industrial process on 0.8 mm FR4 material. The entire IF circuit has a total gain of about 10 dB. Since the center IF frequency is 1.95 GHz, the radiometer operating frequency is set to 12.65 GHz.

The square-law power detector (true rms detector) operates at 1.95 GHz and is integrated on the same board as the IF. It is implemented with a zero bias Schottky diode (HSMS2850) together with a narrow band LC impedance matching. The obtained detector sensitivity is about $7.2\text{ mV}/\mu\text{W}$. A 5 ms analog integrator consists of a simple passive RC filter connected to the square-law detector output. Video amplification is done with an instrumentation amplifier whose voltage gain is factory trimmed to 100.

The radiometer is fully calibrated to compensate for both gain and system noise temperature drifts. This is achieved using a movable black body and noise injection circuitry. The movable black body (see right panel of Fig. 4) is used to correct for receiver noise temperature drifts, i.e. to determine the radiometric offset β . It consists of a piece of pyramidal microwave absorbing material. A servo motor periodically moves the black body in front of the horn antenna to close the horn aperture. Meanwhile, a temperature sensor measures the physical temperature of the black body. Instead, the noise injection circuit uses the MT7600 laboratory noise source from Maury Microwaves and a -20 dB Moreno coupler in the WR75 waveguide (see left panel of Fig. 4). When the bias input of the MT7600 is set to 28 V, a known amount of noise power is generated by this device and injected into the receiver input through the directional coupler. Recently, integrated avalanche noise diodes have been proposed that allow an extreme miniaturization of such a circuit [3].

With these calibration mechanisms, two equations similar to (20) can be set, and as a result, α and β can be determined. The receiver gain is updated every 3 s (noise injection), while the receiver noise temperature is corrected every 30 min. It is important to note that since there is a strong dependence of the radiometric gain on the internal physical temperature of the instrument, estimation and compensation techniques can be successfully implemented as proposed in [4].

5 Results

A proof of concept for the low-cost microwave radiometer is presented in this section. The experimental discussion is divided into two parts: first, the RTL-SDR radio is validated as a digital instrument backend. Then, the radio telescope is pointed at the Sun, the antenna noise temperature is measured, and the results are compared with the developed theory.

5.1 RTL-SDR Characterization

Since the use of the SDR as a digital backend of the microwave radiometers is quite novel, it is necessary to demonstrate the feasibility of such an approach. For this purpose, two different experiments are designed as shown in Fig. 5. In the first experiment, the RTL-SDR is connected to an RF signal generator (Rohde & Schwarz SMB100B up to 30 GHz) and the radio is tested with continuous wave (CW) signals. In the second experiment, a laboratory noise source (Keysight 346C-K01) is used instead to characterize the radio against noisy signals.

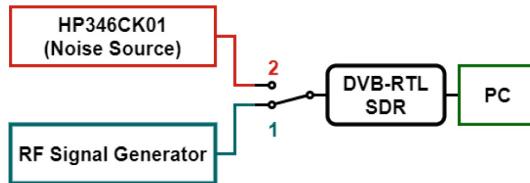


Fig. 5. Experimental setup adopted to characterize the RTL-SDR.

The CW setup is used to characterize the RTL-SDR as a function of the gain settings that are software-programmed into the device. To do this, the RF generator applies a specific carrier to the input. The available power level of the R&S SMB100B can range from -120 to 20 dBm and is therefore suitable for checking both the sensitivity and the saturation limits of the device under consideration. The I/Q signals produced by the RTL-SDR under these conditions are sampled, transferred to the PC and used to evaluate the output power with the Eqs. (22), (23). At $f_0 = 1$ GHz, the values obtained are shown in Fig. 6 (upper panel) and clearly show that as the gain is increased, the operating range of the radio moves towards lower power levels. The dynamic range (distance between saturation and noise limits) is about 40 dB and, as mentioned before, is determined by the number of ADC bits (8 in our case). With this experiment it is also possible to determine the true gain G_{sdr} of the radio as a function of the gain settings. Using such a true gain, the input power can be retrieved from the measured output power, as shown in Fig. 6 (bottom panel). From this figure, it is clear that within the dynamic range, and almost ideal behavior is obtained.

The noise figure F_{sdr} is the second parameter used to model the RTL-SDR according to (24). The noise setup of Fig. 5 is used to experimentally determine

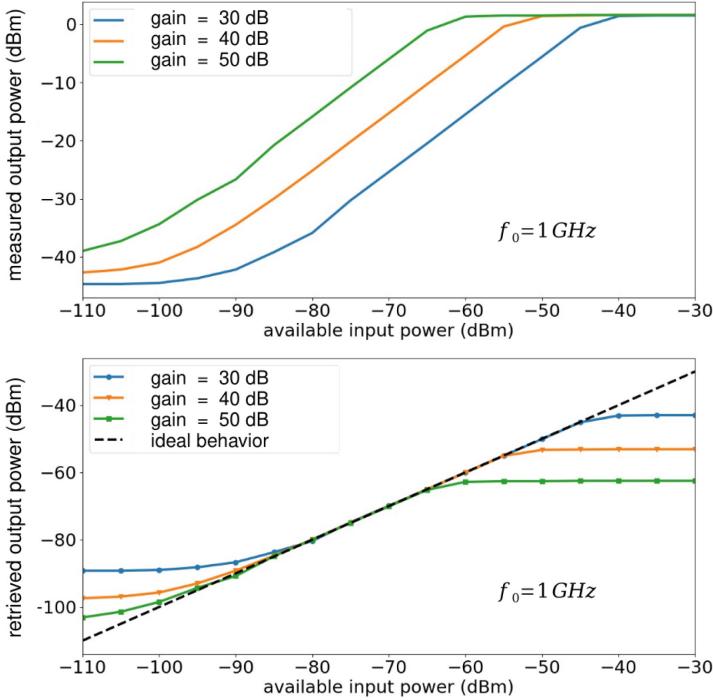


Fig. 6. Results of the RTL-SDR continuous-wave (CW) experiments. Measured output power (top) and retrieved input power (bottom) for different gain settings. This characterization is carried out at 1 GHz.

F_{sdr} . For this purpose, the Y-factor method is applied [1] and the results are shown in Fig. 7 (upper panel) as a function of the gain settings when the receiver is tuned at 1 GHz. The noise figure obtained follows the typical behavior of a receiver with variable LNA gain. When the gain of the first stage of the RF chain is increased, a general decrease in the noise figure is observed. On the other hand (see Fig. 6) the radio saturates at lower power levels. The RTL-SDR parameters determined with the above experiments are summarized in Table 1.

In a final experiment, the RTL-SDR input is connected to a matched load at ambient temperature and the input equivalent noise temperature is retrieved from the measured output power and using the previously estimated device parameters (i.e., G_{sdr} and F_{sdr}). It is seen that the radio can detect its own noise and that the fluctuations of the retrieved noise temperature (standard deviation) can be reduced by increasing the integration time τ . In a more rigorous way, the Allan deviation of the input noise temperature fluctuations are evaluated together with the corresponding confidence intervals [20]. In fact, through the correct interpretation of the Allan deviation result, a large amount of information directly related to the acquisition system performance can be extracted [11].

Table 1. RTL-SDR parameters

gain settings (dB)	G_{sdr} (dB)	F_{sdr} (dB)
30	44.3	22.3
35	49.4	18.4
40	54.4	13.1
45	58.8	10.8
50	63.6	7.0

$$f_0 = 1 \text{ GHz}, B_{sdr} = 2 \text{ MHz}$$

From the analysis performed on the RTL SDR, shown in Fig. 7, it can be seen that the acquisition starts to drift after about 100 s.

5.2 Sun Experiments

Successful Sun observations were made on October 27, 2023 with the radiometer of Fig. 4. As mentioned above, the instrument operates at 12.65 GHz and has a radiometric resolution of 1-K when observing a black body at ambient temperature. The instrument is equipped with a 70 cm off-axis parabolic antenna for satellite TV applications and is mounted on a stable base. In these experiments, the antenna is pointed in a fixed direction in the sky and the Sun passes through the beam due to the Earth's rotation. The pointing direction (azimuth and elevation angles) was predicted using astronomical software according to the radio telescope's location and the time of day.

To use the antenna temperature model summarized by Eq. (12) four parameters must be known, namely: the antenna half-power angular radius ρ_H , the antenna efficiency η_A , the atmospheric transmissivity τ_a , and the apparent sky temperature T'_{sky} . The latter can be easily determined as the measured antenna noise temperature when the Sun is completely outside the antenna beam. In our experiments we measure a value around 47 K, as shown in the figure.

The true sky temperature and the atmospheric transmissivity are a function of the elevation angle (30° in our case), the sky conditions (clear sky during the experiments), and other parameters such as temperature, pressure, and relative humidity at ground level. Very accurate remote sensing models are nowadays available to predict these parameters [13]. The October 27, 2023 was a rather hot afternoon and the external radiometer temperature sensor measured about 30 C ($T_{amb} = 303$ K). Pressure and humidity were taken from those reported by the Perugia weather station. As a result a true sky temperature $T_{sky} = 12.7$ K and an atmospheric transmissivity $\tau_a = 0.96$ were estimated. Now, reversing the relationship between true and apparent sky temperature, the antenna efficiency is obtained:

$$\eta_A = 1 - \frac{T'_{sky} - T_{sky}}{T_{amb}} \quad (25)$$

As a result we get $\eta_A \simeq 0.89$, a quite interesting value.

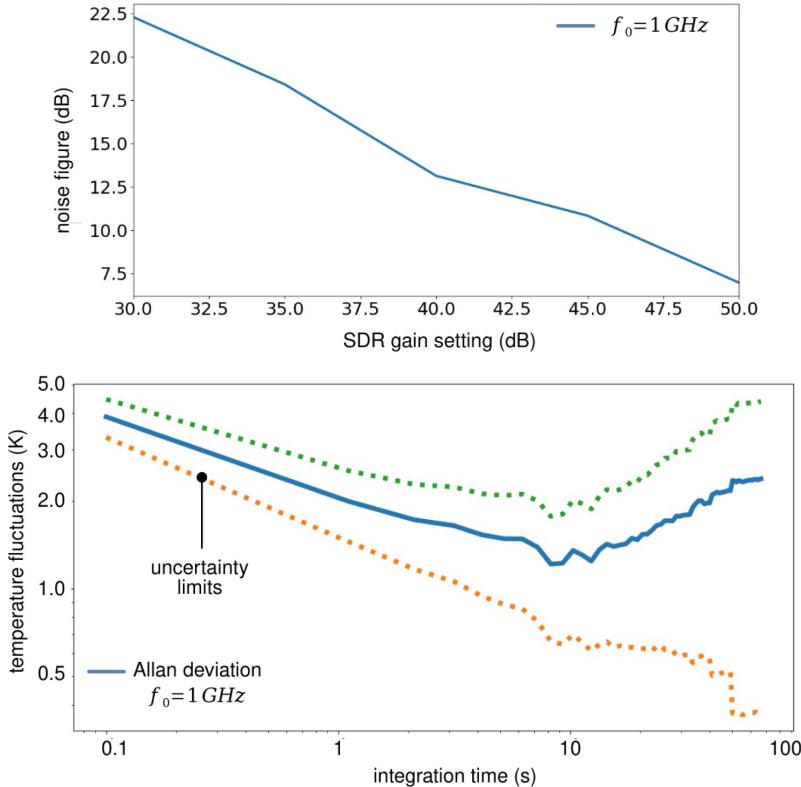


Fig. 7. Results of the RTL-SDR noise experiments. Noise figure at 1 GHz (top) and Allan deviation of the input noise temperature fluctuations (bottom). The 100 s integration time corresponds to 1000 samples at 10 Hz acquisition rate

The antenna radiation pattern with the instrument in its final configuration (parabolic dish, feed horn, structure) is determined using the Sun as the radio source and the Earth's rotation as the scanning mechanism. In particular, it is obtained from the measured antenna noise temperature by removing the sky offset and normalizing the peak of the curve to one. Finally, the acquisition time is converted into an angle using the Earth's rotation speed of 4° per minute, and this is plotted on the x -axis. The radiation pattern derived in this way is shown in the upper left panel of Fig. 4 and is well approximated by Eq. (13) with a half-power beamwidth ($2\rho_H$) equal to 2.2° ² (Fig. 8).

Figure 4 (lower left panel) represents another recording experiment. A peak noise temperature of 450 K is obtained when the instrument is pointed at the

² In this study the solar disk is not deconvolved, i.e. the Sun is assumed to be a point source. Furthermore, due to the latitude and time of observation, the Sun passes diagonally through the antenna beam. As a result, the curve obtained does not represent a radiation pattern cut in the vertical or horizontal plane.

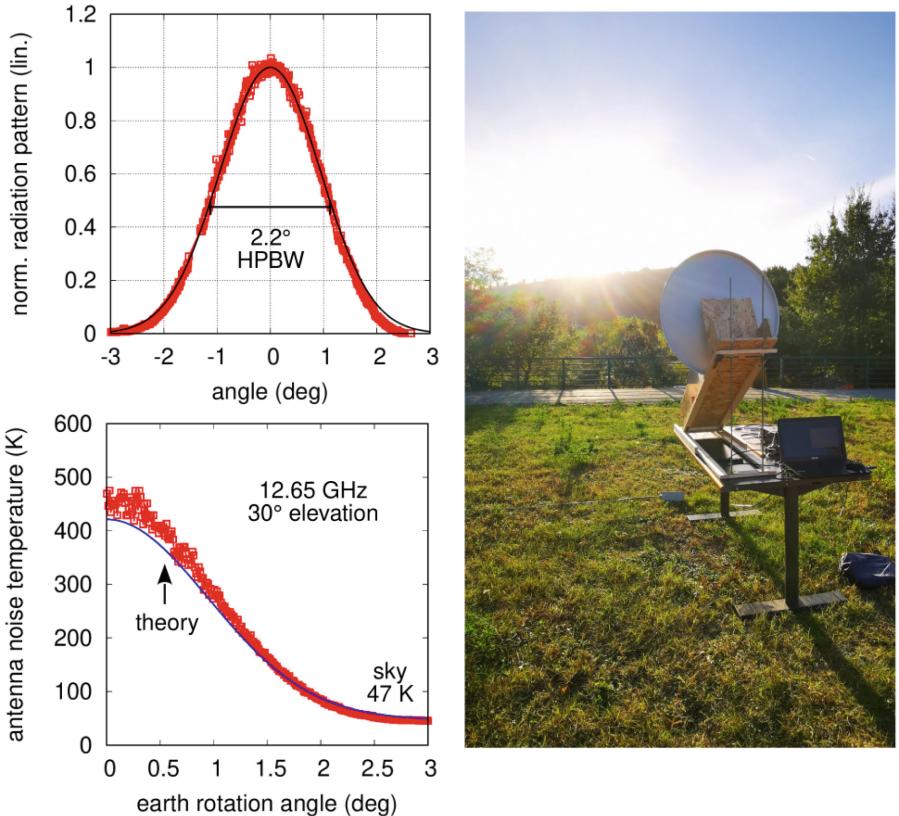


Fig. 8. Results of the October 27, 2023 experiments. The Gaussian beam approximation (13) is in good agreement with measured data (top left panel).

center of the Sun (starting point). The measurements are in good agreement with the proposed theory (system parameters previously estimated) and with solar brightness temperature models [12]. This result is very promising, as it shows that scientific quality data can be obtained with a simple and inexpensive instrument.

6 Conclusion

The breadboards of a low-cost microwave radiometer and radio telescope have been designed and successfully tested in a significant environment. The prototype instrument is capable of measuring the Sun's brightness temperature, and the experimental results are in good agreement with theoretical models.

A joint student project has been launched between the University of Perugia and the Technical University of Berlin, focusing on the construction of small radio telescopes for solar observation. The project is intended to be carried out

by students following an electronic engineering curriculum, and is an opportunity for them to practice with electronics, antennas, microwave systems, and data processing. In addition to the educational value of the project, the students will be able to approach real scientific activities and broaden their knowledge in an interdisciplinary way, particularly in the direction of physics and astronomy.

Finally, based on the foundations laid by this work and as a further development of the proposed breadboards, it will be possible to conceive a miniaturized instrument suitable for flight on board Cubesats. With such an approach, solar observations and solar flare detection will be possible from a space-based platform, thus eliminating the errors associated with atmospheric transmissivity variations. To the best of the author's knowledge, such a scientific mission has never been attempted worldwide.

Acknowledgements. This work is partially supported by: the Erasmus+ programme, the Italian Ministry of University and Research (MUR) in the frame of the “PON 2022 Ricerca e Innovazione” action, the University of Perugia with the “AstroCube” project, and the European Union with the ERC “ELEPHANT” project, contract nr. 948624.

The authors wish to acknowledge Prof. Stefania Bonafoni for the computation of sky temperature and atmospheric transmissivity with the most accurate remote sensing models available in the literature.

F. Alimenti wish to acknowledge the students Simone Burchia and Keidi Kacaku, University of Perugia, for their contribution to some of the experimental results reported in the paper. M. Burla also wishes to acknowledge all the students of the 2024 SIERRA project at TU Berlin for their contributions to the first experimental implementation of an amateur radio telescope at TU Berlin.

References

1. Agilent Technologies: Application Note 57-1: Fundamental of RF and Microwave Noise Figure Measurements (2000)
2. Alimenti, F., et al.: A low-cost microwave radiometer for the detection of fire in forest environments. *IEEE Trans. Geosci. Remote Sens.* **46**(9), 2632–2643 (2008)
3. Alimenti, F., Tasselli, G., Botteron, C., Farine, P., Enz, C.: Avalanche microwave noise sources in commercial 90-nm CMOS technology. *IEEE Trans. Microwave Theory Tech.* **64**(5), 1409–1418 (2016)
4. Bonafoni, S., Alimenti, F., Roselli, L.: An efficient gain estimation in the calibration of noise-adding total power radiometers for radiometric resolution improvement. *IEEE Trans. Geosci. Remote Sens.* **56**(9), 5289–5298 (2018)
5. Farhad, M., Alam, A., Biswas, S., Rafi, M., Gurbuz, A., Kurum, M.: SDR-based dual polarized L-band microwave radiometer operating from small UAS. *IEEE J. Sel. Top. Appl. Earth Obs. Remote Sens.* **17**, 9389–9402 (2024)
6. Fernandez, L., et al.: SDR-based Lora enabled on-demand remote acquisition experiment on-board the Alainsat-1. In: *IEEE International Geoscience and Remote Sensing Symposium (IGARSS)*, Brussels, Belgium, pp. 8111–8114 (2021)
7. Goldsmith, P.F.: *Quasioptical Systems: Gaussian Beam, Quasioptical Propagation and Applications*. IEEE Press (1998)
8. Hersman, M.H., Poe, G.A.: Sensitivity of the total power radiometer with periodic absolute calibration. *IEEE Trans. Microwave Theory Tech.* **29**(1), 32–40 (1981)

9. Italian National Institute for Astrophysics (INAF): A Smart Solar Imaging System at High Radio Frequency for Continuous Solar Monitoring and Space Weather Applications (2023). <https://sites.google.com/inaf.it/solar>. Accessed 21 June 2024
10. Kraus, J.D.: Radio Astronomy. McGraw-Hill, New York (1966)
11. Land, D., Levick, A., Hand, J.: The use of the Allan deviation for the measurement of the noise and drift performance of microwave radiometers. *Meas. Sci. Technol.* **18**, 1917–1928 (2007)
12. Landi, E.: The quiet-sun differential emission measure from radio and UV measurements. *Astrophys. J.* **370**, 1629–1636 (2008)
13. Mattioli, V., Basili, P., Bonafoni, S., Ciotti, P., Westwater, E.: Analysis and improvements of cloud models for propagation studies. *Radio Sci.* **44**, 1–13 (2009)
14. Munoz-Martin, J., Capon, L., de Azua, J.R., Camps, A.: The flexible microwave Payload-2: a SDR-based GNSS-reflectometer and L-band radiometer for Cubesats. *IEEE J. Sel. Top. Appl. Earth Obs. Remote Sens.* **13**, 1298–1311 (2020)
15. Nelson, M.: Implementation and evaluation of a software defined radio based radiometer. Master's thesis, Iowa State University (2016)
16. Rawle, W.D., Lonic, W.P.: A small microwave total power radiometer. *IEEE Antennas Propag. Mag.* **34**(2), 53–54 (1992)
17. Schiavolini, G., et al.: SDR based radio-frequency noise measurements. In: 2024 IEEE Space Hardware Radio Conference (SHaRC), San Antonio, TX, USA, pp. 27–29 (2024)
18. Tasselli, G., Alimenti, F., Bonafoni, S., Basili, P., Roselli, L.: Fire detection by microwave radiometric sensors: modeling a scenario in the presence of obstacles. *IEEE Trans. Geosci. Remote Sens.* **48**(1), 314–324 (2010)
19. Vachhani, K., Mallari, R.: Experimental study on wide band FM receiver using GNURadio and RTL-SDR. In: International Conference on Advances in Computing, Communications and Informatics (ICACCI), Kochi, India, pp. 1810–1814 (2015)
20. Wiegelmann, A., Drake, S., Rehman, S., Chen, S.: Cost-effective Allan deviation measurement in SDRs using integrated ADC. In: IEEE Radio and Wireless Symposium (RWS), San Antonio, TX, USA, pp. 130–133 (2024)
21. Zirin, H., Baumert, B., Hurford, G.: The microwave brightness temperature spectrum of the quiet sun. *Astrophys. J.* **370**, 779–783 (1991)

Sensors Microsystems and Instrumentation



Resistorless Current-Mode Schmitt Trigger for Single-Event Detection in Photomultipliers Front-Ends

Davide Colaiuda^{1,2} , Alfiero Leoni^{1,2} , Gianluca Barile¹ , Vincenzo Stornelli^{1,2} , and Giuseppe Ferri¹ 

¹ Department of Industrial and Information Engineering and Economics, University of L'Aquila, 67100 L'Aquila, AQ, Italy

davide.colaiuda1@graduate.univaq.it, {alfiero.leoni, gianluca.barile,vincenzo.stornelli,giuseppe.ferri}@univaq.it

² INFN Laboratori Nazionali del Gran Sasso, 67100 Assergi, AQ, Italy

Abstract. This work proposes an integrated current-mode non-inverting Schmitt Trigger in a 150nm CMOS technology, without any feedback passive element, for photomultipliers single-event detection. The proposed device is triggered by a current input signal and provides an output voltage that is suitable for interfacing with digital systems. The small currents associated with a reduced number of photoelectrons require a high transimpedance gain and a narrow hysteresis width, making conventional approaches impractical. The proposed device shows a current threshold value to trigger the system, offering a high detection capability also with small currents. In addition, it makes the trigger hysteresis width less sensitive to supply variations. The proposed circuit has great design flexibility, also allowing user to tune the threshold currents using bias voltage reference. The proposed device properly operates under a power supply voltage 1.8 V to 3.3 V. Static power consumption is 10 μ W, with a propagation delay of 25 ns and a total detection delay of 34 ns, driving a 3 pF load capacitance.

Keywords: Photomultipliers · Current-mode · Schmitt Trigger · CMOS

1 Introduction

Recently, Silicon Photomultipliers (SiPMs) gained a lot of interest as photodetectors in scientific, medical, and industrial applications. Their high sensitivity, together with the reduced dimensions, make them suitable for single photon counting and detection purposes [1]. However, to gain benefits from the use of SiPMs, a proper front-end should be designed to avoid load effects and speed limitations, especially when operating with faint signals. According to the applied reverse voltage and to the physical realization of the SiPM itself, currents in the order of a few microamps could be associated with a single photon count.

Many front-end interfaces and ASICs (Application-Specific Integrated Circuits) have been proposed in the literature [2–4], typically involving significative biasing current to achieve an extended dynamic range [5]. However, recent research focused on

devices with extremely reduced power consumption [6–10], due to the large number of autonomous devices that are battery-powered for different applications [11–13]. In addition, great attention has been paid to energy harvesting methods as an auxiliary or main source of energy [14, 15], so that power and area reduction is essential for this kind of systems.

In the field of single-photon detection, the high bias currents of typical SiPMs ASICs, within the range of milliwatts, could result in a waste of power. Moreover, the use of a conventional CMOS Schmitt Trigger, whose area and consumption are extremely low, shows a quite wide hysteresis width [16]; thus, a sufficiently high transimpedance gain is required from the input stage, increasing circuit complexity.

For these reasons, this paper presents a current-mode CMOS Schmitt Trigger (CM-ST) with tunable current thresholds and no passive elements. The current thresholds featured by the device allow a fine control of the responsivity to SiPM pulses. The transistor level schematic, designed in a 150 nm CMOS technology, is presented and its behavior is described, showing the layout and simulations carried out on Cadence Virtuoso environment.

2 Current-Mode Trigger Design

2.1 Theory of Operation

Current-mode signal processing has shown significant benefits in applications involving unconventional signals (*i.e.*, voltage for both input and output) and several blocks have been proposed in the literature [17–20]. Figure 1 depicts a simplified configuration of the circuit, showing the principle of operation of the CM-ST with current thresholds.

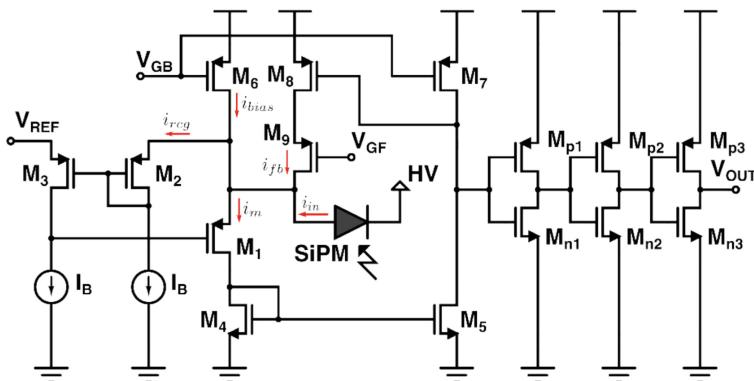


Fig. 1. Schematic of the proposed circuit.

The input stage, consisting of transistors M₁-M₃ (and their bias generators I_B), is a regulated common gate amplifier, featuring a reduced input impedance over a wide bandwidth; this reduces the load effect on the SiPM. The SiPM anode is connected to an AC ground, while the cathode is connected to a DC high voltage (HV) to put it into

Geiger mode; note that the anode DC voltage is virtually V_{REF} due to the local feedback. Bias current to the input stage is provided by M_6 through a bias voltage V_{GB} . The input current is fed to M_4 , which mirrors it into M_5 . The decision stage together is formed by M_5 and M_7 : the high output impedance forces the drain of both transistors to either V_{DD} or ground, depending on which transistor tries to force more current. The positive feedback path is added by M_8 , which acts as a switch, and M_9 , that provide a constant current through the bias voltage V_{GF} that adds up to the current sunk by M_1 ; note that when this additional current is turned on, less current is required to change back the output stage and turn it off (*i.e.*, the DC bias current in M_1 increases and M_5 drives more current, neglecting the input). Finally, a series of three cascaded inverters $M_{n1}-M_{n3}$ and $M_{p1}-M_{p3}$ increases the drive capability of a high capacitive load, while also providing sharp edges of the trigger.

2.2 Current Threshold and Hysteresis

The described behavior can be modeled considering the dynamic currents on each input device of Fig. 1. When a current pulse is provided by the SiPM, the total current flowing into M_1 is equal to:

$$I_m = I_{bias} - I_{rcg} + i_{in} + i_{fb} = I_{DC} + i_{in} + i_{fb} \quad (1)$$

The fixed current I_{DC} represents the effective DC current flowing into M_1 , while the only dynamic contribution is given by i_{in} and i_{fb} , which depends on the output state. First, assuming i_{fb} equal to zero (so output voltage at ground) and defining as $i_{7,sat}$ M_7 saturation current, we find that the first threshold current value is given by:

$$I_{th,H} = I_{7,sat} - I_{DC} \quad (2)$$

When the total current in M_1 , mirrored to M_5 , overcomes this value, the drain of M_5 and M_7 are forced to ground, with M_5 going to the triode region, turning on the feedback current source M_9 (that further force this node to ground) moving the output to V_{DD} . Since part of the current I_m is now supplied by the additional current i_{fb} provided by M_9 , to force the output back to ground, the input current should decrease below a threshold value that is given by:

$$I_{th,L} = I_{7,sat} - I_{DC} - i_{fb} = I_{th,H} - i_{fb} \quad (3)$$

2.3 Design Criteria

This analysis is affected by transistor channel width modulation, that slows down the response and shifts the effective threshold values. First, the non-finite output resistance at M_7 drain makes the decision stage less responsive if the input signal overcomes the threshold by a very small amount. Thus, increasing the output resistance at this node can increase the triggering responsivity: this can be done by increasing channel length or cascading the two devices. M_9 drain voltage is maintained at V_{REF} , so that the effective feedback current (that defines the hysteresis width) is less affected by channel modulation

effects of M_9 . To achieve this, the local feedback gain regulating M_1 gate should have a sufficient gain. To let the voltage variation on M_1 gate quickly change its current, a short channel should be implied: the responsivity of the trigger depends on the speed of this device, of the gate amplifier, and of the current mirror (which is however not critical). The cascaded inverters M_{n1} - M_{n3} and M_{p1} - M_{p3} must be sized depending on the fanout required; for small load capacitance, a single inverter can be implied. To improve the threshold switch, the gate of M_8 can be driven with two cascaded inverters, providing a sharp switch.

3 Simulations and Results

The proposed device has been simulated on Cadence Virtuoso using the LF150A CMOS technology provided by LFoundry. This technology enables SPAD (Single-photon Avalanche Diode) integration, that can simplify the integration of the trigger in a full ASIC. The circuit operates with a 1.8 V supply and can be supplied up to 3.3 V, due to the thick gate oxide of the devices. Bias voltages V_{GB} and V_{GF} have been implemented by diode-connected transistors (properly dimensioned), setting the two threshold currents to approximately 800 nA and 300 nA, respectively. The reference voltage is kept at 900 mV (half of the dynamics), while the bias current for the gate-regulation amplifier is set to 2 μ A, and the bias current of M_1 is set to 1 μ A.

To emulate the SiPM behavior, the equivalent model proposed in [21] has been considered; Fig. 2 shows the parameters used for simulations, taken from measurements on an FBK SiPM. In static conditions, with output at ground and the feedback device turned off, the static power consumption is approximately 10 μ W.

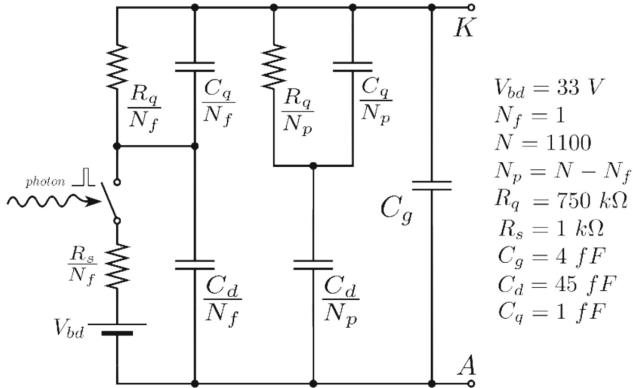


Fig. 2. Equivalent SiPM model used in simulations.

Figure 3 shows the layout of the designed CM-ST, while in Fig. 4 the hysteresis curve is reported for different PVT variations, considering typical, fast and slow processes (and their combinations) for each device, with voltage supply equal to 1.8 V \pm 100 mV and for -40°C , 27°C and 80°C , obtaining a total of 45 corners. The matched devices used to

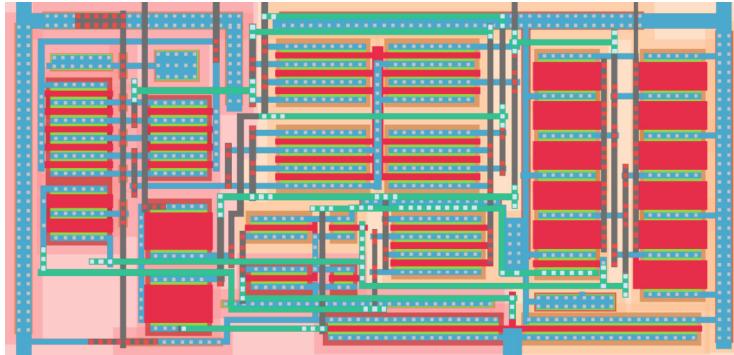


Fig. 3. Layout of the proposed device, the total area is $684 \mu\text{m}^2$.

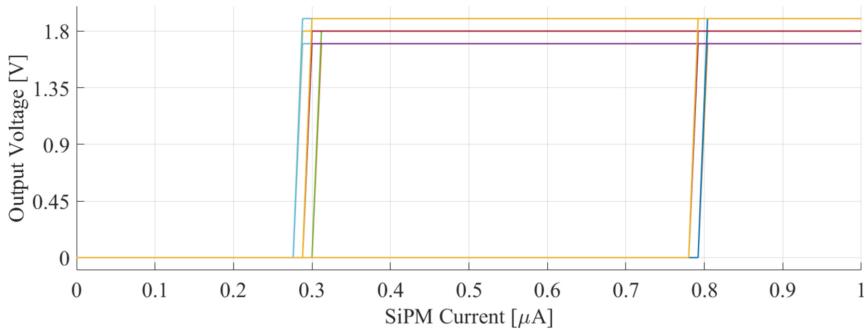


Fig. 4. DC transfer characteristics of the CM-ST; the 45 corners curves overlay due to the current resolution step used in the simulations.

generate the bias voltages reduce the PVT variations over the threshold voltages, whose value relies on the quality of the current reference used.

For the transient analysis, the I/O pad of the technology has been connected to the output as a load; this has a capacitance of approximately 3 pF. The circuit response of a single photoelectron is shown in Fig. 4. The propagation delay of the trigger was found to be 25 ns; however, the total delay from the photon incoming (that can be assumed as the true delay time) is equal to 34 ns, generating a 186 ns positive pulse that can efficiently be processed by a digital interface. Thanks to the output inverters, the slope of this pulse reaches approximately 1000 V/ μs for both the rising and the falling edge.

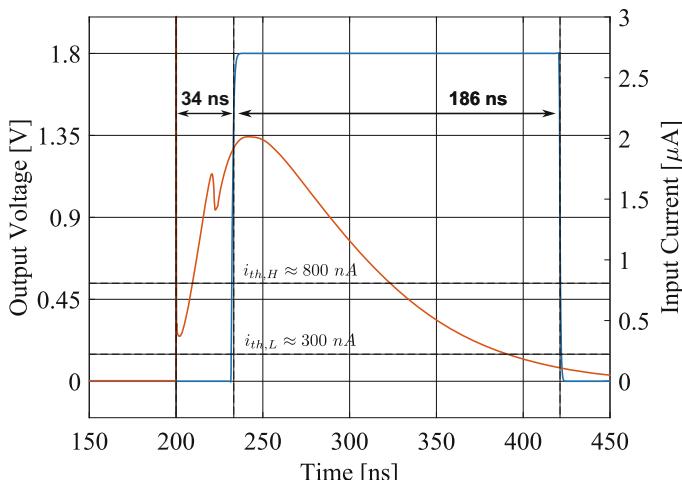


Fig. 5. Transient response of the proposed current-mode trigger considering the detection of a single photoelectron from the SiPM.

4 Conclusions

This work proposed a novel current-mode Schmitt Trigger for single photon detection with SiPMs in CMOS technology. The device shows reduced power consumptions and a high detection capability, that can be tuned by properly designing the active components bias voltages. The design has great flexibility, and sizing can be optimized depending on the required specifications on power consumption and time delay. The reduced delay times, together with reduced consumption and drive capability, make the proposed circuit a valid solution for single-event detection application involving photomultipliers towards the development of standalone battery-powered portable devices.

References

1. Gundacker, S., Heering, A.: The silicon-photomultiplier: fundamentals and applications of a modern solid-state photon detector. *Phys. Med. Biol.* **65**(17) (2020). <https://doi.org/10.1088/1361-6560/ab7b2d>
2. Dorosz, P., Baszczyk, M., Kucewicz, W., Mik, Ł.: Low-power front-end ASIC for silicon photomultiplier. *IEEE Trans. Nucl. Sci.* **65**(4), 1070–1080 (2018). <https://doi.org/10.1109/TNS.2018.2816239>
3. Argentieri, A., Corsi, F., Foresta, M., Marzocca, C., Del Guerra, A.: Design and characterization of CMOS multichannel front-end electronics for silicon photomultipliers. *NIM-A* **652**(1), 516–519 (2011). <https://doi.org/10.1016/j.nima.2010.08.067>
4. Topkar, A., Singh, A., Aggrawal, B., Chakraborty, S., Kumar, A.: Development of Silicon Photomultiplier sensors using a 180 nm custom CMOS process technology. *J. Instrum.* **15**(03), P03032–P03032 (2020). <https://doi.org/10.1088/1748-0221/15/03/P03032>
5. Corsi, F., Foresta, M., Marzocca, C., Matarese, G., Del Guerra, A.: A self-triggered CMOS front-end for silicon photomultiplier detectors. In: Proceedings of IWASI 2009, Trani, Italy (2009). <https://doi.org/10.1109/IWASI.2009.5184772>

6. Della Sala, R., Centurelli, F., Scotti, G.: A novel differential to single-ended converter for ultra-low-voltage inverter-based OTAs. *IEEE Access* **10**(1), 98179–98190 (2022). <https://doi.org/10.1109/ACCESS.2022.3206014>
7. Barile, G., et al.: CMOS adaptive biased second generation voltage conveyor. In: *Proceedings of BATS 2023*, Catanzaro, Italy (2023). <https://doi.org/10.1109/BATS59463.2023.10303178>
8. Barile, G., et al.: Nonlinear adaptive biasing for low-voltage class-AB OTAs. In: *Proceedings of SIE 2023*, Noto, Italy (2023). https://doi.org/10.1007/978-3-031-48711-8_4
9. Ballo, A., Grasso, A.D., Palumbo, G., Tanzawa, T.: Charge pumps for ultra-low-power applications: analysis, design, and new solutions. *IEEE Tran. Circ. Syst. II: Espress Briefs* **68**(8), 2895–2901 (2021). <https://doi.org/10.1109/TCSII.2021.3070889>
10. Park, K., Yeom, S., Kim, S.Y.: Ultra-low power CMOS image sensor with two-step logical shift algorithm-based correlated double sampling scheme. *IEEE Trans. Circ. Syst. I: Regular Papers* **67**(11), 3718–3727 (2020). <https://doi.org/10.1109/TCSI.2020.3012980>
11. Wentzloff, D.D., Alghaihab, A., Im, J.: Ultra-low power receivers for IoT applications: a review. In: *Proceedings of CICC 2020*, Boston, MA, USA (2020). <https://doi.org/10.1109/CICC48029.2020.9075938>
12. Colaiuda, D., et al.: Smart Internet of Things (IoT) system for construction sites monitoring. In: *Proceedings of AISEM 2023*, Virtual, Online (2022). https://doi.org/10.1007/978-3-031-25706-3_31
13. Min, J., et al.: An autonomous wearable biosensor powered by a perovskite solar cell. *Nat. Electron.* **6**, 630–641 (2023). <https://doi.org/10.1038/s41928-023-00996-y>
14. Sherazi, H.H.R., Zorbas, D., O'Flynn, B.: A comprehensive survey on RF energy harvesting: applications and performance determinants. *Sensors* **22**(8), 2990 (2022). <https://doi.org/10.3390/s22082990>
15. Leoni, A., Ferri, G., Colaiuda, D., Stornelli, V.: Micro energy harvesting from the soil of indoor living plants. In: *Proceedings of SpliTech 2022*, Split, Croatia (2022). <https://doi.org/10.23919/SpliTech55088.2022.9854259>
16. Hosseinejad, M., Erfanian, A., Karami, M.A.: On the design of low power CMOS schmitt trigger for biomedical application. In: *Proceedings of ICEE 2019*, Yazd, Iran (2019). <https://doi.org/10.1109/IranianCEE.2019.8786613>
17. Safari, L., Barile, G., Stornelli, V., Ferri, G.: A review on VCII applications in signal conditioning for sensors and bioelectrical signals: new opportunities. *Sensors* **22**(9), 3578 (2022). <https://doi.org/10.3390/s22093578>
18. Kumar, P., Kaushik, B.K., Ranjan, R.K.: A novel second generation current conveyor (CCII)-based high frequency memristor model. *Microelectron. Eng.* **271272**, 111938 (2023). <https://doi.org/10.1016/j.mee.2023.111938>
19. Colaiuda, D., Leoni, A., Barile, G., et al.: Characterization of a novel SiPM sensor interface using an off-the-shelf second-generation voltage conveyor. In: *Proceedings of SIE 2023*, Noto, Italy (2023). https://doi.org/10.1007/978-3-031-48711-8_23
20. Chaturvedi, B., Kumar, A., Mohan, J.: Low voltage operated current-mode first-order universal filter and sinusoidal oscillator suitable for signal processing applications. *AEU-Int. J. Electron. Commun.* **99**, 110–118 (2019). <https://doi.org/10.1016/j.aeue.2018.11.025>
21. Marano, D., Belluso, M., Bonanno, G., et al.: Silicon photomultipliers electrical model extensive analytical analysis. *IEEE Trans. Nucl. Sci.* **61**(1), 23–34 (2014). <https://doi.org/10.1109/TNS.2013.2283231>



The Front-End Charge Readout IC for the LEM-X Mission Concept

Filippo Mele^{1(✉)}, Marco Grassi², Irisa Dedolli¹, Piero Malcovati², Riccardo Campana³, Ettore Del Monte⁴, Yuri Evangelista⁴, Marco Feroci⁴, and Giuseppe Bertuccio¹

¹ Politecnico di Milano, 22100 Como, Italy
filippo.mele@polimi.it

² Università di Pavia, 27100 Pavia, Italy

³ INAF-OAS, 40129 Bologna, Italy

⁴ INAF-IAPS, 00133 Rome, Italy

<https://sdiclab.deib.polimi.it/>

Abstract. The application specific integrated circuit (ASIC) for the front-end charge readout of the X-ray detector for the LEM-X lunar mission concept is presented. The bare die ASIC is composed by a linear array of 32 channels with 150 μm pitch directly wire-bonded to a large-area multi-anode silicon drift detector (SDD) used as the detection plane of an X-ray coded aperture camera. Each anode readout channel integrates an independent analog/ mixed-signal spectroscopic chain composed by a continuous-reset charge sensitive amplifier, a current-mode shaping amplifier, an amplitude discriminator for event detection, a peak-detect and hold circuit for external sampling and time-stamping, and a pile-up rejection logic. The top level circuitry is dedicated to the analog multiplexing and SPI communication with the off-chip back-end electronics. The ASIC, sent for production on a 0.35 μm ultra low-noise CMOS technology, when coupled to the detector, permits to reach a simulated system equivalent noise charge of less than 13 electrons rms, allowing the readout of low-energy X-ray photons from 0.5 keV up to 70 keV at 0 °C, and complying with an functional temperature range from -55 °C to +30 °C.

Keywords: Application Specific Integrated Circuit · Nuclear Microelectronics · Semiconductor Radiation Detectors

1 Introduction

The Lunar Electromagnetic Monitor in X-rays (LEM-X) is an all-sky monitor mission concept for the 2–50 keV energy band based on coded aperture X-ray cameras [1]. Exploiting an installation site on the surface of the Moon, the LEM-X detection instruments is conceived to present a wide angular coverage of the sky realizing a “dome” of modular camera assemblies [2], hardly achievable on satellite-borne instruments, due to the known limits in size, weight and power resources. The basic camera module makes use of the coded aperture mask imaging technique, and relies on the heritage of the wide field monitor instrument (WFM) developed for the eXTP space mission [3].

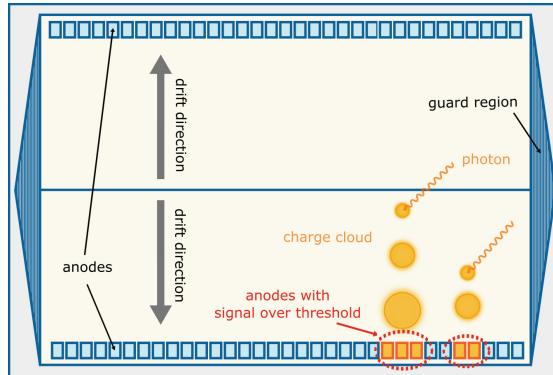


Fig. 1. The concept of large-area linear silicon drift detector (SDD). The anodes and the readout ASICs are located at both top and bottom edges of the sensor, which collect signals from two symmetrical drift regions. Upon arrival of X-ray photons, the charge cloud produced is drifted, and expands during the drift, triggering multiple anode readout channels. Dimensions are not to scale.

2 Detector Assembly

Each camera will be realized with four detector assemblies (DA), tiled together on the same tray to realize a large detection plane. The energy dispersive sensor of each DA will be a multi-anode large area (approx. 45 cm^2) silicon drift detector (SDD) with $450\text{ }\mu\text{m}$ thickness developed in Italy by a collaboration of INFN (Istituto Nazionale di Fisica Nucleare), INAF (Istituto Nazionale di Astrofisica), ASI (Agenzia Spaziale Italiana) and FBK (Fondazione Bruno Kessler), with both imaging and spectroscopic capabilities. To achieve a large active area and high spatial resolution, the LEM-X project adopts linear SDDs [4]; with respect to more common pixel-based imaging sensors, linear SDDs allow to reconstruct the X-ray position of interaction with a reduced number of readout channels, allowing at the same time a smaller power consumption and a more compact front-end electronics setup. With this architecture, the charge produced by the X-ray photons absorbed in the active area of the detector, is drifted toward a linear array of 384 finely spaced anodes located on both opposite edges of the sensor, as conceptually shown in Fig. 1. As the charge cloud drifts across the fully-depleted high-resistivity sensor's volume, it expands per effect of electrostatic repulsion and diffusion phenomena [5], spreading over an area covered by multiple anodes, and triggering the readout from several channels in the front-end ASIC. The evaluation of the charge cloud diameter by a simultaneous readout of neighbouring anode charge signals, allows thus a reconstruction of drift time, and consequentially, the original position of the photon interaction.

In its foreseen final application [6], a front-end board will host one large-area sensor and the 24 readout ASICs (12 on each of the drift sides of the detector), designed for tiling with minimum dead-area overhead on the detection plane. In order to allow a direct wire-bonding interconnection between the SDDs and

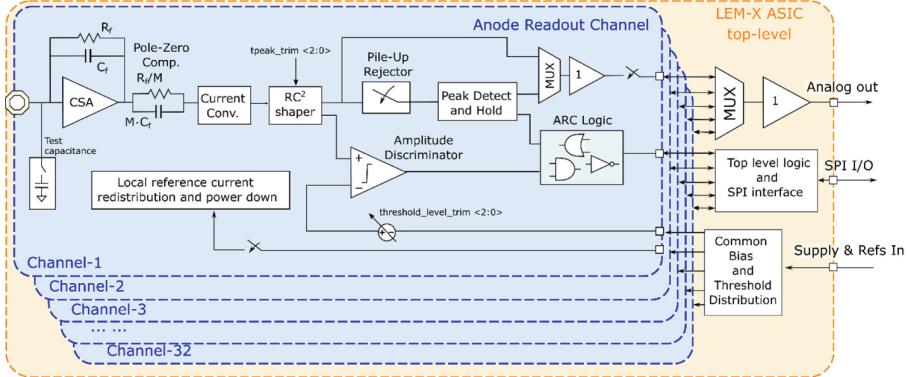


Fig. 2. Schematic representation of the LEM-X front-end ASIC architecture.

the readout ASICs, the anode-pitch of the SDDs ($169 \mu\text{m}$) are matched to the 32-channel-pitch of the ASIC ($150 \mu\text{m}$), with some minimal clearance ($<1 \text{ mm}$) reserved for the ASIC placement. This allows to keep the stray capacitance due to the anode interconnection as low as possible, ranging, according to FEM (Finite Element Method) simulation, from 40 to 150 fF. However, the overall input capacitive load is relatively high considering that the anode capacitance is estimated to be about 90 fF, setting an extremely tight constraint in the noise budget of the front-end circuitry, which is required to operate with an equivalent noise charge (ENC) of less than 13 electrons rms.

3 Readout IC Architecture

A schematic representation of the ASIC block diagram is presented in Fig. 2. The ASIC consists of a linear array of 32 Anode Readout Channels (ARC). Each channel independently collects the charge signal at a single anode of the multi-anode SDD at which it is connected. The ARC blocks realize most of the analog signal processing functions (charge to voltage conversion, signal amplification, signal shaping, peak detection and sampling [7], pile-up rejection etc.) with several configurable parameters, such as a selectable shaping time for in-operation optimum noise filtering and an analog trimming for the MOS-based continuous reset discharge time constant, the energy threshold for the global (i.e. at ASIC-level) and local (i.e. at channel level) tuning and the signal baseline level control. As soon as a charge signal on one ARC exceeds the energy threshold, the trigger signal can be forwarded to adjacent ARC (OR trigger modality) of the same ASIC, or to adjacent ASICs on the same sensor side (external trigger). This internal/external trigger synchronization is of particular interest for the linear SDD architecture, because it allows to perform a trigger-based readout of ARC cells that are collecting the signals at the edges of the charge cloud, typically characterized by a smaller signal which can easily fall below the threshold of detection.

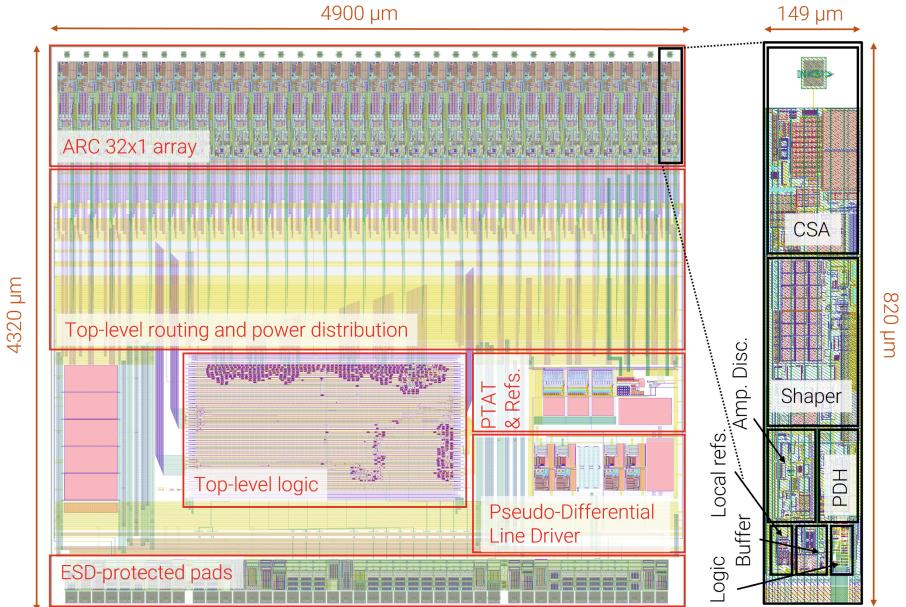


Fig. 3. Physical layout of the first 32-channel front-end ASIC prototype. A zoom of a single Anode Readout Cell is shown on the right.

The top-level circuitry collects and multiplexes the analog output signals produced by the ARC array, delivering a pseudo-differential analog signal, proportional to the readout charge, to the external analog to digital converter. Due to the sparsified nature of signals, that are only collected by a reduced number of channels, at an input count rate lower than 100 counts per second, the multiplexing allows a significant simplification in the external routing, constrained by the very small dimensions of the detection assembly PCB. Additionally, the top-level circuitry provides the proper analog and digital supply and control voltages/currents for each channel, and arranges the communication with the external control logic by means of a Serial Peripheral Interface (SPI) synchronous serial protocol (Fig. 3).

4 Physical Implementation and Simulation Results

The layout of the complete 32-channel ASIC FE is represented in Fig. 2. The ASIC was realized on 0.35 μm CMOS technology (C35B3C3) by AMS. The adopted technology demonstrated in previous projects and extremely low-noise performance in baseband up to 50 MHz [8] and sufficient radiation hardness to ensure compatibility to the mission requirements in terms of TID (total ionizing dose), SEL (single event latchup) and SEU (single event upset) robustness [9]. With respect to other state-of-the-art ASICs realized at SDIC-Lab [10] for other

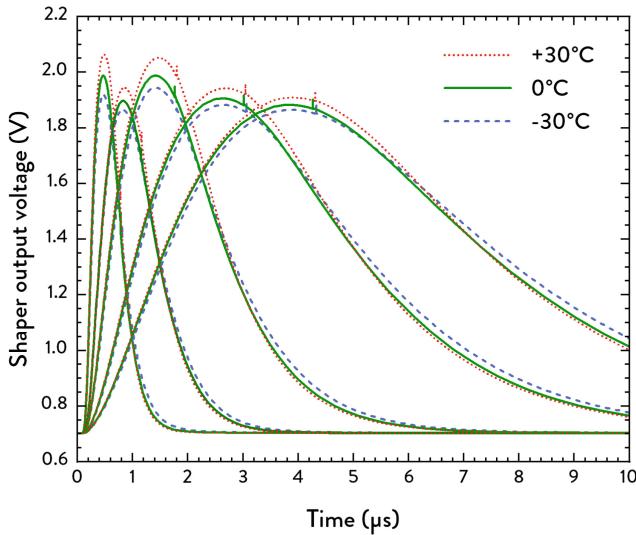


Fig. 4. Simulation of the voltage transient at the output of the shaping amplifier at different temperatures ($-30, 0, +30^{\circ}\text{C}$) for the selectable shaping times ($0.4/0.9/1.4/2.6/3.8\ \mu\text{s}$). A small spike after the shaper peaking time is caused by the peak-detect and hold circuit, which enables the internal pile-up rejection, effectively disconnecting the shaper output from the back-end processing chain.

SDD-based space mission/concepts Table 1, the LEM-X ASIC is characterized by the most stringent requirement of low-noise performance (13 electrons of equivalent noise charge, when connected to a total input load capacitance of $250\ \text{fF}$, and in presence of a typical detector reverse current of $3\ \text{pA}$) and a narrow pixel pitch ($150\ \mu\text{m}$). As often happens in nuclear microelectronics applications characterized by different detector specifications, a substantial redesign of the CSA is necessary for the achievement of the capacitive matching condition at the input stage [11]. A large functional temperature range of $-60/+80^{\circ}\text{C}$ and a performance operating range of $-30/+30^{\circ}\text{C}$ are linked to the ASIC application on the Moon surface. With this respect, proportional to absolute temperature (PTAT) current-mode bias distribution circuitry, helps to guarantee a better stability of the devices transconductance over large multi-channel arrays [12]. Using an SPI protocol, the shaping amplifier peaking time can be modified to optimally filter the noise components, rising from different temperature and detector leakage conditions. The ASIC can be configured to set 5 different shaping times, from $0.4\ \mu\text{s}$ to $3.8\ \mu\text{s}$. The conversion gain for the different selections is internally equalized to show a uniform signal amplitude to the external ADC, as shown by the simulation in Fig. 4.

Simulation results predict an optimum equivalent noise charge of 12 electrons rms at the optimum peaking time of $1.4\ \mu\text{s}$ at the nominal operating temperature of -30°C , and less than 14 electrons rms, over the complete functional

temperature range from -55°C to $+30^{\circ}\text{C}$, assuming a worst-case SDD capacitance of 250 fF and 3 pA of anode dark current. The ASIC shows a maximum input charge of approximately 260 000 electrons, corresponding to an equivalent maximum input energy of 70 keV on silicon. The expected power consumption is of 950 μW per channel, with the possibility to power down each channel independently for operation on different detectors with reduced number of anodes.

Table 1. Comparative table of ASICs produced for space missions at Politecnico di Milano - Semiconductor Devices and Integrated Circuits laboratory.

Reference	Project/Mission	Maximum Energy Range	Detector type	Pixel pitch	Input load ($C_{det} + C_{stray}$)	ENCL(optimum)	Power consumption	Area (per channel)	Shaping	ADC
This work	LEM-X	70 keV in Si	Linear SDD	150 μm	<250 fF	12 el. (bias) w/ C_{det}	1 nW/ch.	0.67 mm ²	2nd order semi-gauss.	External
ORION [13]	THESESUS	3.6 MeV in Cd(Tl)	SDD-SiSwitch	7 μm	<50 fF	>-31 el. (meas.) w/ C_{det}	0.34 mW/ch.	0.51 mm ² (FE) + 5.1 mm ² (BD)	1st/3rd order semi-gauss.	12-bit 2 nd or incremental
LYRA [14]	HERMES	2.2 MeV in GAGG	SDD-SiSwitch	7 μm	<50 fF	>-22 el. (meas.) w/ C_{det}	0.6 mW/ch.	0.26 mm ² (FE) + 0.51 mm ² (BD)	1st order semi-gauss.	External
RIGEL [15]	ADAM/ Psd0	0.0 keV in Si	MinSDDmatrix	300 μm	<40 fF	>-14 el. (meas.) w/ C_{det}	0.55 mW/ch.	0.4 mm ²	1st order semi-gauss.	10-bit Wilkinson
VEGA [16]	LOFT	60 keV in Si	Linear SDD	970 μm	<350 fF	>12 el. (meas.) open input	0.55 mW/ch.	0.51 mm ²	1st order semi-gauss.	External
STAR-X [17]	LF-ESA	50 keV in GaAs	Pixel matrix	300 μm	<400 fF	>15 el. (meas.) w/ C_{det}	0.50 mW/ch	0.09 mm ²	1st order semi-gauss.	10-bit Wilkinson

References

1. Skinner, G.K.: Nuclear instruments and methods in physics research section a: accelerators. *Spectrom. Detect. Assoc. Equip.* **221**(1), 33 (1984)
2. Lombardi, G., Evangelista, Y., Biancolini, M.: In IOP Conference Series: Materials Science and Engineering, vol. 1306 (IOP Publishing, 2024), vol. 1306, p. 012016 (2024)
3. Hernanz, M., et al.: In: Space Telescopes and Instrumentation 2022: Ultraviolet to Gamma Ray, vol. 12181 (SPIE, 2022), vol. 12181, pp. 484–497
4. Gramegna, C., et al.: *IEEE Trans. Nucl. Sci.* **42**(5), 1497 (1995)
5. Quercia, J., Mele, F., Eremeev, I., Bertuccio, G.: In: 2023 IEEE Nuclear Science Symposium, Medical Imaging Conference and International Symposium on Room-Temperature Semiconductor Detectors (NSS MIC RTSD) (IEEE, 2023), p. 1
6. Ceraudo, F., et al.: In: Space Telescopes and Instrumentation 2024 (SPIE)
7. Mele, F., Dedolli, I., Bertuccio, G.: *IEEE Solid-State Circuits Letters* **5**, 74 (2022)
8. Mele, F., et al.: *IEEE Trans. Nucl. Sci.* **68**(3), 379 (2021)
9. Ceraudo, F., et al.: Nuclear instruments and methods in physics research section a: accelerators. *Spectrom. Detect. Assoc. Equip.* **1037**, 166903 (2022)
10. Politecnico di Milano - Semiconductor Devices and Integrated Circuits laboratory. <https://sdiclab.deib.polimi.it/>
11. Bertuccio, G., Mele, F.: *IEEE Transactions on Nuclear Science* (2023)
12. Dedolli, I., Mele, F., Bertuccio, G.: In: 2023 IEEE Nuclear Science Symposium, Medical Imaging Conference and International Symposium on Room-Temperature Semiconductor Detectors (NSS MIC RTSD) (IEEE, 2023), p. 1
13. Mele, F., et al.: *IEEE Trans. Nucl. Sci.* **68**(12), 2801 (2021)
14. Gandola, M., Mele, F., Grassi, M., Malcovati, P., Bertuccio, G.: *J. Instrum.* **16**(12), T12013 (2021)
15. Gandola, M., Grassi, M., Mele, F., Dedolli, I., Malcovati, P., Bertuccio, G.: Nuclear instruments and methods in physics research section a: accelerators. *Spectrom. Detect. Assoc. Equip.* **1040**, 167249 (2022)

16. Ahangarianabhari, M., Macera, D., Bertuccio, G., Malcovati, P., Grassi, M.: Nuclear instruments and methods in physics research section a: accelerators. Spectrom. Detect. Assoc. Equip. **770**, 155 (2015)
17. Bastia, P., et al.: Starx32: a complete on-chip x-ray spectroscopy readout system with imaging capability (2010)



Sensor-Based Monitoring of Physical Activity for Glucose Management in Diabetic Patients: A Review

Sara Campanella^(✉) and Lorenzo Palma

Department of Information Engineering, Università Politecnica delle Marche,
Via Brecce Bianche 12, 60131 Ancona, Italy
s.campanella@pm.univpm.it, l.palma@staff.univpm.it

Abstract. Continuous glucose monitoring makes it possible to forecast the trajectory of future glucose concentrations. Meals, insulin, and other physiological and metabolic changes, such as physical activity, all impact glucose concentration. Devices monitoring patients' physical activity are being developed to solve these problems. This review focuses on non-invasive sensors used to enhance glucose monitoring in patients with type 1 diabetes by utilising physiological characteristics associated with physical exercise. The search yielded 37 original research publications, from which we selected the most significant aspects regarding the devices, the various types of sensors and data acquired, the physiological signal, and the methodologies applied to analyze and use this data. The capacity to evaluate physiological data in real-time has been transformed by the growing integration of embedded artificial intelligence systems, enabling a more precise and prompt assessment of patient circumstances, including measuring glucose levels.

Keywords: Wearable sensors · Physical activity monitoring · Embedded AI system · CGM · Diabetes · Wireless Sensor Network

1 Introduction

Diabetes is a long-term metabolic disease that causes hyperglycemia due to problems with insulin secretion or action. Diabetes care requires close monitoring of blood glucose levels. Although widely used, techniques such as finger pricks and continuous glucose monitoring (CGM) devices have drawbacks, particularly when it comes to identifying hypoglycemia. Several technologies have been put forward for the noninvasive measurement of blood glucose levels. The goal of “minimally invasive CGM” or “non-invasive continuous glucose monitoring” (NI-CGM) was to provide more consistent, or even real-time, glucose readings, enabling more effective self-monitoring. These technologies take use of the modifications that the presence of glucose molecules makes on the chemical and physical characteristics of tissues [12]. However, meaningful interpretation

of glucose levels requires additional context, including but not limited to food, exercise, medicine, sleep patterns, and mental health [18].

Globally, wearable and mobile technologies are opening up new possibilities for safe, affordable medical care as well as information transmission. They are extremely useful in the healthcare industry due to their ability to collect, store, and occasionally analyse data. Doctors and patients can use these features to manage, treat, and evaluate their diseases [30]. Numerous biosensors, most of which are non-invasive, are now being developed to track patients' physical activity levels and cardiac data, such as electrocardiograms, or ECGs. They have shown to be useful in determining when T1DM patients start and stop engaging in physical activity [12]. Additionally, recent research has employed vital sign sensors and physical exercise to anticipate hypoglycemia and maintain euglycemia [25,26].

Artificial intelligence (AI) will cause a paradigm shift in diabetic management through data-driven precision care [14]. These algorithms can be used to create strategies for assessing and identifying relevant components from the previously provided data to understand their influence on diabetes therapy. AI enables patients to have knowledge and to be empowered. Digital solutions have a significant influence on patient behaviours, comorbidities, length of stay in hospitals, frequency of travel to and interaction with healthcare professionals, and other aspects of healthcare systems [15]. Integrated with wearable devices, AI offers real-time data analysis, diet and exercise recommendations, remote monitoring, and improved medication adherence. This seamless integration enables proactive management and better health outcomes for diabetic patients.

Thus, this paper aims to investigate sensors that make use of physiological factors linked to physical activity to improve glucose monitoring in individuals with type 1 diabetes. By examining the integration of these sensors with AI and wearable technology, the research explores how continuous monitoring and analysis of physical activity can enhance the accuracy and effectiveness of glucose management (Fig. 1). The goal is to provide a comprehensive understanding of how physiological data, such as heart rate, activity levels, and other vital signs, can be utilized to optimize glucose control and predict fluctuations.

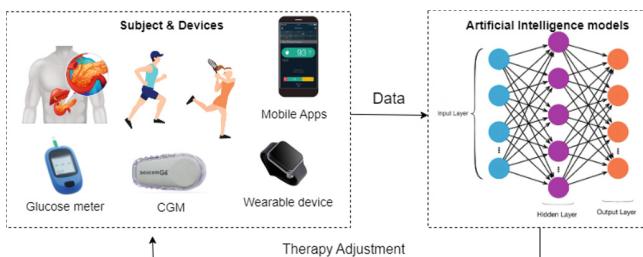


Fig. 1. Schematic representation of physical activity monitoring and its usage for AI model.

2 Materials and Methods

To ensure adherence with the PRISMA statement [27], a comprehensive analysis was conducted using PubMed, Web of Science, IEEE Xplore, Scopus, and Google Scholar databases in April-May 2024. Using the chosen databases, it was easier to evaluate technical and medical papers thoroughly. The phrases “diabetes”, “type 1”, “physical activit*”, “device*”, “wristband”, “band”, “monitoring”, “CGM”, “parameter*”, “adulescent*”, and “adult*” were among those whose terms were included in the query search utilising the truncation symbol *. The Boolean operators “OR” and “AND” were used. We extract the following information: data collection equipment, integrated sensors, physiological collected data, conditions by which these physiological signals were obtained, and methods to analyse them. The studies were imported into Mendeley Reference Manager to remove duplicates. Review papers were excluded; only research papers with titles, abstracts, and the complete text were considered. The following criteria were used to exclude titles, abstracts, and complete texts: i) no English publications; ii) insufficient information about the study design and results; iii) comparative studies in the medical field.

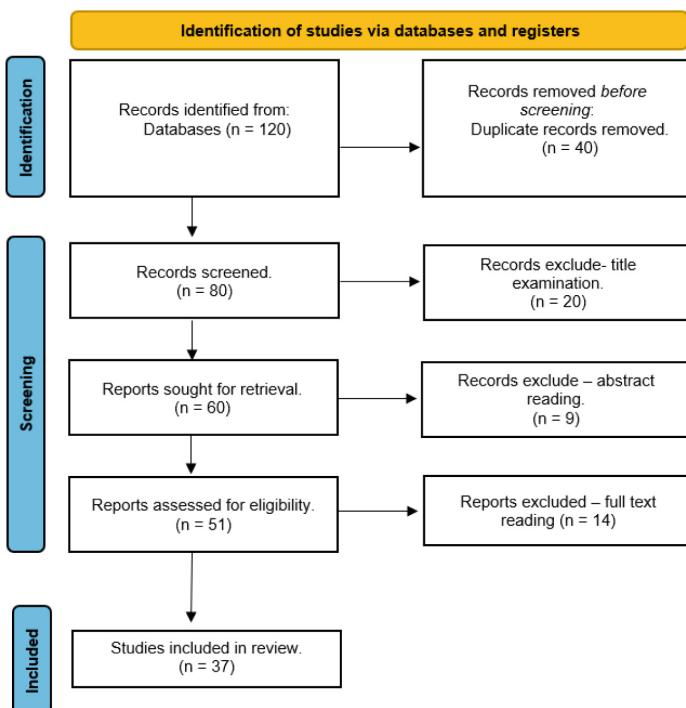


Fig. 2. Selection process of the eligible articles.

3 Results and Discussion

After the removal of the duplicates, we obtained 80 articles eligible for the next steps from the 120 original ones. Firstly, we excluded the articles based on the titles. So, 60 articles were examined in the second step. Here, the abstract was evaluated and 51 articles were selected for the full-text-reading procedure. We manually assessed the eligibility of the remaining papers by full-text inspection and included 34 documents in the final collection. In Fig. 2, it is reported the selection process.

Similar structures could be found in the 34 articles that were kept. Each study collected data using a clinical protocol that involved gathering two types of data: (1) phenotypic characteristics of the T1D participants (e.g., age, sex, duration of diabetes, glucose and glycated haemoglobin levels (HbA1c)); (2) physiological function of interest (e.g., cardiac autonomic function), by measuring one or more physiological parameters. All articles referred to clinical studies involving human participants.

Our analysis of the retained articles evolved along the axis of this survey's research question: *Do the existing wearable, noninvasive sensors have the potential to improve how T1D is monitored, especially during physical exercises, and to increase the accuracy of AI algorithms to treat diabetes?*

The two main categories into which the examined studies were grouped are as follows: i) those with a special interest in examining how exercise affects glucose control ($n = 18$); ii) those who have integrated exercise into the overall diabetes care plan ($n = 19$).

In Table 1 a full analysis of all the selected articles is reported.

3.1 Devices

Wearable sensors may be worn in different parts on the body and come in a variety of shapes and sizes. At the moment, physiological data including skin temperature (ST), electrochemical skin conductance (ESC), heart rate (HR), respiratory rate, oxygen saturation (SpO₂), and galvanic skin response (GSR) are monitored by wearables. The latest devices include electrocardiogram (ECG) monitoring, which provides comprehensive data regarding characteristics of the heart condition, such as heart rate variability (HRV). Additionally, accelerometers are frequently employed for movement analysis, measuring acceleration forces to track physical activity and gestures.

Upon reviewing various articles, it becomes evident that the majority of wearable devices discussed are either commercial smartwatches or chestbands. These devices dominate the market due to their accessibility, convenience, and integration with other smart technologies. The most used is Empatica E4 ($n = 8$). It is a wearable device that collects continuous and instantaneous physiological data through its four sensors: temperature sensor, accelerometer, EDA and PPG sensors. Among the commercial ones, there is also the FitBit ($n = 3$) which offers a comprehensive suite of features designed to help users monitor their daily activity, exercise, sleep, and overall health (SpO₂ tracking, ECG, and skin

Table 1. Selected articles and the extracted information

Application	Devices	Algorithm	Type of Diabetes	Variables	Paper
Physical activity recognition	SenseWear Pro Empatica E4 Polar RS800CX Zephyr BioHarness3, Fitmate Metabolic Pro Unite Verily study watch Empatica E4, Cosmed k5, Bioplux - Empatica E4, Cosmed Omnia k5 ActiGraph wGT3X-BT, Polar Fitbit Charge HR, Microsoft Band 2 triaxial activPAL3 accelerometer sweat patch, self-made band	Classification and regression algorithm Random forest, threshold algorithm Kalman filter KNN Random forest PLS-DA, LSTM Classification and regression algorithm SVM, NB, DT, NN, LSTM PCA-based method Linear regression Multitask LSTM custom model Multitask RNN-LSTM RPBSID RNN-LSTM PLGS Kalman filter	T1D, T2D T1D T1D T1D T1D T1D T1D T1D T1D, T2D - T1D T1D T1D T1D T1D T1D T1D T1D	ST, GSR, Body motion, heat flux ACC, BVP, GSR, ST HR HR, VO2 ACC, HR ACC, BVP, GSR, ST, SpO2, HR, MO2 ECG, ACC ACC, BVP, GSR, ST, HR ACC, HR HR, GSR, METS, HR, ST, Steps ACC Sweat, HR, SpO2, Motion ACC, BVP, GSR, ST, SpO2, HR, MO2 ACC, BVP, GSR, ST ACC, BVP, GSR, ST HR, ACC HR, ACC	[33] [7] [6] [39] [8] [10] [32] [9] [23] [13] [19] [1] [31] [11] [36] [35]
Glucose Monitoring	SenseWear Mi Band 2, Mi smart scale, CareSens, Omron Self made device Pedometer Biosensors MAZ30100, GROVE GSR sen00183 Empatica E4 Zephyr Biopatch SenseWear Pro3 Polar M-600 SenseWear Pro3 Garmin Vivoactive 4s, Empatica E4 Riversong wave O2 colored Empatica E4, Basis Peak FitBitAlta HR wristband SenseWear FitBit	SVR with Gaussian function LSTM NB, RF, SMO, ZeroR Random Tree AlexNet Custom NN ARISES model Glucose mathematical model PBSD LSTM Armax model Decision Tree RF, SVR, MLP, Fuzzy Logic Bidirectional RNN MLP, SVM PLS RFPR, MLP	T1D T1D - - - H T1D T1D T1D T1D T1D T1D T1D T1D T1D T1D T1D T1D T1D TD	ST, GSR, Body motion, heat flux HR, BG, BP ST and steps ST and steps HR GSR, BVP ACC, BVP, GSR, ST ACC, HR ST, GSR, Body motion, heat flux HR ST, GSR, Body motion, heat flux HR, GSR BP, HR, SpO2, Body Temperature, Sweat ACC, BVP, GSR, ST HR ST, GSR, Body motion, heat flux HR, Calories, Steps	[16] [3] [29] [28] [34] [20] [42] [21] [17] [22] [37] [24] [2] [41] [5] [38] [40]

temperature tracking). Another widespread device is the SenseWear bracelet ($n=5$), developed by BodyMedia. They are advanced wearable sensors designed for comprehensive physiological monitoring and activity tracking (heart rate, heat flux, galvanic skin response, skin temperature). There is also a wide use of the Zephyr BioHarness band since it still is a gold standard for this kind of acquisition ($n=4$). In addition to this, there has been significant use of other devices designed to track various parameters like VO₂ max, energy expenditure, and metabolic rate. These devices provide comprehensive insights into an individual's physical performance and health status.

3.2 Artificial Intelligence Integration

One significant use of AI in the collected articles is in the analysis and improvement of blood glucose prediction. By leveraging machine learning and deep learning algorithms and large datasets, AI can predict blood glucose levels more accurately, helping individuals manage diabetes more effectively. Additionally, AI is utilized for the classification and identification of physical activity. Advanced algorithms analyze data from wearable devices and sensors to distinguish between different types of activities, such as walking, running, cycling, and resting.

Among the various machine learning algorithms, some of the most widely used are Random Forest ($n=4$), Naive Bayes ($n=2$), SVM ($n=3$) and KNN ($n=2$). Random Forest is a versatile ensemble method that constructs multiple decision trees, enhancing accuracy without overfitting. Naive Bayes assumes pre-

dicator independence, effective for large datasets. SVM excels in high-dimensional data, optimal for classification, regression, and outlier detection.

Among deep learning algorithms, LSTM and its variations ($n = 7$) is widely utilized. LSTM, designed to overcome the vanishing gradient problem in RNNs, excels in sequential data tasks such as speech recognition and natural language processing. Its variants, like Bidirectional LSTM and GRU (Gated Recurrent Unit), enhance performance in specific contexts. Their ability to retain information over time makes them pivotal in applications requiring context awareness and temporal dependencies.

There are also instances where data collected from sensors are used not to train AI models, but rather to validate mathematical models ($n = 5$). These datasets serve to refine theoretical frameworks and enhance predictive accuracy in fields such as physics, engineering, and environmental science.

3.3 Measured Variables

Data from numerous studies in this survey demonstrated that various physiological parameters are associated with aspects of glycemic control, particularly hypoglycemia. Furthermore, physical activity plays a crucial role in influencing these physiological parameters, as it can significantly affect glucose levels and overall metabolic health.

The measurement of HR is one of the most widespread parameters in all the papers ($n = 19$). It is a critical indicator of cardiovascular health and physical fitness. It provides insights into the heart's condition and the body's response to various stimuli, including stress and physical exertion. Monitoring heart rate allows for the assessment of heart rate variability (HRV), which is a key indicator of autonomic nervous system function. Moreover, accelerometers are widely used in this field ($n = 14$). They measure acceleration forces in multiple directions (usually along the x, y, and z axes). This data is crucial for tracking physical activity, movement patterns, and posture. It enables the assessment of daily activity levels, detection of falls, and analysis of gait. The last most widespread variable is the GSR ($n = 16$). It measures the electrical conductance of the skin, which varies with its moisture level. This parameter is closely linked to emotional and stress responses, as the sweat glands are controlled by the sympathetic nervous system. Changes in GSR provide insights into psychological or physiological arousal, making it a valuable indicator of stress, emotional states, and overall well-being.

Recent advancements in technology have led to the development of new devices capable of acquiring additional biometric signals, expanding the scope of physiological monitoring. One of the significant advancements is the introduction of sudorimeters. These devices are designed to measure sweat rate and composition more accurately. Sudorimeters provide detailed information about sweat gland activity, which can be used to infer hydration status, and electrolyte balance, and even detect certain medical conditions [19, 34].

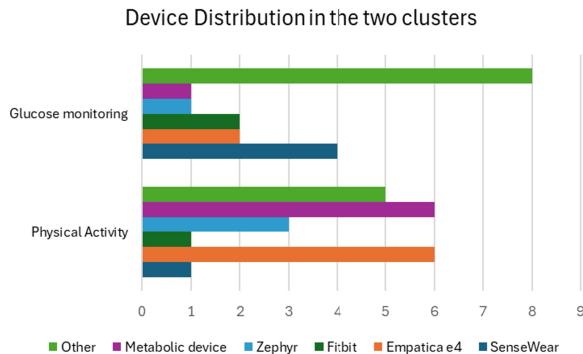


Fig. 3. Devices distribution between the clusters.

3.4 Cross Sectional Analysis

We conducted a cross-sectional analysis to understand the relationships between AI models, application domains, devices, and the variables acquired. In the following sections, we will analyze the results of this analysis in detail.

There is a wide variety of devices for the physical activity tracking cluster, some bulky as they are designed for lab testing purposes. In contrast, for glucose monitoring, smaller and more personalized devices (e.g., “other”) enable daily usability and integration with existing systems. This difference highlights the adaptability and convenience offered by the smaller devices in everyday scenarios compared to the bulkier ones intended primarily for controlled environments (see Fig. 3).

Analyzing the AI models in the two clusters, which can be appreciated in Fig. 4, in the physical activity tracking cluster, ML and supervised techniques have been frequently employed, akin to the use of situation-specific devices in lab settings. In contrast, for glucose monitoring, due to its broader scope, DL algorithms have been chosen for their ability to identify hidden features within

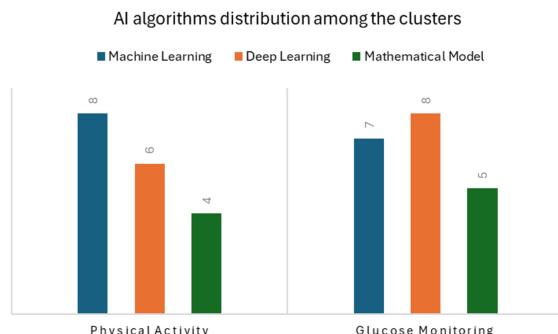


Fig. 4. Distribution of AI models between the clusters.

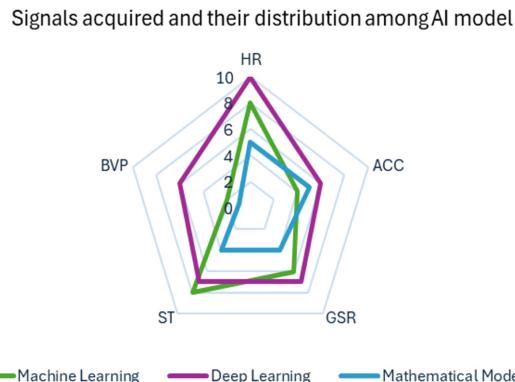


Fig. 5. AI application and collected variables.

signals. This approach allows for more comprehensive analysis and detection capabilities, catering to the complex nature of glucose monitoring beyond controlled environments.

In Fig. 5, it can be noted that HR is widely utilized in both DL and ML frameworks due to its presence in various devices and its derivation from multiple signals. ST, being a relatively stable and point-specific metric, is predominantly used in ML applications. Conversely, metrics like ACC, BVP, and GSR find extensive application in DL due to their variability over time, requiring sophisticated pattern recognition algorithms for analysis. These distinctions reflect the adaptability of different metrics across ML and DL methodologies based on their inherent characteristics and variability.

3.5 Future Challenges

The intricate relationships between these biomarkers and glucose regulation present a challenge. Further research is needed to develop models and simulations, design treatment strategies incorporating new inputs, and conduct additional clinical trials to demonstrate the methods' enhanced clinical impact. Moreover, wearable data is typically noisier, often contaminated by motion artefacts, and generally less accurate. Consequently, analyzing and interpreting wearable data poses unique challenges that require advanced algorithms and robust validation methods to ensure its usefulness in clinical and health monitoring applications. Advanced data processing techniques must be created to extract information from the data gathered by wearable sensors to fully fulfil the opportunity of wearables. Additionally, this can help AI models that need to be highly precise and accurate. Second, to lessen the number of devices on the body and the previously noted faults in the collecting procedure, it would be useful to include some of the above sensors in the CGM or the insulin pump.

Looking ahead, there's a growing push to incorporate stress monitoring into diabetes management, as stress significantly impacts blood glucose levels. Mod-

ern tools like wearable sensors and mobile apps could detect stress markers, offering holistic insights for personalized diabetes care. Integrating stress data with glucose trends may unveil new correlations, aiding in proactive interventions and enhancing overall health outcomes for individuals managing diabetes.

4 Conclusion

Wearable devices hold promise for diabetes treatment by utilizing physiological signals from physical activity. Yet, exercise alters glucose dynamics, complicating blood sugar regulation. The increasing integration of embedded artificial intelligence systems in these devices has revolutionized the ability to analyze physiological data in real-time.

In line with the emphasis on personalization, there is a growing preference for using unsupervised AI algorithms over supervised ones in this application. Unsupervised algorithms excel in identifying patterns and anomalies in data without the need for extensive labelled datasets. This capability is particularly beneficial for diabetes management, where patient data can be highly variable and individualized. Moreover, there is a growing use of both commercial and custom wearable devices. Custom devices, in particular, can be tailored to better fit individual patient needs, enhancing the move towards person-based therapy.

The combination of wearables, CGM, and AI could lead to a significant advancement in fully automated or closed-loop glycemic control systems. These advanced systems can continuously monitor glucose levels, predict future fluctuations, and automatically adjust insulin delivery without the need for manual intervention.

Abbreviation

In this section, there is a list of all the used abbreviations of this paper.

Full Name	Abbreviation	Full Name	Abbreviation
Accelerometer	ACC	Naive Bayes	NB
Artificial Intelligence	AI	Neural Network	NN
Blood Volume Pulse	BVP	Non-invasive Continuous Glucose Monitoring	NI-CGM
Continuous Glucose Monitoring	CGM	Partial least squares-discriminant analysis	PLS-DA
Decision Tree	DT	Principal Component Analysis	PCA
Galvanic Skin Response	GSR	Predictor Based Subspace Identification	PBSID
Glycated Haemoglobin	HbA1c	Random Forest	RF
Heart Rate	HR	Recurrent Neural Network	RNN
K-Nearest Neighborhood	KNN	Sequential Minimal Optimization	SMO
Long Short-Term Memory	LSTM	Skin Temperature	ST
Multi-Layer Perceptron	MLP	Support Vector Machine	SVM
Type 1 Diabetes	T1DM	Support Vector Regression	SVR

Acknowledgment. This work has been carried out within the project Italian National Recovery and Resilience Plan (NRRP) of NextGenerationEU, partnership on “Telecommunications of the Future” (PE00000001 – CUP F83C22001690001), project “RESearch and innovation on future Telecommunications systems and networks, to make Italy more smART” (RESTART).

References

1. Abdel-Latif, M., et al.: Multi-task classification of physical activity and acute psychological stress for advanced diabetes treatment. *Signals* **4**(1), 167–192 (2023)
2. Ahmed, A., Aziz, S., Qidwai, U., Abd-Alrazaq, A., Sheikh, J.: Performance of artificial intelligence models in estimating blood glucose level among diabetic patients using non-invasive wearable device data. *Comput. Methods Programs Biomed. Update* **3**, 100094 (2023)
3. Alfian, G., Syafrudin, M., Ijaz, M.F., Syaekhoni, M.A., Fitriyani, N.L., Rhee, J.: A personalized healthcare monitoring system for diabetic patients by utilizing BLE-based sensors and real-time data processing. *Sensors* **18**(7), 2183 (2018)
4. Askari, M.R., Abdel-Latif, M., Rashid, M., Sevil, M., Cinar, A.: Detection and classification of unannounced physical activities and acute psychological stress events for interventions in diabetes treatment. *Algorithms* **15**(10), 352 (2022)
5. Bertachi, A., et al.: Prediction of nocturnal hypoglycemia in adults with type 1 diabetes under multiple daily injections using continuous glucose monitoring and physical activity monitor. *Sensors* **20**(6), 1705 (2020)
6. Breton, M.D., et al.: Adding heart rate signal to a control-to-range artificial pancreas system improves the protection against hypoglycemia during exercise in type 1 diabetes. *Diab. Technol. Ther.* **16**(8), 506–511 (2014)
7. Cescon, M., et al.: Activity detection and classification from wristband accelerometer data collected on people with type 1 diabetes in free-living conditions. *Comput. Biol. Med.* **135**, 104633 (2021)
8. Cho, S., et al.: Design of a real-time physical activity detection and classification framework for individuals with type 1 diabetes. *J. Diab. Sci. Technol.* 19322968231153896 (2023). <https://doi.org/10.1177/19322968231153896>, epub ahead of print
9. Dasanayake, I.S., et al.: Early detection of physical activity for people with type 1 diabetes mellitus. *J. Diabetes Sci. Technol.* **9**(6), 1236–1245 (2015)
10. Dave, D., et al.: Detection of hypoglycemia and hyperglycemia using noninvasive wearable sensors: electrocardiograms and accelerometry. *J. Diabetes Sci. Technol.* **18**(2), 351–362 (2024)
11. Dénes-Fazakas, L., et al.: Physical activity detection for diabetes mellitus patients using recurrent neural networks. *Sensors* **24**(8), 2412 (2024)
12. Ding, S., Schumacher, M.: Sensor monitoring of physical activity to improve glucose management in diabetic patients: a review. *Sensors* **16**(4) (2016). <https://doi.org/10.3390/s16040589>. <https://www.mdpi.com/1424-8220/16/4/589>
13. van Doorn, W.P., et al.: Machine learning-based glucose prediction with use of continuous glucose and physical activity monitoring data: The maastricht study. *PLoS ONE* **16**(6), e0253125 (2021)
14. Ellahham, S.: Artificial intelligence: the future for diabetes care. *Am. J. Med.* **133**(8), 895–900 (2020)
15. Fagherazzi, G., Ravaud, P.: Digital diabetes: perspectives for diabetes prevention, management and research. *Diabetes Metabolism* **45**(4), 322–329 (2019)

16. Georga, E.I., Protopappas, V.C., Ardigo, D., Polyzos, D., Fotiadis, D.I.: A glucose model based on support vector regression for the prediction of hypoglycemic events under free-living conditions. *Diabetes Technol. Ther.* **15**(8), 634–643 (2013)
17. Hajizadeh, I., et al.: Incorporating unannounced meals and exercise in adaptive learning of personalized models for multivariable artificial pancreas systems. *J. Diabetes Sci. Technol.* **12**(5), 953–966 (2018)
18. Hermanns, N., Ehrmann, D., Shapira, A., Kulzer, B., Schmitt, A., Laffel, L.: Coordination of glucose monitoring, self-care behaviour and mental health: achieving precision monitoring in diabetes. *Diabetologia* **65**(11), 1883–1894 (2022)
19. Hong, Y.J., et al.: Multifunctional wearable system that integrates sweat-based sensing and vital-sign monitoring to estimate pre-/post-exercise glucose levels. *Adv. Func. Mater.* **28**(47), 1805754 (2018)
20. Islam, M.M., Manjur, S.M.: Design and implementation of a wearable system for non-invasive glucose level monitoring. In: 2019 IEEE International Conference on Biomedical Engineering, Computer and iNformation Technology for Health (BECITHCON), pp. 29–32. IEEE (2019)
21. Jacobs, P.G., et al.: Incorporating an exercise detection, grading, and hormone dosing algorithm into the artificial pancreas using accelerometry and heart rate. *J. Diabetes Sci. Technol.* **9**(6), 1175–1184 (2015)
22. Jacobs, P.G., et al.: Integrating metabolic expenditure information from wearable fitness sensors into an AI-augmented automated insulin delivery system: a randomised clinical trial. *Lancet Digit. Health* **5**(9), e607–e617 (2023)
23. Laguna Sanz, A.J., Díez, J.L., Giménez, M., Bondia, J.: Enhanced accuracy of continuous glucose monitoring during exercise through physical activity tracking integration. *Sensors* **19**(17), 3757 (2019)
24. Lehmann, V., et al.: Noninvasive hypoglycemia detection in people with diabetes using smartwatch data. *Diabetes Care* **46**(5), 993 (2023)
25. Lipponen, J.A., et al.: Hypoglycemia detection based on cardiac repolarization features. In: 2011 Annual International Conference of the IEEE Engineering in Medicine and Biology Society, pp. 4697–4700. IEEE (2011)
26. Nguyen, L.L., Su, S., Nguyen, H.T.: Identification of hypoglycemia and hyperglycemia in type 1 diabetic patients using ECG parameters. In: 2012 Annual International Conference of the IEEE Engineering in Medicine and Biology Society, pp. 2716–2719. IEEE (2012)
27. Page, M.J., et al.: The Prisma 2020 statement: an updated guideline for reporting systematic reviews. *Int. J. Surg.* **88**, 105906 (2021)
28. Rghioui, A., Lloret, J., Harane, M., Oumnad, A.: A smart glucose monitoring system for diabetic patient. *Electronics* **9**(4), 678 (2020)
29. Rghioui, A., Lloret, J., Sendra, S., Oumnad, A.: A smart architecture for diabetic patient monitoring using machine learning algorithms. In: *Healthcare*, vol. 8, p. 348. MDPI (2020)
30. Rodriguez-León, C., Villalonga, C., Muñoz-Torres, M., Ruiz, J.R., Baños, O.: Mobile and wearable technology for the monitoring of diabetes-related parameters: systematic review. *JMIR Mhealth Uhealth* **9**(6), e25138 (2021)
31. Sevil, M., Rashid, M., Hajizadeh, I., Park, M., Quinn, L., Cinar, A.: Physical activity and psychological stress detection and assessment of their effects on glucose concentration predictions in diabetes management. *IEEE Trans. Biomed. Eng.* **68**(7), 2251–2260 (2021)
32. Sevil, M., et al.: Determining physical activity characteristics from wristband data for use in automated insulin delivery systems. *IEEE Sens. J.* **20**(21), 12859–12870 (2020)

33. Sobel, S.I., Chomentowski, P.J., Vyas, N., Andre, D., Toledo, F.G.: Accuracy of a novel noninvasive multisensor technology to estimate glucose in diabetic subjects during dynamic conditions. *J. Diabetes Sci. Technol.* **8**(1), 54–63 (2014)
34. Srinivasu, P.N., JayaLakshmi, G., Jhaveri, R.H., Praveen, S.P.: Ambient assistive living for monitoring the physical activity of diabetic adults through body area networks. *Mob. Inf. Syst.* **2022**(1), 3169927 (2022)
35. Stenerson, M., Cameron, F., Payne, S., et al.: The impact of accelerometer use in exercise-associated hypoglycemia prevention in type 1 diabetes [published online ahead of print September 17, 2014]. *J. Diabetes Sci. Technol.*
36. Stenerson, M., et al.: The impact of accelerometer and heart rate data on hypoglycemia mitigation in type 1 diabetes. *J. Diabetes Sci. Technol.* **8**(1), 64–69 (2014)
37. Turksoy, K., Bayrak, E.S., Quinn, L., Littlejohn, E., Cinar, A.: Multivariable adaptive closed-loop control of an artificial pancreas without meal and activity announcement. *Diabetes Technol. Ther.* **15**(5), 386–400 (2013)
38. Turksoy, K., Monforti, C., Park, M., Griffith, G., Quinn, L., Cinar, A.: Use of wearable sensors and biometric variables in an artificial pancreas system. *Sensors* **17**(3) (2017). <https://doi.org/10.3390/s17030532>. <https://www.mdpi.com/1424-8220/17/3/532>
39. Turksoy, K., et al.: Classification of physical activity: information to artificial pancreas control systems in real time. *J. Diabetes Sci. Technol.* **9**(6), 1200–1207 (2015)
40. Vahedi, M.R., et al.: Predicting glucose levels in patients with type1 diabetes based on physiological and activity data. In: Proceedings of the 8th ACM MobiHoc 2018 Workshop on Pervasive Wireless Healthcare Workshop (2018)
41. Zhu, T., Li, K., Herrero, P., Georgiou, P.: Personalized blood glucose prediction for type 1 diabetes using evidential deep learning and meta-learning. *IEEE Trans. Biomed. Eng.* **70**(1), 193–204 (2022)
42. Zhu, T., Uduku, C., Li, K., Herrero, P., Oliver, N., Georgiou, P.: Enhancing self-management in type 1 diabetes with wearables and deep learning. *NPJ Digit. Med.* **5**(1), 78 (2022)



Analysis of Non-linearity Sources in Piezoresistive Gyroscopic Systems

Gabriele Laita¹ , Andrea Buffoli^{1,2} , and Giacomo Langfelder¹

¹ Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano,
Milan, Italy

gabriele.laita@polimi.it

² CEA-Leti, Univ. Grenoble Alpes, 38000 Grenoble, France

Abstract. Gyroscopes, essential in numerous navigation and stabilization tasks, are highly valued for their precision and reliability. However, achieving optimal accuracy remains a significant challenge, also due to inherent non-linearities. This study focuses on identifying sources of non-linearity in NEMS-based piezoresistive MEMS gyroscopes. A comprehensive Simulink model was developed and simulated to represent the entire gyroscope system, and the results were compared with experimental data. The model identified contributions from the AQC circuit and the Wheatstone bridge, but these did not align with experimental findings. Our investigation suggests that the dominant non-linearity contribution may be due to the CFIA or the piezoresistive effect, which will be thoroughly analyzed in future works.

Keywords: Gyroscopes · Piezoresistivity · Non linearity sources

1 Introduction

Micro-Electro-Mechanical Systems (MEMS) gyroscopes have become integral components in a wide range of modern applications, ranging from consumer electronics to advanced aerospace systems [1]. These miniaturized devices are prized for their ability to measure angular velocity with high precision and reliability, making them essential for navigation, stabilization, and control systems.

MEMS gyroscopes operate on principles of vibrating structures, where Coriolis forces generated by rotation cause measurable displacements. This motion is typically detected using capacitive, piezoelectric, or piezoresistive sensing methods. At the state of the art, the most impressive results were achieved by using:

- large-area devices with specialized packages and accurate calibration algorithms (Challoner in [2] (Boeing gyroscope), Endean in [3] (Honeywell gyroscope), Koenig in [4] (Northrop Grumman gyroscope));
- 3D processes (as demonstrated by Singh in [5]);
- the Nuclear Magnetic Resonance (NMR) (Walker in [6]);

- Nano-Electro-Mechanical systems (NEMS) based piezoresistive MEMS gyroscopes, which demonstrated unprecedented performance with a 1.3-mm² die size (Gadola in [7]).

Despite their advantages, achieving optimal accuracy with MEMS gyroscopes remains challenging, also due to inherent non-linearities in their operation. These non-linearities can arise from various sources, including the mechanical structure of the gyroscope, the sensing elements, and the associated signal processing circuits. Understanding and mitigating these non-linearities is crucial for enhancing the performance and reliability of MEMS gyroscopes [8].

This paper aims to explore sources of non-linearity in NEMS-based piezoresistive MEMS gyroscopes. By developing and simulating a comprehensive Simulink model and comparing it with experimental measurements, we seek to identify non-linearity sources and compare them with experimental results. Section 2 will describe the device and the system used to evaluate the non-linearity error of the gyroscope and the experimental findings. Section 3 will discuss the investigated sources of non-linearity and the discrepancies observed with respect to the experimental measurements. Finally, Sect. 4 will present the conclusions of this work and provide guidelines for future research.

2 System Description and Measurements

2.1 1.3-mm² NEMS-Based Piezoresistive MEMS Gyroscope

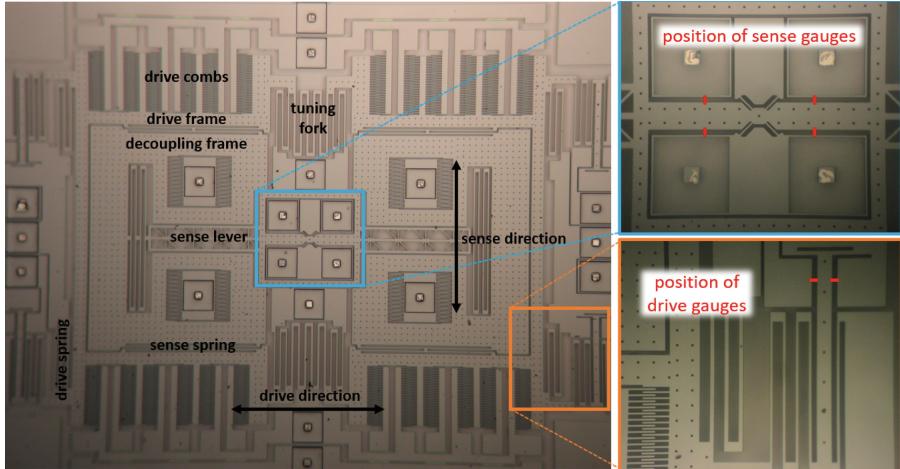


Fig. 1. SEM image of a NEMS-based piezoresistive MEMS gyroscope.

The gyroscope (shown in Fig. 1) is fabricated using the M&NEMS process by CEA-LETI [9], featuring a 20 μm thick MEMS structural layer and a 250 nm

NEMS layer for piezoresistive sensing with high stress concentration. The device has a total footprint of $1.45 \times 0.91\text{ mm}^2$. This sensor operates through amplitude-modulated energy transfer between drive and sense modes at frequencies around 25 kHz via Coriolis coupling. The piezoresistive sensing allows for ultra-low noise performance even in mode-split configuration, with a nominal frequency difference of a few hundred Hz between the drive and sense modes. Drive forcing is achieved through a push-pull, comb-finger electrostatic actuation, while NEMS piezoresistive readout is used for both drive and sense motions. The doubly decoupled structure includes a drive frame, a Coriolis decoupling frame with specific electrodes for electromechanical quadrature compensation, and a sense lever. During operation, the displacement for drive oscillation is set to 9 μm . The decoupling mass, rigidly connected to the drive frame, is sensitive to Coriolis acceleration when an angular rate is present, causing displacement along the sense mode. Both drive and sense motions are transferred to piezoresistive NEMS gauges through appropriately sized lever systems, and both these signals are then read by a dedicated analog front-end through a half Wheatstone bridge configuration.

2.2 Analog Front-End

The ASIC is manufactured using the HCMOS9LP technology by STMicroelectronics. For the analog circuits, transistors with a thick oxide layer are used. These transistors have a minimum channel length of 0.35 μm and can handle a maximum voltage of 3.6 V. This allows them to support a wide dynamic range with high sensitivity.

The IC incorporates the standard blocks of an amplitude modulated (AM) gyroscope, but these have been modified for NEMS gauge-based devices and optimized for stability. The blocks include:

- The drive loop, required to maintain the oscillation along the drive axis from the NEMS piezoresistive frontend to the push-pull actuation and to provide the two demodulation references;
- The automatic gain control loop (AGC), regulating and stabilizing the amplitude of the drive oscillation through a reference voltage (V_{ref});
- The sense chain, adopting the same NEMS piezoresistive front-end as the drive readout to minimize the demodulation phase error and maximize stability [10];
- A bandgap current reference, needed to provide biasing to the active stages and optimized for optimal stability against temperature changes;
- 2 indirect current-feedback instrumentation amplifiers (CFIA), acting as the amplifier of the signal coming from the Wheatstone bridges, coupled with dedicated offset compensation circuits (whose working principle is shown in [11, 12]).

The reader can find more details about the device and the analog front-end in [13].

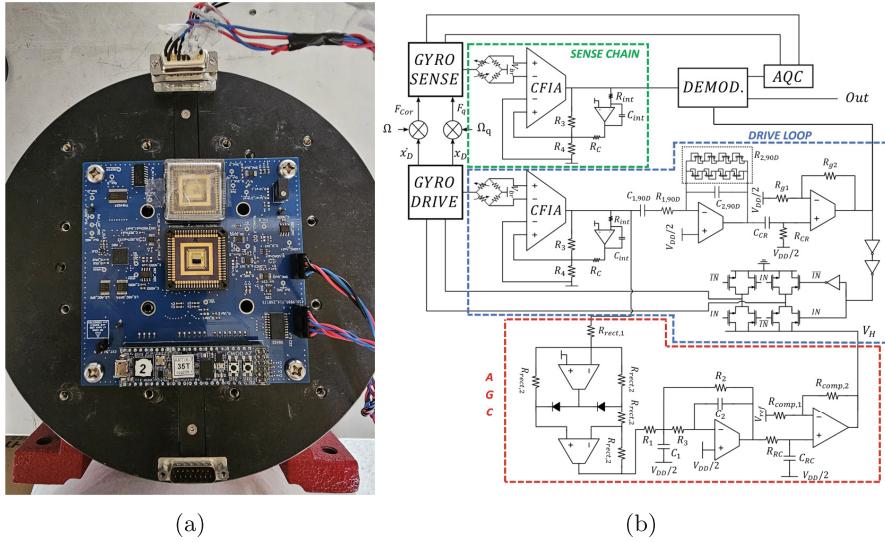


Fig. 2. a) Complete measurement setup; b) System schematization.

2.3 Complete System

The complete system is schematically depicted in Fig. 2, where the CFIA are represented as 4-input blocks. Unlike most integrated drive-loop designs, it is noteworthy that the front-end output here is single-ended rather than differential, requiring the loop to be designed accordingly. The digital demodulation and the automatic quadrature compensation (AQC) loop are implemented via FPGA. The reader can find more details about the used system in [14].

2.4 Experimental Non-Linearity Measurements

The measurements are conducted by placing the system on the Acutronics 1120S, a single-axis rate table, as presented in Fig. 2a. The rate table is programmed to perform symmetric ramps, with peak values of ± 1000 dps, at a frequency of 100 mHz. The signal coming from the analog front-end is elaborated and then sent to the PC via RS-422. After data acquisition, the collected data (like the ones shown in Fig. 3) are processed and analyzed using MATLAB. Specifically, the analysis involves filtering the data to remove white noise and isolating the positive ramps. These positive ramps are then cut (to avoid possible non-linearities introduced by the rate table reaching the peak angle rate and then decelerating) and averaged to create a single representative curve. The non-linearity of this averaged curve is subsequently evaluated creating a linearized version of this curve exploiting the data around 0 dps, whose coefficients are obtained through a least-square method.

The results present a less-than linear experimental curve, like the one shown in Fig. 4a. The relative error of this non-linearity is evaluated as:

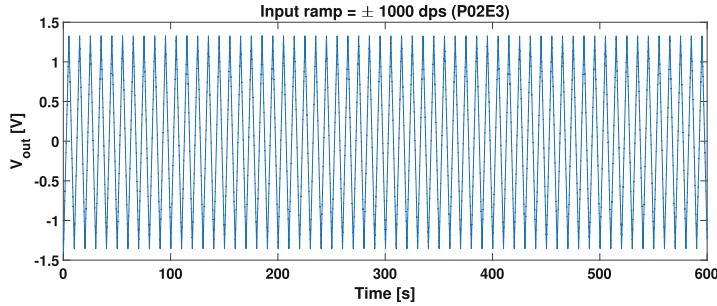


Fig. 3. Captured data with a full cycle of 10 min.

$$rel_{err} = \frac{ramp_{aver} - ramp_{lin}}{\max(ramp_{aver})} * 100 \quad (1)$$

Fitting the curve presented in Fig. 4b with a least-squares method, we observe this error presents a cubic trend, which might hint at which its origin is.

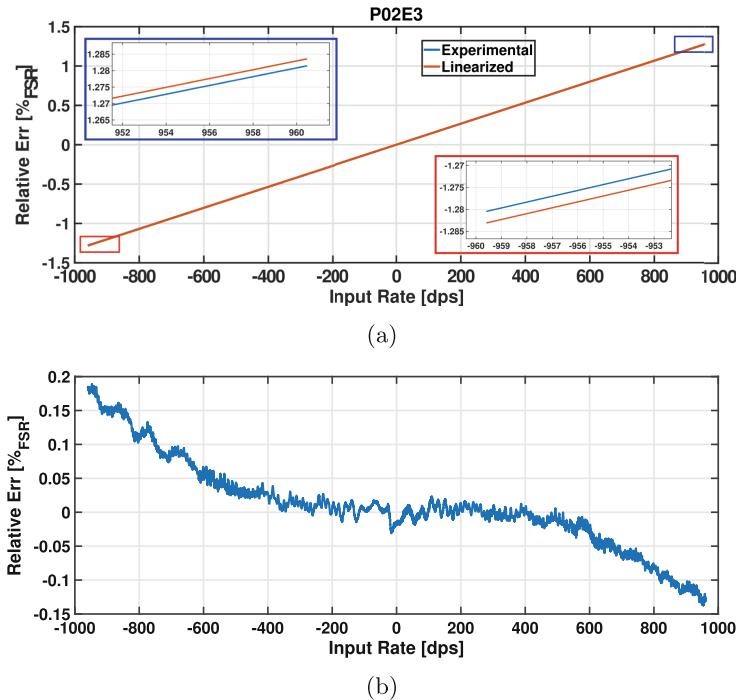


Fig. 4. a) Post-processed data vs linearized curve; b) Evaluated relative NL error

3 Investigated Non-linearity Sources

To assess the impact of non-linearity sources within this system, a comprehensive Simulink model (presented in Fig. 5) was developed to simulate the entire gyroscope system. This setup allows us to switch between the real version of various blocks and a linearized approximation, facilitating a clearer evaluation of the impact of each individual source.

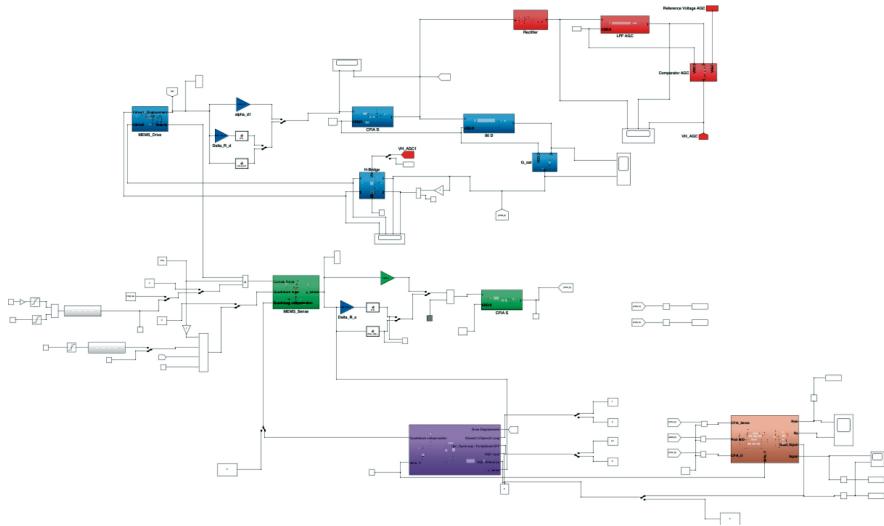


Fig. 5. Simulink model of the gyroscope system

3.1 Wheatstone Bridge and Offsets

As outlined in Sect. 2.1, the nano-gauges are arranged in a half Wheatstone bridge (WB) configuration (illustrated in Fig. 6a) to measure the piezoresistive effect. The lever mechanism compresses one gauge while elongating its symmetric counterpart, generating a differential signal. Assuming all resistances have the same nominal value, the output signal from the WB is:

$$\frac{V_{out}}{V_{br}} = \frac{R + \Delta R}{2R + \Delta R} - \frac{R - \Delta R}{2R - \Delta R} = \frac{2R\Delta R}{4R^2 - \Delta R^2} \quad (2)$$

From Eq. 2, we see that the output signal does not vary linearly with the resistance change. By expanding this formula using Taylor series, we obtain:

$$\frac{2R\Delta R}{4R^2 - \Delta R^2} \approx \frac{\Delta R}{2R} \left(1 + \left(\frac{\Delta R}{2R} \right)^2 + \dots \right) \quad (3)$$

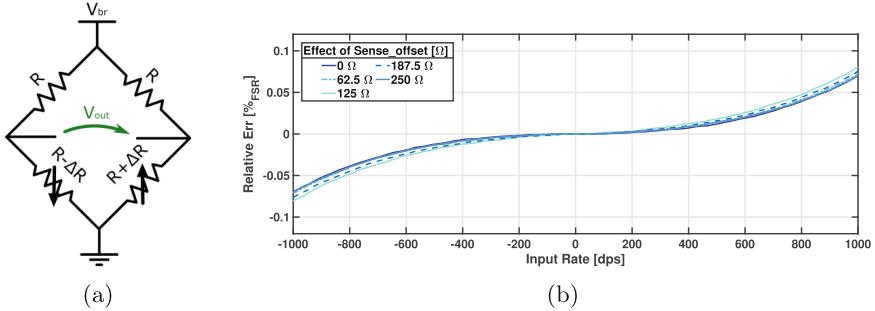


Fig. 6. a) Wheatstone bridge schematization; b) Simulated relative error

Indeed, there is a cubic trend linked to this nonlinearity, as confirmed by the Simulink model. However, the resulting curve appears more than linear, which does not match the experimental measurements. Furthermore, also the possible presence of offsets in the bridge has been considered, but as we can see in Fig. 6, their impact is quite limited.

This discrepancy suggests the presence of other nonlinear contributions with an opposite trend, thus compensating for the nonlinearity of the WB.

3.2 AQC Circuit and Quadrature Values

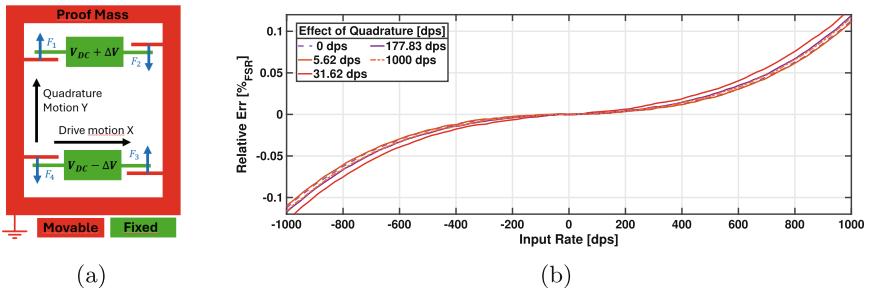


Fig. 7. a) Tatar quadrature electrodes schematization; b) Simulated relative error

The AQC circuit is designed to compensate the quadrature error [15], a significant non-ideality in MEMS gyroscopes. To achieve this, dedicated electrodes are strategically positioned within the Coriolis mass following the scheme presented by Tatar in [16]. These electrodes complete a feedback loop capable of assessing the impact of quadrature error and applying corrective forces to counteract it. This compensation mechanism ensures improved accuracy and performance of the gyroscope. A schematic representation of this concept is provided in Fig. 7a.

The forces, acting on the Coriolis mass, are equal to:

$$F_1 = +\frac{\epsilon_0 h N_{comb} (L_{ov} + x)}{2(D_q - y)^2} (V_{DC} + \Delta V)^2 \quad (4)$$

$$F_2 = -\frac{\epsilon_0 h N_{comb} (L_{ov} - x)}{2(D_q + y)^2} (V_{DC} + \Delta V)^2 \quad (5)$$

$$F_3 = -\frac{\epsilon_0 h N_{comb} (L_{ov} + x)}{2(D_q + y)^2} (V_{DC} - \Delta V)^2 \quad (6)$$

$$F_4 = +\frac{\epsilon_0 h N_{comb} (L_{ov} - x)}{2(D_q - y)^2} (V_{DC} - \Delta V)^2 \quad (7)$$

where ϵ_0 is the vacuum permittivity, h is the thickness of the combs (which is the thickness of the entire MEMS structure), N_{comb} is the number of electrodes per structure (in Fig. 7a only one electrode is shown for clarity), L_{ov} is the nominal overlap between the electrodes, x is the drive displacement, D_q is the nominal gap between the electrodes, y is the sense displacement, V_{DC} is the bias voltage of the quadrature electrodes while ΔV is the voltage difference generated by the AQC to compensate the quadrature error.

Typically, being y much smaller than D_q , this term is ignored. This brings to a total force which is linear with x and independent from y . Instead, summing all the terms and expanding with Taylor series up to the third order, we obtain:

$$F_{tot} = 4 \frac{\epsilon_0 h N_{comb}}{D_q^2} \left(-x V_{DC} \Delta V + \frac{L_{ov} (V_{DC}^2 + \Delta V^2) y}{D_q} - 3 \frac{V_{DC} \Delta V x y^2}{D_q^2} + 3 \frac{L_{ov} (V_{DC}^2 + \Delta V^2) y^3}{D_q^3} \right) \quad (8)$$

A third order element following the same trend as the Wheatstone bridge is present (as shown in Fig. 7b). The contribution of different quadrature values has been evaluated, but this element proved to have a minor impact on the non-linearity of the system (as we can see in Fig. 7b). This suggests that even this contribution is overcome by other non-linearity sources, with a different trend, yet to be investigated.

4 Conclusion and Future Researches

As depicted in Sect. 3, different sources of non-linearity have been studied. Anyway, their contribution does not explain the experimentally observed non-linearity error. Our best guess is that other sources yet to be investigated are causing the measured non-linearity. The best candidates are:

- the non-linearity introduced by the CFIA approaching saturation;
- the non-linearity of the piezoresistive effect [17].

Future works will be dedicated to fully investigate these phenomena, trying to understand their role in the non-linearity of the system to finally implement a compensation of this error. Together with the ultra-low noise ($0.005^\circ/\sqrt{h}$) and stability ($0.015^\circ/h$) of this kind of gyroscopes, the assessment and correction of non-linearity will result in the best-in-class mm² gyroscope for navigation application.

References

1. Langfelder, G., Bestetti, M., Gadola, M.: Silicon MEMS inertial sensors evolution over a quarter century. *J. Micromech. Microeng.* **31**, 084002. <https://doi.org/10.1088/1361-6439/ac0fbf>
2. Challoner, A.D., Ge, H.H., Liu, J.Y.: Boeing disc resonator gyroscope. In: Proceedings of the IEEE/ION Position, Location and Navigation Symposium (PLANS), Monterey, CA, USA, May 2014, pp. 504–514. <https://doi.org/10.1109/PLANS.2014.6851410>
3. Endean, D., et al.: Near-navigation grade tuning fork MEMS gyroscope. In: Proceedings of the IEEE International Symposium on Inertial Sensors and Systems (INERTIAL), Naples, FL, USA, April 2019, pp. 1–4. <https://doi.org/10.1109/ISISS.2019.8739669>
4. Koenig, S., et al.: Towards a navigation grade Si-MEMS gyroscope. In: Proceedings of the DGON Inertial Sensors System (ISS), Braunschweig, Germany, September 2019, pp. 1–18. <https://doi.org/10.1109/ISS46986.2019.8943770>
5. Singh, S., Woo, J.K., He, G., Cho, J.Y., Najafi, K.: $0.0062^\circ/\sqrt{hr}$ angle random walk and $0.027^\circ/hr$ bias instability from a micro-shell resonator gyroscope with surface electrodes. In: 2020 IEEE 33rd International Conference on Micro Electro Mechanical Systems (MEMS), Vancouver, BC, Canada, pp. 737–740 (2020). <https://doi.org/10.1109/MEMS46641.2020.9056391>
6. Walker, T.G., Larsen, M.S.: Spin-exchange-pumped NMR gyros. In: Advances in Atomic, Molecular, and Optical Physics, vol. 65, pp. 373–401 (2016). <https://doi.org/10.1016/bs.aamop.2016.04.002>
7. Gadola, M., Buffoli, A., Sansa, M., Berthelot, A., Robert, P., Langfelder, G.: 1.3 mm² Nav-grade NEMS-based gyroscope. *J. Microelectromechanical Syst.* **30**(4), 513–520 (2021). <https://doi.org/10.1109/JMEMS.2021.3088940>
8. Tatar, E., et al.: Nonlinearity tuning and its effects on the performance of a MEMS gyroscope. In: 2015 Transducers - 2015 18th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS), Anchorage, AK, USA, pp. 1133–1136 (2015). <https://doi.org/10.1109/TRANSDUCERS.2015.7181127>
9. Dellea, S., et al.: In-plane and out-of-plane mems gyroscopes based on piezoresistive NEMS detection. *J. Microelectromech. Syst.* **24**(6), 1817–1826 (2015). <https://doi.org/10.1109/JMEMS.2015.2441142>
10. Gaffuri Pagani, L., et al.: Direct phase measurement and compensation to enhance mems gyroscopes zro stability. *J. Microelectromech. Syst.* **30**(5), 703–711 (2021). <https://doi.org/10.1109/JMEMS.2021.3096031>
11. Witte, J.F., Huijsing, J.H., Makinwa, K.A.A.: A Current-Feedback Instrumentation Amplifier with $5\mu V$ Offset for Bidirectional High-Side Current-Sensing.: IEEE International Solid-State Circuits Conference - Digest of Technical Papers. San Francisco, CA, USA **2008**, 74–596 (2008). <https://doi.org/10.1109/ISSCC.2008.4523063>

12. Ahmed, M., Mohamad, S., Bermak, A.: A power-efficient current-feedback instrumentation amplifier for precision bridge readout. In: 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Singapore, pp. 555–558 (2015). <https://doi.org/10.1109/EDSSC.2015.7285174>
13. Buffoli, A., Gadola, M., Sansa, M., Langfelder, G.: $0.02^\circ/\text{h}$, $0.004^\circ/\sqrt{\text{h}}$, 6.3-mA NEMS gyroscope with integrated circuit. *IEEE Trans. Instrum. Measur.* **72**, 1–8, Article no. 2002108 (2023). <https://doi.org/10.1109/TIM.2023.3244248>
14. Buffoli, A., Robert, P., Langfelder, G.: Upgrading a gyroscope from a lab-based setup into a pre-industrial demo: challenges and lessons learned. In: IEEE International Symposium on Inertial Sensors and Systems (INERTIAL), Hiroshima, Japan, pp. 1–4 (2024). <https://doi.org/10.1109/INERTIAL60399.2024.10502082>
15. Kempe, V.: Inertial MEMS: Principles and Practice. Cambridge University Press (2011)
16. Tatar, E., Alper, S.E., Akin, T.: Quadrature-error compensation and corresponding effects on the performance of fully decoupled MEMS gyroscopes. *J. Microelectromech. Syst.* **21**(3), 656–667 (2012). <https://doi.org/10.1109/JMEMS.2012.2189356>
17. Matsuda, K., Suzuki, K., Yamamura, K., Kanda, Y.: Nonlinear piezoresistance effects in silicon. *J. Appl. Phys.* **73**(4), 1838–1847 (1993). <https://doi.org/10.1063/1.353169>



Effect of Intrinsic Layer Thickness on the Performances of Amorphous Silicon P-I-N Junction

Nicola Lovecchio¹ , Silvia Casalinoovo¹ , Augusto Naselli² , Giampiero de Cesare¹ , and Domenico Caputo¹

¹ Department of Information Engineering, Electronics and Telecommunications, Sapienza University of Rome, Rome, Italy
nicola.lovecchio@uniroma1.it

² School of Aerospace Engineering, Sapienza University of Rome, Rome, Italy

Abstract. Hydrogenated amorphous silicon (a-Si:H) p-type/intrinsic/n-type junctions are widely used in thin film-based microelectronics. Recently, they have been investigated as photodiodes and temperature sensors integrated on a single glass substrate to develop lab-on-chip systems featuring compactness and lightweight. In such applications, a-Si:H photodiodes can detect chemiluminescence, bioluminescence or fluorescence. Depending on the wavelength to be revealed, the spectral response of the photosensor could be properly tuned. In the present work, we report on the fabrication and optoelectronic characterization of a-Si:H p-i-n junctions to study the effect of the intrinsic layer thickness on quantum efficiency and temperature sensitivity of the sensors. Results show that the photo-diode spectral response is highly affected by the i-layer thickness, while the temperature sensor performances do not show any significant dependence on it.

Keywords: hydrogenated amorphous silicon · thin film technology · photosensors · temperature sensors · quantum efficiency

1 Introduction

Hydrogenated amorphous silicon (a-Si:H) is a widely used material in thin film structures in different applications such photovoltaic/thermal systems [1] and active-matrix display [2]. Lab-on-chip (LoC) is another emerging research field [3–5], where a-Si:H materials find applications as photosensors and absorption filter [6], temperature sensors [7, 8] or plasmonic waveguide sensor [9].

One important LoC research topic is the development of technologies and integration process that can enable the path from “chip-in-a-lab” to “true lab-on-chip” [10, 11], where the limitation of using bulky equipment for thermal treatment and/or detection is overcome. Within this framework, we have already presented a compact optoelectronic platform, which integrates on a single glass substrate a-Si:H photosensors and temperature sensors, metallic thin film heaters and thin film interferential filter [12]. The a-Si:H devices are p-type/intrinsic/n-type stacked structure, where the intrinsic layer is the active

region of the photosensors, while the doped regions sustain the electric field inside the i-layer in order to collect the photogenerated carrier by drift. a-Si:H photosensors in lab-on-chip applications can detect chemiluminescence [13], bioluminescence [14] or fluorescence, phenomena that can produce luminescence in different spectral ranges. Considering the exponential decrease of the light intensity ruled by the Lambert-Beer's law in a material and the decrease of absorption coefficient with increasing wavelength, in this paper we report the effect of the i-layer thickness on the performances of the a-Si:H devices in order to verify the suitability to act as highly sensitive temperature sensors and at the same time as low-noise, highly sensitive and tunable photosensor.

2 a-Si:H Sensor Structure and Fabrication

By using standard microelectronic technology steps, we have fabricated 3 different arrays of sensors with thickness of the intrinsic layer equal to 0.4 μm , 1.2 μm and 2.5 μm . The fabrication steps are the following:

1. cleaning of the glass substrate by piranha solution and subsequent ultrasonic treatment in deionized water;
2. deposition by magnetron sputtering of a 100 nm-thick layer of Indium Tin Oxide (ITO) and patterning by UV-photolithography acting as the front transparent contact of the photodiode;
3. growth by Plasma Vapor Deposition of the a-Si:H layers. For all the three different intrinsic layer thicknesses, the p-doped and n-doped layer have been set to 10 nm and 50 nm, respectively;
4. deposition by vacuum evaporation of a Cr/Al/Cr stacked layer, acting as bottom contact of the photosensor;
5. patterning of the Cr/Al/Cr stack and a-Si:H layers by means of wet and dry etching, respectively, to delineate the photosensors' geometry;
6. deposition and patterning of a 5 μm -thick layer of SU-8 3005 (MicroChem, Westborough, MA, USA), which acts as passivation and insulation layer on the lateral walls of the diodes. The patterning step defines the via holes on the diodes;
7. deposition, by magnetron sputtering, of a 200 nm-thick TiW layer and subsequent patterning for contacting the bottom contact of the diodes through the via holes defined in step 6 and for the electrical connections to external pads.

To determine the deposition time for achieving the different thickness of the i-layer we have made a preliminary characterization of the PECVD system. We have found the deposition rate of 4 \AA/s , 1.9 \AA/s and 1.7 \AA/s for the p-doped, intrinsic and n-doped layer respectively. Starting from these values, we have estimated a deposition time of 35 min, 120 min and 240 min for achieving 0.4 μm , 1.2 μm and 2.5 μm respectively.

The schematic cross section of a single sensor and a picture of the fabricated array is reported in Fig. 1. Each array has 5×6 sensors, that have the same common top electrode (the comb-shaped geometry in the picture) and separated bottom contacts (not visible because are made in ITO). Each sensor has an active area of $2 \times 2 \text{ mm}^2$.

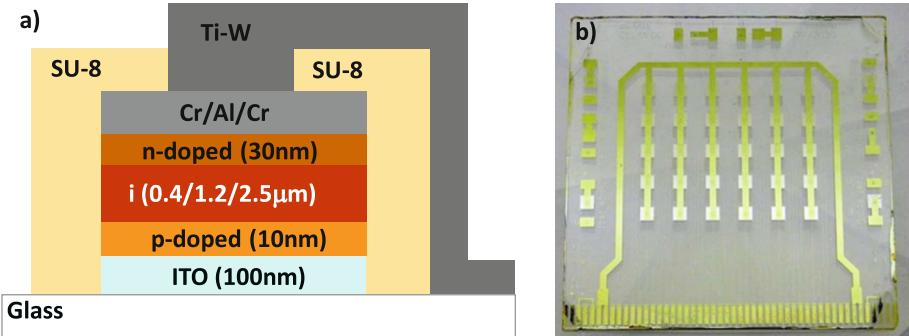


Fig. 1. Cross section (a) and picture of the array (b) of the a-Si:H sensors.

3 Results and Discussion

The a-Si:H devices have been preliminarily characterized in dark condition by measuring their current-voltage (I-V) characteristics from room temperature up to 110 °C by means of a Source Measure Unit Keithley 236. Figure 2 reports the I-V curves vs temperature for the sensors with thickness equal to 0.4 μm. For the curve at room temperature, each point is the average value of 10 sensors of the array, while for the curve at higher temperatures each point is averaged over 5 devices. The standard deviation has been calculated to be below 5%, demonstrating the very good reproducibility and spatial uniformity of the fabrication process.

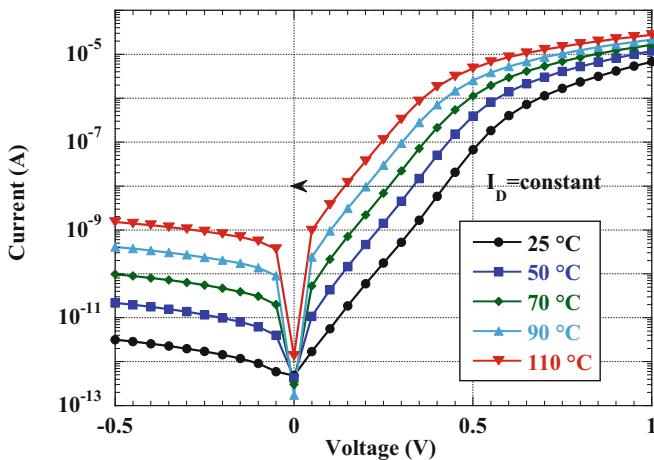


Fig. 2. I-V curves of a sensor characterized by an intrinsic layer of 0.4 μm.

From Fig. 2 we observe that the reverse saturation current at room temperature is around 10^{-12} A in the investigated reverse voltage range. Even though it is well known that a-Si:H devices suffer for 1/f noise [15], in this paper we consider only the contribution

of the shot noise in evaluating the noise performance of the device. Considering that the measurements have a bandwidth of 2 Hz, the corresponding shot noise current is around 1 fA. The measurements at higher temperatures show an exponential increase of the reverse saturation current with temperatures. In particular, at 110 °C the current at –0.5 V is around 2 nA, which leads to a shot noise current around 25 fA. Dark current noise in the order tens of fAs have been achieved also for the other two fabricated arrays, demonstrating that the i-layer thickness does not degrade the low noise properties of a-Si:H photosensors.

In the forward bias voltage range of Fig. 2, we observe that, as expected, increasing temperature at fixed current value (10 nA in Fig. 2) the voltage decreases. Similar behaviors have been found also for the device with 1.2 and 2.4 μm thickness of the intrinsic layer. Figure 3 reports the characterization of the a-Si:H junction, as temperature sensors, by plotting the voltage drop across the diode at constant forward bias current (10 nA) for the three different i-layer thicknesses. From the slopes of the linear fitting of the experimental data we found a sensitivity equal to 3.6, 3.4 and 4.1 mV/°C for the 0.4, 1.2 and 2.5 μm i-layer thickness, respectively. These results demonstrate that the temperature performances do not show substantial dependence on the i-layer thickness keeping their high sensitivity.

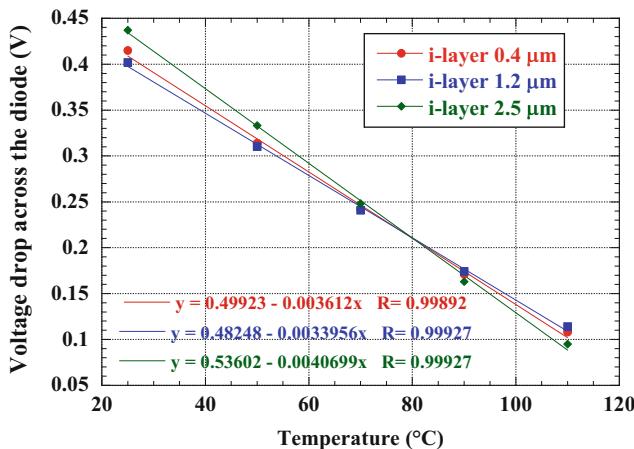


Fig. 3. Sensitivity of the investigated a-Si:H temperature sensors. Points refer to the experimental voltage drops across the diodes measured at constant forward current equal to 10 nA, while solid lines are the linear fittings.

To determine the spectral response, we measured the external quantum efficiency (QE) by means of a dual-branches measurement set-up which includes halogen lamp, monochromator, beam splitter, lenses and a calibrated crystalline silicon. Figure 4 reports the normalized QE curves of the photodiodes. Each point, for each thickness, refers to the averaged value over 5 devices. Depending on the i-layer thickness, the QE shows a peak at different wavelengths. We observe that the device with 0.4, 1.2 and 2.5 μm i-layer display a peak in the green, red and blue region, respectively. While the red-shifted response was expected for the 1.2 μm device, the blue-shifted response for the

$2.5 \mu\text{m}$ was surprising because a longer i-layer should lead to a greater absorption of the longer wavelengths (in the red region) that present lower absorption coefficient. A qualitative and preliminary explanation of this behavior can be the following, considering that light is impinging on the device from the glass substrate (see Fig. 1). A longer i-layer thickness leads to a decrease of the electric field in the whole i-layer, hampering the collection of the photogenerated carriers. However, electrons can still be efficiently collected at the n-doped layer due to their higher mobility-lifetime ($\mu\tau$) product, while holes showing a lower $\mu\tau$ product recombine before reaching the p-doped layer.

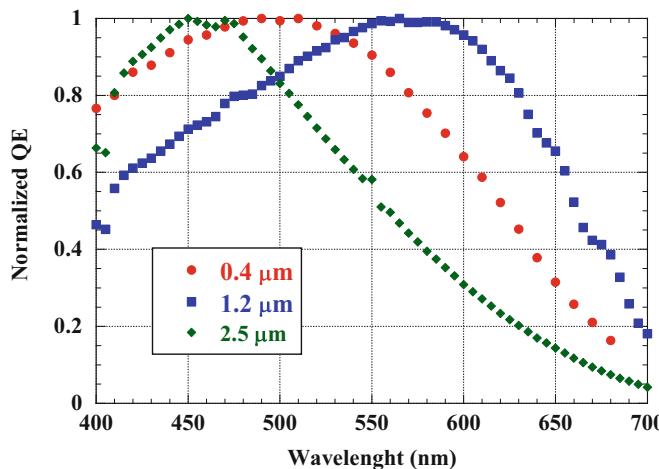


Fig. 4. Normalized quantum efficiency curves for the three investigated devices.

4 Conclusions

In this study we have presented the fabrication and optoelectronic characterization of a-Si:H p-i-n junctions with different thickness of the intrinsic layer. The demand for this study comes from the use of a-Si:H device as temperature sensor and photosensors in lab-on-chip applications, where radiation at different wavelengths need to be detected. Our investigation demonstrates that a proper design of the i-layer thickness can tune the spectral response of the device without degrading neither the noise performances when working as photosensor nor the sensitivity when operating as the temperature sensor.

References

1. Ren, X., Li, J., Jiao, D., Gao, D., Pei, G.: Temperature-dependent performance of amorphous silicon photovoltaic/thermal systems in the long-term operation. *Appl. Energy* **275**, 115156 (2020)
2. Shim, G.W., Hong, W., Cha, J.H., Park, J.H., Lee, K.J., Choi, S.Y.: TFT channel materials for display applications: From amorphous silicon to transition metal dichalcogenides. *Adv. Mater.* **32**(35), 1907166 (2020)

3. Xue, L., Jiang, F., Xi, X., Li, Y., Lin, J.: Lab-on-chip separation and biosensing of pathogens in agri-food. *Trends Food Sci. Technol.* (2023)
4. Karthik, V., Karuna, B., Kumar, P.S., Saravanan, A., Hemavathy, R.V.: Development of lab-on-chip biosensor for the detection of toxic heavy metals: a review. *Chemosphere* **299**, 134427 (2022)
5. Hou, T., et al.: Smartphone based microfluidic lab-on-chip device for real-time detection, counting and sizing of living algae. *Measurement* **187**, 110304 (2022)
6. Nikolaidou, K., et al.: Monolithically integrated optical interference and absorption filters on thin film amorphous silicon photosensors for biological detection. *Sens. Actuators B Chem.* **356**, 131330 (2022)
7. Rao, S., Pangallo, G., Della Corte, F.G.: Integrated amorphous silicon pin temperature sensor for CMOS photonics. *Sensors* **16**(1), 67 (2016)
8. Lovecchio, N., Caputo, D., Costantini, F., Di Meo, V., Nascetti, A., de Cesare, G.: On the stability of amorphous silicon temperature sensors. *IEEE Trans. Electron. Devices* **67**(8), 3348–3354 (2020)
9. Fantoni, A., Costa, J., Fernandes, M., Vygranenko, Y., Vieira, M.: A simulation analysis for dimensioning of an amorphous silicon planar waveguide structure suitable to be used as a surface plasmon resonance biosensor. In: Fourth International Conference on Applications of Optics and Photonics, vol. 11207, pp. 62–67. SPIE (2019)
10. Dekker, S., Isgor, P.K., Feijten, T., Segerink, L.I., Odijk, M.: From chip-in-a-lab to lab-on-a-chip: a portable Coulter counter using a modular platform. *Microsyst. Nanoeng.* **4**(1), 34 (2018)
11. Adamopoulos, C., et al.: Lab-on-chip for everyone: introducing an electronic-photonic platform for multiparametric biosensing using standard CMOS processes. *IEEE Open J. Solid-State Circ. Soc.* **1**, 198–208 (2021)
12. Lovecchio, N., Costantini, F., Nascetti, A., de Cesare, G., Caputo, D.: Thin-film-based multifunctional system for optical detection and thermal treatment of biological samples. *Biosensors* **12**(11), 969 (2022)
13. Santos, D.R., Soares, R.R., Chu, V., Conde, J.P.: Performance of hydrogenated amorphous silicon thin film photosensors at ultra-low light levels: towards attomole sensitivities in lab-on-chip biosensing applications. *IEEE Sens. J.* **17**(21), 6895–6903 (2017)
14. Mirasoli, M., Bonvicini, F., Lovecchio, N., Petrucci, G., Zangheri, M., Calabria, D., Nascetti, A.: On-chip LAMP-BART reaction for viral DNA real-time bioluminescence detection. *Sensors Actuators B: Chem.* **262**, 1024–1033 (2018)
15. Blecher, F., Schneider, B., Sterzel, J., Böhm, M.: Noise of a-Si: H pin diode pixels in imagers at different operating conditions. *MRS Online Proc. Library (OPL)*, **557**, 869 (1999)



Role of Feedthrough Capacitance in Mode-Split MEMS Gyroscope Bias-Instability

Luca Pileri^(✉) and Giacomo Langfelder

MEMS Lab, Department of Electronics, Information and Bioengineering (DEIB),
Politecnico di Milano, Milan, Italy
luca.pileri@polimi.it
<https://www.sensorlab.deib.polimi.it/>

Abstract. MEMS gyroscopes play a crucial role in navigation and stabilization tasks across both consumer and high-end markets. To meet the requirements of these applications, the system must maintain the output stability under external perturbations, like temperature and stress, while minimizing calibration and design costs. In this paper, we investigate the drive loop feedthrough capacitance impact on the system bias instability. Notably, we find that even an aF feedthrough variation forces the drift of the drive oscillation frequency and the change of the optimal demodulation phase. The consequence is a variation of the measured output or, in other words, a non-negligible bias instability contribution. To support our findings, we develop a mathematical model and conduct relative simulations in a controlled Simulink environment. The evaluation matches with Allan variance simulation and with preliminary experiment. By shedding light on the origins of feedthrough contribution, our research lays the groundwork for more precise strategies for bias instability compensation and for discussing other potential sources.

Keywords: MEMS gyroscope · Bias instability · Allan variance

1 Introduction

One critical challenge in current MEMS technology is offset drift, more commonly referred as bias instability (BI), a persistent issue which influences the accuracy of the device during the operation. In recent years, various researchers have proposed different study approaches to investigate source of this non-idealities. Baha Erim Uzunoglu et al. work exploited a stress compensation method to minimize the measured bias instability [1]. Tobias Hiller et al. described the impact of flicker noise [2] on gyroscope Allan analysis. He demonstrates a correlation between the reduction of the flicker noise and BI coefficient measured through the Allan standard analysis. Instead, Milos Vujadinovic et al. pointed

SIE 2024, June 26–28, 2024, Genova, Italy.

© The Author(s), under exclusive license to Springer Nature Switzerland AG 2025
M. Valle et al. (Eds.): SIE 2024, LNEE 1263, pp. 205–212, 2025.
https://doi.org/10.1007/978-3-031-71518-1_23

out the sensitivity stability [3] as source of zero-rate offset (ZRO) drift and bias-instability. In this study, we discuss the impact of feedthrough capacitance (C_{FT}). Specifically, we examine how small variations in C_{FT} affect the overall readout mechanism. To address this problem, we start with a tested MEMS gyroscope and a finely detailed behavioral model of it (Sect. 2). Beyond the overall system mechanism, the feedthrough capacitance contribution is discussed under a mathematical perspective (Sect. 3). The simulation will clarify the dependence of the optimal demodulation phase on C_{FT} and compare it with the retrieved mathematical model. Finally, we present the feedthrough capacitance impact using the Allan deviation analysis, showing agreement with expected results (Sect. 4).

2 System Overview

A MEMS gyroscope measures the angular rate it is subject through the readout of the Coriolis force. For the correct operation of the gyroscope, the mechanical proof mass of the device is controlled by an oscillation loop circuit and a readout sense chain. The former ensures stability in the drive oscillation. Its typical architecture consists of a charge amplifier (CA), an instrumentation amplifier (INA), and a phase-shifter stage. The latter can be implemented either as an analog 90° phase shift stage or through a phase-locked loop circuit. An automatic gain control (AGC) stabilizes the drive displacement amplitude, rejecting the oscillation variation due to thermal drifts. The described electronic configuration guarantees both the Barkhausen criteria at the drive frequency, i.e. $|G_{loop}(j\omega_{drive})| \geq 1$ for magnitude and $\angle G_{loop}(j\omega_{drive}) = 0^\circ$ for phase. After performing a demodulation step between output sense chain and drive phase shifter signal, the input rate (Ω_{IN}) is extracted. The accuracy of the measured rate is affected by quadrature (B_q), which represents a spurious sense displacement super imposed to the Coriolis response, but shifted by 90°. When the reference signal phase perfectly matches the sense one, the contribution of the quadrature component becomes null thanks to demodulation step. However, over time, the initial calibration degrades due to the interaction with external perturbations like temperature, humidity or pressure. This phase shift drift contributes to the alteration of the measured rate. In addition, also sensitivity is affected by environmental condition, thus introducing an error in the rate calculation. Both reference phase and scale factor fluctuation are sources of output (bias) instability. An overview of the system is shown in Fig. 1.

The device of reference is a quad mass amplitude modulated gyroscope, provided by STMicroelectronics and described in De Pace et al. work [4]. Its control electronics uses a 90° stage to shift the single-ended signal. However, the following discussion has a general validity. As we will highlight, the feedthrough capacitance impact is independent from the control electronics. Instead, its relation with outputs depends on the electro-mechanical parameters of the gyroscope. Table 1 reports some device parameters which will become useful in the problem discussion.

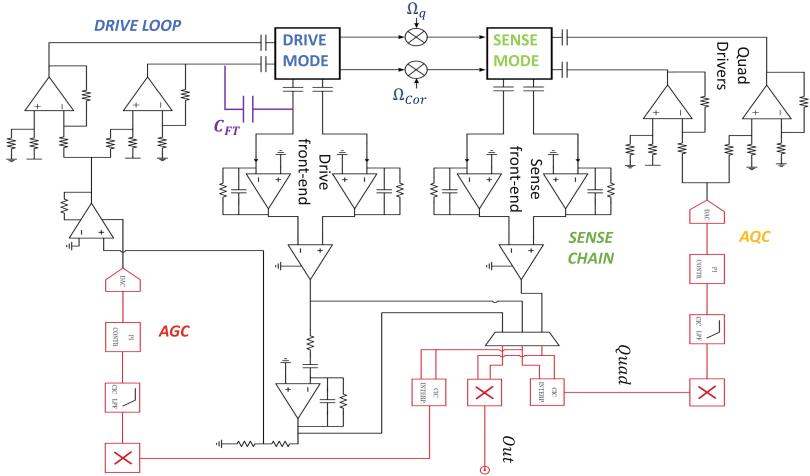


Fig. 1. Overview of the control electronic of the entire system presented in De Pace et al. work [4]. The feedthrough capacitance is highlighted in purple.

Table 1. Starting scenario details.

Parameter	Value
Rotor voltage V_{rot}	4 V
Mode-split Δf_{sp}	1080 Hz
Worst-case quadrature B_q	1000 dps
Residual phase error $\Phi_{err,0}$	0.1°
Nominal C_{FT*}	0.6 fF

*from experimental measures conducted by ST.

3 Feedthrough Capacitance

A feedthrough capacitance is a parasitic component that feeds a spurious parallel signal from the drive loop actuation to the drive front-end virtual ground. Feedthrough capacitance originates from the parasitic coupling between closely spaced electrodes, interconnects, and wiring in a MEMS gyroscope drive oscillation circuit. The physical layout, manufacturing variations, and environmental factors could affect the parasitic capacitance value. The primary impact of C_{FT} fluctuations is the introduction of an additional phase contribution in the drive loop. As a consequence, the Barkhausen criteria for phase is no longer satisfied at the design resonance frequency. The system will adapt itself to oscillate at a slightly different frequency. This minor variation can negatively impact the overall accuracy of the readout by altering the gyroscope sensitivity and the optimal phase for demodulation. To understand this effect better, let's analyze these two

relationships separately. The goal is the derivation of a mathematical prediction for each effect in terms of feedthrough capacitance variation.

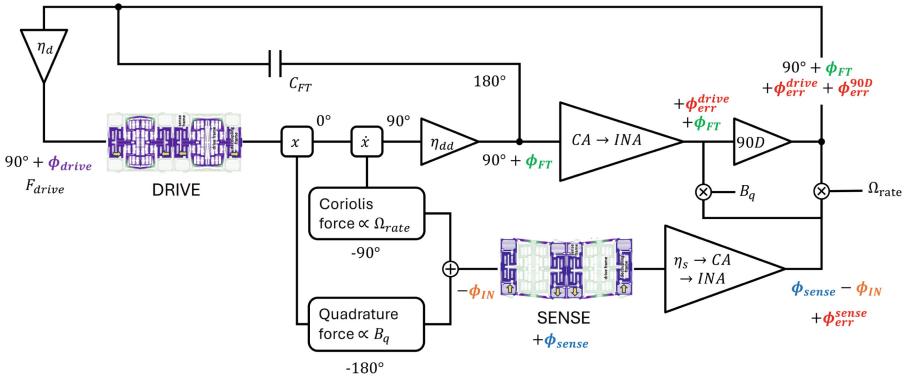


Fig. 2. Block scheme of a generic AM gyroscope architecture. All the reported phases are referred to the drive displacement. η_d , η_{dd} and η_s are, respectively, the transconductance of the drive, drive detection and sense electrodes. Red phases are related to stage singularities. Blue ones come from mechanics transfer function. ϕ_{FT} is the discussed contribution of feedthrough capacitance.

We will refer to a general model of an amplitude-modulated gyroscope, whose drive and sense schemes are illustrated in Fig. 2. For simplicity, the shown model includes just a single feedthrough capacitance between the single-ended drive actuation and detection. C_{FT} is electrical equivalent to the differential feedthrough configuration. It can be shown that the following analysis also applies to a differential circuit scheme. Note that automatic gain control and automatic quadrature compensation are omitted in the model. Their impact on the output signal can be considered negligible to a first-order approximation.

3.1 Impact on Phase

Both in the sense and drive circuit, the architecture stages introduce additional phase errors. Their primary sources are related to the feedthrough capacitance and the singularity of the electronic stages. The consequence is a phase mismatch between the matched output voltage over the demodulation references. Thus, the contribution of B_q is interpreted as rate signal (and viceversa), introducing error in our readout (or AQC circuit). If the electronic stages can be designed to have a negligible and stable phase contribution on signal, the C_{FT} is a parasitic component. Neither its nominal value nor its variation under environmental changes are known or easily predictable. Hence, we need a mathematical relation between C_{FT} and demodulation phase to highlight its contribution.

The current entering in the charge amplifier is the sum of a drive detection component i_{dd} and feedthrough one i_{FT} . Passing through their phasor definitions, we can define the phase of the resulting current at the drive loop front-end input as follows:

$$\Phi_{FT} = \arctan \left(\frac{i_{FT}}{i_{dd}} \right) = \arctan \left(\frac{C_{FT}}{\eta_d \eta_{dd}} \frac{Q_{drive}}{k_{drive}} \right). \quad (1)$$

η_{dd} and η_d are the transconduction of the drive electrodes, respectively of drive detection and actuation. Q_{drive} and k_{drive} are, instead, mechanical parameters of the gyroscope drive architecture. The relation in the Eq. (1) is now applied to the system under test. A variation of just 1 aF over 0.6 fF of nominal value corresponds to a phase shift of 200μ degrees. In presence of a non-compensated quadrature of 1000 degree per seconds (dps), the phase shift causes an output variation of 3.5 milli-dps. The integration of this error leads to a non-negligible source of bias-instability for navigation applications.

3.2 Impact on Oscillating Frequency

The phase error contribution of feedthrough has also a negative impact on the drive loop. Indeed, at the designed frequency f_{drive} the Barkhausen criteria on the phase is not respected. The system still oscillates, but at a slightly different frequency. The drive circuit adapts itself introducing of an additional phase terms given by drive mechanical transfer function (Φ_{drive}). This phase-shift rises when the drive oscillation mechanism is not driven at the resonance peak f_{drive} , but at a frequency in its proximity. From the mechanical phase relation, we can express the actual oscillation frequency as:

$$f_{osc} = f_{drive} - 2 \cdot (\Phi_{err}^{drive} + \Phi_{err}^{90D} + \Phi_{FT}) \cdot \frac{f_{drive}}{Q_{drive}}, \quad (2)$$

where ϕ_{err}^{drive} and ϕ_{err}^{90D} are phase-errors introduced by stage singularities.

As for the discussion on optimal phase demodulation, the Eq. 2 is related to feedthrough capacitance and its variation over time. The phase contribution of electronic drive stages are still considered as negligible and deterministic component. The f_{osc} motion changes the response of the sense chain. Indeed, the Coriolis force and the mechanical response of sense mass has a magnitude gain which depends on the drive oscillation frequency. The consequence is a change in sensitivity which depends only on feedthrough capacitance. However, the frequency variation has a less significant impact with respect to demodulation phase one. Using the same the device numbers, the expected variation is just of 9 mHz for an apto-Farad feedthrough change. The reason behind this negligible contribution is clear in the expression 2: Φ_{FT} components is divided by the drive quality factor, whose value is, typically, in the order of 10^3 to 10^4 .

4 Simulation Outcomes

The verification of the discussed mathematical models consists in two steps. Firstly, the theoretical relations are compared with simulation outcomes. The Simulink model is fed with different nominal value of feedthrough capacitance. The collected data gives the value of drive oscillation frequency f_{osc} , demodulation phase error ϕ_{err} and measured rate Ω for different value of C_{FT} . The C_{FT} is swept between ± 0.2 fF around its nominal value (0.6 fF). The choice of a high, unrealistic, capacitance swept was made to clearly highlight the discussed effect. Then, longer simulations are performed with predefined feedthrough fluctuation of ± 2 aF around 0.6 fF. The Allan analysis of the measured rate will show the bias-instability point of the system. Further experimental analysis will give a more accurate relation between external factor and feedthrough capacitance. The results are reported in Fig. 3, alongside with the theoretical prediction.

Figure 3a and 3b evidence a match between the mathematical model and the simulations. The impact of the frequency variation on scale factor and demodulation phase modifies the measured output. As reported in Fig. 3c, a variation of 1 aF only of the feedthrough capacitance (nominal value of several fF) corresponds to a 3.6 mdps variation, or, in other words, to a bias instability. This trend is in agreement with mathematical prediction. The simulated Allan deviation Fig. 3d validates the extracted correlation. Indeed, the minimum point of the Allan standard deviation gives the bias-instability parameter of the analyzed device. Interestingly, this closely match experimental results on the device Fig. 3d, showing a bias-instability which is similar to the simulated one. However, a fair comparison will be possible in future replicating the same boundary condition of the simulations in a controlled experimental environment.

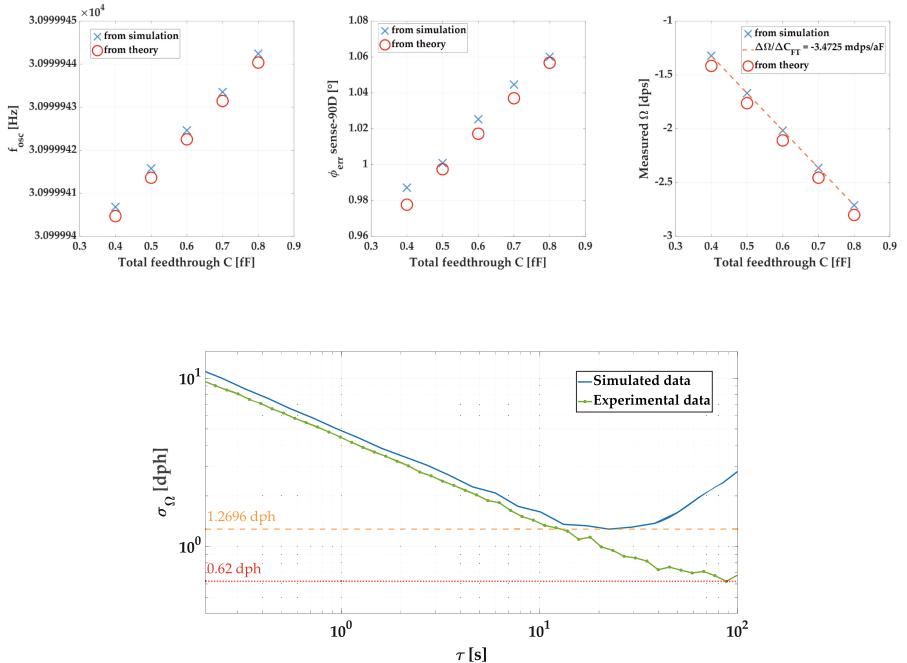


Fig. 3. Simulation results under the following condition: input rate of 1000 dps, quadrature of 1000 dps, AQC loop open. For the Allan evaluation d), the C_{FT} varies between $\pm 2 \text{ aF}$ around its nominal value of 0.6 fF. The simulation result is over imposed to an experimental data.

5 Conclusions

This study emphasizes the significant influence of feedthrough capacitance on MEMS gyroscope bias instability. The alignment between our mathematical model and simulation outcomes provides valuable insights on the system behavior. This set the basis for the investigation of other non-idealities contribution like quality factor variation or mechanical spring non-linearity. Future development will focus on experimental test of the discussed phenomena. The approach will consist in the design of a dedicated electronics in order to isolate and reproduce the C_{FT} variation imposed in Simulink. The extracted experimental data will confirm or correct our simulation model.

References

1. Uzunoglu, B.E., Erkan, D., Tatar, E.: A ring gyroscope with on-chip capacitive stress compensation. *J. Microelectromech. Syst.* **31**(5), 741–752 (2022)
2. Hiller, T., Kuhlmann, B., Buhmann, A., Roth, H.: Noise contributions in a closed-loop MEMS gyroscope for automotive applications. In: IEEE International Symposium on Inertial Sensors and Systems (INERTIAL). Kauai, HI, USA 2017, pp. 62–65 (2017)
3. Vujadinović, M., et al.: Scale factor instability noise in mode-split open-loop MEMS gyroscopes. In: IEEE International Symposium on Inertial Sensors and Systems (INERTIAL). Lihue, HI, USA 2023, pp. 1–4 (2023)
4. De Pace, M., et al.: Split is not dead: a case study on the performance gap between MEMS automotive-grade gyroscopes and high-end applications. *IEEE Sens. Lett.* **7**(12), 1–4 (2023). Art no. 2504904



Efficient Human Activity Recognition: Machine Learning at the Sensor Level

Arianna De Vecchi¹(✉), Alice Scandelli¹, Federica Bossi²,
Benedetta Caterina Casadei², Hazem Hesham Yousef Shalby¹, Marco Boschi²,
and Federica Villa¹

¹ Politecnico di Milano, 20133 Milan, Italy
{arianna.devecchi,federica.villa}@polimi.it

² STMicroelectronics, 20010 Cornaredo, MI, Italy

Abstract. Wearables equipped with Inertial Measurement Units (IMUs) can be used for Human Activity Recognition (HAR) in real-life scenarios. Typically, activity classification occurs within the microcontroller embedded in the wearable device. In this paper, we demonstrate the feasibility of performing real-time HAR at the extreme edge, hence directly within the smart sensor. The evaluation has been carried out on two 6-axis IMUs developed by STMicroelectronics, namely the LSM6DSV16BX and the LSM6DSO16IS, featuring a Machine Learning Core (MLC) and an Intelligent Sensor Processing Unit (ISPU), respectively. In this study, data were collected by using an earbud, and two tasks were analyzed. The first one focused on dynamic activities (go upstairs, go downstairs, sit on a chair, stand up from a chair, walk, stay still), while the second one led to the recognition of a subject's posture (sitting still, standing still). The best results for the first task were achieved by the ISPU of the LSM6DSO16IS programmed with a Convolutional Neural Network (CNN) having an accuracy of 99.2% with 3 s long windows as input. The second task was better handled by a decision tree in the MLC of the LSM6DSV16BX, with an accuracy of 79.1% with 4 s long inputs. The two IMUs showed an energy consumption per inference of 930 nWh and 1180 nWh, respectively.

Keywords: Human Activity Recognition (HAR) · Inertial Measurement Units (IMU) · earable devices · edge computing

1 Introduction

Human Activity Recognition (HAR) refers to the possibility of classifying the movements or actions of a subject by using data collected from sensors [10]. It can be possible to distinguish typical indoor and outdoor activities (walking, running, sitting) or more specific ones, such as the ones carried out in a factory [10]. Moreover, one can choose to exploit HAR in order to monitor a disease or stress levels [10]. HAR has become more common thanks to wearables, as they

made the acquisition of a large amount of data in real-life conditions possible [10].

The main sensors used to classify activities are Inertial Measurement Units (IMUs), i.e. sensors including accelerometers, gyroscopes and sometimes also magnetometers. These can be embedded in head-worn devices, which allow to successfully achieve HAR while leaving the subject hands-free and reducing the amount of movement artifacts with respect to smartphones [12]. Moreover, earables, such as earbuds and headphones, are commonly owned objects [8], which makes them good candidates to perform HAR.

Different studies featuring head-worn devices for HAR are present in the literature, using IMUs, sometimes associated with other sensors such as barometers [10]. Most of these studies are related to smart glasses [2,3,5,7,10,11], where the activity classification is carried out either through signal processing, Machine Learning (ML) or Deep Learning (DL). Among these, only [5] studies the possibility of performing HAR on-the-edge by exploiting the wearable device itself. In [5], 8 classes were analyzed (standing, sitting, walking, lying, going downstairs, going upstairs, running, drinking) and the obtained DL algorithm was successfully loaded in the microcontroller embedded in the smart glasses. Regarding the use of earables, two studies were deemed relevant. In [4], 7 activities were studied, with a focus on head movements (eating, speaking, shaking the head, nodding, walking, staying still, speaking while walking). [6] used both earbuds and a smartwatch to recognize 5 classes (lying, sitting, standing, movement, non-movement) proving that using one single device led to a lower accuracy for specific classes. In fact, data from the earbuds only are not sufficient to distinguish between sitting and standing.

A lack of studies achieving on-the-edge HAR starting from head-worn devices (especially earables) is evident, as, typically, the classification task is carried out in post-processing or in cloud. Moreover, to the best of our knowledge, no studies bringing the HAR process to the extreme edge through smart sensors are present in the literature. However, especially for what concerns the use of earables, it is crucial to develop methods that can process data in real-time [1] and to reduce the battery usage of the device [8], for example by decreasing the data throughput of the device.

In this study, we aim to bring HAR to the extreme edge, i.e. directly on smart IMU sensors, hence proving the feasibility of embedding real-time HAR algorithms in smart IMUs, namely the LSM6DSV16BX and the LSM6DSO16IS, embedded with a Machine Learning Core (MLC) and an Intelligent Sensor Processing Unit (ISPU). Both sensors led to an energy consumption per inference below 1200 nWh.

2 Materials

2.1 IMUs and Earable Devices

Two 6-axis IMUs developed by STMicroelectronics were used in this study. The LSM6DSV16BX is embedded with a Machine Learning Core (MLC), which can

classify an input window into one of the user-selected classes through one or more decision trees (DTs). The trees directly take an input from the IMU and classify it according to the settings, selected through Unico GUI, a software developed by STMicroelectronics. The LSM6DSO16IS, instead, features an Intelligent Sensor Processing Unit (ISPU), a core that can be programmed in C language, having an 8 kB RAM for data storage and a 32 kB RAM for program memory. DL algorithms can be trained through Python and converted in C language for the ISPU thanks to a STMicroelectronics proprietary software.

In order to collect data, an earable device resembling an earbud, previously developed by STMicroelectronics, (Fig. 1) was used. This device embeds an LSM6DSV16BX IMU and a Bluetooth Low-Energy (BLE) module and it can be connected to a smartphone in order to save data.

Some additional hardware, such as a NUCLEO-F401RE microcontroller, was used to easily program the smart IMUs.

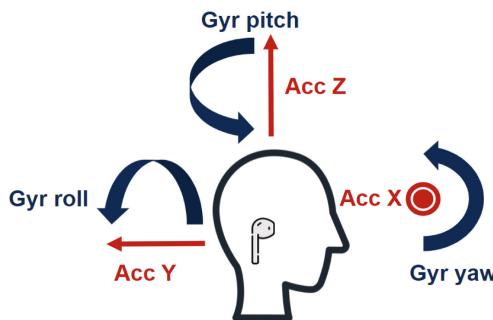


Fig. 1. Earable device axes.

2.2 Dataset

In order to collect the dataset, the LSM6DSV16BX embedded in the earable device was used, with 60 Hz Output Data Rate (ODR) and sampling all 6 axes of the IMU. The accelerometer had a Full-Scale Range (FSR) of $\pm 16\text{ g}$, while the gyroscope had FSR equal to $\pm 2000\text{ dps}$. The dataset, which focused on 7 different classes, was acquired following three different protocols:

1. **Protocol 1:** 5 subjects (2 males, 3 females), aged 30 ± 5 years
 - (a) **Walk:** walking for 15 min at a preferred pace.
2. **Protocol 2:** 24 subjects (16 males, 8 females), aged 34 ± 11 years
 - (a) **Sitting:** sitting down on a chair 10 times.
 - (b) **Standing:** standing up from a chair 10 times.
 - (c) **Down:** walking down 85 steps.
 - (d) **Up:** walking up 85 steps.

3. **Protocol 3:** 8 subjects (5 males, 3 females), aged 31 ± 10 years
 - (a) **Still-Sit:** sitting for 3 min.
 - (b) **Still-Stand:** standing for 3 min.

The data for the class Walk (Protocol 1) had already been acquired by STMicroelectronics for a different study, but we exploited it for this study as well. Protocol 2 includes dynamic activities, whereas Protocol 3 focuses on static activities (Still). Note that in the Still class subjects were free to talk, work on a laptop or use a smartphone during the acquisitions, simulating real-life data. Moreover, no instructions were provided for the other classes as well, as the actions were performed according to the subject's preference.

3 Methods

The data collected with LSM6DSV16BX have also been used to train and test the performance of the algorithms implemented in the ISPU of the LSM6DSO16IS. Since the two sensors work at different ODRs, the data were resampled at 52 Hz to emulate a dataset acquired with the LSM6DSO16IS. Moreover, both datasets (at 60 Hz and 52 Hz ODR) were split into windows of 3 and 4 s, to find the best input size, and used for training and testing using a 70:30 ratio.

Due to the difficulty in recognizing the Still-Sit and Still-Stand classes [6], two tasks were tested. The first one consisted of dynamic activity recognition (Down, Up, Sitting, Standing, Walk, Still), using data from all three protocols. The second one focused on a binary classification of the subject's posture (Still-Sit, Still-Stand), using data from Protocol 3. Both tasks could be performed at the same time when using the MLC, while the software used to program the ISPU allowed to embed one model at a time in the core.

Starting from the MLC, the data were labeled and fed into the Unico GUI interface, which allowed us to select the DT features, such as the mean, variance, energy, distance among peaks, number of positive and negative zero-crossings of the accelerometer and gyroscope axes, of their norm or their squared norm. For what concerns the ISPU, various Convolutional Neural Network (CNN) architectures were tested, as these are the best-performing in HAR [9] and can classify complex patterns without the need for explicit feature extraction [4]. A grid search exploration was performed to select the DTs and the CNNs parameters.

4 Results

The results of the comparison are summarized in Table 1, alongside the best window size.

Regarding dynamic activity recognition, the normalized matrices for the best DT and CNN are presented in the top section of Fig. 2. The DT, having 48 leaves and using 20 features, showed issues in distinguishing the Sitting and Standing classes. The signals related to these classes show similar patterns, which could be difficult to differentiate through the features available in the MLC. The analysis

Table 1. Test set results for dynamic activities recognition (Standing, Sitting, Down, Up, Walk, Still) and posture recognition (Still-Sit, Still-Stand).

		Input shape	Window size	Accuracy	F1-Score	Recall
Dynamic	DT	[240, 6]	4 s	95.4%	87.6%	88.1%
	CNN	[156, 6]	3 s	99.2%	97.9%	97.9%
Posture	DT	[240, 6]	4 s	79.1%	78.7%	78.5%
	CNN	[156, 6]	3 s	73.2%	70.7%	71.9%

shows that CNNs performed better than DTs for dynamic activities, achieving 99.2% accuracy and 97.9% F1-score. Such CNN is composed of 3 convolutional blocks. The convolutional layer of the first block had kernels of size 5 and stride 2 and presented 4 feature maps. The convolutional layers of the other two blocks featured the same kernels, but the number of maps was doubled. Finally, the dense layer featured a softmax activation function.

The normalized confusion matrices for the posture recognition task are presented in the bottom part of Fig. 2. The CNN had 5 convolutional blocks, with the convolutional layer of the first one having 2 feature maps and the same kernel as the CNN used for dynamic activity recognition. The dense layer featured a hyperbolic tangent activation function. Moreover, batch normalization layers had to be added in order to reduce overfitting. However, such a model performed poorly when compared to a DT, having 18 leaves and using 12 features, which achieved 79.1% accuracy and 78.7% F1-score.

In conclusion, for what concerns dynamic activity recognition, the CNN greatly outperformed the DT embedded within the MLC. On the other hand, the obtained performances for posture recognition using CNNs are comparable to those presented in [5], while the implemented DT outperformed other studies where head-worn devices were used [5, 6, 10].

Moreover, the advantages of our study are not only in terms of performance but also in terms of power consumption. The energy consumption per inference was measured by supplying the two IMUs with 1.8 V and configuring them to raise an interrupt upon processing completion. Such values include the energy consumption for both running the IMU and performing an inference. As such, the LSM6DSV16BX consumed about 1180 nWh per inference over an input window of 4 s classifying the subject's posture, while the LSM6DSO16IS showed an energy consumption of about 930 nWh per inference over an input window of 3 s when recognizing dynamic activities. Such values are much lower than those presented in [5], where 1120 nWh are required by the microcontroller just to perform an inference, without including data collection, which consumed 9100 nWh. These results prove that bringing the computation to the extreme edge through smart sensors greatly reduces the energy consumption required for collecting and processing the data. In fact, in our application, the energy consumption for data transmission is greatly reduced, as only 1 byte, describing the classification output, is read per inference, instead of the raw data (over 1 kB).

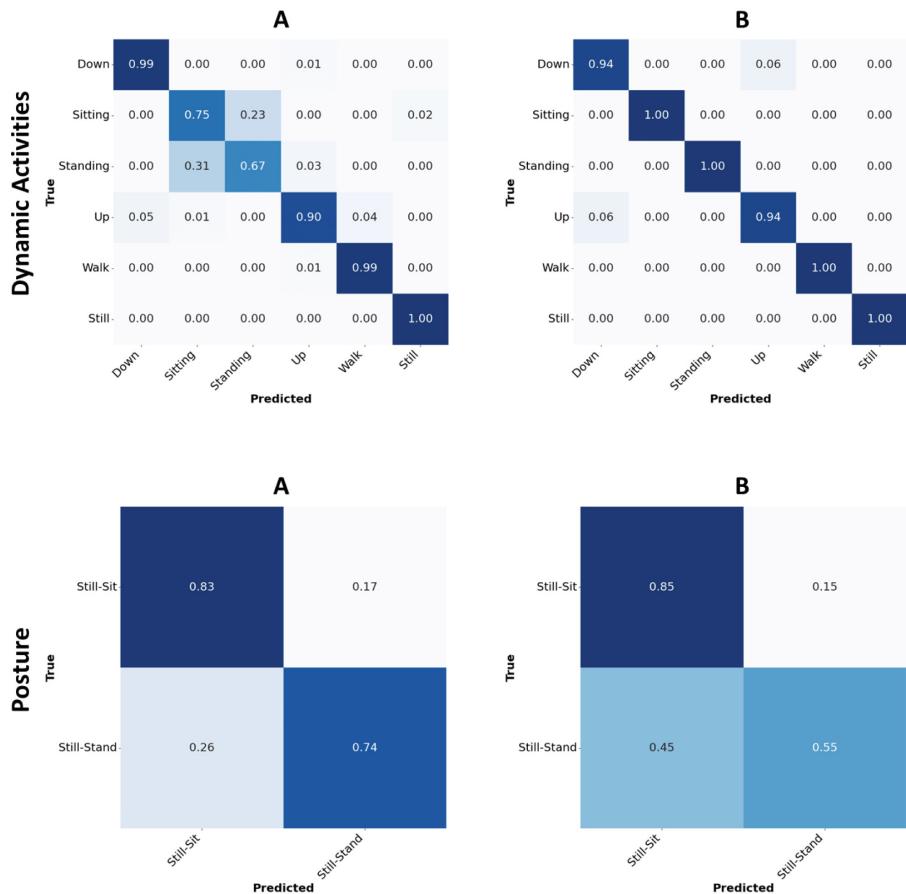


Fig. 2. Normalised test set confusion matrices for dynamic activity recognition through a DT (top A) and a CNN (top B), and for posture recognition through a DT (bottom A) and a CNN (bottom B).

5 Conclusions and Future Developments

The feasibility of bringing HAR algorithms to the extreme edge was proven, successfully filling the gap encountered in the literature. Two smart IMUs by STMicroelectronics, the LSM6DSV16BX and the LSM6DSO16IS, were correctly programmed to perform HAR. The results were obtained using a realistic dataset, especially regarding the classes related to the subject's posture, and the classification was split into two tasks to achieve better results regarding all classes.

The dynamic activity recognition task (Down, Up, Sitting, Standing, Walk, Still) was better handled by a CNN implemented on the ISPU, with an accuracy of 99.2% and an F1-score of 97.9%. On the other hand, the subject's posture (Still-Sit, Still-Stand) was better classified by the MLC, programmed with a decision tree having an accuracy of 79.1% and an F1-score of 78.7%.

Our study also showed favorable results regarding energy consumption, as the energy per inference consumed by the LSM6DSV16BX for posture classification and by the LSM6DSO16IS for dynamic activity recognition corresponded to 1180 nWh and 930 nWh, respectively. This proved that bringing HAR to the extreme edge not only reduces the data throughput of the sensor but also the energy consumption with respect to the traditional methods.

Future works will encompass the simultaneous usage of two devices, one equipped with an LSM6DSV16BX and the other with an LSM6DSO16IS, to test the developed algorithms in real-time conditions.

References

1. Ashry, S., Ogawa, T., Gomaa, W.: Charm-deep: continuous human activity recognition model based on deep neural network using IMU sensors of smartwatch. *IEEE Sens. J.* **20** (2020). <https://doi.org/10.1109/JSEN.2020.2985374>
2. Cristiano, A., Sanna, A., Trojaniello, D.: Daily physical activity classification using a head-mounted device. In: 2019 IEEE International Conference on Engineering, Technology and Innovation (ICE/ITMC), pp. 1–7. IEEE (2019)
3. Gjoreski, H., et al.: Head-AR: human activity recognition with head-mounted IMU using weighted ensemble learning. In: Activity and Behavior Computing pp. 153–167 (2021)
4. Islam, M.S., Hossain, T., Ahad, M.A.R., Inoue, S.: Exploring human activities using eSense earable device. In: Ahad, M.A.R., Inoue, S., Roggen, D., Fujinami, K. (eds.) *Activity and Behavior Computing. Smart Innovation, Systems and Technologies*, vol. 204, pp. 169–185. Springer, Singapore (2021). https://doi.org/10.1007/978-981-15-8944-7_11
5. Novac, P.E., Pegatoquet, A., Miramond, B., Caquineau, C.: UCA-EHAR: a dataset for human activity recognition with embedded AI on smart glasses. *Appl. Sci. (Switz.)* **12** (2022). <https://doi.org/10.3390/app12083849>
6. Rashid, N., Nemati, E., Ahmed, M.Y., Kuang, J., Gao, J.A.: MM-HAR: multimodal human activity recognition using consumer smartwatch and earbuds. In: 2023 45th Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC), pp. 1–4. IEEE (2023)
7. Raychoudhury, M., Yu, H., Kiper, J.: ActiviSee: activity transition detection for human users through wearable sensor-augmented glasses (2022). <https://doi.org/10.1145/3544793.3560397>
8. Seneviratne, S., et al.: A survey of wearable devices and challenges (2017). <https://doi.org/10.1109/COMST.2017.2731979>
9. Shukla, P.K., Vijayvargiya, A., Kumar, R., et al.: Human activity recognition using accelerometer and gyroscope data from smartphones. In: 2020 International Conference on Emerging Trends in Communication, Control and Computing (ICONC3), pp. 1–6. IEEE (2020)

10. Stankoski, S., et al.: Recognizing activities of daily living using multi-sensor smart glasses (2023). <https://doi.org/10.23919/MIPRO57284.2023.10159701>
11. Wahl, F., Freund, M., Amft, O.: WiseGlass: smart eyeglasses recognising context (2015). <https://doi.org/10.4108/eai.28-9-2015.2261470>
12. You, Z., et al.: Activity monitoring using smart glasses: exploring the feasibility of pedometry on head mounted displays. In: Alam, M.M., Hämäläinen, M., Mucchi, L., Niazi, I.K., Le Moullec, Y. (eds.) BODYNETS 2020. LNICST, vol. 330, pp. 153–167. Springer, Cham (2020). https://doi.org/10.1007/978-3-030-64991-3_11



Bio-reconfigurable Impedance-Based Platform for Multiplexing Diagnostic

Arianna Adelaide Maurina¹(✉), Cainā de Oliveira Figares¹, Francesco Damin², Chiara Capelli², Laura Sola², Marcella Chiari², Francesco Zanetto¹, Giorgio Ferrari¹, and Marco Sampietro¹

¹ Politecnico di Milano, Milan, Italy

ariannaadelaide.maurina@polimi.it

² Centro Nazionale di Ricerca (CNR) – SCITEC, Milan, Italy

Abstract. An innovative portable bioelectronic platform capable of multiplex detection, enabling simultaneous reading of multiple targets on a biosensor chip, has been developed. The platform utilizes Differential Impedance Sensing (DIS) with nanoparticle amplification. It features a sensor surface with 7 gold-interdigitated microelectrodes arranged differentially to minimize temperature and ion content fluctuations. This system facilitates simple adjustment of bio-probes for individual sensing sites, allowing for versatile detection of targets, ranging from DNA oligonucleotides to antigen-antibody complexes. This multiplexing diagnostic capability is essential for both current and future diagnostic instruments.

Keywords: Multiplex detection · Impedance sensing · Biosensor · Point-of-care instrumentation · Bio-probe · Diagnostic

1 Introduction

In the past decades, the world has exceeded 8 billion in population, a value that continues to grow. Moreover, the movement of people has reached its high for leisure, migratory and working reasons; new infections may arise quickly, spreading and posing a threat to public health. The necessity for efficient, adaptable, rapid, selective and highly sensitive diagnostic tools is evident, as the COVID-19 pandemic has shown us. Viral infection diagnosis is realized through two main approaches: identification of antibodies produced against viral proteins during or after the virus's incubation period [1] or direct detection of the entire virus or its constituents, including viral nucleic acids (DNA and RNA), viral proteins, intact viral particles. Traditional methods such as polymerase chain reaction (PCR), virus culture, and enzyme-linked immunosorbent assay (ELISA) are commonly used for detection.

In this paper, we present a purely electronic method that is adaptable and bio-reconfigurable, targeting parallel diseases from a single clinical sample. This system measures the impedance between metal electrodes with a lock-in approach, evaluating the medium conductivity variation whenever the target is present.

2 Electronic Platform

2.1 Biosensor

Biochip

The biosensor chips are constituted by 7 interdigitated electrodes (IDE). They are realized over a borosilicate substrate, evaporating 5 nm of Cr, 120 nm of Au, and a few μm of a non-conductive and biocompatible polymer SU8 patterned over the wiring to reduce parasitism and noise. COMSOL simulation suggested the ideal IDE parameters: 3 μm width, 3 μm gap and 90 μm length, resulting in a final optimal sensitivity of 100 ppm. The biochip enables the immobilization of molecules thanks to a copolymer, specifically MCP-4, offering anti-fouling properties.

The utilized copolymers consist of dimethylacrylamide (DMA), 3-(trimethoxysilyl)propyl methacrylate (MAPS), and a third monomer, typically N-acryloyloxy succinimide (NAS). NAS, as a functional group, reacts with amines, thereby facilitating the binding of proteins, peptides, and amino-modified oligonucleotides [2].

To prevent non-specific binding on the chip surface, the functionalization step is followed by surface passivation using ethanolamine: this process occupies any free binding sites not attached to the probes.

The surface modification with the MCP-4 is essential for bio-functionalization, as each interdigitated electrode (IDE) is spotted and covered with biological probes such as antigens, antibodies, or specific oligonucleotide strands, depending on the target molecule in the sample.

The experimental spectrum of the IDEs before surface treatment exhibits the behavior shown in Fig. 1(a). In order to improve the wettability and enhance the high frequencies conductivity where the resistive plateau the surface has been treated. Initial improvement is achieved with oxygen plasma treatment, presented in Fig. 1(a), and comparable enhancement is observed in the spectrum obtained with copolymer coating, Fig. 1(b), which is essential and indispensable for biofunctionalization.

However, the copolymer induces a reduction in the double-layer capacitance by thickening the interfacial layer, resulting in a shift of the resistive plateau to higher frequencies, approaching the upper limit of the instrument's operational bandwidth.

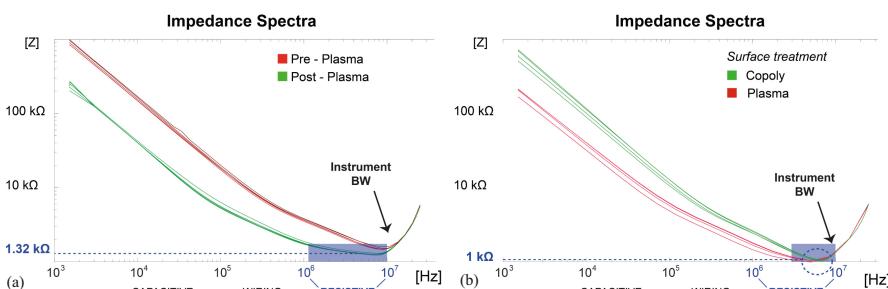


Fig. 1. Impedance spectrum (a) before and after plasma (b) only plasma and with copoly.

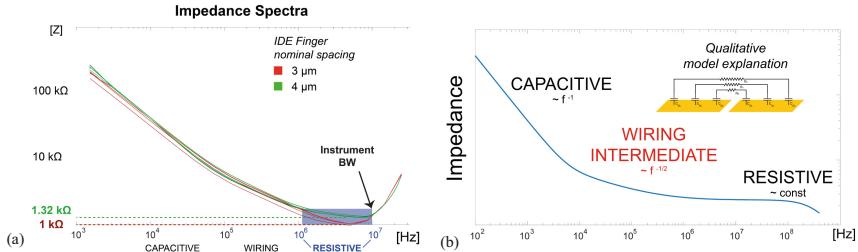


Fig. 2. (a) Impedance spectrum of 3 μm or 4 μm IDE width and gap (b) COMSOL wiring spectrum qualitative simulation

Due to this shift at higher frequencies, recent considerations have been made to slightly modify the IDE design by increasing the width and gap, thereby lowering the frequency at which the resistive plateau appears, as shown in Fig. 2(a). However, this design adjustment would result in a sensitivity worsening, therefore a careful tradeoff must be implemented. The resistive plateau region identifies the frequency interval in which the measurement will take place, and, typically, it emerges after an intermediate region where the frequency dependence transitions between capacitive and resistive behavior. In Fig. 2(b) a COMSOL spectrum simulation of the wiring structure is shown, identifying it as the responsible for the transition region.

2.2 Multiplexing

Multiplexing capabilities are enabled by the multiple IDE configuration shown in Fig. 3. Each sensor contains seven IDEs: one is always left clean to serve as a reference in the differential measurement approach, thereby reducing common mode errors due to global variations. The remaining IDEs can be spotted with different probes, depending on the number of targets under study. The structure is designed to ensure the same voltage drop across various wirings, thereby applying the same V_{IDE} to each electrode.

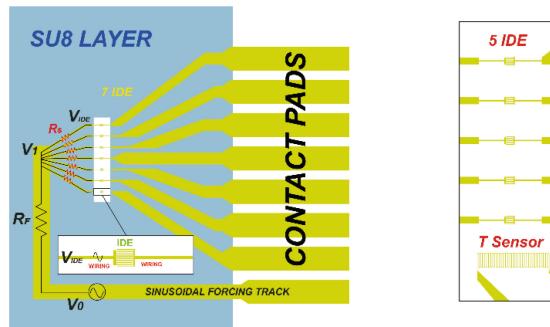


Fig. 3. Multiplexing chip structure and resistive model

Additionally, whenever the temperature of the chamber wants to be measured and controlled, a local serpentine replaces two IDEs, so that the sensor is inside the chamber and close to the active sensing area, measuring the local impedance variation.

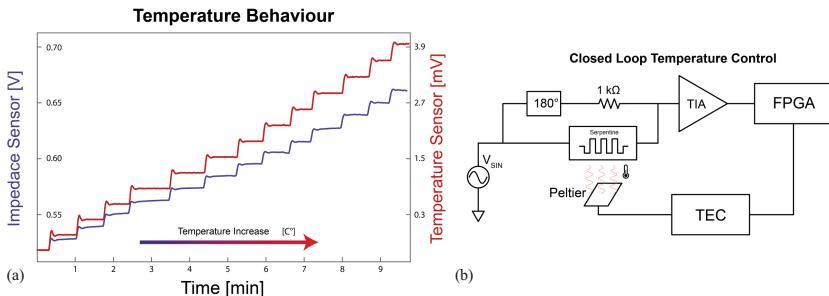


Fig. 4. (a) Voltage temperature curves of serpentine sensor and IDEs with increasing temperature
(b) Schematic representation of closed loop temperature control cleotides chains.

2.3 Temperature Control

One of the critical parameters to be controlled during biological experiments is the temperature. Within the microfluidic chamber, the thermal conditions of the liquid influence not only its ionic conductivity but also the structural conformation and integrity of biological entities immobilized over the sensor, like antigens, antibodies or oligonucleotides chains.

Figure 4(a) displays the voltage curves acquired by the serpentine temperature sensor, depicted in red, which directly correlate with temperature variations. Additionally, the figure shows in blue the signal acquired by the interdigitated electrode (IDE), which is influenced by temperature fluctuations due to changes in the resistive behaviour of the liquid. The temperature control system, schematically illustrated in Fig. 4(b), is integrated into the platform. The output from the serpentine sensor is initially processed by an analog front-end incorporating a transimpedance amplifier (TIA), followed by digital processing using an FPGA. The FPGA output is then converted via a DAC and sent to the TEC that regulates the Peltier cell situated beneath the chamber, thereby closing the feedback loop for precise temperature control.

2.4 Measurement Technique

The measurements are conducted in PBS, which closely replicates the human serum ionic composition and conductivity. Variations in impedance are computed by tracking changes in conductivity upon the binding of the target molecule.

The objective of this measurement is to determine the presence of the target molecule (antigen, antibody, etc.) within the sample and ascertain its binding to the probe. However, this mere binding does not induce a significant change in impedance due to the minimal steric hindrance of these molecules. To amplify the current and thereby enhance

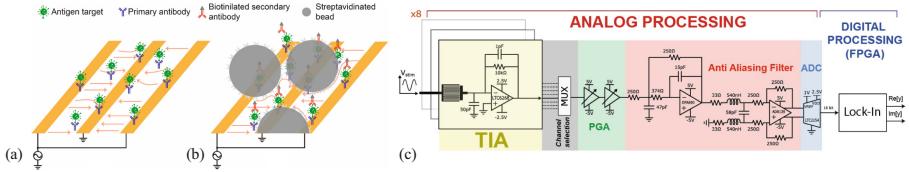


Fig. 5. Current variation after target binding (a) without (b) with beads enhancement. (c) board schematic of analog and digital signal acquisition and processing.

the impedance variation, streptavidin-coated polymeric beads, which are non-conductive and have a diameter of 800 nm, are employed and bind to the formed biotinylated biological complex, as illustrated in Fig. 5.

Given a volume V_f containing a fluid with conductivity σ_f , and a dispersed particle with σ_p conductivity much smaller than the fluid one, the effective fluid-mixture σ_{mix} can be derived using Maxwell's mixture theory [3]:

$$\sigma_{mix} = \sigma_f \left(1 + 3 \frac{V_p}{V_f} \frac{\sigma_p - \sigma_f}{\sigma_p + 2\sigma_f} \right) \approx \sigma_f \left(1 - \frac{3V_p}{2V_f} \right) \quad (1)$$

Finally, by substituting this expression in the evaluation of the relative resistance variation caused by the particle, we obtain:

$$\frac{\Delta R}{R_{sol}} = \frac{R_{mix} - R_{sol}}{R_{sol}} = \frac{3V_p}{2V_f} \quad (2)$$

The impedance variation is captured and processed using a combined analog and digital methodology. The current from each interdigitated electrode (IDE) is detected by eight transimpedance amplifiers (TIAs) and processed via a single channel facilitated by an initial multiplexer (MUX) selection. Analog filtering is employed for anti-aliasing, and a Lock-In amplifier is digitally implemented on the FPGA. The measurement is conducted in the MHz frequency range, thereby isolating the resistive component and effectively filtering out noise and capacitive contributions to the signal.

3 High Sensitivity Probe-Target Detection

Antibody detection - The whole instrument has been validated and tested for the detection of Dengue primary antibodies in human serum. Different antibodies concentration results in proportional beads binding and impedance changes. Figure 6(a) shows the experimental LOD curve extending over 4 decades of target concentrations, resulting in a detection capability down to 88 pg/mL [4]. The microphotographs visually show the correspondence between the electrical measurements and the concentration of the complete biological complex attached to the beads.

Antigen detection - Current on-going experiments are targeting direct antigen detection in human serum: P24 antigen for HIV and the SARS-CoV-2 spike proteins. (b) presents the time evolution of the differential signals obtained before and after the streptavidinated beads binding to the HIV biotinylated complex. The amplitude of

the signal step is correlated to the number of hybridized targets on the surface of the biosensor. This result demonstrates the bio-reconfigurability of the platform, able to detect both antibodies and antigens of various pathogens by simply modifying the biofunctionalization.

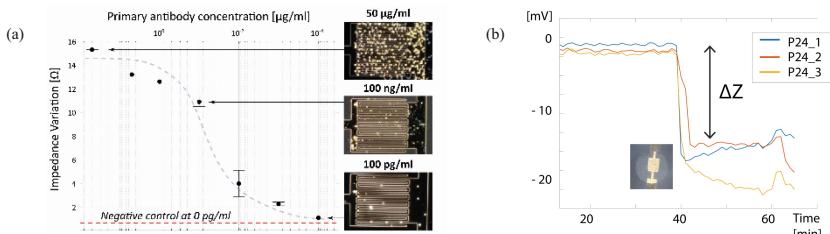


Fig. 6. (a) Dengue LOD curve of IDE impedance variation[4] (b) Differential voltage output P24 antigen binding experiment of three different IDE.

DNA detection - The system has been already validated also for DNA oligonucleotide detection [5], where the spotted probe is a single short DNA strand, and the target is the complementary biotinylated sequence. Current research is focusing on more complex reagents, such as PCR-amplified biotinylated sequences of respiratory pathogens. A significant challenge arises from the three-dimensional conformation adopted by long sequences when immobilized on a surface. Specifically, the extended PCR sequence may only partially bind to the probe, with the unbound segment potentially folding back, thereby hindering the accessibility of the terminal biotin to the polystyrene streptavidin-coated bead. To address this issue, we are investigating the incorporation of a stabilizer—a short sequence complementary to the unbound segment of the PCR product—to enhance the rigidity of the entire biological complex, ensuring the biotin remains exposed and readily accessible to the beads.

Acknowledgements. The authors wish to thanks the staff of Polifab, the nanofabrication facility of Politecnico, N.Clementi and E.Criscuolo from Laboratory of Microbiology and Virology of San Raffaele Hospital (Milano) for useful discussions on Multiplex analysis, and the financial support of the Italian MUR with PRIN project 2022EJL28B.

References

1. Khan, M.Z.H., et al.: Ultrasensitive detection of pathogenic viruses with electrochemical biosensor: state of the art. *Biosens. Bioelectron.* **166** (2020)
2. Vanjur, L., et al.: Copolymer coatings for DNA biosensors: effect of charges and immobilization chemistries on yield, strength and kinetics of hybridization. *Polymers (Basel)* (2021)
3. Granqvist, C.G., Hunderi, O.: Conductivity of inhomogeneous materials: effective-medium theory with dipole-dipole interaction. *Phys. Rev. B* (1978)

4. Piedimonte, P., et al.: Differential impedance sensing platform for high selectivity antibody detection down to few counts: a case study on dengue virus. In: Biosens.& Bioelectron, vol. 202 (2022)
5. Piedimonte, P., et al.: Bio-reconfigurable differential impedance electronic platform for multiplex biomarker detection. In: IEEE BioCAS Conference (2023)



Architectural Modeling and Experimental Characterization of a SPAD-Based Imager Developed for Fast-Quantum Ghost Imaging Applications

Enrico Manuzzato^{1,3(✉)}, Massimo Gandola¹, Matteo Perenzoni^{1,2}, Leonardo Gasparini¹, and Roberto Passerone³

¹ Fondazione Bruno Kessler, Trento, Italy

manuzzato@fbk.eu

² Sony Semiconductor Solutions Europe, Trento, Italy

³ Department of Information Engineering and Computer Science, University of Trento, Trento, Italy

Abstract. Quantum Ghost Imaging (QGI) uses quantum light properties to investigate biological samples. It involves a single quantum source generating two beams: a visible signal beam detected by an image sensor and an idler beam with sample information detected by a single-channel bucket detector. Temporal correlations between these two detectors are exploited to create a ghost image of the sample at the target wavelength without requiring an expensive custom detector. This study presents a Monte Carlo simulation model of a Single Photon Avalanche Diode (SPAD) based array for QGI microscopy highlighting the key features and major limitations. A 100×100 -pixel array prototype is presented and characterized showing a less than 3% false-event rate and an average correlation window ranging between 3 and 7.8 ns with 0.4 and 0.6 ns standard deviation respectively. A smart zero-suppression readout allows fast QGI up to 80 kframe/s.

Keywords: Single Photon Avalanche Diode (SPAD) · Quantum Ghost Imaging (QGI) microscopy · time correlation · high frame rate

1 Quantum Ghost Imaging Microscopy

Quantum Ghost Imaging (QGI) microscopy is a well-established technique that enables the diagnostics to exploit the quantum light properties. This involves the excitation of a non-linear crystal with a high-energy laser pump to generate entangled photon pairs via spontaneous parametric down-conversion (SPDC). Due to the conservation of energy and momentum, the resulting photons have lower wavelengths and exhibit anti-correlated momenta. Figure 1 illustrates the working principle in a QGI setup. The entangled photons, commonly referred to as the *signal* and *idler* are correlated in their spatio-temporal characteristics.

Only the idler photons interact with the sample under investigation, and their presence is detected by a bucket detector specifically designed for this purpose. In contrast, the signal photons do not interact with the sample, but their position is captured using a camera-like detector operating in the visible portion of the light spectrum. Then, time correlation is applied to build the ghost image by combining the information of both detectors. In this way, sample QGI can be performed at different wavelengths, without using unavailable or expensive cameras operating in a specific portion of the light spectrum.

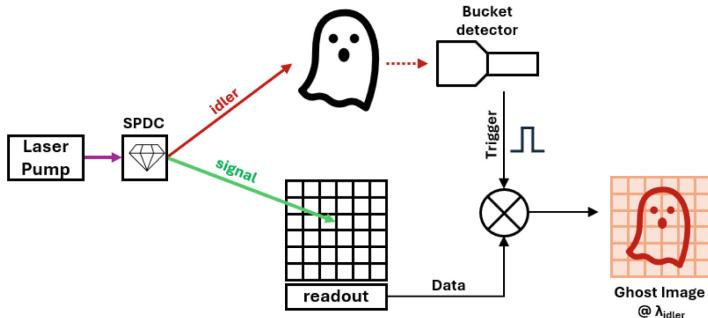


Fig. 1. Ghost imaging technique: working principle.

This principle was first experimentally demonstrated by Strekalov et al. [1] and Pittman et al. [2] using single channel detectors and a scanning procedure. In later demonstrations [3,4], imaging configurations based on time-gated Intensified Charge-Couple Devices (ICCD) were introduced relying on synchronous individual frame analysis, eliminating the need for a scanning procedure. However, these implementations involve bulky optical image-preserving delay lines and suffer lengthy acquisition time. More recently, Single Photon Avalanche Diode (SPAD)-based arrays with timestamping capability were adopted by Gili et al. [5] and Pitsch et al. [6], replacing ICCDs. Thanks to the pixel Time-to-Digital Converter (TDC), correlations between pixels and bucket detector signals are asynchronously reconstructed based on post-processing timestamp comparison. This allows distinguishing entangled pairs from background noise without the need for image-preserving-delay lines and shortening the acquisition times by two orders of magnitude. However, despite the recent advancements in QGI, current implementations are still limited by a relatively long acquisition time, which makes them unsuitable for fast moving objects or biological sample analysis. The overall acquisition speed can be further improved by reducing the required post-processing time by embedding the correlation directly into the sensor array focal plane [7].

This work introduces a Monte Carlo simulation model for a SPAD based array developed for QGI microscopy highlight the key features and limitations. A prototype chip previously developed for QGI is presented and characterized

showing the effectiveness of the proposed sensor architecture and an agreement between simulated and measured data trends.

The document is structured as follows: Sect. 2 provides a description of the “looking-back” detection mechanism. The following section shows the developed numerical model and the Monte Carlo simulation results. Section 4 describes the experimental results and sensor characterization. The conclusions are reported in Sect. 5.

2 “Looking Back” Detection Mechanism

The architecture of the detector is based on the SPAD-based imager proposed by Gandola et al. [7] which performs time correlations between bucket trigger and signal photons directly at the pixel level enabling real-time ghost imaging without requiring data post-processing. Figure 2 shows a timing diagram of the detection scheme and the pixel architecture employing the “looking back” principle. The pixel integrates a compact electrical delay line along with a correlation network and a 1-bit SRAM memory cell to store the possible correlation detected by the pixel. The delay line compensates the intrinsic bucket electrical delay T_{delay} , usually in the order of tens of nanoseconds, shifting the output of the SPAD front-end (FE) in time. The correlation network enables the detection of photon pairs within a tunable correlation window T_{win} , only when bucket trigger and the *pulse* signals, generated by a monostable, are simultaneously detected. The output of the correlation network is then stored in the pixel SRAM in order to be read out.

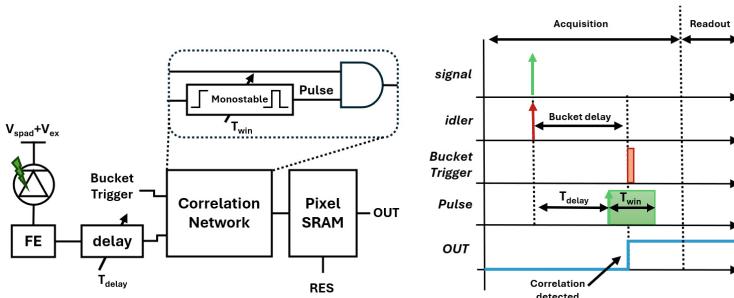


Fig. 2. Pixel architecture and timing diagram.

3 Monte Carlo Simulation Model

3.1 Numerical Model

A Monte Carlo simulation model is developed to understand the system trade-offs and to optimize the design. The false-event triggering probability due to

the intrinsic dark count noise of the SPAD detector is derived varying the SPAD excess voltage (V_{ex}), the sensor size, the number of deactivated hot-pixels (screamers), as well as the width of the in-pixel time correlation window T_{win} . Each SPAD is modeled as a Poissonian source of noise with inter-arrival time of noisy events for each pixel given by expression (1):

$$T_{int}(x, y) = -\frac{\ln(U(0, 1))}{\lambda} \quad (1)$$

where $U(0, 1)$ represents a random uniform distribution and λ is Poissonian distribution parameter equal to the average SPAD Dark Count Rate (DCR). The DCR values assigned to individual pixels are randomly sampled from a distribution observed in previously fabricated devices using the same technology. These DCR values were then adjusted based on the expected pitch (17 μm) and fill-factor (33%), resulting in the distribution shown in Fig. 3 for three different values of (V_{ex}).

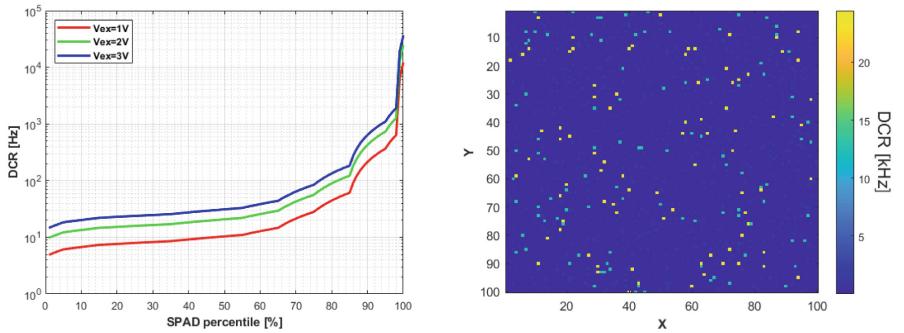


Fig. 3. Synthesized SPAD Dark Count Rate (DCR) and distribution map for the 100 \times 100 pixel array.

The time of arrival of the bucket detector is arbitrarily set at $t = T_{win}/2$, while the number false correlations are extracted by checking whether the generated $T_{int}(x, y)$ for each pixel falls within the interval $(0, T_{win})$. The false trigger $f_{trig}(x, y)$ is given by expression (2):

$$f_{trig}(x, y) = \begin{cases} 1 & 0 < T_{int}(x, y) \leq T_{win} \\ 0 & T_{int}(x, y) > T_{win} \end{cases} \quad (2)$$

The false triggering probability for a given number of simulations (N_{sim}) is defined by Eq. (3). Note that a false trigger is counted only once even if multiple false correlations occur within a single frame.

$$P_{f_{trig}} = \frac{1}{N_{sim}} \sum_{i=1}^{N_{sim}} \left[\left(\sum_{j=1}^{x,y} f_{trig}(x, y) \right) > 0 \right] \quad (3)$$

3.2 Monte Carlo Simulation Results

Figure 4a shows the simulation results for a 100×100 pixels array. The false triggering probability is derived varying T_{win} and V_{ex} .

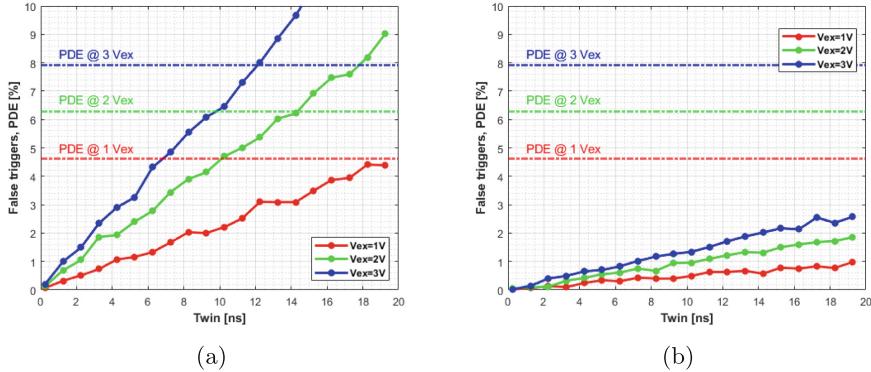


Fig. 4. False triggering probability versus time correlation window width (T_{win}) and SPAD excess bias (V_{ex}) with all pixels activated (a) and 3% of the hot-pixels turned off (b).

When a trigger is obtained from the idler detector, the probability of detecting the photon in the signal path is determined by the Photon Detection Efficiency (PDE). To assess the performance and efficiency, the percentage of false events has to be compared with the detector PDE, which is given by the product of the SPAD Photon Detection Probability (PDP) and the pixel fill-factor. It is crucial that the PDE exceeds the false triggering rate to minimize the additional noise in the reconstructed image. The PDP is determined from previous measurements and corresponds to values of 14%, 19%, and 24% at the wavelength of 600 nm for the three different values of V_{ex} . The simulation results show that the sensor should operate with narrow T_{win} values to reduce the DCR induced false correlations. Moreover, it appears that excessively biasing the SPAD at a large excess bias is not particularly advantageous because the noise effect becomes dominant. Figure 4b shows the effects on the generated number of false correlations when turning off only 3% of the hot pixels. The PDE is higher than the false triggering probability for the entire range of T_{win} values leading to higher signal-to-noise ratio (SNR). This clearly improves the overall quality of the resulting image especially at higher V_{ex} , despite the reduction in the number of active pixels. This effect is shown in Fig. 5, where a ghost image is obtained from 1 M acquisitions, setting T_{win} and V_{ex} to 5 ns and 3 V, respectively. Notably, removing 3% of the noisy pixels does not significantly compromise the overall image quality. Additionally, post-processing techniques, such as pixel substitution using nearest neighbors or interpolation, could be employed to replace the missed information for the deactivated pixels.

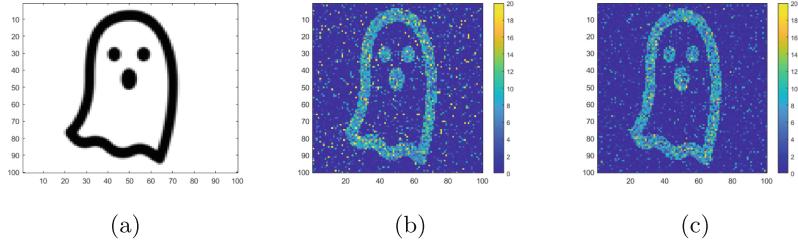


Fig. 5. Simulation of the ghost-imaging experiment with 1 M acquisitions and 5 ns T_{win} . From left to right: (a) original image, (b) all pixels activated, and (c) with 3% of the hot pixels disabled.

Figure 6a shows the variation of the false triggering probability with respect to the total number of pixels of the array considering all pixels activated. For clarity reasons, only the number of pixels along one dimension of the focal plane is reported. The plot shows a worsening of the performance when increasing the sensor size. For example, in a 512×512 -pixel array there is no actual value of T_{win} to be used to keep the false triggering rate below 5%. Furthermore, implementing the necessary in-pixel electronics, which allows precise and uniform T_{win} below 1 ns, represents a challenge for such a large sensor.

Figure 6b shows the achievable improvement in terms of false triggers setting T_{win} and V_{ex} to 5 ns and 1 V respectively, and turning off a certain percentage of hot pixels with respect to the sensor size. The numbers of false triggers is reduced by roughly a factor of 4 by disabling only 3% of the hot-pixels independently from the sensor size. The performance does not improve further by switching off additional hot pixels because the majority of the pixels which contribute to the false correlations have already being disabled. Interestingly, large sensors will always be affected by a higher false detection rate simply due to the larger number of pixels. This can be explained by considering that the medium-noise devices still represent the majority of active pixels within the array.

The simulation results identify the sensor key features to minimize the false triggering probability. A short and precise correlation window T_{win} , high PDE and the capability of disabling noisy pixels are imperative to avoid false detections, especially for large arrays. Additionally, post processing techniques such as pixel interpolation or calibration based on a false detection map may be evaluated to improve the final image quality.

4 Experimental Results and Characterization

The proposed architecture was implemented in a 100×100 -pixel array fabricated in a 110 nm CMOS process as proof of concept. The array integrates two different pixel flavors, exhibiting 17 μm pitch and fill factor between 19% and 31%. In order to perform ghost-imaging at high speed, a zero-suppression readout mechanism allows skipping the empty rows, enabling fast data transfer between

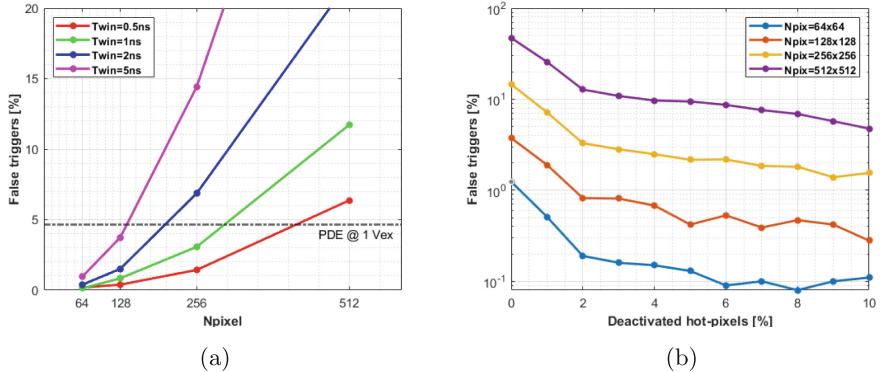


Fig. 6. (a) False triggering probability versus correlation window T_{win} and number of pixels along a single focal-plane dimension. (b) False triggering probability variation with respect to the percentage of disabled hot pixels and different sensor size.

the sensor and the external controller for only the pixels that detected a correlation. When a single row is selected the readout mechanism allows skipping up to 8 pixels for each clock cycle. When analyzing a single triggered pixel, the minimum readout time corresponds to 12.5 μ s, ultimately achieving a maximum sensor readout speed of 80 kframes/s. This capability reduces acquisition time and enhances the sensor duty cycle. Figure 7 shows the chip module and pixels layout.

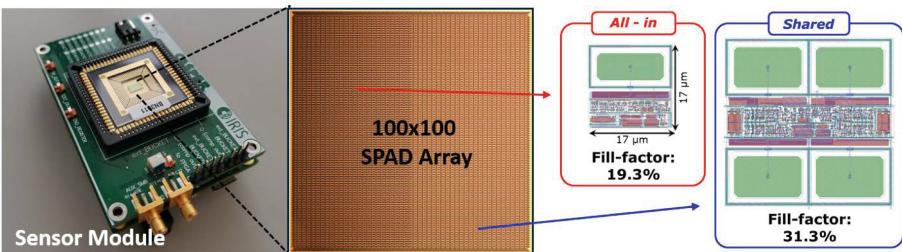


Fig. 7. Chip Module integrating a 100 \times 100 SPAD sensor for quantum ghost imaging (QGI).

The sorted pixel DCR distribution is reported in Fig. 8 showing an average of 720 Hz at 3 V excess bias. As expected, the distribution differs from the one

used in the model, however the number of pixels with DCR higher than 10 kHz are still represented by a few percentage of the total population. A pulsed laser source synchronized with a pulse generator simulating the electrical trigger from the bucket detector has been used to evaluate the false correlations. Figure 8b shows a measured false triggering probability below 3% for a T_{win} equal to 3 ns when all pixels are activated, highlighting the effectiveness of the proposed architecture and an agreement between simulated and measured data trends.

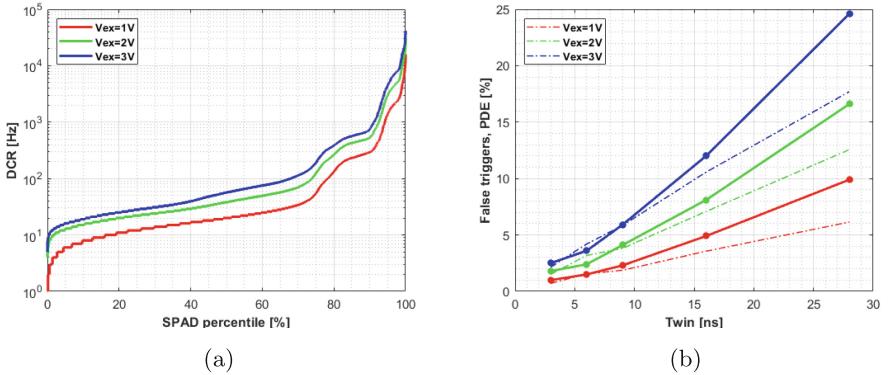


Fig. 8. (a) Measured sorted SPAD distribution. b) Measured (continuous line) versus simulated (dashed line) false triggering probability.

The in-pixel delay mechanism enables bucket delay compensation of up to 40 ns together with a tunable T_{win} ranging from 1.6 to 22.8 ns [7]. Figure 9 depicts the measured spatial distribution and histogram for a short, medium and large value of T_{win} . A fixed delay value T_{delay} equal to 18 ns is used during the characterization. The shortest reported average T_{win} is less than 3 ns with a standard deviation of 0.41 ns throughout the whole array including the bucket delay dispersion. The measurements shows a worsening of the absolute variation for larger T_{win} values which is attributed to the non-uniformity of the transistors due to the process variations and mismatch as well as signaling and biasing voltages distribution within the focal plane array.

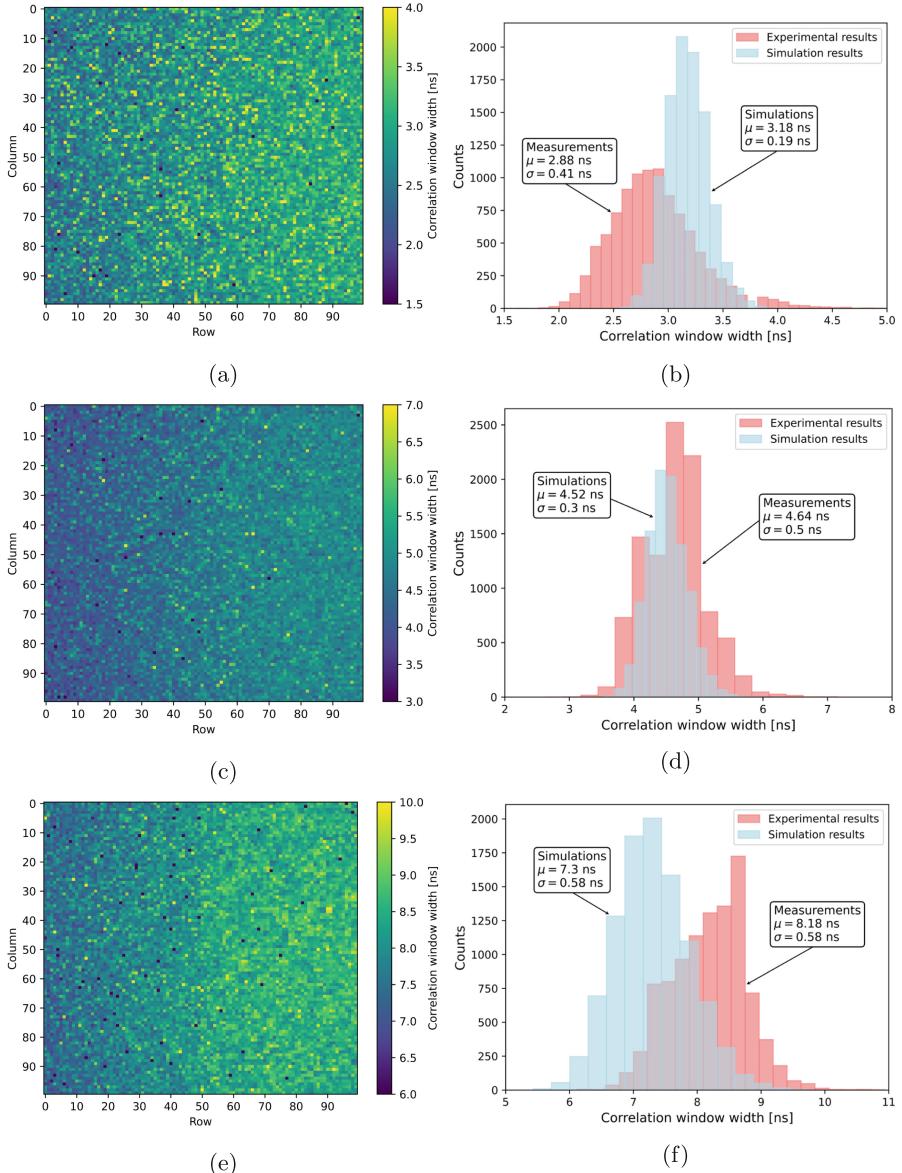


Fig. 9. Spatial distributions and histograms for different values of T_{win} : (a, b) short; (c, d) medium; (e, f) large.

5 Conclusions

A sensor architecture for asynchronous detection of photon pairs in QGI experiments is presented. A Monte Carlo simulation model is developed highlighting

the key features and limitations. A 100×100 SPAD-based sensor for QGI applications is presented and characterized. The prototype demonstrates less than 3% false-event rate and an average correlation window ranging between 3 and 7.8 ns with 0.4 and 0.6 ns standard deviation respectively. A smart zero-suppression readout scheme allows fast QGI up to 80 kframe/s.

References

1. Strekalov, D.V., Sergienko, A.V., Klyshko, D.N., Shih, Y.H.: Observation of two-photon “ghost” interference and diffraction. *Phys. Rev. Lett.* **74**, 3600–3603 (1995). <https://doi.org/10.1103/PhysRevLett.74.3600>
2. Pittman, T.B., et al.: Optical imaging by means of two-photon quantum entanglement. *Phys. Rev. A* **52**, R3429–R3432 (1995). <https://doi.org/10.1103/PhysRevA.52.R3429>
3. Morris, P., Aspden, R., Bell, J., et al.: Imaging with a small number of photons. *Nat. Commun.* **6**(5913) (2015). <https://doi.org/10.1038/ncomms6913>
4. Aspden, R.S., Tasca, D.S., Boyd, R.W., Padgett, M.J.: EPR-based ghost imaging using a single-photon-sensitive camera. *N. J. Phys.* **15**(7) (2013). <https://doi.org/10.1088/1367-2630/15/7/073032>
5. Gili, V.F., et al.: Quantum ghost imaging based on a “looking back” 2D SPAD array. *Appl. Opt.* **62**(12), 3093–3099 (2023). <https://doi.org/10.1364/AO.487084>
6. Pitsch, C., Walter, D., Grosse, S., Brockherde, W., Bürsing, H., Eichhorn, M.: Quantum ghost imaging using asynchronous detection. *Appl. Opt.* **60**(22), F66–F70 (2021). <https://doi.org/10.1364/AO.423634>
7. Gandola, M., et al.: A 100×100 CMOS SPAD array with in-pixel correlation techniques for fast quantum ghost imaging applications. In: IEEE 49th European Solid State Circuits Conference (ESSCIRC), pp. 105–108 (2023). <https://doi.org/10.1109/ESSCIRC59616.2023.10268722>



Pilot Study: Experimental Analysis of PVDF Sensors Response to Slippage

Razan Khalifeh^(✉), Christian Gianoglio, Yahya Abbass, and Maurizio Valle

Department of Electrical, Electronic, Telecommunication Engineering, and Naval Architecture DITEN, University of Genoa, Genoa, Italy

razan.khalifeh@edu.unige.it

Abstract. One of the most important actions in dexterous object manipulation is preventing slippage. Most robotic hands still lack the sense of touch and fail to perceive actions like object slippage. Utilizing a distributed tactile sensing system is crucial for achieving a stable grasp and preventing slippage. This paper presents a tactile sensing system based on PVDF sensors for slippage detection. Frequency analysis was performed to analyze the behavior of PVDF sensors to contact actions including sliding. Results illustrated the efficacy of the sensing system in detecting slippage paving the way for efficient object manipulation.

Keywords: Object manipulation · PVDF sensors · tactile sensing system · slippage

1 Introduction

The human hand can actively grasp objects while regulating force levels with very fast reaction times. Such a performance is achieved by thousands of tactile mechanoreceptors that exhibit a frequency range of up to 1 kHz [1]. Despite the recent advancement in the control of prosthetic hands, the lack of tactile sensation still presents a main challenge. For instance, one of the most important actions that tactile sensing systems encounter is object slippage [2]. Such action is classified as the unstable grasp of an object resulting in the object sliding resulting in high-frequency vibrations [3]. Since it is difficult to manipulate real objects and avoid their slippage, plenty of sensing systems and detection algorithms have been developed to detect slippage. In [4] authors used biomimetic tactile sensors to extract useful tactile information needed for robust robotic grasping and manipulation to prevent slippage phenomena. A method based on estimating the normal and tangential forces that usually happen while manipulating objects was proposed. Another algorithm to detect slippage has been developed in [5], where an ON/OFF signal relating to the presence/absence of slippage has been developed. A 2×2 array of piezoresistive MEMS sensors has

SIE 2024, June 26–28, 2024, Genova, Italy.

© The Author(s), under exclusive license to Springer Nature Switzerland AG 2025
M. Valle et al. (Eds.): SIE 2024, LNEE 1263, pp. 238–243, 2025.
https://doi.org/10.1007/978-3-031-71518-1_27

been used to evaluate the performance of the algorithm. Since distributed tactile information sensing is crucial for the stable grasping and manipulation of intelligent robotics, a flexible tactile sensor array has been developed in [6]. The proposed tactile sensor array has 3×3 sensing units. Another approach which lately attracted the attention of researchers is the Wavelet Transform (WT). For instance, authors in [7] and [8] used piezoresistive sensors combined with rectification methods and Wavelet Transform (WT) respectively to detect slippage. In [9], an initial slip detection method based on wavelet transformation has been proposed. Most of the techniques extracted the high-frequency component of the tactile signals as an indication of slippage. Furthermore, using the discrete wavelet transform analysis, the threshold values of wavelet coefficients have been used in [6] for slip detection. Among tactile sensors, piezoelectric sensors gain attention for detecting sliding in prosthetics [2]. Such sensors are characterized by a frequency bandwidth of 1 Hz–1 kHz which covers the frequency response of the mechanoreceptors in the human skin [10]. For example in [11], authors developed a rigid PVDF-based tactile sensor and power amplifier to detect incident slippage and the static friction coefficient. Table 1 provides an overview of existing literature on slippage detection, detailing the sensors utilized in various studies and their sampling frequencies.

In this paper, we propose a tactile sensing system based on flexible PVDF-based sensing arrays and embedded electronics for sliding detection. The response of the sensing system to contact onsets and sliding was analyzed using the wavelet transform, thus highlighting the capabilities of the proposed sensing system in detecting sliding actions.

Table 1. Comparison of sensor types and their sampling frequencies in the literature.

References	Sensor	Sampling Frequency
[4]	BioTac	300 Hz
[8]	Piezoresistive	380 Hz
[13]	Piezoceramic	500 Hz
[14]	Optical	100 Hz
This work	PVDF	2 kHz

2 Materials and Methods

This section will describe the proposed system that aims to investigate the response of tactile sensing array to 3 different actions. A PVDF sensing array based on piezoelectric materials was used, and a wavelet transform (WT) method was developed to analyze the frequency response of the sensors while applying “Press”, “Sliding” and “Release” actions.

2.1 System Description

Figure 1 presents the block diagram of the system divided into three main blocks. The first block represents the piezoelectric sensing array (e-skin) of 12 sensors. The e-skin generates an electrical signal (one signal per sensor) in response to mechanical stimuli. Sensor signals are acquired, sampled, and sent to the host PC by the embedded electronics (second block). Finally, the third block represents a LabVIEW GUI that was developed to visualize and save the tactile signals.

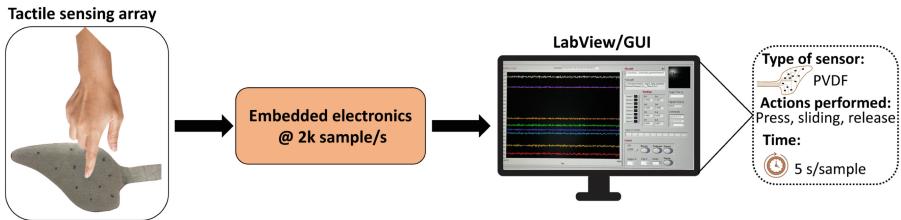


Fig. 1. System setup. The system comprises a tactile sensing array, embedded electronics for signal acquisition and conditioning, and a host PC where LabVIEW software is developed to receive, visualize, and save the tactile signals.

Sensor Array Structure. In this study, a fully screen-printed flexible sensor array based on P(VDF-TrFE) poly(vinylidene fluoride trifluor-oethylene) piezoelectric polymer sensors were used. The fabrication procedure is based on the manufacturing process described in [15]. A bottom electrode is screen-printed on a transparent and flexible (175 μm thick) DIN A4 plastic foil (Melinex® ST 725) substrate. A ferroelectric polymer P(VDF-TrFE) layer (5.1 μm thick) is then screen-printed onto the bottom electrodes, followed by screen printing the top electrodes (Either PEDOT: PSS or carbon have been used). A UV-curable lacquer layer is then deposited on top for overall sensor protection (see Fig. 2). Finally, a poling procedure aligns (in the thickness direction) the randomly oriented dipoles contained in the P(VDF-TrFE) crystallites. The sensing array was shielded using conductive tapes and connected to the embedded electronics using a flat cable.

Embedded Electronics. The embedded electronics used in [16] consists of two main stock devices: BL600 module (Laird Connectivity, US) for Bluetooth connectivity and DDC232 (Texas Instrument, US) current-input analog-to-digital converters that can handle up to 32 sensors. It reads, processes, and transmits the data to the host PC through a USB cable. In this work, the embedded electronics was configured to collect data from 1 sensor at 2 KSamples/s.

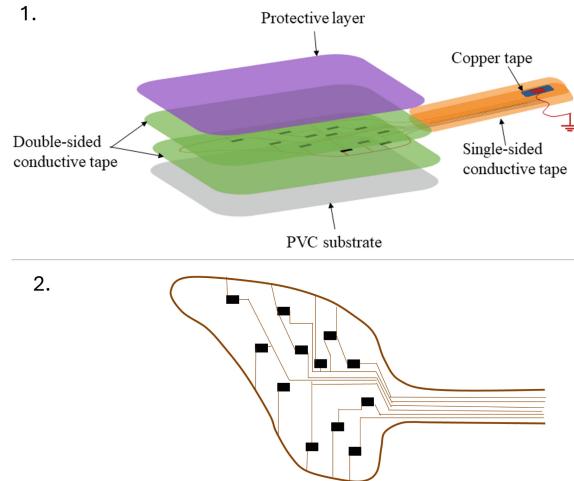


Fig. 2. 1. structure of the skin patch and 2. layout of the skin patch for the palm.

2.2 Experimental Setup

This study aims to analyze the response of the sensing system to 3 different contact actions, ‘Press’, ‘Sliding’, and ‘Release’. A dataset from a PVDF tactile sensing array was collected. Healthy subjects were asked to perform a sequence of touches on the sensing array as shown in Fig. 1, such as “Press”, “Sliding” and “Release”. In particular, the subjects were asked to press on the sensor, slide their finger vertically and horizontally, and finally release their finger. Figure 3a shows the response of the PVDF sensor to the sequence of touch actions. To analyze the response of the sensing system to the touch actions, a wavelet transform (WT) was used to study the frequency component of each action as illustrated in Fig. 3b. Since the slip signals contain high-frequency component characteristics, by using WT, the high-frequency components of the measured signals can be distinguished, and therefore, slippage can be detected.

3 Preliminary Results

Figure 2(b) shows the waveform transform of the response of a single sensor to ‘Press’, ‘Sliding’, and ‘Release’ actions. The sensor’s response to the ‘Press’ and ‘Release’ actions is characterized by a steep increase in the voltage amplitude. This is aligned with the frequency components of such response in which the WT reflects a range of frequencies starting from 1 Hz up to 800 Hz with the highest power at \sim 600 Hz. Unlike the ‘Press’ and ‘Release’ actions, the ‘Sliding’ action results in a wider frequency range reaching 1000 Hz with the highest power at \sim 800 Hz. However, with lower magnitude at the low frequencies. Moreover, it exhibits a frequency spread over time as shown in Fig. 2(b). These findings are

aligned with the fact that slippage exhibits a high-frequency component making PVDF sensors an ideal candidate for slippage detection.

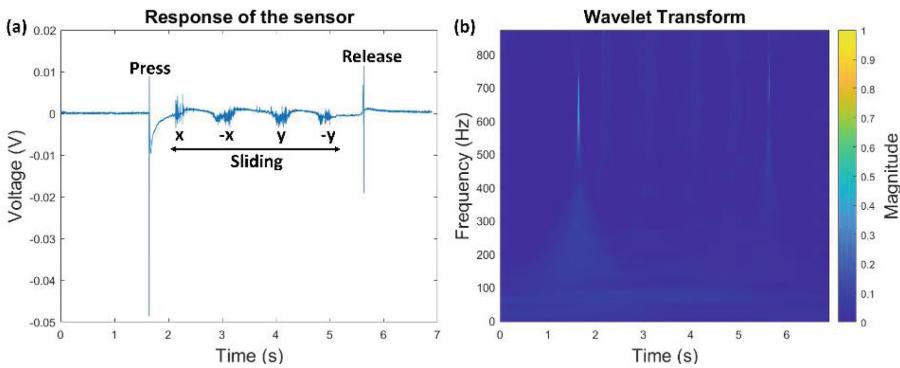


Fig. 3. (a) response of the sensor, (b) wavelet of the actions performed.

4 Conclusion and Future Work

In this study, we proposed a tactile sensing system for touch and slippage detection. The system is composed of flexible PVDF-based sensing arrays and embedded electronics. We analyzed the response of the sensor to touch and sliding action using the wavelet transform. Results showed that the sliding actions exhibit high-frequency components up to 1000 Hz with lower magnitude at low frequencies. The findings of this study pave the way for an effective sensing system for robotic hands that is capable of detecting slippage and maintaining object grasp.

References

1. Johansson, R.S., Westling, G.: Signals in tactile afferents from the fingers eliciting adaptive motor responses during precision grip. *Exp. Brain Res.* **66**, 141–154 (1987)
2. Romeo, R.A., Zollo, L.: Methods and sensors for slip detection in robotics: a survey. *IEEE Access* **8**, 73027–73050 (2020)
3. Srinivasan, M.A., Whitehouse, J.M., LaMotte, R.H.: Tactile detection of slip: surface microgeometry and peripheral neural codes. *J. Neurophysiol.* **63**(6), 1323–1332 (1990)
4. Su, Z., et al.: Force estimation and slip detection/classification for grip control using a biomimetic tactile sensor. In: 2015 IEEE-RAS 15th International Conference on Humanoid Robots (Humanoids), pp. 297–303. IEEE (2015)
5. Romeo, R.A., Oddo, C.M., Carrozza, M.C., Guglielmelli, E., Zollo, L.: Slippage detection with piezoresistive tactile sensors. *Sensors* **17**(8), 1844 (2017)

6. Wang, Y., Wu, X., Mei, D., Zhu, L., Chen, J.: Flexible tactile sensor array for distributed tactile sensing and slip detection in robotic hand grasping. *Sens. Actuat. A* **297**, 111512 (2019)
7. Romeo, R.A., Lauretti, C., Gentile, C., Guglielmelli, E., Zollo, L.: Method for automatic slippage detection with tactile sensors embedded in prosthetic hands. *IEEE Trans. Med. Robot. Bionics* **3**(2), 485–497 (2021)
8. Romeo, R.A., et al.: Identification of slippage on naturalistic surfaces via wavelet transform of tactile signals. *IEEE Sens. J.* **19**(4), 1260–1268 (2018)
9. Zhang, Y., Duan, X.G., Zhong, G., Deng, H.: Initial slip detection and its application in biomimetic robotic hands. *IEEE Sens. J.* **16**(19), 7073–7080 (2016)
10. Dahiya, R.S., Metta, G., Valle, M., Sandini, G.: Tactile sensing—from humans to humanoids. *IEEE Trans. Rob.* **26**(1), 1–20 (2009)
11. Chuang, C.H., Liou, Y.R., Chen, C.W.: Detection system of incident slippage and friction coefficient based on a flexible tactile sensor with structural electrodes. *Sens. Actuat. A* **188**, 48–55 (2012)
12. Fares, H., Abbass, Y., Valle, M., Seminara, L.: Validation of screen-printed electronic skin based on piezoelectric polymer sensors. *Sensors* **20**(4), 1160 (2020)
13. Dario, P., Lazzarini, R., Magni, R., Oh, S.R.: An integrated miniature fingertip sensor. In: MHS 1996 Proceedings of the Seventh International Symposium on Micro Machine and Human Science, pp. 91–97. IEEE (1996)
14. Jiang, C., Zhang, Z., Pan, J., Wang, Y., Zhang, L., Tong, L.: Finger-skin-inspired flexible optical sensor for force sensing and slip detection in robotic grasping. *Adv. Mater. Technol.* **6**(10), 2100285 (2021)
15. Zirkl, M., et al.: An all-printed ferroelectric active matrix sensor network based on only five functional materials forming a touchless control interface. *Adv. Mater.* **23**(18), 2069 (2011)
16. Saleh, M., Abbass, Y., Valle, M.: Embedded implementation of signal pre-processing for tactile sensing system. In: International Conference on System-Integrated Intelligence, pp. 727–736. Springer, Cham (2022)



Stability and Functionalization of Carbon Nanotube Electrolyte-Gated Field-Effect Transistors

Anna Tagliaferri^{1,2}(✉) , Bajramshahe Shkodra¹ , Martina Aurora Costa Angeli¹ , Moritz Ploner¹ , Mattia Petrelli¹ , Antonio Altana^{1,3} , Pietro Ibba¹ , Paolo Lugli^{1,3} , and Luisa Petti¹

¹ Sensing Technologies Laboratory (STL), Faculty of Engineering,
Free University of Bozen-Bolzano, 39100 Bolzano, Italy
atagliaferri@unibz.it

² Faculty of Agricultural, Environmental and Food Sciences,
Free University of Bozen-Bolzano, 39100 Bolzano, Italy

³ Competence Center for Mountain Innovation Ecosystems,
Free University of Bozen-Bolzano, 39100 Bolzano, Italy

Abstract. Electrolyte-gated carbon-nanotube field-effect transistor-based biosensors often face stability and functionalization challenges. This paper addresses stability by introducing a lipophilic membrane on the channel: this leads to reduced stabilization times, down to 34 min, and to enhance the sensor performance and functionality up to 12 h and 5 repeated uses. In addition, the gate is separated from source and drain, to enable cleaning and gate functionalization with aptamers and polyethylene glycol. This approach allows to replace the gate, while still maintaining the same source and drain electrodes; this ultimately reduces cost and environmental impact.

Keywords: Carbon nanotubes · Biosensor · Lipophilic membrane

1 Introduction

Electrolyte-gated field-effect transistors (EG-FETs) are innovative devices compatible with biological systems thanks to the presence of the electrolyte; this encourages their application in biosensors for health, food, and environmental monitoring [1–3], including the possibility to use them in wearable devices [4]. When a voltage is applied to the gate, an electric field is generated, causing the movement of anions and cations in solution toward their oppositely charged poles, i.e., the gate and semiconductor channel; the accumulated charges thus form two parallel electric double layers that effectively shield the gate from the semiconductor, mimicking dielectric behavior [5]. Moreover, electrolytes, such as phosphate buffer saline (PBS), have higher relative permittivity than metal oxides, resulting in increased capacitance and consequent signal amplification,

all the while working at low voltages [6–8]. Carbon nanotubes (CNTs) emerged as EG-FET semiconductor owing to high carrier mobility and flexibility, driving the development of EG-CNTFET-based biosensors [6]. In addition to the EG-CNTFET signal transducer, biosensors require a biorecognition element, e.g., antibodies and aptamers, for analyte selectivity; these can be attached exploiting various strategies, including binding to CNTs, both via covalent and non-covalent bonds, or to the gate, often comprising thiol-gold chemistry [6].

This paper addresses ongoing challenges regarding the stability and functionalization of EG-CNTFETs: We propose a rapid and cost-effective solution by encapsulating the single-walled carbon nanotube (SWCNT) channel with a lipophilic membrane, to enhance their resilience to environmental and electrical stresses, and to reduce the stabilization time to 34 min, i.e., half of the state-of-the-art [9]. The challenge of functionalization emerges from our work with planar EG-CNTFETs, where the aim is to functionalize the gate; the issue found here is that the surface of the transistors is susceptible to carbon contamination, which prevents covalent bond formation. However, chemically cleaning the gate is non-trivial as harsh agents pose the risk of delamination; similarly, post-SWCNT deposition cleaning of the device with ozone or oxygen plasma is detrimental to the channel integrity. The solution theorized in this work is to use an external gate in conjunction with the encapsulated IDEs; this way, the gate can be cleaned by means of oxygen plasma without structural damage and functionalized separately not to disrupt the SWCNT network. This simple approach allows to reuse the IDEs multiple times, interchanging the gate, with the prospect of less wasteful and more cost-effective electronics.

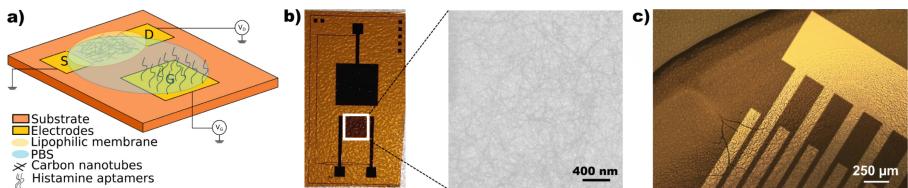


Fig. 1. a) Scheme of EG-CNTFET-based biosensor. b) EG-CNTFET and SEM micrograph of the random network of SWCNTs. c) Close-up image of the membrane.

2 Materials and Methods

EG-FETs were fabricated on a flexible 150 μm polyimide (PI) substrate using a planar geometry with interdigitated electrodes (IDEs). The fabrication was carried out in a single-step process of negative photolithography followed by the deposition of 10 nm of titanium and 50 nm of gold for the IDEs and planar gate. Semiconducting SWCNTs were then spray-coated in the IDEs region,

following the protocol developed by [10]. A water-based ink containing SWCNTs, prepared with carboxymethyl cellulose as a surfactant, was sprayed using a shadow mask to protect the electrodes. Sixty layers of the dispersion were deposited to achieve the desired SWCNT density, followed by acid treatment to remove the surfactant (60 min in 2.90M nitric acid, followed by 30 min in diH₂O, then drying on a hot plate for 30 min). A lipophilic membrane was drop-casted on the sprayed area to protect the SWCNTs from degradation; the membrane was prepared according to the protocol in [11], containing 5% tetradodecylammonium tetrakis(4-chlorophenyl) borate, 32.3% poly(vinyl chloride), and 62.7% plasticizer dioctyl sebacate. The membrane was applied in two phases, dropcasting respectively 8 µL and 7 µL, allowing 30 min between each layer for solvent evaporation and drying. Functionalization was performed by incubating the gate electrode with 5 µM histamine thiolated aptamers diluted in 1x PBS for 2 h, followed by rinsing it three times with 1x PBS. This was then followed by a 2-h incubation in 500 µM thiolated polyethylene glycol (PEG), another three rinses with 1x PBS, and an overnight incubation in 1x PBS. PEG is necessary as blocking agent, in order to prevent any specific binding on the surface that could lead to altered measurements.

Morphological characterization was used to preliminarily determine the quality of the fabricated devices: scanning electron microscopy (SEM, JSM-IT 100, JEOL, Japan) operating at an accelerating voltage of 3 V, with a working distance of 8 mm was used to monitor the SWCNT morphology (Fig. 1b), and the membrane thickness was characterized with a KLA Tencor P-6 Surface Profilometer.

Electrical characterization was carried out to investigate the performance of the devices. Resistance between the drain and source (R_{DS}) was measured with a semiconductor device parameter analyzer, selecting devices with R_{DS} between 1 and 10 kΩ to ensure optimal EG-CNTFET functionality and to reduce device-to-device variability. The resistance was then re-measured after membrane deposition. To ensure coverage of the electrodes with 1x phosphate buffer saline (PBS), a custom polyethylene chamber was mounted on the substrate. Device performance and stability were then evaluated by collecting transfer characteristics with 200 µL of 1x PBS in the chamber. Transfer curves were recorded by sweeping the gate voltage (V_{GS}) from 0.2 V to -0.8 V for different time intervals, with the drain voltage (V_{DS}) fixed at -0.1 V. Further electrical characterization of the gate functionalization steps included cyclic voltammetry (CV) measurements: the potential was swept from -0.4 V to +0.6 V with a scan rate of 0.1 V. All measurements were conducted at room temperature and in air.

Chemical characterization of the gate surface was conducted by X-ray photoelectron spectroscopy (XPS), employing a Omicron Nanotechnology Multiprobe UHV-surface-analysis system equipped with a AlKα source (1486.7 eV).

3 Results

Initial morphological characterization revealed a dense, uniformly dispersed random network of SWCNTs, as seen in Fig. 1b. The membrane was later character-

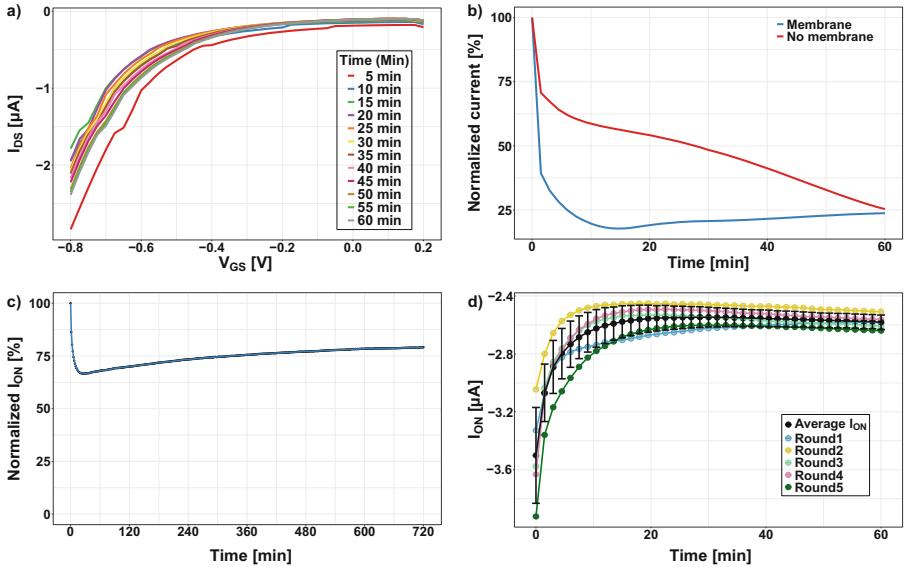


Fig. 2. Evaluation of EG-CNTFET stability through electrical characterization. a) Transfer characteristics of a device with membrane encapsulation: the current increases after each curve collected. b) Normalized I_{ON} : the device with bare SWCNTs shows a steep linear decrease of current over time, whereas the device with membrane encapsulation exhibits a big drop in the very beginning, after which a linear increase is evident starting from approximately 30 min. c) Stability testing over 12 h: the devices with membrane encapsulation withstand electrical stress for a prolonged time, while maintaining comparable performance to shorter measurements. d) Repeated measurements on a single device: the performance shows very little variation over the 5 measurements taken, with less than 2% variability after the 30 min required for stabilization.

ized and an optimal membrane thickness of 45 μm was identified after thorough and careful testing; it was in fact necessary to entirely cover the SWCNTs while not hindering charge transport within the network. It is noteworthy that the membrane dried remaining transparent, leaving the interdigitated electrodes visible underneath it, as seen in Fig. 1c.

A preliminary electrical characterization showed that membrane deposition caused an R_{DS} increase from $2.25 \pm 0.94 \text{ k}\Omega$ to $24.63 \pm 7.95 \text{ k}\Omega$, due to its insulating nature. Stability was evaluated by first collecting transfer curves (Fig. 2a) as explained in the previous section, then extracting the ON current (I_{ON}), *i.e.* the drain current (I_{DS}) measured at $V_{GS} = -0.8 \text{ V}$, over time (Fig. 2b): with membrane encapsulation, I_{ON} decreased at first during the so-called “stabilization phase” [12], followed by a linear increase of 11 nA/min (“constant slope phase”); during the former phase, the electrical double layer (EDL) forms, albeit slow due to the presence of the membrane. Once the EDL is established, the system is at a newfound equilibrium and the current starts rising again. On the other hand, devices without the membrane showed a linear decrease of

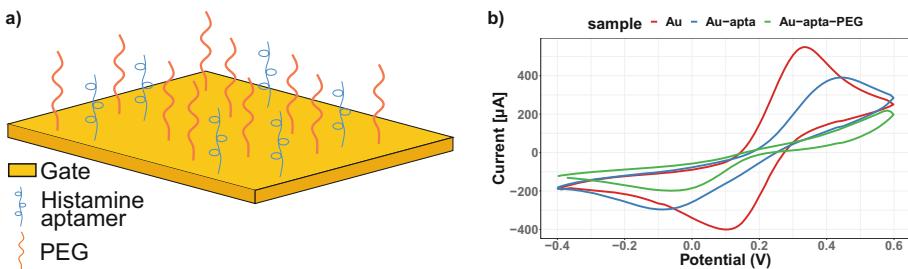


Fig. 3. Gate functionalization. a) Schematics of gate functionalized with histamine thiolated aptamers (in blue) and thiolated PEG (in orange). b) Cyclic voltammogram of functionalization steps: the peak shifts in position and diminishes in intensity as the surface gets progressively covered by aptamers and PEG.

710 nA/min [13]. This continuous, rapid decrease in I_{DS} for the bare devices is rooted in SWCNTs degradation upon contact with air and electrolyte. To further test stability and resilience of the devices with encapsulated channel, they were subjected to prolonged and repeated electrical stress, namely collecting transfer characteristics over 12 h and repeating the 1 h test 5 times on each device. Testing them over 12 h (Fig. 1c) indicated that they are able to maintain increasing current levels, still maintaining high linearity of I_{ON} over time, as highlighted by the coefficient of determination of 0.97. The repeated measurements (Fig. 2d) also showed a positive outcome, with high reproducibility among each round: the variability among the five measurements is in fact lower than 2% already after the 30 min necessary for the stabilization determined above, indicating that they can be reliably used multiple times [14].

Once the stability issue was settled, it was necessary to proceed with gate functionalization. XPS analyses showed that electrode functionalization was initially hindered by 42% carbon contamination. Cleaning planar EG-CNTFETs, however, proved difficult due to the thin electrode thickness and previously deposited CNTs: harsh chemicals, such as modified, milder versions of piranha solution, caused the gate to delaminate, while ozone or oxygen plasma cleaning damaged the SWCNTs, even with the protection of the lipophilic membrane. Our solution proposes to separate the gate from the IDEs. The introduction of an extended gate allowed electrode cleaning with oxygen plasma before functionalization with aptamers and PEG (a schematics of the functionalization result is visible in Fig. 3a). XPS indicated that this process reduced carbon contamination to 18%. Figure 3b shows how this strategy lead to aptamer attachment: the CV plot ($N = 5$) shows distinct shape and intensity for the bare gold electrode, displaying decreased intensity and peak shifts after aptamer and PEG deposition (blocking agent), indicating reduced surface area for electron transfer. Ultimately, the complete coverage of the electrode by PEG prevented further electrochemical activity, resulting in peak disappearance [15]. It is noteworthy that the extended gate strategy allows easy replacement of the sensor recognition component by exchanging the gate, while reusing the signal transduction

component (IDEs). This not only reduces fabrication costs but also minimizes waste generation.

4 Conclusion

This work highlights fabrication challenges of EG-CNTFETs for biosensing purposes and proposes solutions to overcome them. Firstly, SWCNT instability was tackled by encapsulating the channel in a lipophilic membrane, leading to stabilization in 34 min, that is a twofold improvement over state-of-the-art devices, and increased resilience, allowing measurements up to 12 h with a performance comparable to shorter measurements, and 5 distinct rounds of collection of 40 consecutive transfers with very little variability already at 30 min, *i.e.* the time necessary for stabilization. Secondly, carbon contamination of the Au electrode precluded functionalization, which was solved by decoupling the electrode from the IDEs, cleaning it separately with oxygen plasma for 5 min.

References

1. Pullano, S.A., et al.: EGFET-based sensors for bioanalytical applications: a review. *Sensors* **18**(11), 4042 (2018)
2. Bobrinetskiy, I., et al.: Advances in nanomaterials-based electrochemical biosensors for foodborne pathogen detection. *Nanomater. (Basel Switz.)* **11**(10), 2700 (2021)
3. Elli, G., et al.: Field-effect transistor-based biosensors for environmental and agricultural monitoring. *Sensors* **22**(11) (2022)
4. Petrelli, M., et al.: Flexible sensor and readout circuitry for continuous ion sensing in sweat. *IEEE Sens. Lett.* **7**(6), 1 (2023)
5. Torricelli, F., et al.: Electrolyte-gated transistors for enhanced performance bioelectronics. *Nat. Rev. Methods Primers* **1**(1), 66 (2021)
6. Shkodra, B., et al.: Electrolyte-gated carbon nanotube field-effect transistor-based biosensors: principles and applications. *Appl. Phys. Rev.* **8**(4), 041325 (2021)
7. Velický, M.: Electrolyte versus dielectric gating of two-dimensional materials. *J. Phys. Chem. C* **125**(40), 21803 (2021)
8. Bertolazzi, E., Frego, M.: A note on robust biarc computation. *Comput.-Aided Design Appl.* **16**(5) (2019)
9. Molazemhosseini, A., Viola, F.A., Berger, F.J., Zorn, N.F., Zaumseil, J., Caironi, M.: A rapidly stabilizing water-gated field-effect transistor based on printed single-walled carbon nanotubes for biosensing applications. *ACS Appl. Electron. Mater.* **3**(7), 3106 (2021)
10. Shkodra, B., Petrelli, M., Angeli, M.A.C., Inam, A.S., Lugli, P., Petti, L.: Optimization of the spray-deposited carbon nanotube semiconducting channel for electrolyte-gated field-effect transistor-based biosensing applications. *IEEE Sens. J.* (2022)
11. Joshi, S., et al.: Using lipophilic membrane for enhanced-performance aqueous gated carbon nanotube field effect transistors. *Phys. Status Solidi (A)* **215**(11), 1700993 (2018)
12. Petrelli, M., et al.: Method for instability compensation and detection of ammonium in sweat via conformal electrolyte-gated field-effect transistors. *Organic Electron.* **122** (2023)

13. Tagliaferri, A., et al.: In: 2023 IEEE BioSensors Conference (BioSensors), pp. 1–4. IEEE (2023)
14. Tagliaferri, A., et al.: Manuscript submitted for publication (2024)
15. Koterwa, A., et al.: An electrochemical biosensor for the determination of hormone human chorionic gonadotropin (HCG) in human serum. *Electroanalysis* **35**(11), e202300095 (2023)



Stress Transmission in a Soft Electronic Skin with Viscoelastic Properties

Chiara Micheli¹(✉), Giovanni Berselli², and Lucia Seminara¹

¹ DITEN, University of Genova, 16145 Genoa, Italy

chiara.micheli@edu.unige.it, lucia.seminara@unige.it

² DIME, University of Genova, 16145 Genoa, Italy

giovanni.berselli@unige.it

Abstract. Soft skin interfaces enhance haptic interactions. We focus on a soft electronic skin integrating PVDF (polyvinylidene fluoride tetrafluoroethylene) piezoelectric polymer transducers. Previous research revealed the PVDF's output signal dependence on grasping speed, suggesting a viscoelastic mechanical behavior that the soft layer could influence, too. Through finite element analysis (FEA), we explore how the viscoelastic properties of the soft protective layer of an electronic skin affect stress transmission to the PVDF piezoelectric transducers below.

Keywords: Soft tactile sensors · Viscoelasticity · PVDF transducers

1 Introduction

The sense of touch is crucial for human interaction with the environment. Insights from human tactile sensing and haptic perception guide the development of artificial haptic systems, aiming to replicate the versatility of human touch. These systems need to manage spatially distributed and time-varying contact information [1, 2]. Advanced sensing solutions, inspired by biomimicry, include soft interfaces with integrated transducers. Here, we present an electronic skin (e-skin) based on PVDF transducers, integrated on a rigid substrate and covered by a soft silicone layer. In a previous study [3], we demonstrated that the grasping speed influenced the output signal of PVDF transducers covered by a soft protective layer. This suggested a viscoelastic behavior that may be mainly attributed to the soft protective layer. Indeed, we neglect the loss component of the PVDF, as it was proved that the imaginary part of the relevant piezoelectric coefficient for the thickness-mode operation was negligible over the explored frequency range [1 Hz–1 kHz] [4].

In this publication, we investigate through a novel finite element analysis (FEA) how the viscoelastic behavior of the soft cover affects the stress transmission to PVDF transducers placed below.

2 Materials and Methods

The design of our sensing patch (see Fig. 1a) entails a rigid substrate, an array of PVDF piezoelectric polymer transducers (see [5] for the fabrication process), and a soft silicone layer on top. In this configuration, PVDF transducers directly transform the received pressure (specifically, the average normal stress \bar{T}_3) into an electrical signal, specifically a charge (Q) [6], such that [7]:

$$Q = d_{33}\bar{T}_3\pi r_t^2 \quad (1)$$

where, d_{33} is the piezoelectric coefficient and r_t is the transducer radius.

The total charge Q on the sensor surface is converted into an output voltage signal through an interface electronics based on charge amplifiers [8] (see Fig. 1b).

Figure 2 shows the Printed Circuit Board (PCB) and the interface electronics design block diagram. The circuit incorporates two primary off-the-shelf components: the BL600 module (Laird Connectivity, US) for Bluetooth connectivity and the DDC232 (Texas Instruments, US) current-input analog-to-digital converter. The PCB is equipped with digital integrated circuits for power management (e.g., voltage regulator) and a USB interface for data transfer (e.g., FTDI232). The design supports up to 32 sensors via two sockets, each with 16 input channels. Both sockets are connected to an offset circuit to adjust the baseline of the bipolar signals generated by the sensors, enabling the DDC232 to process both positive and negative signal polarities. The DDC232 chip includes multiple current-to-voltage integrators and delta-sigma analog-to-digital converters. It is configured for 16-bit resolution and covers the maximum input charge response. The device architecture allows for simultaneous sampling of the 32 input channels with a configurable sampling rate of up to 6 kHz. Data acquired by the DDC232 is transmitted to the BL600 module via UART. The BL600 features an ultra-low-power microcontroller based on an ARM Cortex M0 chip, which reads, processes, and transmits the sensor data. The USB connection powers the PCB and provides a serial interface for data transfer across the system [9]. The interface electronics has been preliminary validated in [8].

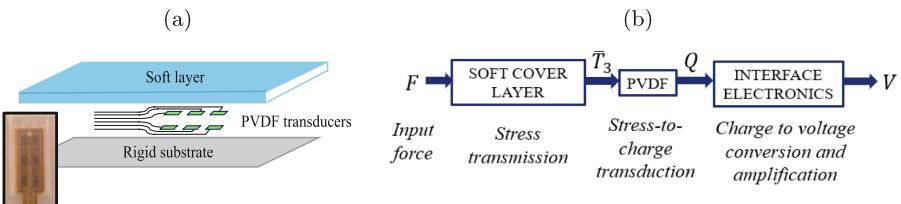


Fig. 1. (a) Illustrative picture of the sensing patch; (b) block diagram of the whole sensing system.

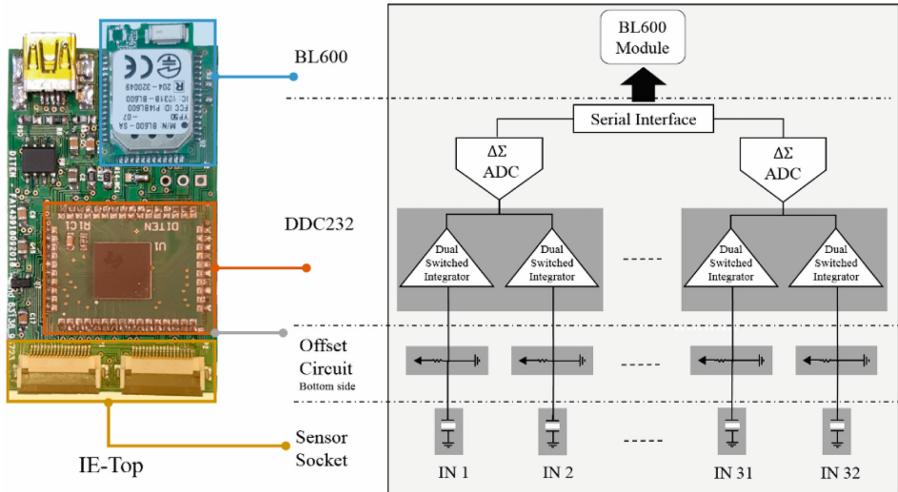


Fig. 2. Interface electronics [8].

In [3] for the first time, a soft protective layer was applied to our PVDF transducer array. A soft interface is beneficial for safety and sensor protection, allowing the soft skin to better conform to surfaces and objects.

In the present work, the silicone-based soft skin is made of *dragon skin*, a widely used material in robotics [10]. The Dragon Skin (Dragon Skin 10 Medium, Smooth-On) material is chosen for several reasons. It is easily disposable and involves a straightforward fabrication process, including preparation, pouring, and catalyzation. The material elastic and hyperelastic properties are well-documented, which facilitates FEM simulations and analysis. Furthermore, Dragon Skin offers a softness similar to human skin, making it an ideal choice for this application.

Stress-strain curves exhibit significant variability with the indentation velocity [11], suggesting a viscoelastic behavior. In the absence of a proper characterization of such viscoelasticity, we use the viscoelastic characterization of the human skin [12], which has similar mechanical properties. Here, we investigate how this viscoelastic component would affect the transmission of normal stress to the PVDF transducers below. We perform Finite Elements Model (FEM) simulations consisting of indentations at different velocities and forces, employing a rigid indenter acting on the outer skin surface and generating a normal force distribution modelled as Hertzian. We study stress transmission through the soft cover layer and compute the average normal stress \bar{T}_3 on the bottom of such layer (where transducers are located) as a function of force and velocity of the applied stimulus on the outer surface. The e-skin soft layer fills a spatial region shaped like a cylinder, with a diameter d and height h ($= 2$ mm), where d significantly exceeds the radii of both the transducer ($r_t = 1$ mm) and the indenter ($R = 4$ mm). The silicone-based soft layer is modeled both as an elastic material (dragon

skin with $E=152$ kPa) as introduced in [10] and as viscoelastic, with the stress relaxation parameters of the Prony series $g_1 = 0.148$, $g_2 = 0.252$ (relative moduli - viscoelastic components), $\tau_1 = 2.123$ and $\tau_2 = 9.371$ (relaxation times) [12]. A fixed support is positioned at the bottom surface of the soft layer, serving as the rigid substrate to prevent any translation and rotation. A preload of 1 N is applied, followed by an increasing displacement. The indentation velocity is varied between 0.1 and 10 mm/s. The software chosen for the simulations is ANSYS Workbench 2019 R3. A 2D axisymmetric configuration is adopted to reduce the computational time, assuming a perfect alignment between the indenter and the transducer. PLANE183 is the element used to mesh the model. CONTA172 and SURF153 are the elements chosen for the frictionless contact between the indenter and the soft layer. The 2D model was meshed in 9587 nodes and 3596 elements. The processor used to perform the simulations was Intel®Core™ i9-9900K, CPU @ 3.60 GHz, with a 32.0 GB RAM. The computational time for a single simulation is 14 min. The meshed model is shown in Fig. 3. The normal indentation force is aligned with the y axis and it has a negative sign when the indenter is pressed on the e-skin. In the software, the PVDF transducer is not modeled as a piezoelectric material but instead it is represented as a line (a path), as long as the taxel radius and axially aligned with the indenter (see Fig. 3).

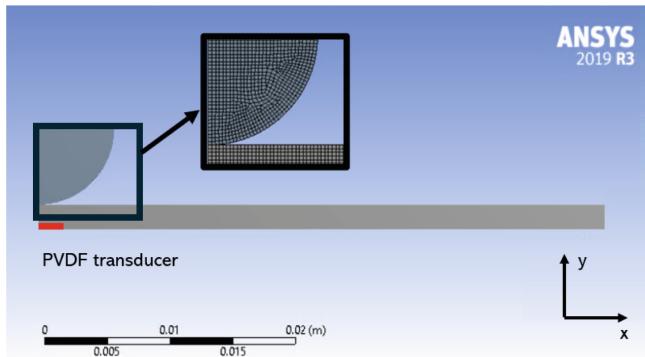


Fig. 3. FEM design showing the chosen mesh.

3 Results

In an indentation experiment, the contact force increases up to a maximum (press phase) and then returns to zero (release phase). Figure 4a depicts the total deformation of the soft protective layer under indentation. It can be observed that the maximum deformation occurs at the center of the contact area resulting from the indenter touching the soft layer. In Fig. 4b, the contact pressure is plotted at the

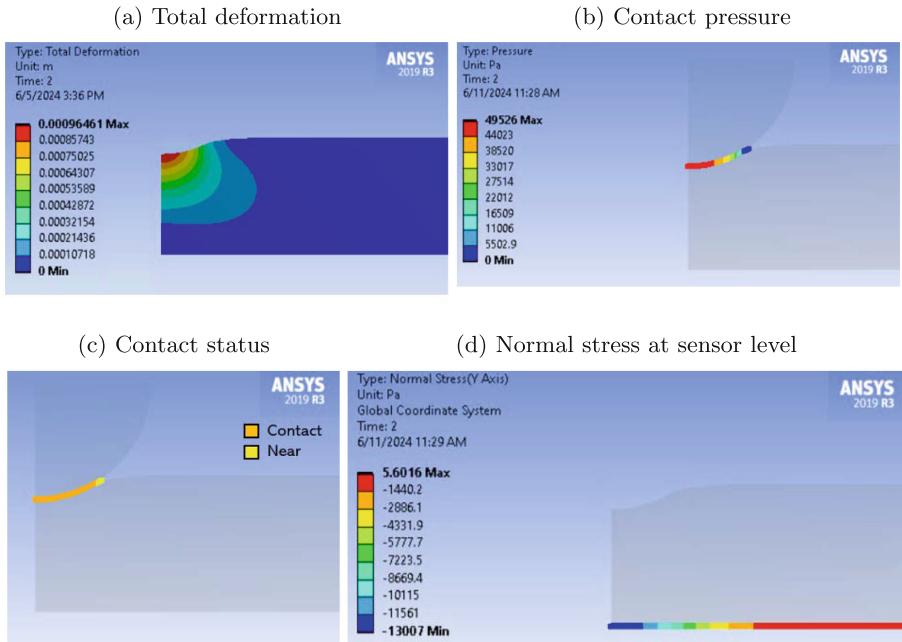


Fig. 4. Example of FEM results on Ansys: the total deformation of the protective layer [m] (a), the contact pressure [Pa] (b), the contact status (c) and the normal stress (namely T_3) at the transducer level [Pa] (d).

contact profile, while Fig. 4c highlights the contact state (contact/no contact) between the indenter and the soft protective layer. Lastly, Fig. 4d displays the normal stress T_3 at the transducer level, which is positioned at the bottom of the protective layer. For normal forces, it is evident that the maximum stress at the transducer level coincides with the projection of the indenter axis on the bottom plane. This suggests that if there was another transducer (as in the actual scenario where the e-skin comprises multiple transducers), not aligned with the indenter, it would be capable of detecting the contact happening nearby.

Figure 5 shows the electronic skin stimulus and the simulated input of the PVDF (\bar{T}_3) over time. The former represents the displacement applied on the skin outer surface, the latter is the result of the stress transmission analysis performed by FEM simulations. The \bar{T}_3 is computed as an average of the normal stress on the path representing the PVDF.

In Fig. 6, the maximum value of the \bar{T}_3 profile calculated through FEM for indentation at fixed force (1 N) and different velocities is plotted, with a dashed line representing the result for a purely elastic material. It can be observed that, as the velocity increases, the maximum value of the \bar{T}_3 profile also increases. At our highest velocities (i.e. 10 mm/s), the result approaches the purely elastic material characterization.

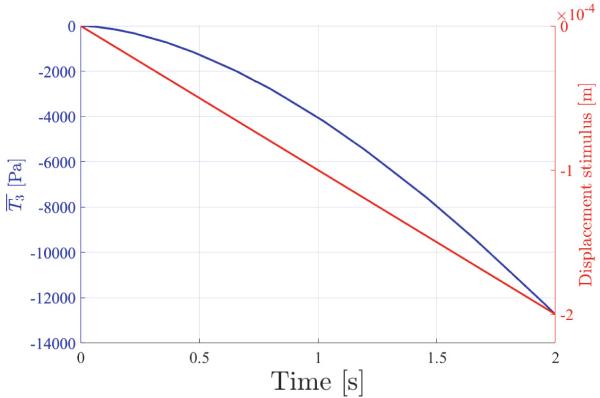


Fig. 5. Stimulus of the electronic skin (displacement) and input of the PVDF (\overline{T}_3) vs the indentation time.

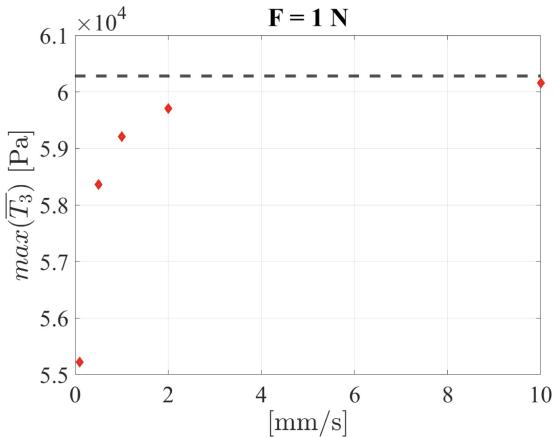


Fig. 6. The maximum value of the \overline{T}_3 profile is plotted as a function of the indentation velocity (viscoelastic characterization). The dashed line represents the elastic characterization.

4 Conclusion and Future Steps

These results can be regarded as the first step towards interpreting the velocity dependence of sensor outputs. However, it will be necessary to investigate the potential viscoelastic piezoelectric behavior of PVDF transducers at frequencies below 1 Hz, as the employed velocities in this study all correspond to frequencies in that range. Furthermore, the next step will be to characterize the viscoelastic components of the Dragon Skin, to correctly estimate the viscoelastic influence of the soft protective layer on stress transmission through the layer and on the output signals of the e-skin.

Acknowledgment. This work was supported by AI-Powered Manipulation System for Advanced Robotic Service, Manufacturing and Prosthetics (IntelliMan) project EU H2022 under Grant 101070136.

References

1. Johansson, R.S., Flanagan, J.R.: Coding and use of tactile signals from the fingertips in object manipulation tasks. *Nat. Rev. Neurosci.* **10**(5), 345–359 (2009)
2. Delhaye, B.P., Long, K.H., Bensmaia, S.J.: Neural basis of touch and proprioception in primate cortex. *Compr. Physiol.* **8**(4), 1575 (2018)
3. Micheli, C., Abbass, Y., Gianoglio, C., Seminara, L.: A pilot study: electronic skin sensitive to the grasping speed. In: 2023 18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME), pp. 305–308 (2023)
4. Seminara, L., Capurro, M., Cirillo, P., Cannata, G., Valle, M.: Electromechanical characterization of piezoelectric PVDF polymer films for tactile sensors in robotics applications. *Sens. Actuat. A* **169**(1), 49–58 (2011)
5. Fares, H., Abbass, Y., Valle, M., Seminara, L.: Validation of screen-printed electronic skin based on piezoelectric polymer sensors. *Sensors* **20**(4), 1160 (2020)
6. Seminara, L.: Modeling electronic skin response to normal distributed force. *Sensors* **18**(2), 459 (2018)
7. IEEE Standard on Piezoelectricity. ANSI/IEEE Std 176-1987, pp. i–66 (1988)
8. Saleh, M., Abbass, Y., Ibrahim, A., Valle, M.: Experimental assessment of the interface electronic system for PVDF-based piezoelectric tactile sensors. *Sensors* **19**(20), 4437 (2019)
9. Abbass, Y., Saleh, M., Dosen, S., Valle, M.: Embedded electrotactile feedback system for hand prostheses using matrix electrode and electronic skin. *IEEE Trans. Biomed. Circuits Syst.* **15**(5), 912–925 (2021)
10. Massari, L., et al.: Functional mimicry of Ruffini receptors with fibre Bragg gratings and deep neural networks enables a bio-inspired large-area tactile-sensitive skin. *Nat. Mach. Intell.* **4**(5), 425–435 (2022)
11. Tramacere, F., Kovalev, A., Kleinteich, T., Gorb, S.N., Mazzolai, B.: Structure and mechanical properties of octopus vulgaris suckers. *J. R. Soc. Interface* **11**(91), 20130816 (2014)
12. Wu, J.Z., Dong, R.G., Rakheja, S., Schopper, A., Smutz, W.: A structural fingertip model for simulating of the biomechanics of tactile sensation. *Med. Eng. Phys.* **26**(2), 165–175 (2004)



FPGA Implementation of a Convolutional Recurrent Neural Network for Real-Time Sensor Data Processing

Riccardo Testa^(✉), Mohamad Yaacoub, Christian Gianoglio, and Maurizio Valle

Department of Naval, Electrical, Electronics, and Telecommunications Engineering,
University of Genoa, Genoa, Italy
riccardo.testa@edu.unige.it

Abstract. This paper proposes a shallow Convolutional Recurrent Neural Network (C-RNN) that directly employs raw signals for classification, implemented on a Field Programmable Gate Array (FPGA) for artificial texture classification. Data was collected using a tactile sensing system based on piezoelectric polymers for eight artificial textures. Preliminary experimental results show that the neural network achieves an accuracy of 96.54%, and the implementation utilizes a total of 208,441 LUTs, 1,247 DSPs, 74,679 flip-flops, and 306 BRAM. The estimated latency is 1,242 clock cycles, corresponding to 6.21 μ s with a 200 MHz clock used in the synthesis.

Keywords: Tiny Machine Learning · Field Programmable Gate Array (FPGA) · Artificial Skin

1 Introduction

Endowing sensors with intelligence is becoming increasingly crucial in various application domains, including robotics and prosthetics [1]. Significant efforts have been dedicated to enabling intelligent tasks through machine learning (ML) algorithms [2]. ML offers powerful tools for data interpretation and the resolution of complex, nonlinear problems using a learning-by-examples approach. Nevertheless, the computational complexity inherent in ML methodologies often restricts their implementation on resource-constrained embedded systems. Therefore, more effort should be dedicated to hardware architectures to address implementation issues and achieve an adequate trade-off between real-time functionality and hardware resource utilization.

The efficient hardware implementation of ML algorithms, particularly for applications requiring real-time inference, has paved the way for more powerful embedded systems. Field-programmable gate arrays (FPGAs) have gained substantial attention for accelerated processing, offering a promising solution to overcome the limitations of conventional embedded systems [3]. Compared to traditional hardware like CPUs and GPUs, FPGAs provide significant advantages

through low-level customizability, resulting in increased efficiency and reduced inference latency [4–6]. For example, the authors in [7] proposed an FPGA implementation of a hybrid fixed-point binary convolutional neural network (H-CNN) for real-time touch modality, achieving a classification accuracy of 99.6% and an inference time of 0.8 ms. Similarly, in [8], researchers developed an implementation of a convolutional recurrent neural network (C-RNN) on a Zynq FPGA using high-level synthesis (HLS) for gesture recognition and motion evaluation, achieving a classification accuracy of 99%. In [9], an implementation of a fully connected multilayer perceptron and a supervised sequential learning algorithm on FPGA for hand gesture tracking achieved an accuracy of 96.33%.

In this paper, we designed a C-RNN that achieved an accuracy of 96.8%. Using the hls4ml Python package, the model was transformed into an HLS project, retaining an accuracy of 96.54%. The HLS project was then synthesized using Vivado HLS 2019.1. The synthesis report was analyzed to determine the model's viability for real-time inference in the application of surface texture classification using tactile sensing system based on P(VDF-TrFE) poly(vinylidene fluoride trifluoroethylene) (PVDF).

The rest of the paper is organized as follows: Sect. 2 illustrates the proposed approach, Sect. 3 reports the results obtained, and finally conclusions are drawn in Sect. 4.

2 Materials and Methods

2.1 Dataset

The dataset used in this work was collected in [10]. The dataset comprises the response of piezoelectric sensors integrated into a biomimetic fingertip, comprising 8 sensors in a skin patch, which was mounted on a Cartesian robot. The robot was programmed to explore 8 artificial gratings with different patch sizes (p) at three indentation forces (3N, 6N, and 12N), and two sliding velocities (8.6 mm/s and 13.7 mm/s). For each combination of force and velocity, 100 trials were conducted, each consisting of 10 s of sliding and sampled at 2 KSamples/second. This resulted in 600 trials for each grating, covering the 6 combinations. Additionally, 10 random segments of dimensions (300 time steps, 8 channels) were extracted from each trial. The resulting dataset is expressed as follows: $\mathcal{D} = \{(\mathcal{X}, y)_i; \mathcal{X}_i \in \mathbb{R}^{8 \times 300}; y_i \in \{\text{Grating1}, \dots, \text{Grating8}\}; i = 1, \dots, 34400\}$ where 8 corresponds to the number of channels, and 300 corresponds to the time information.

2.2 Classifier and Training Strategy

Classifier: Figure 1 illustrates the generic architecture of the C-RNN [11] network employed in this study to process the spatiotemporal nature of the tactile signals. The network embeds a single one-dimensional convolution layer that processes a 2-D input tensor, where one dimension corresponds to the number of

sensors and the other to the time samples. The convolution layer includes f 2-D kernel (k) with the same geometry as the input tensor. These kernels slide along the time axis creating f feature vectors through the scalar product operation.

Rectified Linear Unit (ReLU) is used as an activation function, followed by a batch normalization layer. The Max pooling performs a maximum pooling operation with dimension 2×1 . Followed by an LSTM layer with n hidden neurons. After the LSTM layer, the data is passed through a flattened layer, which converts the multi-dimensional output from the LSTM layer into a single one-dimensional vector. Finally, a fully connected layer with c units (corresponding to the number of the gratings) and Softmax as an activation function.

Training Strategy: The training procedure involved model selection, i.e., tuning the classifier architecture hyper-parameters. That procedure explored a grid of candidates, using different combinations of filters (f), kernel sizes (k), and LSTM hidden neurons (n) as follows:

- $f = \{4, 8, 16, 32\}$
- $k = \{3, 4, 5, 6\}$
- $n = \{4, 8, 16, 32\}$

A total of 64 C-RNN configurations were evaluated based on the f , k , and n values. In each training experiment, the dataset was split into 80% for training, 10% for validation, and 10% for testing. The networks were all implemented in Python using the Keras API with the following settings: Adam optimizer with a learning rate of 10^{-2} , batch size of 128, and number of epochs $ep = 200$. Moreover, a patience $p = 10$ was set to implement an early stop criterion on the validation loss.

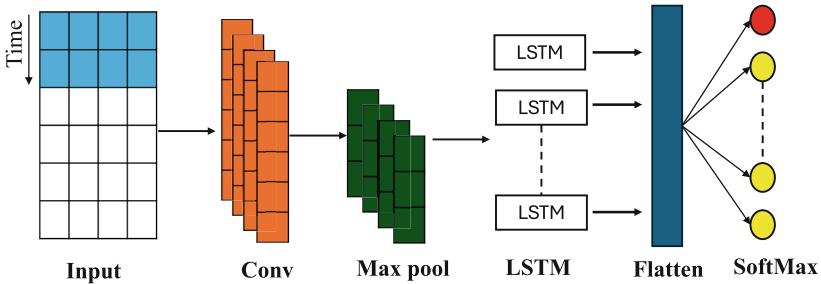


Fig. 1. CRNN architecture.

2.3 Synthesis

Upon completing training, the network with the best hyperparameters was converted into an HLS project and synthesized for the ZCU106 board, which is

equipped with an AMD Xilinx XCZU7EV-FFVC1156-2-E FPGA. This FPGA includes a quad-core ARM Cortex-A53 and dual-core ARM Cortex-R5F processors, alongside programmable logic featuring 1728 DSP slices, 230400 LUTs, and 460800 FFs.

Synthesis was facilitated using the hls4ml Python package [12–14] to generate the HLS project, subsequently processed by Vivado HLS 2019.1 to convert it into RTL and synthesize it.

The hls4ml package automatically translates a Python-designed machine learning model into HLS, allowing customization of per-layer attributes such as fixed-point precision, resource optimization strategy, DSP slice reuse factor, and other parameters. These features provide users with the flexibility to tailor the model for various FPGA configurations and application requirements. Table 1 outlines the key parameters, their descriptions, and the selected values for this particular model.

Table 1. Parameters of hls4ml model building function

Parameter	Description	Value chosen
Strategy	FPGA implementation focused towards latency or resource usage	Latency
Reuse Factor	Sets how many times a multiplier/DSP slice will be used for different queued operations in a layer	4
Precision	Fixed point precision used by model and layers	ap_fixed<20,7>
IO Type	Type of data structure used for inputs, intermediate activation between layers and outputs. Stream (FIFOs) or Parallel (RAM)	Stream

The model was optimized for minimal latency, prioritizing speed over resource usage. This aimed to explore the latency boundaries to assess the feasibility of deploying the model on FPGA for real-time inference tasks. While resource usage was deprioritized, to fit the model in the FPGA DSP availability, the reuse factor was set to 4, meaning that each DSP will perform 4 different sequential or queued operations. The IO type was set to `io_stream`. Finally, a precision of 20-bit with 7-bit integer part was chosen to cover most of the weight and bias values, while preventing accuracy reduction. The coverage of the weight and bias values can be seen in Fig. 2. The weight and bias values were represented in Q6.13 fixed-point precision. In Fig. 2 the gray background boxes in each layer depict all the values that can be represented with Q6.13, while the box plot visualizes the distribution of actual values, including outliers, for model parameters. Notably, some weights in the convolutional and LSTM layers do not fall within the possible Q6.13 values. However, these deviations did not affect the model accuracy because the numbers not completely covered by the Q6.13 are outliers.

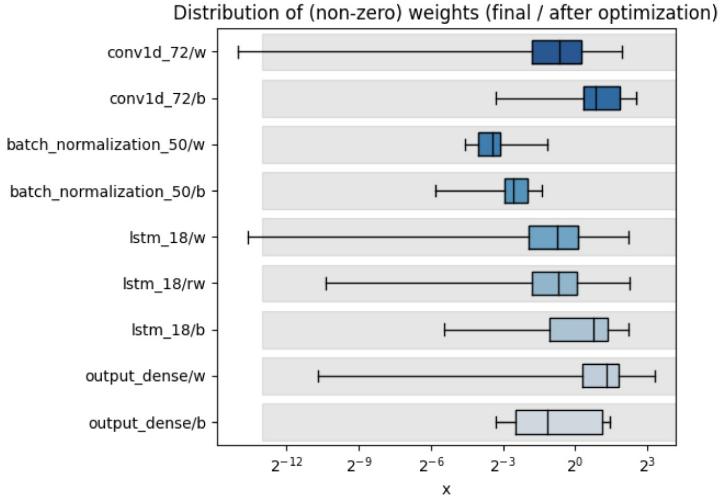


Fig. 2. Coverage (gray background) of the fixed point precision with respect to weight and bias values of the neural network.

3 Results and Discussion

3.1 Classification Accuracy

The best-performing network, which included a filter dimension $f = 32$, kernel size $k = 5$, and number of hidden neurons in the LSTM layer $n = 16$, exhibited a classification accuracy \mathcal{ACC} of 96.8%. Figure 3a illustrates the confusion matrix for the classification results. Notably, misclassification occurred between grating 0 and grating 1, as well as between grating 2 and grating 3. These errors can be attributed to the similarity in the pinch size of the respective textures; for more details refer to [10].

3.2 HLS Conversion

The selected network was quantized to a 20-bit fixed point representation using the hls4ml API, leading to a slight reduction in $\mathcal{ACC} \approx 0.36\%$. This drop can be attributed mainly to the so-called quantization error (i.e. difference in format precision). Figure 3b shows the confusion matrix post-quantization, showing similar misclassification patterns to those observed before quantization, particularly between grating 0 and grating 1, as well as between grating 2 and grating 3, as discussed in Sect. 3.1.

3.3 Synthesis

Using Vivado HLS 2019.1, the HLS project was synthesized with the Xilinx board ZCU106 as the target. The board features a Zynq Ultrascale+ XCZU7EV-

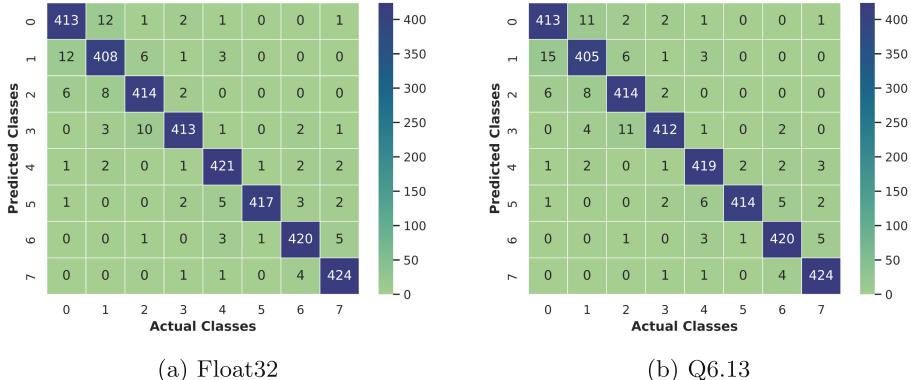


Fig. 3. Confusion Matrices: (a) Pre-Quantization, (b) Post-Quantization.

FFVC1156-2-E FPGA. Table 2 presents the parameters accepted by Vivado HLS, along with a brief description and an indication of whether they were enabled.

Table 2. Parameters accepted by the Vivado HLS tool

Parameter	Description	Value chosen
csim	HLS C simulation with a user-provided or Vivado-generated input	True
synth	Transformation of the project from HLS to RTL by Vivado HLS	True
vsynth	Full synthesis and technology mapping of the project, outputs report on expected latency and resource usage of the IP	True
export	Export of the IP for FPGA integration	True
cosim	C/RTL cosimulation, can be compared with C simulation to check the correct transformation of HLS to RTL	False

Table 3 shows that the model uses a high number of LUTs in the FPGA. However, it is to be noted that, as stated by the hls4ml documentation, this preliminary estimate should decrease in the final implementation. It can be interesting to observe the per-layer resource usage (Table 4) to understand where the model can be optimized to have a smaller resource footprint. This optimization is outside the scope of this study, but these insights will be used in future works to reduce the size of the model.

Table 3. Estimated resource usage of the synthesized C-RNN

Name	Expression	FIFO	Instance	TOTAL	Available	Usage
BRAM_18K		272	34	306	624	49%
DSP48E			1247	1247	1728	72%
FF		6154	68527	74679	460800	16%
LUT	2	7544	200895	208441	230400	90%

Table 4. Per-layer resource usage after the synthesis

Layer	BRAM_18K	DSP48E	FF	LUT
Conv1D_pad			435	701
Conv1D		320	14567	48590
Conv1D_relu			659	1935
BatchNorm		29	1155	2191
MaxPooling1D			5621	7066
LSTM	32	864	42977	132838
Dense		32	1762	5172
Dense_softmax	2	2	1351	2402

The layer taking the most of the resources is the LSTM, followed by the convolution layer due to the high number of parameters in the two layers: 3136 for the LSTM and 1312 for the Conv1D.

Finally, the expected latency for this IP is 1242 clock cycles. Since the clock considered for this synthesis has a 200 MHz frequency, the latency results in 6.21 microseconds. This latency is extremely low and is more than fit for real-time operation with a 2Ksample/s ADC.

4 Conclusion and Future Work

This paper proposes a Convolutional Recurrent Neural Network (C-RNN) for an eight-class artificial texture classification problem. The core strength of the C-RNN is its ability to directly process raw signals from a PVDF-based sensing system. The network was evaluated on an FPGA, demonstrating its potential for real-time classification with a latency of 6.21 μ s and a classification accuracy of 96.54%. This approach seems suitable for biomedical applications requiring rapid computation near the sensors. Future work will focus on optimizing the C-RNN for greater efficiency. This includes architectural refinements, quantization, and pruning to reduce latency and power consumption. A complete FPGA implementation will be developed and tested in real-world biomedical applications to validate its performance.

References

1. Seminara, L., et al.: Towards integrating intelligence in electronic skin. *Mechatronics* **34**, 84–94 (2016)
2. Shih, B., et al.: Electronic skins and machine learning for intelligent soft robots. *Sci. Robot.* **5**(41), eaaz9239 (2020)
3. Dhouibi, M., et al.: Accelerating deep neural networks implementation: a survey. *IET Comput. Digit. Tech.* **15**(2), 79–96 (2021)
4. Sanaullah, A., et al.: Real-time data analysis for medical diagnosis using FPGA-accelerated neural networks. *BMC Bioinform.* **19**, 19–31 (2018)
5. Al-Ali, F., et al.: Novel casestudy and benchmarking of AlexNet for edge AI: from CPU and GPU to FPGA. In: 2020 IEEE CCECE, pp. 1–4. IEEE (2020)
6. Pacini, F., et al.: Design and evaluation of CPU-, GPU-, and FPGA-based deployment of a CNN for motor imagery classification in brain-computer interfaces. *Electronics* **13**(9), 1646 (2024)
7. Younes, H., et al.: Hybrid fixed-point/binary convolutional neural network accelerator for real-time tactile processing. In: 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pp. 1–5. IEEE (2021)
8. Liu, H., et al.: An FPGA-based upper-limb rehabilitation device for gesture recognition and motion evaluation using multi-task recurrent neural networks. *IEEE Sens. J.* **22**(4), 3605–3615 (2022)
9. Heidaryan, M., et al.: FPGA implementation of two multilayer perceptron neural network in cascade for efficient real time hand gestures tracking. *Microprocess. Microsyst.* **100**, 104849 (2023)
10. Ali, H.A.H., et al.: Neuromorphic tactile sensing system for textural features classification. *IEEE Sens. J.* (2024)
11. Shi, B., et al.: An end-to-end trainable neural network for image-based sequence recognition and its application to scene text recognition (2015)
12. FastML Team. HLS4ML (2023). <https://github.com/fastmachinelearning/hls4ml>
13. Duarte, J., et al.: Fast inference of deep neural networks in FPGAs for particle physics. *JINST* **13**(07), P07027 (2018)
14. Arrestad, T., et al.: Fast convolutional neural networks on FPGAs with HLS4ML. *Mach. Learn. Sci. Tech.* **2**(4), 045015 (2021)



Electrical Characterization of Red Blood Cells with a Nanoelectrode Array Sensor

Mariano José Guillén^{1,2}, Jacopo Nicolini^{1(✉)}, Daniele Goldoni¹, Rossana Madrid², and Luca Selmi¹

¹ DIEF, University of Modena and Reggio Emilia, Modena, Italy
jacopo.nicolini@unimore.it

² Dpto. de Bioingeniería - FACET-UNT/INSIBIO-CONICET,
San Miguel de Tucumán, Argentina

Abstract. We report high-frequency capacitance measurements and simulations of human red blood cells by a nanoelectrode array imager with submicron spatial resolution. The measurements are compared to numerical finite element method (FEM) simulations within the Poisson-Nernst-Plack modeling framework carried out with a commercial multi-physics platform (COMSOL). Insights on the shape, cartesian position and tilting of the cells on the array are discussed. Two sets of measurements are compared in terms of cell diameter to evaluate the effect of centrifugation on the samples.

Keywords: red blood cell · nanoelectrode array · high frequency · capacitance imaging

1 Introduction

Among multiple sample characterization approaches, optical imaging [19] and fluorescence-based chemical sensors [7] are mainstream technologies amenable to real-time applications at low cost and with high selectivity. Electrochemical impedance spectroscopy (EIS) is also an attractive method [12, 21, 22] that enables the characterization of electrode-bound biomolecules and analyte dispersions without bulky optical access and with on-par resolution to optical and chemical methods [1–4]. In particular, cell counting and cell shape detection are relevant applications of the branch of EIS known as electrochemical impedance cytometry (EIC) [8, 14], focused on the electrical characterization of cells. However, the sensing volume of EIC is limited by Debye screening at biocompatible saline concentrations. EIC at high frequency, close to or beyond the electrolyte dielectric relaxation cut off frequency [18, 23] has the potential to overcome these limits, and even to non-invasively probe across the cellular membrane [14], an exciting but unexplored possibility at submicron resolution scale.

In this paper, we report exploratory high-frequency impedance cytometry study of red blood cells (RBC) using a newly developed simulation setup for

the commercial finite-element simulator (COMSOL Multiphysics ® [5]) and a CMOS nanoelectrode array biosensing platform, with the aim to characterize single RBCs. Some insights are also provided about the characterization of RBC biconcave shape.

2 Materials and Methods

As regards the simulations, the RBC discocyte was initially modeled with a newly developed simulation setup in COMSOL Multiphysics ® using the continuous 4th degree equation of the surface proposed in [17], and with an external diameter of 7 μm . The overall volume is 86 fL, in line with the average volume of healthy RBCs. The membrane thickness is set to 7.5 nm, with a relative permittivity value of 13.1. The permeability of the membrane is neglected. In COMSOL the membrane is treated in the thin layer approximation for computationally more efficient simulations. The cell's dielectric properties are those reported in [24]. The intracellular ion concentrations are (in mM): 140 K⁺, 11 Na⁺, 80 Cl⁻, and 0.006 Ca²⁺ [15]. These initial parameters are then adjusted to optimal values to reproduce the experiments, as discussed in Sect. 3.2.

The simulation domain comprises a 17×15 nanoelectrodes portion of the surface of the 256×256 array used for the measurements. The surrounding medium consists of a 154 mM concentration NaCl, water-based electrolyte that mimics the ionic strength of a PBS solution. The measurements were taken with the nanoelectrode sensing platform described in [9, 10, 23]. The platform, endowed with individually addressable nanoelectrodes having 180 nm diameter and 600 nm by 890 nm pitch resolution, performs spectrally resolved charge-based capacitance measurement in the 1–70 MHz range [23]. A capacitive image is obtained by scanning the rows one by one, with all other rows acting as counter electrodes.

The system is temperature-controlled [23] and is coupled to a microfluidic apparatus for sample insertion in an optimized microchamber [10]. Following the calibration steps detailed in [23], the capacitance image acquired by the measuring system at $frame_s$ is normalized electrode-by-electrode to a reference frame ($frame_0$) without red blood cells on the array, obtaining the sensing information as the capacitance variation: $\Delta C = C_{w/\text{analyte}} - C_{w-o/\text{analyte}}$, as in previous works [6, 9, 10, 20]. Additionally, to remove possible offsets, at frame s the average $\overline{\Delta C}_s$ of a portion of the array without RBCs is calculated and subtracted from the calculated ΔC of each electrode ($\Delta C(i, j) = \Delta C(i, j) - \overline{\Delta C}_s$), obtaining a zero mean value ΔC distribution of the electrodes without the RBCs, as expected. The experiments were done at room temperature (approximately 22 °C). Two experiments were conducted to evaluate the effect of the different conditions on the RBC diameter. The first experiment employed a reference RBC sample obtained by dilution of whole blood in phosphate buffer saline (PBS). In the second experiment, the RBC sample was obtained by dilution in PBS of only the solid part of the blood, which was separated from plasma by centrifugation (5415D centrifuge by Eppendorf, at 6000 rpm for 10 min). In both cases, the hematocrit of the analyzed sample was ≈1%.

3 Results

In this section, we explain the procedure used to analyze the capacitive images of RBCs and we report the results.

3.1 Validation of the COMSOL Simulation Setup

The new COMSOL model and simulation setup were tested and matched to the established, in-house simulator ENBIOS, a CVFEM solver implementing high-frequency impedance spectroscopy (HFIS) calculations based on the Poisson-Boltzmann and Poisson-Nerst-Planck equation sets in DC and AC, respectively. ENBIOS has been extensively tested in previous works [9, 10, 20, 23]; hence it was used as a reference for testing the new COMSOL setup.

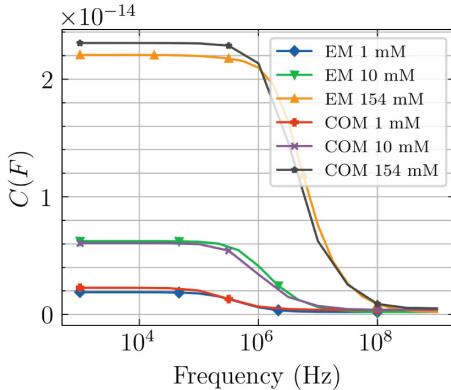


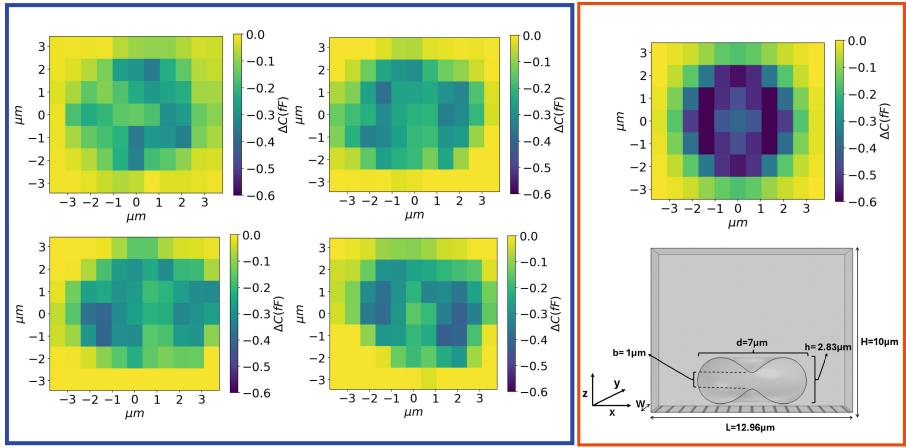
Fig. 1. Capacitance spectra of the nanoelectrode array platform without analytes at different electrolyte salt concentrations using the COMSOL model (COM) and ENBIOS model (EM) setups.

Figure 1 compares simulations of the nanoelectrode response to a few electrolyte environments without analytes. The curves show a very good agreement between the two simulators, with only small discrepancies likely due to the different meshes adopted by the two codes. The agreement demonstrates the correctness of the new COMSOL simulation deck and its ability to provide reliable results in line with the tried-and-tested ENBIOS tool.

3.2 First Set of Experiments: Diameter of Non-centrifuged Samples

After testing the proper functionality of the software, we run COMSOL simulations without any Stern layer on the electrodes and with one RBC placed in the center of the array and parallel to the array surface. Figure 2 shows capacitance

images at $f = 32$ MHz. Notice that $\Delta C < 0$, as expected due to the dielectric nature of the lipidic membrane. We observe a reasonably good agreement between the measured and the simulated capacitance images. The latter exhibits a well recognizable internal dimple and external ring, although the magnitude of the signal is not quite the same as in the measurements.



Experiments

Simulation

Fig. 2. Measured capacitance images of a few RBCs (left), and simulated capacitance image assuming 250 nm elevation above the array, no tilt, and no Stern layer. The sketch reports the dimensions initially used to match the experiments. RBC parameters as detailed in Sect. 2.

Figure 3 shows the ΔC profiles along the electrode row underneath the center of the RBC for different electrolyte concentrations as detailed below. The simulated response in a PBS-like solution is higher (in absolute value) than in the experiments but retains its doubly peaked shape. Interestingly, the discrepancy can be strongly reduced by adopting the electrical parameters in [11, 13] for healthy RBCs, adjusting the dimple thickness to 0.5 μm , reducing the RBC volume to 80 fL (which is still within physiological values), and reducing the electrolyte salinity from 154 to 130 mM, which is within the uncertainty limits of the experiment. The asymmetry between the peaks can be explained by a modest tilting of the cell with respect to the substrate.

However, an even better match with experiments is obtained by retaining the simulation parameters listed in Sect. 2, an elevation above the electrode of 250 nm but including the Stern layer on top of the electrodes in the simulation setup, and adjusting within healthy limits the diameter of the cell. The Stern layer represents a fixed and typically large capacitance ($\approx 0.2 \text{ F/m}^2$), in particular we adopted the same set of Stern layer parameters as in [6], that is, the permittivity $\epsilon_r = 7$ and the thickness of the layer $t = 0.25 \text{ nm}$. This results

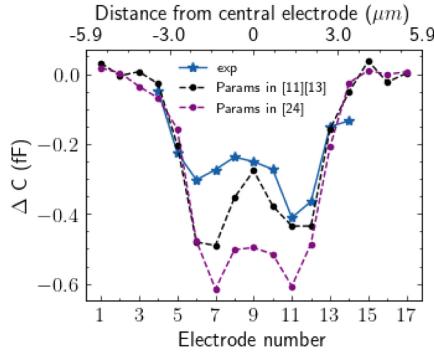


Fig. 3. Capacitance profile along the electrode central row at different concentrations for an elevation of 250 nm. The bottom x-axis reports the electrode's number; the top x-axis the distance.

in a Stern layer capacitance of 0.24 F/m². The introduction of the Stern layer significantly improves the agreement between measurements and simulations, even without the (less justified) modifications to the RBC shape and external concentration described above, see Fig. 4. This is due to the high salinity of the solution, which increases the diffused layer capacitance to non-negligible values compared to the Stern layer capacitance, thus lowering the predicted response.

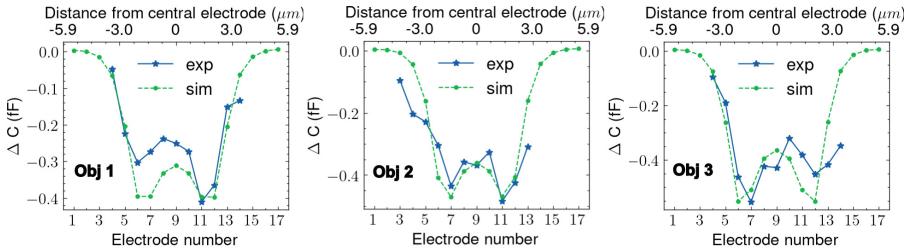


Fig. 4. Measurements and best-fit simulations of the capacitance response along the central row of electrodes for three RBCs in the reference sample. The bottom x-axis reports the electrode's number; the top x-axis the distance. All simulations include the Stern layer.

The RBC diameters in Fig. 4 are 7.5 μm , 7 μm , and 7.5 μm for object 1, 2, and 3, respectively. The RBC volume changes according to the diameter but remains within physiological values. All other parameters are the same as detailed in

Sect. 2. Note that the experimental curves extend over fewer electrodes than the simulated ones to cut out interference signals from neighboring cells and from calibration columns interleaved in the array. The remaining discrepancies in Fig. 4 are likely due to a slight lateral offset of the RBC parallel to the sensor surface and a slight tilt, not accounted for in the simulations.

3.3 Second Set of Experiments: Diameter of Centrifuged Samples

For the next set of results, we consider measurements at $f = 50\text{ MHz}$ where the sample has been centrifuged at 6000 RPM for 10 minutes with the 5415D centrifuge by Eppendorf. The hematocrit and all other characteristics of the blood sample remain the same of the previous experiment.

Figure 5 reports the best-fit simulations for three RBCs in the centrifuged sample. Once again good agreement could be obtained with only small adjustments to the RBC diameters, which are now set to $7.8\text{ }\mu\text{m}$ for object 5 and to $7.3\text{ }\mu\text{m}$ for objects 4 and 6, respectively. This analysis, however limited in number, suggests that the diameter of the RBCs does not suffer large changes due to centrifugation and remains in the typical range for healthy cells [16]. They also exemplify the use of the sensor, in combination with advanced FEM simulations, for purely electrical cytometry of RBCs.

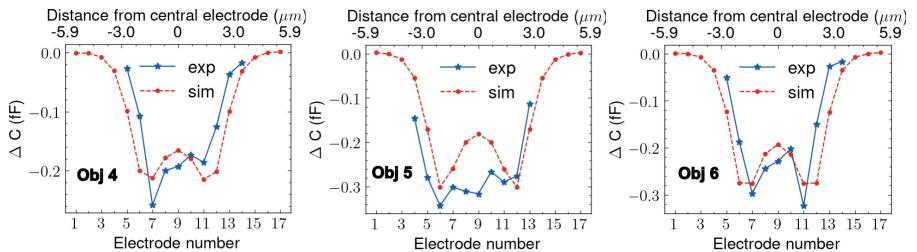


Fig. 5. Measurements and best-fit simulations of the capacitance response along the central row of electrodes for three RBCs in the centrifuged sample. The bottom x-axis reports the electrode's number; the top x-axis the distance. All simulations include the Stern layer.

Notice that the two sets of measurements were taken at different frequencies. In order to test if the frequency may induce systematic errors, Fig. 6 reports the normalized RBC spectra at 32 and 50 MHz, showing that the RBC diameter remains the same, and the normalized traces are almost identical. This observation confirms the possibility to directly compare the diameters extracted at two different frequencies as done in Fig. 4 and Fig. 5.

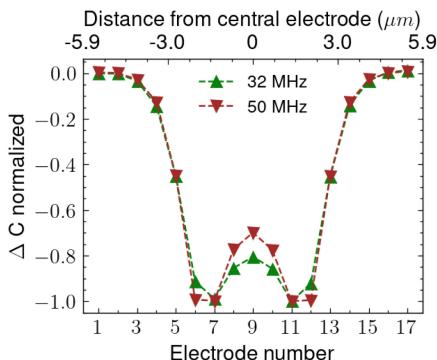


Fig. 6. Normalized profile of the capacitance response along the central row of electrodes for simulations at $f = 32$ MHz and $f = 50$ MHz.

4 Conclusions

We demonstrated the potential of combining a CMOS nanoelectrode array platform and a full 3D finite element model of the sensor response, to support purely electrical imaging and high-frequency impedance cytometry of human RBCs.

The normalized capacitance response along a diametral row of electrodes is almost independent of the measurement frequency and is useful to determine the RBC diameter by comparison with FEM simulations. The analysis of RBC images from two experiments confirm that properly chosen centrifugation steps, as those routinely used to analyze blood samples, do not affect the RBC in terms of diameter.

These results widen the application range of CMOS-based nanoelectrode array sensors for high-frequency impedance spectroscopy. They underline the potential and relevance of label-free electrical imaging of cells as a diagnostic tool in biomedical applications, possibly enhancing the current mainstream technology with future non-invasive intracellular probing capabilities. Future work with more extensive sample datasets will be key to thoroughly prove these potentialities.

Acknowledgements. This work was supported in part by ESF REACT-EU for National Operational Programme (PON) Research and Innovation 2014-2020 and by NextGenerationEU, Linea 1.3, Partenariati Area 6, PNRR HEAL ITALIA Project PE 0000019. The authors acknowledge NXP Semiconductors and Frans Widdershoven for providing the chips, and Federico Leva for fruitful discussions.

References

1. Berggren, C., et al.: *Electroanalysis* **13**(3), 173–180 (2001). [https://doi.org/10.1002/1521-4109\(200103\)13:3<173::AID-ELAN173>3.0.CO;2-B](https://doi.org/10.1002/1521-4109(200103)13:3<173::AID-ELAN173>3.0.CO;2-B)
2. Carminati, M., et al.: *Sens. Actuat. A* **172**(1), 117–123 (2011). <https://doi.org/10.1016/j.sna.2011.02.052>
3. Carneiro, P., et al.: *Talanta* **211**, 120700 (2020). <https://doi.org/10.1016/j.talanta.2019.120700>
4. Ciccarella, P., et al.: *IEEE J. Solid-State Circuits* **51**(11), 2545–2553 (2016). <https://doi.org/10.1109/JSSC.2016.2607338>
5. Comsol, Inc., Comsol Multiphysics v. 6.0
6. Cossettini, A., et al.: *IEEE Sens. J.* **21**(4), 4696–4704 (2021). <https://doi.org/10.1109/JSEN.2020.3032712>
7. Geng, W., et al.: *Angew. Chem. Int. Ed.* **60**(36), 19614–19619 (2021). <https://doi.org/10.1002/anie.202104358>
8. Gökçe, F., et al.: *Biomicrofluidics* **15**(6) (2021). <https://doi.org/10.1063/5.0073457>
9. Goldoni, D., et al.: *IEEE Sens. J.* **23**(17), 20180–20188 (2023). <https://doi.org/10.1109/JSEN.2023.3296158>
10. Goldoni, D., et al.: In: *2023 IEEE Sensors*, pp. 1–4 (2023). <https://doi.org/10.1109/SENSORS56945.2023.10325169>
11. Gramse, G., et al.: *Biophys. J.* **104**(6), 1257–1262 (2013). <https://doi.org/10.1016/j.bpj.2013.02.011>
12. Hedayatipour, A., et al.: *Biosens. Bioelectron.* **143**, 111600 (2019). <https://doi.org/10.1016/j.bios.2019.111600>
13. Honrado, C., et al.: *J. R. Soc. Interface* **15**(147), 20180416 (2018). <https://doi.org/10.1098/rsif.2018.0416>
14. Honrado, C., et al.: *Lab Chip* **21**(1), 22–54 (2021). <https://doi.org/10.1039/DOLC00840K>
15. Hughes, M.P., et al.: *Sci. Rep.* <https://doi.org/10.1038/s41598-021-98102-9>
16. Kinnunen, M., Kauppila, A., Karmenyan, A., Myllylä, R.: *Biomed. Opt. Express* **2**(7), 1803–1814 (2011). <https://doi.org/10.1364/BOE.2.001803>
17. Kuchel, P.W., et al.: *Sci. Rep.* (2021). <https://doi.org/10.1038/s41598-021-92699-7>
18. Lemay, S.G., et al.: *Acc. Chem. Res.* **49**(10), 2355–2362 (2016). <https://doi.org/10.1021/acs.accounts.6b00349>
19. Leonardi, A.A., et al.: *ACS Sens.* **3**(9), 1690–1697 (2018). <https://doi.org/10.1021/acssensors.8b00422>
20. Lombardo, F., et al.: *Eng. Appl. Artif. Intell.* **127**, 107246 (2024). <https://doi.org/10.1016/j.engappai.2023.107246>
21. Manickam, A., et al.: *IEEE Trans. Biomed. Circuits Syst.* **4**(6), 379–390 (2010). <https://doi.org/10.1109/TBCAS.2010.2081669>
22. Poghossian, A., Schöning, M.J.: *Sensors* **20**(19), 5639 (2020). <https://doi.org/10.3390/s20195639>
23. Widdershoven, F., et al.: *IEEE Trans. Biomed. Circuits Syst.* **12**(6), 1369–1382 (2018). <https://doi.org/10.1109/TBCAS.2018.2861558>
24. Zhananov, A., Yang, S.: *Anal. Methods* **10**(2), 168–179 (2018). <https://doi.org/10.1039/C7AY01692A>



The Safety Monitoring System for the SND@LHC Experiment at CERN

Francesco Fienga^{1,3(✉)}, Vincenzo Romano Marrazzo^{1,3(✉)}, Michele Riccio¹,
Antonia Di Crescenzo^{2,3,4}, Giovanni De Lellis^{2,3,4}, Salvatore Buontempo^{2,3},
Andrea Irace¹, and Giovanni Breglio^{1,3}

¹ Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Naples, Italy

{francesco.fienga, vincenzoromano.marrazzo}@unina.it

² Istituto Nazionale di Fisica Nucleare (INFN), Rome, Italy

³ European Organization for Nuclear Research (CERN), Meyrin, Switzerland

⁴ Department of Physics “Ettore Pancini”, University of Naples Federico II, Naples, Italy

Abstract. At the forefront of particle physics research, the SND@LHC experiment stands, strategically positioned 480 m downstream of the ATLAS interaction point within the LHC tunnel. Within this pioneering experiment, the SND Security Monitoring System (SND-SMS) acts as a vigilant guardian, employing IoT technology to safeguard the experiment’s integrity and operational stability. Utilizing a network of Arm Cortex-M7 MCU and Sensirion SHT31D sensors, SND-SMS meticulously monitors environmental parameters such as temperature, humidity, and smoke levels across the experimental apparatus. Powered by ARM RTOS Mbed OS firmware and MQTT protocol, this system orchestrates real-time data collection, alarm classification, and initiative-taking safety measures, ensuring prompt responses to anomalies, from minor deviations to critical events, thereby upholding the SND@LHC’s safety standards and operational efficiency.

Keywords: Safety Monitoring System · IoT node · Sensor network · CERN

1 Introduction

SND@LHC [1] is a compact experiment situated 480 m downstream of the ATLAS interaction point at CERN’s LHC. It features a hybrid detector system composed of tungsten plates, emulsion, and electronic trackers, serving as an electromagnetic calorimeter. Additionally, it includes a hadronic calorimeter and a muon identification system. This setup enables SND@LHC to discern interactions of all three neutrino flavors [2], facilitating investigations into heavy flavor production at the LHC in the forward region. The experiment necessitates both a sophisticated apparatus and a vigilant monitoring system to ensure ongoing surveillance and proactive response to potential hazards, safeguarding the experiment’s integrity and operational stability.

In this context, IoT technology provides advanced solutions for continuous surveillance and proactive responses in experimental settings, enhancing safety and ensuring

operational integrity. Into an IoT-based system, it is possible to easily integrate sensors, actuators, and communication networks to provide real-time monitoring and data analysis with continuous tracking of critical parameters. Triggering an automated intervention when a threshold is overcome, is possible to prevent potential hazards from escalating into serious issues [3]. State-of-the-art research highlights the effectiveness of IoT in various domains. For instance, a study by Hassan et al. [4] demonstrated the use of IoT-based systems to monitor and control environmental conditions in laboratories; another study by Li et al. [5] showcased an IoT framework for detecting gas leaks in industrial settings. Other employment of the IoT in different environments are presented in [6], embedded with optical fiber sensor technology; or in [7] for the detecting of myocardial infarction in biomedical application. In this article, the design and installation of a safety monitoring system, in the framework of the SND@LHC experiment, is described. The system has been running for more than two years, monitoring physical quantities crucial for the correct functionality of the whole SND@LHC experimental apparatus.

2 The SND-SMS

The designed SND Safety Monitoring System (SND-SMS) is based on a IoT paradigm, where itself acts as an IoT node. A schematic illustration of the comprehensive SND-SMS is depicted in Fig. 1. For a better understanding of the proposed system, its description is split into two main parts.

2.1 Hardware Design

The core of the design is an Arm Cortex-M7 MicroController Unit (MCU) with high-performance and DSP with DP-FPU housed on the NUCLEO-F7 development board. Temperature and humidity are measured in 5 distinct locations using digital sensors (Sensirion SHT31D) which guarantee an accuracy of ± 0.2 °C and $\pm 1.5\%$ RH respectively and a reliable I2C communication with the host microcontroller. These sensors were mounted in daisy chain configuration, employing a single cable (five poles) for the communication (SCA, SCL), address, and supply handling (GND, 3.3 V). The SMS system is also equipped with smoke sensors, used for fire and/or smoke detection. Each sensor is characterized by a relay output, connected to microcontroller's digital inputs with interrupt capability. Due to possible malfunction due to the exposure to the LHC tunnel radiation field, a single smoke alarm may be subjected to fake activation (hence, creating a fake alarm condition). This effect is mitigated including a redundancy of three smoke sensors, activating an alarm condition if and only if all the sensors are active. The Nucleo-F7 board is further connected with an external relay shield compatible with its pinout. This latter is equipped with four relays, three of which are used in the proposed design: one providing a reset signal for the smoke sensors; other two providing a kill command to the two CAEN SY5527, handling the power for the whole experiment. Another digital pin of the MCU is occupied with an input signal acquired from the external cooling system, in order to consider a possible failure and the consequent restart time for the alarm control (explained in Sect. 3). Finally, data are published on a mosquitto-based MQTT broker flashed on a Raspberry Pi, connected through an ethernet cable.

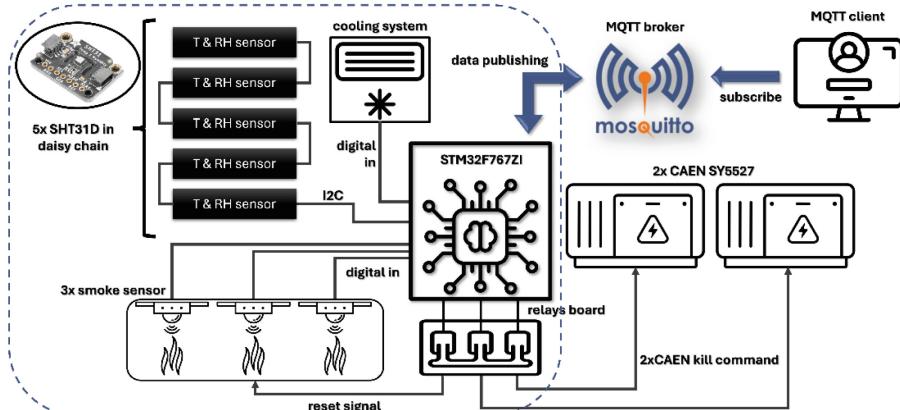


Fig. 1. Schematic view of the safety and environment monitoring system. The items included in the dashed line are those physically installed inside the neutron-shielded box around the target system.

2.2 Firmware Design

The developed firmware is based on Mbed OS Real Time Operating System 6. It manages multiple tasks, including: (i) continuous sensor readings, (ii) establishing an Ethernet connection to an MQTT broker server, (iii) transmitting sensor data and receiving configuration messages from the MQTT broker, and (iv) executing safety actions based on alarm levels.

Temperature sensors are read within a polling cycle with an interval of 500 ms, while relays are controlled using external interrupts. The MQTT protocol is employed for IoT data communication: the SMS system acts as a publisher for sensor data and alarm messages and can receive configuration messages from another client via the MQTT broker. Upon MCU power-up, a secure connection is established using a TCP socket to the broker server's IP address. A hardware watchdog is implemented to enhance the system's robustness and reliability. In the event of network disconnection or any irregularity, the SMS system reboots to its initial state within 30 s.

The system is designed for continuous 24/7 operation, and the frequency of data posting can be configured by the operator.

3 On-Field Installation and Results

Prior to deployment on the SND experiment, the system underwent rigorous testing in the laboratory. This included two specific communication tests: (i) the values from Temperature & Relative Humidity (T&RH) sensors were published on the monitor page of the MOSQUITTO server located at CERN (this ensured that real-time environmental data could be effectively transmitted and displayed); (ii) a simulated smoke alarm trigger was generated, and the corresponding alert was published on the alarm page of the MOSQUITTO server. This test validated the system's capability to handle emergency signals and communicate critical alerts accurately. These tests confirmed the

system's readiness for operational use, demonstrating reliable communication with the MOSQUITTO server for both routine monitoring and emergency responses.

Finally, the system was installed in its final location, assuring a temperature and humidity mapping of comprehensive SND experimental apparatus. The sensors' positions were chosen to minimize the interference with the sci-fi mounting/unmounting (Fig. 2, a). Hence, three sensors were positioned on the inner metal plane perpendicular to the Sci-Fi, monitoring the temperature and humidity close to the emulsion blocks; while the two sensors are placed on the opposite side, facing the cold box. Furthermore, the smoke sensors were placed on the top side of the box (Fig. 2, b) for a better detection in case of smoke. Connecting cables were managed on the top side (for smoke sensors) and bottom side (for T&RH sensors), connected to the Nucleo-F7 board, placed underneath the cooling system (Fig. 2, c). Data are shared from the Nucleo-F7 to the Raspberry PI, in which the MOSQUITTO server was installed, through an ethernet cable running over a long distance, placed in a safe position.

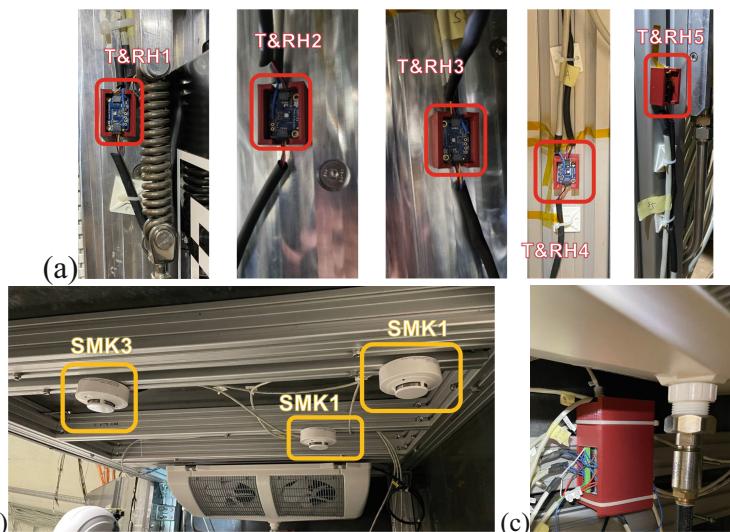


Fig. 2. SMS installation at SND experiment: (a) T&RH sensors positioning close to the scifi; (b) smoke sensors positioning on the top side of the box; (c) Nucleo-F7 board positioning underneath the cooling system.

3.1 Alarm Control

The alarm control algorithm was designed to classify them in three levels. When an alarm occurs the SND-SMS sends an alarm message to the MQTT broker and, according to the level of the alarm, undertakes the needed action to secure the safety of the infrastructure. The low level occurs when temperature or humidity readings of one sensor overcome the set thresholds, or if one smoke sensor is triggered. To ensure compliance with the safety standards of the LHC tunnel in case of fire or smoke, this latter event is handled

in asynchronous way by the SND-SMS: the alarm is raised as soon as a single smoke sensor is triggered. To guarantee the stability of the environmental parameter inside the cold-box, and the safety the latter, the SND-SMS takes under constant monitor the status of the cooling system and, in case of a stop, the time it remains off. Therefore, a transition of the cooling system from on to off will trigger a low-level alarm. If the cooling stays off longer than its grace time, a medium-level alarm will be activated. In this potentially harmful scenario, the SND-SMS while sending an alarm message to the broker, will promptly send a hardware kill command to the CAEN power supply systems. The medium-level alarm is verified even when temperature or humidity readings of two sensors exceed the set thresholds. In case of two, or more, triggered smoke sensors a high-level alarm is raised with consequent shutdown of the system and the related message is posted to the broker, as in the previous case and not as an independent document. The alarm description is further summarized in the following table (Table 1).

Table 1. Alarm control algorithm description.

Alarm	Condition	Output
Low level	<ul style="list-style-type: none"> • one T&RH sensor is over the threshold previously set; • one smoke sensor is triggered; • the cooling system switch from ON to OFF 	<ul style="list-style-type: none"> ✓ CAEN systems remain in on state; ✓ low level alarm message is posted on the dedicated topic
Medium level	<ul style="list-style-type: none"> • two or more T&RH are over the threshold previously set; • the cooling system switches from ON to OFF and remains in OFF state for more than a time previously set 	<ul style="list-style-type: none"> ✓ hardware kill command is sent to the CAEN power supply systems. The kill condition remains until the alarm is cleared; ✓ medium level alarm is posted on the dedicated topic
High level	<ul style="list-style-type: none"> • two or more smoke sensors are triggered 	<ul style="list-style-type: none"> ✓ CAEN systems are turned in OFF state until the alarm is cleared

3.2 Results

After conducting laboratory tests and the subsequent on-field installation, the SMS was activated for a couple of months alongside the comprehensive experiment to monitor its proper functionality. During this period, temperature and relative humidity were monitored through the access on a dedicated webpage, as it is illustrated in Fig. 3, where three days of data are shown in the period 24–27 May 2022. In this plot a dynamic trend can be noted for each sensor, particularly for the T&RH2 (hence, on the sci-fi/emulsion side), whose variation is most pronounced. What is worth to mention is that the proposed system was able to detect a water leak in June 2022, during the mentioned first trial. Due to low level alarm caused by the T&RH5, a sharp rise in relative humidity was found. After this event, the experiment was stopped to allow a technical intervention.

As it is shown in Fig. 4 with three pictures, a water leak was present on a joint close to the T&RH5 sensor (Fig. 4, left), with a significant amount of water on the floor (Fig. 4, center and right). After the trial period, the experiment was fully activated and is now operational, collecting data. In Fig. 5 it is shown the definitive version of the webpage in which all significant data are shown: from top to bottom it can be noted: humidity, temperature, cooling system and smoke sensor alarm. For each plot is possible to exclude one or more sensor data. Concerning the smoke sensor alarm, it is shown as a digital data, set as “1” if the alarm is on (only if all sensors are detecting smoke or are active for a single event), or as “0” (complementary condition). Moreover, it is possible to manually change the thresholds previously set, or to modify the alarm status.

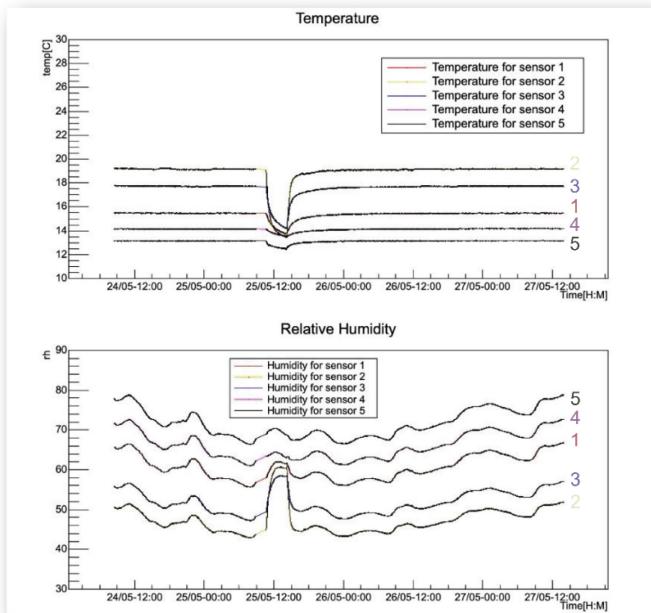


Fig. 3. First test of the SMS publishing data on a CERN webpage. Temperature (up) and relative humidity (down) are shown for all the T&RH sensors for a period of three days.



Fig. 4. Water leak detection from the proposed SMS due to a relative humidity variation sensed from the T&RH5 sensor.



Fig. 5. SMS currently running of the dedicated webpage in which is possible to change thresholds and exclude sensors manually, through JSON string. In the webpage, starting from the upper side, relative humidity, temperature, cooling system, and smoke sensor alarm are shown.

4 Conclusion

The SND Safety Monitoring System (SND-SMS) represents a pinnacle of technological innovation and safety assurance within the SND@LHC experiment. It is based on a Nucleo-F7 board, mounting the STM32F767ZI MCU. Through the I2C communication and digital pin reading, it was possible to design a sensor network comprising of temperature and relative humidity sensors, smoke detector and cooling system activation time monitoring. With the further employment of a relay board, it gives the chance to

send a command to shut down the two CAEN system, and to reset the smoke detectors. Since its inception, SND-SMS has operated tirelessly, 24/7, ensuring the experiment's integrity and operational stability, as demonstrated from the water leak detection in June 2022. Through the access to the dedicated webpage, it is possible to monitor data and modify alarm conditions, through JSON string command. Through its integration of IoT technology, advanced sensors, and real-time data processing, SND-SMS meticulously monitors environmental parameters and implements proactive safety measures. It stands as a crucial guardian, enabling uninterrupted research into particle physics while upholding stringent safety standards. With its robust framework and responsive algorithms, SND-SMS exemplifies excellence in experimental safety systems, contributing to the advancement of scientific discovery at the forefront of particle physics research.

References

1. ACAMPORA, G., et al.: SND@ LHC: the scattering and neutrino detector at the LHC. *Journal of Instrumentation*, 19.05: P05067 (2024)
2. Di Crescenzo, A., Galati, G.: On behalf of the SND@LHC Collaboration. In: SND@LHC: A New Experiment in Neutrino Physics at the LHC. *Symmetry*, vol. 15, 1256 (2023). <https://doi.org/10.3390/sym15061256>
3. Paul, S., Sarath, T.V.: End to end IoT based hazard monitoring system. In: 2018 International Conference on Inventive Research in Computing Applications (ICIRCA). IEEE (2018)
4. Hassan, M.N., et al.: An IoT based environment monitoring system. In: 2020 3rd International Conference on Intelligent Sustainable Systems (ICISS). IEEE (2020)
5. Rajbanshi, A., et al.: DLeak: an IoT-based gas leak detection framework for smart factory. *SN Comput. Sci.* **3**(4), 273 (2022)
6. Marrazzo, V.R., et al.: IoT Node interrogation system for fiber Bragg grating sensors: design, characterization, and on-field test. *IEEE Trans. Instrum. Meas.* **73**, 1–8 (2024)
7. Gragnaniello, M., et al.: Real-time myocardial infarction detection approaches with a microcontroller-based edge-AI device. *Sensors* **24**(3), 828 (2024)

Optoelectronics and Photonics



Experimentally Validated Model of the Optoelectronic and Photonic Section of the Interferometric Fiber-Optic Gyroscope

Teresa Natale^(✉) and Francesco Dell’Olio

Micro Nano Sensor Group, Polytechnic University of Bari, Bari, Italy
t.natale@phd.poliba.it, francesco.dellolio@poliba.it

Abstract. An accurate stochastic model of the optoelectronic and photonic section of the interferometric fiber-optic gyroscope is developed taking into account all noise and disturbances sources. The model is validated using experimental data taken from a prototype of the sensor integrating commercial-off-the-shelf components. The sensing element of the sensor prototype is a fiber coil with a length of 500 m. Experimental and numerically-calculated waveforms match very well demonstrating the model’s ability to accurately predict the experimental reality. The comparison has been carried out applying to the gyro prototype an angular rate of ± 0.44 rad/s. Two different modulating signals, squared and sine-wave, have been used for the validation. The achieved results pave the way for the development of a complete model of the gyro, which also includes the readout electronics.

Keywords: Optoelectronics · Photonics · Gyroscope · FOG · Model

1 Introduction

The interferometric fiber optic gyroscope (IFOG) is an angular velocity sensor that plays a crucial role in inertial measurement units for aerospace, defense, and emerging autonomous systems. Its high precision and accuracy, absence of moving parts, large dynamic range, and reliability in harsh environments make it one of the preferred choices for these applications [1]. Despite its commercial availability for over five decades and numerous theoretical and experimental studies, recent technological advancements have opened new possibilities. Innovations that were once deemed unrealistic are now feasible, enabling the development of IFOGs or more broadly, interferometric optical gyroscopes, with SWaP-C (size, weight, power consumption, and cost) budgets comparable to those of MEMS gyroscopes, while maintaining navigation-grade performance, high reliability, and strong immunity to disturbances even in hostile environments.

Recent progress in Silicon Photonics, the advent of miniaturized high-performance fiber coils with diameters of a few tens of millimeters, and significant advances in digital readout techniques, including AI-enhanced methods, have sparked renewed interest in IFOG miniaturization [2]. For instance, an ultra-small interferometric fiber optic gyroscope integrating a Silicon Photonics chip, an application-specific integrated circuit,

and a small-diameter sensing coil has been reported, showcasing intermediate-grade performance within a compact form factor of 30 mm × 30 mm × 30 mm and a weight of 68 g [3]. Additionally, recent developments have seen both active and passive IFOG components excluding the fiber coil and light source monolithically integrated on a Si-based photonic integrated circuit [4]. These photonic chips are poised to become the foundational elements of future miniaturized IFOGs.

Developing a numerical model that accurately simulates the experimental realities and the main physical effects involved in the operation of IFOGs is essential for several reasons: (i) it facilitates the conception, study, and assessment of innovative readout techniques; (ii) it aids in the proper interpretation of experimental results during the validation and demonstration of new IFOGs; and (iii) it assists in setting up complex models and digital twins of units, subsystems, and systems that include the IFOG, such as the attitude and orbit control subsystem of a satellite. Although some Matlab/Simulink models of the IFOG have been reported in the literature, they have not undergone experimental validation, casting doubt on their predictive accuracy [5].

This paper reports on a Matlab-based model that simulates the behavior of all optoelectronic and photonic components of the angular rate sensor. An IFOG prototype, assembled using only commercially available off-the-shelf components, was integrated and tested under rotation, subsequently serving as the basis for model validation.

2 Numerical Model

The implemented numerical model is based on the equations describing the IFOG behavior. All the photonic and optoelectronic components of the rotation rate sensor have been mathematically modeled, in order to simulate the IFOG output signal. Furthermore, to model the actual behavior of the IFOG, the primary sources of noise and disturbance that affect the output signal of the rotation rate sensor have been introduced into the numerical model. The input power drift and the Kerr effect are some of these noise sources, in addition to the shot and thermal noise introduced by electronic components.

The variation in time of the optical power emitted by the broadband source depends on various unpredictable factors, including changes in ambient temperature, aging of the light source, or variations in the electrical power supply. This effect has been introduced into the numerical model as white noise with a Gaussian distribution and a mean value equal to zero. The noise is added to the value of the light source emitting power P_{in} , which, in the ideal case, should be constant. The broadband source's noisy emitting power is time-dependent and is expressed as in Eq. (1).

$$P_{in}(t) = P_{in} + n(t) \quad (1)$$

In Eq. (1) $n(t)$ represents the modeled noise component.

The Kerr effect is a non-linear source of disturbance in the rotation rate sensor, that is induced by the mismatch between the optical power of the light beams counter-propagating in the fiber coil. A spurious difference in phase $\Delta\phi_k$ between the clockwise (CW) and counterclockwise (CCW) waves that counterpropagate inside the fiber coil, has been introduced due to the non-linear variation of the fiber refractive index.

The difference in phase between the two modulated counterpropagating waves after the interference is then expressed as in Eq. (2).

$$\Delta\phi_m(t) = \phi_m(t) - \phi_m(t - \Delta\tau_g) + \Delta\phi_k(t) \quad (2)$$

In Eq. (2) $\phi_m(t)$ is the phase shift related to the modulating signal waveform and $\Delta\tau_g$ represents the difference in group transit time between the CW and CCW waves. The spurious phase difference was modeled as a random variable with a Gaussian distribution and a mean value equal to zero. The introduction of undesired phase noise affects the angular rate accuracy of the sensor. However, this non-linear effect is generally attenuated by using a broadband source as a light source.

Furthermore, the noise components introduced by the photodiode and the electronics have been modeled. The electronic shot noise related to the photodetector and the thermal noise generated mainly within the transimpedance amplifier (TIA) limit the performance of the IFOG. The shot noise effect, which arises due to the discrete nature of electric charge, has been modeled through a Poisson distribution.

The thermal noise introduced by the electronic components has been modeled as white noise with Gaussian distribution and a mean value equal to zero. Shot and thermal noise contribute to the drift of the rotation rate sensor's output signal, as expressed in Eq. (3).

$$V_{out}(t, \Delta\phi_R) = G_{TIA} \cdot R \cdot P(\Delta\phi_R) + p(t) + g(t) \quad (3)$$

In Eq. (3) G_{TIA} refers to the gain of the transimpedance amplifier, R represents the photodetector responsivity, $p(t)$ represents the modeled shot-noise component, and $g(t)$ refers to the thermal noise component. $P(\Delta\phi_R)$ is the optical power response of the sensor that is related to the rotation induced phase difference $\Delta\phi_R$ between the two counterpropagating waves.

All the previously discussed noise sources have been introduced inside the model, which simulates the voltage at the photodetector output, as expressed in Eq. (4).

$$V_{out}(t, \Delta\phi_R) = G_{TIA} \cdot R \cdot \left(\frac{P_{in}(t)}{2} [1 + \cos(\Delta\phi_R + \Delta\phi_m(t))] \right) + p(t) + g(t) \quad (4)$$

3 Numerical and Experimental Results

The numerical model has been validated using an IFOG prototype that was entirely set up with commercially available components.

The prototype employed for model validation comprises a superluminescent diode (SLED) as a broadband light source, a fiber three-port circulator, a Multi-functional Integrated Optical Chip (MIOC) that includes a lithium niobate (LiNbO₃) push-pull phase modulator, a polarization maintaining fiber coil, and a module housing a germanium photodetector and a TIA.

The polarization maintaining fiber coil has a quadrupolar winding pattern for the Shupe effect mitigation, an internal diameter ID ≥ 80 mm and an external diameter OD ≤ 87 mm, the fiber total length is equal to 500 \pm 10 m.

Figure 1 shows a detailed block diagram of the IFOG prototype measurement setup, which includes a power supply for light source powering, a benchtop digital waveform generator for counterpropagating waves modulation, and a digital oscilloscope for the output signal acquisition. A coarse rotating stage has been used to apply angular velocities.

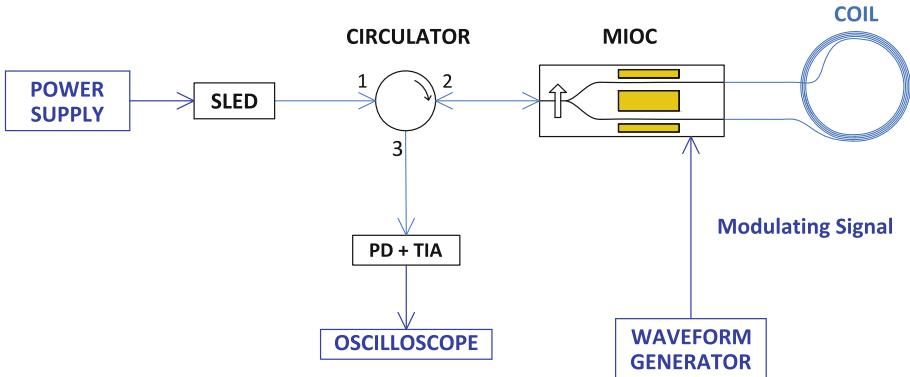


Fig. 1. Detailed block diagram of IFOG prototype measurement setup. PD: photodetector.

In order to validate the numerical model, the output signals of the IFOG prototype (voltage at the TIA output) have been acquired by the oscilloscope at a rotation rate of ± 0.44 rad/s. The validation has been carried out under two typical operating conditions, i.e., square-wave and sine-wave modulating signals.

In Figs. 2 and 3, the model output signal for a rotation rate of ± 0.44 rad/s, for square-wave and sine-wave applied modulating signals has been shown. The signal generated by the numerical model has been evaluated for five different iterations due to the stochastic nature of the model. At every iteration, the stochastic processes, which model the noise effect components, exhibit a different time evolution according to their likelihood density function. The magnitudes of the noise components have been chosen in order to have the best fit between the simulated signals and the signals measured by the oscilloscope.

As shown in Figs. 2 and 3, the noise components have a negligible impact on the IFOG prototype output signals; the waveforms remain predominantly unaffected by noise interference because mitigation strategies for the primary sources of disturbance are implemented in the IFOG prototype. Among the considered noise sources, the Kerr effect exerts the most significant influence. However, it is effectively mitigated by employing the SLED as light source.

For both square-wave and sine-wave modulation, the simulated output signals and the acquired signals exhibit very good agreement.

Through this comparison, the accuracy and reliability of the model are assessed, demonstrating its effectiveness in simulating the sensor's behavior with specific reference to the optoelectronic and photonic sections.

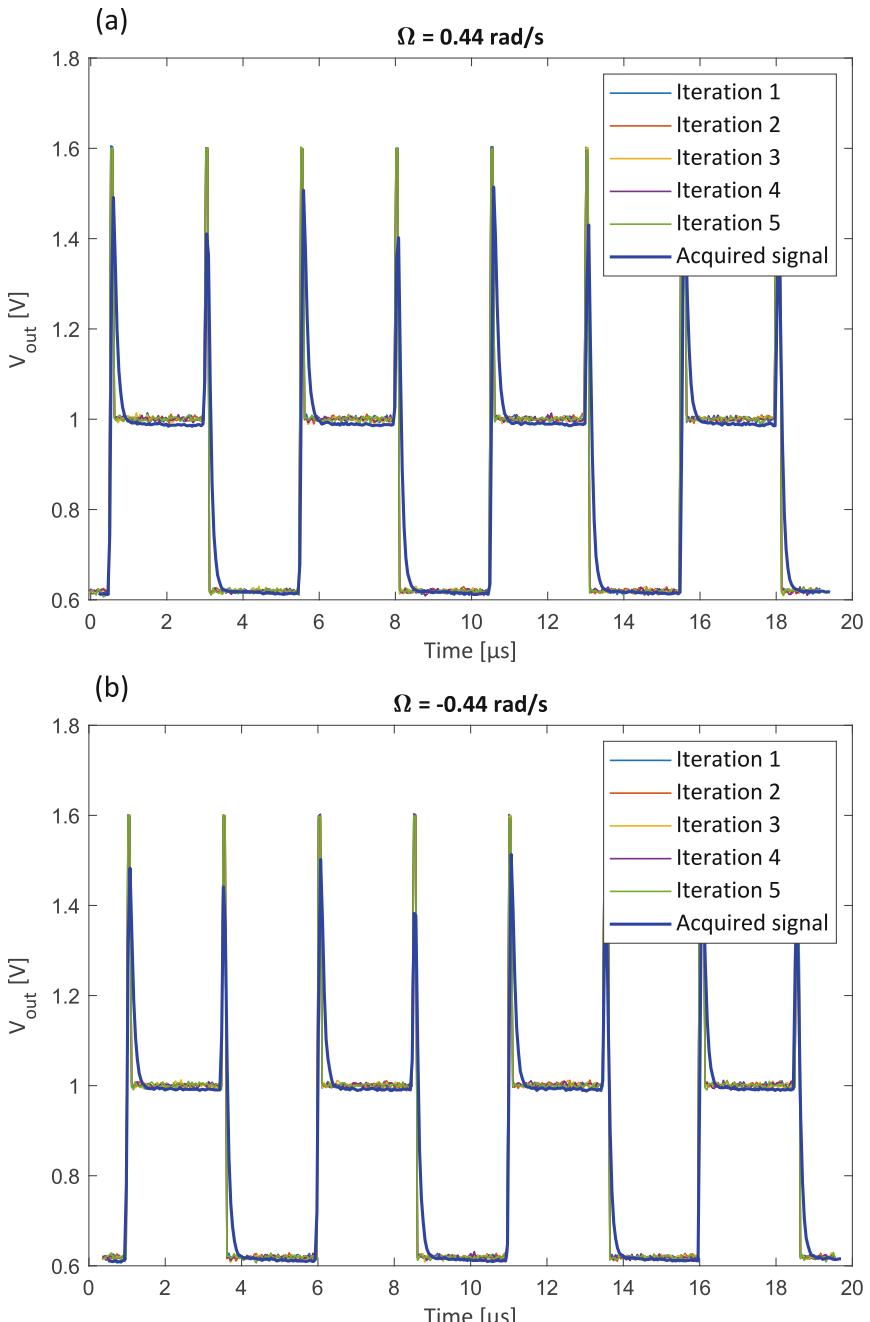


Fig. 2. Comparison between the numerical model output signals and the IFOG prototype output signals (blue lines) for CCW (a) and CW (b) applied rotation rates with a square-wave modulating signal

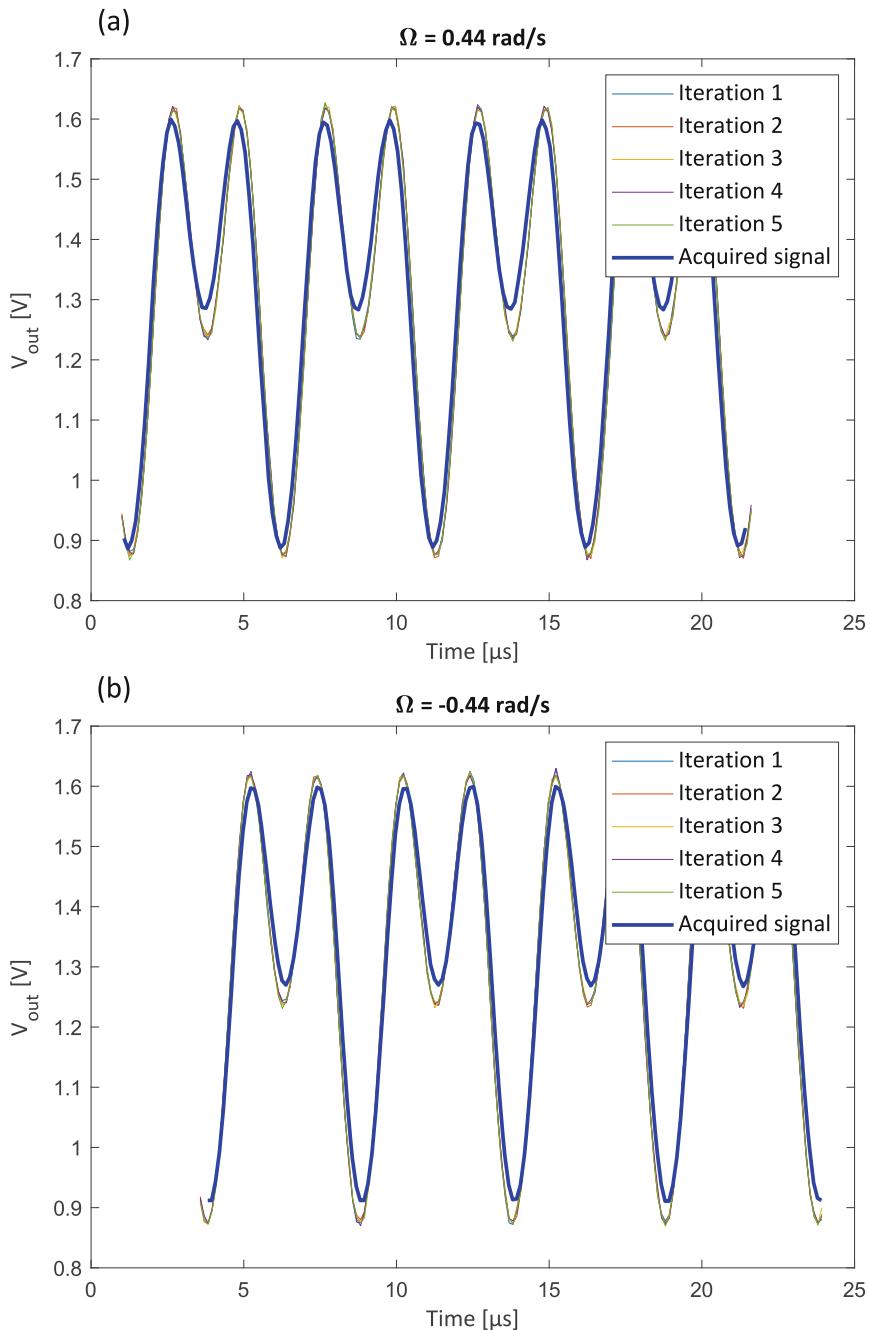


Fig. 3. Comparison between the numerical model output signals and the IFOG prototype output signals (blue lines) for CCW (a) and CW (b) applied rotation rates with a sine-wave modulating signal

4 Conclusions

In this paper a numerical model simulating the behavior of the photonic and optoelectronic components of the IFOG was presented. The model was validated by comparing the simulated output signals with the output signals of an IFOG sensor prototype entirely set up with commercially available off-the-shelf components. The validation assures that the model accurately simulates the main physical effects involved in the operation of IFOGs.

Furthermore, the inclusion of noise sources components that can affect rotation rate measurements allows the model to accurately simulate the IFOG in more complex systems and improve the interpretation of experimental results.

The reliable achieved results can allow the development of a more complex gyroscope model that also includes the read-out electronics.

References

1. Lefèvre, H.C.: The Fiber-Optic Gyroscope, 3rd edn. Artech House, 685 Canton Street Norwood, MA 02062 (2022)
2. Dell'Olio, F., Natale, T., Wang, Y.-C., Hung, Y.-J.: Miniaturization of interferometric optical gyroscopes: a review. *IEEE Sens. J.* **23**(24), 29948–29968 (2023)
3. Shang, K., et al.: Ultra-small interferometric fiber optic gyroscope with an integrated optical chip. *Chin. Opt. Lett.* **20**, art. no. 040601 (2022)
4. Wang, Y.-C., et al.: Silicon photonics multi-function integrated optical circuit for miniaturized fiber optic gyroscope. *J. Lightw. Technol.* **41**(19), 6324–6332 (2023)
5. Babu, G.H., Anuhya, A.V., Venkatram, N.: Digital signal processing scheme for open loop and closed loop IFOG using MATLAB/SIMULINK, **9**(11), 6324–6332 (2016)



A Novel Lab-on-Fiber Platform for Soil Water Content Monitoring

G. M. Berruti, M. Leone, P. Vaiano, G. V. Persiano, M. Consales^(✉),
and A. Cusano^(✉)

Università degli Studi del Sannio, 82100 Benevento, Italy
{consales, acusano}@unisannio.it

Abstract. We present a novel and high-sensitivity Lab-on-Fiber self-heating platform for accurate soil moisture monitoring. It is implemented by combining, within a conventional metallic needle, a standard fiber Bragg grating – working as temperature sensor- and a heating component realized by splicing two monomode fibers with a core offset. The sensor was extensively characterized in the range from 9 to 36%VWC and between 5 °C and 40 °C, providing extremely stable, fast and robust measurements, and exhibiting performance that are comparable with commercial devices. Moreover, the possibility to adjust the input power based on the specific application renders the developed sensor highly adaptable for deployment in extensive areas, offering significant advantages in terms of efficiency, cost reduction and simplicity.

Keywords: Lab-on-Fiber platform · Core-offset · Fiber Bragg grating sensor · Soil moisture sensor

1 Introduction

Soil moisture is an essential parameter in various disciplines such as farming, ecology, geotechnics, hydrologic and environmental engineering. A comprehensive understanding of soil moisture facilitates the development of optimized irrigation strategies, prevents water stress from excessive irrigation and enhances the final product quality. Furthermore, it is essential in reducing the negative effects that unexpected catastrophic floods and landslides have on the environment, the economy and society [1–3].

Traditional methods for monitoring soil volumetric water content (VWC), including time and frequency domain reflectometry (TDR and FDR) and capacitive sensors are inadequate for distributed monitoring over large areas due to the complexities associated with wiring and data logging when multiple sensing points are involved [2]. Table 1 presents an evaluation of the frequently applied techniques in the field of soil moisture measurements, summarizing their sensing principle and highlighting their respective advantages and limitations [4, 5]. In Table 2 the main performance of each method in terms of typical accuracy, measurement range and response time is reported [4, 5].

As an alternative to the traditional soil VWC measurement techniques, fiber optic sensors provide distinct advantages, such as resistance to harsh environment, multiplexity, and compactness, thus making them promising candidates for soil monitoring

Table 1. The most widely used techniques for soil VWC measurements: working principle, strengths and limitations.

Sensor Type	Working principle	Strengths	Drawbacks
TDR/FDR	VWC determination from the dielectric constant of soil (measurement of the time delay/frequency characteristics of electromagnetic pulses traveling through the soil itself)	- Easy to use - Accurate - Fast	- Expensive - Soil calibration required - Temperature correction required - Not suitable to monitor large areas
CAPACITIVE	VWC determination from the dielectric constant of soil (measurement of the capacitance between the electrodes and correlation with the VWC in the surrounding soil)	- Easy to use - Continuous monitoring	- Expensive - Soil calibration required - Temperature correction required - Not suitable to monitor large areas
NEUTRON PROBE SENSOR	VWC determination using elastic neutron scattering with hydrogen atom in soil	- Accurate - Fast	- Expert operator required - Expensive - Radiation hazard
TENSIOMETER	Soil water potential determination from the pressure difference between reference and surrounding	- Independent on soil type - Not affected by electrical conductivity and soil temperature	- Frequent maintenance - Not suitable under freezing conditions - Not suitable to monitor large areas
GYPSUM BLOCK	VWC determination using a resistance change of a porous substance in soil	- Easy to use - Low maintenance - Inexpensive	- Low accuracy - Affected by soil temperature and salinity - Frequent maintenance

in the field of precision agriculture [6]. Several fiber optic-based solutions for VWC measurements have been presented in literature and recently reviewed in [7]. In fiber optic-based distributed sensing approaches, electrically generated pulses are typically used to increase the soil temperature and the resulting thermal variation is used to evaluate the VWC [8–14]. Differently, the platform here proposed relies on the thermal gradient “self-generated” [15] through the use of two single mode fibers spliced together with a

core offset (CO) in the axial direction and determined by a fiber Bragg grating (FBG) realized within same fiber [4].

This platform was experimentally characterized at various soil temperatures in the range [5–40] °C and [9–36)%VWC, by varying the injected power between 112 mW and 214 mW. The reported data indicated that the device is capable to provide real time soil water content measurements with a resolution < 0.25%VWC, time response better than 10 s, and an impressive robustness (repeatability of $\pm 1.5\%$ VWC), thus making it very attractive for monitoring over long distances and/or in extended areas, also in presence of strict requirements in terms of energy consumption, compared to the commercial counterpart.

Table 2. Performance of the most widely used techniques in the field of soil VWC measurements

Sensor Type	Typical accuracy	Range of measurement	Response time
TDR	$\pm 2\%$ VWC	[0–50] %VWC	~30 s
FDR	$\pm 2\%$ VWC	[0–50] %VWC	Instant
CAPACITIVE	< ± 4 VWC%	[0–50] %VWC	Instant
NEUTRON PROBE SENSOR	< $\pm 5\%$ VWC	[0–50] %VWC	1–2 min
TENSIOMETER	$\pm 2\%$ VWC	[0–100] kPa	Instant
GYPSUM			
BLOCK	low	[0–200] kPa	2–3 h

2 Design and Fabrication

The proposed sensor consists of two primary components as depicted in Fig. 1: a CO fusion splice between two SM fibers – working as core-to-cladding coupling element – and a gold (Au)-coated FBG. Light propagating within the core of the fiber is transferred to the cladding and absorbed by the Au coating, causing heat generation and, thus, a thermal change in the soil volume surrounding the device [16, 17]. This thermal increase is correlated to the amount of VWC in the analyzed volume [4]. The presence of the FBG enables the real time determination of such thermal increase and, in turn, of the VWC. The final design of the device (CO value = 6 μm ; FBG length = 5 mm; Au layer length = 10 mm; Au layer thickness = 150 nm) resulted from an optimization process aimed at ensuring high thermal heating efficiency, while minimizing the total thermal mass [16, 17].

The device was housed within a stainless steel needle (approximately 40 mm in length, with internal and external diameters of 600 μm and 900 μm , respectively) acting as a protective capsule for safe deployment in soil while also minimizing the final thermal inertia. The sharp needle termination was sealed by means of a cyanoacrylate glue, while a couple of protective jackets were applied to the device (fiber + needle) to impart the necessary final robustness [4].

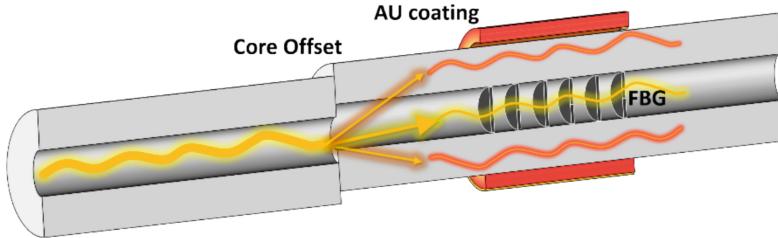


Fig. 1. Schematization of the Lab-on Fiber platform for VWC measurements in soil (Readapted from [4]).

The soil samples used for the experimental characterization (9%, 15.5%, 22.5%, 29.6%, 36%VWC) were prepared considering the gravimetric method [18] and the respective VWC values were measured through a commercial device (5TM from Decagon), serving as a reference sensor. The experimental set-up used for the sensor characterization has been previously detailed in [4]. Tests were conducted in the temperature range of [5–40] °C to additionally explore the impact of the thermal cross-sensitivity on the sensor readings.

3 Experimental Results

Figure 2 depicts the data provided by the Lab-on-Fiber platform to incremental VWC changes for an input power (P_{IN}) of ~110 mW at 20 °C is depicted in Fig. 2. Upon the injection of power into the device, a Bragg red wavelength shift ($\Delta\lambda_{BRAGG}$) was immediately recorded, attributable to the thermal gradient generated over the metallic layer and transferred to the needle. The efficiency of heat dissipation in the soil increases with higher VWC levels in the sample. Consequently, the generated thermal gradient ($\Delta T_{GENERATED}$) diminishes with rising VWC. The device demonstrated rapid response capabilities, with the signal typically transitioning from 10% to 90% of its total response in less than 10 s, thus exhibiting response time comparable to or better than the most commonly used techniques in the field of soil VWC, as presented in Table 2.

Figure 3 shows the results of an experimental sensor characterization in a soil sample at ~30% VWC with P_{IN} varying from 112 mW up to 214 mW. Higher P_{IN} leads to greater $\Delta\lambda_{BRAGG}$ and consequently, higher $\Delta T_{GENERATED}$ (as reported on the left and right axis of Fig. 3, respectively) [16, 17]. Remarkably, the use of the device under identical test conditions (e.g., fixed P_{IN} and fixed site in the soil) yields highly reproducible measurements, with the maximum $\Delta T_{GENERATED}$ being lower than 0.1 °C (less than the resolution of the optical fiber sensor acquisition system).

Figure 4 summarizes the response of the self-heated device at 20 °C across several soil samples (9%, 15.5%, 22.5%, 29.6%, 36%VWC) for incremental injected power values. Every data point is the result of an average among three tests conducted under the same conditions (the corresponding standard deviation is also reported). In agreement with previous works published in the literature [8–14], the sensor exhibited a non-linear response to VWC (a power function was used as fitting curve).

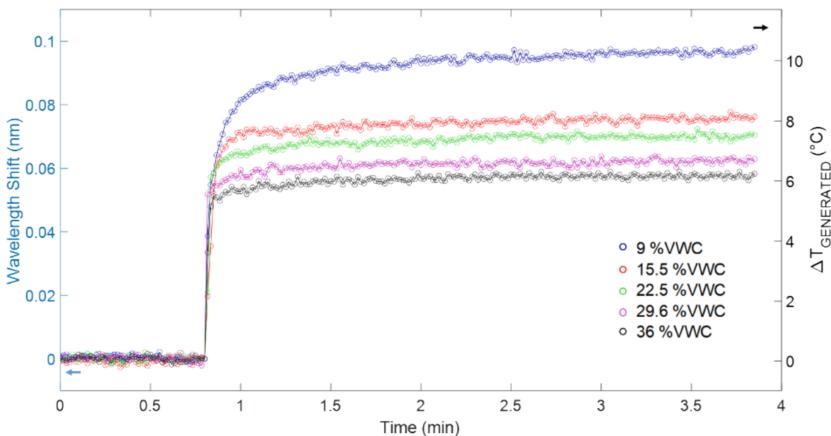


Fig. 2. Response of the Lab-On-Fiber device for soil VWC monitoring at 20 °C and $P_{IN} = 112$ mW (Readapted from [4]).

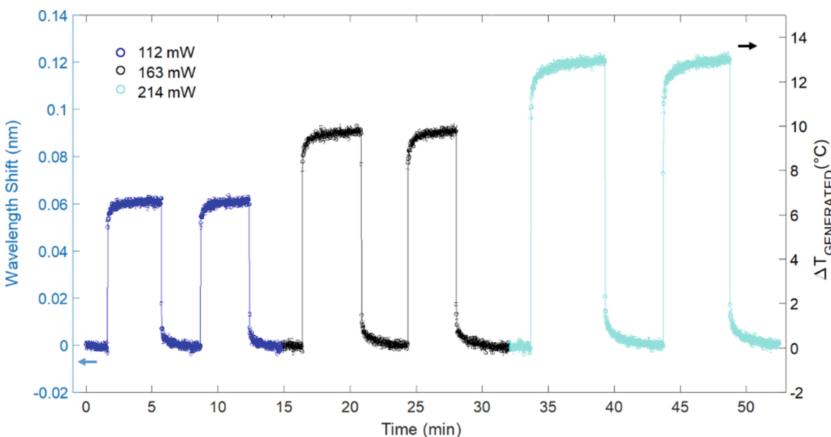


Fig. 3. Lab-On-Fiber sensor response at 20 °C and 29.6%VWC for different P_{IN} (Readapted from [4]).

The sensitivity of the Lab-on-Fiber platform, evaluated as the ΔT generated by a 1%VWC change, was retrieved by deriving the characteristic curves depicted in Fig. 4. It was found to decrease as the soil water content increases (Fig. 5(a)). For instance, for $P_{IN} = 112$ mW and 15%VWC the absolute value of sensitivity is ~ 0.22 °C/%VWC against ~ 0.04 °C/%VWC as evaluated in case of 35%VWC, for the same injected power value. The sensor resolution, defined as the smallest detectable VWC variation, was also assessed, as illustrated in Fig. 5 (b). By injecting $P_{IN} = 112$ mW, a very small resolution of $\sim 0.24\%$ VWC was achieved, while a high resolution of $\sim 0.12\%$ VWC was registered when applying 214 mW.

The sensor repeatability was also assessed after several insertion, extractions and reinsertions of the device into the soil. This study is crucial if considering that the soil

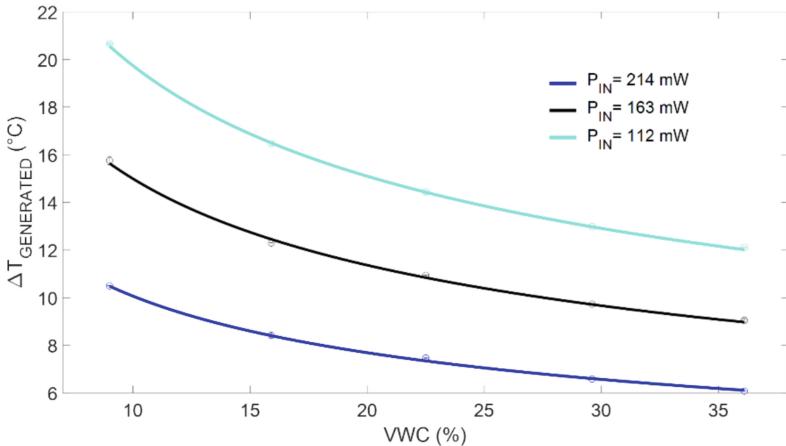


Fig. 4. Characteristic curves at 20 °C for P_{IN} in the range [112 – 214] mW (Readapted from [4]).

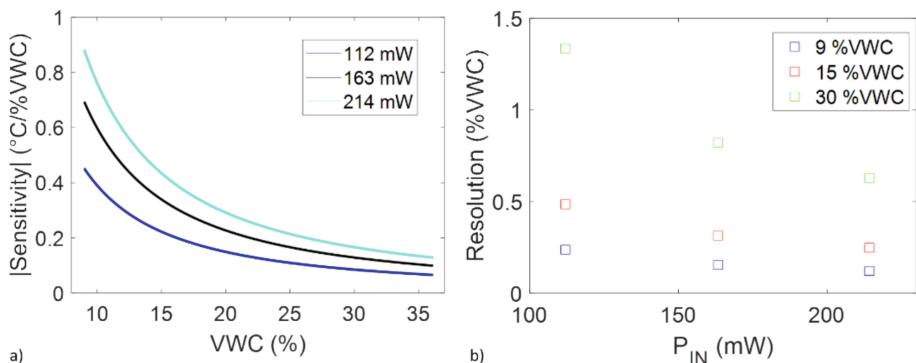


Fig. 5. a) Sensitivity and b) resolution of the proposed Lab-On-Fiber platform (Readapted from [4]).

compaction and granulometry may affect the response of each type of VWC sensor [19]. To this aim, tests were conducted, initially inserting the fiber optic device into the soil sample at approximately 12.4% VWC, and then extracting and reinserting it for subsequent measurements (5 repetitions with $P_{IN} = 214$ mW). An average value of $\Delta T_{GENERATED}$ at $18.8 \text{ }^{\circ}\text{C} \pm 1.0 \text{ }^{\circ}\text{C}$ was measured (Fig. 6) corresponding to $11.8 \pm 1.5\%$ VWC. Similar values were collected from the Decagon 5TM sensor used as reference, which exhibited an s.t.d. of $\pm 0.5\%$ VWC. These findings, coupled with the minimal s.t.d. around $0.1 \text{ }^{\circ}\text{C}$ retrieved in the stationary conditions (Fig. 3), indicate that the variability in the sensor response primarily stems from changes in soil compaction near the needle, rather than instability issues.

The sensor temperature cross-sensitivity was also studied between 5 °C and 40 °C. Considering the same experimental conditions (P_{IN} and soil VWC), the sensor response

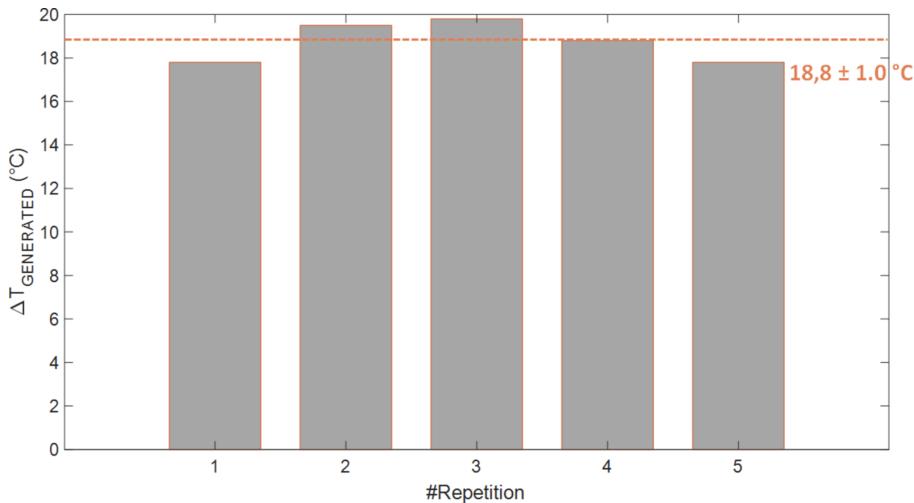


Fig. 6. Evaluations of the sensor repeatability (5 repetitions) (Readapted from [4]).

remained practically unaffected by variations in the soil temperature. Any slight fluctuations around the mean response ($\leq \pm 1.0$ °C) are coherent with the repeatability error attributed to the sensor removal and reinsertion into the soil sample, as previously highlighted.

It is important to emphasize that the sensing platform proposed here is suitable for both continuous and discrete soil water content measurements. The injected power value can be precisely tuned in order to satisfy the requirements of the specific application under analysis, while reducing energy consumption. In fact, by decreasing P_{IN} , the final energy expenditure can be minimized in trade off with the sensor performance and vice versa. With the aim of assessing the effect of increasing laser power on the energy consumption of the final system, the minimum time required for the output signal to stabilize after triggering the optical heating pulse ($t_{settling}$) was retrieved and the energy ingesting needed for each heating was calculated as a function of P_{IN} ($E_{consumption} = t_{settling} \cdot P_{IN}$). To this aim, the fixed consumptions associated with the data acquisition system's operation, the pump laser, and the optical interrogator were disregarded. The results in Table 3 show that the choice of P_{IN} is the result of a trade-off between the sensitivity and resolution of the self-heated device and the overall system energy efficiency. For example, injecting 112 mW for 21 s into the fiber optic device results in an energy consumption of about 0.6 mWh, which is around three times less than injecting 214 mW for 30 s [4].

Table 3. Energy needed for each VWC measure

PIN [mW]	Settling time [s]	Energy Consumption [Wh]
112	21	$0.6 \cdot 10^{-3}$
163	23	$1.0 \cdot 10^{-3}$
214	30	$1.8 \cdot 10^{-3}$

4 Conclusions

In this paper, an innovative self-heated Lab-on-Fiber sensing platform based on FBG technology for water content measurements in soil is experimentally demonstrated. The sensor performed similarly to the most popular and extensively used methods for soil VWC monitoring, demonstrating high stability and fast response. Furthermore, the possibility to adapt the input power based on the specific application makes it particularly flexible and suitable for large-scale or long-range monitoring tasks.

References

1. Datta, S., Taghvaeian, S., Stivers, J.: Understanding Soil Water Content and Thresholds for Irrigation Management. Oklahoma Cooperative Extension Service (2017)
2. Dobriyal, P., et al.: A review of the methods available for estimating soil moisture and its implications for water resource management. *J. Hydrol.* **458**, 110–117 (2012)
3. Breglio, G., et al.: Innovative photonic sensors for safety and security, Part III: environment, agriculture and soil monitoring. *Sensors* **23**(6), 3187 (2023). <https://doi.org/10.3390/s23063187>
4. Berruti, G.M., et al.: All-optical active sensing platform for continuous and sustainable soil water content monitoring. *Opt. Lasers Eng.* **178**, 108209 (2024)
5. Rasheed, M.W., et al.: Soil moisture measuring techniques and factors affecting the moisture dynamics: a comprehensive review. *Sustainability* **14**(18), 11538 (2022)
6. Leone, M., et al.: Fiber optic thermo-hygrometers for soil moisture monitoring. *Sensors* **17**(6), 1451 (2017)
7. Leone, M.: (INVITED)Advances in fiber optic sensors for soil moisture monitoring: a review. *Results in Optics* **7**, 100213 (2022). <https://doi.org/10.1016/j.rio.2022.100213>
8. Steele-Dunne, S., et al.: Feasibility of soil moisture estimation using passive distributed temperature sensing. *Water Resources Research*, **46**(3) (2010)
9. Sayde, C., et al.: Feasibility of soil moisture monitoring with heated fiber optics. *Water Resour. Res.* **46**(6) (2010)
10. Striegl, A.M., Loheide, S.P., II.: Heated distributed temperature sensing for field scale soil moisture monitoring. *Groundwater* **50**(3), 340–347 (2012)
11. Dong, J., et al.: The impacts of heating strategy on soil moisture estimation using actively heated fiber optics. *Sensors* **17**(9), 2102 (2017)
12. Benítez-Buelga, J., et al.: Heated fiber optic distributed temperature sensing: a dual-probe heat-pulse approach. *Vadose Zone J.* **13**(11), 1–10 (2014)
13. Vidana Gamage, D.N., et al.: Soil water measurement using actively heated fiber optics at field scale. *Sensors* **18**(4), 1116 (2018)

14. Vidana Gamage, D.N., et al.: Comparison of heating strategies on soil water measurement using actively heated fiber optics on contrasting textured soils. *Sensors*. **21**(3), 962 (2021)
15. Wang, J., et al.: Rapid response all-fiber moisture sensor. *IEEE Sens. J.* **22**(11), 10594–10601 (2022)
16. Berruti, G.M., et al.: Highly efficient fiber optic thermal heating device based on turn-around-point long period gratings. *J. Lightwave Technol.* **40**(3), 797–804 (2021)
17. Berruti, G.M., et al.: Turn-Around-Point Long Period Gratings As Core-To-Cladding coupling mechanism For Highly Efficient Thermal Heating Devices. *Optical Fiber Sensors.Optica Publishing Group* (2022)
18. Schmugge, T.J., Jackson, T.J., McKim, H.L.: Survey of methods for soil moisture determination. *Water Resour. Res.* **16**(6), 961–979 (1980). <https://doi.org/10.1029/WR016i006p00961>
19. Leib, B.G., Jabro, J.D., Matthews, G.R.: Field evaluation and performance comparison of soil moisture sensors. *Soil Sci.* **168**(6), 396–408 (2003)



Integrating CMOS Analog Electronics in Silicon Photonics

Francesco Zanetto¹(✉) Monica Crico¹ Samuele De Gaetano¹ Giorgio Ferrari² and Marco Sampietro¹

¹ Department of Electronics, Information and Bioengineering, Politecnico di Milano,
piazza Leonardo da Vinci 32, 20133 Milan, Italy
francesco.zanetto@polimi.it

² Department of Physics, Politecnico di Milano, piazza Leonardo da Vinci 32, 20133
Milan, Italy

Abstract. We present the integration of CMOS analog electronics into a pure Silicon Photonics platform, fabricated without modifying the conventional fabrication stack of photonic fabs. The electronics targets the detection and processing of electrical signals directly on the photonic chip. We show the operation of multiplexers for sequentially controlling large-scale photonic systems with few electrical signals and of a transimpedance amplifier for on-chip light monitoring. These examples represent a first step towards complex electronic processing and elaboration in standard Silicon Photonics.

Keywords: Silicon Photonics · CMOS electronics · monolithic integration · electronic multiplexers · transimpedance amplifier

1 Introduction

Silicon Photonics (SiP) has enabled the integration of hundreds of photonic devices in a compact silicon chip, paving the way to designing large-scale optical systems for complex manipulation of light beams. In addition to its excellent optical properties, silicon owes its success as a photonic material because it can be processed with the same mature fabrication facilities of the microelectronic industry. This latter aspect has stimulated the investigation of monolithic electronic-photonic chips, combining the unrivaled bandwidth of optical devices with the versatility of CMOS electronics [1]. Integrating photonic devices into mature microelectronic stacks, properly modified to maximize speed and energy performance, has been successfully pursued to design high-speed transceivers operating at hundreds of Gbit/s [2, 3], thanks to the reduction of parasitic effects that results from placing electronic and photonic devices in close proximity. However, due to its high cost, this approach still struggles to gain popularity in those applications where photonic functionalities prevail and large-scale optical circuits are needed, as in optical computers, quantum photonic processors and neuromorphic systems [4–6]. To overcome this limitation, the opposite approach has

been proposed, with the successful integration of CMOS devices and digital circuits into standard SiP technologies [7]. Although these devices do not show the same performance of state-of-the-art microelectronics, they allow the processing of electrical signals directly on the photonic chip, enabling the control of a large number of optical devices with few external connections [8]. Here, we further extend this concept and show that analog electronic circuits can also be integrated in purely photonic platforms, opening the way to on-chip amplification and processing of electrical signals.

2 CMOS Transistors in Standard Silicon Photonics Technologies

CMOS transistors have been successfully integrated into the photonic chip with a zero-change approach, achieved by using only the fabrication steps already available in the standard technological stack of a commercial photonic foundry (Advanced Micro Foundry, Singapore). Since in SiP technologies the metal layers are relatively far from the silicon to ensure minimum propagation losses in waveguides, the transistors have been designed with lateral silicon gates, by exploiting the minimum waveguide-to-waveguide distance of around 200 nm. The channel width W is thus determined by the silicon layer thickness and is equal to 220 nm. The drain and source contacts have been n -doped (10^{17} cm^{-3}), while a p -type diffusion defines the bulk region. The channel length has been optimized to 4 μm through software simulations to ensure low leakage currents in the off state. Thanks to the intrinsic device isolation given by the silicon-on-insulator (SOI) technology, the bulk and source contacts of each MOSFET have been short-circuited to reduce the body effect. The final transistor is a symmetric elementary cell obtained by mirroring the described structure along the source-drain axis, as shown in Fig. 1a. The two lateral gates have been connected with a common top metal electrode. In order to achieve the desired transistor form factor, the proper number of cells can be connected in series or parallel.

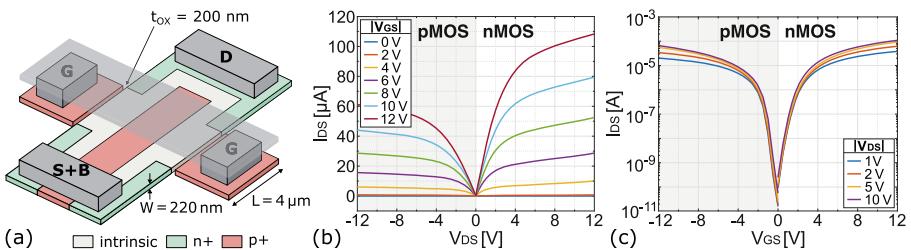


Fig. 1. a) Schematic view of the nMOS transistor structure and measured b) characteristic and c) transcharacteristic curves of both nMOS and pMOS devices.

Both nMOS and pMOS devices have been realized, employing the same geometry while inverting the doping species of the diffusion regions. A reasonably low

threshold voltage around 2 V has been achieved thanks to the fact that the native silicon layer of a photonic chip is naturally depleted of free carriers [7] and it can thus be used as the substrate for both types of transistor. The two devices have been electrically validated, as shown in Figs. 1b and 1c which report their characteristic and transcharacteristic curves, respectively. The devices show good conductivity, a high on-off current ratio and an Early voltage larger than 30 V, demonstrating their correct functionality. The transistors have thus been used to integrate more complex circuits for processing electrical signals on the photonic chip.

3 On-Chip Multiplexers for Sequential Control of Photonic Chips

Figure 2a shows an innovative approach enabled by integrating analog electronics into a programmable photonic circuit (PIC), implemented as a mesh of Mach-Zehnder interferometers (MZI) whose functionality is monitored and controlled at run-time with sensors and actuators. As the number of photonic building blocks increases, the quantity of electrical input-output (IO) connections and the complexity of the external control electronics explode, limiting the scalability of this closed-loop approach. This issue is overcome by serializing the control action with on-chip multiplexers (MUX). One MUX is used to sequentially read the on-chip sensors with a single readout circuit. Similarly, the actuators are driven sequentially through an on-chip demultiplexer (DEMUX). Being most of the photonic actuators volatile, an on-chip electronic memory is needed. This can be achieved by designing a Sample&Hold (S&H) circuit, connected to the power transistors that drive the actuators. The S&H exploits the switches of the DEMUX and a bank of memory capacitors to provide on-chip memory action. To automatically tune each MZI, the dithering technique in combination with integral controllers has been used. The dithering frequency has been set to 2 kHz and the switching of readout MUX to 80 kHz to avoid aliasing in the readout. The deserializer, dithering extraction block, integral controllers and management logic needed to control the chip have been implemented with an FPGA on the external electronic control board. A photograph of the fabricated circuit is shown in Fig. 2b.

Figure 2c reports the measured variation of optical power at the output of a MZI when its heater is controlled with the S&H. The output of the MZI remains stable when the S&H refresh period is kept below 100 ms, which represents the maximum hold time of the circuit. Since the DEMUX addressing can be updated in around 500 ns to select a different actuator [8], hundreds of devices can be effectively multiplexed without relevant penalties on the chip performance. Next, the correct sequential control of the MZIs has been tested. Light has been injected at input port IN1 of the chip and the circuit has been configured to extract it from the output port OUT. Figure 2d shows the automated configuration transient of the mesh. Despite the time-multiplexed approach, the circuit is configured in less than 10 ms, certifying the correct functionality of the on-chip components and

the off-chip electronics. The proposed approach thus provides a scalable solution to extend the control paradigm to hundreds of photonic components without correspondingly extending the number of electrical IOs and external electronic components.

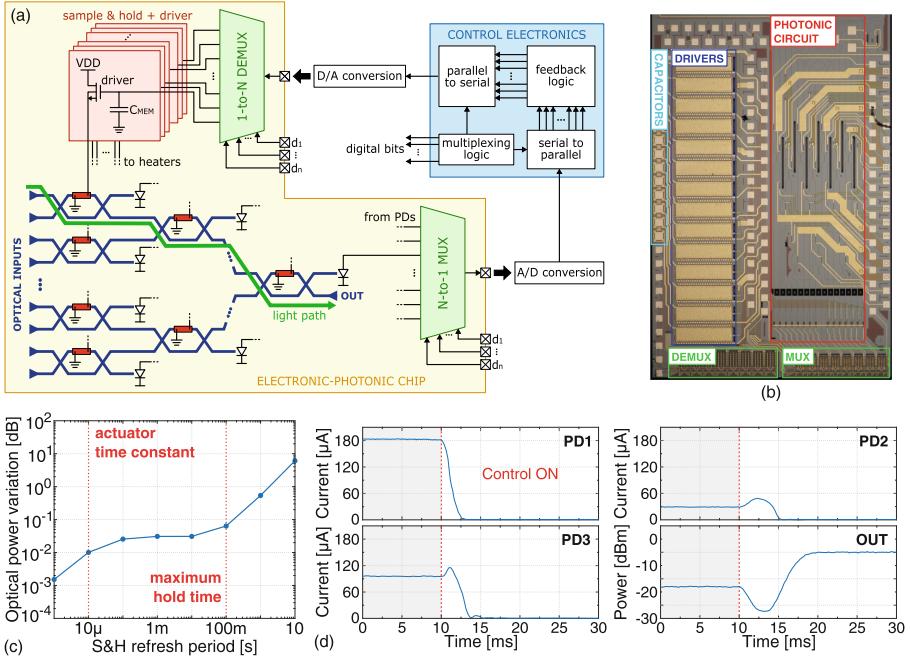


Fig. 2. a) Schematic view of a programmable PIC with on-chip MUXes and S&H circuits. b) Photograph of the realized chip. c) Optical power variation at the output of a MZI when controlling its heater with the S&H, showing no penalties for refresh periods below 100 ms. d) PD currents and output power during the mesh configuration for the IN1-to-OUT path, happening in less than 10 ms

4 Transimpedance Amplifier for on-Chip Light Monitoring

An important electronic building block for on-chip processing and amplification of electrical signals is the operational transconductance amplifier (OTA), which can be used to integrate complex circuits on the photonic chip to monitor and control its behavior. A two-stage operational transconductance amplifier (OTA) has been designed to implement the TIA, as shown in Fig. 3a. The schematic shows the number of MOSFET cells connected in parallel to implement each transistor. The input nMOS pair is biased by a transdiode current generator,

while a current mirror active load guarantees high differential gain and rejection of common-mode signals. Extra gain is provided by a second amplification stage, which is compensated with a Miller capacitance of 600 fF to obtain the desired single pole frequency response. The circuit has been designed to have an open-loop gain of about 40 dB, a gain-bandwidth product of few MHz and a series white noise around $50 \text{ nV}\sqrt{\text{Hz}}$. It operates with a supply voltage of 5 V and has a static power consumption of $400 \mu\text{W}$. The amplifier has been connected in transimpedance configuration with a feedback resistance of $10 \text{ k}\Omega$. A test structure has been fabricated to characterize and validate the operation of the TIA, as shown in Fig. 3b. It is made of a straight waveguide that injects light to an integrated germanium photodiode connected to the on-chip amplifier. The PD, having a responsivity of 0.8 A/W , is provided by the foundry process design kit. To precisely compare the readout performed by the integrated amplifier with conventional bench-top instrumentation, a 90-10 splitter has been used to route 10% of the injected light signal out of the chip. A laser source at 1550 nm, with a variable optical attenuator (VOA) connected to its output, has been used in all the experiments.

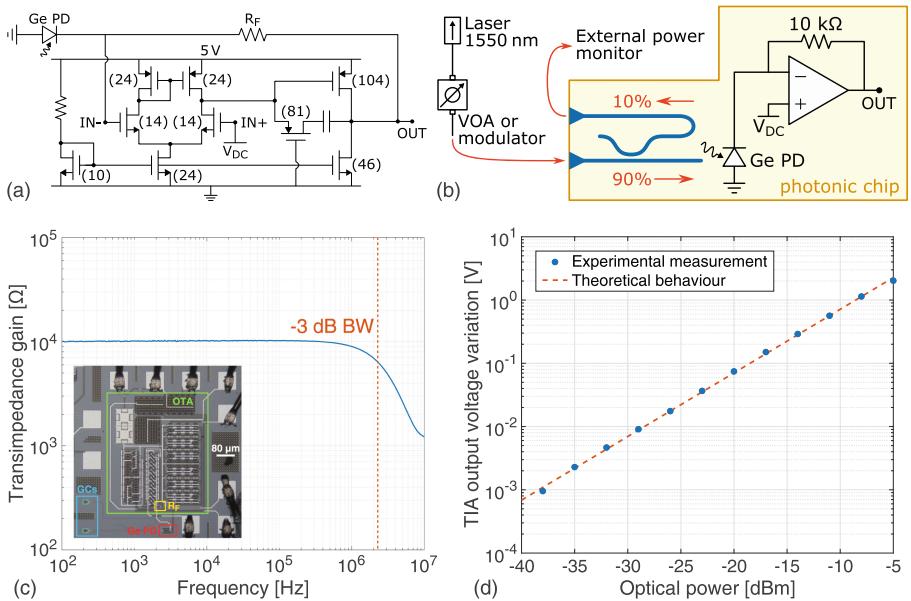


Fig. 3. a) Schematic of the transimpedance amplifier connected to the on-chip germanium photodiode. b) Experimental setup for the characterization of the chip. c) Measured frequency response of the TIA. The inset shows the chip microscope photograph. d) Voltage variation at the TIA output as a function of the optical power reaching the photodiode. The circuit can detect signals down to -40 dbm .

The fabricated amplifier has been first electrically characterized by testing its frequency response (Fig. 3c), showing a -3 dB bandwidth of about 2 MHz, wide enough to perform effective monitoring of the optical power in the most common applications. Then, optical characterization has been carried out. The input light power has been progressively attenuated and the corresponding voltage variation has been measured at the output of the TIA. The relation between optical power and output voltage is linear (Fig. 3d), in agreement with the theoretical behavior, demonstrating the correct operation of the amplifier. The lowest signal that the circuit can detect is around -40 dBm with a 100 Hz readout bandwidth, highlighting the good sensitivity that makes the TIA suitable to perform effective on-chip optical power monitoring.

5 Conclusions

We demonstrated that it is possible to monolithically integrate CMOS electronic circuits on pure photonic platforms, manufactured by commercial foundries without modifications to the standard fabrication flow. First, we showed the possibility of controlling silicon photonic circuits by time-multiplexing on-chip the electrical signals needed to read the sensors and drive the actuators. Non-volatility has been provided to the actuators by integrating a monolithic S&H circuit, with a maximum hold time of 100 ms. A time-multiplexed control strategy has also been developed, allowing the configuration of a MZI mesh in around 10 ms, comparable to the conventional parallel approaches. Then, we integrated a transimpedance amplifier for on-chip optical power monitoring, suitable for reading current signals from integrated germanium photodiodes with a frequency up to 2 MHz and a power down to -40 dBm. This approach will be further developed by employing the realized circuits as a building block for more complex analog structures, aiming at bringing more and more electronic functionalities on the photonic chip.

Acknowledgements. The authors acknowledge A. Melloni, F. Morichetti, A. Martinez, S. Seyedinnavadeh and the Photonic Devices Lab of Politecnico di Milano for joint design and test of the photonic chips. The authors thank Polifab, the nanofabrication facility of Politecnico di Milano, for wirebonding and dicing the chips.

References

- Thomson, D., et al.: Roadmap on silicon photonics. *J. Opt.* **18**(7), 073003 (2016)
- Rakowski, M., et al.: 45nm CMOS - silicon photonics monolithic technology (45CLO) for next-generation, low power and high speed optical interconnects. In: Optical Fiber Communications Conference (OFC), paper T3H.3 (2020)
- Sun, C., et al.: Single-chip microprocessor that communicates directly using light. *Nature* **528**(7583), 534–538 (2015)
- Kari, S.R., Nobile, N.A., Pantin, D., Shah, V., Youngblood, N.: Realization of an integrated coherent photonic platform for scalable matrix operations. *Optica* **11**(4), 542–551 (2024)

5. Bartlett, B., Fan, S.: Universal programmable photonic architecture for quantum information processing. *Phys. Rev. A* **101**(4), 042319 (2020)
6. Pai, S., et al.: Experimentally realized *in situ* backpropagation for deep learning in photonic neural networks. *Science* **380**(6643), 398–404 (2023)
7. Zanetto, F., et al.: Unconventional monolithic electronics in a conventional silicon photonics platform. *IEEE Trans. Electron. Devices* **70**(10), 4993–4998 (2023)
8. Zanetto, F., et al.: Time-multiplexed control of programmable silicon photonic circuits enabled by monolithic CMOS electronics. *Laser Photon. Rev.* 2300124 (2023)



Detection of Selected IR Signatures Through SEIRA Sensing Platform

Valentina Di Meo¹, Alessio Crescitelli¹, Massimo Moccia², Emanuela Iaccarino³, Annamaria Sandomenico³, Vincenzo Galdi², Menotti Ruvo³, Ivo Rendina¹, and Emanuela Esposito¹(✉)

¹ Institute of Applied Sciences and Intelligent Systems, National Research Council, Rome, Italy
emanuela.esposito@cnr.it

² Fields & Waves Lab, Department of Engineering, University of Sannio, Benevento, Italy

³ Institute of Biostructures and Bioimaging, National Research Council, Rome, Italy

Abstract. In this work, a pixeled plasmonic metasurface has been employed as a Surface Enhanced InfraRed Absorption (SEIRA) spectroscopy platform to detect small amounts of compounds containing a peculiar IR signature. In particular, the N₃ bonds vibrational feature (placed around 2100 cm⁻¹) has been chosen due to its location far from the fingerprint region. The proposed platform has demonstrated its capability to detect and amplify the selected IR signature with a compound containing the abovementioned vibrational feature. In particular, the K molecule (Ac-Lys(N₃)-Cys-NH₂) has been considered as a proof of principle molecule, showing both a strong absorption peak corresponding to the detection of the N₃ bonds and a maximum redshift of 65 cm⁻¹ as compared to the naked sensors.

Keywords: Plasmonic Metasurface · Surface Enhanced InfraRed Absorption Spectroscopy · Pixeled platform · Biosensing · Nanoplasmonics

1 Introduction

Mid-infrared (MIR) spectroscopy is a powerful technique that allows the label-free and real time identification of a target molecule through its characteristic vibrational spectrum, especially in the fingerprint region (1500–600 cm⁻¹) [1–3]. Among all the mid-IR possible spectroscopic techniques, Fourier-Transform IR (FTIR) is one of the most commonly used for the structural analysis of chemical and biological molecules. This is due to the possibility to provide structural information on the target analyte in a non-invasive and univocal way [4]. However, due to the low absorption cross-section of infrared vibrations at low concentrations, this technique could fail to detect small amounts of analytes. Surface Enhanced Infra-Red Absorption (SEIRA) spectroscopy allows to overcome this limitation by boosting the light-matter interaction at molecular sites [5–8]. In particular, pixeled metasurfaces (MS) constituted by metallic nanoantennas (NAs) arranged in 2-D periodic arrays with different geometrical parameters can be engineered to support localized surface plasmonic resonances (LSPRs) exactly tuned with the vibrational modes of molecule to be revealed, in order to detect the IR signals coming from very low amounts of a target analytes captured from a solution [9, 10].

In this study, a pixeled plasmonic MS has been employed to study the capabilities of the proposed sensing platform to detect small amounts of analytes containing the N₃ bonds, vibrating around 2100 cm⁻¹. This vibrational feature has been chosen due to its location in a MIR region placed quite far from the rich fingerprint region [11], thus making it employable as a typical IR signature in bioprobes suitably modified to feature the presence of diagnostically and therapeutically relevant molecules or particles, including pathogens and viruses. In particular, the K molecule (Ac-Lys(N₃)-Cys-NH₂) has been employed as a proof of principle chemical probe bearing the abovementioned IR signature. This molecule has been successfully analyzed and detected, observing both a maximum redshift of about 65 cm⁻¹ compared to naked surfaces and the appearance of a strong absorbance peak at around 2100 cm⁻¹ related to the vibration of the N₃ bonds.

2 Materials and Methods

2.1 Metasurface Design

The proposed MS has been designed by means of commercial software COMSOL Multiphysics v.5.1. In particular, the design has been focused on gold cross-shaped NAs (thanks to their independence from the polarization of the impinging light) and, with a proper tuning of NAs geometrical parameters [8–10], it has been possible to place their plasmonic resonances in the range 900–2800 cm⁻¹. In particular, the NAs thickness t has been fixed to 50 nm, the cross arm width W has been fixed to 200 nm, while a parametric study based on the variation of the NAs cross arm length L and the array period P has been conducted to find the geometrical parameters set allowing to tune the plasmonic resonances of the different arrays to the desired wavelengths. The numerical analysis has been conducted on a 3D unit cell (represented in the inset of Fig. 1) assuming an infinite periodicity in the transverse plane (imposing periodic boundary conditions on the lateral walls) and normal incidence of a plane wave coming from the air region having a finite thickness of 10 μm, while for the substrate region (terminated with a perfect matched layer) a thickness of 5 μm has been considered.

In Fig. 1, a comparison of the numerical (black curve) and the experimental (red curve) reflection spectra of a representative pixel is shown. The slight discrepancy between the numerical and the experimental data can be attributed to the fabrication tolerances, always lower than 5%.

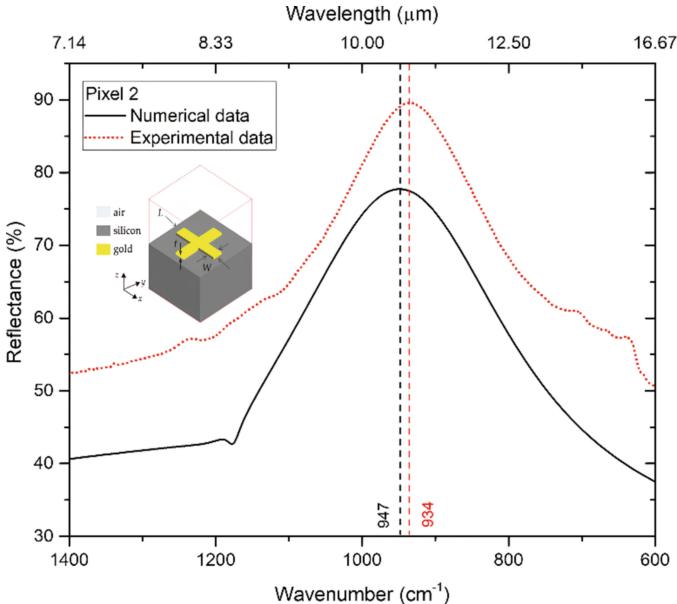


Fig. 1. Comparison between the numerical (black curve) and the experimental (red curve) data pertaining to a representative pixel (Pixel 2). The inset shows the 3D unit cell employed for the numerical simulations.

2.2 Metasurface Fabrication

All the simulated arrays have been fabricated on a float-zone silicon chip ($1.5 \text{ cm} \times 1.5 \text{ cm}$) by means of electron beam lithography and lift-off processes due to the high flexibility of use, reproducibility and reliability offered by this fabrication technique [12, 13]. Each pixel covers an area of $500 \mu\text{m} \times 500 \mu\text{m}$ and is identified by a unique number. In addition, a Cartesian axis system can be fixed in order to precisely find the pixel position on the silicon chip, as schematically shown in Fig. 2. Close to the pixels, four gold mirrors (covering each one an area of $200 \mu\text{m} \times 200 \mu\text{m}$) have been fabricated in order to have a gold reference for the normalization of the IR measurements on the same substrate and which is subjected to the same functionalization steps of the pixels.

In Table 1 are reported the experimental geometrical parameters and the plasmonic resonances of the fabricated pixels.

Table 1. Experimental parameters of the pixels fabricated on the proposed platform.

Pixel number	Geometrical parameters			Experimental resonances [cm ⁻¹]
	L [nm]	W [nm]	P [μm]	
#1	2285	203	2.5	800
#2	1980	200	2.5	934
#3	1685	200	2.0	1054
#4	1575	200	2.0	1163
#5	1383	200	2.0	1285
#6	1185	200	2.0	1406
#7	1080	200	2.0	1524
#8	1195	200	1.5	1534
#9	985	200	1.5	1740
#10	895	200	1.5	1871
#11	785	200	1.5	2082
#12	600	200	1.5	2784
#13	800	200	1.2	2163
#14	800	200	1.0	2313
#15	600	195	1.0	2765
#16	600	195	0.8	2815

2.3 Platform Functionalization and Characterization

The fabricated MS has been characterized by means of a Thermo-Nicolet iN10 MX FTIR spectrometer, by collecting the reflection spectra of each pixel with a 4 cm⁻¹ resolution over the range 4000–600 cm⁻¹ for 256 scans. All the reflection spectra have been collected first in air and then after the immobilization of the target molecule. In particular, a 600 ng/ml solution of K molecule (Ac-Lys(N₃)-Cys-NH₂, 317 Da molecular weight) was prepared by Fmoc solid phase synthesis (PMID: 29486214) using commercially available building blocks. This solution contained a thiol group for the oriented immobilization on the sensor gold surface and was drop casted and then dried at air on the plasmonic platform for 24 h before the IR characterization.

3 Experimental Results

The proposed MS has been functionalized with a solution of K molecule having a concentration of 600 ng/ml. All the collected reflectance spectra exhibit a strong absorption feature localized around 2100 cm⁻¹, corresponding to the vibrational feature of the N₃ bonds, together with the absorption band corresponding to the Amide I and Amide II bands present in the molecule (located in the ranges 1700–1620 cm⁻¹ and 1560–1500 cm⁻¹, respectively [14, 15]). The experimental curves pertaining to the 16 pixels present on the fabricated chips are shown in Fig. 3.

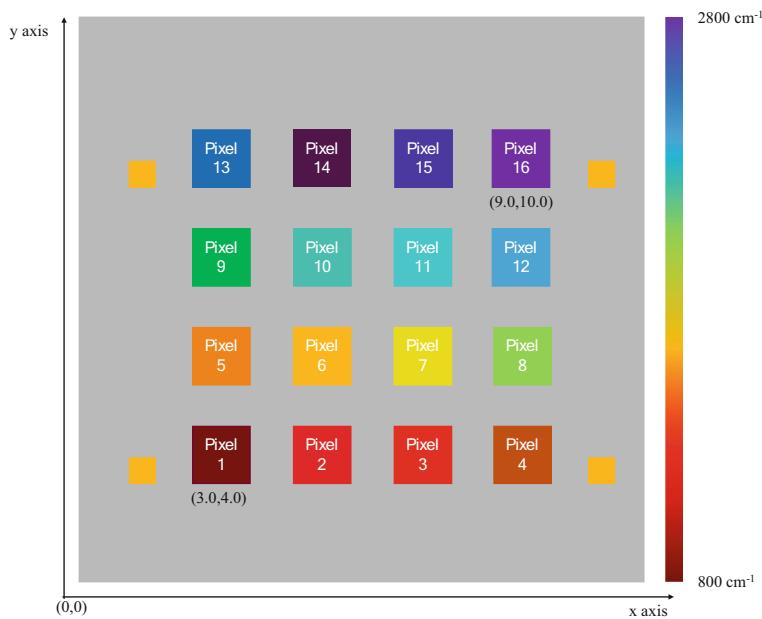


Fig. 2. Schematic representation of the fabricated MS comprising 16 pixels having different plasmonic resonances.

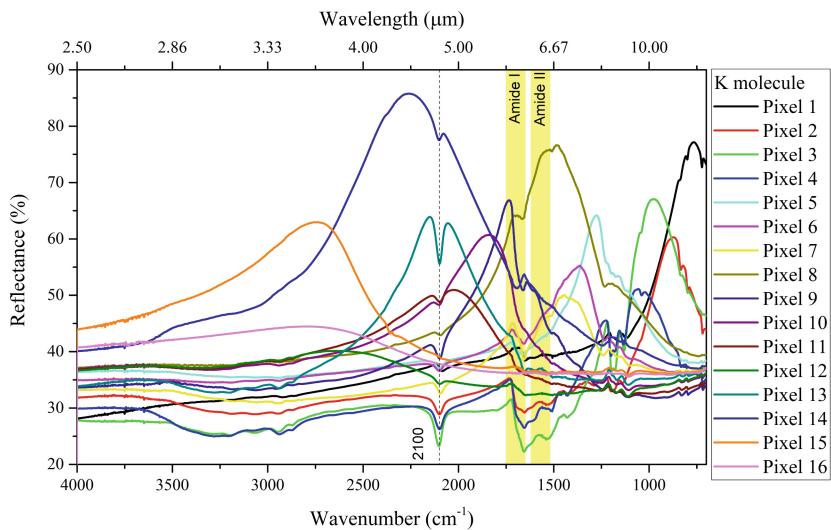


Fig. 3. Reflectance spectra of all the pixels present on the fabricated MS after the functionalization with the K molecule. A strong absorbance peak appears in correspondence of the N_3 vibrational feature.

As shown in Fig. 3, all the pixels exhibit an absorbance peak in correspondence of the N_3 vibrational feature. However, Pixel #13 shows the strongest absorbance peak. This behavior is due to the excellent match between the vibrational feature to be revealed (2100 cm^{-1}) and the plasmonic resonance of the pixel (2163 cm^{-1}), that allows to obtain a strong increase in the detection sensitivity [16]. In addition to this strong absorption peak, also a 65 cm^{-1} redshift compared to the naked surface appears, as shown in Fig. 4, thus confirming the presence of the K molecule on the substrate.

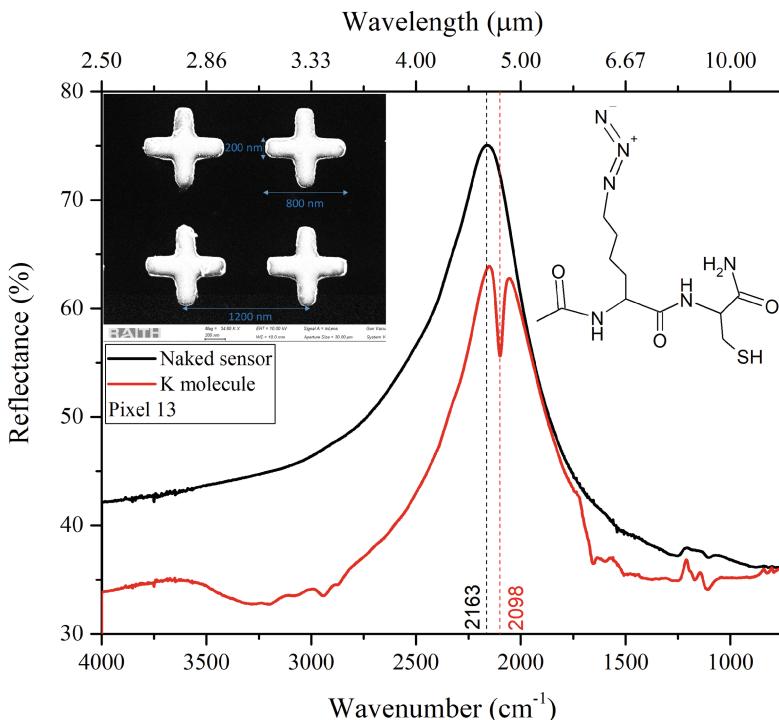


Fig. 4. Comparison of the reflectance curve of Pixel #13 before (black curve) and after (red curve) immobilization of the K molecule, whose structure is shown in the inset together with a SEM image of the NAs array. A redshift of 65 cm^{-1} appears after the pixel functionalization.

At the same time, the presence of pixels whose resonances have the capability to cover the whole range between $2800\text{--}900 \text{ cm}^{-1}$ allows to analyze with a single functionalization step all the different vibrational features of the analyte immobilized on the sensing platform, as shown for example in Fig. 5, where the reflectance curve of Pixel #8 is shown. For this pixel, the N_3 vibrational feature is still clearly visible, but the strongest absorbance peak occurs at 1655 cm^{-1} , mainly attributable to the $\text{C}=\text{O}$ stretching vibrations of Amide I band.

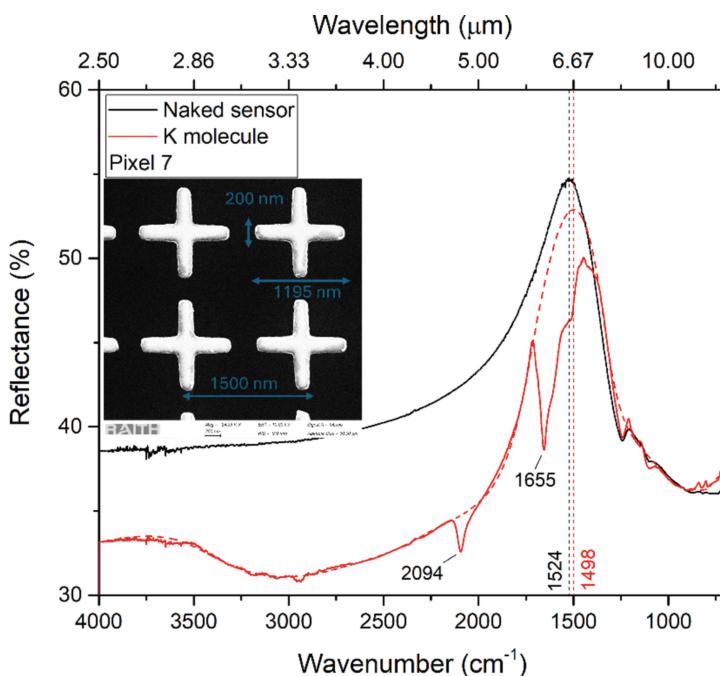


Fig. 5. Comparison of the reflectance curve of Pixel #8 before (black curve) and after (red curve) immobilization of the K molecule. For this pixel, the strongest absorption peak occurs in correspondence of the C=O stretching vibration, occurring at 1655 cm^{-1} . The inset shows the SEM image of the NAs array.

4 Conclusions

In this work, a pixeled plasmonic MS has been employed for the detection of an IR signature placed far from the fingerprint region. In particular, the vibration related to the vibration of the N_3 bonds (2100 cm^{-1}) has been chosen and a small molecule containing the chosen IR feature has been immobilized on the fabricated MS and detected. In particular, the K molecule ($\text{Ac-Lys}(\text{N}_3)\text{-Cys-NH}_2$) has been taken into account as a proof of principle analyte, observing both a relevant redshift (65 cm^{-1}) and the appearance of an absorption peak located at 2100 cm^{-1} . The experimental results hence confirm the suitability of the proposed sensing platform for the identification of precise vibrational features, hence paving the way for the engineering of bioprobes with chosen vibrational features to be uniquely detected with SEIRAS technique. Moreover, the presence of pixels covering a broad range of the IR spectrum allows to analyze the different vibrational features of the selected analyte with a single functionalization step, further confirming the high sensing capability of the proposed platform.

References

1. Stuart, B.H.: Infrared spectroscopy: Fundamental and Application. Wiley and Sons (2004)

2. Neubrech, F., et al.: Surface-enhanced infrared spectroscopy using resonant nanoantennas. *Chem. Rev.* **117**(7), 5110–5145 (2017)
3. De Tommasi, E., et al.: Frontiers of light manipulation in natural, metallic, and dielectric nanostructures. *La Rivista del Nuovo Cimento* **44**(1), 1–68 (2021). <https://doi.org/10.1007/s40766-021-00015-w>
4. Griffiths, P.R., de Haseth, J.A.: *Fourier Transform Infrared Spectrometry*. Wiley (2007). <https://doi.org/10.1002/047010631X>
5. Neubrech, F., et al.: Surface-enhanced infrared spectroscopy using resonant nanoantennas. *Chem. Rev.* **117**(7), 5110–5145 (2017)
6. Di Meo, V., et al.: Metasurface based on cross-shaped plasmonic nanoantennas as chemical sensor for surface-enhanced infrared absorption spectroscopy. *Sens. Actuators, B Chem.* **286**, 600–607 (2019)
7. Vannini, G., et al.: Plasmonic nanoantennas: fundamentals and their use in controlling the radiative properties of nanoemitters. *Chem. Rev.* **111**(6), 3888–3912 (2011)
8. Di Meo, V., et al.: Probing denaturation of protein a via surface-enhanced infrared absorption spectroscopy. *Biosensors* **12**(7), 530 (2022)
9. Di Meo, V., et al.: Pixelled metasurface for multiwavelength detection of vitamin D. *Nanophotonics* **9**(12), 3921–4390 (2020)
10. Di Meo, V., et al.: Advanced DNA detection via multispectral plasmonic metasurfaces. *Front. Bioeng. Bioelectronics* **9**, 666121 (2021)
11. Balan, V., et al.: Vibrational spectroscopy fingerprinting in medicine: from molecular to clinical practice. *Materials (Basel)* **12**(18), 2884 (2019)
12. Vieu, C., et al.: Electron beam lithography: resolution limits and applications. *Appl. Surf. Sci.* **164**, 111–117 (2000)
13. Malaria, P., et al.: Resonant enhancement of plasmonic nanostructured fiber optic sensors. *Sens. Actuators, B Chem.* **273**, 1587–1592 (2018)
14. Konermann, L., et al.: Hydrogen exchange mass spectrometry for studying protein structure and dynamics. *Chem. Soc. Rev.* **40**(3), 1224–1234 (2011)
15. Goormaghtigh, E., et al.: Determination of soluble and membrane protein structure by Fourier transform infrared spectroscopy. II. Experimental aspects, side chain structure, and H/D exchange. *Subcell. Biochem.* **23**, 363–403 (1994)
16. De Marcellis, A., et al.: Design optimisation of plasmonic metasurfaces for mid-infrared high-sensitivity chemical sensing. *Plasmonics* **9**(2), 293–298 (2016)



Optoelectronic Characterization of Nano-Diamond/crystalline Silicon Heterostructures

Arpana Singh¹(✉), Marinus Kunst^{2,3}, Diana Sannino¹, Vito Speranza¹,
Vincenzo Carrano¹, and Heinz-Christoph Neitzert¹

¹ Department of Industrial Engineering (DIIN), Salerno University, Fisciano, Italy
asingh@unisa.it

² Helmholtz-Zentrum Berlin (HZB), Berlin, Germany

³ Marseille, France

Abstract. Time resolved microwave conductivity (TRMC) measurements have been used for the analysis of the charge carrier dynamics in hetero-structures, formed by the deposition of nano-crystalline diamond (NCD) films on top of crystalline silicon substrates. It is found that the NCD film deposition results in all cases in an increase of the crystalline silicon surface recombination. Nevertheless, we could demonstrate the successful realization of diamond film/Silicon heterodiodes when depositing intrinsic or slightly boron-doped diamond films. In a coplanar contact geometry based device a strong sensitivity to UV light irradiation has been found. In this case a fast small positive light induced current signal is followed by a much slower negative signal giving rise to persistent negative photoconductivity.

Keywords: TRMC · nano-crystalline · Diamond · Silicon · Interface

1 Introduction

By deposition of NCD films on silicon substrates heterojunction diodes can be formed that can be used as test structure for the extraction of electrical properties of the NCD films. These heterojunctions have also good potential for high-temperature and high-power applications in photovoltaic devices. [1, 2] and can be used in a variety of sensing applications, as for example the realization of a particle radiation [3] detector. An important property of the heterostructure is the charge carrier kinetics at the interface. TRMC measurements have been used for the characterization of the amorphous silicon/crystalline silicon heterostructure and permitted to optimize the deposition conditions of the a-Si:H layer for minimal interface recombination [4] and for the evaluation of the influence a defective surface layer due to helium and hydrogen plasma exposure of a crystalline silicon substrate [5]. The contactless TRMC technique has already been reported to enable a characterization of NCD film charge carrier mobilities [6]. Here we will report on the first measurements, where the TRMC technique is used for the characterization of the modification of the crystalline silicon surface after deposition of nano-crystalline diamond films.

2 Experimental

Boron-doped diamonds were grown on commercially available p-type FZ-silicon substrates using a two-stage process involving seeding and microwave plasma-enhanced chemical vapor deposition (MWCVD). Seeding was accomplished by immersing the substrates in a water-based suspension of nano-diamond powder. The deposition of the diamond films was done in a multimode clamshell cavity (SDS6K, Seki Diamond Systems) within a 2.45 GHz MWCVD system.

Raman measurements have been done with a Micro Raman system (Invia, Renishaw) equipped with a 514 nm laser. The film surface morphology has been determined using Atomic Force Microscopy (AFM), with a NanoScope III (Digital Instruments (DI) System in tapping mode and film roughness and average grain size have been extracted.

3 Results and Discussion

Atomic force microscopy (AFM) measurements show that an increase in boron content yields a more polished film surface, while the mean grain size diminishes with increased boron concentration. From these measurements are extracted the values of the film roughness and grain size, and listed in Table 1 for the different investigated samples. Additional the values of the sample sheet resistances and the amplitudes of the TRMC-signals (see Fig. 3) are also listed in Table 1. It can be seen that, as expected, the sheet resistance decreased monotonically with increasing boron content in the nano-diamond films with a 200x increase of the conductance for the BDD3 film (5000 ppm B/C ratio) as compared to the sample with the intrinsic film (ID1).

Table 1. Characteristic parameters for the different NCD films: Film roughness and grain size from AFM measurements, NCD film sheet resistance and TRMC - amplitude.

Sample name	B/C (ppm)	Roughness (nm)	Grain size (nm)	Sheet resistance (Ω/\square)	TRMC-ampl (mV)
ID1	0	69.25	94.70	7820	257
BDD1	500	66.20	121.357	1390	240
BDD2	2000	44.67	97.45	110.2	154
BDD3	5000	42.92	78.07	39.52	19

The Raman spectra of diamond layers grown with varying B/C ratios, as depicted in Fig. 1, display the typical characteristics of boron-doped diamond layers exhibiting metallic conduction [7, 8] and, highlight the impact of TMB concentration on the structural composition of the material. In the case of the intrinsic sample (ID 1), a distinct diamond peak at approximately 1331 cm^{-1} is evident, reflecting the presence of sp^3 hybridized carbon atoms within the diamond lattice structure. As the concentration of TMB increases, there is a decrease in the diamond peak at 1331 cm^{-1} , accompanied by the rise in TPA (trans-polyethylene) at the grain boundaries and an enhancement of the

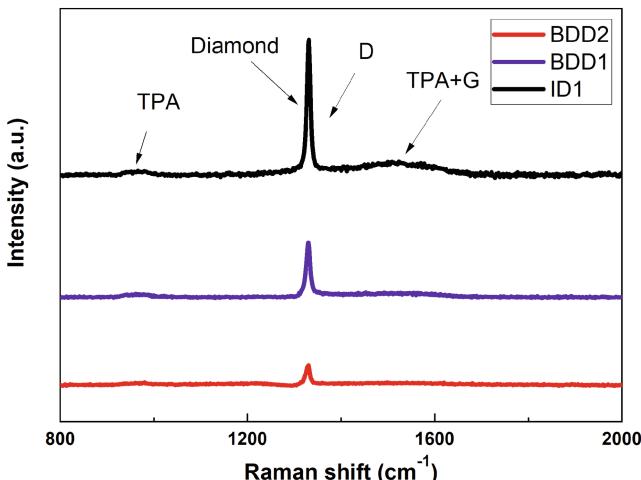


Fig. 1. Raman spectra (514 nm excitation) of intrinsic (ID1) and p-type doped nano-diamond films with different boron concentrations of 500 ppm (BDD1) and 2000 ppm (BDD2), deposited on p-type crystalline Si substrates.

D band in the Raman spectra. This spectral analysis indicates that higher TMB concentrations lead to changes in the structural composition of the material, with a decrease in the diamond peak, increased presence of TPA at grain boundaries, and an amplified D band.

TRMC measurements have been done using a Ka-Band setup with a Gunn diode microwave source, a circulator, and a fast receiver diode with the sample to be characterized terminating an open waveguide and illuminated from the topside with a pulsed 520 nm diode laser. In Fig. 2 we show the TRMC-transients, measured on the ID1 (intrinsic), BDD1 (500 ppm B/C) and BDD2 (2000 ppm B/C) based samples. The observed TRMC-signals are only reflecting the charge carrier changes at the crystalline silicon substrate surfaces, because the charge carrier mobility in the NCD films is orders of magnitude lower than in the c-Si substrate. The decreasing TRMC-amplitude with increasing boron content in the film (see also the data in Table 1) is due to the increase of sub-bandgap absorption in the nano-diamond film.

In all cases a faster charge carrier decay is observed for the samples with nano-diamond films indicating an increase of the surface recombination of the crystalline silicon substrate.

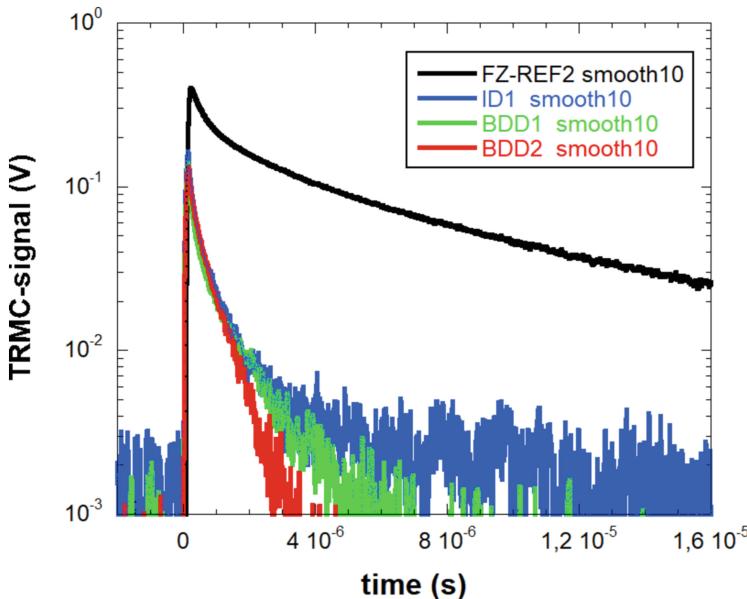


Fig. 2. TRMC-transients, measured after laser excitation at 520 nm from the diamond film side for 3 samples with p-type crystalline Si substrate and different deposited NCD films (ID1, BDD1 and BDD2).

It should be noted that the current-voltage (I-V) characteristics of samples with intrinsic or slightly doped NCD films, contacted in sandwich configuration between a top gold contact and the p-type c-Si back surface, showed a stable diode characteristic with moderate rectification ratio. Best rectification is observed for the ID1 sample with the intrinsic diamond top layer.

In another electrical configuration we tested the sensitivity of the realized heterostructures to 310 nm UV-light. In this case a coplanar geometry has been chosen, avoiding the use of transparent top electrodes. A complex photoelectric behavior has been observed (Fig. 3) with a fast initial small positive photocurrent signal (inset of Fig. 3) followed by a substantial decrease of the conductivity, which persists for a long time. The initial fast positive photo-signal is due to a primary photocurrent due to UV-light absorption in the crystalline silicon substrate. It disappeared when the same experiment had been performed on the same nano-diamond film, grown on an isolating substrate. The negative photoconductivity signal, on the other hand, is related to the diamond film itself. In literature, there are a variety of explanations for negative photoconductivity phenomena, observed in different semiconductor systems [9]. So far only Liao et al. [10] have observed transient negative photoconductivity in thin-film diamond films. In order to understand this effect in the nano-diamond/crystalline silicon heterojunction system, presented here, more experiments are needed, varying for example the optical excitation wavelength and the measurement temperature. Detailed investigations are under way.

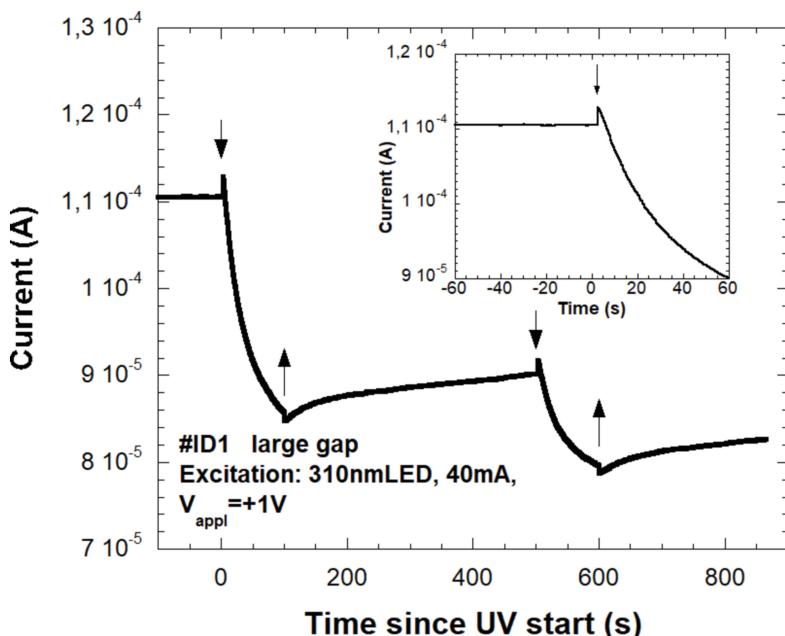


Fig. 3. Monitoring of the current with an applied voltage of 1 V to evaporated gold contacts deposited in coplanar configuration on top of the ID1 sample (intrinsic nano-diamond film grown on top of a p-type crystalline Silicon substrate). During the 2 periods indicated by the arrows the sample has been illuminated by 310 nm LED light.

Acknowledgments. The authors gratefully acknowledge the help of Dr. Dhanajay Kumar Sharma (FZU, Prague) for providing the BDD samples used in this study and useful discussions.

References

1. Sang, X., et al.: A review on optoelectronic properties of non-metal oxide/diamond-based p-n heterojunction. *Molecules* **28**, 1334 (2023)
2. Yao, Y., Sang, D., Duan, S., Wang, Q., Liu, C.: Review on the properties of boron-doped diamond and one-dimensional-metal-oxide based P-N heterojunction. *Molecules* **26**, 71 (2020)
3. Zatko, B., Varga, M., Vanko, G., Izsák, T., Šagátová, A., Kromka, A.: Polycrystalline CVD diamond-based structures for detection of charged particles. *AIP Conf. Proc.* **3054**(1), 050013 (2024)
4. Neitzert, H.C., Hirsch, W., Kunst, M.: Structural changes of a-Si:H films on crystalline silicon substrates during deposition. *Phys. Rev. B* **47**, 4080–4083 (1993)
5. Neitzert, H.C., Layadi, N., Roca I Cabarcas, P., Vanderhaghen, R., Kunst, M.: In-situ measurements of changes in the structure and in the excess charge carrier kinetics at the silicon surface during hydrogen and helium plasma exposure. *J. Appl. Phys.* **75**, 1438–1445 (1995)
6. Seshan, V., et al.: Contactless photoconductance study on undoped and doped nanocrystalline diamond films. *ACS Appl. Mater. Interfaces*. **6**(14), 11368–11375 (2014)

7. Bernard, M., Baron, C., Deneuville, A.: About the origin of the low wave number structures of the Raman spectra of heavily boron doped diamond films. *Diamond Relat. Mater.* **13**, 896–899 (2004)
8. May, P.W., Ludlow, W.J., Hannaway, M., Heard, P.J., Smith, R.K.N.: Raman and conductivity studies of boron-doped microcrystalline diamond, faceted nanocrystalline diamond and cauliflower diamond films. *Diamond Relat. Mater.* **17**(2008), 105–117 (2008)
9. Tailor, N.K., Aranda, C.A., Saliba, M., Sathapati, S.: Negative photoconductivity: bizarre physics in semiconductors. *ACS Mater. Lett.* **4**, 2298–2320 (2022)
10. Liao, M., Koide, Y., Alvarez, J., Imura, M., Kleider, J.P.: Persistent positive and transient absolute negative photoconductivity observed in diamond photodetectors. *Phys. Rev. B* **78**(4), 045112 (2008)



Real-Time Reconfiguration of Free-Space Optical Receivers by Means of Fully Integrated CMOS Controller

Emanuele Sacchi¹ , Francesco Zanetto¹ , Francesco Morichetti¹ , Andrea Melloni¹ , Marco Sampietro¹ , and Giorgio Ferrari²

¹ Department of Electronics, Information and Bioengineering, Politecnico di Milano,
piazza Leonardo da Vinci 32, 20133 Milan, Italy
emanuele.sacchi@polimi.it

² Department of Physics, Politecnico di Milano, piazza Leonardo da Vinci 32,
20133 Milan, Italy

Abstract. Our work presents a fully integrated CMOS architecture that performs real-time reconfiguration of free-space optical receivers built in a CMOS-compatible Silicon Photonics platform. The chip comprises 8 identical and independent channels, dissipating $\approx 10\text{ mW}$ each, and is used to dynamically drive the thermal actuators setting the working point of the photonic integrated circuit. By connecting a pair of ASICs to the photonic chip, we successfully controlled a binary-tree mesh consisting of 15 Mach-Zehnder Interferometers. When put to the test in a laboratory setup simulating real-world operation, our solution proved successful in compensating for atmospheric turbulence up to $\approx 300\text{ Hz}$. This architecture thus stands as a scalable solution for establishing reliable free-space optical links between photonic processors of growing complexity.

Keywords: CMOS · Integrated Circuits · Silicon Photonics · Free-Space Optics

1 Introduction

Programmable photonic integrated circuits (PICs) in CMOS-compatible Silicon Photonics (SiP) platforms offer an alternative way to implement architectures performing arbitrary linear operations, with multiple applications in high-speed communication, quantum information, optical computing, imaging and sensing [1], as they promise to address the need for wide bandwidth and minimal power dissipation needed, for example, by wireless communication in Internet of Things networks. A typical architecture for PICs consists of a mesh of Mach-Zehnder Interferometers (MZIs), employing two phase shifters each to steer the optical power between two output ports. The complexity of programmable PICs is currently limited by the need to finely tune each MZI to compensate for process

and temperature variations and, in Free-Space Optical (FSO) communication, to mitigate the effect of atmospheric turbulence. We thus developed a CMOS integrated circuit that autonomously manages up to 15 MZIs in real-time, providing a scalable solution for closed-loop control of large optical processors. In our application, we considered a binary-tree mesh, whose schematic is reported in Fig. 1a, used to route a FSO beam sampled by an optical phase array (OPA)

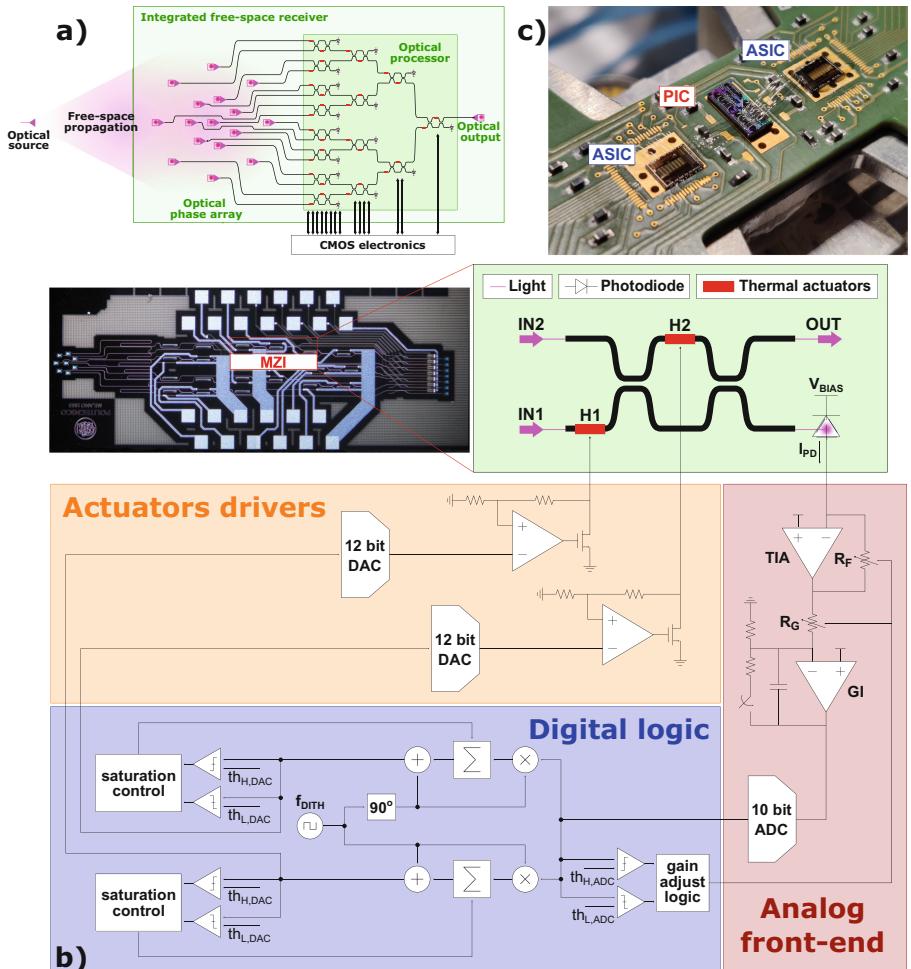


Fig. 1. a) Schematic representation of the FSO receiver, comprising an optical laser source at $\lambda = 1550\text{ nm}$, the OPA to sample the incoming beam and a binary-tree mesh of 15 interferometers, equipped with sensors and actuators; b) dark field micrograph of the PIC and schematic architecture of a single channel of the ASIC controlling one MZI; c) direct wire-bonding between two ASICS and the PIC, all mounted on a custom-designed PCB holder.

towards a single output: the mesh is constantly tuned by our closed-loop control system in order to reconstruct the signal in the optical domain by compensating for atmospheric turbulence along the beam path [2].

2 ASIC Architecture

Each interferometer has one output port connected to an on-chip germanium photodiode (PD), as highlighted in Fig. 1b. Each channel of the ASIC reads the PD current and drives the integrated thermal phase shifters (nominal resistance $R_H \approx 400 \Omega$) of the corresponding MZI. The control algorithm relies on the dithering technique [3] to implement a calibration-free feedback strategy: a pair of DACs (0–6 V) sets the working point of the actuators, at the same time superimposing two orthogonal modulations (called *dithering* signals), with tunable amplitude in the 5–100 mV range and frequency $f_{dith} \approx 8.3$ kHz. Thanks to the resolution of the DAC, it is possible to apply a sufficiently small dithering modulation, which is negligible in terms of output optical power ripple. After amplification with a variable gain Transimpedance Amplifier (TIA), anti-aliasing filtering through a Gated Integrator (GI) stage and digitization by means of a 10-bit successive approximation analog-to-digital (ADC) converter, each channel extracts the two modulated components, which are proportional to the partial derivatives of the MZI $\frac{P_{OUT}}{V_H}$ transfer function. The extracted signals are accumulated to implement a discrete-time integral controller that updates the thermal phase shifters until the detected dithering signals are zeroed. The loop thus minimizes (or maximizes, by simply changing the loop sign) the optical power on the PD: doing it for every channel will consequently maximize the power at the output of the receiver. The analog front-end features a variable transimpedance, adjusted automatically to ensure that the ADC always works over its full-scale range, regardless of the total input optical power, which may span between 0 and –50 dBm. A 2-wire serial interface allows to define several parameters, including the bandwidth of the loop and the dithering amplitude. The loop can also be

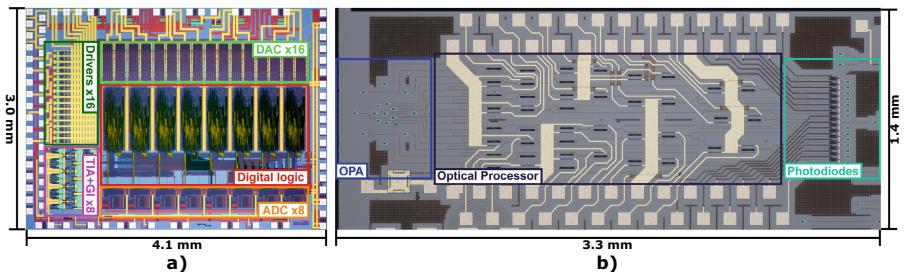


Fig. 2. a) False-color image of the electronic chip; pads on the left were wire-bonded to the sensors and actuators on the PIC, the others were connected to the custom-designed PCB holder for ASIC configuration and communication to the external world; b) micrograph of the FSO receiver used during experimental validation.

turned off to fix the working point of the actuators or to manually set a new configuration, the latter feature being used for characterization purposes. PD current and output voltage of the DACs are also monitored by another interface.

The chip, whose false-color micrograph is shown in Fig. 2a, was fabricated with a 350 nm feature size; each 8-channel ASIC occupies 12 mm² (3.1 × 4.0 mm²), while dissipating only ≈10 mW/channel, less than the heaters required by each MZI. A pair of ICs was mounted on a custom PCB and wire-bonded to the PIC for testing (Fig. 1c).

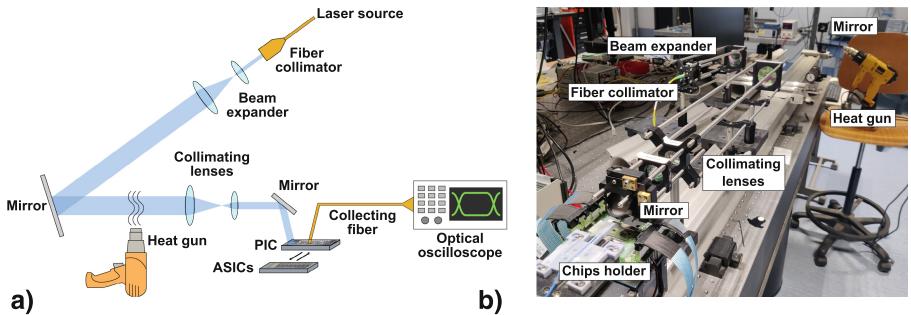


Fig. 3. a) Schematic of the experimental laboratory setup, including a thermal gun used to inject atmospheric-like turbulence; b) Picture of the setup, which was mounted on an optical bench to avoid fiber misalignment due to mechanical vibrations.

3 Experimental Results

A laboratory setup, portrayed in Fig. 3 was built in order to recreate the propagation of the beam into free-space over an optical link of few hundreds meters [2]: laser light is emitted by a 1550 nm fiber source; a couple of lenses then expand the beam up to a diameter of ≈5 cm, before folding the path with a mirror; another pair of lenses, arranged in a telescopic structure, and an additional mirror eventually focus the beam on the OPA. The robustness of the control loop was assessed by artificially introducing free-space turbulence along the beam path with a thermal gun, placed right after the first mirror.

Figure 4 reports results from three different conditions. A reference (yellow) was set by activating the control loop with the gun left off: in this case, the average output power is -20.1 dBm, with $\sigma = 0.055$ dB, as shown in the histogram plot of Fig. 4b. The controller was then paused, fixing the FSO receiver in the state reached with no turbulence, and the gun turned on: the average received power dropped to -21 dBm, with a particularly detrimental effect on standard deviation, increased to $\sigma = 0.34$ dB (blue), since the controller was no longer tracking the ever-changing optimal configuration that would maximize the output power of the receiver. Finally, the ASICs were reactivated: measurements show that the received power now averages -20.4 dBm, with σ shrunk down

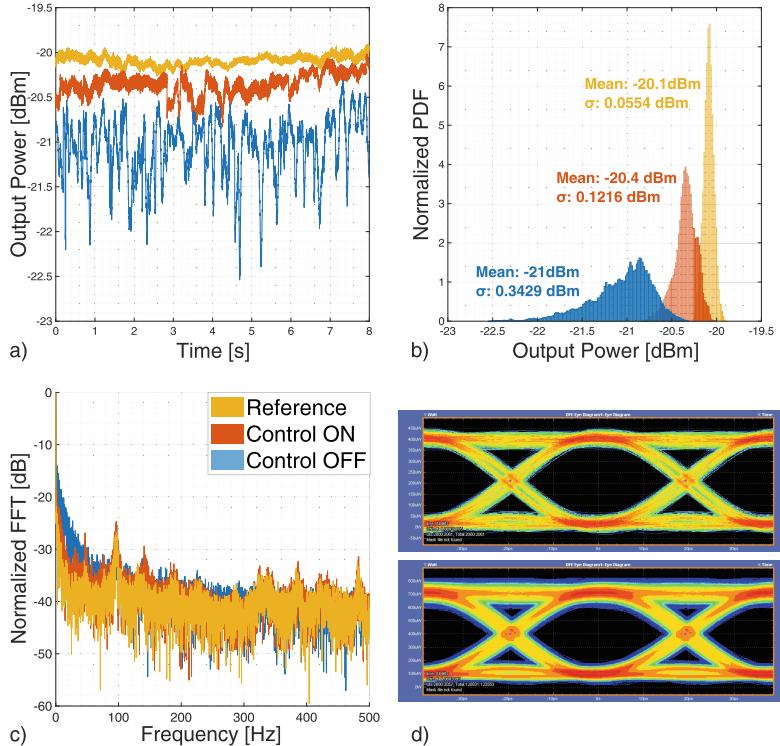


Fig. 4. a) Time traces of the optical power detected by an external photodiode, fiber-coupled to the output of the last interferometer of the binary-tree mesh; b) histogram plot of the output power before and after the activation of the turbulence, with the ASIC on and off; c) power spectra of the data plotted in (a); d) eye diagram at the transmitter side of the FSO link and at the output of the PIC, demonstrating the correct operation of the electro-optical receiver. (Color figure online)

to 0.12 dB (red). Figure 4c characterizes the spectra of the injected turbulence and the effectiveness of the compensation: a good rejection (≈ 10 dB) of disturbances is provided up to ≈ 300 Hz, demonstrating that the system is suitable for real outdoor FSO links. After this frequency, the spectra are almost perfectly superimposed, meaning that no turbulence is present beyond such bandwidth, as expected [4]. Figure 4d finally shows the eye diagram obtained when transmitting a 25 Gbps OOK modulated signal through the FSO link enabled by the PIC. The eye diagram at the output of the receiver does not show significant degradation when compared to the one taken at transmitter side right after the light modulator, certifying the correct operation of the PIC as well as the proper dynamic tuning of the mesh performed by the CMOS electronics.

4 Conclusions

The fully integrated CMOS controller presented in this work provides a viable solution to implement scalable dedicated control electronics needed by PICs of growing complexity. In particular, experimental results show that our solution matches, when applied to a FSO receiver, the performance of other discrete components architectures [2], while consuming only a fraction of their power and area. Future ASICs will be designed targeting even more compact solutions, ideally matching the area occupied by one CMOS electronic channel to the area of the controlled SiP device. This would allow the fabrication of very compact, flip-chip connected photonic-electronic co-designs, thus introducing a chiplet-based approach also in the industry of PICs.

Acknowledgements. The authors would like to acknowledge the support provided by PoliFab, the micro and nano fabrication facility of Politecnico di Milano, for wire-bonding the integrated circuits used during the experiments, as well as the work of Dr. SeyedMohammad SeyedinNavadeh and Dr. Andres Ivan Martinez Rojas from the Photonic Devices Group of Politecnico di Milano, who built the experimental setup.

References

1. Bogaerts, W., et al.: Programmable photonic circuits. *Nature* **586**, 207–216 (2020)
2. Morichetti, F., et al.: Mitigation of atmospheric turbulence in an optical free space link with an integrated photonic processor. In: Optical Fiber Communications Conference, pp. 1–3 (2023)
3. Zanetto, F., et al.: Dithering-based real-time control of cascaded silicon photonic devices by means of non-invasive detectors. *IET Optoelectron.* **15**(2), 111–120 (2021)
4. Cox, M., Mphuthi, N., Nape, I., Mashaba, N., Cheng, L., Forbes, A.: Structured light in turbulence. *IEEE J. Sel. Top. Quant. Electron.* **27**(2), 1–21 (2021)



A Plethysmographic Sensor Based on FBG Embedded in a Soft Silicone Patch

Mariaconsiglia Cuomo¹(✉), Elena De Vita¹, Vincenzo Romano Marrazzo², Giovanni Breglio², Agostino Iadicicco¹, and Stefania Campopiano¹

¹ Department of Engineering, University of Naples “Parthenope”, Naples, Italy
mariaconsiglia.cuomo001@studenti.uniparthenope.it

² Department of Electrical Engineering and Information Technology (DIETI), University of Naples Federico II, Naples, Italy

Abstract. Cardiovascular diseases are the main cause of disability and global death, and their rapid spread is a sign of strong concern for the scientific community. In this scenario, devices, able to continuously and non-invasively monitor heart parameters could be very useful for timely diagnosis, essential for the prevention of premature deaths. Recently, among the most popular wearable devices, sensors based on Fiber Bragg Grating (FBG) play an important role. FBG, in fact, allows to monitor different physiological parameters such as heart rate, body temperature, blood pressure and respiratory rate. The continuous monitoring of these parameters is of extreme importance from the clinical point of view, as it allows detecting physiological warning signals in a timely manner, which in some cases could be fatal. This is due to the many advantages provided by FBG, in fact, in addition to being minimally invasive, they are immune to electromagnetic interference, biocompatible, highly sensitive and allow for the multiplexing.

In this work, we propose, therefore, a new sensor based on FBG for plethysmography of peripheral arteries. The proposed sensor is embedded in a soft silicone matrix capable of increasing wearability and sensitivity, also allowing to protect the sensor from external stress. The preliminary results show that the obtained sensor can record continuously and non-invasively the plethysmographic signal with a clear distinction of the systolic and diastolic peaks, in whose waveform important cardiovascular information is contained.

Keywords: FBG · plethysmography · silicone embedding · wearable sensor

1 Introduction

The speed with which cardiovascular diseases affects humanity is a worrying and high-risk factor, which leads researchers to find increasingly efficient methods in the detection of timely diagnosis. In this context, wearable devices are becoming increasingly attractive to the scientific community, being economical, minimally invasive, and able to provide a good trade-off between adaptability and reliability of results. Of particular interest is the plethysmography of peripheral arteries, since it can be useful in cardiovascular risk monitoring. Plethysmography is a diagnostic technique that allows detecting

the volumetric changes of an organ or part of the body caused by changes in blood flow [1]. In this work, we propose the plethysmography of the peripheral artery that uses a Fiber Bragg Grating (FBG) embedded in soft silicone patches. The plethysmography technique using FBG has already been tested by Shweta Pant et al. [2] who proposed finger plethysmography, using a conical plastic tube with a slit covered with silicone on which an FBG is bonded. In this work, instead, we propose a new plethysmographic technique based on the FBG embedded into a soft silicone patch instead of the FBG bonding over it. The main advantages of embedding the sensor into the silicone is to improve its pressure sensitivity as demonstrated in [3], to simplify the device, and to protect it from external agents. FBG embedment, in fact, is important to preserve the fragile regions of optical fiber from external stresses and to make the FBG sensitive to other parameters, such as 3D shape, force and pressure [3, 5].

2 Materials and Methods

In this section the FBG working principle, numerical simulations and sensor fabrication with experimental setup are reported.

2.1 FBG Operating Principle

An FBG is generally obtained by a periodic perturbation in the effective refractive index of the optical fiber core. The FBG operating principle is based on the light coupling between two modes: the fundamental core mode and the backward propagating mode [4].

In Fig. 1, a schematically representation of FBG working principle is shown.

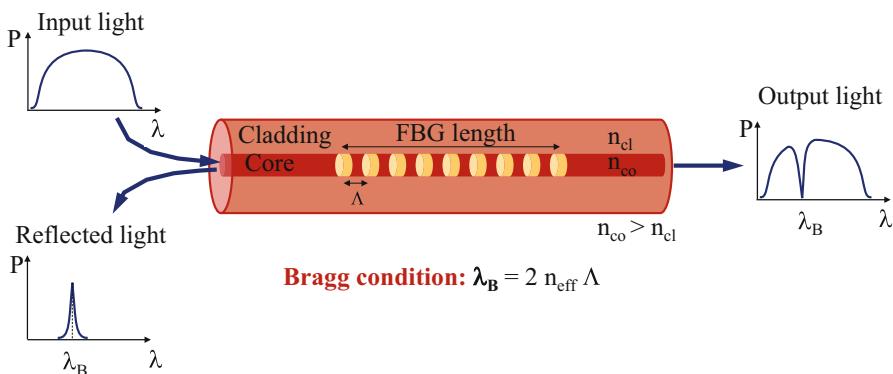


Fig. 1. FBG working principle.

FBGs act as wavelength selective mirrors, in fact feeding the fiber with a broadband light, only the portion of the spectrum centered around a particular wavelength, called Bragg wavelength, is reflected, while the others wavelength will be transmitted. The Bragg wavelength is expressed by the following equation:

$$\lambda_B = 2 \cdot n_{\text{eff}} \cdot \Lambda \quad (1)$$

where n_{eff} is the effective refractive index core, while Λ is the period of the perturbation. The Bragg wavelength depends on n_{eff} and on Λ , so variations of these parameters induce a displacement of Bragg wavelength, and since n_{eff} and Λ depend on temperature and strain, a variation of these parameters induces a shift in the Bragg wavelength, denoted by $\Delta\lambda_B$ and expressed in the following equation:

$$\Delta\lambda_B = \frac{\partial\lambda_B}{\partial T} \Delta T + \frac{\partial\lambda_B}{\partial \varepsilon} \Delta \varepsilon = S_T \Delta T + S_\varepsilon \Delta \varepsilon \quad (2)$$

where S_T and S_ε are thermal sensitivity and strain sensitivity respectively. Consequently, FBGs are sensitive to temperature and strain [3].

2.2 Numerical Simulations

Aiming to increase the pressure sensitivity of the proposed plethysmographic sensor, we use Comsol Multiphysics software, in which we compared two types of silicone, i.e., a commercial silicone, named Ecoflex™ 00–50 by Smooth-On, and a type of silicone included in Comsol Multiphysics material library.

To investigate the effects of silicone patch thickness, three simulations are carried out for each type of silicone. In particular, the silicone patch is simulated as a parallelepiped, on whose upper surface a fixed constraint is applied, with fixed width and length of 20 mm and 40 mm, respectively, but with three different thicknesses of 1.5 mm, 2.5 mm and 3.5 mm. Instead, the FBG sensor is simulated as a cylinder with the same diameter of optical fiber, i.e. 125 μm , on which no constraint is applied. Moreover, to simulate the classical pressure of 70 mmHg that blood flow exerts on vessel walls, a load of 9332.6 N/m² is applied on the lower surface along z-axis.

In Fig. 2 the description of numerical configuration is shown:

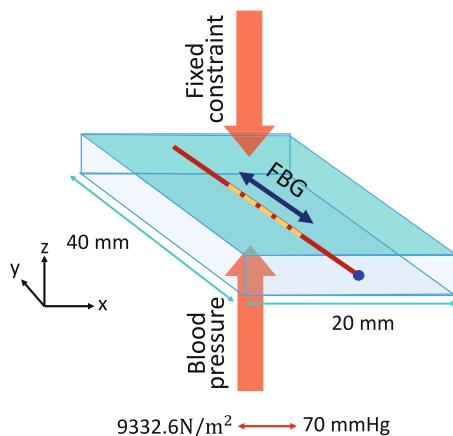


Fig. 2. Description of numerical configuration used in Comsol Multiphysics software.

The simulation results show the displacement field along optical fiber axis, i.e., y-axis, when a pressure and fixed constraint are applied on lower and upper surface

respectively. In particular, in the first and second rows of the Fig. 3, the displacement field is shown when EcoflexTM 00–50 and Comsol library silicone are used, respectively.

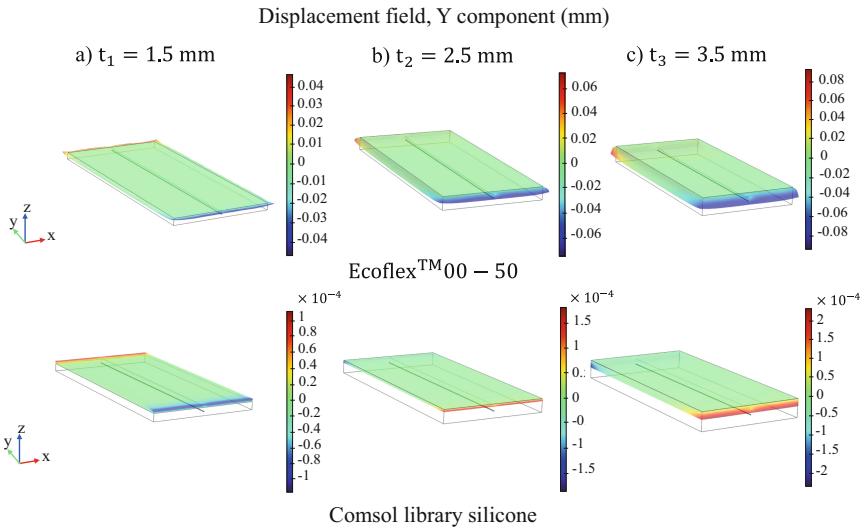


Fig. 3. Simulation results of displacement field along optical fiber axis when a pressure and fixed constraint are imposed on lower and upper surface, respectively, for EcoflexTM 00–50 (first row) and Comsol library silicone (second row) with different patch thickness: a) $t_1 = 1.5$ mm; b) $t_2 = 2.5$ mm; c) $t_3 = 3.5$ mm.

Simulations results show that pressure sensitivity of the proposed sensor increases when thickness increases and when EcoflexTM 00–50 is used with respect to the Comsol library silicone. In fact, when thickness increases, the surface displacement field along optical fiber axis (i.e., y-axis) increases so that the FBG strain increases.

To evaluate the pressure sensitivity of the sensor the displacement in correspondence of the blue point along y-axis, shown in Fig. 2, and its symmetric in the opposite surface of the patch, is observed when a pressure of 9332.6 N/m^2 and a fixed constraint are imposed on lower surface and upper surface respectively.

The expression of strain sensitivity is reported in Eq. (3) and the resulting sensor sensitivity for the two types of silicone at different thicknesses is expressed in the Table 1.

$$\mu \varepsilon_y = \frac{\Delta l}{l} \quad (3)$$

where Δl and l are the length variation and the starting length of the optical fiber, respectively.

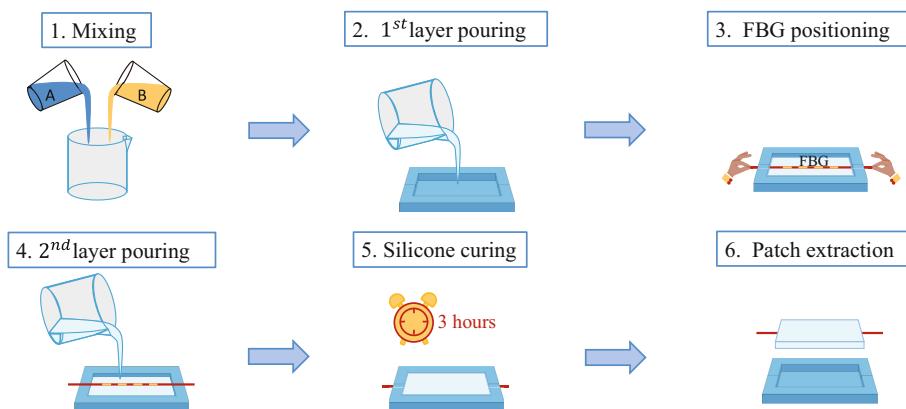
Therefore, the simulations results justify the choice of EcoflexTM 00–50 to embed FBG sensor.

Table 1. Sensor sensitivity

	$t_1 = 1.5 \text{ mm}$	$t_1 = 2.5 \text{ mm}$	$t_1 = 3.5 \text{ mm}$
EcoflexTM 00–50	10	20	32.5
Comsol silicone	0.275	0.6	1.0625

2.3 Sensor Fabrication and Experimental Setup

The plethysmographic sensor is made by embedding a 5 mm long FBG in a silicone patch. In particular, a mix of the two components of Ecoflex™ 00–50 is prepared in equal weight and half of the mixture is poured in a rectangular holder, printed in PLA with the 3D printer Renkforce RF500. Immediately afterwards, the FBG is placed in the center of the holder and a second layer of the silicone mixture is poured. Given the time of silicone curing, about 3 h, the device is extracted from the holder. In Fig. 4 the manufacturing process of silicone patch is shown.

**Fig. 4.** Manufacturing process of silicone patch.

The plethysmographic test, performed on several volunteers, consists in placing the sensor on the ulnar artery on the back of the hand for each volunteer by fixing it with an elastic band, so that the pressure exerted by the band can improve the signal recorded by the sensor. This signal is collected by the dynamic interrogator Micron Optics SM130 with the sampling frequency of 2 kHz and displayed on the computer (see Fig. 5).

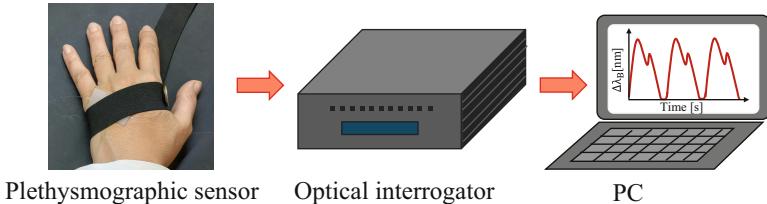


Fig. 5. Experimental setup.

3 Results

In this section, the preliminary results are reported. The signals recorded by the plethysmographic sensor have been filtered, with a 6th-order low-pass Butterworth numerical filter, with a cut frequency of 3 Hz, to remove the movement artifacts. For simplicity, we report, in Fig. 6a, only the plethysmographic signal obtained by the first volunteer. In Fig. 6b, instead, the second derivative of the filtered signal, i.e. the accelerated plethysmography, is shown: it is characterized by five peaks, named a, b, c, d, e, each of which is related to a specific cardiovascular parameter [2]. These peaks can give important information related to the age and to pathologies like cerebrovascular disease and ischemic heart disease, i.e. the ratio b/a increases with age and the ratio c/a, d/a, e/a decreases with age [6].

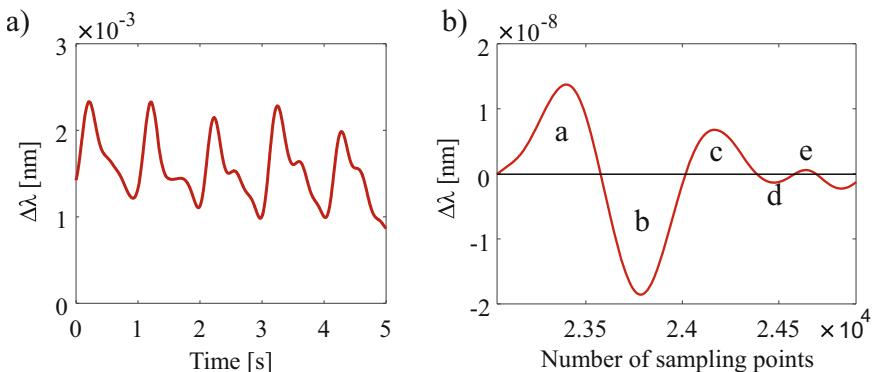


Fig. 6. Preliminary results for the first volunteer. a) Plethysmographic signal. b) Accelerated plethysmography.

4 Conclusion

In this work a new plethysmographic sensor based on FBG embedded in a soft silicone patch is proposed. In particular, the silicone has been chosen for its ability to increase the sensitivity of the FBG to the specific application and it also allows the sensor to better adapt to the place of the measurement without causing any discomfort. Moreover, the

simulation results conducted in Comsol Multiphysics software, demonstrate that patch thickness affects the sensitivity of our sensor since it increases when patch thickness increases.

The preliminary results show that the proposed sensor is able to provide the periodicity of the heartbeat, with a clear distinction between the peaks of cardiac systole and diastole, giving important information from the cardiovascular point of view. To obtain further information related to cardiovascular rigidity, the second derivative of the filtered signal has been calculated showing the accelerated plethysmography.

Acknowledgments. This work was partially supported by the European Union under the Italian National Recovery and Resilience Plan (NRRP) of NextGenerationEU, partnership on “Telecommunications of the Future” (PE00000001 – program “RESTART”).

References

1. Dennis, M.J.: Plethysmography: the new wave in haemodynamic monitoring - a review of clinical applications. *Aust. Crit. Care* **13**(1), 14–20 (2000). [https://doi.org/10.1016/S1036-7314\(00\)70611-4](https://doi.org/10.1016/S1036-7314(00)70611-4)
2. Pant, S., Aumesh, S., Asakan, S.: A novel approach to acquire the arterial pulse by finger plethysmography using fiber bragg grating sensor. *IEEE Sensors J.* **20**(11), 5921–5928 (2020). <https://doi.org/10.1109/JSEN.2020.2973342>
3. Di Palma, P., De Vita, E., Iadicicco, A., Campopiano, S.: Force sensor based on FBG embedded in silicone rubber. *IEEE Sensors J.* **23**(2), 1172–1178 (2023). <https://doi.org/10.1109/JSEN.2022.3226039>
4. Esposito, F., Campopiano, S., Iadicicco, A.: Miniaturized strain-free fiber bragg grating temperature sensors. *IEEE Sensors J.* **22**(17), 16898–16903 (2022). <https://doi.org/10.1109/JSEN.2022.3192355>
5. Di Palma, P., De Vita, E., Iadicicco, A., Campopiano, S.: 3D shape sensing with FBG-based patch from the idea to the device. *IEEE Sens. J.* **22**(2), 1338–1345 (2022). <https://doi.org/10.1109/JSEN.2021.3133704>
6. Takazawa, K., et al.: Assessment of vasoactive agents and vascular aging by the second derivative of photoplethysmogram waveform. *Hypertension* **32**(2), 365–370 (1998). <https://doi.org/10.1161/01.HYP.32.2.365>



Fiber Optic Probes Exploiting Localized Surface Plasmon Resonance for Chemical Detection

Amin Moslemi¹, Lucia Sansone², Flavio Esposito¹, Stefania Campopiano¹, Michele Giordano², and Agostino Iadicicco^{1(✉)}

¹ Department of Engineering, University of Naples “Parthenope”, 80143 Napoli, Italy
agostino.iadicicco@uniparthenope.it

² Institute for Polymers, Composites, and Biomaterials, IPCB-CNR, 80055 Portici, Italy
lucia.sansone@ipcb.cnr.it

Abstract. A facile fiber optic transducer relying on the localized surface plasmon resonance (LSPR) phenomena is reported. It involves a single-ended probe made of an uncladded multimode fiber optics deposited with gold nanoparticles (AuNPs). The reflected spectrum of the device is regulated by the absorption spectral features of the AuNPs, showcasing attenuation bands in visible range. The position of these attenuation bands can be correlated with the external medium refractive index and eventually the presence of bio-chemical compounds attached to the AuNPs. To evaluate the performance of the device, it was tested towards the detection of pesticide Thiram at low concentrations.

Keywords: Fiber optic sensors · Localized Surface Plasmon Resonance · Gold nanoparticles · Chemical sensing · Biosensing

1 Introduction

Optical sensors, especially optical fiber sensors, have become increasingly popular in bio-chemical sensing domain due to several key benefits. These include their compact size and light weight, high sensitivity and resolution, chemical resistance, and biocompatibility. A variety of transducer mechanisms and phenomena are currently utilized to develop refractive index (RI) sensors, including in-fiber gratings, interferometers, lossy mode resonance, and surface plasmon resonance (SPR) [1–3].

Regarding SPR techniques, there is an interaction between input light photons and surface electrons on a metal, causing collective oscillation. When small metallic nanoparticles (typically on the order of tens of nanometers) are considered, they act as resonators and localized SPR occurs (LSPR). LSPR is employed in various fields, including biomedical imaging, photothermal therapy, and bio-chemical sensing [4, 5].

In this work, we illustrate regarding the fabrication and testing of a novel simple fiber optic probe leveraging on LSPR. The structure consists of a cladding removed multimode fiber (MMF) coated with gold nanoparticles (AuNPs). The performance of the device is thus evaluated for the detection of a harmful chemical compound, i.e. pesticide Thiram.

2 Fabrication and Testing

2.1 Transducer Fabrication

The optical probe discussed here primarily includes an etched multi-mode silica glass optical fiber operating in reflection (mirror-ended) configuration, as depicted in Fig. 1(A). The process involves the complete removal of MMF cladding along a short portion of the same by means of HF. This allows the light within the fiber to interact with the medium outside the fiber through evanescent wave, which is highly sensitive to the electrical prospect of its surroundings. A silver thin layer integrated at the fiber tip enables the reflective configuration. Gold nanoparticles (NP) in size of 43 nm are coated on the so-prepared fiber surface. The absorption spectrum of the nanoparticles is dependent on the refractive index of the surrounding medium, the NP size and configuration. Any variation in electrical properties in their vicinity will modify the wavelength and amplitude of the reflected spectrum.

FG105LCA fiber model by Thorlabs, having a core of 105 μm and cladding of 125 μm , was selected for this work. The fiber's acrylate coating was removed by stripper, and a 5 cm section sink in a 24% HF solution for 25 min, then thoroughly washed with deionized water. The etched fiber diameter is about 95 μm , once the cladding has been completely removed and the core is slightly narrowed, this allows light to leak as an evanescent wave from the fiber.

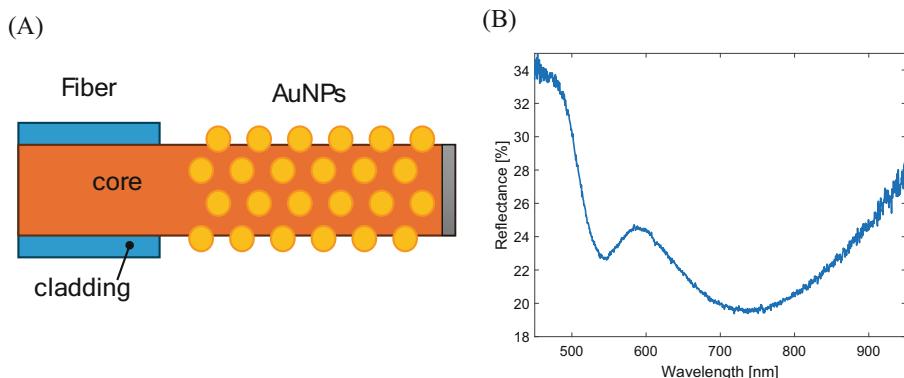


Fig. 1. (A) Representation of the fiber optic sensor; (B) Reflection spectrum of the sensor in an air environment.

The next step involved attaching AuNPs to the etched fiber surface. The etched fiber was functionalized using first piranha solution (mixture of mixture of H_2SO_4 and H_2O_2) and then (3-Aminopropyl) triethoxysilane (APTES). The fiber was sunk in piranha solution for 50 min to form hydroxyl groups, rinsed with water, cut sharply and smoothly, and silver thin layer was coated as mirror via Tollen's reaction to create a reflexive probe. The fiber was then immersed in APTES (5% w/w) for 120 min for surface salinization, rinsed with acetone, and air-dried for 24 h. Finally, the fiber was immersed in a gold nanoparticle solution in size of 43 nm with 1 mM concentration for 4 h then, air-dried

overnight. AuNPs self-organize on various morphology of APTES molecules on the fiber substrate [6, 7].

Spectral analysis during fabrication and performance was conducted using a simple, cost-effective setup. The light from a broadband white light source is sent to the transducer and reflected light is collected by HR2000 + spectrometer by Ocean Optics through a multimode optical fiber coupler.

In Fig. 1(A), a schematic of the so-prepared device is depicted, and in Fig. 1(B), the reflection spectrum of the sensor in an air environment is displayed. The spectrum displays two dips at 546 nm and 731 nm, respectively. The first dip refers to the attenuation band of a single nanoparticle layer attached smoothly on the fiber surface. Due to their superposition, groups of NPs at diverse angles to the evanescent waves result in a smooth second dip that is linked to multi-layer configurations [8].

2.2 Refractometric Characterization

Sensor sensitivity was evaluated against variation in the surrounding medium's refractive index (SRI). Deionized water and glycerin were mixed in different ratios to prepare solutions, and the refractive index of each solution was measured with an Abbe refractometer (resolution of $2 \cdot 10^{-4}$).

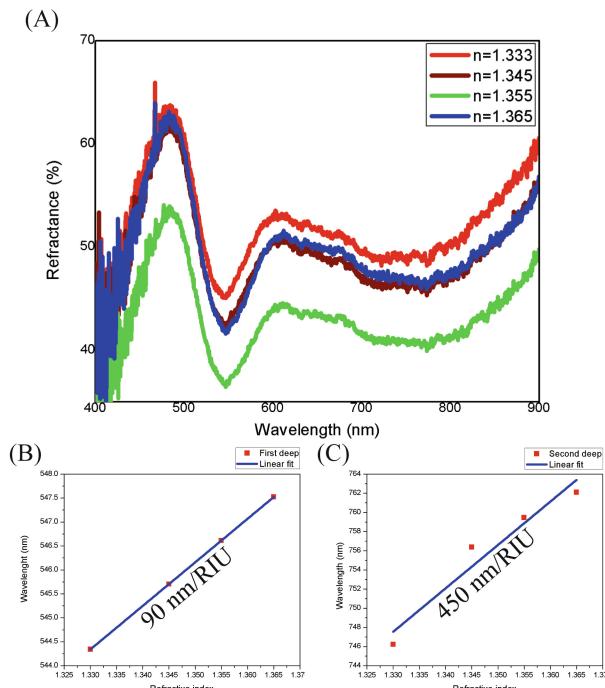


Fig. 2. (A) Reflection spectrum of the transducer in different surrounding refractive index environments. (B) The position of the wavelength of the (B) first dip and (C) second dip in different surrounding refractive indices, along with linear fitting of the experimental data and slope.

The SRI test involved immersing the fiber transducer in solutions with varying refractive indices, starting from lower to higher values. Additionally, after each solution, the transducer was washed with deionized water.

Both spectral peaks shifted to longer wavelengths with increasing refractive index, as shown in Fig. 2(A), (B), and (C), with high sensitivities of 90 nm/RIU and 450 nm/RIU for the first and second resonant wavelengths, respectively, in the 1.33–1.36 range [9, 10].

2.3 Thiram Sensing

Thiram pesticide has functional groups that bind strongly to Au nanoparticles, affecting surface plasmon resonance. The fiber transducer was used to measure Thiram concentration variations in water solutions (0.1–100 μM). The refractive index changes of these solutions were negligible (less than $2 \cdot 10^{-4}$), so the focus was on the first attenuation band for accurate Thiram concentration assessment [11].

Figure 3(A) displays the reflection spectra at various Thiram concentrations, showing clear spectral feature visibility throughout the experiment. Figure 3(B) shows the real-time response in attenuation band resonance wavelength occurred as the probe was exposed to increasing concentrations of the analyte, Thiram. Initially immersed in pure water, the sensorgram recorded data every 30 s, revealing a shift to higher wavelengths of the resonance peak with rising Thiram concentration.

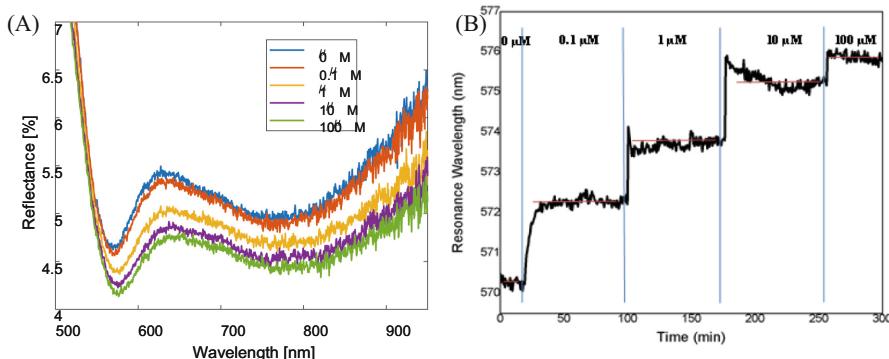


Fig. 3. (A) Reflection spectra in solutions with varying Thiram concentrations after stabilization. (B) Sensorgram showing Thiram concentration over time: The average values of the resonant wavelength after the spectrum stabilizes are marked by the horizontal red lines, while the time instants where the solutions were changed are shown with the vertical lines.

In Fig. 4 the calibration curve is reported, a semi-logarithmic scale is used to show the attenuation band shift with respect to Thiram concentration changes. The baseline resonance wavelength (zero concentration) is indicated, along with the mean values and standard deviations for each data point. The experimental data fit a sigmoidal curve, with parameters $\Delta\lambda_{\text{MAX}} = 6.16 \text{ nm}$, $x_0 = 0.54 \mu\text{M}$, and $p = 0.44$, indicating the sensor's

dynamic range and sensitivity [12, 13] was obtained through the following formula:

$$\Delta\lambda = \Delta\lambda_{MAX} \cdot \left[\frac{\left(\frac{x}{x_0} \right)^p}{1 + \left(\frac{x}{x_0} \right)^p} \right] \quad (1)$$

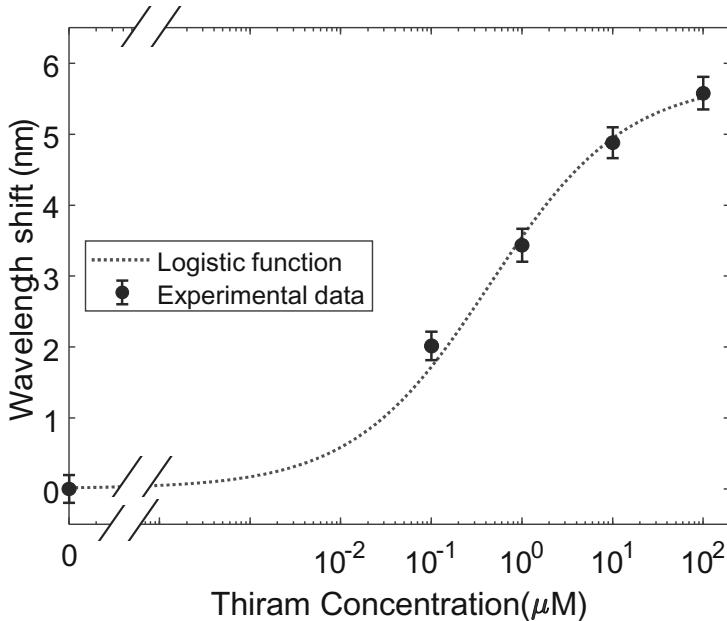


Fig. 4. Calibration curve of the sensor using semi-log scale, obtained from the sensogram of Fig. 3(B). The value corresponding to each concentration of Thiram is expressed in terms of the mean value and the respective standard deviation within 50 acquisitions, whereas the sigmoidal behavior is showcased with dotted line.

3 Conclusions

In this contribution, we have developed a simple fiber optic probe starting from a cladding removed MMF which was subsequently coated with AuNPs. The reflection spectrum of this device is modulated by the absorption spectrum of AuNPs. After a refractometric characterization, the performance of the device was investigated for chemical sensing by using Thiram pesticide as a target. Notably, the simplicity and cost-effectiveness of this sensor provide a distinct advantage over more complex surface enhancement Raman spectroscopy methods and offering a detection at concentrations lower than UV-VIS methods.

References

1. Wang, X., Wolfbeis, O.S.: Fiber-optic chemical sensors and biosensors (2015–2019). *Anal. Chem.* **92**, 397–430 (2020). <https://doi.org/10.1021/acs.analchem.9b04708>
2. Srivastava, A., Esposito, F., Campopiano, S., Iadicicco, A.: Mode transition phenomena into an in-fiber Mach-Zehnder interferometer. *Opt. Fiber Technol.* **80**, 103481 (2023). <https://doi.org/10.1016/j.yofte.2023.103481>
3. Choudhary, S., Esposito, F., Sansone, L., et al.: Lossy mode resonance sensors in uncoated optical fiber. *IEEE Sens. J.* **23**, 15607–15613 (2023). <https://doi.org/10.1109/JSEN.2023.3280675>
4. Lee, S., Song, H., Ahn, H., et al.: Fiber-optic localized surface plasmon resonance sensors based on nanomaterials. *Sensors* **21**, 819 (2021). <https://doi.org/10.3390/s21030819>
5. Singh, R., Wang, Z., Marques, C., et al.: Alanine aminotransferase detection using TIT assisted four tapered fiber structure-based LSPR sensor: from healthcare to marine life. *Biosens. Bioelectron.* **236**, 115424 (2023). <https://doi.org/10.1016/j.bios.2023.115424>
6. Soares, M.S., Vidal, M., Santos, N.F., et al.: Immunosensing based on optical fiber technology: recent advances. *Biosensors* **11**, 305 (2021). <https://doi.org/10.3390/bios11090305>
7. Sypabekova, M., Hagemann, A., Rho, D., Kim, S.: Review: 3-aminopropyltriethoxysilane (APTES) deposition methods on oxide surfaces in solution and vapor phases for biosensing applications. *Biosensors* **13**, 36 (2022). <https://doi.org/10.3390/bios13010036>
8. Moslemi, A., Sansone, L., Esposito, F., et al.: Optical fiber probe based on LSPR for the detection of pesticide Thiram. *Opt. Laser Technol.* **175**, 110882 (2024). <https://doi.org/10.1016/j.optlastec.2024.110882>
9. Lin, Y., Zou, Y., Mo, Y., et al.: E-beam patterned gold Nanodot arrays on optical fiber tips for localized surface Plasmon resonance biochemical sensing. *Sensors* **10**, 9397–9406 (2010). <https://doi.org/10.3390/s101009397>
10. Zhang, Y., Ding, L., Zhao, J., et al.: Localized surface Plasmon resonance-based fiber optic biosensor for acetylcholine detection. *IEEE Sens. J.* **23**, 25987–25995 (2023). <https://doi.org/10.1109/JSEN.2023.3304619>
11. Parham, H., Pourreza, N., Marahel, F.: Determination of thiram using gold nanoparticles and Resonance Rayleigh scattering method. *Talanta* **141**, 143–149 (2015). <https://doi.org/10.1016/j.talanta.2015.03.061>
12. Dudley, R.A., Edwards, P., Ekins, R.P., et al.: Guidelines for immunoassay data processing. *Clin. Chem.* **31**, 1264–1271 (1985). <https://doi.org/10.1093/clinchem/31.8.1264>
13. Esposito, F., Sansone, L., Srivastava, A., et al.: Long period grating in double cladding fiber coated with graphene oxide as high-performance optical platform for biosensing. *Biosens. Bioelectron.* **172**, 112747 (2021). <https://doi.org/10.1016/j.bios.2020.112747>



True Time Delay System Using Phase Change Materials

Rahuldas Kutteeri¹, Martino De Carlo¹, Francesco De Leonardis¹, Richard A. Soref², and Vittorio M. N. Passaro¹(✉)

¹ Photonic Research Group, Department of Electrical and Information Engineering, Politecnico di Bari, Bari, Italy

vittorio.passaro@poliba.it

² University of Massachusetts, Boston, USA

Abstract. By exploiting the high refractive index contrast between the two material phases (amorphous and crystalline) of a phase change material (PCM) and by incorporating the PCM inside a photonic Bragg Grating Resonator (BGR), programable on/off reflectors can be obtained around the operating wavelength. Delay lines containing several BGRs (geometrically separated by specific paths) are designed, and true time delay (TTD) is induced in optical signals in each delay line. In details, the optical delay introduced by each delay line depends on the position of the single BGR along the line that is programmed to work as reflector at the operating wavelength of ~ 1550 nm. By controlling the BGRs in each path, distinct time delays are introduced by different delay lines and used to control a phased-array antenna (PAA) able to steer a microwave beam towards specific angles. In this work design and simulations of different delay lines are presented to realize the steering of an antenna at multiple angles.

Keywords: Bragg grating resonators · Phase Change Materials · True time delay · Microwave Photonics

1 Introduction

Radio frequencies (RF) can be optically carried over optical channels. True time delay (TTD) for phase shifting of such signals (RF) can be performed using photonic beam forming techniques in the optical domain [1–4]. Traditional electronic phase shifter based phased array antennas (PAA) faced beam squinting problem and limited application due to narrow band [5, 6].

TTD method solves the problem of beam squinting and possesses many advantages over traditional electronic phase shifter based PAA such as compact size, light weight, absence of electro-magnetic interference. TTD can provide band width nearly whole RF band (100 GHz) [7], where electronic phase shifters could only provide a bandwidth of 10% ~ 30% of their center frequency [8]. TTD is achieved by selecting various optical path lengths, here the optical path length is chosen by the position of Bragg grating resonator (BGR) incorporating phase change material (PCM) in the designed delay line.

Many of previously studied hybrid optical path delay approaches were later replaced by fully monolithic photonic integrated circuits (PIC), so reducing the sizes from cm to lower scale.

This study investigates the possibility of employing PCM within BGRs for achieving precise TTD for beam steering of microwave phased array antenna (MPAA), offering advantages over previous study [9]. Our primary objective was to optimize the design of the TTD controller to enable both transmission and reflection functionalities, aligning all BGRs initially at a shared resonance wavelength (~ 1468 nm) in the amorphous state of PCM.

2 Basic Concept

Figure 1 illustrates the operation of an on-chip integrated optical True Time Delay (TTD) beamforming system. The device is based on a laser source emitting an optical signal corresponding to ~ 1550 nm, which is then split into multiple paths (delay lines) using couplers. Each delay line incorporates several PCM-based Bragg Grating Resonators (BGRs), working as programmable on/off reflectors.

The optical delay introduced by each delay line depends on the position of the single BGR along the line that is programmed to work as a reflector at the operating wavelength of 1550 nm. The PCM-based BGRs are programmed using reversible phase transition property of PCMs, which adjust their reflection wavelength.

By manipulating the BGRs in each path, distinct time delays are introduced by different delay lines. The optical signals obtained by the several delay lines are then used to modulate the radio signals at an antenna radiator array, thus realizing a phased-array antenna (PAA) able to steer a microwave beam towards specific angles. All the optical components are integrated onto a single chip, enhancing both efficiency and compactness.

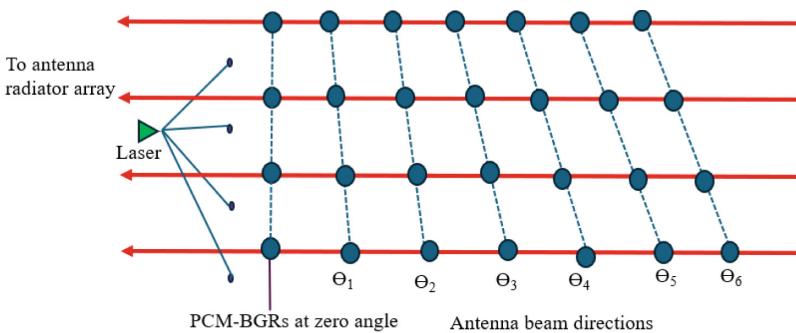


Fig. 1. Basic concept of on-chip integrated optical TTD beamforming system within the antenna.

A principle scheme, containing 7 PCM-based integrated BGRs separated by SOI (Silicon on Insulator) waveguides, is shown in Fig. 2, while the PCM-based BGR is sketched in Fig. 3. Sb₂S₃ (Antimony trisulfide) is used as PCM for precise time delay control, due

to its integration into BGRs, very low losses and high refractive index contrast between amorphous and crystalline states [10]. Activating (transition from amorphous to crystalline PCM state) a specific BGR, its resonance wavelength will shift from λ_{BA} to λ_{BC} (from 1468 nm to 1550 nm).

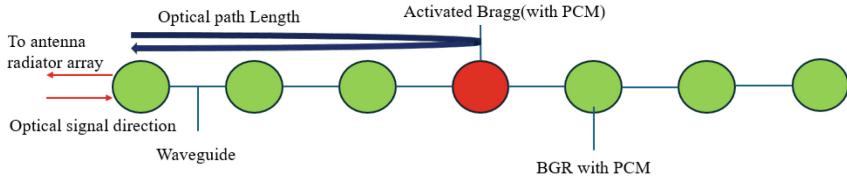


Fig. 2. Delay line containing a cascade of BGRs connected by waveguide sections. The red circle shows the activated BGR (PCM in crystalline phase).

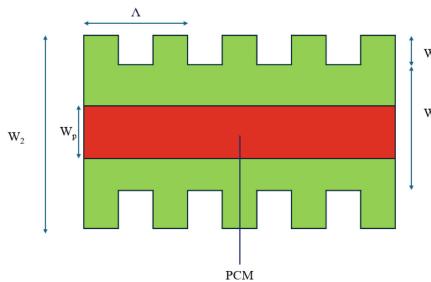


Fig. 3. Top view of Silicon-on-insulator strip showing the geometry of one PCM coated Bragg-grating resonator (BGR).

The Bragg grating in Fig. 3 is structured by alternating two sections, one with a width of 450 nm (W_1) and the other 550 nm (W_2) wide, both sharing a height of 220 nm (H). A period (Δ) of 306 nm ensures resonance at 1550 nm in its crystalline phase. Additionally, the PCM height matches the silicon in the BGR (220 nm), with a selected width (W_p) of 150 nm.

The spectral profile of the guided wave may be effortlessly translated alongside the wavelength when PCM changes from one phase to another. The wavelength of operation is set to λ_{BC} . Adjacent BGRs are separated by a waveguide, as in Fig. 2. Initially, all PCMs are in amorphous state (turned off) and all BGR spectra are aligned at the same resonant wavelength λ_{BA} (i.e., 1478 nm), as in Fig. 4a. Under this situation the delay line has no reflection. When a specific BGR is activated (changing from amorphous to crystalline phase), its reflection wavelength changes from λ_{BA} to λ_{BC} and the guided wave will be reflected as shown in Figs. 2 and 4b. By turning on different PCM-BGRs in different delay line, delay is experienced by the reflected wave because of different path length (depending on the position of turned on BGR) and desired beam steering can be performed by carefully designing the delay line.

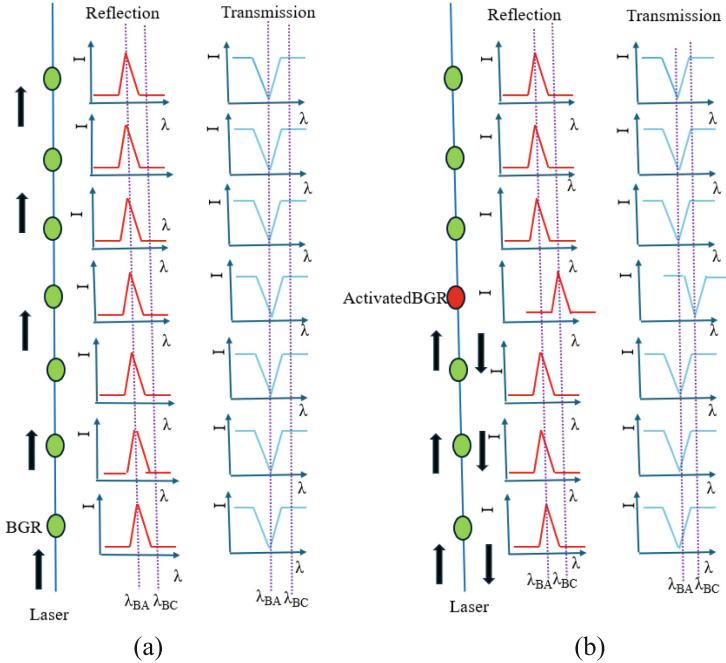


Fig. 4. Programmable optical delay line using PCM-BGRs for the selection of any one of four optical delays. Here λ_{BC} is the wavelength of operation: (a) initial all amorphous (λ_{BA}) BGR line; corresponding R profiles and T profiles; (b) Activation of the 4th BGR (amorphous to crystalline); shift of R profile and shift of T profile for the activated BGR.

3 Numerical Results

We have first calculated the shift along the wavelength axis for the designed single BGR with PCM as shown in Fig. 5 and then examined a series of 7-BGRs delay lines (Fig. 6) to achieve beam steering in the X band (8 to 12 GHz), by adjusting non uniform waveguide lengths between adjacent BGRs (NL indicating the delay line number) [8]. This varied spacing along the delay line allows to achieve the desired beam steering characteristics along specific angles. D_{min} is calculated as 370.4 μm from Eq. (1), where c represents the free space light speed and Θ_{min} the minimum steering angle (8°), n_{eff} is the effective refractive index of BGR and f_{max} is the maximum microwave frequency in the band. The scheme is designed for a set of angles (Θ_i) ranging from 8° to 16° , 24° , 32° , 40° and 48° , according with Eq. (2). In Fig. 2a. $S = 1.25$ cm represents the vertical separation between two delay lines for the X band.

$$d_{min} = \frac{c}{4f_{max}n_{eff}} \sin \Theta_{min} \quad (1)$$

$$d_{i,NL} = NL \cdot d_{min} \frac{\tan \Theta_i}{\tan \Theta_{min}} \quad (2)$$

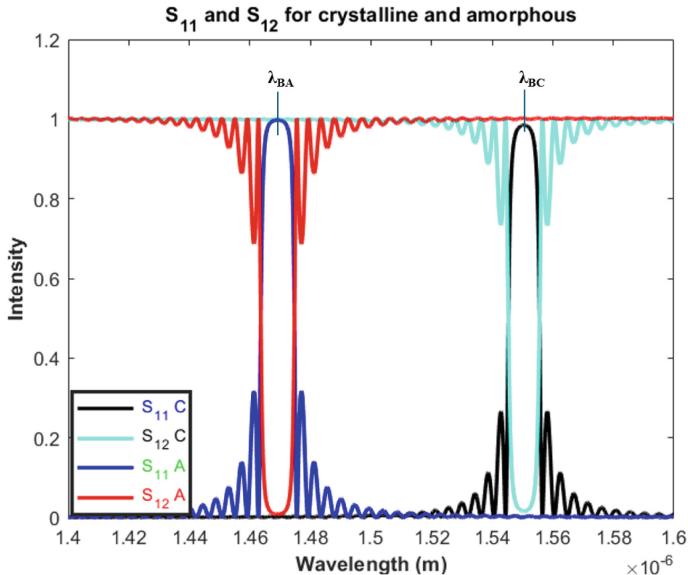


Fig. 5. Reflection and transmission spectral response of PCM coated Bragg resonator. S_{11} and S_{12} are referred as reflection and transmission, in crystalline or amorphous state, respectively.

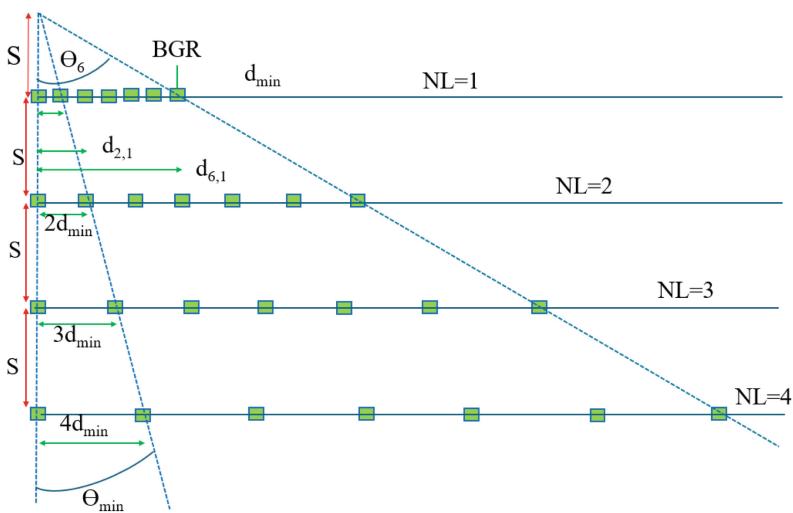


Fig. 6. Array of delay lines with corresponding steering angles.

The group delay of the delay line is calculated as $d\phi/d\omega$, where ϕ is the total phase of the reflected signal, and ω is the angular frequency. Figure 7 illustrates an example of signal amplitude and phase when the fourth BGR in the first delay line is activated. Figure 8 illustrates the varying time delay induced when each BGR is activated across

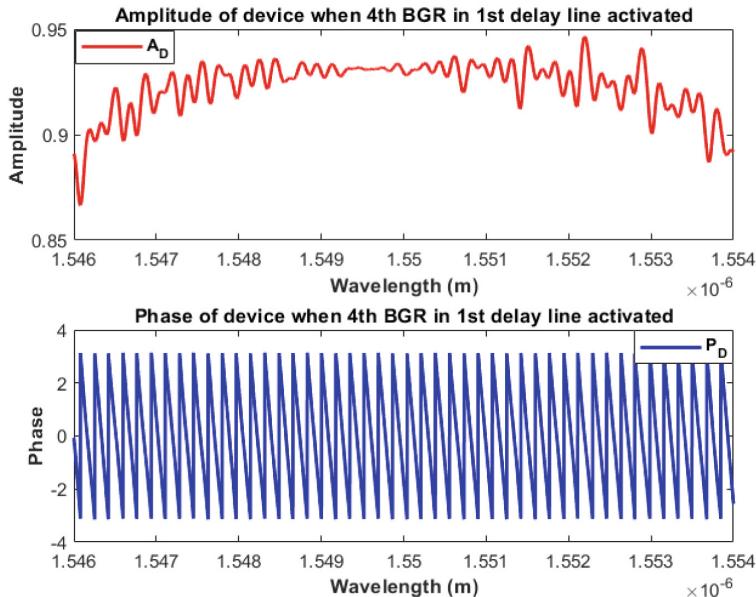


Fig. 7. Signal amplitude (A_D) and phase (P_D) when the fourth BGR in the first delay line is activated.

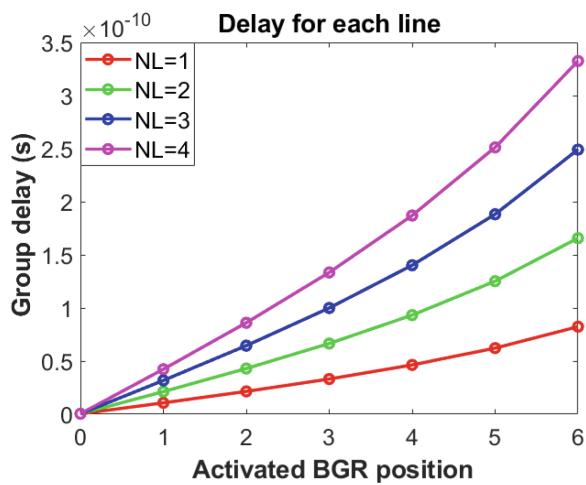


Fig. 8. Group delay induced when each BGR is activated for different delay lines (NL).

different delay lines. The maximum induced time delay achieved (with the last BGR activated) for each line is 82.37 ps, 165.7 ps, 249.1 ps, and 332.5 ps, respectively.

4 Conclusion

This study briefly shows the integration of Phase Change Materials with Bragg Grating Resonators for achieving photonic tunable true time delay in phased array antennas, enhancing performance and enabling a versatile optical integrated approach.

Acknowledgments. This work has been partially supported by the European Union under the Italian National Recovery and Resilience Plan (NRRP) of NextGenerationEU, partnership on “Telecommunications of the Future” (PE00000001 - program “RESTART”).

References

1. Duarte, V.C., Drummond, M.V., Nogueira, R.N.: Photonic true-time delay beamforming system for a phased array antenna receiver (2015). <https://doi.org/10.1109/IMOC.2015.7369095>
2. Ye, X., et al.: Optical true time delay unit for multi-beamforming. *Opt. Express* **23**(8), 10002–10008 (2015)
3. Jung, B.M., Shin, J.D., Kim, B.G.: Optical true time-delay for two dimensional X-band phased array antennas. *IEEE Photon. Technol. Lett.* **19**(12), 877–879 (2007)
4. Subbaraman, H., Chen, M.Y., Chen, R.T.: Photonic crystal fiber based true-time-delay beamformer for multiple RF beam transmission and reception of an X-band phased-array antenna. *J. Lightwave Technol.* **26**(15), 2803–2809 (2008)
5. Mailloux, R.J.: *Phased Array Antenna Handbook*. Artech House (1994)
6. Yao, J.P.: A tutorial on microwave photonics. *IEEE Photon. Soc. News Lett.* **26**(2), 4–12 (2012)
7. Nguyen, L.V.T.: Optical RF phase shifter design employing optical phase manipulation and coherent detection – part i: concept proposal. *Int. J. Microwave Opt. Technol.* **6**(5), 301–309 (2011)
8. Wu, Y.S., Lin, X.Q., Zhang, J., Jiang, Y., Cheng, F., Fan, Y.: Broadband and wide range tunable phase shifter based on composite right/left handed transmission line. *J. Electromagn. Waves Appl.* **26**(10), 1308–1314 (2012)
9. Song, C., et al.: Compact nonvolatile 2×2 photonic switch based on two-mode interference. *Optics Express* **30**, 30430 (2022)
10. Soref, R.A., De Leonardi, F., Passaro, V.M.N.: Integrated on-chip bragg time-delay system for thermo-optical control of a microwave antenna. *J. Lightwave Technol.* **36**, 5849–5856 (2018)

Power Electronics



Model-Based Design and AI for Monitoring Systems in Automotive Power Electronics

Pierpaolo Dini¹ , Sergio Saponara¹ , Giovanni Basso¹, and Claudio Romano²

¹ Department of Information Engineering, University of Pisa, Via G. Caruso, 56100 Pisa, Italy
pierpaolo.dini,sergio.saponara,giovanni.basso}@unipi.it

² Ideas & Motion, Via Moglia, 19, 12062 Cherasco, Italy
claudio.romano@ideasmotion.com

Abstract. The article presents an innovative methodology for the design and validation of monitoring and anomaly detection algorithms, focused on the aging phenomenon linked to the anomalous modification of the $R_{ds_{on}}$ in the switching devices of electronic systems of power in high-performance electric vehicles. The case study concerns an electric traction system with a three-phase axial flux synchronous motor integrated into a drive wheel (Elaphe) and a high-efficiency three-phase inverter with SiC (silicon carbide) technology. The methodology is developed in four phases: 1) creation of a real-time model of electric traction, validated with experimental data from WLTP tests; 2) Generation of a virtual dataset representing aging, via anomaly injection emulating the phenomenon with a scaling factor based on the $R_{ds_{on}}$ on the motor phase current; 3) Design of an estimator of the $R_{ds_{on}}$ using an Artificial Neural Network (ANN) regression model, including feature extraction and reduction techniques. 4) Experimental validation of the method through PIL (Processor-In-the-Loop) tests, integrating the monitoring algorithm on the NXP's32k144 embedded platform, making it interact with the electric traction model with anomaly injection.

Keywords: Power Electronics · Automotive · Model-based Design · Simulation · Embedded Devices · Artificial Neural Networks

1 Introduction

Power electronic systems in modern electric and hybrid vehicles have become more efficient and complex, using wide-bandgap (WBG) technology to increase switching frequencies, improve signal quality and reduce conduction losses [1]. Among these technologies, SiC (silicon carbide) MOSFETs stand out for their low resistance and high ability to handle high frequencies, making them ideal for power systems in electric vehicles [2]. However, these devices are sensitive to deterioration under harsh operating conditions, such as high temperatures and fast switching frequencies, complicating the identification of aging mechanisms [3]. Therefore, it is essential to integrate monitoring algorithms into power systems to ensure timely maintenance and system safety.

The most applied monitoring systems in power converters use sensors to measure currents and voltages, but they are expensive and complex [4]. An alternative method is

the inductive coupling method for impedance estimation, which is fast and safe but sensitive to component position [5]. AI-based algorithms, such as artificial neural networks, are used to detect anomalies, but they require a lot of data and computing resources. One promising approach is to combine accurate mathematical models with neural networks, reducing computational complexity and improving the interpretability of results.

The article proposes an innovative methodology for monitoring and detecting anomalies in vehicle power electronic systems, with key contributions:

- Development of a real-time model of electric traction, validated with experimental data.
- Creation of a virtual dataset representative of aging using simulations.
- Using a compact AI model for integration on resource-constrained embedded platforms.
- Validation using PIL tests, integrating the monitoring algorithm with the electric traction model and anomaly injection.

2 Methodology Description

The proposed innovative methodology is divided into different design phases. In the first stage, a dynamic electro-thermal model for electric traction is developed, which includes real components of the inverter and synchronous traction motor. This model is validated through phase current and angular velocity measurements during a WLTP cycle on the vehicle, allowing the dynamic model to be evaluated and coefficients not provided directly by the electric car manufacturer to be obtained. Furthermore, a thermal model is established to estimate the conduction and switching losses of inverter components based on the data provided by manufacturers.

In the second phase, we proceed with the extraction and reduction of features from the residual dataset, forming a time series dataset using techniques such as multi-dimensional scaling and PCA to select the relevant features. The third phase concerns the design of a regression model based on a feedforward artificial neural network, aimed at estimating the dynamics of the $R_{ds_{on}}$. During this phase, the size of the neural network is evaluated, and the regularization parameters are optimized to balance accuracy and processing time, also verifying the generalization capacity of the model.

The last phase involves Processor-In-the-Loop (PIL) validation, integrating the aging monitoring and detection system on an embedded platform (NXP S32K144). The realistic electric traction model, with an injected aging model, is simulated on the Speedgoat Baseline platform, testing the algorithm on various anomaly profiles.

The workflow is visually described in Fig. 1, which show the detail identification and reduction process steps for the compact model design and the methodology for collecting the anomaly dataset, specifically the aging of the SiC MOSFET components.

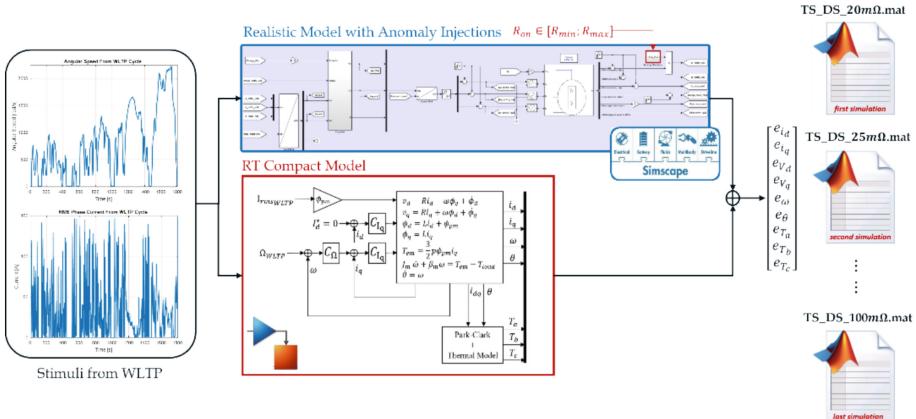


Fig. 1. Schematic workflow description of the proposed methodology.

3 Electro-Thermal Model

The section describes the design of a real-time electrothermal model for an electric drive system, including the inverter and permanent magnet synchronous motor. The experimental data were collected at the Ideas&Motion Laboratory, imposing the simulation of a WLTP cycle, allowing us to carry out parameter estimation and model validation (see Fig. 2). In Table 1 are reported the main parameters of the motor-wheel, provided by manufacturer (and some estimated by data driven procedure).

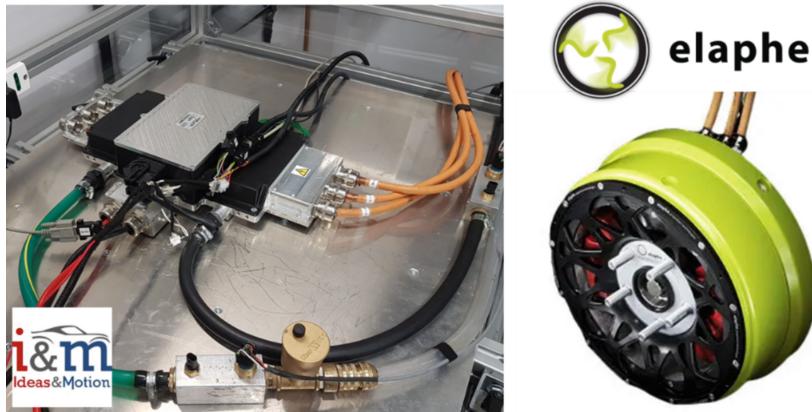


Fig. 2. Ideas&Motion Experimental Setup.

Table 1. Main parameters of the electric drive model.

Symbol	Description	Value	Unit
P_m	Rated motor power	60	kW
T_{em}	Motor torque	87.75	Nm
V_{dc}	DC Voltage (inverter)	350–450	V
I_{rms}	Phase current	145	0000
ω_r	Rotor speed	5000	rpm
R_s	Stator resistance	50	0000
L_{eq}	Stator inductance	800	0000
k_ϕ	p.m. flux linkage	0.192 (estimated)	Vs
J_r	rotor inertia	0.011	0000
b_r	friction coefficient	0.001417 (estimated)	Nms
p	pole pairs	8	-

To avoid the complexity of directly modeling the inverter switching dynamics, an “indirect” monitoring approach was used. This assumes that the average input power matches the average output power, simplifying the simulation (see Fig. 3).

The inverter efficiency is assumed to be nearly unity, with losses modeled algebraically. The inverter is represented by a delay block in the model, which takes switching delays into account and introduces noise to simulate physical disturbances.

The model uses coordinate transformations (Park and Blondel) to represent the dynamics of the three-phase synchronous machine in a simpler and equivalent form (see Eq. 1 which represent the Park Model [6, 7]). Electric power drive modeling integrates these transformations to accurately describe motor behavior.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = R_s \begin{bmatrix} I_d \\ I_q \end{bmatrix} + L_{eq} \frac{d}{dt} \begin{bmatrix} I_d \\ I_q \end{bmatrix} + \begin{bmatrix} -p\omega_r L_{eq} I_q \\ k_\phi + p\omega_r L_{eq} I_d \end{bmatrix} \quad (1)$$

$$J_r \frac{d\omega_r}{dt} + b_r \omega_r = T_{em} - T_{load}$$

The model also includes an identification algorithm that uses gradient descent to determine unknown parameters from experimental data, with the goal of minimizing errors between simulated and real data (Fig. 4).

Inverter losses are modeled mathematically, with switching losses (see Fig. 5) depending on voltage, current, and switching frequency; conduction losses on resistance and current in active state; and driving losses on gate charge and switching frequency (see Eq. 2). The overall inverter efficiency is calculated considering these losses, and model estimates are validated against manufacturer claims and experimental data (see

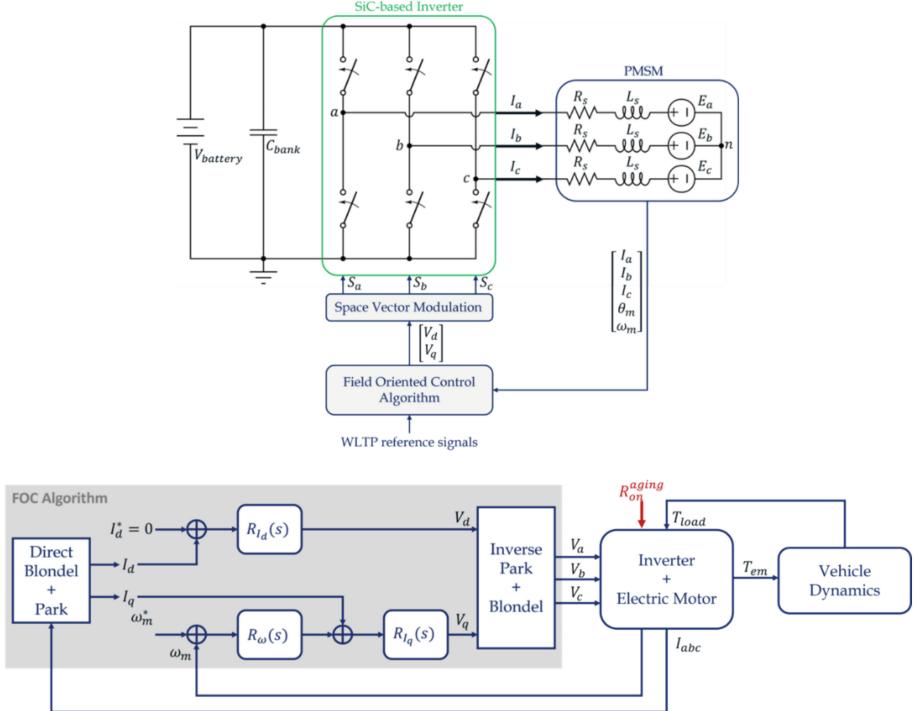


Fig. 3. Simplified (Real-Time) Power Drive Model.

Table 2).

$$\begin{aligned}
 P_{sw} &\cong \frac{1}{2}(V_d I_d + V_q I_q)(t_{sw_{on}} + t_{sw_{off}}) f_{sw} \\
 P_{joule} &\cong R_{ds(on)}(I_d^2 + I_q^2) \\
 P_{driver} &= V_{driver} Q_G(tot) f_{sw}
 \end{aligned} \tag{2}$$

For each of the SiC devices, the total losses are represented by the sum of the three modeled contributions, \$P_{loss} = P_{sw} + P_{joule} + P_{driver}\$, and the estimate of the junction temperature \$T_j\$ results from the Foster linear circuit model. Equation 3 reports the thermal dynamics of junction temperature.

$$T_j(t) = P_{loss} R_{th_{jc}} (1 - e^{-t/\tau_{th}}) + T_c \tag{3}$$

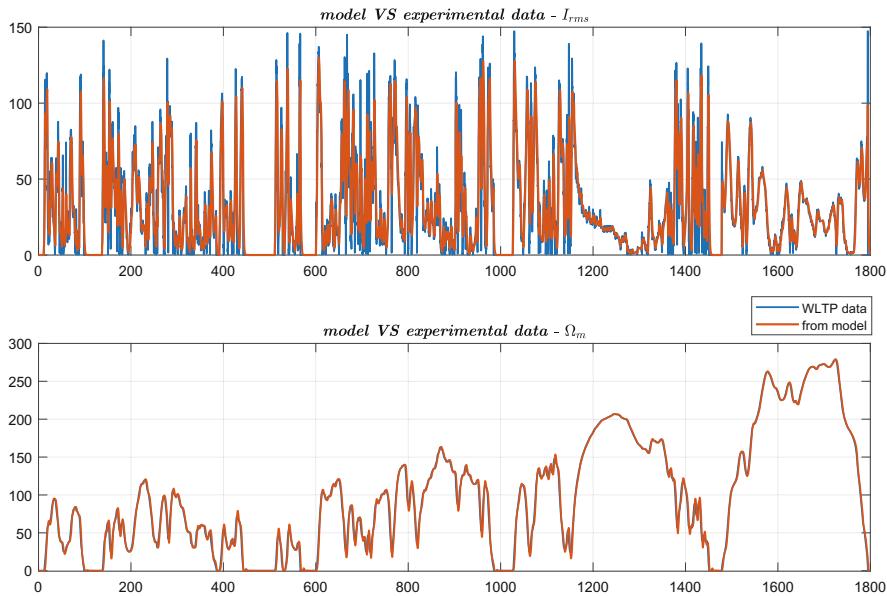


Fig. 4. Experimental data vs real-time model simulation (after model assessment).

Table 2. Main parameters of the SiC devices integrated in the traction inverter [8].

Symbol	Description	Value	Unit
$V_{ds_{max}}$	Drain-Source Voltage	650	V
$I_{d_{max}}$	Drain-Source Current	168	A
V_{gs}	Gain-Source Voltage	-5/22	V
$R_{ds(on)}$	Drain-Source resistance	18	$m\Omega$
$R_{th_{jc}}$	Junction-Case thermal resistance	0.24	C°/W
$Q_{G(tot)}$	total Gate charge (turn-on)	283	nC
$t_{sw_{on}}$	turn-on total delay	25	ns
$t_{sw_{off}}$	turn-off total delay	11	ns
f_{sw}	switching frequency	50	kHz

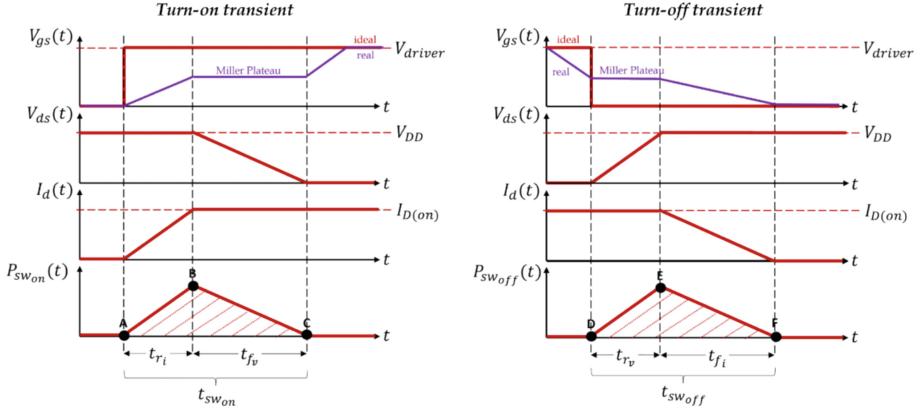


Fig. 5. Schematic representation of the considered switching losses model.

4 SiC Ageing Virtual Dataset Collection

For the aging simulation, the real-time model of the electric drive is “perturbed”. An aging model is applied to collect data on the impact of changes in $R_{ds(on)}$. By repeatedly simulating the WLTP test with different values of $R_{ds(on)}$, time series of residuals between the variables of the compact and realistic models are obtained. This data represents the behavior of the aging system.

The dataset for the neural network design is created as follows: 17 WLTP simulations are run for values of $R_{ds(on)}$ ranging from 25 mΩ to 100 mΩ. Each simulation produces 18,000 samples for each variable, accumulating 10 samples per second over the entire duration of the WLTP cycle. These samples include virtual measurements of voltages, equivalent currents, junction temperatures, speed and angular position of the motor.

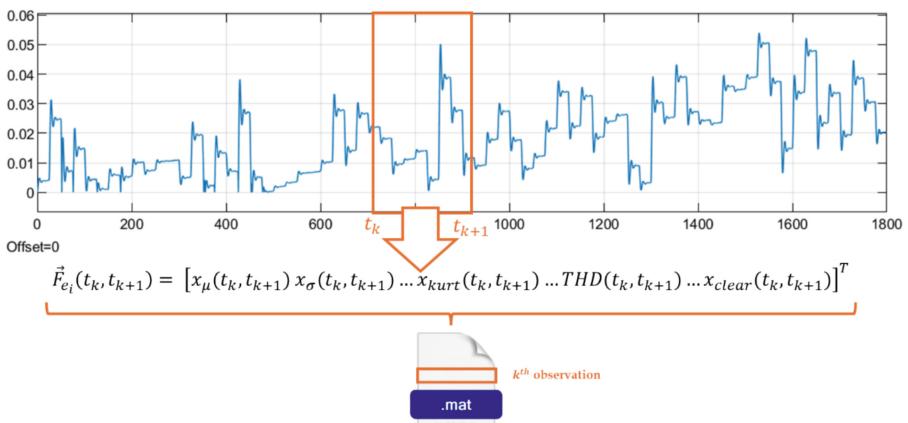


Fig. 6. Schematic explanation of the features extrapolation procedure.

After data collection, features are extracted from the time series (see Fig. 6). The extracted features are divided into three groups: statistical, pulse and signal processing metrics [9]. This extraction process generates a set of 99 features for each signal. Subsequently, PCA (Principal Component Analysis) is applied to reduce the number of features to 18, maintaining more than 98% of the original information content. The resulting dataset is then used to train the neural network, which is designed to be simple and can be integrated in embedded system (Table 3).

Table 3. Features computed from time-series in each extrapolation time horizon.

Selected Feature	Meaning
$x_\mu = \frac{1}{n} \sum_k x_k$	Mean Value represents the average quantity of a set of numbers
$x_\sigma = \sqrt{\frac{1}{n} \sum_k (x_k - x_\mu)^2}$	Standard Deviation indicates the dispersion or variation of data from the mean
$x_{rms} = \sqrt{\frac{1}{n} \sum_n x_k ^2}$	Root Mean Square represents an indication of the “mean value” in the context of fluctuating data
$x_{skew} = \frac{\frac{1}{n} \sum_k (x_k - x_\mu)^3}{\left(\sqrt{\frac{1}{n} \sum_k (x_k - x_\mu)^2}\right)^3}$	Skewness measures the skewness in the distribution of data
$x_{kurt} = \frac{\frac{1}{n} \sum_k (x_k - x_\mu)^4}{\left(\frac{1}{n} \sum_k (x_k - x_\mu)^2\right)^2}$	Kurtosis indicates how concentrated or distributed the data are in the tails of a distribution
$SNR = \frac{P_{signal}}{P_{noise}}$	Signal-to-Noise Ratio measures how strong the signal of interest is relative to background noise
$THD = \frac{\sqrt{\sum_{k \geq 2} P_k^2}}{P_1}$	Total Harmonic Distortion measures the importance of the first harmonic relative to harmonics at higher frequencies
$SINAD = \frac{P_{signal} + P_{noise} + P_{distortion}}{P_{noise} + P_{distortion}}$	Signal-to-Noise and Distortion Ratio combines signal-to-noise ratio with harmonic distortion, indicating signal quality
$x_{if} = \frac{\max x_k }{\frac{1}{n} \sum_k x_k }$	Instantaneous Flatness measures how quickly a signal reaches its maximum peak value
$x_{cf} = \frac{\max x_k }{\sqrt{\frac{1}{n} \sum_k x_k ^2}}$	Crest Factor represents the ratio of a signal’s peak value to its RMS value, indicating signal peaks
$x_{clear} = \frac{\max x_k }{\left(\sqrt{\frac{1}{n} \sum_k \sqrt{x_k}}\right)^2}$	Clearance Factor a safety measure indicating how much a critical quantity exceeds the minimum value needed for safe operation

During the real-time usage phase, features are continuously computed and reduced to provide input to the AI model for estimating $R_{ds(on)}$.

5 Processor-In-The-Loop Results

The experimental validation based on Processor-In-the-Loop (PIL) tests allows evaluating the performance of the proposed algorithm integrated on an embedded platform with computational resources typical of automotive applications [10, 11]. The validation setup includes CAN protocol-based traffic management devices, a Speedgoat Baseline device for interacting with the Simulink simulation environment, and an NXP s32k144 microcontroller evaluation board.

$$\begin{aligned} NN_{size} &= F(N_{features}, N_{layers}, N_{neurons}, DataType) \\ &= sizeof(DataType) \left(N_f n_{L_1} + \sum_{i=1}^{N_L-1} n_{L_i} n_{L_{i+1}} \right) \\ &= 8Bytes * 1100neurons \cong 9kB \end{aligned} \quad (4)$$

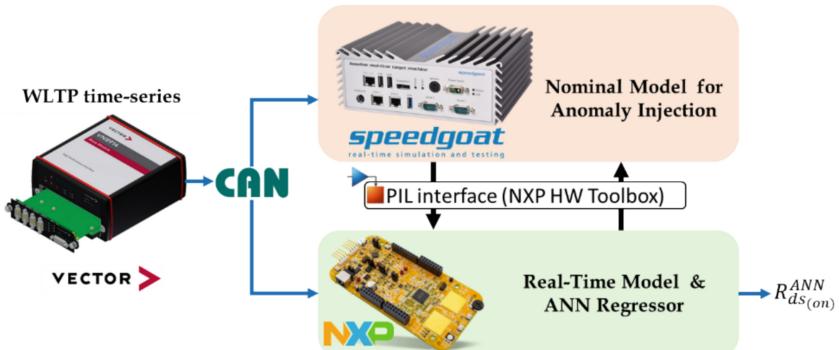


Fig. 7. Schematic representation of the real-time Processor-In-the-Loop validation procedure.

As estimated in Eq. 4, size estimation is based on the number of layers N_L , the number of neurons per layer i^{th} , and the number of features fed into the AI model N_f . The memory allocation for the selected neural network evaluated during the performance validation phase is around 9 kB, which is perfectly suitable for embedded integration, since EVB s32k144 board has 256 kB SRAM available. The feedforward model is fully algebraic, ensuring limited but comparable throughput to that of the real-time model, with most computational resources allocated to computation and feature reduction.

The monitoring method, which includes the compact model, the feature calculation block and the neural network for estimating the $R_{ds(on)}$, has a response time of less than 12 ms, making it suitable for real-time monitoring during device operation and for estimating $R_{ds(on)}$ for aging assessment purposes. The real-time estimation results during the PIL validation show two tested scenarios: slow and linear variation of the nominal resistance value from $m\Omega$ to $\$100 m\Omega$, and an alternating profile to verify the ability of the model to generalize the data, confirming the effectiveness of the method for monitoring and evaluating aging. Figure 7 shows the obtained results during real-time PIL simulation (Fig. 8).

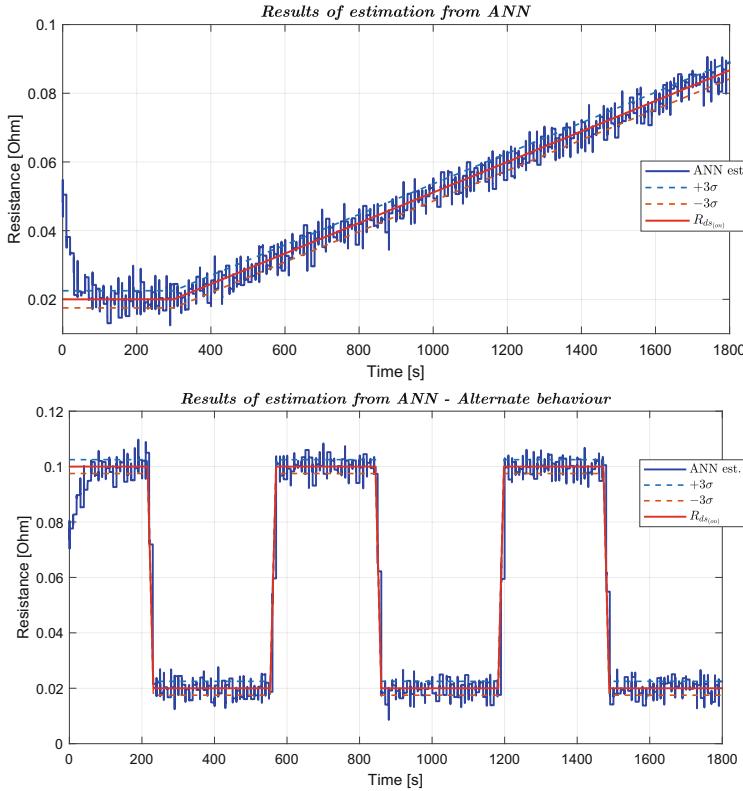


Fig. 8. PIL results: (top) with slowly linear change of resistance; and (bottom) alternated resistance variation.

6 Conclusions

In previous sections, we explored the innovative aspects of the proposed method for monitoring system design, which integrates low computational complexity modeling with an artificial neural network-based regression model. The methodology demonstrates promising performance, compatible with the embedded Cortex-M4 platform, and accurately estimates $R_{ds(on)}$, comparable to direct methods using acquired V_{ds} and I_{ds} values. Unlike direct estimation methods, which require abnormal operating conditions and extensive data accumulation, the proposed method models the aging phenomenon through variations in $R_{ds(on)}$, generating a statistically relevant dataset. This approach, coupled with a high simulation speed model, allows rapid data accumulation for studying the aging phenomenon, thus avoiding lengthy and destructive measurement campaigns. The proposed algorithm undergoes rigorous evaluation through the Processor-In-The-Loop (PIL) approach, a versatile and operationally sound tool critical for assessing system performance on the target embedded platform.

PIL facilitates synchronized run-time interaction between the simulation of the physical process and the algorithm on the MCU, allowing for the injection of anomalies and

realistic evaluation of the algorithm's responsiveness and accuracy. This approach not only provides a controlled environment for testing but also accelerates the validation process by enabling rapid data accumulation, crucial for studying aging phenomena.

References

1. Han, L., Liang, L., Kang, Y., Qiu, Y.: A review of SiC IGBT: models, fabrications, characteristics, and applications. *IEEE Trans. Power Electron.* **36**(2), 2080–2093 (2020)
2. Dini, P., Saponara, S., Chakraborty, S., Hosseinabadi, F., Hegazy, O.: Experimental Characterization & Electro-Thermal Modeling of Double Side Cooled SiC MOSFETs for Accurate and Rapid Power Converter Simulations. *IEEE Access* (2023)
3. Reigosa, P.D., Luo, H., Iannuzzo, F.: Implications of ageing through power cycling on the short-circuit robustness of 1.2-kV SiC mosfet s. *IEEE Transactions on Power Electronics* **34**(11), 11182–11190 (2019)
4. Erturk, F., Ugur, E., Olson, J., Akin, B.: Real-time aging detection of SiC MOSFETs. *IEEE Trans. Ind. Appl.* **55**(1), 600–609 (2018)
5. Dini, P., Basso, G., Saponara, S., Romano, C.: Real-time monitoring and ageing detection algorithm design with application on SiC-based automotive power drive system. *IET Power Electronics* (2024)
6. Bernardeschi, C., Dini, P., Domenici, A., Saponara, S.: Co-simulation and verification of a non-linear control system for cogging torque reduction in brushless motors. In: Software Engineering and Formal Methods: SEFM 2019 Collocated Workshops: CoSim-CPS, ASYDE, CIFMA, and FOCLASA, Oslo, Norway, September 16–20, 2019, Revised Selected Papers 17, pp. 3–19. Springer International Publishing (2020)
7. Dini, P., Saponara, S.: Cogging torque reduction in brushless motors by a nonlinear control technique. *Energies* **12**(11), 2224 (2019)
8. Semiconductor, O.: Datasheet of the SiC-mosfet NTHL015N065SC1. https://www.mouser.it/datasheet/2/308/1/NTHL015N065SC1_D-3150595.pdf. Accessed August 2023
9. Begini, A., Dini, P., Saponara, S.: Design and test of an LSTM-based algorithm for Li-Ion batteries remaining useful life estimation. In: International Conference on Applications in Electronics Pervading Industry, Environment and Society, pp. 373–379. Springer Nature Switzerland, Cham (2022)
10. Dini, P., Ariaudo, G., Botto, G., Greca, F.L., Saponara, S.: Real-time electro-thermal modelling and predictive control design of resonant power converter in full electric vehicle applications. *IET Power Electronics* **16**(12), 2045–2064 (2023)
11. Dini, P., Saponara, S.: Processor-in-the-loop validation of a gradient descent-based model predictive control for assisted driving and obstacles avoidance applications. *IEEE Access* **10**, 67958–67975 (2022)



In-Depth Analysis of the Electrical Ruggedness of Double-Sided Cooled Power Modules

Antonio Pio Catalano^(✉), Ciro Scognamillo, and Vincenzo d'Alessandro

Department of Electrical Engineering and Information Technologies, University Federico II,
Naples, Italy
antoniopio.catalano@unina.it

Abstract. In this contribution, the electrical ruggedness of double-sided cooled (DSC) power modules (PMs) for energy conversion applications is explored through simulations. Attention is focused on the spacing between the interfacing substrates of these assemblies, which is closely related to the size of the bumps. First, highly detailed finite element method (FEM) simulations in COMSOL Multiphysics are employed to evaluate voltage distribution, electric field, and parasitic capacitances of these structures. Subsequently, the above assessments are used to perform realistic SPICE simulations of a typical turn-off event; the maximum electric field waveform is monitored during the turn-off to evaluate the electrical ruggedness of the assemblies. A comparison between designers' estimations and the actual performance of the DSC PMs is also presented.

Keywords: Double-sided cooled · Electrical ruggedness · FEM simulations · Power modules · SPICE simulations

1 Introduction

In the modern scenario of energy generation, harvesting, and management, the role of electronics is increasingly crucial [1]. It is indeed true that every area of industrial engineering demonstrates a significant need for compact, efficient, reliable, and affordable semiconductor-based circuits devoted to the electrical power conversion. Decades ago, power modules (PMs) were conceived [1]; they consist of assemblies embedding electronic devices (such as VDMOSFETs or IGBTs) already arranged in a general-purpose configuration [2, 3]. These products have been successfully adopted in numerous industrial applications, to the point of steering research towards discovering increasingly effective solutions. Among these, the recent double-sided cooled (DSC) technology represents the most promising one for manufacturing PMs by virtue of (i) enhanced thermal behavior, (ii) reduced inductive loops, and (iii) the compactness of the assembly [4–6].

Although DSC PMs are already available on the market, intensive research is ongoing to further improve their performance and expand their safe operating area. A significant effort is devoted at enlarging their electrical ruggedness, which is the capability to withstand high voltages. Typically, the two interfacing direct bonded copper (DBC) substrates are biased with significantly different voltages (ΔV_{DBC}), potentially subjecting the insulating gel in the PM to a very high electric field (EF) [7]. This high EF may exceed

the gel's critical electric field (EF_{crit}) causing detrimental or irreversible effects such as partial discharge [8] or dielectric breakdown [9]. In the Authors' former contribution [9], the PM samples shown in Fig. 1 were manufactured to experimentally demonstrate that increasing the spacing between DBCs by using wider bump radii (r_{BUMP}) – contrary to expectations – leads to a reduction in the PM voltage capability. In Fig. 2, the schematic cross-section of a DSC PM shows the interfacing DBCs (top and bottom), the materials constituting the assembly, and the device and bump position. It can be easily noticed that the bump size determines the spacing between the DBCs [10, 11]. The experimental campaign has involved PM samples with bump radii ranging from 0.5 to 1.5 mm.

In this paper, we further investigate the electrical ruggedness of DSC PMs by (i) conducting a comprehensive examination of the voltage distribution within the assembly through finite-element method (FEM) simulations and (ii) using SPICE simulations to assess the PM electrical ruggedness under practical device usage conditions.

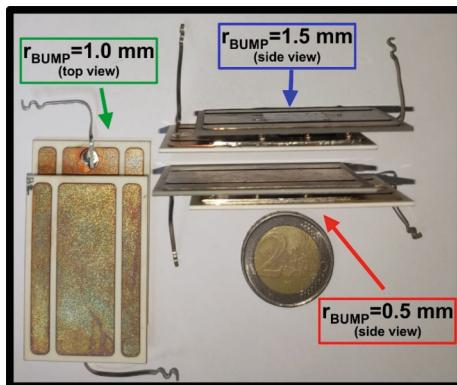


Fig. 1. Photograph of the DSC PM samples manufactured for the experimental campaign. The structure built in COMSOL mimics the ones depicted in the image. Both the side views (with $r_{BUMP} = 0.5$ mm and 1.5 mm) and the top view (with $r_{BUMP} = 1.0$ mm) are illustrated.

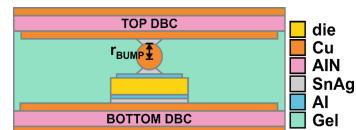


Fig. 2. Schematic cross-section (not to scale) of the DSC PM.

2 FEM Investigation

Following an analytical 1-D approach, the average EF (EF_{avg}) in the gel is expected to vary with r_{BUMP} as

$$EF_{avg} = \frac{\Delta V_{DBC}}{DBC\ distance} = \frac{\Delta V_{DBC}}{t_{die} + t_{solder} + 2 \cdot r_{BUMP}} \quad (1)$$

where t_{die} and t_{solder} are the thicknesses of the die and the solder layers, respectively. The electrical problem of DSC PMs resembling those shown in Fig. 1 was simulated with the FEM-based COMSOL Multiphysics software package [12] by varying r_{BUMP} in the range 0.5 ÷ 1.5 mm. The bias conditions were defined according to what shown

in Fig. 3. The device source (i.e., the top surface of the die) was set to GND, whereas the drain (bottom surface) is allowed to switch (SW). The location of triple points is also highlighted, as these are the regions where three materials are in contact (in Fig. 3, the involved materials are copper, semiconductor, and gel), and where the maximum EF value is expected to be located. Figure 4 illustrates the 3-D structure and mesh in COMSOL, while Fig. 5 provides details of the bumps for three r_{BUMP} values (lower, higher, and intermediate within the above range). The influence of the gate pad and bump was disregarded, as we demonstrated that they do not impact the research outcomes.

A first set of FEM simulation results are given in Fig. 6 as voltage maps in the PM at different bump sizes. The maps illustrate the voltage distribution in the structure with a $\Delta V_{\text{DBC}_S} = 2 \text{ kV}$. In the region far from the bump, a uniform EF is observed, with the voltage linearly decreasing from ΔV_{DSC} to 0 V. The region surrounding the die (denoted as the critical EF region) benefits from a small spacing (i.e., small r_{BUMP}) to achieve a more even bias, which, in accordance with the experimental results, reduces the maximum EF in the triple points area.

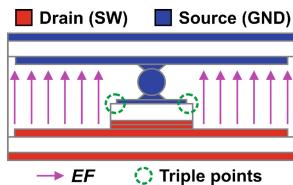


Fig. 3. Schematic depiction of the bias condition of the DSC PM used in FEM simulations. Triple points and vectors for the EF are also highlighted.

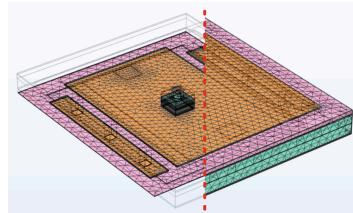


Fig. 4. 3-D domain in COMSOL Multiphysics with mesh and materials (colors are aligned with those in Fig. 1). On the left of the red dashed line, the top DBC and volumes of insulating gel are hidden. Notably, regarding the mesh, special attention was given to achieving consistency in discretization – especially in the proximity of triple points – to obtain precise assessments of EF_{\max} .

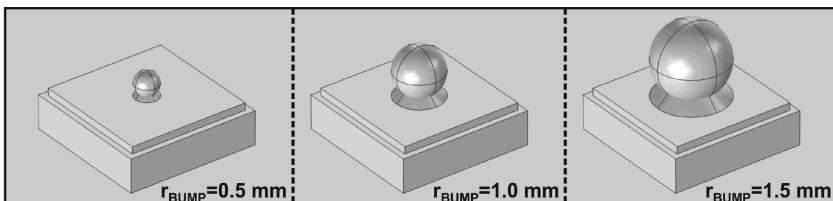


Fig. 5. Magnification of the device region highlighting the position of the bump connecting the source at various r_{BUMP} values.

The maximum EF (EF_{\max}) in the PMs determined with simulations is reported in Fig. 7 along with the analytical EF_{avg} evaluated with (1); it can be inferred that, while EF_{avg} increases with smaller bumps, EF_{\max} unexpectedly *decreases*, as the regions in the

surroundings of the die where triple points are located turn out to be more evenly biased with smaller bumps. FEM simulations were also employed to accurately quantify the parasitic capacitance due to interfacing DBCs (C_{DSC}) at different r_{BUMP} . C_{DSC} values turned out to fall in the range of ~ 86 pF to ~ 103 pF for the cases of $r_{BUMP} = 1.5$ mm and $r_{BUMP} = 0.5$ mm, respectively.

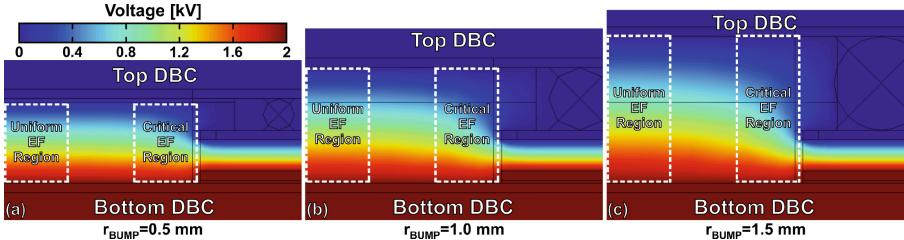


Fig. 6. FEM simulation results showing the voltage distribution in the DSC PMs at different r_{BUMP} values.

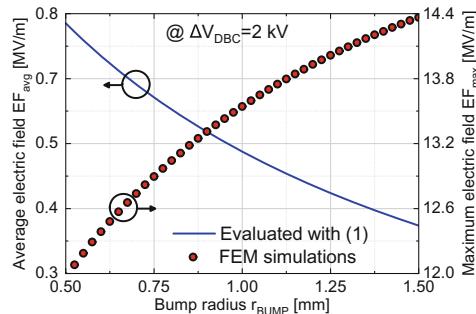


Fig. 7. Electric fields at $\Delta V_{DBC} = 2$ kV vs. r_{BUMP} . EF_{avg} (solid blue line) is associated to the left y-axis and was evaluated through (1). EF_{max} values (red dots) were extracted through 41 FEM simulations and are linked to the right y-axis.

3 SPICE Simulations

A SPICE simulation campaign in the popular commercially-available OrCAD PSPICE [13] was conducted to evaluate the electrical ruggedness of the PMs under investigation. The circuit depicted in Fig. 8 was employed to simulate a turn-off event, causing a fast and significant variation in the drain voltage (V_D). The value of the parasitic capacitance C_{DSC} was appropriately changed according to r_{BUMP} considering the data extracted in FEM simulations; the three cases 0.5, 1.0, and 1.5 mm were chosen. The MOSFET model was derived following the approach outlined in [14] and represents a SiC-based device withstanding $2 +$ kV. Additionally, the simulation includes the model of a fast recovery SiC-based Schottky diode. During the simulations, the gate voltage (V_G) switched from 20 V to -10 V at $t = 10 \mu s$. Results shown a V_D rise from ~ 0 V to $V_{DD} = 2.2$ kV, with oscillations due to presence of the inductor L_{DD} .

As a first remarkable result, regardless of the bump size, the effect of C_{DSC} is not significant; reasonably, the VDMOS internal parasitic capacitances are bigger than the one introduced by the PM assembly, making the circuit behavior insensitive with C_{DSC} . To calculate the EF within the gel, the waveforms of $\Delta V_{DBC}(t)$ in the three cases were extracted and scaled. Results are shown in Figs. 9 and 10.

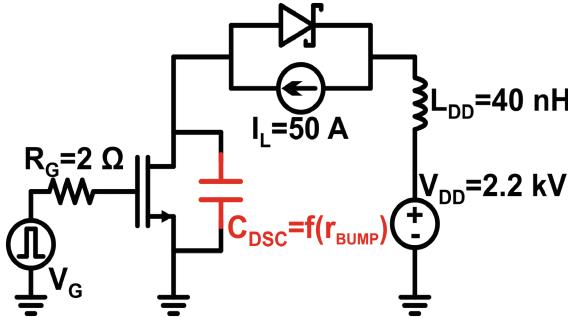


Fig. 8. Schematic of the circuit drawn in SPICE to simulate the turn off event.

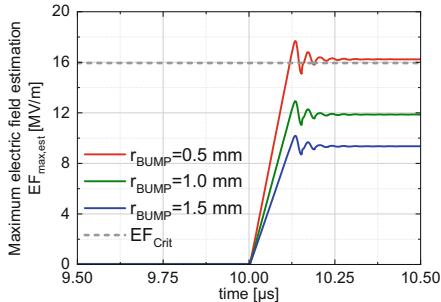


Fig. 9. Maximum electric field estimation vs. time during the turn-off evolution (at 10 μ s) for different r_{BUMP} values. The critical electric field (EF_{crit}) at 15.9 MV/m is also shown (dashed gray line). Curves for small, medium, and big bumps are drawn with red, green, and blue solid lines, respectively.

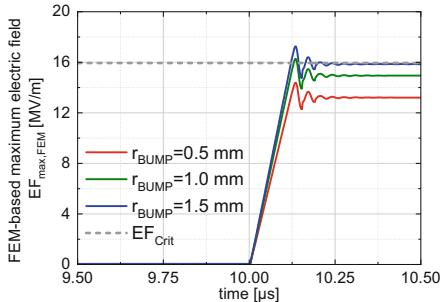


Fig. 10. FEM-based maximum electric field vs. time during the turn-off evolution (at 10 μ s) for different r_{BUMP} values. The critical electric field (EF_{crit}) at 15.9 MV/m is also shown (dashed gray line). Curves for small, medium, and big bumps are drawn with red, green, and blue solid lines, respectively.

DSC PMs designers typically adopt a conservative strategy by estimating a maximum EF ($EF_{max,est}$) as 20 times the value calculated using Eq. (1). Therefore, they would obtain results shown in Fig. 9. In the light of these outcomes, the PM with small bumps ($r_{BUMP} = 0.5$ mm) would be discarded for this application since the related $EF_{max,est}$ overcomes the dielectric breakdown of the gel. Nevertheless, following this design strategy, medium-sized and large bumps would ensure the integrity of the PM and would be adopted. The results from simulations considering the more realistic FEM-based maximum EF ($EF_{max,FEM}$) are shown in Fig. 10, revealing significantly different outcomes. In this more realistic scenario, SPICE $\Delta V_{DBC}(t)$ waveforms were scaled with results in Fig. 7 (right y-axis). With respect to what shown Fig. 9, this finding reveals a distinctly different

trend: DSC PMs featuring small bumps are well within the DSC PM safe operating area. Due to voltage oscillation, the adoption of medium-sized bumps may potentially lead to PM damage, and the use of large bumps must be strongly discouraged.

4 Conclusion

In this contribution, the electrical ruggedness of double-sided cooled (DSC) power modules (PMs) has been investigated by varying the distance between interfacing direct bonded copper (DBC) substrates. Detailed finite element method (FEM) simulations have been performed in the COMSOL Multiphysics environment. The findings have confirmed that PMs with smaller spacing between DBCs (achieved by using smaller bumps) benefit from a reduction in the maximum electric field, thereby expanding the safe operating area. In addition to the FEM investigation, SPICE simulations were employed to evaluate the electrical ruggedness of PMs in practical circuit applications. A comparative analysis between the conventional design strategies and the actual performance of PMs with different bump sizes was conducted. Specifically, during a switching event, the assembly with smaller spacing between DBCs proved to be more reliable, despite general reluctance of designers to adopt this configuration.

In summary, simulations highlighted the significant risks associated with relying on the intuitive, yet overly simplistic, 1-D estimation of the PM electric field. This study underscores the importance of adopting more accurate and realistic modeling techniques to ensure the reliability and performance of DSC PMs.

Acknowledgements. This study was carried out within the NEST - Network 4 Energy Sustainable Transition (D.D. 1243 02/08/2022, PE00000021) and received funding under the National Recovery and Resilience Plan (NRRP), Mission 4 Component 2 Investment 1.3, funded by the European Union - NextGenerationEU.

References

1. Abu-Rub, H., Malinowski, M., Al-Haddad, K.: Power electronics for renewable energy systems, transportation and industrial applications. John Wiley & Sons (2014)
2. Yamada, T., et al.: Next generation power module. In: IEEE Proceedings of the 6th International Symposium on Power Semiconductor Devices and Ics, pp. 3–8 (1994)
3. Li, H., Munk-Nielsen, S., Bęczkowski, S., Wang, X.: A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules. *IEEE Trans. Power Electron.* **31**(12), 8042–8045 (2016)
4. Ghimire, P., de Vega, A.R., Bęczkowski, S., Rannestad, B., Munk-Nielsen, S., Thogersen, P.: Improving power converter reliability: Online monitoring of high-power IGBT modules. *IEEE Ind. Electron. Mag.* **8**(3), 40–50 (2014)
5. Mandray, S., Guichon, J.M., Schanen, J.L., Guyennet, M.M., Dienot, J.M.: Electromagnetic considerations for designing double-sided power modules. *IEEE Trans. Ind. Appl.* **45**(2), 871–879 (2009)
6. Li, B., Yang, X., Wang, K., Zhu, H., Wang, L., Chen, W.: A compact double-sided cooling 650V/30A GaN power module with low parasitic parameters. *IEEE Trans. Power Electron.* **37**(1), 426–439 (2021)

7. Liu, M., Coppola, A., Alvi, M., Anwar, M.: Comprehensive review and state of development of double-sided cooled package technology for automotive power modules. *IEEE Open Journal of Power Electronics* **3**, 271–289 (2022)
8. Datasheet of SylgardTM 567 silicon encapsulant online available at: <https://ostecmaterials.ru/upload/iblock/59a/59a09262db348aec70c3591e26cc139c.pdf>
9. Lebey, T., et al.: Partial discharges phenomenon in high voltage power modules. *IEEE Transactions on Dielectrics and Electrical Insulation* **13**(4), 810–819 (2006). Shammas, N.Y.: Present problems of power module packaging technology. *Microelectronics Reliability* **43**(4), 519–527 (2003)
10. Scognamillo, C., Catalano, A.P., Lasserre, P., Duchesne, C., d'Alessandro, V., Castellazzi, A.: Combined experimental-FEM investigation of electrical ruggedness in double-sided cooled power modules. *Microelectron. Reliab.* **114**, 113742 (2020)
11. Li, J., Castellazzi, A., Dai, T., Corfield, M., Solomon, A.K., Johnson, C.M.: Built-in reliability design of highly integrated solid-state power switches with metal bump interconnects. *IEEE Trans. Power Electron.* **30**(5), 2587–2600 (2014)
12. COMSOL Multiphysics, User's Guide, Release 5.3A, (2018)
13. PSPICE User's Manual, Cadence OrCAD 16.5 (2011). <https://www.orcad.com>. Accessed on 25 May 2024
14. d'Alessandro, V., Codecasa, L., Catalano, A.P., Scognamillo, C.: Circuit-based electrothermal simulation of multicellular SiC power MOSFETs using FANTASTIC. *Energies* **13**(17), 4563 (2020)



Out-of-SOA Performance of 3.3 kV SiC MOSFETs: Comparison Between Planar and Quasi-Planar Trench

C. Scognamillo¹, A. Borghese¹(✉), K. Melnyk⁴, I. Nistor², V. d'Alessandro¹, M. Boccarossa¹, V. Terracciano¹, M. Riccio¹, A. P. Catalano¹, G. Breglio¹, N. Lophitis^{3,5}, M. Antoniou⁴, M. Rahimo², A. Irace¹, and L. Maresca¹

¹ Department of Electrical Engineering and Information Technologies,
University of Federico II, 80125 Naples, Italy

alessandro.borghese@unina.it

² mQSem AG, CH-6300 Zug, Switzerland

³ Faculty of Engineering, Nottingham NG7 2RD, UK

⁴ University of Warwick, Coventry, England

⁵ Faculty of Engineering and Technology, Cyprus University of Technology,
Limassol, Cyprus

Abstract. Multidimensional device structures can improve the typical performance trade-off of semiconductor power transistors. In this paper, the on-state, reverse, and short-circuit performance of a SiC quasi-planar trench MOSFET are compared to those of a classical planar device through advanced 3-D TCAD simulations.

Keywords: short circuit · SiC MOSFET · TCAD simulation

1 Introduction

Solid-state power transistors, including Insulated Gate Bipolar Transistors (IGBTs) and power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), are designed with a multicellular architecture. This structure involves the parallel connection of multiple elementary cells to achieve the desired current handling capability. Over the past few decades, Silicon (Si) planar power devices have been refined to a degree where their performance is nearing the theoretical limits defined by one-dimensional figures of merit [1].

The development and release of advanced devices featuring innovative cell architectures, such as the charge-coupled [2] and super-junction [3] MOSFETs, have significantly extended these performance boundaries and brought new margins for improvement [4, 5]. A similar development cycle has been observed for silicon carbide (SiC), where, after the standard planar MOSFET architecture, more advanced structures have emerged: some recalling the ones already seen in Si, such as the FinFET [6], others devised to tackle specific problems of SiC, such as the SiC gate-all-around MOSFETs [7, 8].

While the aforementioned advancements are mainly targeted at improving within-SOA performance, others aim at enhancing the out-of-SOA capability of the device [9–11]. In particular, the short-circuit (SC) robustness is still an area that requires improvement [12, 13]. Moreover, the short-channel effect has shown to be more pronounced in SiC MOSFETs [14, 15].

Although it is presumed that the short-channel effect negatively impacts SC robustness, their impact has never been thoroughly investigated in the scientific literature. The objective of this paper is to introduce a new SiC MOSFET elementary-cell structure that enhances the SC capability by mitigating the short-channel effect.

As shown in the singular point source MOS (see [16–18]), the introduction of the trench in the JFET region of SiC power MOSFETs strongly reduces the channel-shortening effect. Here, for the first time, a quasi-planar trench (QPT) power MOSFET based on [17] and [18] is conceived and its main advantages with respect to planar devices are reported; more specifically, (i) on-resistance R_{on} , (ii) saturation current I_{Dsat} , (iii) breakdown voltage BV , and (iv) SC capability are determined through highly-detailed 3-D TCAD simulations, where the cell half-pitch and the trench depth are varied.

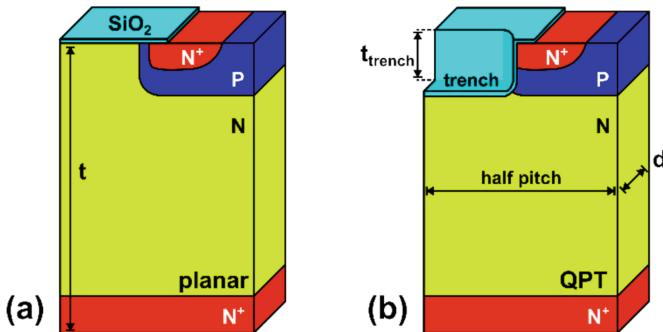


Fig. 1. Schematic representation (not to scale) of (a) planar and (b) QPT 3.3 kV SiC MOSFET elementary cell.

2 Methodology and Results

3-D replicas of the two structures schematically shown in Fig. 1 were built in Sentaurus TCAD: differently from the planar device, the QPT 50 nm-thin gate silicon dioxide (SiO_2) covers both the planar region and the trench walls, and the gate contact extends all over the SiO_2 top surface. For both elementary cells: $t = 30 \mu\text{m}$, $d = 1 \mu\text{m}$. Moreover, they have a $0.5 \mu\text{m}$ -long channel, while the QPT trench reaches the Source diffusion region (N^+). The overall device is assumed to have an area of 0.25 cm^2 . Half pitch and trench depth were selected as geometrical parameters and their impact on R_{on} , I_{Dsat} , and BV was quantified. Half pitch was varied in the range $3\text{--}9 \mu\text{m}$, by keeping the total area constant, while the trench depth spanned the range $0.5\text{--}1.1 \mu\text{m}$.

QPT devices benefit from a longer effective channel – it being made of (i) the inversion layer created at the SiO_2 -body interface and (ii) the accumulation layer at

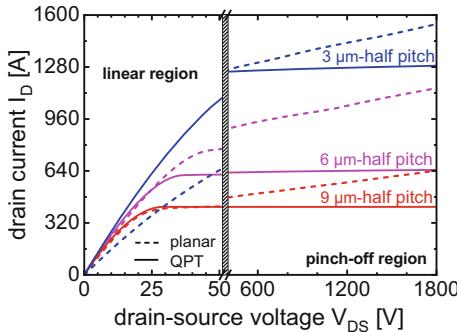


Fig. 2. 3-D TCAD simulations: output characteristics of planar (dashed lines) and QPT (solid lines) design having a 3, 6, and 9 μm -half pitch.

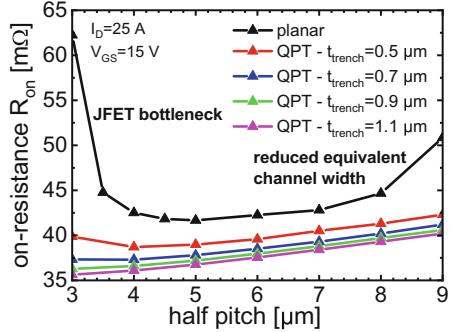


Fig. 3. 3-D TCAD simulations: $I_D = 25 A$ and $V_{GS} = 15 V$ on-resistance R_{on} vs. half pitch in the planar and QPT MOSFET cells at a given total area of 0.25 cm^2 .

Table 1. 3-D TCAD simulations: breakdown voltage (BV) as a function of half pitch in the MOSFET cells under investigation.

	half pitch [μm]	BV [V]
Planar	3	4382
	6	4217
	9	4146
QPT	3	4440
	6	4448
	9	4449

the SiO_2 -drift interface in the JFET region – which confirms the abovementioned *suppression of the short-channel effect*. Figure 2 shows that, in the pinch-off region, QPT MOSFETs enjoy a lower I_D vs. V_{DS} slope; if the trench is too shallow, a contribution of the JFET region arises. Compared with the reference planar design, the QPT structure offers a lower R_{on} in the investigated half pitch range regardless of the depth of the trench (Fig. 3). During conduction, the presence of inversion and accumulation layer encourages a laminar I_D flow in the QPT structure concentrated on the back of the cell.

The breakdown voltage BV of QPT devices turns out to be higher than that of the planar counterparts (Table 1). Figure 4 shows the equipotential lines near the body-epilayer junction, where the maximum electric field E_{max} is observed in the standard cell [19]. QPT cells suffer from higher electric field in the SiO_2 w.r.t. the planar design; to mitigate this drawback, a trench P shield (10^{17} cm^{-3}) was put underneath the trench (see Table 2).

The experimental parameter evaluating the SC capability is the SC withstand time [13]. This parameter represents the maximum duration for which the device can sustain

SC stress without exhibiting failure or degradation. However, transient TCAD simulations of elementary cells cannot accurately evaluate this parameter, as they neglect several critical failure mechanisms, such as mechanical stress and electromigration. It has been established that one of the primary catastrophic failure mechanisms for SiC MOSFETs during SC events is thermal runaway. Thermal runaway failure is associated with a rapid increase in internal temperature [13]. Once the temperature exceeds a critical threshold, the number of thermally-generated electron-hole pairs in the body/drift space charge region becomes significant, leading to a drain leakage current. This leakage current is indicated by a change in the slope of the drain current waveform (marked by red points in Fig. 5). The thermal generation rate of carriers surpasses the rate of heat dissipation, resulting in a self-sustained electrothermal instability that ultimately destroys the device. Consequently, an alternative indicator used in simulations is the time after which the drain current begins to increase.

Table 2. 3-D TCAD simulations: $\text{SiO}_2 E_{\text{max}}$, BV, and R_{on} in 6 μm -half pitch, trench dept $t_{\text{trench}} = 1.1 \mu\text{m}$ structures.

	$\text{SiO}_2 E_{\text{max}} @ V_{\text{DS}} = 3.3 \text{ kV}$	BV [V]	$R_{\text{on}} [\text{m}\Omega]$
Planar	4.58 MV/m	4217	42.3
QPT w/o P shield	10.38 MV/m (+127%)	4448	37.5 (-11.35%)
QPT w/ P shield	9.74 MV/m (+112%)	4432	39.3 (-7.09%)

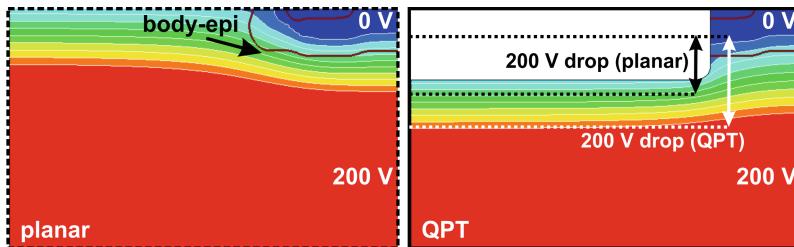


Fig. 4. 3-D TCAD simulations: $V_{\text{DS}} = 3300 \text{ V}$ and $V_{\text{GS}} = 0 \text{ V}$ electrostatic potential lines in the planar 6 μm cell (left) and the QPT one (right).

The almost flat saturation region of the $I_{\text{D}} - V_{\text{DS}}$ curves leads to an improved SC capability. As demonstrated in Fig. 5 and in [11], the SC capability rises as the saturation drain current I_{Dsat} reduces. In planar designs, a lower I_{Dsat} is obtained by increasing the half pitch, in turn worsening R_{on} and BV. On the other hand, QPTs relax this tradeoff by virtue of the reduced/suppressed short channel effect; therefore, they can offer the same SC capability (i.e., the same I_{Dsat}) with better R_{on} and BV.

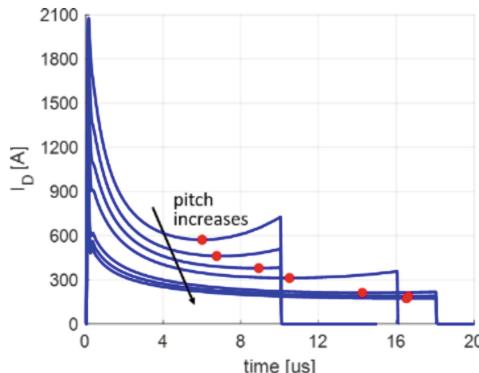


Fig. 5. 2-D TCAD simulations: I_D vs. time during short circuit @ $V_{DS} = 2200$ V in planar cells. Red points indicate the onset of the electrothermal instability.

3 Conclusion

In this work, the performance of a novel type of elementary cell for SiC MOSFETs (QPT) has been compared to those of the standard planar cell through highly-detailed 3-D TCAD simulations of a 3.3 kV SiC MOSFET. From the outcomes it is inferred that the QPT-based SiC power MOSFET mitigates the short-channel effect by introducing a trench in the JFET region. Moreover, a reduction in the R_{on} of ~11% is observed, along with the simultaneous improvement of BV and SC capability. These properties are critical for devices in high-performance high-reliability converters and drives such as in transport and energy domains.

Acknowledgments. The AdvanSiC project has received funding from the European Union's Horizon Europe programme under grant agreement No 101075709. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union. Neither the European Union nor the granting authority can be held responsible for them.

References

1. Zhang, Y., Udrea, F., Wang, H.: Multidimensional device architectures for efficient power electronics. *Nat. Electron.* **5**, 723–734 (2022). <https://doi.org/10.1038/s41928-022-00860-5>
2. Baliga, B.J.: Advanced Power MOSFET Concepts. Springer, US, Boston, MA. (2010). <https://doi.org/10.1007/978-1-4419-5917-1>
3. Fujihira, T.: Theory of semiconductor superjunction devices. *Jpn. J. Appl. Phys.* **36**, 6254 (1997). <https://doi.org/10.1143/JJAP.36.6254>
4. Saito, W.: Comparison of theoretical limits between superjunction and field plate structures. In: 2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD). Presented at the 2013 25th International Symposium on Power Semiconductor Devices & IC's (ISPSD), pp. 241–244. IEEE, Kanazawa (2013). <https://doi.org/10.1109/ISPSD.2013.6694461>

5. Kang, H., Udrea, F.: True material limit of power devices—applied to 2-D superjunction MOSFET. *IEEE Trans. Electron Devices* **65**, 1432–1439 (2018). <https://doi.org/10.1109/TED.2018.2808181>
6. Udrea, F., et al.: The FinFET effect in Silicon Carbide MOSFETs. In: 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD). Presented at the 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 75–78. IEEE, Nagoya, Japan (2021). <https://doi.org/10.23919/ISPSD50666.2021.9452282>
7. Yang, D., Wirths, S., Knoll, L., Han, Y., Buca, D.M., Zhao, Q.T.: Enhanced device performance with vertical SiC gate-all-around nanowire power MOSFETs. *KEM* **945**, 77–82 (2023). <https://doi.org/10.4028/p-0ta22r>
8. Maresca, L., et al.: SiC GAA MOSFET concept for high power electronics performance evaluation through advanced TCAD simulations. *KEM* (2024)
9. Agarwal, A., Baliga, B.J.: Performance Enhancement of 2.3 kV 4H-SiC Planar-Gate MOSFETs Using Reduced Gate Oxide Thickness. *IEEE Trans. Electron Devices* **68**, 5029–5033 (2021). <https://doi.org/10.1109/TED.2021.3102473>
10. Boccarossa, M., et al.: Short-Circuit Rugged 1.2 kV SiC MOSFET with a Non-Linear Dielectric Gate Stack. In: 2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD). Presented at the 2023 35th International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 354–357. IEEE, Hong Kong (2023). <https://doi.org/10.1109/ISPSD57135.2023.10147604>
11. Yin, S., Cao, W., Hu, X., Ge, X., Liu, D.: A novel super-junction DT-MOS with floating p regions to improve short-circuit ruggedness. *Micromachines* **14**, 1962 (2023). <https://doi.org/10.3390/mi14101962>
12. Romano, G., et al.: A comprehensive study of short-circuit ruggedness of silicon carbide power MOSFETs. *IEEE J. Emerg. Sel. Topics Power Electron.* **4**, 978–987 (2016). <https://doi.org/10.1109/JESTPE.2016.2563220>
13. Borghese, A., et al.: Short-circuit and Avalanche Robustness of SiC Power MOSFETs for Aerospace Power Converters. In: 2023 IEEE Aerospace Conference. Presented at the 2023 IEEE Aerospace Conference, pp. 1–8. IEEE, Big Sky, MT, USA (2023). <https://doi.org/10.1109/AERO55745.2023.10115580>
14. Noborio, M., Kanzaki, Y., Suda, J., Kimoto, T.: Experimental and theoretical investigations on short-channel effects in 4H-SiC MOSFETs. *IEEE Trans. Electron Devices* **52**, 1954–1962 (2005). <https://doi.org/10.1109/TED.2005.854269>
15. Tachiki, K., Ono, T., Kobayashi, T., Kimoto, T.: Short-channel effects in SiC MOSFETs based on analyses of saturation drain current. *IEEE Trans. Electron Devices* **68**, 1382–1384 (2021). <https://doi.org/10.1109/TED.2021.3053518>
16. Rahimo, M.T.A., Nistor, I., Green, D.: Singular Point Source MOS Cell Concept (S-MOS) Implemented on a Narrow Mesa Trench IGBT. In: 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD). Presented at the 2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD), pp. 27–30. IEEE, Nagoya, Japan (2021). <https://doi.org/10.23919/ISPSD50666.2021.9452228>
17. Rahimo, M.T., Nistor, I., Green, D.: Advanced 1200V SiC MOSFET concept based on singular point source MOS (S-MOS) technology. *MSF* **1062**, 539–543 (2022). <https://doi.org/10.4028/p-u88313>
18. Rahimo, M.T., Nistor, I., Green, D.: Suppression of short channel effects for a SiC MOSFET based on the S-MOS cell concept. *KEM* **945**, 83–89 (2023). <https://doi.org/10.4028/p-g4w5h5>
19. Kimoto, T.: High-voltage SiC power devices for improved energy efficiency. *Proc. Jpn. Acad. Ser. B* **98**, 161–189 (2022). <https://doi.org/10.2183/pjab.98.011>



An Ultra-Fast Overcurrent Protection Circuit Based on SMD Shunt Resistors for Wide Band-Gap Devices

Emanuele Martano^(✉) ID, Giovanni Busatto ID, Annunziata Sanseverino ID,
Simone Palazzo ID, and Francesco Velardi ID

University of Cassino and Southern Lazio, 03043 Cassino, FR, Italy
emanuele.martano@unicas.it

Abstract. Since a sudden increase in drain current is a clear indicator of a short-circuit in a power device, SC protection systems based on a direct current measurement are often the most straightforward and efficacious solutions. However, when dealing with wide band-gap (WBG) technologies, the limitations of current sensing techniques pose a significant challenge to the design of short circuit (SC) protection, especially for gallium nitride (GaN) power devices. Specifically, in the case of GaN, protection systems based on principles other than current sensing remain a viable option, but the effectiveness of these protection systems is limited by the need for complex circuitry to meet the stringent intervention time requirements. This paper presents a straightforward and fast overcurrent protection (OCP) system based on direct current measurement applied to 650 V E-mode gallium nitride (GaN) high electron mobility transistors (HEMTs). The monitoring of the current is achieved through the use of a surface-mount device (SMD) shunt resistor and a basic passive network. A simple logic mechanism promptly identifies when the current exceeds the predefined overcurrent limit, thereby enabling the automatic shutdown of the device under test (DUT). As it is based on current monitoring, this system can protect the device from both overcurrent and SC conditions. Consequently, there is no longer a need to build two different systems to perform these functions.

Keywords: GaN · Wide band-gap · short-circuit · overcurrent · protection

1 Introduction

Wide band-gap semiconductors, such as silicon carbide (SiC) and GaN, enable the fabrication of power devices with improved electrical properties compared to conventional silicon (Si) devices. However, the fast switching phases of these emerging devices present a number of technical challenges. One of these is the current measurement limitations, which are currently constrained by the need for compactness, low insertion impedance and high bandwidth required by the newly designed converters. This aspect is particularly pronounced in the case of GaN devices, where switching speeds are significantly

higher than those of other technologies. In addition, the GaN material exhibits a remarkable sensitivity to short circuits, making it highly susceptible to failure when the drain voltage exceeds 300 V and the gate voltage exceeds 5 V [1, 2]. Consequently, to maintain the efficiency and resilience of the GaN device, it is essential to implement robust protection systems that can intervene within a few hundred nanoseconds. Given the challenges inherent in measuring current, the desaturation-based system has emerged as a dominant technology among the various solutions proposed in the literature. This system employs the rise in drain-source voltage to detect a short circuit [3, 4]. While the response dynamics of this technique are impressive, the high switching speed of GaN HEMTs introduces concerns regarding interference, stemming from the high dv/dt and di/dt . This can lead to circuit designs that are complex and costly. An alternative solution based on a direct measurement of the current was proposed in [5]. In this case, the current is monitored using a shunt resistor and a passive network consisting of a resistor and inductor, which is used to compensate for the leakage inductance of the measuring shunt. The compactness, low cost, and incredible intervention speed (68 ns) of the preceding solutions were the prerequisites for the development of the circuit proposed in this paper, which is configured as a new, more compact, and potentially faster version of what shown in [5].

2 The OCP System

Figure 1 shows a simplified electrical diagram of the test circuit used to validate the first version of the OCP, as detailed in [5]. In this diagram, the SMD shunt is depicted as a series of a resistor and an inductor, denoted as R_S and L_S respectively. It should be noted that, according to [6], the voltage V_{sense} is proportional, even during transients, to the current I_d as shown in the following relationship:

$$V_{sense} = \frac{R_S}{R_S + R_{1\Omega}} R_{1\Omega} I_d \quad (1)$$

The above equation allows the computation of the intervention threshold (V_{ref}) of the protection circuit considering the limit set for the drain current. This value can be used as a reference to the comparator input to compare with V_{sense} and activate the protection at the occurrence of an overcurrent. To create overcurrent conditions, a Type I short circuit test can be performed on the circuit shown in Fig. 1. In this case, the Q1 transistor must be turned on before the Q2 (DUT) transistor and must remain on for the entire duration of the Q2 conduction phase [7]. The circuit is designed to deactivate the driver of the protected device when the sense signal, represented by V_{sense} , indicates a current that exceeds the normal operating limit. To prevent the DUT driver from being enabled until the system is reset, it is crucial to have a latch circuit on the output of the comparator. Otherwise, when the V_{sense} voltage returns below the V_{ref} threshold, the gate driver is re-enabled, causing the DUT to turn on again in a process that involves continuous on/off cycling of the DUT.

Finally, in order to guarantee the isolation of the gate driver, the digital signal on the output of the detection system is also isolated.

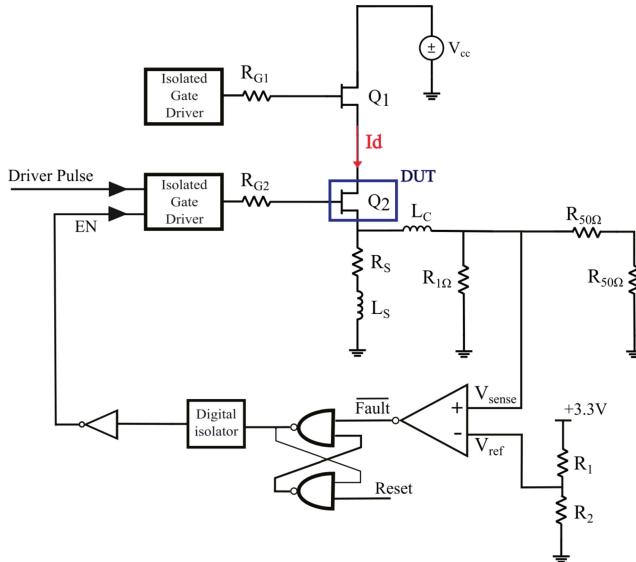


Fig. 1. Simplified diagram of the test circuit implementing the first version of the OCP

Despite the promising results demonstrated in [5], this system, which intervenes by disabling the gate driver, does not guarantee a smooth shutdown of the DUT. Consequently, it is a protection system that becomes less safe the greater the stray inductance associated with the loop formed by the decoupling and the bridge leg of the power devices. In the case of a wide bandgap (WBG) converter, where fast transients amplify the effect of parasitic inductance in the circuit, this inductance has the potential to produce a high voltage spike on the DC link that could damage the power devices if the DUT is shut down too quickly under high current conditions.

In response to the necessity for a gradual shutdown, an enhanced version of the OCP was developed. The new scheme, illustrated in Fig. 2, adheres to the same fundamental principles as its predecessor but presents a more compact and potentially faster intervention system.

In addition to a smoother switch-off, the new project also proposes the implementation of an RC network instead of an RL one to compensate for the effect of the shunt stray inductance [8]. The use of a capacitor instead of an inductor offers advantages such as better integration, greater market availability and lower cost.

As in the previous version, it is possible to establish a purely resistive relationship between the current I_d and the voltage V_{sense} by selecting the correct parameters for the compensation network (R_C and C_C). In this case, this relationship is as follows:

$$V_{sense} = R_S I_d \quad (2)$$

Once more, this relationship permits the estimation of the reference value V_{ref} for the intervention of the protection system.

During a SC or an overcurrent event, when the current overcomes the set limit, the comparator generates a fault signal that activates the MOSFET M1. Contrarily to what

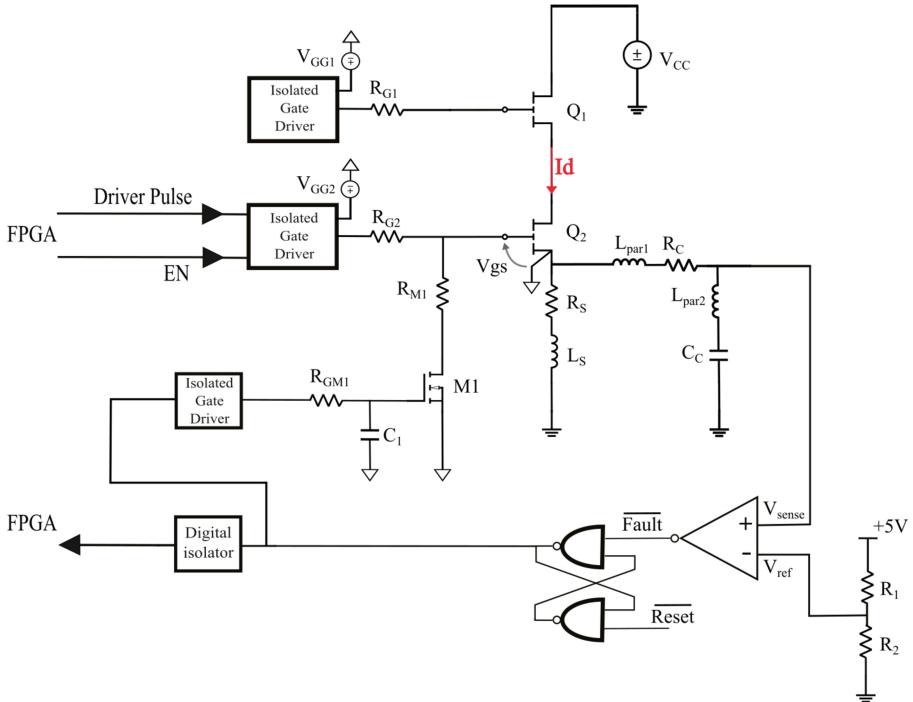


Fig. 2. Simplified diagram of the test circuit implementing the second version of the OCP

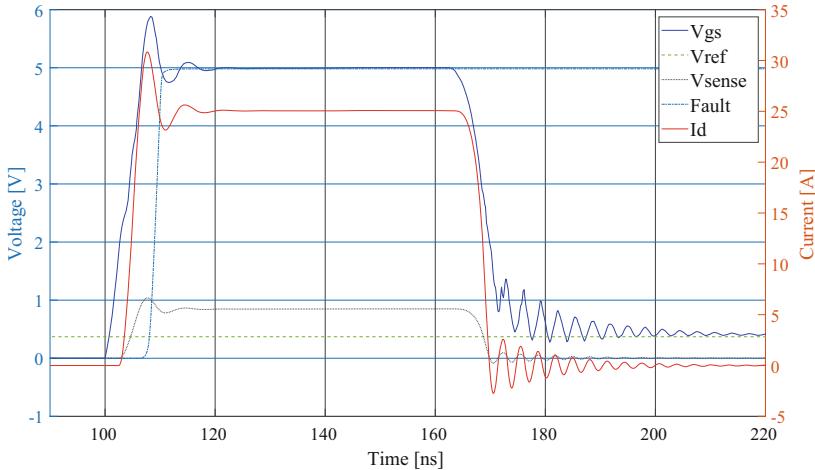
happens in the protection circuit in [5], the activation of M_1 allows the gate voltage to gradually decrease taking advantages of the turn-on transient of the MOSFET, whose rise time can be adjusted by regulating R_{GM1} and C_1 . The presence of resistor R_{M1} allows for a two-stage turn-off process, whereby the initial stage is a soft turn-off and the subsequent stage is a hard turn-off. This specific intervention method serves to further reduce the DC link voltage spike. In particular, when M_1 is activated to protect the devices, the voltage supplied by the DUT's gate driver is divided between the two resistors R_{G2} and R_{M1} . This results in a reduction of the gate-to-source voltage on the DUT, which is then completely turned off disabling its gate driver with the FPGA. To achieve a single-step shutdown, it is necessary to short-circuit the resistor R_{M1} to bring the DUT's gate-to-source voltage directly below its threshold. In this scenario, to prevent the R_{G2} resistor from overheating, the fault signal is still sent to the FPGA to disable the DUT driver after an adjustable delay.

2.1 Simulation Results

The validity of the proposed circuit was verified by reproducing the circuit shown in Fig. 2 in the LTspice environment. The simulation was performed with two 8A - 650 V (Table 1) GaN HEMTs using the model provided by the manufacturer. The gate resistors were both set to $10\ \Omega$ with R_{M1} short-circuited and C_1 set to $50\ pF$. The I_d current limit was $14\ A$, while the V_{GG2} and V_{CC} values were $5\ V$ and $50\ V$, respectively. The remaining circuit

Table 1. Simulated components and parameters

TON	R _S	L _S	C _C	R _C	Comp. & Latch	M1 driver	R _{GMI}	M1
400 ns	33 mΩ	2 nH	300 pF	200 Ω	LT1711	MAX22702	350 Ω	NX3008NBK

**Fig. 3.** Simulated Waveforms

parameters, with the exception of the leakage inductances L_{par1} and L_{par2} , which were not considered in this simulation, are presented in Table 1. The simulated waveforms are shown in Fig. 3. The total duration of the simulated intervention is 64 ns, which represents a significant improvement over [5], since the proposed new version, for a comparable intervention time, allows a more gradual deactivation of the device under test (DUT) after the overcurrent event. As already stated, this helps to limit the peak DC link voltage, which is mainly caused by the stray inductance of the loop formed by the decoupling capacitors and the phase leg of power devices.

However, as pointed out in [8], capacitive compensation of L_S can induce problems caused by resonance between the compensation capacitor C_C and the parasitic inductance of the branch comprising it ($L_{par1} + L_{par2}$). For such an application it is not necessary to use a matched 50 Ω line because the comparator can be positioned close to the shunt and there is no need to feed the signal to a 50 Ω oscilloscope input as it was requested in [8]. So it gives the freedom to choose high values of R_C and low values of C_C , resulting in high resonance frequency and damping factor. To investigate this phenomenon, the above simulation was reproduced with and without the stray inductance of the measurement branch. The resulting data was then compared and are shown in Fig. 4. The outcomes indicate that in the worst scenario described in reference [8], where the values of L_{par1} and L_{par2} have been set to 10 nH and 200 pH, respectively, there is no discernible effect on either the drain current or the intervention time.

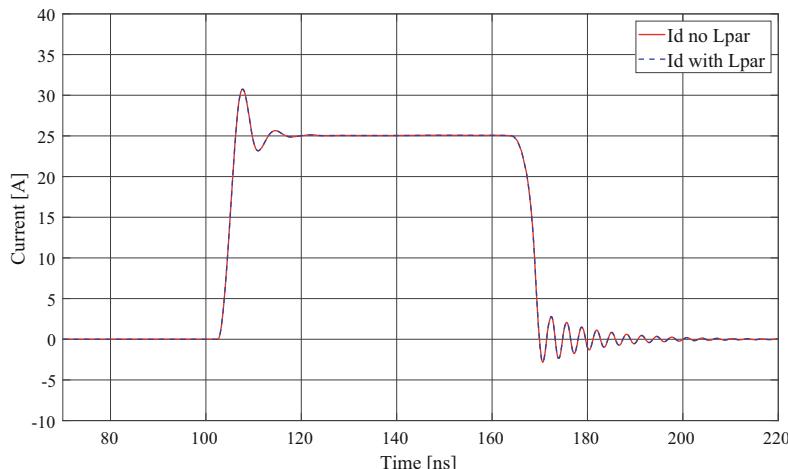


Fig. 4. Comparison of drain currents in the case with and without measurement branch leakage inductance

3 Conclusions

The present article introduces a novel approach to overcurrent protection for wide-bandgap devices based on the monitoring of drain current through a passive network. The network consists of three components: an SMD shunt, an SMD capacitor and an SMD resistor, which facilitate the system's practicality and suitability for the compact requirements of WBG converters. Moreover, their lower cost makes the current monitoring system a more economical alternative to commonly used methods such as the Rogowski coil and coaxial shunt. The efficacy of the proposed overcurrent protection has been demonstrated through simulation, where the intervention times are so rapid that they permit the system to be adapted to accommodate the turn-off di/dt of the DUT in a manner compatible with the diverse applications.

References

1. Abbate, C., et al.: Failure analysis of 650 V enhancement mode GaN HEMT after short circuit tests. *Microelectron. Reliab.* **88–90**, 677–683 (2018)
2. Li, H., et al.: Robustness of 650-V Enhancement-Mode GaN HEMTs Under Various Short-Circuit Conditions. *IEEE Transactions on Industry Applications* **55**(2), 1807–1816 (2019)
3. Hou, R., Lu, J., Quan, Z., Li, Y.W.: A simple desaturation-based protection circuit for GaN HEMT with ultrafast response. *IEEE Trans. Power Electron.* **36**(6), 6978–6987 (2021)
4. Wu, J., Meng, W., Zhang, F., Dong, G., Shu, J.: A short-circuit protection circuit with strong noise immunity for GaN HEMTs. *IEEE Trans. on Power Electron.* **36**(2) (2021)
5. Martano, E., et al.: Simple and Low Cost Overcurrent Protection System Based on Commercial Shunt for Wide-Bandgap Devices. accepted to PCIM Europe 2024
6. Abbate, C., et al.: An accurate switching current measurement based on resistive shunt applied to short circuit GaN HEMT characterization. *Appl. Sci.* **11**, 9138 (2021)

7. Abbate, C., Busatto, G., Sanseverino, A., Tedesco, D., Velardi, F.: Experimental study of the instabilities observed in 650 V enhancement mode GaN HEMT during short circuit. *Microelectron. Reliab.* **76–77**, 314–320 (2017)
8. Meissner, M., Schmitz, J., Weiss, F., Bernet, S.: Current measurement of GaN power devices using a frequency compensated SMD shunt. PCIM Europe 2019; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, pp. 1–8 (2019)



Performance Analysis of a Custom DC-DC Buck Converter for Smart Plug Applications in Nanogrids

Danilo Santoro^(✉) ID, Armel Asongu Nkembi ID, Paolo Cova ID,
and Nicola Delmonte ID

University of Parma, Parma, Italy
danilo.santoro@unipr.it

Abstract. To improve power management systems in micro- and nanogrid applications, it is crucial to thoroughly evaluate the efficiency, output ripple, and operating frequency of DC-DC converters. This paper presents a detailed investigation of these critical parameters for custom laboratory-built DC-DC buck converters with Gallium Nitride (GaN) transistors. The study analyses and compares measurements to assess the converter's performance under varying load conditions. Efficiency is examined by varying input voltages and load levels to unveil the converter's operational boundaries. The investigation extends to the characterization of the output ripple. Furthermore, the impact of working frequency on both characteristics and design requirements is explored, providing insights into optimal frequency selection. A comparative analysis with industry-standard benchmarks underscores the converter's strengths and areas for improvement. This study not only contributes to the advancement of DC-DC converter design methodologies but also provides practical insights for enhancing power management efficiency in Smart Plug applications within micro- and nanogrid environments.

Keywords: DC-DC converters · buck converters · Smart Plugs · microgrids · nanogrids

1 Introduction

DC-DC converters integrated with smart management algorithms, also known as Smart Plugs, are a significant advancement in decentralized energy management. These converters improve control and efficiency in power distribution for a wide range of applications [1], enabling the integration and management of diverse load devices [1]. An example of a nanogrid with different Smart Plugs is shown in Fig. 1. Nanogrids can be designed with a variety of configurations [2]. These configurations can include systems that are either connected to the main power grid or operate independently as standalone systems [3]. Furthermore, nanogrids can utilize either DC buses or AC buses, each with its own characteristics and challenges [4]. For instance, voltage regulation, as well as protection and safety, are the main issues for DC bus-based nanogrids [5], while synchronization, reactive power management, and common mode currents may be the main

challenges for AC bus-based nanogrids [6]. However, Smart Plugs must meet several requirements: compatibility across a spectrum of load devices, reversibility, high power transmission rates, compact form factors for retrofit installations within existing buildings, and adaptive voltage and current capabilities [7]. For these reasons, a dynamic adjustment to match the requirements of the connected load is essential, along with efficient energy delivery, especially during peak demand or when powering multiple devices simultaneously [8]. In addressing these issues, DC-DC buck converters emerge as promising solutions [9]. These converters offer efficient voltage step-down capabilities, enabling seamless integration with low-voltage DC systems prevalent in micro and nanogrid configurations.

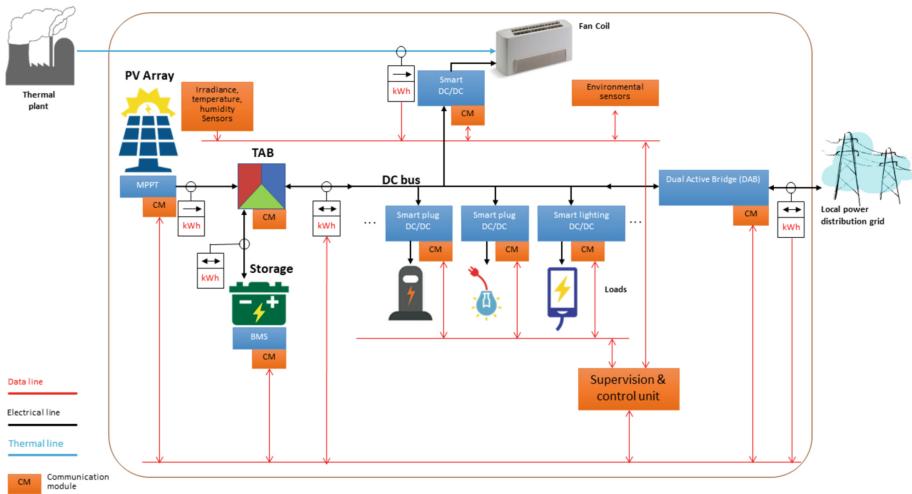


Fig. 1. Nanogrid architecture example.

Classical parameters such as efficiency and output ripple serve as fundamental metrics for evaluating the performance and suitability of DC-DC converters for Smart Plug applications. Additionally, working frequency influences both the electrical metrics and the mechanical ones. However, a trade-off between electrical and mechanical characteristics must be determined. Starting from these considerations, the paper proposes a comprehensive analysis of DC-DC buck converter prototypes. The focus is on efficiency, output ripple, and working frequency as key parameters.

2 Analyzed Smart Plugs

In this work, two Smart Plug prototypes were analyzed: a custom-made circuit version with GS61004 GaN System transistors, and a second version including the commercial GaN System GS-EVB-HB-61008P-ON evaluation board. Both prototypes are controlled by a NUCLEO-F446RE STMicroelectronics evaluation board and are designed with the same passive components as output filters. The two solutions follow similar designs.

However, in the custom-made circuit, the input voltage track is approximately half the length and twice the width, and it has been placed on both the top and bottom layers of the board, incorporating a substantial number of vias. Additionally, mirror-image capacitors have been positioned along the track path on both sides. Furthermore, the track between the GaN transistors and the inductor is significantly shorter. Given the particularly low resistance of the inductor, which is not greater than $9.68\text{ m}\Omega$, in the second version with the commercial GaN evaluation board, the resistance introduced by the connection between the board where the GaN transistors are placed, and the interface board is not negligible. Finally, concerning the logic control circuitry, the custom-made board features logic signals with the PWM signal that are notably shorter and consistently accompanied by a ground plane to optimize signal quality. Given the operating frequency, a possible increase of the propagation delay of the PWM signals of a few nanoseconds could result in small variations in efficiency. The component choice is shown in Table 1.

Table 1. Passive components choice for the two Smart Plug prototype versions.

Manufacturer	ID	Component type	Value	Quantity
Wurth Elektronik	74437529203470	Inductor	$47\text{ }\mu\text{H}$	1
TDK	C5750X7R2A475K230KA	Capacitor	$4.7\text{ }\mu\text{F}$	12
TDK	C3216C0G2A104J160AC	Capacitor	100 nF	8

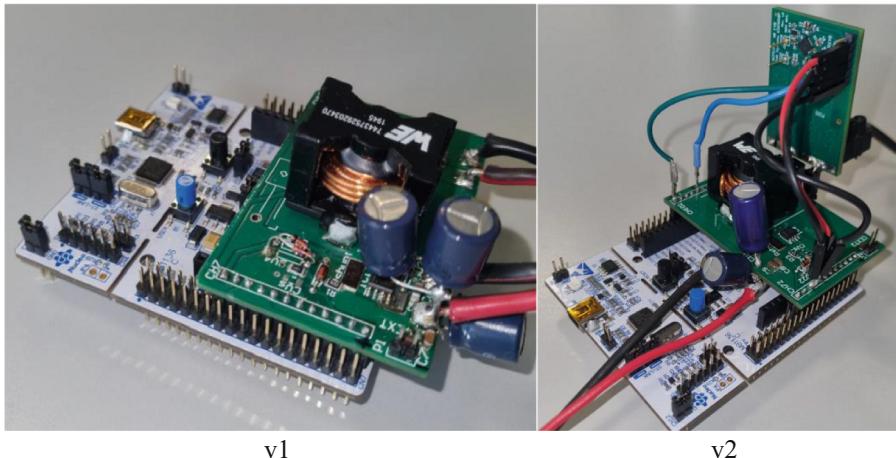


Fig. 2. Smart Plug prototypes: on the left (v1) custom-made DC-DC converter with GS61004 transistors; on the right (v2) DC-DC converter with the commercial half-bridge, which is the vertical board in the picture.

The sizing of the converter passive component is defined considering a target switching frequency of 1 MHz, a maximum current of 12 A, and a maximum power of 300 W. Figure 2 shows the two versions of Smart Plug prototypes.

3 Experimental Results

A first comparison, shown in Fig. 3, has been done on the efficiency of the two prototypes at two different working frequencies: 500 kHz and 1 MHz, at a constant output power of 50 W with an input voltage of 48 V. It can be noticed that the integration of the active devices on the same board increases the performances both at the desired 1 MHz switching frequency and at 500 kHz. However, compared to version 2, the custom-made board shows some relevant differences at higher output voltages. In particular, the efficiency increases substantially at 500 kHz switching frequency.

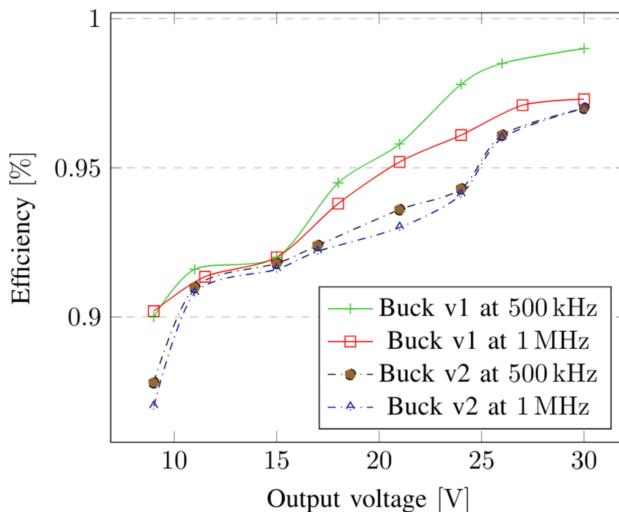


Fig. 3. Efficiency comparison at 1 MHz and 500 kHz switching frequencies ($V_{\text{input}} = 48$ V, Output Power = 50 W).

To better analyze the relation between frequency and efficiency for the custom-made board, Fig. 4 shows the efficiency and the output voltage ripple over different working frequencies with an input voltage of 19 V, an output voltage of 5 V, and a load current of 5 A.

It can be noticed that the efficiency reaches the optimal working frequency value at 200 kHz, while the output voltage ripple doesn't improve at working frequencies over 600 kHz. Therefore, the design can be improved by allowing a match between the two optimal conditions following key design steps. In this case, the output voltage ripple magnitude sets the limit. Considering a voltage ripple target of 2% of the output voltage, an optimal working frequency of 360 kHz has been defined. To determine how to reach

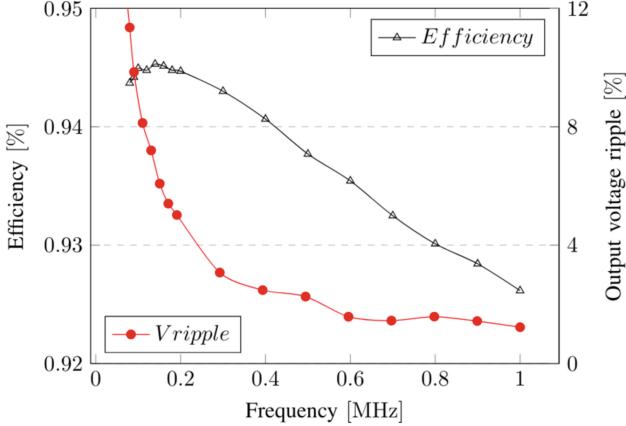


Fig. 4. Smart Plug prototype v1: efficiency and output voltage ripple over switching frequency ($V_{\text{input}} = 19$ V, $V_{\text{out}} = 5$ V, and $I_{\text{load}} = 5$ A).

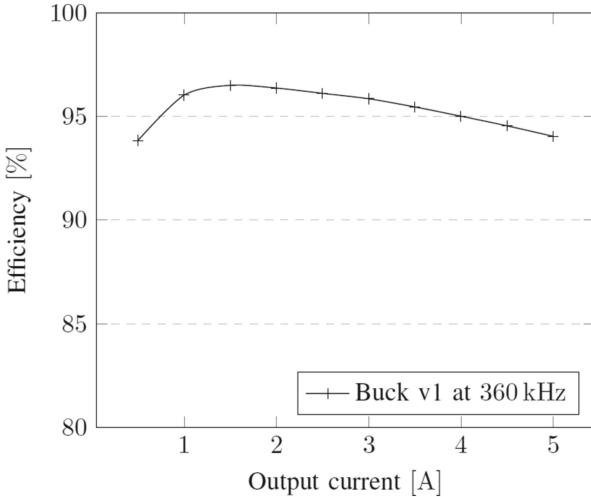


Fig. 5. Smart Plug prototype v1: efficiency vs the output current ($V_{\text{input}} = 19$ V, $V_{\text{out}} = 5$ V).

the optimal trade-off, it is also necessary to consider the efficiency analysis over different load conditions with an input voltage of 19 V and an output voltage of 5 V (see Fig. 5).

It can be shown that the minimum efficiency value corresponds to both the points of minimum and maximum current values, therefore with a good distribution of the efficiency values of the overall output current range. Considering the Smart Plug application, where there isn't a prevailing load type with a specific current and voltage rating, the current required on the load may vary on a quite wide current range. This shows a good design of the converter concerning the load variation, which may be difficult to further improve. For this reason, an optimization can be reached by integrating more

capacitors during the design phase. In this way, the working frequency can be reduced at the optimum efficiency value, without the limitations due to the output voltage ripple. The choice of the capacitors to be added can be made considering the 200 kHz target frequency, therefore their series AC resistance should be at its minimum value at this frequency.

Finally, a comparison with industry-standard benchmarks is shown in Table 2.

Table 2. Comparison with industry-standard benchmarks.

Converter ID	Input voltage [V]	Output voltage [V]	Max output current [A]	Rated power [W]	Efficiency [%]	Typ. Ripple [%]
Smart Plug prototypes v1	48	5–48	12	300	90–99	2
Smart Plug prototypes v2	48	5–48	12	300	88–97	2
RSD-300C-48	33.6–62.4	48	6.3	302.4	83–92	0.375
RPMGQ-20	18–75	5	20	100	91–94	N.A
RBBA3000	9–60	0–60	50	600 W*	85–96	0.42
RGC4W300W012A-003	9–53	5.0–28	12.5	300	91–96	2
COBO 1031501	48	12	12.5	300	> 89	0.83
VCCR300-12	33.6–160	12	25	300	Max. 92	1
I7C4W012A050V-001-R	9–53	5–28	12.5	300	91–96	4

* With 24 V input voltage and 12 V output voltage

4 Discussion

The first prototype of a DC-DC converter for Smart Plug was made to obtain higher efficiency with a more compact solution, while the second prioritized a modular approach with a commercial half bridge. Prototype 1 exhibited an efficiency between 90% and 99% varying the load and output voltage, sensibly higher than the average efficiency of commercial units, which ranges between 83 and 97% at the same power and voltage rates. Prototype 2, while not as efficient, still performed commendably with an efficiency between 88% and 97%.

In both solutions, output voltage ripple was a crucial performance metric, especially considering the Smart Plug application requires stable voltage supplies for the different possible loads. The design following standard buck converter equations doesn't allow us to obtain easily the best trade-off between efficiency and output voltage ripple concerning the working frequency. It must be highlighted that the choice of inductors and capacitors significantly impacts both efficiency and output ripple. For instance, low Equivalent Series Resistance (ESR) capacitors were essential for minimizing ripple at high frequencies. However, a bottleneck is reached at a certain frequency which shows

that enhancing the working frequency doesn't improve the output voltage ripple performances. For this reason, the converter sizes may not sensibly decrease by increasing the switching frequency due to the need for a greater number of small capacitors to decrease ESR and Equivalent Series Inductance (ESL), and the reduction of efficiency even with the use of Wide Bandgap Semiconductors (WBS) such as GaN transistors.

Moreover, this study demonstrates how the design of the Printed Circuit Board (PCB) affected the performance of the converter. The study compared two prototypes with identical components but different layouts. Thoughtful routing of power and ground planes, as well as minimizing the length of high-current paths, resulted in reduced noise and improved overall efficiency.

5 Conclusions

This study investigated the design, development, and performance evaluation of two prototypes of Smart Plug DC-DC buck converters, comparing their efficiency and output voltage ripple with commercial converters. The efficiency of both prototypes was thoroughly tested and benchmarked against commercial converters.

The development and evaluation of the two Smart Plug DC-DC buck converter prototypes highlighted the importance of tailored design choices to meet specific performance criteria. Efficiency and output ripple, while both critical, often require trade-offs that must be carefully managed through design considerations such as component selection and PCB layout.

The switching frequency emerged as a key factor influencing these trade-offs, demonstrating that a nuanced approach is necessary to achieve an optimal balance between size, efficiency, and output voltage ripple.

References

1. Ahmed, M.S., et al.: Smart plug prototype for monitoring electrical appliances in home energy management system. In: IEEE Student Conference on Research and Development (2015)
2. Boroyevich, D., et al.: Future electronic power distribution systems - A contemplative view. Proc. Int. Conf. Optim. Electr. Electron. Equipment, pp. 1369–1380. OPTIM (2010). <https://doi.org/10.1109/OPTIM.2010.5510477>
3. Blanchard, R., Little, M.: Developing an open access monitoring device for off-grid renewables. In: ICDRET 2016 - 4th International Conference on the Developments in Renewable Energy Technology, pp. 1–6. UIU (2016). <https://doi.org/10.1109/ICDRET.2016.7421511>
4. Boroyevich, D., Cvetkovic, I., Burgos, R., Dong, D.: Intergrid: a future electronic energy network? IEEE. J. Emerg. Sel. Top. Power Electron. **1**, 127–138 (2013). <https://doi.org/10.1109/JESTPE.2013.2276937>
5. Asad, R., Kazemi, A.: A quantitative analysis of effects of transition from AC to DC system, on storage and distribution systems. Asia-Pacific Power Energy Eng. Conf. APPEEC. (2012). <https://doi.org/10.1109/APPEEC.2012.6307519>
6. Concari, L., et al.: H8 architecture for reduced common-mode voltage three-phase PV converters with silicon and SiC power switches. In: IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, pp. 4227–4232 (2017). <https://doi.org/10.1109/IECON.2017.8216725>

7. Heo, S., Park, W.-K., Lee, I.: Energy management based on communication of Smart Plugs and inverter for smart home systems. In: 2017 International Conference on Information and Communication Technology Convergence (ICTC), pp. 810–812 (2017). <https://doi.org/10.1109/ICTC.2017.8190788>
8. Nordman, B., Christensen, K.: Local power distribution with nanogrids. In: 2013 Int. Green Comput. Conf. Proceedings, IGCC 2013 (2013). <https://doi.org/10.1109/IGCC.2013.6604464>
9. Nayanasiri, D., Li, Y.: Step-Down DC–DC Converters: An Overview and Outlook. *Electronics* **11** (2022). <https://doi.org/10.3390/electronics11111693>



Modeling and Optimization of 1.2 kV SiC-Based Pre-package Power Module in Half-Bridge Arrangement Using Finite Element Analysis

Saimir Frroku^{1(✉)}, Ankit Bhushan Sharma², Till Huesgen², Andrea Irace³, and Giovanni A. Salvatore^{1(✉)}

¹ Department of Molecular Science and Nanosystems, Ca' Foscari University of Venice, Venice, Italy

{saimir.frroku,giovanni.salvatore}@unive.it

² Electronics Integration Laboratory, University of Applied Sciences Kempten, Kempten, Germany

³ Department of Electrical Engineering and Information Technologies, University of Naples Federico II, Napoli, Italy

Abstract. The wide band gap (WBG) power devices, silicon carbide (SiC) and gallium nitride (GaN), have emerged as a promising alternative to the traditional silicon (Si) based devices. This is primarily due to Si's theoretical limits regarding high voltage endurance and high-frequency operation [1, 2]. To optimize the performance of WBG semiconductors, it is crucial to develop new packaging technologies and thermal-electric designs that facilitate efficient and rapid device switching while minimizing energy losses. This study delves into the thermal, electrical, and mechanical behavior of new prepackage embedding technologies using finite element simulation, aiming to create a digital twin block. The research explores insulated substrates, including direct bonded copper (DBC) with various dielectrics such as AlN, Al₂O₃, and Si₃N₄, as well as insulated metal substrates (IMS), with a focus on commercially available materials and thicknesses. A thermo-mechanical Pareto-optimization methodology is proposed to identify the optimal substrate configuration. The sintered silver layer, prone to delamination, is modeled using a temperature-dependent bi-linear hardening model to account for plasticity and creep. The results highlight that the DBC with AlN substrate configuration offers the best thermal and mechanical performance, with a thermal resistance of 0.34 K/W and an accumulative plastic strain of 0.18%. Moreover, the study assesses the parasitic inductance of multiple prepackages to scale the module's power. Effective design implementation can reduce the stray inductance to as low as 1.23 nH for two prepackages and 2.85 nH for four prepackages, demonstrating the practical implications of this research in improving the efficiency and performance of power modules.

Keywords: WBG power devices · Finite element simulation · Pre-package embedding technologies · Thermo-mechanical Pareto-optimization

1 Introduction

Wide bandgap semiconductors (WBG) such as Gallium Nitride (GaN) and Silicon Carbide (SiC) play a pivotal role in the development of next-generation power electronics modules, surpassing the limitations of Silicon (Si)-based devices [1, 2]. WBG are revolutionizing the field of power electronics, surpassing the limitations of Si-based devices. The well-known challenges associated with Si, such as the breakdown field and thermal behavior, underscore the need to harness all WBG's advantages. To do so, new packaging technologies are essential, considering top interconnection, bonding, cooling, and mechanical design to minimize power losses and ensure a clean switching [3]. Among these, chip scale packaging (CSP) stands out as one of the most promising technologies. It involves embedding multiple power devices to lower parasitic inductances, offering a potential solution to current challenges [4]. This paper takes an approach to address all the current packaging challenges using the multiphysics simulation, a robust and reliable methodology that connects different physical domains and helps understand their influence on each other. A pre-packaged CSP comprising a semiconductor module that has been attached to a copper (Cu) or molybdenum (Mo) metallic substrate, enclosed in an epoxy molding compound (EMC), and structured and electroplated to establish connections with the chip was employed as a simulation model. This approach opens up new possibilities for designing and optimizing power modules [5, 6]. The article investigated three aspects of the design. In the first part, an accurate power loss model was built using a thermo-electrical simulation, and the second part examined the influence and ways to improve the mechanical behavior caused by the mismatch between the coefficient of thermal expansion (CTE) and various insulated substrates (ceramic and insulated metal substrates - IMS).

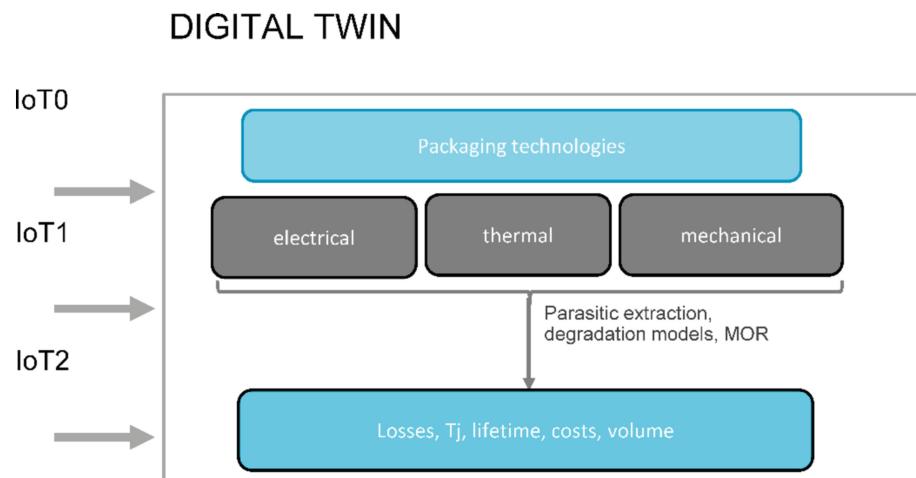


Fig. 1. Proposed Digital Model Twin to address WBG packaging challenges.

Electromagnetic simulations have been utilized to optimize two designs, each consisting of two and four pre-packages arranged in a half-bridge configuration. This optimization is particularly relevant for applications necessitating a range of power levels. The stray inductance is maintained below 3 nH, with evenly distributed mutual coupling between the chips to ensure uniform current distribution. The final output is the generation of a digital twin of the power module, which incorporates electrical, thermal, and mechanical behavior (see Fig. 1), showcasing the nature of this research.

2 Methodology for Modelling and Simulation

2.1 Geometrical Modelling

The simulated pre-package unit comprises two SiC MOSFETs (with a voltage rating of 1200 V, CPM31200-0016A) in a half-bridge configuration. A double silver sinter layer (SAG) of 20 μm was used to attach the MOSFETs to a direct-bond copper (DBC) substrate, and the bonding methodology was used for the top interconnection.

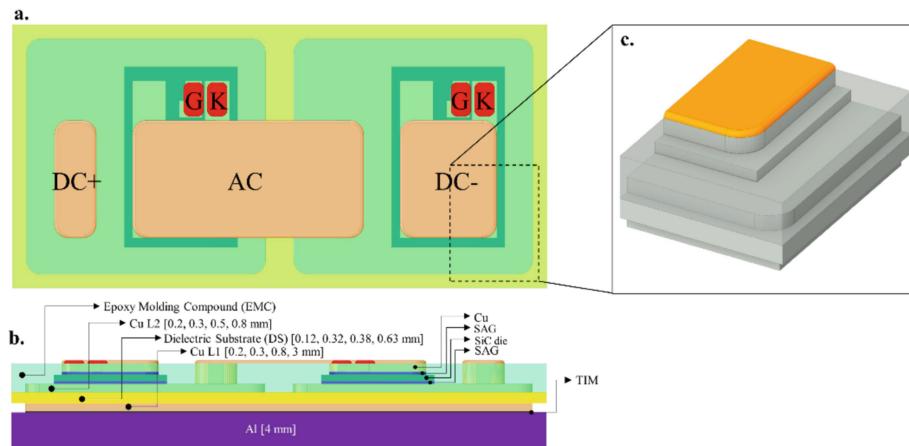


Fig. 2. a. Proposed pre-package design with an insulated substrate with two SiC chips connected in half-bridge configuration, b. Cross-section structure, c. Quarter Model of SiC MOSFET.

The pre-package uses a 4 mm thick heatsink, and thermal interface material (TIM) is in between the heatsink and the Cu baseplate to improve the accuracy of the thermal simulation (see Fig. 2a, b). The last operation was to parametrize the thickness of each layer in the DBC and dielectric type to identify the best configuration (see Table 1). A quarter module (see Fig. 2c) was employed to perform the thermo-mechanical simulation; the primary motivation was to improve the meshing quality and the result accuracy.

2.2 Material Modelling

Material properties data represent a benchmark to obtain an accurate result and prevent convergence issues during simulation. Another critical requirement is the use of the non-linear dataset, which changes as temperature changes, especially during the mechanical

Table 1. Simulated split design

Design	Cu L1 (mm)	DS* (mm)	Cu L2 (mm)	DS*
DP0	0.3	0.38	0.3	Al ₂ O ₃
DP1	0.3	0.38	0.3	Si ₃ N ₄
DP2	0.8	0.32	0.8	Si ₃ N ₄
DP3	0.3	0.63	0.3	AlN
DP4	0.3	0.63	0.3	Al ₂ O ₃
DP5	0.2	0.63	0.2	AlN
DP6	0.2	0.63	0.2	Al ₂ O ₃
DP7	3	0.12	0.5	IMS A
DP8	3	0.12	0.5	IMS B
DP9	3	0.12	0.5	IMS C

* DS – Dielectric Substrate

simulation. The models take into account the yield stress (σ_y), Young's modulus (E), Poisson's ratio (v), thermal conductivity (λ), thermal expansion (CTE), and specific heat (c_p) (see Table 2).

Table 2. Material Properties Table

Material	CTE ($10^{-6}/K$)	E (GPa)	λ (W/mK)
SiC	4	410	450
EMC	$8^1/34^2$	$29.1^1/1.3^2$	0.8
Ag	18.9	83	429
Cu	17	110	400
Al ₂ O ₃	6.5	400	26
Si ₃ N ₄	2.3	250	90
AlN	4.6	323	163
IMS A	$17^3/40^4$	$10^3/6.1^4$	5.2
IMS B	$15^3/34^4$	$39^3/31^4$	11.1
IMS C	$12^3/37^4$	$27^3/21^4$	14.4
TIM	Z = 0.2 °C·cm ² /W		

1 For T < T_g where T_g = 165 °C | 2 For T > T_g where T_g = 165 °C

3 For T < T_g where T_g(IMS A) = 195 °C, T_g(IMS B,C) = 205 °C

4 For T > T_g where T_g(IMS A) = 195 °C, T_g(IMS B,C) = 205 °C

The bilinear hardening model is needed to evaluate the plastic strain in the SAG layer, which is most prone to delamination and failure.

Table 3. Material properties table temperature depended for SAG [7] and Cu soft [8].

	22 °C	60 °C	80 °C	SAG 100 °C	125 °C	150 °C	Cu 22 °C
E (GPa)	32.4	27.6	24.4	19.9	17.9	16.3	120
σ_y (MPa)	52	37	33	32	28	23	49.75
TM* (GPa)	16	13	11	8	6.5	5	0.64

*TM – Tangent Modulus

The data reported in Table 3 are necessary to generate the model (see Fig. 3).

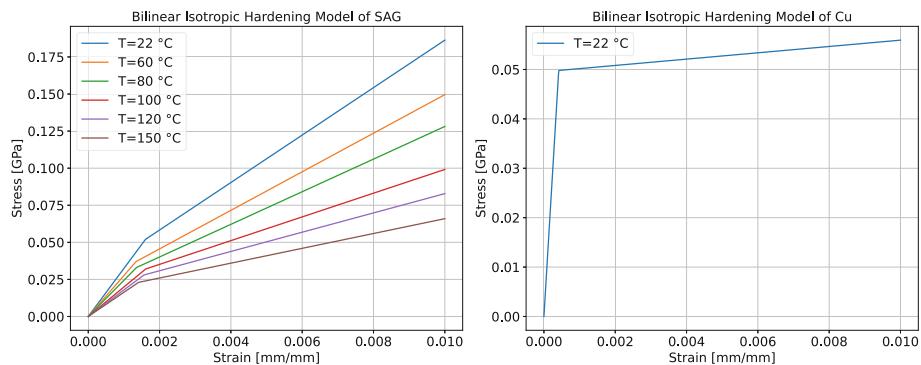


Fig. 3. Bilinear hardening model of SAG [7] and Cu [8].

2.3 Meshing Modelling

Meshing is a critical step in the simulation process, with particular attention needing to be paid to proximity effects, division of layers, and the use of quadratic elements where applicable. Refinement of meshing at contact interfaces is necessary for accurate results (see Fig. 4). Failure to follow these guidelines may result in inaccuracies, such as incorrect strain distribution where the highest strain is located at the symmetry cross section and not the edge (which is not true). The highest strain is experienced at the edge because the highest thermal expansion mismatch is located at the edge, representing the initial point where delamination starts [9].

2.4 Boundary Conditions

Setting up the boundary conditions is one of the most challenging tasks. One must find a realistic combination that works without over-constrained the model. The section reports the boundary conditions for the thermal and thermo-mechanical parts. In the thermal simulation, the conditions that were applied were a power source of 100 W on the top surface of each of the SiC die and a convection thermal condition (with a heat

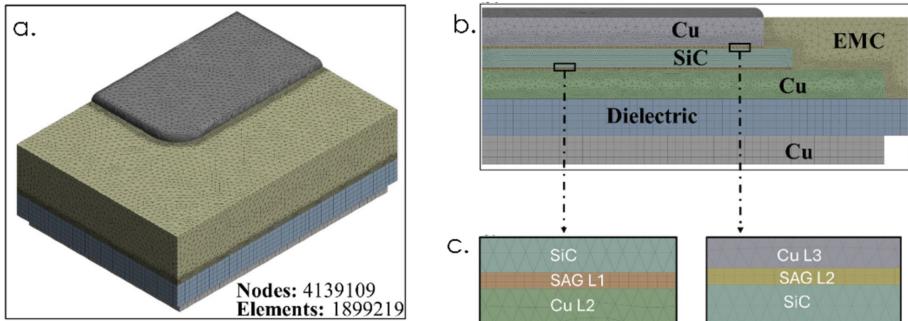


Fig. 4. a. Meshing profile of the quarter module and respective statistics, b. Meshing statistic of the quarter module, c. Zoom view of the SAG layers.

transfer coefficient of $5000 \text{ W/m}^2\text{K}$ and a reference temperature of 85°C) on the bottom surface of the aluminum (Al) heatsink. A zero thickness layer (TIM) with a thermal impedance condition ($Z = 0.2 \text{ }^\circ\text{C}\cdot\text{cm}^2/\text{W}$) was inserted between the heatsink and the baseplate (see Fig. 5).

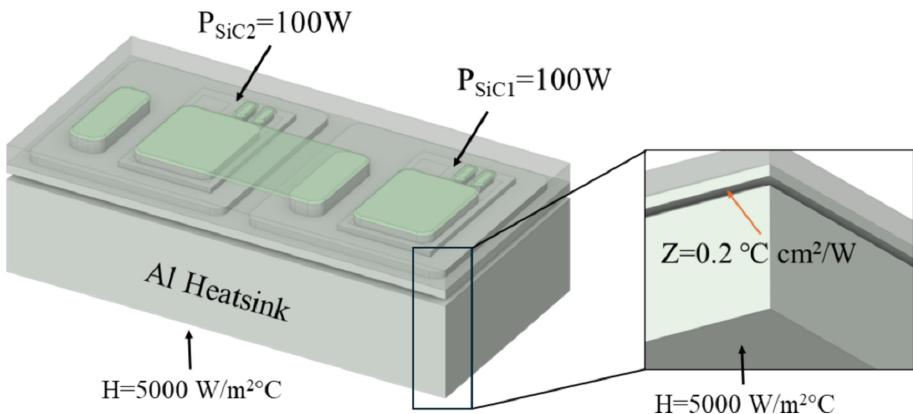


Fig. 5. Applied boundary condition in the thermal simulation.

In the thermo-mechanical simulation phase, a quarter model was divided from the full model, and the Al heatsink was removed. To account for the results for the entire model, two symmetry/frictionless boundary conditions were applied in combination with a fixed support at the vertex, where the cross-section of the symmetry planes is (see Fig. 6). The setup was configured to replicate the passive cycling, where the model was cooled down from 180°C (stress-free) to -40°C .

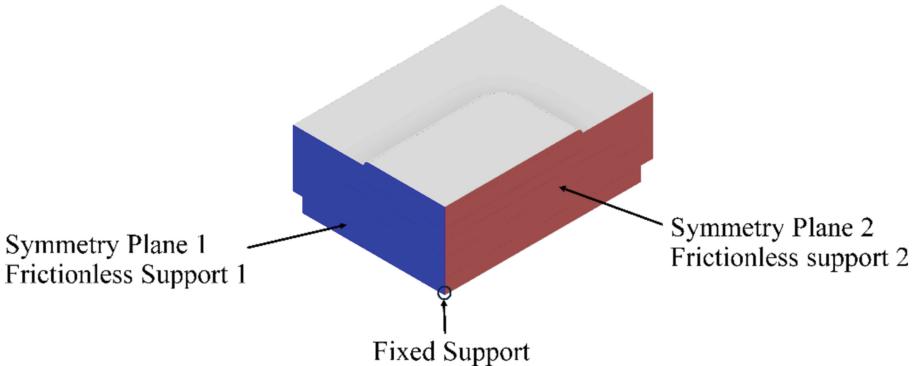


Fig. 6. Applied boundary condition in the thermo-mechanical simulation.

3 Results

3.1 Thermal Simulation

The thermal simulation results clearly show that the temperature distribution is uniform and that the difference in temperature between the two dies is in the range of 0.7 °C. The cross-section shows that the TIM layer strongly influences the pre-packaged module's heat dissipation capability (Fig. 7).

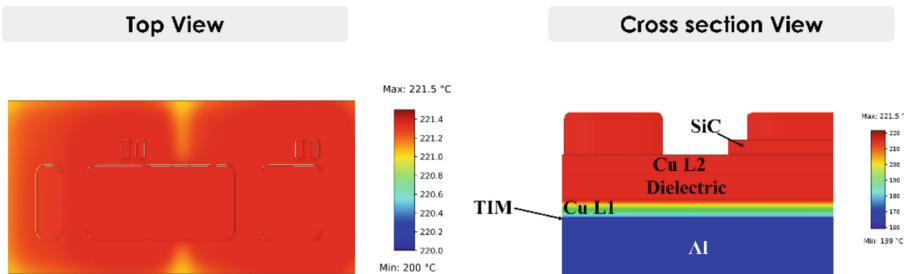


Fig. 7. The thermal profile of the pre-packaged unit is presented in two different views: Top and cross-section.

The best configuration from a thermal point of view is DP2 (in terms of lowest thermal resistance), which currently employs a silicon nitride (Si_3N_4) substrate, and the worst configuration is DP6, which uses the aluminum oxide substrate. The main difference in the thermal behavior is the thermal conductivity of Si_3N_4 , which is three times higher than that of Al_2O_3 . Another factor that impacts the thermal behavior is the thickness of the dielectric substrate, which explains why Si_3N_4 performs better than AlN (see Fig. 8). To determine the thermal resistance, the following equation has been employed:

$$R_{TH} = \frac{T_j - T_{hsk}}{P} (K/W) \quad (1)$$

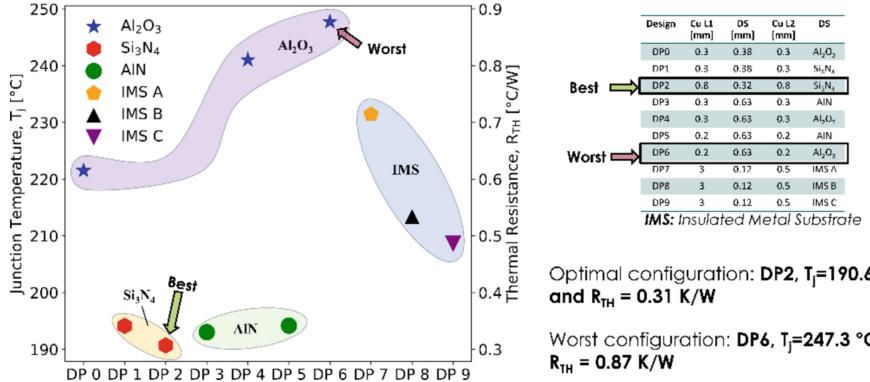


Fig. 8. Junction temperature and thermal resistance versus the proposed designs.

3.2 Double Pulse Testing Simulation

Double pulse testing is a standard method in power electronics to assess a power device's switching parameters, E_{on} , E_{off} , and Q_{rr} [10], which will be used later to evaluate the switching losses accurately.

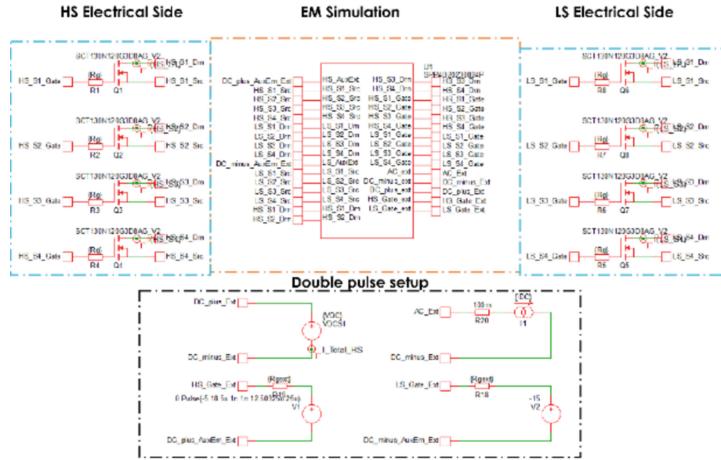


Fig. 9. The double pulse setup evaluated the switching parameters.

The setup considers four pre-packaged in a half-bridge configuration, which undergoes an electromagnetic simulation to extrapolate the parasitic inductances and the equivalent circuit. The circuit will then be used in the double pulse test, and an accurate reading of the switching energy will be performed in combination with the spice model, which represents the electrical side (see Fig. 9). When the simulation is completed, the final output will be the switching parameters for each side, low side, and high side (see Fig. 10). The switching energy has been determined by integrating the power in each switching

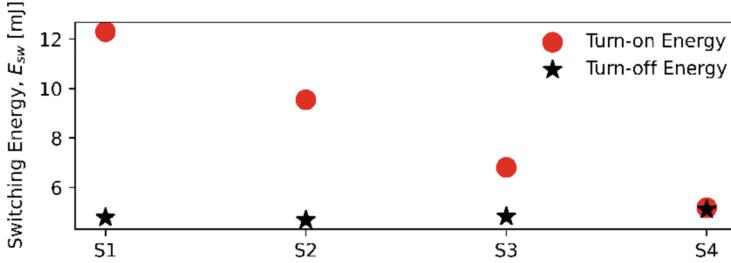


Fig. 10. Example of overall switching energy for each switch obtained from the double pulse test simulation of the entire circuit.

equation. When the parameters have been determined, they will be used as input in the electro-thermal simulation to obtain an accurate result of the power loss.

3.3 Electro-Thermal Simulation

This section presents the derivation of the electro-thermal model starting from the CAD model. It is followed by the development of a power loss model and is completed by inserting the thermal MOR block of the material obtained from the thermal simulation (see Sect. 3.1).

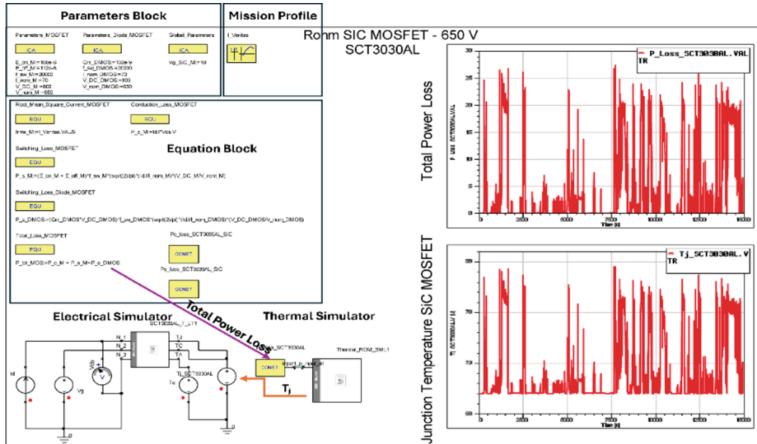


Fig. 11. A thermo-electrical simulation framework is used to determine the total power losses.

The procedure comprises four blocks: SPICE, MOR, the equation, and the mission profile block. The mission profile block determines the total power loss, and the measured losses serve as input in the MOR block, which calculates the unit's junction temperature (T_j). When T_j is measured, it goes as a secondary input in the spice model, affecting the magnitude of the power loss. This temperature change primarily affects the conduction loss, and by involving the loss, T_j changes again. In a few words, between the spice and

the more model, a two-way coupling interaction is created that considers the temperature component to determine a more realistic result for the power losses. (see Fig. 11).

Compared with the traditional methods (like Foster and Cauer), the thermal MOR considers the model geometry and allows the incorporation of the convective boundary condition into the block.

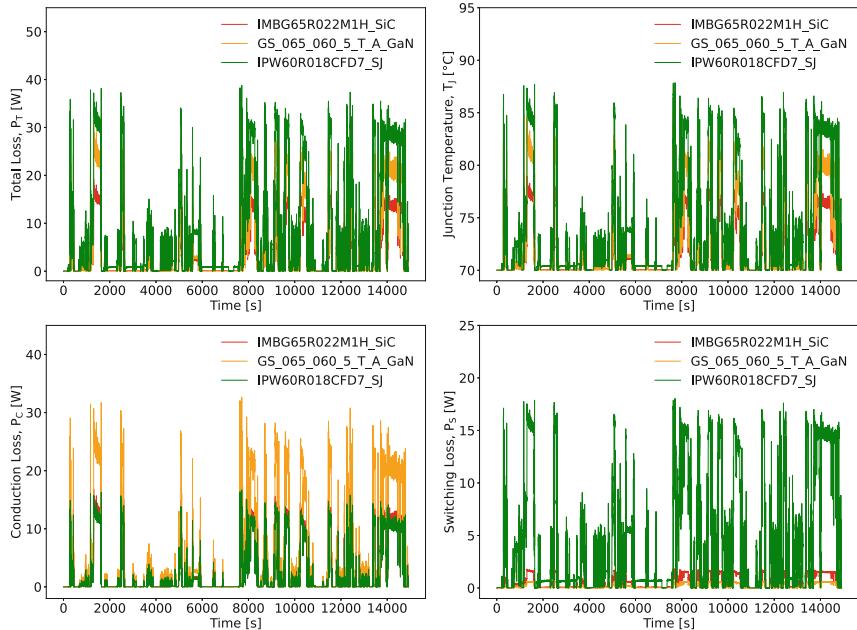


Fig. 12. Power loss comparison and junction temperature profile ($f_{sw} = 20$ kHz, $T_{ref} = 70$ °C).

This section is completed by making a comparison between Si SJ/SiC and GaN-based power modules in a voltage rating of 650 V, where all three can be employed in an application to determine the best device, and as an input is the mission profile of an electrical boat operating in the bay of Venice. Regarding total power loss, the simulation results show that the SiC-based device performs better than the other for this type of application. A more refined analysis shows that GaN-based devices experience the highest conduction loss, and Si SJ-based devices experience the lowest because of the on-state resistance (see Table 4, Fig. 12), which is the lowest in this case.

When we perform the same analysis for the switching losses, it is clear that GaN outperforms the other devices because it has the lowest turn-on/turn-off energies and a reverse recovery charge of 0 nC (see Fig. 12).

3.4 Thermo-Mechanical Simulation

The simulation was set up to replicate a passive cycling process where the device is in the off state and is cooled down from $T = 180$ °C (stress-free) to -40 °C, and a reading of

Table 4. On-state resistance comparison between various power MOSFETs

Device name	Type	R _{D5(on)} (mΩ)
IPW60R018CFD7	Si SJ*	18
IMBG65R022M1H	SiC	22
GS-065-060-5-T-A	GaN	25

* SJ – Super Junction

the stress and plastic strain is done. In all the simulated splits (see Table 1), the highest stress was recorded in the SiC die and the lowest in the Cu baseplate. Regarding the plastic strain, the highest plastic strain was recorded in the contact face between the sinter layer and the SiC die. In terms of magnitude, the highest was recorded at the edge of the SAG layer, where the highest mismatch of CTE is expected, as observed in experimental observations of delamination of the SAG layer (Fig. 14).

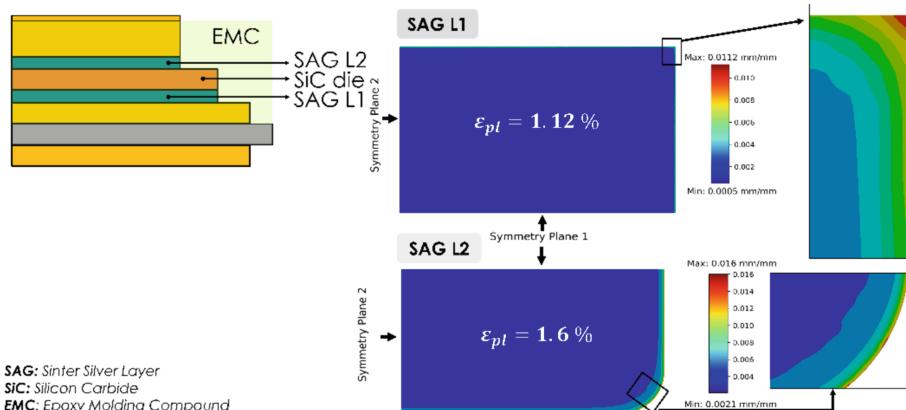


Fig. 13. Plastic strain distribution in the sintering layer during the passive cycling process (a quarter model was simulated to reduce the simulation complexity).

The maximum value of the plastic strain was 1.12% and 1.6% for SAG L1 and SAG L2, respectively (see Fig. 13). A normalized value, average cumulative plastic strain ($\bar{\epsilon}_{pl}^{avg}$), had to be extrapolated to compare the plastic strain between various splits. The strain is propagated from one corner of the quarter model to a length “a” determined based on a 10% area delamination. The values of “a” are 0.127 mm and 0.11 mm for SAG L1 and SAG L2, taking into account the differing areas of the two layers ($A_{SAG-L1} = 3.22 \times 2.02 \text{ mm}^2$, $A_{SAG-L2} = 2.92 \times 1.72 \text{ mm}^2$). The average planar strain ($\bar{\epsilon}_{pl}^{avg}$) is calculated accordingly [7]:

$$\bar{\epsilon}_{pl}^{avg}(a) = \frac{1}{a} \int_0^a \bar{\epsilon}_{pl}(s) ds \quad (2)$$

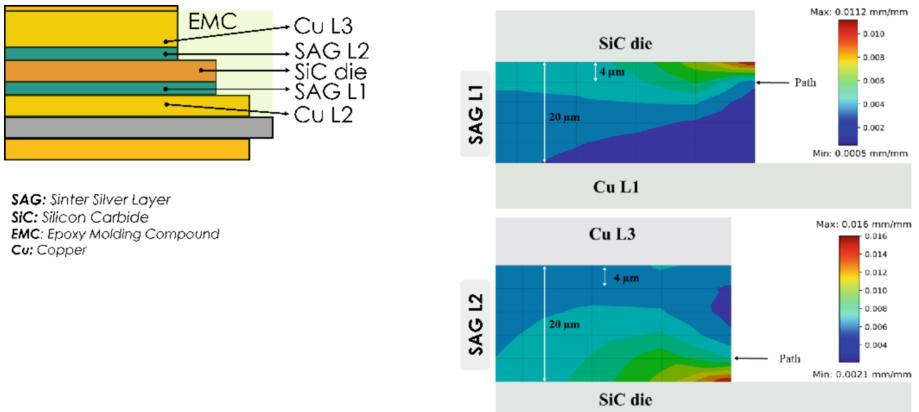


Fig. 14. The distribution of plastic strain along a specific path.

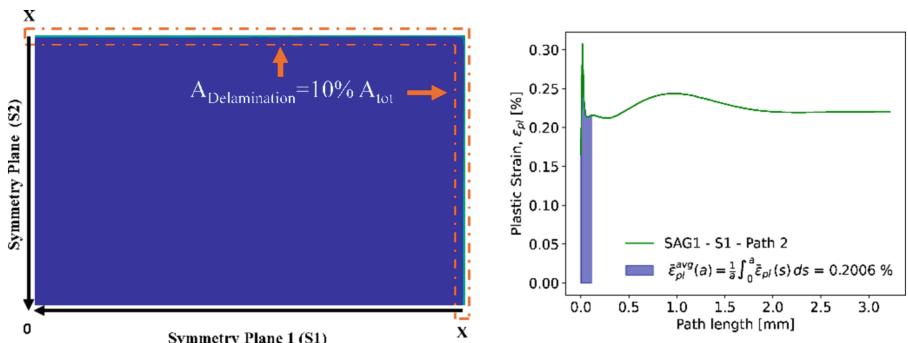


Fig. 15. a. Strain distribution in the SAG layer with the red-dashed lines indicating 10% of the total area; b. Plastic strain along the direction S1 and the equivalent ε_{pl}^{avg} .

Figure 16 shows the ε_{pl}^{avg} for each configuration and includes both SAG layers along the two directions, S1 and S2.

3.5 Discussion

The graphical representations facilitate the observation of distinct trends in substrate properties. The average ε_{pl}^{avg} of IMS substrates is notably three times greater than that of DBC substrates in the Sintering Layer 1 (SAG L1) located at the base of the SiC die. Conversely, the ε_{pl}^{avg} in Sintering Layer 2 (SAG L2) remains relatively constant across all configurations. Additionally, the ε_{pl}^{avg} in SAG L2 is consistently higher than in SAG L1 for DBC technology. Figure 17 synthesizes the findings of thermal and mechanical simulations into a single graph for SAG L1 and SAG L2, offering insights for achieving optimal thermo-mechanical performance through Pareto optimization. It is suggested that the most favorable configuration should be situated close to the bottom left corner of the graph.

The analysis of the two graphs indicates the following conclusions:

- In SAG L1, the configuration featuring IMS and Al_2O_3 materials exhibits subpar performance compared to the others due to the high $\varepsilon^{\text{avg}}_{\text{pl}}$ (IMS) and inferior R_{TH} (Al_2O_3) values. The AlN substrate offers the most balanced compromise among the options.
- In SAG L2, no clear choice emerges. IMS shows the lowest $\varepsilon^{\text{avg}}_{\text{pl}}$ values, while AlN and Si_3N_4 display the lowest R_{TH} values.
- Given the narrow range of $\varepsilon^{\text{avg}}_{\text{pl}}$ value in SAG L2, the preferred design options are Si_3N_4 and AlN.

3.6 Paralleling Configuration

A stacked structure was required to facilitate interconnection between prepackaged components and enable the paralleling process. Using prepackaged insulated substrates offers a significant advantage in allowing for easy parallel scaling of power levels through a modular assembly approach.

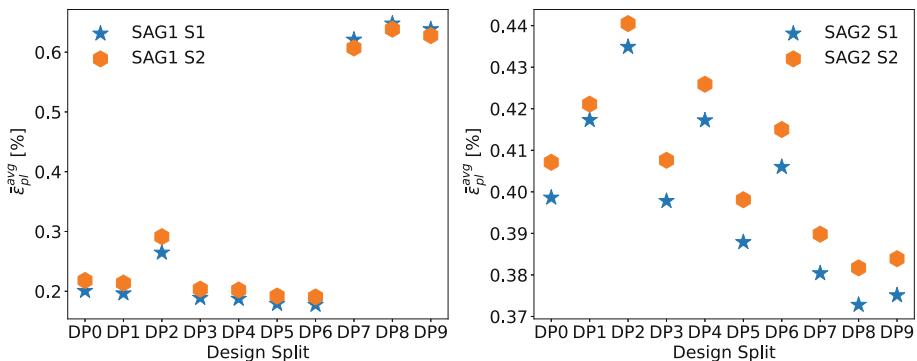


Fig. 16. Accumulated equivalent plastic strain along the path with the highest plastic strain. The singularity point was excluded from the analysis, (left) SAG L1, (right) SAG L2. S1 and S2 in the plot legend denote the orientation along the symmetry planes from which the highest plastic strain was extracted.

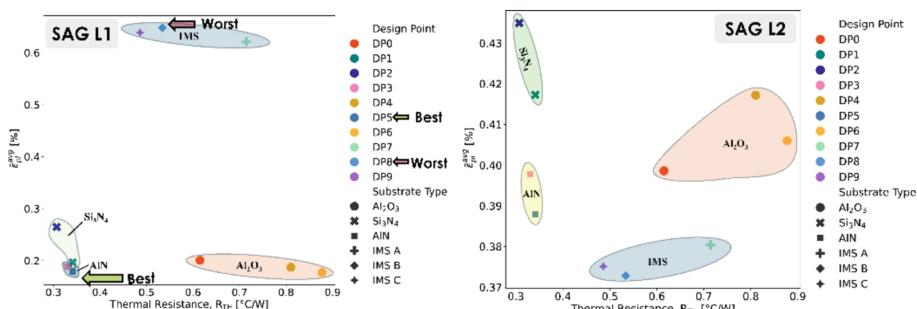


Fig. 17. The graphs for SAG L1 (left) and SAG L2 (right) depict the relationship between accumulated equivalent plastic strain and thermal resistance in the proposed pre-package design.

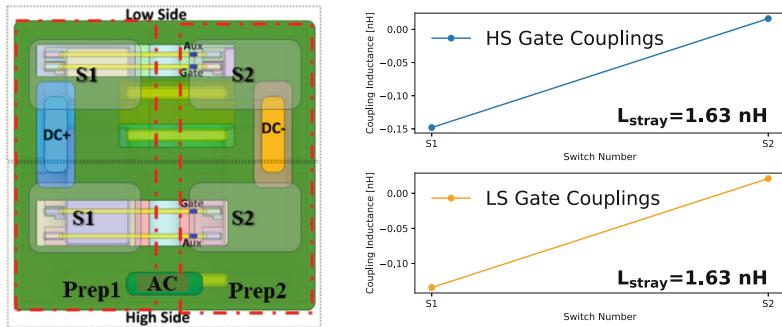


Fig. 18. Left: Suggested parallel configuration for two pre-packaged units. Right: Simulated mutual inductances for two pre-packaged units.

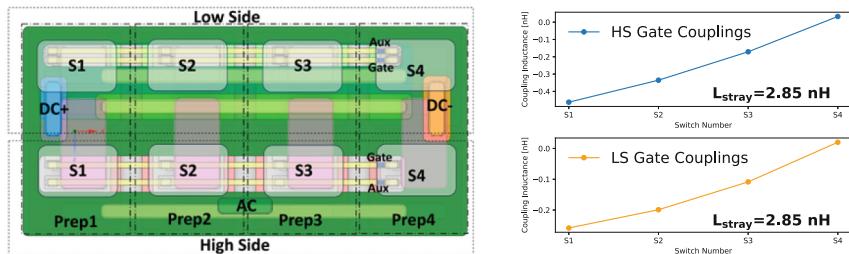


Fig. 19. Left: Suggested parallel configuration for four pre-packaged units. Right: Simulated mutual inductances for four pre-package units.

However, to fully leverage the capabilities of wide bandgap semiconductors, it is essential to minimize stray inductance. Electromagnetic simulations predict the parasitic stray inductance when connecting two or four prepackages in parallel. Figures 18 and 19 depict the paralleling of two and four prepackages, respectively, showing the mutual gate coupling for each chip, which accounts for the inductance resulting from the interaction of the commutation current with the gate loop. The positions of each prepackage are represented by dashed-dotted lines (red in Fig. 18 and black in Fig. 19), with the letter "S" followed by a corresponding number indicating the positions of the MOSFET units. Notably, the stray inductance is below 2 nH for the two-prepackage module and below 3 nH for the four-prepackage version.

4 Conclusions

In conclusion, the article broadly overviews the main challenges in packaging WBG-based devices. The strategy reported in the article involves using multiple physical simulation tools and explains how to combine them. The article's main focus was to find a geometrical configuration through the Pareto optimization methodology, which satisfies the requirements of lower R_{TH} and plastic strain. The simulation showed that the configuration, which uses a ceramic-based substrate, Si_3N_4 , and AlN, fulfills those

requirements at best. It was also demonstrated that paralleling is possible using the pre-packaged units, which is an acceptable stray inductance under 3 nH. Future work will focus on creep investigation, power cycling, and lifetime estimation.

References

1. Chow, T.P., Tyagi, R.: Wide bandgap compound semiconductors for superior high-voltage power devices. In: Proceedings of the 5th International Symposium on Power Semiconductor Devices and ICs, IEEE, pp. 84–88 (1993)
2. Wide Bandgap Semiconductor Power Devices. Elsevier (2019)
3. Hoene, E., Ostmann, A., Marczok, C.: Packaging very fast switching semiconductors. In: CIPS 2014; 8th International Conference on Integrated Power Electronics Systems, pp. 1–7 (2014)
4. Reiner, R., et al.: PCB-Embedding for GaN-on-Si Power Devices and ICs. In: CIPS 2018; 10th International Conference on Integrated Power Electronics Systems, pp. 1–6 (2018)
5. Thomas, T., et al.: Presentation of a Reliable Molded Power-PrePackage. CIPS 2022; 12th International Conference on Integrated Power Electronics Systems, pp. 1–8 (2022)
6. Huesgen, T., et al.: Reliability Screening of a Hybrid DBC/PCB power semiconductor prepackage. In: 2021 23rd European Microelectronics and Packaging Conference & Exhibition (EMPC), IEEE, pp. 1–5 (2021)
7. Heilmann, J., Wunderle, B., Zschenderlein, U., Wille, C., Pressel, K.: Physics of failure based lifetime modelling for sintered silver die attach in power electronics: Accelerated stress testing by isothermal bending and thermal shock in comparison. *Microelectron. Reliab.* **145**, 114973 (2023)
8. <https://www.jahm.com>, Materials Database.
9. DeVoto, D.J., Paret, P.P., Wereszczak, A.A.: Stress intensity of delamination in a sintered-silver interconnection. Additional Conferences (Device Packaging, HiTEC, HiTEN, and CICMT), vol. 2014, no. HITEC, pp. 000190–000197 (2014)
10. <https://www.tek.com/en/solutions/industry/power-semiconductor/double-pulse-testing>, Double Pulse Testing.

Electronic Systems and Applications



Supporting in-Sensor Computing with Hardware-Aware Neural Architecture Search

Andrea Mattia Garavagno^{1,2,3(✉)}, Edoardo Ragusa¹, Rodolfo Zunino¹,
Antonio Frisoli^{2,3}, and Paolo Gastaldo¹

¹ Department of Electrical, Electronic, Telecommunications Engineering, Naval
Architecture (DITEN), University of Genoa, 16126 Genoa, GE, Italy

AndreaMattia.Garavagno@edu.unige.it

² Department of Excellence in Robotics and AI, Scuola Superiore Sant'Anna, Piazza
Martiri della Libertà 33, 56127 Pisa, Italy

³ Institute of Mechanical Intelligence, Scuola Superiore Sant'Anna, Ghezzano, 56010
Pisa, Italy

AndreaMattia.Garavagno@santannapisa.it

Abstract. Hardware-aware neural architecture search (HW-NAS) is a powerful tool for the automatic design of tiny neural architectures able to fit the tight memory constraints of commodity electronics, like microcontroller units (MCU). However, new sensors equipped with neural processing units (NPUs) are reaching the market. In contrast to common MCUs, NPUs often do not feature the traditional division of the memory constraint between RAM and Flash usage. This is an issue for state-of-the-art HW-NAS, which are designed to fit the two constraints distinctly. This work proposes a novel HW-NAS for designing tiny Convolutional Neural Networks (CNNs) that can effectively deal with NPUs, achieving state-of-the-art results in just 5 h and 48 min on the Visual Wake Words dataset, a tinyML benchmark.

Keyword: In-sensor computing, hardware-aware neural architecture search, tinyML

1 Introduction

Hardware-aware neural architecture search (HW-NAS) has become a popular option for the automatic design of tiny neural architectures able to fit the tight constraints of commodity electronics, like microcontroller units (MCU) [4]. However, commodity electronics is changing to satisfy the arising need of running neural architectures at the edge. New sensors equipped with neural processing units (NPUs) are reaching the market. Such sensors, like Sony's IMX 500 [5], shown in Fig. 1, and STM's ISPU [15], feature a small SRAM, supposed to contain the application's code, parameters, and memory buffers needed to perform inference. The latter memory architecture is not supported by state-of-the-art

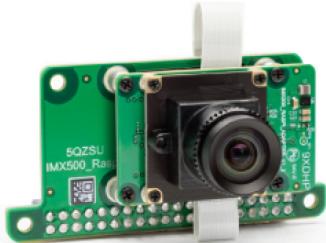


Fig. 1. Sony IMX500 development kit.

HW-NAS for commodity electronics [2, 7, 8, 10, 12–14, 16, 17], which require the user to specify the MCU’s RAM and Flash.

To overcome the problem, the end-user could run the HW-NAS multiple times, changing the amount of RAM and Flash so that the sum is always equal to the amount of SRAM available to the NPU. Considering that a run of HW-NAS can take up to 40,000 h [13], it could not be convenient.

Therefore, we propose a novel HW-NAS targeting in-sensor NPUs, for effectively supporting in-sensor computing. The proposed HW-NAS produces tiny Convolutional Neural Networks (CNNs) meant to run inside new-generation vision sensors featuring an NPU. The proposed HW-NAS provides state-of-the-art results on the Visual Wake Words dataset [6], a tiny machine learning benchmark [1, 3], while fitting the resource constraints of the new IMX500 Sony’s vision sensors, equipped with an NPU.

2 Proposal

The proposed HW-NAS inherits the overall design from [9]. Indeed, enhanced versions of both the optimization problem and the search strategy are adopted to meet the emergent needs of vision sensors equipped with an NPU. HW-NAS automatizes the process of finding a suitable neural architecture for performing a specific task on a given hardware. A HW-NAS has three hallmarks: the optimization problem used to find the best fit for the chosen hardware and the given task; the search space, i.e., the set of rules applied to build candidate architectures; and the search procedure, i.e., how the fittest architecture is chosen.

Equation 1 shows the new optimization problem P proposed in the present paper, where function f returns the maximum validation accuracy after three epochs of training. The constraint ϕ_M represents the peak memory occupancy of the network, including code, parameters and memory buffers. Thanks to the global constraint on the available memory, the algorithm can autonomously set the amount of memory reserved, respectively, for code and weights and for the buffers supporting inference.

$$P : \begin{cases} \max f(x) \\ \phi_M(x) \leq \xi_M \\ \xi_M > 0 \end{cases} \quad (1)$$

$$n_c = \begin{cases} k \\ \lceil (2 - \sum_{i=1}^{c-1} 2^{-i}) \cdot n_{c-1} \rceil \end{cases} \quad \begin{cases} c = 0 \\ c \geq 1 \end{cases} \quad (2)$$

The proposed HW-NAS seeks the best architecture inside a cell-wise search space, represented in Fig. 2 where candidates are built staking cells upon a bi-dimensional convolutional layer having k kernels. Staked cells are composed of a max pooling layer, halving the input resolution, followed by a bi-dimensional convolutional layer having the number of kernels k based on the number of previous cells c , as per Eq. 2, and a batch normalization layer followed by relu activation. The obtained features are then reduced by a global average pooling layer feeding a fully connected classifier with softmax activation, having the number of neurons equal to the number of classes of the problem. All convolutional layers have 3 by 3 kernels. Candidates can be conveniently described by the tuple (k, c) where k is the number of kernels used in the first convolutional layer and s is the total number of staked cells.

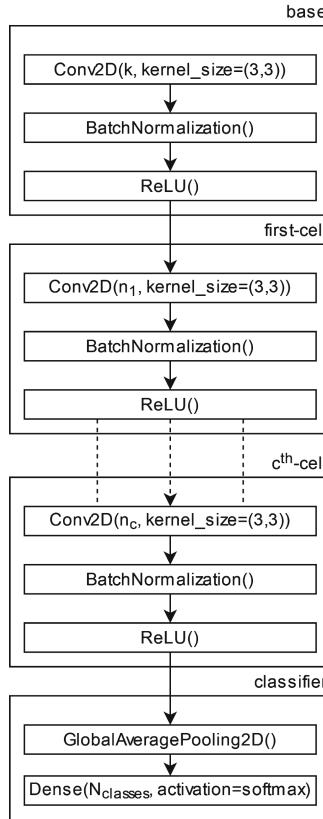


Fig. 2. Adopted cell-wise search space.

The search strategy consists of a bi-level optimization technique acting alternatively on k and s . The search starts with $k = 1$ kernels in the first layer. Given k , the algorithm increments the number of cells c until the corresponding $CNN(k, c)$ 1) satisfies the constraints imposed by 1 and 2) scores a validation accuracy $f(k, c)$ larger than that achieved with $CNN(k, c - 1)$. Then, the same process is completed with $k + 1$. If the best CNN obtained with $k + 1$ betters the best CNN obtained with k , the search continues by further incrementing k . Otherwise, the search stops.

3 Results

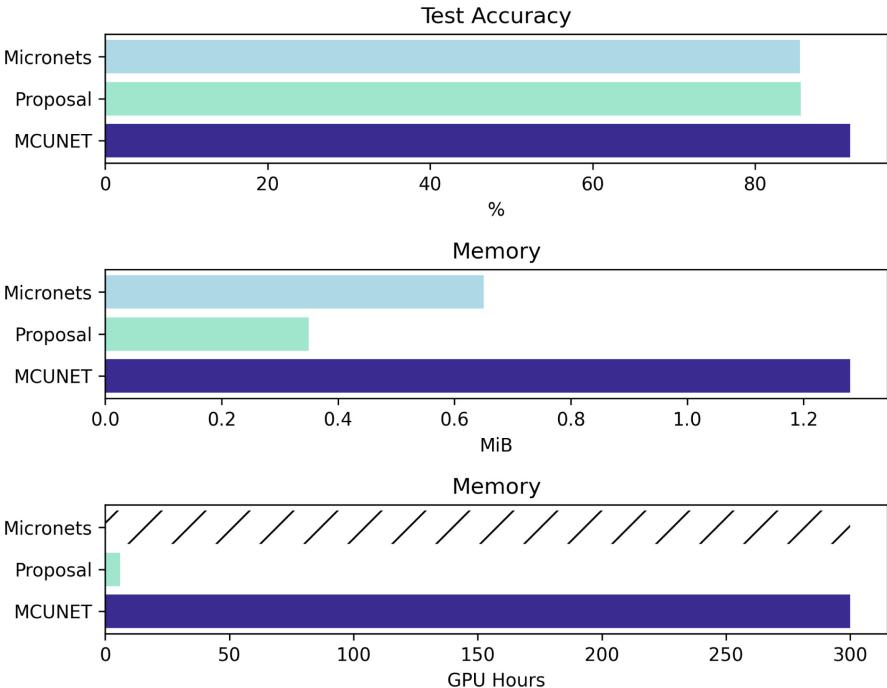


Fig. 3. Comparison with existing HW-NAS on VWV dataset. GPU hours are not available for Micronets.

The proposed method has been run on the Visual Wake Words dataset [6] with $180 \times 180 \times 3$ input resolution and with 8 MiB as global memory constraint which corresponds to the memory available to the NPU mounted inside the IMX500 vision sensor, using a laptop equipped with an Intel Core i7-11370H, 16 GiB of LPDDR4x RAM, and an NVIDIA GeForce RTX 3050 Ti with 4 GiB of dedicated GDDR6 RAM. The resulting architecture has been trained for 50 epochs with a

learning rate of 0.01 and a batch size of 128 using Adam optimizer [11]. Figure 3 shows the memory consumption and the test accuracy of the resulting model, as well as the ones of the best-performing models in terms of test accuracy, offered by state-of-the-art HW-NAS for MCUs, for comparison purposes.

As can be seen, the proposed method achieves a test accuracy comparable to Micronets' [2] model, but less than MCUNet [13]. At the same time, the proposed method is the most economical in memory consumption, showcasing a model 3.7 times smaller than MCUNet and 1.9 times smaller than Micronets. All of that in 5 h and 48 min, the smallest execution time among all, confirming that a small hand-crafted search space can provide state-of-the-art results in a short time [7].

References

1. Banbury, C., et al.: Mlperf tiny benchmark. arXiv preprint [arXiv:2106.07597](https://arxiv.org/abs/2106.07597) (2021)
2. Banbury, C., et al.: Micronets: neural network architectures for deploying tinyml applications on commodity microcontrollers. Proc. Mach. Learn. Syst. **3**, 517–532 (2021)
3. Banbury, C.R., et al.: Benchmarking tinyml systems: challenges and direction. arXiv preprint [arXiv:2003.04821](https://arxiv.org/abs/2003.04821) (2020)
4. Benmeziane, H., El Maghraoui, K., Ouarnoughi, H., Niar, S., Wistuba, M., Wang, N.: Hardware-aware neural architecture search: survey and taxonomy. In: IJCAI, pp. 4322–4329 (2021)
5. Bonazzi, P., Rüegg, T., Bian, S., Li, Y., Magno, M.: Tinytracker: Ultra-fast and ultra-low-power edge vision in-sensor for gaze estimation. In: 2023 IEEE SEN-SORS, pp. 1–4. IEEE (2023)
6. Chowdhery, A., Warden, P., Shlens, J., Howard, A., Rhodes, R.: Visual wake words dataset. arXiv preprint [arXiv:1906.05721](https://arxiv.org/abs/1906.05721) (2019)
7. Cui, J., Chen, P., Li, R., Liu, S., Shen, X., Jia, J.: Fast and practical neural architecture search. In: Proceedings of the IEEE/CVF International Conference on Computer Vision, pp. 6509–6518 (2019)
8. Garavagno, A.M., Ragusa, E., Frisoli, A., Gastaldo, P.: A hardware-aware neural architecture search algorithm targeting low-end microcontrollers. In: 2023 18th Conference on Ph. D Research in Microelectronics and Electronics (PRIME), pp. 281–284. IEEE (2023)
9. Garavagno, A.M., Ragusa, E., Frisoli, A., Gastaldo, P.: An affordable hardware-aware neural architecture search for deploying convolutional neural networks on ultra-low-power computing platforms. IEEE Sensors Lett. (2024)
10. Garavagno, A.M., Ragusa, E., Frisoli, A., Gastaldo, P.: Running hardware-aware neural architecture search on embedded devices under 512mb of ram. In: 2024 IEEE International Conference on Consumer Electronics (ICCE), pp. 1–2. IEEE (2024)
11. Kingma, D.P., Ba, J.: Adam: a method for stochastic optimization. arXiv preprint [arXiv:1412.6980](https://arxiv.org/abs/1412.6980) (2014)
12. Liberis, E., Dudziak, L., Lane, N.D.: μ nas: constrained neural architecture search for microcontrollers. In: Proceedings of the 1st Workshop on Machine Learning and Systems, pp. 70–79 (2021)
13. Lin, J., Chen, W.M., Lin, Y., Gan, C., Han, S., et al.: Mcunet: tiny deep learning on IoT devices. Adv. Neural. Inf. Process. Syst. **33**, 11711–11722 (2020)

14. Marchisio, A., Massa, A., Mrazek, V., Bussolino, B., Martina, M., Shafique, M.: Nascaps: a framework for neural architecture search to optimize the accuracy and hardware efficiency of convolutional capsule networks. In: Proceedings of the 39th International Conference on Computer-Aided Design, pp. 1–9 (2020)
15. Pau, D.P., Randriatsimiovalaza, M.D.: Electromyography gestures sensing with deeply quantized neural networks. In: 2023 IEEE International Conference on Metrology for eXtended Reality, Artificial Intelligence and Neural Engineering (MetroXRAINE), pp. 711–716. IEEE (2023)
16. Tan, M., et al.: Mnasnet: platform-aware neural architecture search for mobile. In: Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pp. 2820–2828 (2019)
17. Wu, B., et al.: Fbnnet: hardware-aware efficient convnet design via differentiable neural architecture search. In: Proceedings of the IEEE/CVF Conference on Computer Vision and Pattern Recognition, pp. 10734–10742 (2019)



Enhancing Vibration Inspection via Compressed Sensing Based on Embedded Phase Change Memories

Federica Zonzini^{1,2(✉)}, Francesco Zavalloni², Daniele Martinelli², Alessio Antolini^{1,2}, Eleonora Franchi Scarselli^{1,2}, Marco Pasotti³, and Luca De Marchi^{1,2}

¹ DEI Department, University of Bologna, 40136 Bologna, Italy

{federica.zonzini,alessio.antolini,eleonora.franchi,l.demarchi}@unibo.it

² ARCES, University of Bologna, 40136 Bologna, Italy

{francesco.zavalloni2,daniele.martinelli5}@unibo.it

³ STMicroelectronics, Agrate Brianza, Italy

Abstract. Analog In-memory Computing (AIMC) based on Embedded Phase-change Memory (ePCM) has the potential to outbreak the performances of sensor-near computing frameworks thanks to its unique capability to parallelize multiply-and-accumulate operations. The latter are, among the many others, at the basis of the Compressed Sensing (CS) theory. This work aims at exploiting the characteristics of an AIMC prototype based on an ePCM array, both designed in a 90-nm CMOS technology by STMicroelectronics, for the purpose of CS-driven acceleration data compression in the context of vibration inspection. This application domain, indeed, necessitates from novel architectures and computing paradigms in order to be compatible with real-time and energy-efficient implementations. To this end, we have evaluated the impact of input datum quantization and conductance drift on the quality of the reconstructed spectra, prioritizing its suitability for damage detection, along with its electrical and computational performances.

Experimental analyses conducted on a representative laboratory testbed revealed that the exploitation of an ePCM-based AIMC prototype can be 4× less power demanding and 6× faster than standard 32-bit MCU architectures. Importantly, spectral peak identification necessary for structural assessment is demonstrated even in presence of deeply quantized (8 bit) data and against the influence of cell drift.

Keywords: Analog In-memory Computing · Compressed Sensing · Embedded Phase Change Memory · Vibration Inspection

1 Introduction

Structural Health Monitoring (SHM) based on vibration data is the preferable method for the inspection of dynamic systems [1]. The presence of relevant

shifts in the peak spectral values can be interpreted as a symptom of structural deterioration. However, novel approaches and computing paradigms are urged, necessary to fasten the diagnostic process and support energy-efficient implementations [2]. Data compression offers a means for system-level optimization and is suitable for extreme-edge deployment via Compressed Sensing (CS) thanks to its algebraic-friendly nature. CS resorts to a matrix vector multiplication to shrink data dimension, an operation which only requires multiply and accumulate (MAC) instructions [3]. In this work, we explore the implementation of CS-based data compression in the context of vibration SHM exploiting the superior MAC capabilities of Analog In-memory Computing (AIMC) based on embedded Phase Change Memories (ePCM). Notably, for the first time to the best of our knowledge, this represents the first exploratory study about the applicability of AIMC as an accelerator for inspection system encompassing also the effect of low bit-width quantization of the input datum and conductance drift, which are unavoidable in real field deployments.

The rest of the paper is organized as follows. In Sect. 2, the defining characteristics of the target ePCM array are described, along with the working principles at the basis of the CS theory. Specific attention is dedicated to the mapping and quantization procedure of the encoding stage, such that it is compatible with the target device. Then, an experimental section (Sect. 3) related to the health inspection of a laboratory testbed (steel beam) is presented, confirming the superiority of the ePMC-based solution. Conclusions and future perspectives end the manuscript.

2 Quantized CS Based on ePCM

2.1 PCM-Based AIMC

AIMC has established as a valid solution among hardware accelerators for data-centric applications. The advantages of power efficiency in AIMC architectures arises typically from the massive parallelism of a dense array of millions of memory devices performing computations [4]. However, the AIMC approach can only offer limited precision due to the analog nature of the operations performed within the memory. The most common operation suitable for AIMC is the Matrix-Vector Multiplication (MVM). Analog computing elements can be used to perform MVM operations exploiting the possibility to map a two-dimension matrix into a physical memory array. Peripheral circuitry is devoted to the execution of sums and multiplications typically exploiting Ohm's and Kirchhoff's laws.

The ePCM technology has been gaining attractiveness in this context thanks to its multilevel storage capability, which opens up the possibility to store MVM coefficients with high storage density. Multilevel intermediate PCM conductance levels for AIMC applications can be achieved by applying sequences of current pulses within program-and-verify algorithms.

During computation, PCM cells are typically read at constant read voltage, hence, the information is provided in the form of a conductance g for each stored

matrix coefficient. As a result, conductance non-idealities that characterize PCM cells directly affect the analog output precision. Among these, conductance time drift is one of the most significant, so that various strategies aimed at its mitigation have been proposed at different levels of abstraction. The conductance time drift is attributable to amorphization and relaxation phenomena of the cells crystal lattice, and manifests itself as a random decrease of the conductance of the memory element, according with the following power-law in time [5]

$$g(t) = g_0 \left(\frac{t}{t_0} \right)^{-\nu} \quad (1)$$

where g_0 is the conductance at arbitrary time t_0 , and ν is the drift coefficient, which is cell-to-cell variable and slightly depends on g_0 .

Here, we specifically evaluate this aspect for the task of vibration data compression via CS taking into consideration the specificity of the AIMC prototype in [6]. It consists of a peripheral unit interfaced with a 128 kB ePCM array in a 90-nm STMicroelectronics CMOS technology [7], which performs one-step signed MAC operations. Elements of the input vector are converted into voltages, whereas the MAC coefficients are obtained through the conductances stored in a wordline (WL) of the ePCM array. A 8-bit length quantization of the inputs has been chosen to stress the achievable performance of the proposed testchip and to match the reduced bit precision of the ADC employed to sample the MAC results.

2.2 Basics of CS

The theoretical assumption behind CS is that the class of signals to be processed in sparse in a specific domain [3]. In mathematical terms, if $x \in \mathbb{R}^n$ represents the generic signal to be compressed, a sparsity basis Φ should exist such that the projection $x = \Phi \times c$ contains at most k non null coefficients c [8] (x is said to be k -sparse in this case). The sparsity condition perfectly applies to signals collected from structures in dynamic regime, since their spectral profile is characterized by the presence of a few and localized frequency peaks, corresponding to the natural modes of vibrations, that carry most of the total structural energy [9]. Coherently, the Discrete Cosine Transform (DCT) can be used as a suitable sparsifying basis. Under these circumstances, it is possible to compress vibration data (eventually, below the Shannon's theorem) with a negligible loss of information [10].

The entire CS workflow consists of two steps: the encoding, responsible for the actual data reduction, and the decoding, aimed at reconstructing the original raw signal. Data compression is performed by a matrix-vector multiplication $y = A \times x$, where $A \in \mathbb{R}^{m \times n}$ is known as the *Sensing Matrix*. Since the number of rows, m , is smaller than the number of columns, n , the result of this operation is a new vector $y \in \mathbb{R}^m$ with a smaller number of components according with the compression ratio $\rho = \frac{n}{m}$. In such a framework, designing the proper sensing matrix is crucial to reach the best trade-off between the quality of the retained

information and the compression depth. In vibration-based inspection, which aims at monitoring frequency-related quantities, adapted methods based on the maximization of the signal energy can profitably be exploited. In particular, the Model-assisted Rakeness-based CS (MRak-CS) strategy in [1] can be particularly effective thanks to its conservative nature, i.e., it allows to design the spectral profile of the monitored structure without incurring in overfitting with respect to one particular structural configuration. For this reason, it has been exploited as the preferable design method.

The reconstruction process works by estimating a proxy of the original time series, let's call it $\hat{x} \in \mathbb{R}^n$, and its sparse support. Even if multiple algorithms can be adopted for the purpose, methods postulating a convex optimization problem are among the most effective. One of them is the Basis Pursuit Denoising Problem, which can be formulated as [11]:

$$\begin{aligned} \hat{x} = \min_{\tilde{x}} \quad & \|\tilde{x}\|_1 \\ \text{such that: } & \|y - A \times \tilde{x}\|_2 \leq \sigma \end{aligned} \quad (2)$$

where the term σ takes into account the noise in the data while forcing tolerance on the residual and \tilde{x} is used to define all the possible solutions $\in \mathbb{R}^n$ that satisfy the constraints.

In this work, emphasis is given to the optimization of the encoder, which is parallelized through an ePCM array, while standard architectures and techniques are used for decompression. More specifically, the decoder relies on the SPGL1 solver, which has been selected because of its capability to deal with large-scale one-norm regularized least squares [12].

2.3 Processing Flow: from Encoding to Diagnostics

As a preliminary proof-of-concept, the entire processing framework (depicted in Fig. 1) has been simulated at a software level taking into consideration both the non-idealities introduced by the ePCM array (i.e., the drift) and the noise caused by the quantization of the input datum.

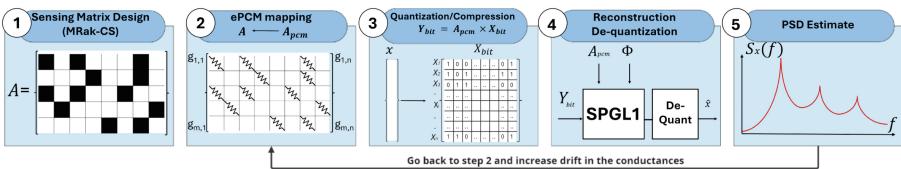


Fig. 1. Processing flow mapping CS encoder on the ePCM array while taking into consideration quantization and drift.

The first step (Step 1) pertains to the generation of the sensing matrix A given a prescribed compression ratio and the spectral signature of the structure under

analysis; the latter is a mandatory *a priori* information for the applicability of the MRak-CS method in [1]. To reduce the complexity of the following compression stage while minimizing the power consumption of the cells, antipodal $a_{i,j} = \{-1, +1\}$ or binary $a_{i,j} = \{0, +1\}$ values of A can be applied.

Since each entry of the sensing matrix will be implemented as a conductance value of an ePCM array (Step 2), it is necessary to examine how the reconstruction phase of CS performs in the presence of the device non-idealities. Consequently, a conductance target g can be selected to implement the non-zero elements of the sensing matrix. To this end, mapping is achieved after selecting one current value I and normalizing its value by its maximum. In this way, the ratio between the current and its maximum is comparable, with good approximation, to a value of normalized conductance as the reference voltage V_{ref} remains constant, i.e., $g(t) = \frac{I(t)}{V_{ref}}$. Then, a single instance of the sampling matrix A_{pcm} can be generated from A by multiplying all coefficients $a_{i,j}$ by a randomly selected conductance value among those programmed for the chosen current level.

The quantization/compression stage (Step 3) is quite straightforward: each frame x of n samples is converted into a vector x_j of b bits, where $b = \{8, 16\}$, resulting in a matrix $X_{bit} \in \mathbb{R}^{n \times b}$. The compressed variant $Y_{bit} \in \mathbb{R}^{\frac{n}{\rho} \times b}$ is obtained as $Y_{bit} = A_{pcm} \times X_{bit}$. Then, bit-wise reconstruction (Step 4) is implemented via SPGL1 returning an estimate of the input sample \hat{x}_j , followed by a de-quantizer necessary to restore the complete signal \hat{x} . Finally, vibration analysis (Step 5) is implemented by computing the Power Spectral Density (PSD) of \hat{x} . Step 2–5 can be repeated using different conductances measured at regular intervals after programming, so that every entry of A_{pcm} will drift across time and move towards 0. In this way, it is possible to evaluate the effect of the drift on the spectrum of the compressed-reconstructed signal.

3 Experimental Validation

PCM Cells Characterization. In order to properly analyze the impact of PCM devices in the proposed framework, a set of 76 PCM cells was programmed to a conductance target g , which represents the non-zero elements of the sensing matrix. The employed programming method of PCM cells consists in a SET Stair-Case (SSC) strategy [13]. The procedure begins by setting the desired conductance level along with an arbitrary variance, δg . Initially, a RESET pulse is applied to the memory cell. Subsequently, a series of incremental SET pulses is invoked. After each pulse, the conductance of the cell is measured. If the conductance falls within the predefined range, the programming process concludes. In case the conductance exceeds the desired range, the process restarts with the RESET pulse. Conversely, if the conductance is below the desired range, the cell is stimulated with another SET pulse with increased amplitude to get higher conductance. Then, each PCM cell was measured at constant voltage over a period of 49 h at room temperature with a sampling period of 30 min, which allows to estimate both the conductance evolution due to the effect of drift and

the variability of each cell, for a total amount of 99 cell measurements. The monitored normalized conductance of a sample cell is reported in Fig. 2, where it is evident its decreasing trend in time.

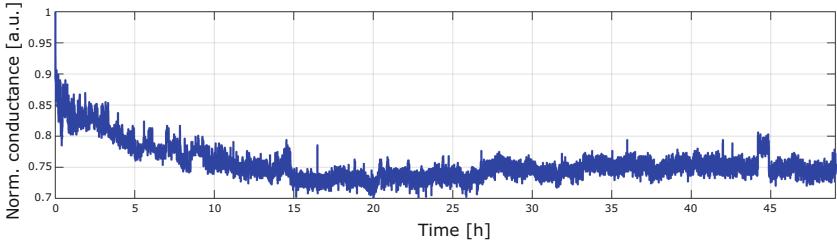


Fig. 2. Normalized conductance of a sample PCM cell monitored over 49 h after the programming phase.

Materials and Methods. Experiments have been conducted on a simply supported steel beam under ground motion excitation. The structure has been damaged by adding masses of different weight ($MA = 1.0\text{ kg}$ and $MB = 1.8\text{ kg}$) at a distance of 20 cm from the support. For each of the three configurations, four compression levels $\rho = \{4, 6, 8, 10\}$ have been investigated while the MRak-CS method in [1] has been exploited to generate the compression matrix in antipodal form. The absolute values of the corresponding entries have been mapped using the aforementioned set of cells, whereas their signs have been assumed as ideal thanks to their intrinsic binary implementation, as described in [6]. The corresponding entries have been mapped into the ePCM array through the conductance of two PCM cells. One is related to the sign of the associated weight and is programmed in a binary fashion, the other one represents the weight absolute value and it is programmed at a low conductance level.

Results. Representative results (in nominal conditions) are provided in the waterfall plot of Fig. 3. In this figure, the vertical axis is divided into 4 main blocks (one per compression ratio ρ), showing, in cascade, the high-level energy distribution computed for the CS-decoded signals for each of the 99 measurements of the ePCM cell (49 h) to account for the conductance drift. As can be seen, the whole framework is resilient to the effect of the cells conductance drift, as the PSD estimation and the location of the most energetic peaks (those vertical lines in yellow) is not sensibly affected in time. This is of paramount importance since SHM systems are supposed to be permanently installed on the target asset, thus demanding for robust processing solution which could ensure reliable output independently from system aging.

Starting from this preliminary outcome, the effect of low bit-width has been appraised. To this end, aggregated results depicting the spectra for the three

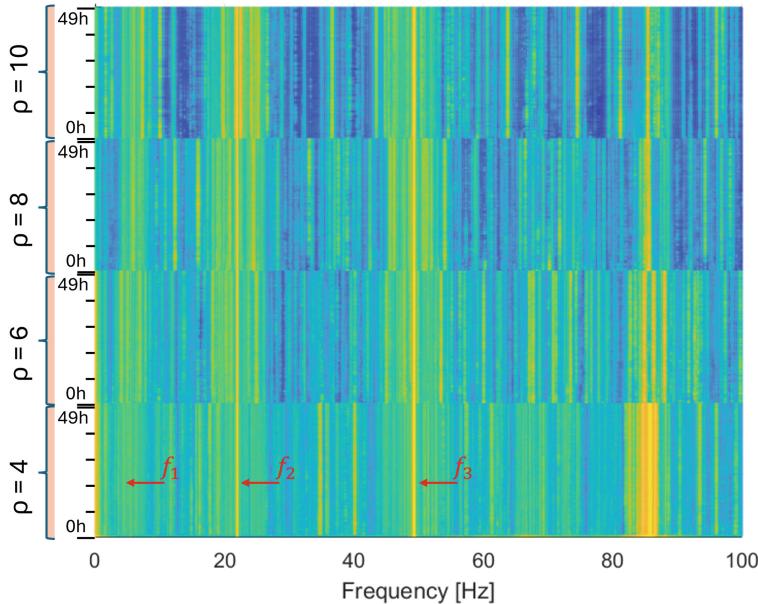


Fig. 3. Waterfall of the spectra for the nominal condition with different ρ over the 49 h of cell measurements per compression level.

structural configurations with non quantized (left) and quantized (right) data are provided in Fig. 4. More specifically, Fig. 4(b) proves that even considering a 8-bit quantization it is possible to retrieve changes in the frequency peak location if compared with the original, non quantized setting (Fig. 4(a)). Interestingly, similar evidence concerning the negligible impact of drift can be noticed also for the case Damage MA and Damage MB, as testified by the presence of clearly localized and constant frequency peaks in the related waterfalls. From a mere diagnostic perspective, it is worth mentioning that the proposed ePCM-based CS workflow preserves full damage detection capability, here intended as the possibility to advertise changes in the location of the three most energetic frequency components (located at about $f_1 = 6$ Hz, $f_2 = 22$ Hz, and $f_3 = 49$ Hz, respectively). Indeed, as highlighted by the red arrows, all of the three peaks reduces when moving from the reference to the unhealthy configurations, with frequency f_3 eventually disappearing in presence of Damage MB. Importantly, such variations are due to the actual geometrical and physical properties of the structure and do not depend on artifacts or inaccuracies generated by the non-idealities of the computing architecture.

Finally, the time and energy performances have been compared with those obtained by deploying the standard CS processing flow on an STM32L496 MCU based on an ARM-Cortex M4 processor. Results, summarized in Table 1, show

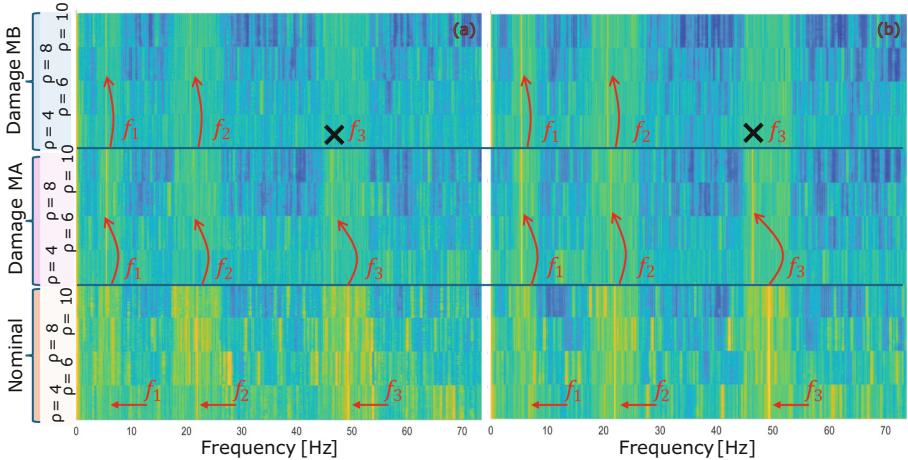


Fig. 4. Aggregated waterfall of the spectra for different damage configurations and compression levels in case of non quantized (a) and quantized (b) data. Frequency shifts are highlighted with arrows and crosses.

that, despite being the energy per operation required by the ePCM implementation comparatively higher and the clock rate lower, the very low number of operations to be performed (95% lower) makes it 6× faster and 4× more energy efficient.

Table 1. Time/energy performances of ePCM-based CS compared with a conventional MCU deployment.

Computing platform	# op.	F_{clk} [MHz]	Energy/op [nJ/op]	Energy [μ J]	Exec. time [ms]
ARM-Cortex (STM32L496)	98176	80	1.093	143.141	1.227
ePCM-based AIMC	1024	5	33.5	34.304	0.205

4 Conclusions and Outlooks

In this work, the possibility to employ an ePCM array to enhance vibration data compression based on CS has been explored. A dedicated quantization procedure has been proposed to entail practical difficulties, such as the low bit-width of the input datum and the effect of drift affecting the PCM cells over time. Results conducted on a laboratory testbed revealed that vibration data can effectively be compressed via the ePCM encoder, showing a negligible loss in the quality of the reconstructed spectra if compared with non quantized solutions. Importantly, in the proposed framework, it has been found that drift minimally

impacts on the frequency peak locations exploited for diagnostics. Finally, significant improvement in time and energy has been prospected if compared with standard computing architectures.

In future studies, actual deployment on the target ePCM array will be tested, as well as real we will benchmark more complicated application scenarios.

References

1. Zonzini, F., Zauli, M., Mangia, M., Testoni, N., De Marchi, L.: Model-assisted compressed sensing for vibration-based structural health monitoring. *IEEE Trans. Ind. Inf.* **17**(11), 7338–7347 (2021)
2. Zonzini, F., Dertimanis, V., Chatzi, E., De Marchi, L.: System identification at the extreme edge for network load reduction in vibration-based monitoring. *IEEE Internet Things J.* **9**(20), 20467–20478 (2022)
3. Donoho, D.L.: Compressed sensing. *IEEE Trans. Inf. Theory* **52**(4), 1289–1306 (2006)
4. Haensch, W., Gokmen, T., Puri, R.: The next generation of deep learning hardware: analog computing. *Proc. IEEE* **107**(1), 108–122 (2019)
5. Ielmini, D., Sharma, D., Lavizzari, S., Lacaita, A.L.: Physical mechanism and temperature acceleration of relaxation effects in phase-change memory cells. In: 2008 IEEE International Reliability Physics Symposium, pp. 597–603 (2008)
6. Antolini, A., et al.: An embedded pcm peripheral unit adding analog mac in-memory computing feature addressing non-linearity and time drift compensation. In: ESSCIRC 2022-IEEE 48th European Solid State Circuits Conference (ESSCIRC), pp. 109–112 (2022)
7. Carissimi, M., et al.: An extended temperature range epcm memory in 90-nm bcd for smart power applications. In: ESSCIRC 2022-IEEE 48th European Solid State Circuits Conference (ESSCIRC), pp. 373–376 (2022)
8. Kutyniok, G.: Theory and applications of compressed sensing. *GAMM-Mitteilungen* **36**(1), 79–101 (2013)
9. Zonzini, F., Girolami, A., De Marchi, L., Marzani, A., Brunelli, D.: Cluster-based vibration analysis of structures with gsp. *IEEE Trans. Ind. Electron.* **68**(4), 3465–3474 (2020)
10. Peyre, G.: Best basis compressed sensing. *IEEE Trans. Signal Process.* **58**(5), 2613–2622 (2010)
11. van den Berg, E., Friedlander, M.P.: Probing the pareto frontier for basis pursuit solutions. *SIAM J. Sci. Comput.* **31**(2), 890–912 (2008)
12. van den Berg, E., Friedlander, M.P.: SPGL1: A solver for large-scale sparse reconstruction (2019). <https://friedlander.io/spgl1>
13. Antolini, A., et al.: Characterization and programming algorithm of phase change memory cells for analog in-memory computing. *Materials* **14**, 1624 (2021)



Towards Energy-Efficient Smart Sensing Nodes for Automatic Structural Health Monitoring

Edoardo Ragusa¹, Federica Zonzini^{2(✉)}, Paolo Gastaldo¹, Rodolfo Zunino¹,
and Luca De Marchi²

¹ DITEN, University of Genoa, Genova, Italy

² DEI and ARCES, University of Bologna, Bologna, Italy

federica.zonzini@unibo.it

Abstract. Moving data analytics to the extreme edge demands for the accurate selection of the trade-off between computational complexity and power requirements. This is crucial for Structural Health Monitoring (SHM) systems where sensors are typically battery-operated and equipped with resource-constrained processors. This paper considers the possibility to perform inference by using just one sensing node, hosting a tiny Convolutional Neural Network (CNN), for the prediction of the health status of the structure from vibration data. Emphasis is given to the importance of selecting the optimal sampling parameters (length of the acquisition window and sampling frequency). Experiments on the Z24 bridge benchmark show that a tiny CNN can achieve classification scores comparable with state-of-the-art results (>96%), while avoiding data transmission. An in-depth energy profiling has been conducted after deploying the sought model on a wireless node based on an STM32L496 processor and an accelerometer. It reveals that the selection of a proper duration of the acquisition time (half than typical duration) can halve the energy consumption of the sensor per hour (from 130 mJ/h down to 31 mJ/h) while introducing a minimal drop in the prediction accuracy (less than 1%).

Keywords: Energy profiling · Smart Sensors · Tiny CNNs · Vibration inspection

1 Introduction: Background and Motivations

Structural Health Monitoring (SHM) systems can benefit largely from extreme-edge data processing thanks to the better management of the available computing resources and data volume [1,2]. Performing automatic SHM, on-site, using battery-powered devices, requires minimizing energy requirements for data acquisition, processing, and communications [3]. Implementing prediction

E. Ragusa and F. Zonzini—Equally contributed to this work.

directly on the sensing nodes cancels transmission costs but imposes hard constraints on the power requirements and computational complexity of the algorithms [4]. Importantly, besides inference, sampling parameters have to be chosen properly to optimize the entire system performance in support of the data analytics and data management units. Indeed, even if the power spent in sensing mode is, in principle, minimal if compared with data transmission or analytics, prolonging sampling over long time intervals can amount to a non negligible part of the overall expenditure per monitoring cycle [5].

In this work, we specifically evaluate the impact of the sampling frequency and length of the acquisition time on the balance between energy budget and damage detection capabilities for vibration diagnostics based on a tiny Convolutional Neural Network (CNN). Our investigations are supported by experimental analyses conducted on a real field bridge dataset.

The remainder of the paper is organized as follows. In Sect. 2, aspects related to the joint evaluation of sensing and inference are elucidated, discussing the importance of selecting the diagnostic model and the policy to determine the optimal sampling parameters. Section 3 deals with the description of the experimental scenario, related to a well-known bridge use case: first, classification performances of different solutions are presented; then, energy profiling measured after deployment on a custom acceleration sensor is presented. Conclusions and future perspectives end the manuscript.

2 Energy Efficient Sensing Node with Sampling and CNN

Decentralized SHM systems have proven to be highly effective thanks to the optimal balancing of the involved computational resources. Sensor-near diagnostic, in fact, offers a dual strategy for system level optimization since it can implement both data compression and energy minimization, reducing the amount of information to be transmitted (eventually, only one bit - safe/unsafe - is sufficient) at the price of a small processing overhead for the sensing unit. To support such functionality, the sensing node should be equipped with four main constituting blocks, namely, an accelerometer for sensing, a microcontroller unit (MCU) for analytics and overall system management, a transmission module for communication, and a battery ensuring plentiful energy autonomy.

In this scenario, both inference and sensing are critical since they can equally impinge on key performance parameters, first among all the memory requirements of the node and the duty cycling compatible with real-time and long-term operations. This is schematically depicted in the high-level sketch in Fig. 1, where it is emphasized how sensing (blue block) and its defining parameters contribute to the power consumption and memory occupation, as well as to the model size and inference time (green block).

Concerning structural health prediction, machine learning proved effective in many configurations [6, 7]. In particular, deep neural networks obtained state-of-the-art (SOTA) results [8]. However, an appropriate model architecture has to be selected, whose complexity can also fit the limited computational capabilities

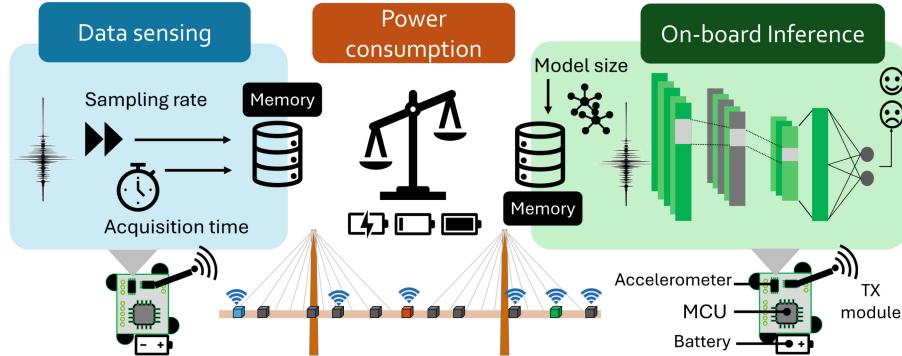


Fig. 1. High level representation of the application scenario

of low-end devices [9]. In our approach, a network based on 1D-CNN is proposed since tiny 1D-CNN can purposely trade-off computing costs and generalization performance [8]. More specifically, the chosen model (represented in the green-shaded box of Fig. 1) consists of a simple architecture with two 1D-CNN layers with 5 and 3 filters, with a max-pooling layer following the first convolutional layer. A global average pooling layer and the output classification layer complete it. The proposed architecture has been selected based on the output of previous research topologies [8, 10] proving that convolution in the time domain can appropriately extract meaningful diagnostics information from vibration time histories.

On the other hand, sampling frequency and acquisition duration are crucial parameters: long sampling time at high frequency conveys fine-grained information, but inflated energy and memory consumption [11, 12]. This configuration is usually preferred for stiffened structures, showing limited vibration motion, which can be characterized by tightly coupled and/or very low frequency vibration modes [13]. Thus, having a huge number of time samples over long observation windows can be beneficial to reach detailed frequency resolution [14]. Note that, this condition applies to the majority of civil infrastructures, such as bridges and residential buildings. Consequently, oversampling approaches and very long acquisition intervals are preferred within the SHM community to grant enough temporal and frequency resolution [15]. Here, we aim to include these sensing-related parameters at the neural network design stage by proposing a joint evaluation of the sensing and inference stages.

3 Experimental Validation

3.1 Materials and Methods

Dataset. Acceleration signals from the Z24 highway viaduct in Switzerland have been used for analyses. A sensor network consisting of eight force-balance-type FBA-11 accelerometers (see Fig. 2) was installed on the facility before its

demolition, getting data over a monitoring period of one year. In its pristine configuration, each sensing unit was configured to work with a sampling frequency of 100 Hz gathering 32768 samples for a total acquisition window of nearly 11 min. The dataset contains 5651 measurements, 4922 related to normal conditions and 729 to defective configurations.

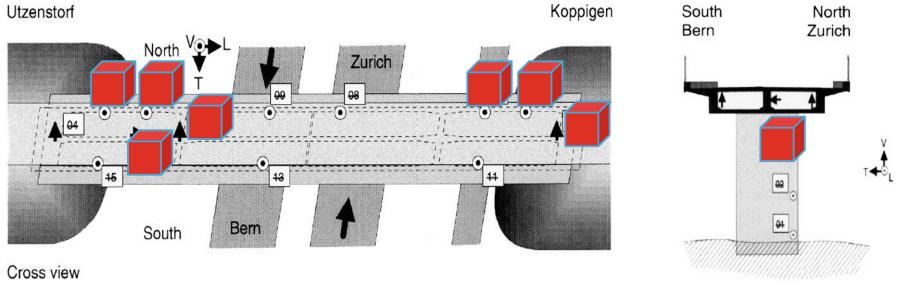


Fig. 2. Sensor installation plan on the Z24 bridge.

Evaluation Process. Eight different 1D-CNNs, one per sensing unit, have been trained after reshaping the input datum in successive frames of 512 samples necessary to shrink the complexity in handling, in practical scenarios, long time series. Two different sampling frequencies, $F_{s2} = 30\text{ Hz}$ and $F_{s1} = 50\text{ Hz}$ have been considered; the former, in particular, corresponds to the Nyquist limit given the fact that the uppermost frequency of vibration of interest is proximal to 15 Hz. Alongside, two values for the observation windows, $T_1 = 11\text{ min}$ and $T_2 = 5.5\text{ min}$, have been explored to account for long and modest acquisition times for the considered class of structures. In total, three different configurations of these two parameters have been explored: ($F_{s1}-T_1$) which equates the original sensing settings, ($F_{s1}-T_2$) that reduces the time duration, and ($F_{s2}-T_1$) which diminishes the data points by lowering the sampling rate.

Classification Results. Figure 3 reports the experimental results in terms of standard classification scores computed on the test set for the sensor installed on the central pillar of the bridge which, thus, experiences the lowest vibration response and can be considered as a worst-case sensing point. The comparison is a distributed solution, using information from all eight sensors, that sets the SOTA [8] in terms of generalization performance. When sampling settings used in previous works are imposed ($F_{s1}-T_1$), the performance is near to the SOTA. Comparing the effect of sampling frequency reduction with acquisition time decrement, the latter ($F_{s1}-T_2$) is more relevant since it leads to a more significant deterioration of 1% on average still remaining stably above 96% for all metrics.

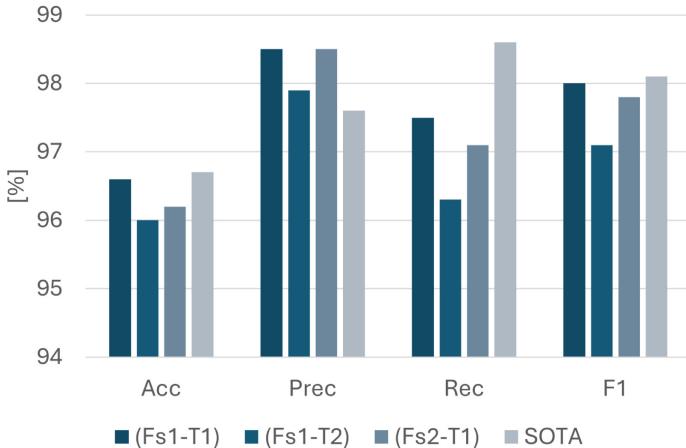


Fig. 3. Classification scores for the three considered sensing configurations compared with the state-of-the-art.

3.2 Model Deployment and Energy Profiling

Once the effect of sampling frequency/time has been ascertained, a cost-benefit analysis has been executed by deploying the sought model on the wireless sensor in [16]. The node, represented in Fig. 4(a), is equipped with an SM32L496 MCU based on an ARM-Cortex M4 processor, it integrates an high-precision ADXL355 accelerometer and transmits data via the 802.15.4 protocol through the Digi XBee 3 module. Two different quantization strategies have been considered for the sake of model conversion into an MCU-compliant format: full float and integer-only data. Energy consumed in four operative modes (sleep, idle, acquisition, and inference) is summarized in the bar chart of Fig. 4(b). As can be seen, the expenditure due to inference and acquisition is almost balanced for the float model; conversely, on-board data processing can become negligible with respect to sampling in case integerization is exploited for the sake of time reduction. This observation applies independently from the considered combination of parameters, with the model ($F_{s1}-T_2$) pertaining to the shorter acquisition window being the most energy efficient since it requires only 31 mJ/h compared with 130 mJ/h of the full model. Summing together the classification and energy analyses, outcomes suggest that a reduction of the time duration can lead to the best compromise between energy consumption and network computational complexity, still preserving the damage detection capabilities of the entire SHM system.

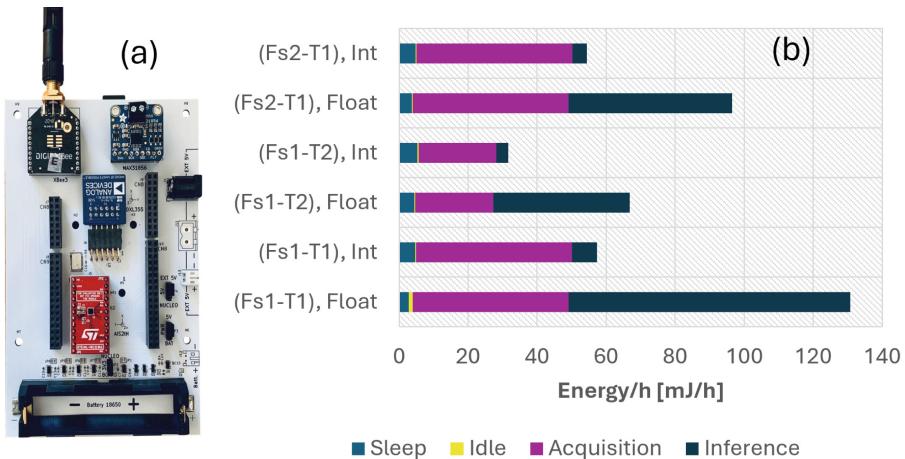


Fig. 4. (a) Prototype wireless accelerometer and (b) Energy profiling and cost-benefit analysis of the investigated sensing/inference strategies after deployment.

4 Conclusions

This work tackled the need for joint optimization of the sensing and inference stages in the context of sensor-near vibration inspection. In particular, it has been verified how a reduction of the sampling rate and/or the length of the acquisition window can affect the classification scores while favoring the memory requirements, computation time, and power expenditure. A tiny CNN architecture has been trained, tested, and deployed on a custom accelerometer sensor for the purpose of structural monitoring directly from vibration time series. Experimental tests conducted on the Z24 bridge revealed that shortening the acquisition time could be a more favorable approach if compared with conventional strategies (high rate, long time), improving energy efficiency by more than 4x while suffering from a minor drop in accuracy (less than 1%). Future explorations will focus on more complicated scenarios (e.g., industrial settings implicitly characterized by higher rates) as well as encompass search space procedures to define the optimal parameters.

References

1. Tokognon, C.A., Gao, B., Tian, G.Y., Yan, Y.: Structural health monitoring framework based on internet of things: a survey. *IEEE Internet Things J.* **4**(3), 619–635 (2017)
2. Scuro, C., Sciammarella, P.F., Lamonaca, F., Olivito, R.S., Carni, D.L.: IoT for structural health monitoring. *IEEE Instrument. Meas. Maga.* **21**(6), 4–14 (2018)
3. Zonzini, F., Dertimanis, V., Chatzi, E., De Marchi, L.: System identification at the extreme edge for network load reduction in vibration-based monitoring. *IEEE Internet Things J.* **9**(20), 20467–20478 (2022)

4. Saha, S.S., Sandha, S.S., Srivastava, M.: Machine learning for microcontroller-class hardware: a review. *IEEE Sensors J.* **22**(22), 21362–21390 (2022)
5. Morin, E., Maman, M., Guizzetti, R., Duda, A.: Comparison of the device lifetime in wireless networks for the internet of things. *IEEE Access* **5**, 7097–7114 (2017)
6. Favarelli, E., Giorgetti, A.: Machine learning for automatic processing of modal analysis in damage detection of bridges. *IEEE Trans. Instrum. Meas.* **70**, 1–13 (2020)
7. Ni, F., Zhang, J., Noori, M.N.: Deep learning for data anomaly detection and data compression of a long-span suspension bridge. *Comput.-Aided Civil Infrastruct. Eng.* **35**(7), 685–700 (2020)
8. Ragusa, E., Zonzini, F., Gastaldo, P., De Marchi, L.: Combining compressed sensing and neural architecture search for sensor-near vibration diagnostics. *IEEE Trans. Ind. Inf.* (2024)
9. Biglari, A., Tang, W.: A review of embedded machine learning based on hardware, application, and sensing scheme. *Sensors* **23**(4), 2131 (2023)
10. Zonzini, F., Ragusa, E., De Marchi, L., Gastaldo, P.: Evaluating the effect of intrinsic sensor noise for vibration diagnostic in the compressed domain using convolutional neural networks. In: International Conference on Applications in Electronics Pervading Industry, Environment and Society. Springer, Heidelberg (2023)
11. Sadeghi, N., D'Antuono, P., Noppe, N., Robbelein, K., Weijtjens, W., Devriendt, C.: Quantifying the effect of low-frequency fatigue dynamics on offshore wind turbine foundations: a comparative study. *Wind Energy Sci. Discuss.* **1–20**, 2023 (2023)
12. Gholizadeh, N., Katebi, J.: Fully data-driven model for increasing sampling rate frequency of seismic data using super-resolution generative adversarial networks. arXiv preprint [arXiv:2402.00153](https://arxiv.org/abs/2402.00153) (2024)
13. D'Antuono, P., Weijtjens, W., Devriendt, C.: On the minimum required sampling frequency for reliable fatigue lifetime estimation in structural health monitoring. how much is enough? In: European Workshop on Structural Health Monitoring, pp. 133–142. Springer, Heidelberg (2022)
14. Brincker, R., Ventura, C.: Introduction to Operational Modal Analysis. John Wiley & Sons, Hoboken (2015)
15. Zonzini, F., Girolami, A., De Marchi, L., Marzani, A., Brunelli, D.: Cluster-based vibration analysis of structures with gsp. *IEEE Trans. Ind. Electron.* **68**(4), 3465–3474 (2020)
16. Zauli, M., et al.: A novel smart sensor node with embedded signal processing functionalities addressing vibration-based monitoring. In: European Workshop on Structural Health Monitoring, pp. 1000–1008. Springer, Heidelberg (2022)



A Multi-parameter Sensing Device for Vital Signs Monitoring

Chiara Botrugno^(✉), Elisabetta Leogrande, Teresa Natale,
and Francesco Dell’Olio

Micro Nano Sensor Group, Polytechnic University of Bari, Bari, Italy
{chiara.botrugno,francesco.dellolio}@poliba.it,
{e.leogrande1,t.natale}@phd.poliba.it

Abstract. In recent years, significant advances in digital health made possible to provide more personalized and timely care, and health systems to become more efficient. With this study, we propose a multi-parameter device, at a prototypal level, which represents a convenient and efficient solution in order to accurately monitor health and collect vital data: it is able to return blood pressure values, heart rate, blood oxygen saturation levels and body temperature, relying only on two different sensors, multi-wavelength photoplethysmography (PPG) and thermal camera, combined with AI algorithms. The performances are promising, with an average relative error of less than 5% for heart rate and blood saturation, and a Mean Absolute Error of 5.08 ± 8.83 mmHg and 4.37 ± 7.08 mmHg for systolic and diastolic pressure respectively. The MLX90640 thermal camera accurately measured patients body temperature in a non-invasive and continuous manner, with a maximum absolute error equal to 0.2°C .

Keywords: vital signs monitoring · photoplethysmography · thermal camera

1 Introduction

Digital health is one of the newest frontiers in healthcare innovation and vital sign monitoring is one of its main focuses: it uses easily integrated equipment to provide continuous and remote control over physiological data, eliminating the need for invasive procedures or hospital stays. Photoplethysmography (PPG) is a valuable non-invasive technique for monitoring vital parameters, as it allows for the continuous measurement of heart rate and blood oxygen saturation levels. By analyzing PPG signals, healthcare providers can detect irregularities in cardiovascular function, aiding in the early diagnosis and management of conditions such as arrhythmias and hypoxemia. Furthermore, PPG approach for optical pulse detection can be used in many wearable devices to monitor changes in blood volume in the vascular bed beneath the skin. Heart rate, blood oxygen saturation and blood pressure are primary vital signs that must be monitored

regularly for the early detection, prevention, and treatment of cardiovascular diseases [1]. While heart rate and SpO₂ are measured in a simple manner using pulse oximeters, invasive and cuff-based traditional blood pressure measuring methods have been adopted, which are unreliable, inconvenient, and uncomfortable for patients. Various research efforts have explored the effectiveness of machine learning algorithms, including Multilayer Perceptron (MLP) and Convolutional Neural Networks (CNN), in predicting arterial pressure solely from photoplethysmography (PPG) signals [4]. Traditional methods often rely on the inverse relationship between Pulse Transit Time (PTT) and blood pressure, necessitating the use of two PPG sensors. Despite their widespread use, these approaches require a calibration phase to synchronize the signals from both sensors. On the other hand, monitoring body temperature is crucial as it offers early indicators of various medical conditions, including infections, inflammatory responses, and autoimmune diseases. Moreover, fever can be identified more easily and accurately compared to other symptoms. There are several tools available for measuring body temperature, such as mercury, digital, and infrared thermometers, with numerous certified options on the market. However, the size and design of these traditional thermometers do not meet the compact device requirements for vital sign monitoring systems. This has led to growing research into miniaturized embedded electronic systems that incorporate micro infrared cameras for non-contact temperature measurement. The goal of this study is to combine heart rate, SpO₂, blood pressure and temperature monitoring in a single device, by using the only PPG technique and a thermal camera [3]. Since different wavelengths interact with the skin differently, we used multiwavelength PPG [2] to improve the precision of the outcome and contribute to motion artifact removal.

2 Materials and Methods

2.1 Heart Rate and Blood Oxygen Saturation Monitoring

Among the easiest metrics to extract from the PPG signal there are heart rate (HR) and blood oxygen saturation (SpO₂). A measuring technique that involves simultaneously detecting the PPG signal using a reflectance sensor and the real heart rate and SpO₂ using a standard pulsoxymeter has been created in order to validate the algorithm. A low-pass filter (LPF) is applied to the raw infrared and red signal after the data has been read and loaded (Fig. 1). The infrared component has been selected for the HR evaluation: by dividing the peak distances (in samples) by the sampling frequency, the RR interval can be calculated, divided by 60 to get the heart rate in beats per minute (bpm). For SpO₂ evaluation, the device has to employ signals from two different wavelengths: red light and infrared light. In this case, Principal Component Analysis (PCA) was used to address the problem of noise, performing artifact reduction. For SpO₂ calculation, the root mean square (RMS) for both red and infrared components and their ratio R are computed. The value of the SpO₂ can be estimated as:

$$SpO_2 = K_1 R^2 + K_2 R + K_3 \quad (1)$$

The absolute error with respect to the reference device was determined as an evaluation parameter in order to assess the algorithm's accuracy as well as the outcomes that were obtained.

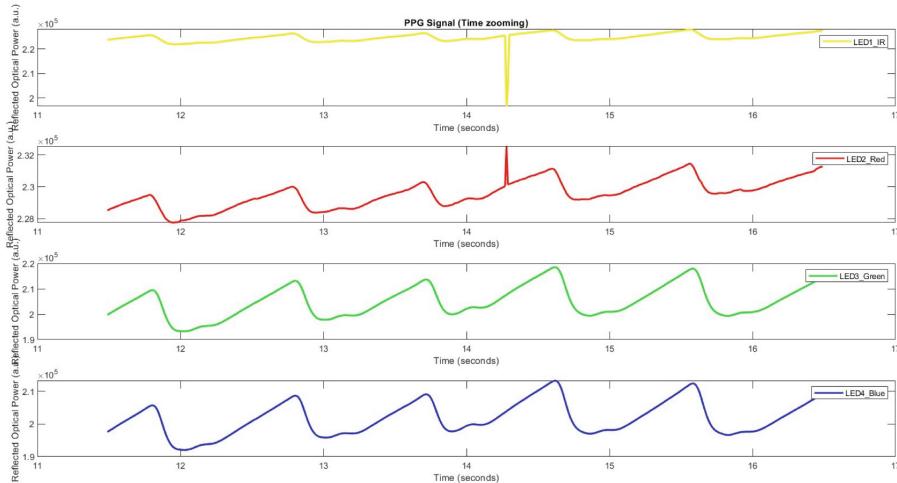


Fig. 1. Four PPG signals corresponding to four different wavelengths. IR and RED signals show rapid and wide peaks that should be removed.

2.2 Blood Pressure Monitoring

PPG signals are also used for cuff-less blood pressure prediction. After accurate signal pre-processing which aims to remove motion artifacts and slow fluctuations, this system uses an algorithm based on feed-forward artificial neural network (ANN) to estimate both systolic and diastolic blood pressure, using temporal and spectral features. The algorithm is first trained on the PPG-BP Database, given the large amount of data required, and then tested on a new dataset. For acquiring new data, the measurement protocol involves simultaneously capturing the PPG signal using the MAX86916 Evaluation Board (Fig. 2) and obtaining systolic and diastolic blood pressure readings with a certified sphygmomanometer (OMRON, accurate to ± 3 mmHg), as showed in Fig. 3.

A photodiode and four LEDs with four different wavelengths—red (655–663), green (520–535 nm), blue (455–466 nm), and infrared (930–955 nm)—combine to form the MAX86916, a multi-wavelength optical module. Two cables connect the MAX32630FTHR Cortex-M4F microcontroller, which drives the MAX86916 EV system, to a host PC: a Micro USB-USB cable connects the board's microprocessor to the computer, and a USB-FDTI connector delivers data from the sensor to the PC. Device Studio, an integrated piece of software that lets you see and save data in a file format, is part of the evaluation system.csv, which

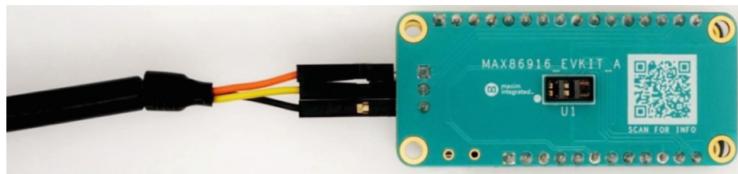


Fig. 2. MAX86916 EV System Board.

stores the sample values for each time sample of the four different PPG signals, also known as the infrared, red, green, and blue wavelengths.

Each session lasts around 30 s, the time required for the sphygmomanometer to deliver precise pressure measurements. The PPG signal is gathered by placing the right index finger on the board's optical sensor, while blood pressure is measured on the left arm with the sphygmomanometer. The study includes 88 individuals, evenly split between males and females, ranging in age from 19 to 84 years. The performance of the algorithm are given in terms of Mean Absolute Error (MAE) and Standard Deviation (SD) .



Fig. 3. Experimental setup for the simultaneous recording of PPG signal and BP values.

The goal is to meet the requirements imposed by the Association for the Advancement of Medical Instrumentation (AAMI), which states that *Mean Absolute Error* $\leq 5 \text{ mmHg}$ with *Standard Deviation* $\leq 8 \text{ mmHg}$ for SBP and DBP.

2.3 Temperature Monitoring

The electronic device also incorporates a system based on the Teensy 4.0 microcontroller board and the MLX90640 thermal camera. To conduct the measurement, a hollow, rectangular support structure was fabricated using a 3D printer and constructed from plastic, making it an economical choice. The thermal camera was installed inside this support (Fig. 4). The use of this support was chosen for several reasons:

- *Stability*: Placing the wrist on the support ensures a stable position, leading to more precise measurements.
- *Repeatability*: A standardized support allows for consistent placement of the wrist during each measurement, ensuring reliable and reproducible results.
- *Comfort*: The flat surface of the support offers a more comfortable experience, reducing movements that could compromise measurement accuracy.
- *Consistent Distance*: The support helps maintain a fixed distance between the sensor and the wrist, enhancing measurement accuracy

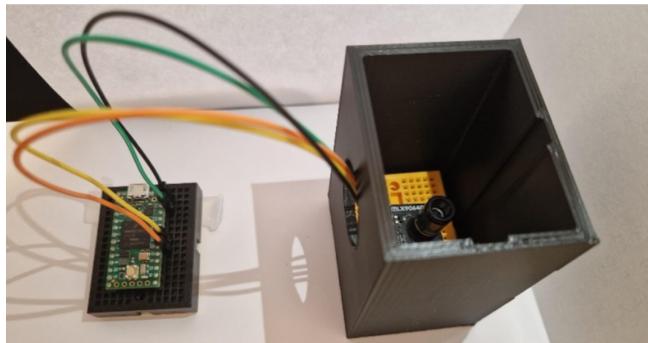


Fig. 4. Actual setup with the wrist support.

The measurement protocol involves the simultaneous recording of temperature using the electronic system and a certified infrared thermoscan on the market, which serves as a reference device, with an accuracy of $\pm 0.2^\circ\text{C}$. Specifically, the temperature is detected by placing the wrist on the support of the camera, and the reference value is measured on the same wrist using an IR thermometer.

3 Results and Conclusions

The performances are promising (Table 1), with an average relative error of less than 5% for heart rate and blood saturation, and a Mean Absolute Error of 5.08 ± 8.83 mmHg and 4.37 ± 7.08 mmHg for systolic and diastolic pressure

respectively. The MLX90640 thermal camera accurately measured patients body temperature in a noninvasive and continuous manner, with a maximum absolute error equal to 0.2°C . The work presented in this paper demonstrates how the single PPG signal allows one to easily monitor vital conditions in a continuous and non-invasive manner. Among the strengths of this method, it is possible to recognize: (1) the absence of calibration, which takes time and makes the algorithm not generalizable, (2) the only use of PPG signal for vital parameters, which does not require additional hardware and more expensive set-ups, (3) the non-contact approach for body temperature, which provides a better experience to patients with burn wounds or skin irritations and babies with limited attachment points. Among the limits, we can recognize that this method has been tested on healthy subjects only and the electronic device has been developed for an initial prototypal stage.

Table 1. Estimated vital parameters and errors with respect to the reference device.

VITAL PARAMETER	ERROR
Heart Rate	2%
SpO ₂	3%
Blood Pressure (SBP and DBP)	$5.08 \pm 8.83 \text{ mmHg}$ $4.37 \pm 7.08 \text{ mmHg}$
Temperature	0.2°C

References

- Ray, D., Collins, T., Woolley, S.I., Ponnappalli, P.V.S.: Review of wearable multi-wavelength photoplethysmography. *IEEE Rev. Biomed. Eng.* **16**, 136–151 (2023)
- Analog Devices: MAX86916 Evaluation System
- Botrugno C., Leogrande E., Natale T., Dell'Olio F.: Smart combination of ECG and PPG signals: an innovative approach towards an electronic device for vital signs monitoring. In: 2023 IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), Monopoli, BA, Italy (2023)
- El-Hajj, C., Kyriacou, P.A.: A review of machine learning techniques in photoplethysmography for the non-invasive cuff-less measurement of blood pressure. *Biomed. Signal Process. Control* **58**, 101870 (2020)



A Front-End Board for Modular Ultrasound Open Scanners

F. Lagonigro^(✉), A. Vignoli, V. Meacci, P. Verdi, P. Tortoli, A. Ramalli, and E. Boni

Department of Information Engineering, University of Florence, Florence, Italy
{francesco.lagonigro,enrico.boni}@unifi.it

Abstract. The development of advanced techniques for three-dimensional (3D) ultrasound imaging demands open scanners able to simultaneously and independently control thousands of piezoelectric transducers on two-dimensional (2D) array probes. This work proposes a modular solution based on a 64-channel front-end module (FEM) capable of transmitting, receiving, conditioning, and digitizing ultrasound signals, and of transferring them to an elaboration unit through a 10GEthernet protocol with a global data-rate of 40 Gbps. Multiple FEM units can synchronously operate by sharing a common front-plane board to build high channel count ($N \times 64$) open scanners.

Keywords: ultrasound imaging · open scanner · modular open platform · high channel count

1 Introduction

Medical ultrasound (US) echographic systems are increasingly used for their diagnostic capabilities, non-invasiveness, real-time operation, low-cost, and portability. These systems consist of a multi-channel electronic scanner and an array of transducers. The scanner contains the electronics for the generation of the transmission (TX) signals and the reception (RX), acquisition, and processing of the echo signals. In clinical scanners, the number of TX/RX channels is 256 at most. Such number, which is limited by the complexity of electronics and of the probe-scanner connection, is adequate only for controlling one-dimensional (1D) probe heads. In the research context, the development of advanced techniques for three-dimensional (3D) ultrasound imaging [1–4] requires open scanners (i.e., systems characterized by high flexibility, programmability, and access to raw echo data) [5] able to simultaneously and independently control thousands of piezoelectric transducers on two-dimensional (2D) array probes. The SARUS scanner [6] (Technical University of Denmark), can control up to 1024 transducer elements of a matrix probe. Housed in a double rack of size $120 \times 200 \times 60$ cm, this complex system is characterized by high computational power, but no constraints in terms of portability and cost were considered. Alternatively, the channel count can be increased by synchronizing multiple research scanners [7–9], but the management of such an architecture is extremely complex, and, to some extent, physically and computationally prohibitive. Moreover, this solution presents limitations on the data transfer among systems as well

as toward host PCs [10–13]: such limitations are due to the communication devices, which cannot sustain the high rates (in the order of tens/hundreds of Gbps) required to transfer, acquire, and possibly process the raw radiofrequency data.

This work proposes a 64-channel front-end module (FEM), which can be replicated to build high channel count ($N \times 64$) open scanners exploiting the synchronous operation of multiple FEM units that share a common front-plane board.

2 Methods

2.1 Front-End Module Architecture

Each FEM manages 64 TX and RX channels: it controls the TX of high voltage signals, conditioning and analog to digital conversion of echo signals, and data transfer to a cascade processing back-end module (BEM).

The FEM consists of two stacked boards (Fig. 1): the baseboard (BB), which is a 16×10 cm printed circuit board (PCB), and the FPGA PCB, which is 6×8 cm. As sketched in Fig. 2, the BB hosts four 16-channel TX devices (STHV1600, STM, Italy), which generate 3/5-level, pulsed waveforms with amplitude up to 100 V, and manage the TX/RX transition. The parameters of each transmitter are communicated to an internal memory via serial peripheral interface (SPI). In RX, the analog signals gathered by the probe [14] are amplified, filtered, and digitized by two 32-channel analog front-end (AFE) chips (AFE5832LP, Texas Instruments, USA). The amplification is performed by a low noise amplifier (LNA), a variable attenuator for time-gain compensation, and a selectable gain amplifier. A third-order low-pass filter can be set at the desired cut-off frequency. The integrated analog to digital converters (ADCs) work with 10-bit resolution at 50 MSPS.

The FEM communicates with a BEM through a quad small form-factor pluggable (QSFP +) optical transceiver (FTL410QE4N, Finisar, USA). This is inserted in a metal cage and connected to an optical fiber with a multi-fiber termination push-on connector to be easily linked to different processing units.

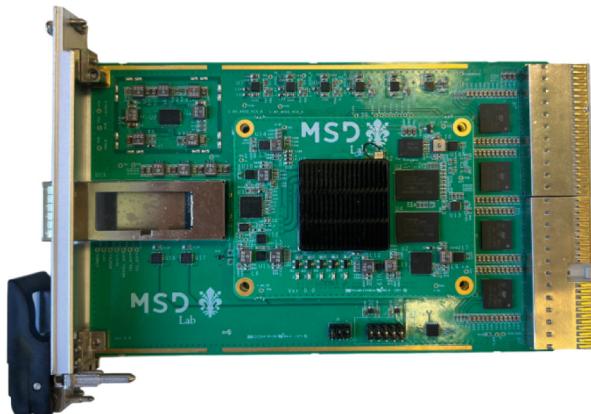


Fig. 1. Picture of the two stacked board of the FEM

The FPGA module embeds two 1-GB random access memory (DDR3) chips and an FPGA (Cyclone 10 GX, Intel, USA). The latter currently oversees the control of the BB's devices and the communication with the BEM. Having the FPGA on a different PCB facilitates the possible upgrade based on new, more powerful, and/or cost-effective devices.

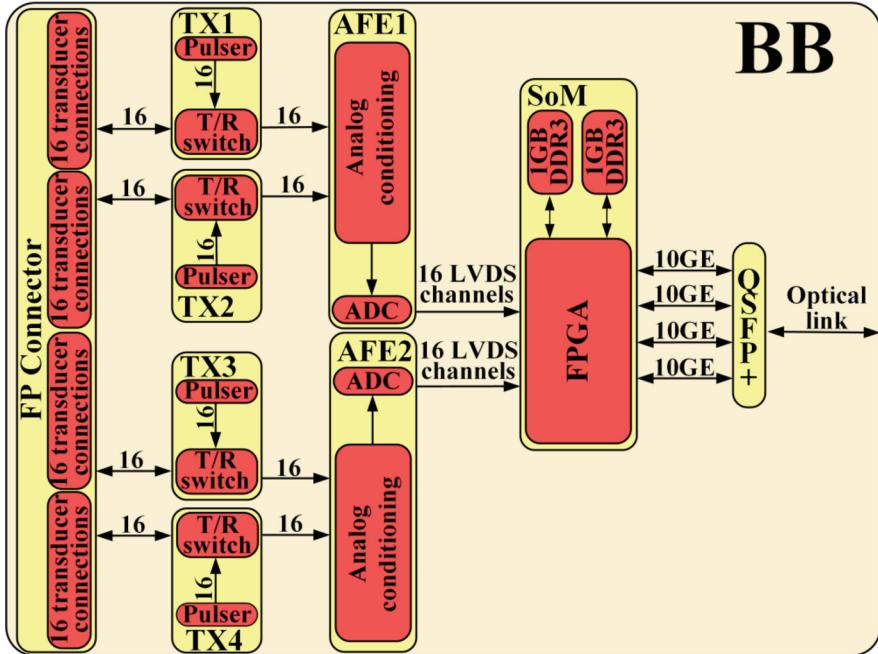


Fig. 2. Functional block-diagram of the FEM baseboard.

2.2 FPGA Firmware

The FPGA oversees the communication between FEM and BEM and manages the commands to control and program the transmitters, AFEs, and transceivers. Figure 3 sketches the firmware main functional blocks, which are the Configuration Block (CB) and Transceiver Manager (TM). The CB includes the programming interfaces for pulsers, AFEs, and transceivers, as well as a Configuration unit and is responsible for managing the SPI and I²C communication. The TM contains all the logic required to generate and transmit as well as receive 10GEthernet packets; since the FPGA drives four separate optical channels, the TM block is replicated four times.

The FPGA receives 2×16 LVDS digital streams from the ADCs: this data is deserialized by two instances of the LVDS SERDES Intel FPGA IP core, and then segmented into standard Ethernet packets. Finally, these data streams are sent to the BEM through four 10GEthernet channels via optical communication. To correctly implement

the media access controller (MAC) and the physical (PHY) layers of the 10GEthernet protocol, the firmware relies on the Low Latency (LL) Ethernet 10G MAC and the Intel Cyclone 10GX Transceiver PHY Intel FPGA IP cores. The current operational settings of transmitters and AFE interfaces and of optical transceivers are selected by the BEM, which sends the programming commands to the FPGA through the four Ethernet channels. The Ethernet packets are received and manipulated so that the data content of the Ethernet packets is serialized and eventually forwarded to the CB. This FPGA block is designed to decode the commands, determine the recipient module, and forward the commands to the driver of the desired interface programmer.

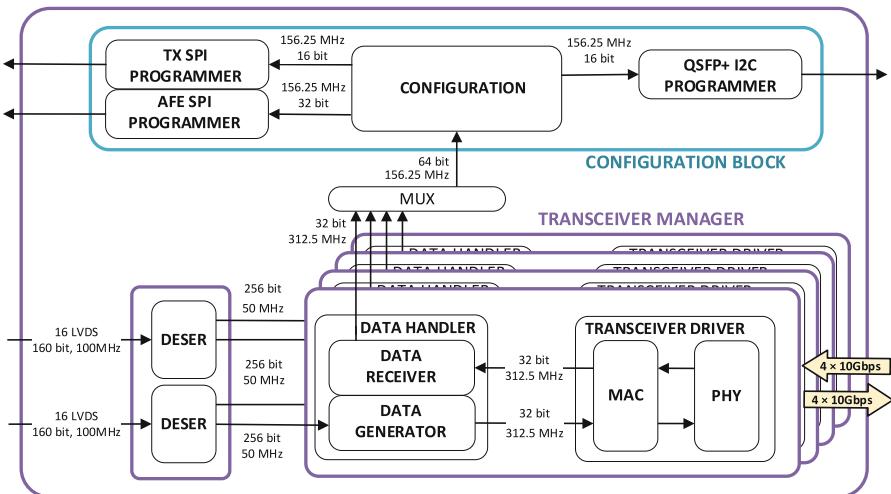


Fig. 3. Schematic overview of the FPGA firmware functional blocks.

Inside the FPGA, separate blocks communicate with each other mostly through the Avalon Streaming (AS) and Avalon Memory Mapped (AMM) interfaces [15]. Data transmission between the Ethernet protocol MAC and PHY layers relies on the standard 10-gigabit media-independent interface (XGMII).

3 Results and Discussion

As a proof-of-concept, the hardware and firmware of the TX/RX chain were tested for one of the 192 elements of an Esaote LA532 linear array probe and the results are shown in Figs. 4 and 5. The former shows the TX signal acquired and stored by an oscilloscope (DSOX2014A, Keysight, USA) when the channel was programmed to generate a 20 V amplitude, 4-cycle burst at 6 MHz. Figure 5 depicts the echo signal reflected by a flat metal plate positioned at the bottom of a water tank, at about 25 mm distance from the probe. The echo was acquired by the AFE, set with a total gain of 18 dB; the digitized data was then transferred via LVDS to the FPGA and deserialized; this deserialized signal was eventually visualized and stored through a signal analyzer software (Intel

SignalTap II Logic Analyzer) and, finally, the stored TX and RX data were exported to Matlab for plotting.

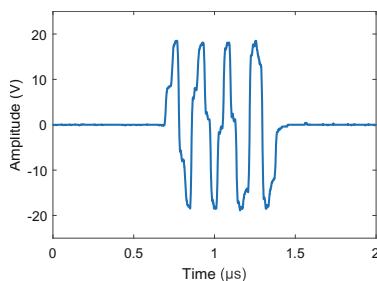


Fig. 4. Transmitted signal

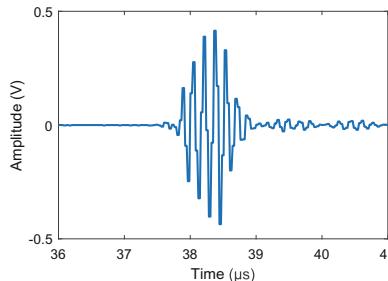


Fig. 5. Received signal amplified by 18 dB

The data transfer rate towards the BEM was measured by generating, directly on the FPGA, test frames that were transferred through the four optical channels to a PC equipped with a standard network interface card (NIC). The quad data-stream was buffered and transmitted as 10GEthernet protocol frames through four independent high-speed bitstreams (10 Gbps per channel) to the optical transceivers, and a maximum output data rate of 40 Gbps (4×10 Gbps) was measured.

In conclusion, these results confirm the correct behavior of main board functionalities. Work is in progress towards testing the combination of multiple (N) boards to implement an $N \times 64$ channel echographic system. First, a (3×64) channel system capable of controlling standard 192-element clinical probes will be tested. Then, the number of boards sharing the front-plane board will be increased up to 32, to reach the goal of controlling 2048-element probes.

Acknowledgments. This work was supported by the contribution of the project PRIN 2020 - CONUS (grant number 20205HFXE7) - funded by the Italian Ministry of Education, University and Research (CUP: B13C21000190005).

References

1. Provost, J., Papadacci, C., Arango, J.E., et al.: 3D ultrafast ultrasound imaging *in vivo*. *Phys. Med. Biol.* **59**, L1–L13 (2014). <https://doi.org/10.1088/0031-9155/59/19/L1>
2. Holbek, S., Ewertsen, C., Bouzari, H., et al.: Ultrasonic 3-D vector flow method for quantitative *in vivo* peak velocity and flow rate estimation. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **64**, 544–554 (2017). <https://doi.org/10.1109/TUFFC.2016.2639318>
3. Giangrossi, C., Ramalli, A., Dallai, A., et al.: Requirements and hardware limitations of high-frame-rate 3-D ultrasound imaging systems. *Appl. Sci.* **12**, 6562 (2022). <https://doi.org/10.3390/app12136562>
4. Papadacci, C., Finel, V., Villemain, O., et al.: 4D simultaneous tissue and blood flow Doppler imaging: revisiting cardiac Doppler index with single heart beat 4D ultrafast echocardiography. *Phys. Med. Biol.* **64**, 085013 (2019). <https://doi.org/10.1088/1361-6560/ab1107>

5. Boni, E., Yu, A.C.H., Freear, S., et al.: Ultrasound open platforms for next-generation imaging technique development. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **65**, 1078–1092 (2018). <https://doi.org/10.1109/TUFFC.2018.2844560>
6. Jensen, J.A., Holten-Lund, H., Nilsson, R.T., et al.: SARUS: A synthetic aperture real-time ultrasound system. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **60**, 1838–1852 (2013). <https://doi.org/10.1109/TUFFC.2013.2770>
7. Mazierli, D., Ramalli, A., Boni, E., et al.: Architecture for an ultrasound advanced open platform with an arbitrary number of independent channels. *IEEE Trans. Biomed. Circuits Syst.* **15**, 486–496 (2021). <https://doi.org/10.1109/TBCAS.2021.3077664>
8. Risser, C., Hewener, H., Fournelle, M., et al.: Real-time volumetric ultrasound research platform with 1024 parallel transmit and receive channels. *Appl. Sci.* **11**, 5795 (2021). <https://doi.org/10.3390/app11135795>
9. Petrusca, L., Varray, F., Souchon, R., et al.: Fast volumetric ultrasound b-mode and doppler imaging with a new high-channels density platform for advanced 4D cardiac imaging/therapy. *Appl. Sci.* **8**, 200 (2018). <https://doi.org/10.3390/app8020200>
10. Hager, P.A., Benini, L.: LightProbe: a digital ultrasound probe for software-defined ultrafast imaging. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **66**, 747–760 (2019). <https://doi.org/10.1109/TUFFC.2019.2898007>
11. So, H., Chen, J., Yiu, B., Yu, A.: Medical ultrasound imaging: to GPU or not to GPU? *IEEE Micro* **31**, 54–65 (2011). <https://doi.org/10.1109/MM.2011.65>
12. Yiu, B.Y.S., Walczak, M., Lewandowski, M., Yu, A.C.H.: Live ultrasound color-encoded speckle imaging platform for real-time complex flow visualization in vivo. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **66**, 656–668 (2019). <https://doi.org/10.1109/TUFFC.2019.2892731>
13. Cacko, D., Jarosik, P., Lewandowski, M.: Real-time shear wave Elastography implementation on a portable research ultrasound system with GPU-accelerated processing. In: 2023 IEEE International Ultrasonics Symposium (IUS), pp. 1–4 (2023)
14. Maione, E., Tortoli, P., Lypacewicz, G., et al.: PSpice modelling of ultrasound transducers: comparison of software models to experiment. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **46**, 399–406 (1999). <https://doi.org/10.1109/58.753029>
15. Introduction to the Avalon® Interface Specifications. In: Intel. <https://www.intel.com/content/www/us/en/docs/programmable/683091/22-3/introduction-to-the-interface-specifications.html>. Accessed 20 Jun 2024



Miniaturized Low-Power Head-Mounted PPG Board

Alice Scandelli¹(✉), Ilaria Crupi¹, Andrea Giudici¹, Pietro Bartoli¹, Arianna De Vecchi¹, Giacomo Gervasoni², Diana Trojaniello², and Federica Villa¹

¹ Politecnico di Milano, Piazza L. Da Vinci 32, 20133 Milano, Italy

{alice.scandelli, federica.villa}@polimi.it

² EssilorLuxottica Smart Eyewear Lab, EssilorLuxottica, Milano, Italy

{giacomo.gervasoni, diana.trojaniello}@luxottica.com

Abstract. This work presents the development of a miniaturized, low-power, Printed Circuit Board (PCB) probe used to explore various head locations for Photoplethysmography (PPG) monitoring. In the testing phase, the system consumes 83.5 mW, in the worst conditions. The optimal position for head PPG acquisitions proved to be the angular artery on the nose.

Keywords: Wearable Sensors · Low-Power Printed Circuit Board (PCB)
Design · Head Worn Device · Photoplethysmography (PPG)

1 Introduction

Photoplethysmography (PPG) is a non-invasive and inexpensive optical measurement method that is widely used to measure physiological parameters such as heart rate (HR), blood oxygen saturation (SpO_2), and heart rate variability (HRV) [1]. PPG technique uses a light source and a photodetector placed at the skin surface to measure the volumetric variations of blood in the microvascular bed.

Since 2010s, PPG sensors are frequently integrated into wearable devices like smart-watches and fitness trackers, which are now used by millions of people each day [2]. While these devices have demonstrated significant utility in continuous health monitoring, they are not without limitations, particularly in terms of signal quality and user comfort.

Thanks to the vascular-rich nature of the head, smart eyewear hold promise for hands-free cardiovascular parameter monitoring [3]. This integration offers unique advantages that could enhance the effectiveness and user experience of continuous health monitoring. For instance, smart eyewear provide a more comfortable and non-intrusive solution for users. Many people already wear glasses daily for vision correction, making it seamless to incorporate health monitoring technology into this familiar accessory. This can potentially improve user compliance and comfort by eliminating the need for additional wearable devices that may cause discomfort over prolonged use. Additionally, smart eyewear may be exploited as a platform for multiple sensors integration by combining

PPG sensors with other sensors, such as Inertial Measurement Units (IMUs) [4] and electrocardiography (ECG) sensors, providing comprehensive health monitoring and data collection. In the case of smart eyewear, the correct integration of the sensing unit in the eyeglasses' frame, the overall dimensions and the overall wearability of the system are essential requirements [5]. As a consequence, the sensing unit should have reduced dimensions and should seamlessly replace one or more elements of the eyeglasses. Furthermore, the sensors and the associated electronics should be properly selected to minimize the device's power consumption and to ensure a long-lasting operational lifetime.

This study investigates the integration of PPG sensors into smart glasses, ensuring comfortable wear and long operational lifetime. A miniaturized low-power Printed Circuit Board (PCB) probe was developed to test different head locations to determine the optimal site for PPG monitoring.

2 Hardware Design and Device Power Consumption

To easily integrate the PPG probe into different points of the eyeglasses' frame, the probe board was designed as a rigid-flex PCB. The rigid part, $14\text{ mm} \times 7\text{ mm} \times 2.4\text{ mm}$ 4-layer board, serves as a sensing site housing a 6-axis IMU and a PPG sensor equipped with three internal LEDs (red, infrared, and green) and a photodiode (Fig. 1). Conversely, the flexible part, $89\text{ mm} \times 6.6\text{ mm} \times 0.16\text{ mm}$, extends from the rigid stack-up as a 2-layer interface and is exclusively dedicated to routing signal traces from the sensors to the main board. Both the rigid and flexible segments feature external pads functioning as connectors to the main board. The probe can adapt to various regions of the eyewear' frame thanks to its rigid-flex technology of the PCB; in addition, the flexible part can be easily detached, allowing for easy repositioning of the rigid PCB on different head locations.

The probe is connected to a main board that provides the power supply, drives the sensors and stores the data. The main board comprises a Microcontroller Unit (MCU), a standalone Linear Li-Ion Charger with Micropower Low-Dropout (LDO) regulator, a micro Secure Digital (SD) slot, and a Micro USB connector, and it is powered up using a single cell LiPo battery with a 3.7 V nominal voltage and 230 mAh capacity. The final system, obtained from the connection of the probe board with the main board, is illustrated by the block diagram in Fig. 2.

In order to evaluate the device's functioning, a comprehensive analysis of the overall system's power consumption was conducted under different conditions (Table 1). The current consumption of the probe board was evaluated using an oscilloscope and a $10\text{ }\Omega$ resistance in series with the 3.3 V supply voltage. In particular, at first, the IMU was turned into shutdown mode and the PPG sensor current consumption was measured with all the 3 LEDs on, having pulse amplitude set to 6 mA, pulse width set to 411 μs and sample rate set to 100 Hz, equivalent to a duty cycle of 4.1% for each single LED. In these conditions, the measured current consumption of the PPG sensor is 740 μA , leading to a power consumption of 2.4 mW. Then, the PPG sensor was turned into shutdown mode while the IMU was configured in high-performance mode with 120 Hz sample rate. Rate noise density in high-performance mode is independent of the output data rate and full

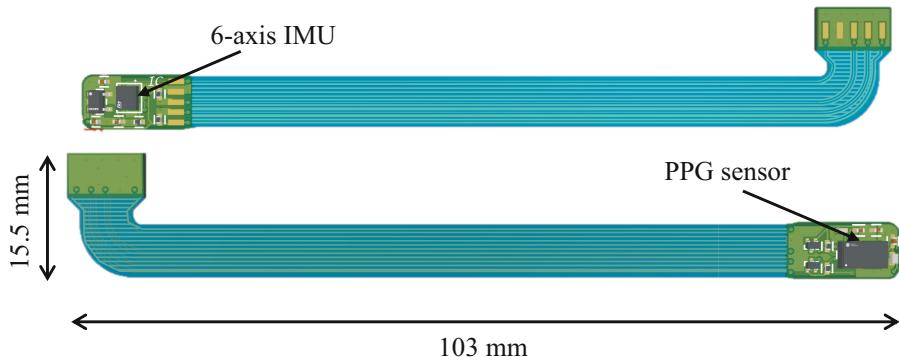


Fig. 1. Probe board 3D layout.

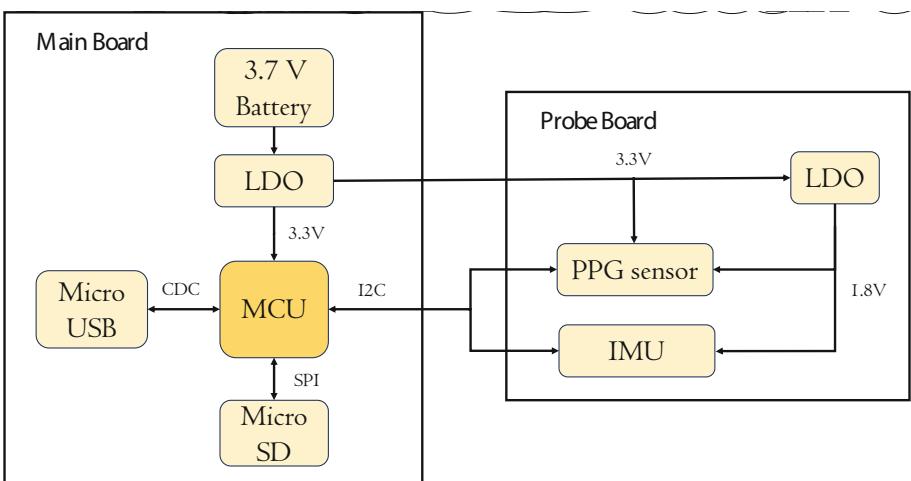


Fig. 2. Final System block diagram.

scale setting. In this case, the IMU consumes $580 \mu\text{A}$, resulting in a power consumption of 1.9 mW .

The main board characterization was then performed at two MCU system clock frequencies (i.e., 84 and 32 MHz) and by shutting down the two sensors on the probe board. With these settings, the measured power consumption is of 79.2 mW and 33.0 mW, respectively.

The overall system in worst conditions (main board with MCU at 84 MHz connected to one probe board with PPG and IMU sensors powered on) consumes 83.5 mW, leading to an estimated battery lifetime up to 9 h. This can be further reduced to 37.3 mW if the MCU's clock frequency is decreased to 32 MHz.

Table 1. Probe board and main board power consumption considering 3.3 V supply voltage.

Testing condition	Power Consumption [mW]
3-LED PPG at 100 Hz with 6 mA Pulse Amplitude and 411 μ s Pulse Width	2.4
ACC and GYR in High-Performance Mode	1.9
Main board (MCU SysClk: 84 MHz)	79.2
Main board (MCU SysClk: 32 MHz)	33.0

3 Experimental Positioning Test

Three specific head locations (Fig. 3) have been chosen for their association with larger arteries and their natural contact with the glass frame when wearing eyewear. The selected locations include: on the nose, aligned with the nose-pad (P1), where the pulsatile flow of the angular artery is measured; behind the ear (P2), corresponding to the posterior auricular artery; and above the ear (P3), where the superficial temporal artery is situated.

To accurately compare the quality of PPG signal in the three different positionings P1, P2 and P3, we designed a controlled experimental protocol and asked participants to perform three simple actions (Fig. 4) including 3 min of sitting at rest and in free breathing, one apnea after taking a deep breath, 1 min of recovery and 3 min of standing in free breathing. Between these activities, the subject was asked to perform some movements (jumping or shaking the head) to facilitate the subsequent data synchronization. We chose a controlled study since it enables conducting a detailed analysis of the phenomenon under investigation and it is suitable for the reproducibility of the data collection procedure. Ten subjects (5 males, 5 females, mean age: 28 years, standard deviation: 5 years) were recruited and voluntarily took part in the study. None of the participants had any underlying heart or respiratory condition and were in good health at the time of the study. All subjects provided voluntary written, informed consent to the experimental protocol, approved by the Ethical Committee of the Politecnico di Milano (date of approval: October 16th, 2023, number 33/2023) in accordance with the Declaration of Helsinki of 1975, as revised in 2000. To simultaneously acquire PPG signals from the three distinct locations, three PPG probes were integrated into the eyewear frame. Each probe was used to record 3-wavelength PPG, along with 3-axis acceleration, and 3-axis rotation data from the IMU, at a sampling rate of 100 Hz. Furthermore, the Movesense Flash Sensor (Movesense Ltd, Vantaa, Finland), a portable ECG chest band with an integrated IMU, was used as gold standard for extracting cardiovascular parameters.

The Mean Absolute Percentage Error (MAPE) between the number of heartbeats in the ECG reference signal, determined using the Pan Tompkins algorithm [6], and the number of heartbeats in the PPG signal, calculated using the PPG beat detection algorithm by Peter Charlton [7], was computed (Table 2).

Table 2 displays the percentage error between the estimated number of beats calculated from the reference ECG signal and the number of beats computed from the PPG signals, along with the percentage of signals discarded because the PPG waveform

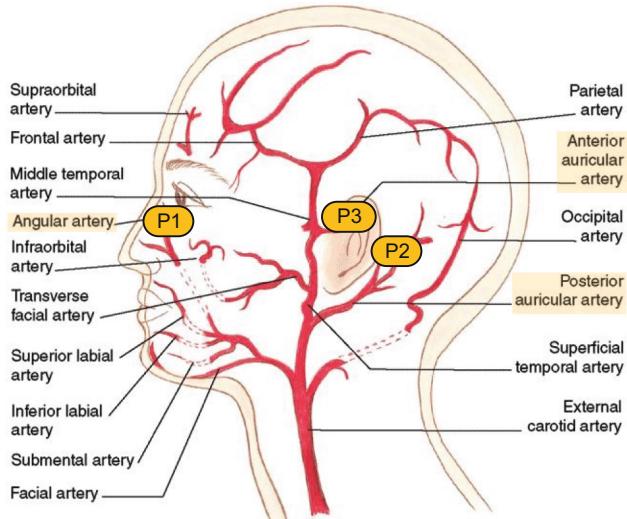


Fig. 3. Selected positions: angular artery (P1), posterior auricular artery (P2) and superficial temporal artery (P3).

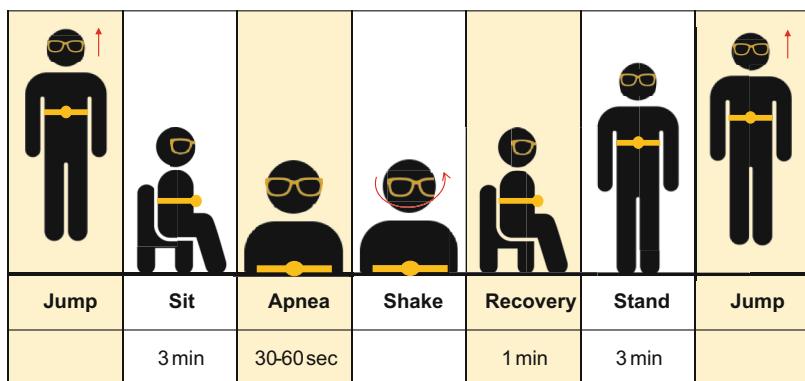


Fig. 4. Experimental protocol.

wasn't noticeable and thus the beat detection algorithms weren't applicable. This shows that position P1 generated fewer bad signals. Additionally, position P1 exhibited smaller errors compared to positions P2 and P3, further supporting the notion that the nose may be the optimal location for measuring the PPG signal.

Table 2. MAPE on the number of beats estimation, and percentage of discarded signals, identified as signals where the beat detection algorithms couldn't be applied.

Activity	Sit		Apnea		Stand	
	MAPE	% discarded	MAPE	% discarded	MAPE	% discarded
P1	5%	3%	3%	4%	4%	7%
P2	10%	68%	14%	61%	15%	64%
P3	8%	63%	14%	70%	14%	64%

4 Conclusions

This work presents the development of a miniaturized, low-power probe board designed to explore different sensor placements for head PPG monitoring. The probe has been seamlessly integrated into a pair of eyewear and positioned in three different locations: the angular artery, the posterior auricular artery, and the superficial temporal artery.

The overall system, consisting of a main board (MCU at 84 MHz) connected to one probe board, consumes 83.5 mW, resulting in an estimated battery lifetime of approximately 9 h, making it suitable for daily use in real-time scenarios. This power consumption can be further reduced by scaling down the MCU system clock frequency. From the positioning tests, the angular artery exhibited smaller errors and fewer discarded signals compared to the posterior auricular artery and the superficial temporal artery, suggesting that the nose may be the optimal site for head PPG acquisitions.

Future developments include analyzing potential sources of noise in the PPG signal, such as sweat or facial movements, and studying the combination of IMU signals with the PPG signal to address these artifacts. Additionally, the sample size of 10 subjects may limit the generalizability of the results, and the controlled environment may not fully represent real-world scenarios. Nevertheless, this study provides a comprehensive evaluation of the system, demonstrating its suitability for positioning experiments and data collection for further processing, while maintaining a small size and low power consumption.

Acknowledgements. This work was carried out in the EssilorLuxottica Smart Eyewear Lab, a Joint Research Center between EssilorLuxottica and Politecnico di Milano.

References

1. Castaneda, D., Esparza, A., Ghamari, M., Soltanpur, C., Nazeran, H.: A review on wearable photoplethysmography sensors and their potential future applications in health care. *Int. J. Biosensors & Bioelectronics* **4**(4) (2018). <https://doi.org/10.15406/ijbsbe.2018.04.00125>
2. Charlton, P., et al.: The 2023 wearable photoplethysmography roadmap. *Physiological Measurement* (2023). <https://doi.org/10.1088/1361-6579/acead2>
3. Holz, C., Wang, E.J.: Glabella. *Proceedings of the ACM on Interactive, Mobile, Wearable and Ubiquitous Technologies* **1**(3), 1–23 (2017). <https://doi.org/10.1145/3132024>

4. Hernandez, J., Li, Y., Rehg, J.M., Picard, R.W.: BioGlass: Physiological parameter estimation using a head-mounted wearable device. International Conference on Wireless Mobile Communication and Healthcare, pp. 55–58 (2014). <https://doi.org/10.1109/mobihealth.2014.7015908>
5. Amft, O., Wahl, F., Ishimaru, S., Kunze, K.: Making regular eyeglasses smart. IEEE Pervasive Comput. **14**(3), 32–43 (2015). <https://doi.org/10.1109/MPRV.2015.60>
6. <https://it.mathworks.com/matlabcentral/fileexchange/45840-complete-pan-tompkins-implementation-ecg-qrs-detector>. Last accessed 5 March 2024
7. Charlton, P.: PPG Beat Detection. <https://petercharlton.github.io/project/ppg-beats/>. Last accessed 7 March 2024



A Modular Portable Current Stimulator for Electrical Stimulation of Excitable Tissues

Riccardo Collu¹ ID, Stefano Lai¹ ID, Antonello Mascia¹ ID, Roberto Paolini² ID,
Elena Ferrazzano¹ ID, Loredana Zollo² ID, Piero Cosseddu¹ ID,
and Massimo Barbaro¹ ID

¹ University of Cagliari, 090123 Cagliari, Italy
riccardo.collu@unica.it

² Università Campus Biomedico di Roma, 00128 Rome, Italy

Abstract. Electrical stimulation can be applied to excitable tissues to obtain sensory feedback, as in the case of stimulation of the peripheral nervous system, or mechanical actuation, as in the case of the stimulation of muscle tissues. In this study, a current stimulator for the stimulation of excitable tissues is proposed. The stimulator, created using a “stacked” approach, is made up of three separable units, namely a microcontroller unit, a stimulation frontend unit, and a power unit. The stimulator, made with Components-Off-the-Shelf (COTS), guarantees a working voltage of up to ± 90 V and a stimulation current of up to 18 mA. The system has been tested for the stimulation of the peripheral nervous system on healthy volunteers, making it capable of inducing distinguishable sensations in the lower limb and on the upper limb, both through the use of conventional electrodes and ultra-conformable tattoo electrodes. Furthermore, the stimulator was tested for the control of a biohybrid actuator made up of muscle tissues showing the possibility of inducing twitch and tetanic contraction.

Keywords: Neurostimulator · COTS · portable electronic system · tattoo electrodes · haptic feedback · biohybrid machines

1 Introduction

Electrical stimulation of excitable tissues has been widely explored over the years [1], thus outlining the main stimulation paradigms that control muscle tissues’ contractile activity or convey information through neurons. In the field of sensory feedback, the use of electrical stimulation has proven effective in allowing the restoration of tactile information in amputee subjects [2]. However, the main studies on sensory feedback are focused on the use of invasive technologies, such as implantable electrodes [3–6], which, as such, require surgery to be used, therefore limiting their field of applicability. Another substantial limitation is the need for more portable technology that can be integrated into the prosthetic system or the user’s clothing, thus leading to benchtop use and the execution of tests mainly within laboratories [7]. The potential of non-invasive technologies to revolutionize the widespread use of electrical stimulation for sensory

feedback is a promising development. Several studies have already demonstrated the effectiveness of transcutaneous electrical stimulation in inducing electrical sensations in peripheral limbs [8–10], thereby presenting a viable alternative to invasive technologies. The control of biohybrid actuators, and biohybrid machines in general, can be achieved through various methods, including magnetic, optical, chemical, and electrical actuation [11, 12]. Electrical stimulation offers several advantages over other methods, such as remote control, rapid activation of the actuator, and the ability for parallel and selective stimulation, making it a compelling choice. In this regard, however, electrical stimulation is usually performed under voltage and using benchtop instruments, even if this strategy does not guarantee optimal control over the injected charge, thus leading to the establishment of hydrolysis reactions.

The use of current electrical stimulation is the safest electrical stimulation strategy, both for sensory stimulation and for controlling biohybrid actuators. This work discusses the development of a portable and modular current stimulator designed to stimulate excitable tissues. The simulator has been tested in three different case tests: stimulation of peripheral nervous systems via commercial and tattoo electrodes, stimulation of biohybrid actuator, and evaluation of intracortical electrode.

2 The Designed Stimulator

To ensure the portable stimulator system remains small enough, the circuit has been designed as a stacked system measuring 59 mm × 28 mm × 25 mm (length × width × height). It consists of two custom Printed Circuit Boards (PCBs) and a commercial microcontroller unit, as shown in Fig. 1. This setup separates the power management units from the stimulation Frontend (FE), creating a modular device that can be easily adjusted for voltage compliance and stimulation current characteristics. Each PCB is a 59 mm × 28 mm, two-layer board designed to stack neatly on the commercial development microcontroller unit (MCU) board ESP32-WROOM-32UE. This MCU is a dual-core 32-bit microprocessor with a built-in Bluetooth module and USB peripheral.

2.1 Stimulation Frontend

The FE unit PCB is positioned in the middle of the stack. It receives the high-voltage bipolar supply from the power management unit and the 5 V supply from the MCU. It contains a four-channel 16-bit bipolar digital-to-analog converter (DAC) ADC, Analog Devices LTC2664, which is connected to the four stimulating channels. Each output channel consists of a voltage programmable voltage-to-current converter that delivers the current to the load using two amplifiers. One is a low voltage rail-to-rail amplifier from Analog Devices (Massachusetts, USA) AD8519ARTZ, and the other is a high voltage amplifier from Texas Instruments (Dallas, Texas, USA) OPA462IDDA. The MCU utilizes the SPI protocol to program the DAC, enabling users to turn ON or OFF any of the four channels. The low voltage amplifier serves as a buffer to sink/source the stimulation current, which is determined by the DAC output voltage and resistor R_{stim}. The load requiring stimulation is connected in feedback to the high-voltage amplifier to

ensure the flow of the stimulation current as described in [7, 13]:

$$I_{stim} = \frac{V_{DAC}}{R_{stim}} \quad (1)$$

2.2 Power Management Unit

The power management unit PCB is situated at the bottom of the stack. It consists of two booster circuits utilizing switching voltage regulators from Analog Devices Inc. (Wilmington, MA, USA) LT8365, and a voltage inverting circuit using components from Maxim Integrated (San Jose, CA, USA) MAX889RESA to produce the required -5 V for the stimulation FE. The LT8365 is a voltage converter used to boost or invert voltages, ensuring low quiescent current and minimal output ripple. It is responsible for generating the $\pm 90\text{ V}$ voltage compliance necessary for the stimulation output channel from the 5 V supply provided by the MCU.

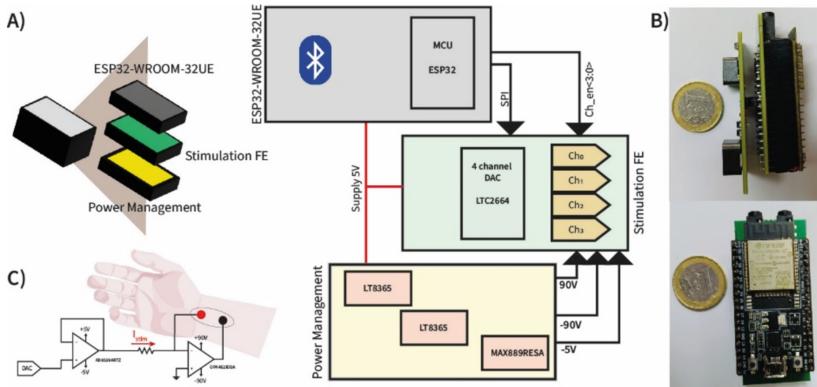


Fig. 1. The proposed prototype. **A)** The system is composed of three different modules, a MCU, a frontend unit and a Power management unit. **B)** Front and lateral view of the prototype. **C)** Stimulation FE schematic.

2.3 Electrical Stimulation

The device can be fully programmed to provide stimulation with various waveforms, allowing for custom stimulation protocols. The capability to generate stimulation waveform is limited by the SPI to 2 ksp. The resolution of the current can be programmed between 381 nA and 762 nA.

3 System Evaluation

The power consumption of the device has been measured to be 1.3 W. The proposed system has been tested for three tasks: electrical stimulation of peripheral nerves in healthy volunteers, electrical stimulation of biohybrid actuator, and evaluation of intracortical electrode for invasive stimulation.

3.1 Electrical Stimulation of Peripheral Nervous System

The stimulation of peripheral nerves has been performed on ten healthy volunteers using commercial electrodes and three volunteers using ultra-conformable tattoo electrodes [13–15]. Commercial electrodes were positioned on the leg of the volunteers to target the tibial nerve. Stimulation was performed at different frequency and different amplitudes, modulating the injected charge. The maximum frequency employed was 500 Hz. The descriptions of sensations in terms of quality and naturalness were collected, as shown in Fig. 2.

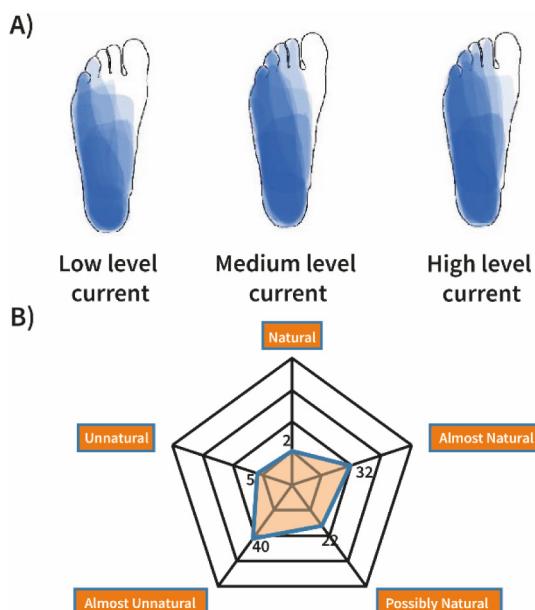


Fig. 2. Electrical stimulation of the tibial nerve in 10 healthy subjects. Following the stimulation, the projection areas of the induced sensation were collected based on the level of current applied (A) and the qualities of the sensations in terms of naturalness (B).

Ultra-conformable tattoo electrodes were used to stimulate the upper limb. The electrodes were positioned in correspondence of the median nerve. The reported sensations were collected in terms of position on the hand and quality, as shown in Fig. 3.

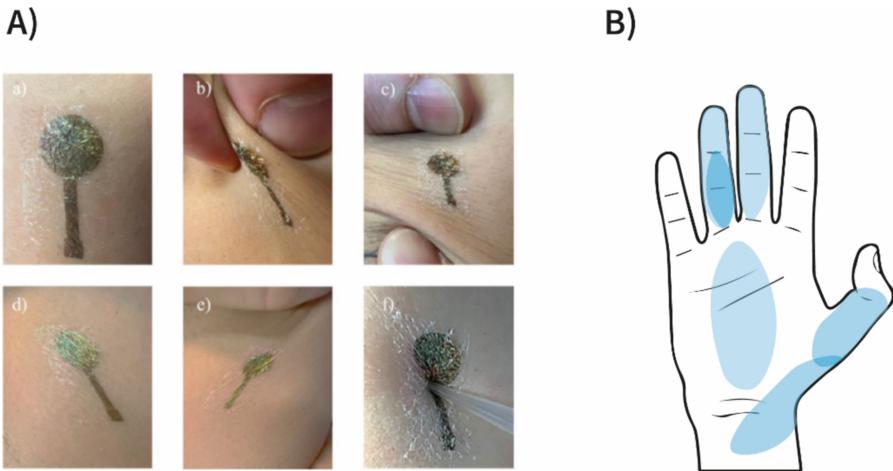


Fig. 3. Electrical stimulation using Tattoo electrodes. A) Tattoo electrodes allow high adhesion to tissues, ensuring they follow the skin's natural folds and remain adherent even following mechanical bending. B) Sensations collected following stimulation of the median nerve in three healthy subjects

3.2 Electrical Stimulation of Biohybrid Actuator

The soft robotics field has also verified the ability to stimulate and control excitable tissues by including biohybrid actuators based on skeletal muscle tissue [16]. In order to use biohybrid actuators, such as muscle tissues, in the robotic field, it is essential to control the actuator's contractions to control and maintain the flexions of the joints to be controlled. In particular, to create a structure such as a catheter, it would be necessary for the actuator to maintain the contraction to guarantee the routing of the catheter inside the blood vessels while still guaranteeing a rapid and precise contraction. Skeletal muscle tissue was selected to verify the suitability of the stimulator in the soft robotics sector, as shown in Fig. 4A-B. Skeletal muscle tissue was stimulated using symmetrical biphasic waveforms to induce tetanic contraction, as shown in Fig. 4C, or short contractions, as shown Fig. 4D. The tetanic contraction was obtained using stimulation trains between 20 and 35 Hz, while twitch was induced at 1 Hz.

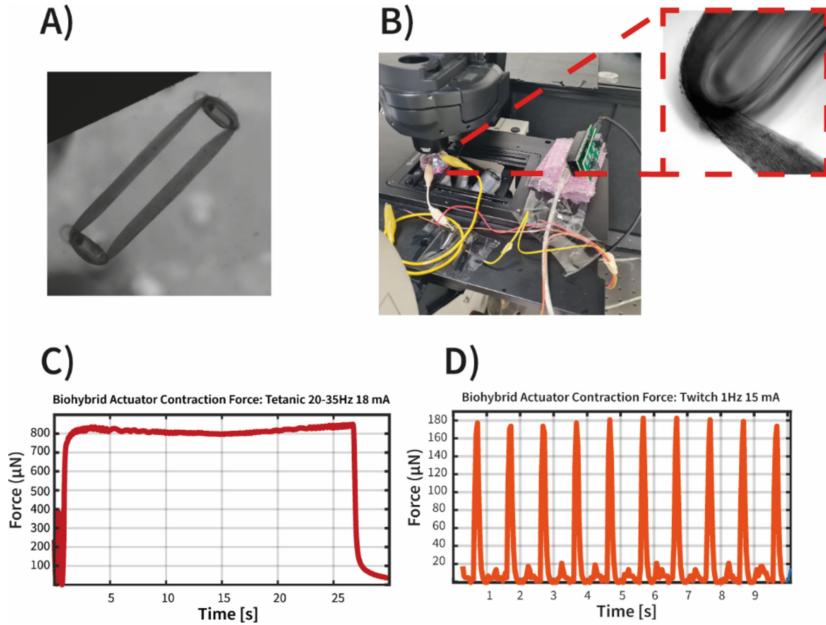


Fig. 4. The stimulator has been employed in the electrical stimulation of a biohybrid actuator for soft robotics applications. A) View of the biohybrid actuator. B) Stimulation setup. The setup is composed by the Leica Thunder Imaging system and the stimulator. C) The stimulator was capable of inducing controllable tetanic contraction on the actuator leading to contraction forces up to 800 μ N. D) The stimulator was capable of inducing controllable twitch contraction on the actuator.

3.3 Evaluation of Intracortical Electrodes for Invasive Stimulation

The system was also used in the preliminary evaluation of implantable electrodes for intracortical electrical stimulation. An example of the electrodes used is shown in Fig. 5A. The impedance was evaluated by immersing the electrodes in a physiological solution and imposing electrical stimuli using the stimulator. The voltage across the active stimulation sites was recorded and used to estimate the resistive part of the impedance. The resulting impedance is shown in Fig. 5B. The impedance of the active sites is always higher than 25 k Ω , showing how it is necessary to have a high voltage compliance to be able to stimulate effectively. Considering the voltage compliance of ± 90 V of the proposed device, an impedance of 25 k Ω leads to a maximum stimulation current equal to 3.6 mA, which is adequate for intracranial stimulation. However, in many cases, the impedance reaches values higher than 100 k Ω , a value that would limit the current to a maximum of 900 μ A.

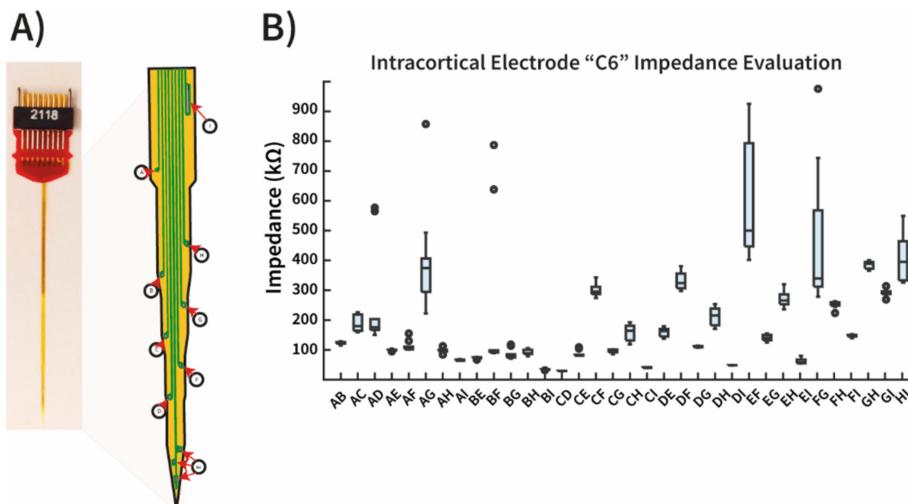


Fig. 5. Evaluation of intracortical electrodes for invasive stimulation. A) The electrode used is based on the TIME structure and is made up of nine different active stimulation sites B) The impedances of the active sites of the intracortical electrode were measured through the prototype. Stimulation sites have a minimum impedance of $25\text{ k}\Omega$ (CI) but can reach more than $500\text{ k}\Omega$, making high voltage compliance necessary for proper stimulation of nerve tissue.

4 Conclusions

The power consumption of the device has been measured to be 1.3 W. The device has been tested on healthy volunteers, showing the capability to stimulate the peripheral nervous system properly and induce referred sensations on the leg and the hand through commercial and ultra-conformable tattoo electrodes. The stimulator was employed to control and induce contractions on a biohybrid actuator based on skeletal muscle tissue, showing the capability to induce twitch and tetanic contraction, reaching huge contraction forces up to $800\text{ }\mu\text{N}$. The high voltage range also makes the stimulator suitable for working with intracortical electrodes, where the impedance of the stimulation sites can reach several hundreds of $\text{k}\Omega$. To verify this, the prototype was used to evaluate the impedance of the stimulation channels of an intracortical electrode and will soon be used for intracortical neural stimulation of rodents.

Acknowledgment. This project has received funding from the European Union's Horizon Europe research and innovation programme under grant agreement No. 101070328.

References

1. Zhao, S., Mehta, A.S., Zhao, M.: Biomedical applications of electrical stimulation. *Cellular and Molecular Life Sciences* **77**(14). Springer, pp. 2681–2699 (2020). <https://doi.org/10.1007/s00018-019-03446-1>

2. Pasluosta, C., Kiele, P., Stieglitz, T.: Paradigms for restoration of somatosensory feedback via stimulation of the peripheral nervous system. *Clinical Neurophysiology* **129**(4), 851–862. Elsevier Ireland Ltd. (2018). <https://doi.org/10.1016/j.clinph.2017.12.027>
3. Raspopovic, S., et al.: Restoring natural sensory feedback in real-time bidirectional hand prostheses. *Sci. Transl. Med.* **6**(222), 222ra19 (2014). <https://doi.org/10.1126/scitranslmed.3006820>
4. Zollo, L., et al.: Restoring tactile sensations via neural interfaces for real-time force-and-slippage closed-loop control of bionic hands (2019). <http://robotics.sciencemag.org/>
5. Tyler, D.J.: Neural interfaces for somatosensory feedback: Bringing life to a prosthesis. *Current Opinion in Neurology* **28**(6), 574–581. Lippincott Williams and Wilkins (2015). <https://doi.org/10.1097/WCO.0000000000000266>
6. Tan, D.W., et al.: A neural interface provides long-term stable natural touch perception. *Sci. Transl. Med.* **6**(257), 257ra138–257ra138 (2014). <https://doi.org/10.1126/scitranslmed.3008669>
7. Collu, R., et al.: Wearable high voltage compliant current stimulator for restoring sensory feedback. *Micromachines (Basel)* **14**(4) (2023). <https://doi.org/10.3390/mi14040782>
8. Collu, R., Earley, E.J., Barbaro, M., Ortiz-Catalan, M.: Non-rectangular neurostimulation waveforms elicit varied sensation quality and perceptive fields on the hand. *Sci. Rep.* **13**(1), 1588 (2023). <https://doi.org/10.1038/s41598-023-28594-0>
9. Scarpelli, A., Demofonti, A., Terracina, F., Ciancio, A.L., Zollo, L.: Evoking apparent moving sensation in the hand via transcutaneous electrical nerve stimulation. *Front Neurosci.* **14** (2020). <https://doi.org/10.3389/fnins.2020.00534>
10. Demofonti, A., Scarpelli, A., Cordella, F., Zollo, L.: Modulation of sensation intensity in the lower limb via Transcutaneous Electrical Nerve Stimulation. In: Proceedings of the Annual International Conference of the IEEE Engineering in Medicine and Biology Society, EMBS. Institute of Electrical and Electronics Engineers Inc. (2021). pp. 6470–6474. <https://doi.org/10.1109/EMBC46164.2021.9630871>
11. Ricotti, L., et al.: Biohybrid actuators for robotics: A review of devices actuated by living cells (2017). <https://www.science.org>
12. Ricotti, L., Menciassi, A.: Bio-hybrid muscle cell-based actuators. *Biomed. Microdevices* **14**(6), 987–998 (2012). <https://doi.org/10.1007/s10544-012-9697-9>
13. Collu, R., et al.: A microcontroller-based portable transcutaneous electrical nerve stimulator via ultra-comfortable tattoo electrodes for haptic feedback. In: *Lecture Notes in Electrical Engineering*, 385–395. Springer Science and Business Media Deutschland GmbH (2024). https://doi.org/10.1007/978-3-031-48711-8_47
14. Collu, R., et al.: A wearable electronic system for EEG recording. In: PRIME 2022 - 17th International Conference on Ph.D Research in Microelectronics and Electronics, Proceedings (2022). <https://doi.org/10.1109/PRIME55000.2022.9816817>
15. Mascia, A., et al.: Wearable system based on ultra-thin Parylene C tattoo electrodes for EEG recording. *Sensors* **23**(2) (2023). <https://doi.org/10.3390/s23020766>
16. Guix, M., et al.: Biohybrid soft robots with self-stimulating skeletons. *Sci. Robot.* **6**, 7577 (2020)



Investigating Cutaneous Mechanoreceptors for Neuromorphic Tactile Texture Classification

Haydar Al Haj Ali^(✉), Yahya Abbass, Christian Gianoglio, and Maurizio Valle

Department of Electrical, Electronic, Telecommunication Engineering,
and Naval Architecture DITEN, University of Genoa, Genoa, Italy

^(✉)Haydar.AlHajAli@edu.unige.it,
^{Yahya.abbass, christian.gianoglio, maurizio.valle}@unige.it

Abstract. This paper investigates the computational cost of modeling the response of the Type-I and Type-II cutaneous human mechanoreceptors for neuromorphic texture classification. We examined both the number of floating operations for modeling the receptors, and the number of synaptic operations for recurrent spiking neural networks (RSNNs) used in classification. Results show that deeper receptors (Type-II) require a greater computational cost to be modeled than those close to the surface (Type-I). However, RSNNs linked with deeper receptors exhibit a lower cost. We evaluated the energy consumption of the modeling and classification parts, each on its dedicated hardware device. The results suggest that pairing Type-I receptors with their corresponding RSNNs offers the best trade-off between energy consumption and classification accuracy.

Keywords: Tactile sensing system · mechanoreceptors · computational cost

1 Introduction

The physiological structure of human skin has inspired significant advancements in artificial tactile sensing systems, aiming to replicate the intricate perception of touch [1]. These advancements involve replicating the behavior of the cutaneous mechanoreceptors found in the glabrous skin such as Type-I receptors: RA-I, SA-I, and Type-II: RA-II, SA-II [2], by developing complex soft models [3] and circuits [4] that closely mimic their spiking behavior. However, the tactile sensing system operates under strict hardware constraints such as limited power budget and storing capacity [1]. For that reason, a trade-off between the computational cost of modeling and the necessary biological precision is crucial to meet the application's demands (i.e. robotics [5], and prosthetics [6]). The literature addresses and analyzes the utilization of the spiking behavior of mechanoreceptors, either in combination or individually, across diverse neuromorphic-based texture classification applications [2, 7, 8] and [9]. Nevertheless, there is a lack of examination regarding the effectiveness of each receptor and its contribution to

the overall system. In this work, we investigate the computational cost behind modeling each type of these mechanoreceptors for tactile texture classification, in terms of the required number of floating operations (FLOPs). In particular, the aforementioned mechanoreceptors were modeled to convert the tactile texture signals into spikes (digital pulses), followed by employing spiking neural networks (SNN) for classification. The investigation also covers the computational cost of the SNNs measured in the total number of synaptic operations (SOPs). Overall, this study sets the stage for determining the suitable level of biological abstraction from human skin for a future end-to-end neuromorphic framework for the extraction of tactile information.

2 Methodology

This study extends the work in [6], where the authors collected tactile signals from 8 artificial gratings under different controlled experimental conditions using 8 PVDF sensors and interface electronics. The experimental conditions include two sliding velocities ($v_1 = 8.6 \text{ mm/s}$, and $v_2 = 13.7 \text{ mm/s}$) and three indentation forces ($f_1 = 3 \text{ N}$, $f_2 = 6 \text{ N}$, and $f_3 = 12 \text{ N}$). All the collected signals were merged in a single dataset (D_{mixed}) and converted into spikes through an encoding layer comprising 8 SA-I and 8 RA-I mechanoreceptors (the tactile signal of each PVDF is used to model 1 SA-I and 1 RA-I). Following this, the emitted spikes were classified using a recurrent spiking neural network (RSNN) trained by the Surrogate Gradient Descent (SGD) [10]. As reported in [6], modeling the SA-I and RA-I mechanoreceptors was done in two steps: 1) converting the tactile signals into appropriate input current (Eq. 1 and Eq. 2), and 2) applying this current to the Leaky-Integrate-and-Fire (LIF) neuron for encoding and spike emission (Eq. 3). The equations are as follows:

$$I_{SA-I}(t) = SC_{SA-I} \times V_{sensor}(t), \quad (1)$$

$$I_{RA-I}(t) = SC_{RA-I} \times \left| \frac{d}{dt} V_{sensor}(t) \right| \quad (2)$$

$$\tau_m \frac{du(t)}{dt} = u_{rest} - u(t) + R_m \times I(t) \quad (3)$$

where I_{SA-I} and I_{RA-I} are the SA-I and RA-I currents processed from the sensor signals $V_{sensor}(t)$, and both SC_{SA-I} and SC_{RA-I} are their corresponding scaling coefficients. The generated $I_{SA-I}(t)$ and $I_{RA-I}(t)$ are applied as input current $I(t)$ to the LIF neuron with the following parameters: τ_m is the voltage decay constant, $u(t)$ is the voltage membrane of the neuron, u_{rest} is the resting voltage value after spike emission, and R_m is the resistance (1Ω). The applied $I(t)$ will be accumulated in the $u(t)$ until reaching a defined threshold V_{th} and emitting a spike. The chosen parameter values are: $SC_{SA-I} = 3200/\text{M}\Omega$, $SC_{RA-I} = 3200/\text{M}\Omega$, $\tau_m = 10 \text{ ms}$, $u_{rest} = -65 \text{ mV}$, and $V_{th} = -55 \text{ mV}$.

In this work, we model the SA-II and RA-II mechanoreceptors to develop a new encoding layer (SA-II & RA-II) as follows [2]:

$$I_{SA-II}(t) = SC_{SA-II} \times V_{sensor}(t), \quad (4)$$

$$I_{RA-II}(t) = SC_{RA-II} \times \left| \frac{d^2}{dt^2} V_{sensor}(t) \right| \quad (5)$$

where I_{SA-II} and I_{RA-II} are the SA-II and RA-II currents, with $SC_{SA-II} = SC_{RA-II} = 3200/\text{M}\Omega$ and $SC_{RA-II} = 70000/\text{M}\Omega$ scaling coefficients respectively. The two input currents are applied to the LIF neurons with the same parameters chosen in [6], with a change in u_{rest} (-100 mV instead of -65 mV) only for the emulation of the SA-II to exhibit a spike frequency adaption with a more uniform Inter-pike interval. We employed the same RSNNs used in [6] (with hidden layer (N) sizes 20, 30, 40, and 50), trained with SGD to classify these gratings based on the emitted spikes from the new encoding layer. We used the same dataset D_{mixed} with an input duration of 150 ms (300 time steps (t_s)).

3 Preliminary Results

3.1 Classification Accuracy and Computational Cost

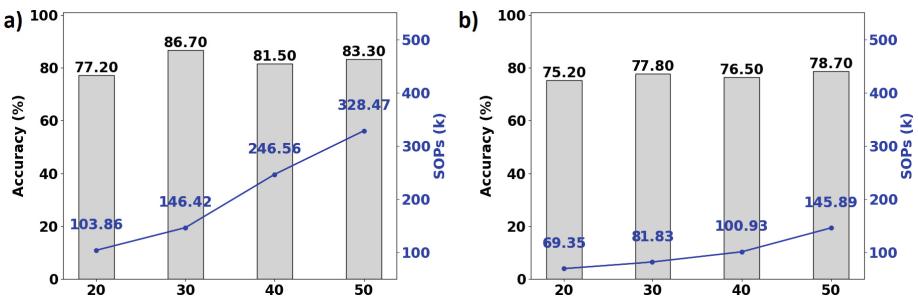


Fig. 1. Classification accuracy and SOPs of the RSNNs linked with RA-I & SA-I (a) and RA-II & SA-II (b). x-axis represents the hidden layer size (N) of each RSNN. y1-axis (left) is the accuracy (%). y2-axis (right) is the number of SOPs.

Figure 1 shows the results of the RSNNs already obtained in [6] using the encoding layer RA-I & SA-I (a), and the RA-II & SA-II combination (b) implemented in this study. In general, the RSNNs associated with RA-I & SA-I exhibited higher classification accuracy (average of $\approx 5\% \pm 2.46\%$) than RSNNs with RA-II & SA-II. However, this comes at the cost of a higher number of SOPs ($\approx 1.99\%$ average ratio). We measured the computational cost of modeling each

receptor, including the preprocessing stage (Eqs. 4 and 5), and LIF neuron simulation in terms of FLOPs per single time step (t_s) and for the entire input duration (300 t_s), following the guidelines in [11] and [12] respectively. Table 1 reports the obtained values. Modeling the SA-I & RA-I combination [5] requires 5.7 k FLOPs. Conversely, modeling the SA-II & RA-II combination requires higher #FLOPs = 6.6 k. This can be attributed mainly to the more complex mathematical operations applied to emulate the response of the RA-II receptors (i.e. second order of derivation compared to the first order applied for RA-I) that requires higher number of FLOPs. However, the RSNNs accompanied by the SA-I & RA-I combination attained more SOPs across all the N sizes (Fig. 1). This identifies that Type-I receptors (SA-I & RA-I) exhibit a higher firing rate (spike count) compared to Type-II receptors (SA-II & RA-II), which allowed the RSNNs to achieve higher classification accuracy.

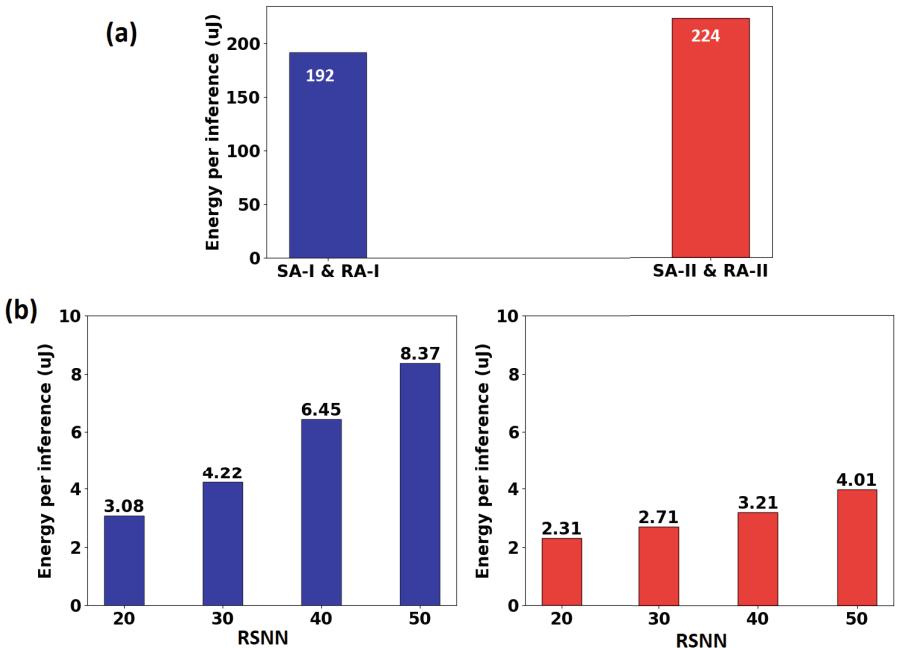


Fig. 2. Estimated energy consumption per inference for the encoding procedure on the Intel i7-4960X CPU (a), and for the RSNNs on the Intel Loihi chip (b). Blue bars correspond to the classification approach based on SA-I & RA-I receptors. Red bars correspond to the SA-II & RA-II approach.

3.2 Energy Consumption Estimation

We used the obtained computational cost to estimate the energy consumption on dedicated hardware devices. In particular, we used the energy consumption per

Table 1. # FLOPs of Modeling the Mechanoreceptors per one sensor.

combination	Preprocessing		LIF		Total
	t_s	$300 t_s$	per t_s	$300 t_s$	
SA-I & RA-I	$1 + 8 = 9$	$300 + 2.4 \text{ k} = 2.7 \text{ k}$	$5 + 5 = 10$	$(1.5 + 1.5 = 3) \text{ k}$	5.7 k
SA-II & RA-II	$1 + 11 = 12$	$300 + 3.3 \text{ k} = 3.6 \text{ k}$	$5 + 5 = 10$	$(1.5 + 1.5 = 3) \text{ k}$	6.6 k

FLOP reported in [13] to estimate the hardware cost of each encoding combination on the Intel i7-4960X CPU. Consequently, we used the energy consumption per synaptic operation (SOP) on the Intel Loihi research chip in [14] for the RSNNs inferences. Figure 2 depicts the obtained values. As illustrated, emulating the SA-II & RA-II mechanoreceptors exhibit ≈ 32 uJ higher energy consumption compared to the SA-I & RA-I on the i7-CPU. Conversely, the RSNNs associated with the latter combination exhibited an average of $\approx 2.47 \pm 1.41$ uJ higher energy consumption on the Loihi chip.

3.3 Discussion

To investigate the suitable encoding combination for neuromorphic texture classification, we should assess the trade-off between the obtained energy consumption and classification accuracy. In particular, the $\approx 2.47 \pm 1.41$ uJ gain in energy exhibited by the RSNNs associated with the SA-I & RA-I allowed for an improvement of $\approx 5\%$ in accuracy compared to the RSNNs with SA-II & RA-II. Additionally, emulating the former mechanoreceptors combination requires ≈ 32 uJ less energy compared to the latter. Therefore, the SA-I & RA-I encoding combination can be represented as more suitable for texture classification. For example, an RSNN with $N = 30$ achieved a classification accuracy of 86.3% with a total energy consumption of 196.22 uJ. This is at least 31.7 uJ less than any RSNNs linked with the SA-II & RA-II combination while showing a superiority of at least 8% in classification accuracy.

4 Conclusion and Future Work

In this study, we investigated the computational cost behind modeling Type-I and Type-II cutaneous mechanoreceptors for neuromorphic texture classification. We found that modeling the RA-II & SA-II combination requires higher computational cost compared to SA-I & RA-I in [6]. However, the RSNNs associated with the former combination exhibited lower cost. We attribute the disparity in SOPs to the firing rate of each type of receptor. This suggests that deeper receptors have a lower firing rate compared to the shallower receptors. We estimated the energy consumption of both modeling these mechanoreceptors and performing classification through the RSNNs, each on a dedicated hardware device using guidelines from the literature(i.e. CPU for emulation and encoding, and Intel Loihi chip for RSNN classification). We found that the classification

approach liked by the SA-I & RA-I receptors exhibits the best trade-off between accuracy and energy consumption. Future work will focus on real hardware deployment and assessing the modeling and classification components on the same devices. This will allow for a comprehensive comparison using additional evaluation metrics, such as execution time, power, and energy consumption, since there may be differences between the estimated and actual values.

References

1. Dahiya, R.S., Mittendorfer, P., Valle, M., Cheng, G., Lumelsky, V.J.: Directions toward effective utilization of tactile skin: a review. *IEEE Sens. J.* **13**(11), 4121–4138 (2013)
2. Rostamian, B., et al.: Texture recognition based on multi-sensory integration of proprioceptive and tactile signals. *Sci. Rep.* **12**(1), 21690 (2022)
3. Ali, H.A.H., Dabbous, A., Ibrahim, A., Valle, M.: Spiking neural network based on threshold encoding for texture recognition. In: 2022 29th IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 1–4. IEEE (2022)
4. Alea, M.D., et al.: A fingertip-mimicking 12×16 $200\text{ }\mu\text{m}$ -resolution e-skin taxel readout chip with per-taxel spiking readout and embedded receptive field processing. *IEEE Trans. Biomed. Circ. Syst.* (2024)
5. Bologna, L.L., Pinoteau, J., Brasselet, R., Maggiali, M., Arleo, A.: Encoding/decoding of first and second order tactile afferents in a neurorobotic application. *J. Physiol.-Paris* **105**(1–3), 25–35 (2011)
6. Ali, H.A.H., Abbass, Y., Gianoglio, C., Ibrahim, A., Oh, C., Valle, M.: Neuromorphic Tactile sensing system for textural features classification. *IEEE Sens. J.* (2024)
7. Rasouli, M., Chen, Y., Basu, A., Kukreja, S.L., Thakor, N.V.: An extreme learning machine-based neuromorphic tactile sensing system for texture recognition. *IEEE Trans. Biomed. Circuits Syst.* **12**(2), 313–325 (2018)
8. Gupta, A.K., Nakagawa-Silva, A., Lepora, N.F., Thakor, N.V.: Spatio-temporal encoding improves neuromorphic tactile texture classification. *IEEE Sens. J.* **21**(17), 19038–19046 (2021)
9. Ali, H.A.H., Dabbous, A., Ibrahim, A., Valle, M.: Assessment of recurrent spiking neural networks on neuromorphic accelerators for naturalistic texture classification. In: 2023 18th Conference on Ph. D Research in Microelectronics and Electronics (PRIME), pp. 285–288. IEEE (2023)
10. Neftci, E.O., Mostafa, H., Zenke, F.: Surrogate gradient learning in spiking neural networks: bringing the power of gradient-based optimization to spiking neural networks. *IEEE Signal Process. Mag.* **36**(6), 51–63 (2019)
11. Thant, H.A., San, K.M., Tun, K.M.L., Naing, T.T., Thein, N.: Mobile agents based load balancing method for parallel applications. In: 6th Asia-Pacific Symposium on Information and Telecommunication Technologies, pp. 77–82. IEEE (2005)
12. Izhikevich, E.M.: Which model to use for cortical spiking neurons? *IEEE Trans. Neural Netw.* **15**(5), 1063–1070 (2004)
13. Degnan, B., Marr, B., Hasler, J.: Assessing trends in performance per watt for signal processing applications. *IEEE Trans. Very Large Scale Integrat. (VLSI) Syst.* **24**(1), 58–66 (2015)
14. Davies, M., et al.: Loihi: a neuromorphic manycore processor with on-chip learning. *IEEE Micro* **38**(1), 82–99 (2018)



On-Edge 1-D Convolutional Neural Network for Hand-Gesture Classification

Daniella Shebly^{1,2(✉)}, Haydar Al Haj Ali¹, Mohamad Yaacoub¹, Hussein Chibli², Maurizio Valle¹, and christian Gianoglio¹

¹ DITEN, University of Genoa, Genoa, Italy
daniella.shebly@edu.unige.it

² MECRL Laboratory, Lebanese University, Beirut, Lebanon

Abstract. This study presents the development of a real-time hand gesture classification system utilizing inertial measurement units (IMUs) and a lightweight 1-D convolutional neural network (CNN) implemented on an embedded system. The IMU sensors were positioned on the index and thumb of the participants' hands to accurately capture data for four distinct gestures, each representing different geometric shapes: square, triangle, circle, and line. Experimental results indicated that the proposed system achieved a classification accuracy of 75%, with an inference time of 11.82 milliseconds and an energy consumption of 0.58 millijoules.

Keywords: Real-time classification · embedded system · hand gestures recognition

1 Introduction

Integrating intelligence into numerous biomedical applications has recently garnered significant interest [1]. These applications encompass prosthetic devices and rehabilitation procedures that leverage feedback systems powered by intelligent actions [2]. This trend is primarily driven by increasingly powerful computational paradigms in machine learning (ML). However, embedding intelligence into these applications is constrained by hardware limitations, such as limited storage capacity and power budgets. Consequently, developing lightweight computing methods to meet these hardware constraints is essential [3]. Several recent studies showcase innovative methods for overcoming these constraints. For instance, Liu et al. proposed a finger-worn ring with an inertial sensor for recognizing on-surface handwriting, achieving a character error rate of 1.05% and a word error rate of 7.28% using a combination of LSTM and CNN models [4]. Mummadri et al. introduced an IMU-based glove that recognizes 22 French sign language gestures with 92% accuracy in real-time using onboard processing and data fusion techniques [5]. Similarly, Ott et al. evaluated and compared the performance of various handwriting recognition models using sensor-enhanced pens, highlighting the efficacy of different models and augmentation techniques, and suggesting future research directions to improve classification accuracy for

diverse writing styles [6]. Younas et al. developed a low-cost IMU sensor system for finger air writing that captures and reconstructs 2D trajectories from casual finger motions to create human-readable virtual texts, validated through a user study [7]. Wehbi et al. presented a digital pen that uses an IMU for handwriting trajectory reconstruction and word recognition, achieving a normalized error rate of 0.176 and a character error rate of 19.51% [8]. Pan et al. discussed a method for reconstructing handwriting trajectories using low-cost sensors, achieving high accuracy in recognizing written characters through effective data preprocessing and model training [9]. Additionally, Lichtenauer et al. combined Statistical Dynamic Time Warping (SDTW) with novel statistical classifiers for sign language recognition, demonstrating improved performance over traditional HMM and DTW methods [10]. Wang et al. presented an IMU-based pen and its trajectory reconstruction algorithm designed to accurately reconstruct motion trajectories and recognize handwritten digits by minimizing sensor noise and drift through an orientation error compensation method [11]. Furthermore, Wang et al. introduced an accelerometer-based digital pen and a trajectory recognition algorithm that translates acceleration signals into feature vectors, enabling online recognition of handwritten digits and gestures with high accuracy using probabilistic neural networks [12]. Building on these advancements, this paper proposes an end-to-end framework based on a 1-D convolutional neural network (CNN) implemented on a low-power microcontroller unit (MCU) for real-time hand-gesture classification. The system demonstrates the feasibility of achieving a classification accuracy of 75% with an inference time of 11.82 ms and energy consumption of less than 1mJ per inference. This advancement represents a significant step forward in integrating ML into constrained hardware environments, making it a promising candidate for further investigation in human-in-the-loop or closed-loop biomedical applications [13].

2 Methodology

The developed system (Fig. 1) employed an STM32F401RE microcontroller board in addition to two ICM-20948 Inertial Measurement Unit (IMU) sensors to predict hand gestures in real-time. The IMU sensors, each integrating a 3-axis gyroscope, a 3-axis accelerometer, and a 3-axis magnetometer, were strategically positioned to capture comprehensive motion data from the top of the thumb and index fingers. This raw data from the IMUs was fed into a carefully designed 1-D Convolutional Neural Network (CNN) [14], which processed and elaborated on the sensor inputs to predict hand gestures. The trained CNN model was then deployed on the STM32 board, enabling the system to perform real-time inference, thereby demonstrating a practical application of embedded machine learning for gesture recognition and hand motion [15]. The choice of the STM32F401RE microcontroller was driven by its balance of computational power and low energy consumption, making it ideal for wearable applications where battery life is crucial. The system's architecture emphasizes modularity and scalability, allowing for future enhancements and easy integration of addi-

tional sensors or improved algorithms. Moreover, this setup has potential applications beyond gesture recognition, such as in robotics, virtual reality, and other domains requiring precise motion tracking and real-time data processing.

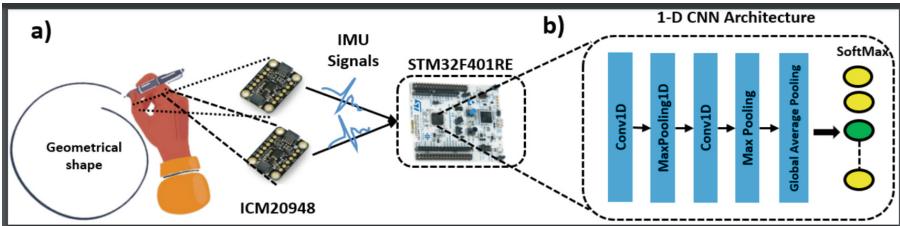


Fig. 1. Block diagram of the proposed system: a) data collection of hand gestures; b) 1-D CNN architecture deployed on the STM32.

2.1 Dataset

Figure 1 (a) shows the experimental setup for the data collection. The system incorporated two 9-axis IMU sensors mounted to the thumb and index of the subject's hand. These sensors were connected to the STM32 using the I2C protocol. Specifically, the accelerometer data from the sensors provided information along three axes: x, y, and z. The STM32 board was connected to the host PC via USB for seamless data acquisition and processing. The data were collected with a high sampling rate of 200 samples per second, ensuring that even the most rapid hand movements were accurately recorded.

Three subjects participated in the experiment, each tasked with drawing four distinct geometric shapes (square, triangle, circle, and line) using a pen on paper. The choice of these shapes was to provide a diverse dataset. Each subject conducted 20 trials for each shape, with each trial lasting 1 s, resulting in precise and consistent data capture across all trials. In total, 240 trials were recorded, providing a robust dataset for subsequent analysis. This extensive dataset is essential for training and validating machine learning models aimed at recognizing and classifying different hand movements based on accelerometer data.

2.2 Elaboration System

The elaboration system is shown in Fig. 1(b) and involved a 1-D CNN to process the IMU signals of each gesture and perform subsequent classification. Once the 1-D CNN was trained, it was deployed on the STM32 microcontroller performing an online classification based on the acquired signals. The network processed data from a 2D tensor with a shape 200×6 , where 200 represents the time steps and $6 = 3 \text{ axes} \times 2 \text{ IMUs}$ are the input channels. The dataset was split into 60% for training, 20% validation, and 20% testing. The resulting best model obtained

by tuning the parameters of the 1-D CNN and evaluating it on the validation set has the following architecture: two Conv1D layers with 32 and 16 filters in the first and second layers, respectively, with a kernel size of 5, followed by a batch normalization layer. The activation function of each convolution layer is the ReLU. Max-pooling operation with dimension 2×1 is applied after each convolution layer, effectively reducing the temporal dimension by half while preserving the feature maps' spatial structure. After the convolution and pooling layers, a global average pooling layer is employed to reduce each feature map to a single value by computing the average of all values in the feature map. This reduces the spatial dimensions to a single vector, which is then fed into the output layer. The output layer is composed of 4 neurons with softmax as an activation function, to classify the 4 hand gestures (circle, triangle, line, square). The softmax activation function ensures that the output is a probability distribution, where each neuron represents the probability of a particular gesture class. The model was implemented in Python using the TensorFlow framework. It was trained with the Adam optimizer (learning rate = 0.001) for efficient convergence. The training process involved iterating over the training data multiple times (epochs) and adjusting the weights of the network to minimize the loss function. Once the training was complete, the model was quantized to reduce its size and increase inference speed, a crucial step for deploying it on the resource-constrained STM32 microcontroller. The quantized model was then converted to the TensorFlow Lite format, which is optimized for deployment on embedded devices. The performance of the system was evaluated using four metrics: classification accuracy (%), inference time (ms), power consumption (mW), and energy consumption per inference (mJ). The classification accuracy measures how well the model correctly identifies the gestures, while the inference time indicates how quickly the model can make predictions. Power consumption and energy consumption per inference are critical metrics for battery-operated devices, as they reflect the system's efficiency. To measure the power and energy consumption of the MCU system, the X-NUCLEO-Ipm01a board was used. This board allows for precise measurement of the power and energy used by the microcontroller during inference, providing valuable insights into the system's overall efficiency and suitability for real-world applications.consumption of the MCU system.

Table 1. Experimental Results

Model	Accuracy (%)	Inference (ms)	Power (mW)	Energy (mJ)
1-D CNN	75	11.82	49.14	0.58

3 Results

Table 1 presents the experimental results of the 1-D Convolutional Neural Network (CNN) model used in the study. The model achieved an accuracy of 75%,

indicating that it correctly classified 75% of the hand movement patterns associated with the different geometric shapes. The inference time for the model is 11.82 milliseconds, which reflects the time taken to process and classify a single instance of the input data. This relatively low inference time demonstrates the model's efficiency, making it suitable for real-time applications where quick responses are essential. The power consumption of the model is 49.14 milliwatts (mW), highlighting the energy requirements for running the model on the hardware used. This measurement is critical for evaluating the model's feasibility for deployment in portable and low-power devices, such as wearable sensors or mobile applications. Finally, the energy consumption per inference is 0.58 millijoules (mJ). This metric combines the power consumption and inference time to provide a comprehensive view of the energy efficiency of the model. Low energy consumption is particularly advantageous for battery-operated devices, ensuring longer operational periods without the need for frequent recharging. Overall, the experimental results indicate that the 1-D CNN model is both accurate and efficient, balancing the trade-offs between performance and energy consumption, making it a feasible option for real-time hand movement recognition applications.

4 Conclusion and Future Work

In this paper, we have developed an embedded system utilizing a 1-D CNN and a low-power host for real-time hand gesture classification, achieving a 75% accuracy with an inference time of 11.82 ms and an energy consumption of 0.58 mJ. Future improvements include the implementation of a more biologically realistic IMU sensor setup via a wearable glove and the integration of tactile sensors [16] for enhanced sensory data[17]. Investigating the sensitivity of IMU positioning and 3D orientation, expanding the dataset to include a wider variety of gestures and participants, and ensuring inclusiveness for left-handed users will further enhance the system's robustness and applicability. These enhancements will enable the system to perform more sophisticated tasks related to human-like perception and proprioception, expanding its potential in biomedical and assistive technologies. Additionally, the system's ability to be customized for specific user needs and environments will make it a adaptable tool in various medical and technological fields. By leveraging advanced machine learning techniques and sensor integrations, our system improves human-computer interaction.

References

1. Shih, B., et al.: Electronic skins and machine learning for intelligent soft robots. *Sci. Rob.* **5**(41), eaaz9239 (2020)
2. Abbass, Y., Dosen, S., Seminara, L., Valle, M.: Full-hand electrotactile feedback using electronic skin and matrix electrodes for high-bandwidth human-machine interfacing. *Phil. Trans. R. Soc. A* **380**(2228), 20210017 (2022)
3. Amin, Y., Gianoglio, C., Valle, M.: Embedded real-time objects' hardness classification for robotic grippers. *Futur. Gener. Comput. Syst.* **148**, 211–224 (2023)

4. Liu, Z.-T., Wong, D.P., Chou, P.H.: An imu-based wearable ring for on-surface handwriting recognition. In: 2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT), pp. 1–4. IEEE (2020)
5. Mummadri, C.K., et al.: Real-time and embedded detection of hand gestures with an imu-based glove. In: Informatics, vol. 5, no. 2, p. 28 (2018)
6. Ott, F., Rügamer, D., Heublein, L., Hamann, T., Barth, J., Bischl, B., Mutschler, C.: Benchmarking online sequence-to-sequence and character-based handwriting recognition from imu-enhanced pens. Int. J. Doc. Anal. Recogn. (IJDAR) **25**(4), 385–414 (2022)
7. Younas, J., Margarito, H., Bian, S., Lukowicz, P.: Finger air writing-movement reconstruction with low-cost imu sensor. In: MobiQuitous 2020-17th EAI International Conference on Mobile and Ubiquitous Systems: Computing, Networking and Services, pp. 69–75 (2020)
8. Wehbi, M., et al.: Surface-free multi-stroke trajectory reconstruction and word recognition using an imu-enhanced digital pen. Sensors **22**(14), 5347 (2022)
9. Pan, T.-Y., Kuo, C.-H., Liu, H.-T., Hu, M.-C.: Handwriting trajectory reconstruction using low-cost imu. IEEE Trans. Emerg. Topics Comput. Intell. **3**(3), 261–270 (2018)
10. Lichtenauer, J.F., Hendriks, E.A., Reinders, M.J.: Sign language recognition by combining statistical dtw and independent classification. IEEE Trans. Pattern Anal. Mach. Intell. **30**(11), 2040–2046 (2008)
11. Wang, J.-S., Hsu, Y.-L., Liu, J.-N.: An inertial-measurement-unit-based pen with a trajectory reconstruction algorithm and its applications. IEEE Trans. Ind. Electron. **57**(10), 3508–3521 (2009)
12. Wang, J.-S., Chuang, F.-C.: An accelerometer-based digital pen with a trajectory recognition algorithm for handwritten digit and gesture recognition. IEEE Trans. Ind. Electron. **59**(7), 2998–3007 (2011)
13. Seminara, L., et al.: A hierarchical sensorimotor control framework for human-in-the-loop robotic hands. Sci. Rob. **8**(78), eadd5434 (2023)
14. Gianoglio, C., Ragusa, E., Zunino, R., Valle, M.: 1-d convolutional neural networks for touch modalities classification. In: 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), pp. 1–6. IEEE (2021)
15. Khalife, R., Mrad, R., Dabbous, A., Ibrahim, A.: Real-time implementation of tiny machine learning models for hand motion classification. In: International Conference on Applications in Electronics Pervading Industry, Environment and Society, pp. 487–492. Springer, Heidelberg (2023)
16. Ali, H.A.H., Abbass, Y., Gianoglio, C., Ibrahim, A., Oh, C., Valle, M.: Neuromorphic tactile sensing system for textural features classification. IEEE Sens. J. (2024)
17. D'Alonzo, M., Dosen, S., Cipriani, C., Farina, D.: HyVE—hybrid vibro-electrotactile stimulation—is an efficient approach to multi-channel sensory feedback. IEEE Trans. Haptics **7**(2), 181–190 (2013)



TinyML Acceleration with MAX78000

Ali Dabbous , Luca Lazzaroni , Francesco Bellotti, Sara Muñoz Presentación,
Alessandro Pighetti , and Riccardo Berta

Department of Electrical, Electronic and Telecommunication Engineering (DITEN), University
of Genoa, Via Opera Pia 11a, 16145 Genova, Italy
luca.lazzaroni@edu.unige.it

Abstract. The advancement of edge devices equipped with specialized hardware accelerators has brought the deployment and execution of Deep Neural Network (DNN) models nearer to users and real-world sensor systems. This paper investigates the potential of the MAX78000 microcontroller in accelerating Tiny Machine Learning applications, which require real-time processing and low power consumption. We compare its performance against other platforms like the STM32H7 and Raspberry Pi 4, focusing on a case study involving the detection of miniature mobile robots using an ultra-low-resolution Time-of-Flight sensor. Despite slightly lower accuracy, the MAX78000 outperforms other platforms in terms of inference time, power, and energy consumption, making it a reliable choice for power-constrained applications.

Keywords: Convolutional Neural Network · Hardware Accelerator ·
MAX78000 · Power Consumption · Time-of-Flight · Tiny Machine Learning

1 Introduction

In recent years, the field of machine learning (ML) has expanded beyond data centers and cloud environments to encompass edge devices, giving rise to what is now known as Tiny Machine Learning (TinyML) [1]. TinyML refers to the tailored deployment of lightweight ML models on devices with limited computational resources, enabling intelligent decision-making directly on the device with minimal energy consumption (e.g., [2]). This approach is particularly advantageous for applications where rapid, real-time processing is essential, and connectivity may be limited or non-existent. Examples include predictive maintenance sensors in remote industrial locations, wearable devices, sports and human activities, and smart home systems [3–5].

One of the main challenges in TinyML is balancing performance with power constraints. The MAX78000, a brand-new ultra-low-power Microcontroller Unit (MCU) with a hardware-based neural network (NN) accelerator, represents a significant advancement in this field. This MCU is specifically designed for convolutional neural network (CNN) computations and, therefore, exhibits an exceptional ability to reduce inference times and energy usage.

This paper aims to investigate the effectiveness of the MAX78000 in accelerating TinyML applications. To this end, we compare its performance in terms of accuracy, inference time, and power and energy consumption against other platforms well-known in the embedded domain. Specifically, the STM32H7 board is favored in professional applications for its robust processing capabilities, and the Raspberry Pi 4, is popular in commercial and educational settings for its versatility. The focus is on a specific case study involving the detection of miniature mobile robots using an ultra-low resolution Time-of-Flight (ToF) sensor, a common field of study in the TinyML domain [6]. As mobile robots are nearly always battery-powered, optimizing energy consumption is crucial to extend operational lifespan and enhance the practicality of micro-robotics applications in real-world scenarios.

2 Related Work

With the rise of the IoT paradigm, it has become necessary to make embedded devices smart so that they are not directly dependent on the cloud, both during data collection [7, 8] and inference [9, 10]. In this scenario, TinyML has garnered significant attention due to its potential to bring intelligent processing to resource-constrained devices. A cornerstone is a work by Han et al. [11], which introduced model compression techniques such as pruning and quantization to reduce the size and enhance the speed of deep learning models in hardware-limited environments. Subsequent research has built upon these foundations, incorporating hardware-specific optimizations to further enhance performance (e.g., [9, 12]).

Regarding embedded devices suitable for TinyML tasks, the STM32 MCU family, particularly the STM32H7 series, has been extensively used for its high processing power and versatility. Falaschetti et al. [4] implemented high-performance CNNs on the STM32H7, highlighting its capability to handle complex ML tasks with high accuracy. On the other hand, the Raspberry Pi has emerged as a popular platform for both educational purposes and commercial applications due to its versatility and ease of use. However, while it offers commendable flexibility and computational power, it falls short in energy efficiency compared to more specialized MCUs [13]. With its hardware-based neural network accelerator, the MAX78000 is designed specifically for executing CNN computations efficiently. Recent studies [14, 15] indicated that the MAX78000 significantly outperforms general-purpose MCUs and even some specialized ML hardware in terms of inference time and efficiency for CNN tasks. This positions the MAX78000 as a promising candidate for applications requiring low-power, real-time inference capabilities.

3 MAX78000 Platform

3.1 Hardware Overview

The MAX78000 is an AI microcontroller engineered for running neural networks with ultra-low power consumption on small-scale devices. It comprises two primary processing modules: a dual-core microcontroller (MCU) and a convolutional neural network

(CNN) accelerator. The microcontroller features an Arm Cortex-M4 processor with a floating-point unit (FPU) operating at up to 100 MHz, alongside a 32-bit RISC-V co-processor running at up to 60 MHz. The hardware-based CNN accelerator includes 64 parallel physical channel processors, each equipped with a pooling unit and a convolutional engine with dedicated weight memory. The CNN engine offers 442 KB of weight storage memory and supports weights of 1, 2, 4, and 8 bits. Additionally, it has 512 KB of data memory. Beyond the CNN engine's memory, the MAX78000 includes on-chip system memory for the microcontroller core, comprising 512 KB of flash memory and up to 128 KB of SRAM.

During inference, data is read from the shared data memory (one instance shared by four processors) and transferred to the accelerator's dedicated data memory. Multiple layers can be connected in sequence, with each layer's operations individually configurable. The output from one layer serves as the input for the next layer, supporting up to 32 layers. In-flight pooling and in-flight element-wise operations are not counted as separate layers.

3.2 Development Workflow

Figure 1 illustrates the MAX78000 development workflow. Since the MAX78000 does not support on-chip training, models must be trained and compiled in a desktop environment before being deployed on the chip for inference using the model binary. MAX78000 supports PyTorch for model development, offering custom layer implementations for quantized and fused operations, as well as pipelines for quantization-aware training or post-training quantization.

After training, specific tools convert PyTorch checkpoints or TensorFlow-exported ONNX files into C code, which can then be compiled and executed on the MAX78000 in a process called synthesis. During synthesis, a YAML file defining the model architecture and processor IDs is created, along with a dataset sample file.

Following training and synthesis, the deployment process takes place, where the converted C code is embedded on the MAX78000, and execution is performed. The device supports a range of accelerated operations, including 1D convolution with kernel sizes from 1 to 9, 2D convolution with 1×1 or 3×3 kernel sizes, linear (fully connected) layers, max pooling, average pooling, ReLU and Abs activations, and batch normalization. Other operations can be executed on the Arm or RISC-V cores, though these will increase latency.

During model execution, the MCU transfers configuration data, input data, and weights to the CNN accelerator, which processes each layer sequentially. For each layer, kernels are loaded from memory, and input channels are assigned to convolutional processors, achieving acceleration through parallel processing across multiple processors.

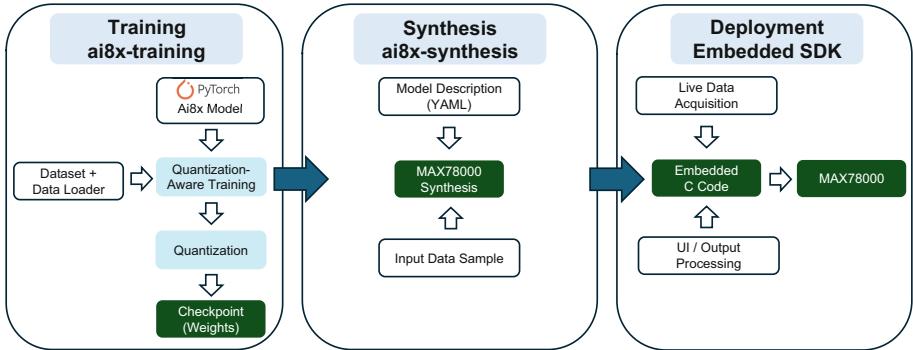


Fig. 1. MAX78000 Development Workflow.

4 Experiment

4.1 Dataset

The dataset we used, referenced as [16], is composed of 4,150 distinct ToF images, both with and without a miniature mobile robot in the observed environment, which is predominantly made up of sand and rocks. These images are labeled for binary classification purposes. Images have been captured through an ultra-low resolution ToF sensor, capable of measuring distances up to 4 m at a frequency of 60 Hz. This sensor can capture depth images with a resolution of up to 8×8 8-bit pixels, where each pixel represents a distance ranging from 0 to 50 cm.

4.2 Training Setup

For the training of our model, we opted for a CNN-based architecture. The architecture comprises two convolutional layers followed by two fully connected layers. The activation function used is the Rectified Linear Unit (ReLU). The experiment is set with a learning rate of 0.001, employing the Adam optimizer. In all the experiments the network is trained over 100 epochs to keep consistency.

Given the MCU target, we employed a Quantization-Aware Training (QAT) approach for model training [17], quantizing all the NN weights to 8 bits. QAT is a method that enables the model to adapt to the quantization process during its training phase. Unlike post-training quantization techniques, QAT offers the advantage of enabling the model to adjust to quantization during training, potentially leading to more robust performance during inference. This is attributed to the model's ability to learn and compensate for the quantization errors introduced during the training phase.

4.3 Results

We deployed our model on different embedded platforms, namely MAX78000, Raspberry Pi 4, and STM32H7. For the MAX78000, we trained and deployed using the official suite [18] which relies on a modified version of PyTorch dedicated to MAX

boards, while for the Raspberry Pi 4 and the STM32H7 we used TensorFlow [19] for training and TensorFlow Lite [20] for deploying. We remark that the use of standard frameworks for training and deploying streamlines these procedures, whereas the MAX suite, while being comprehensive, has a steeper learning curve and requires more time to set up the experiment. Table 1 reports the accuracy, inference time, power consumption, and energy consumption for the proposed models across the mentioned edge devices. We employed a USB multimeter connected between the power supply and the device to track power variations. Energy is then computed by multiplying power per inference time. Reported values are averages over 100 runs.

Results are also compared with the CNN-based model presented in [16]. In all cases, our model outperforms the state-of-the-art baseline in terms of all the metrics considered. Considering the three platforms under test, the TensorFlow Lite model deployed for Raspberry Pi 4 and STM32H7 has better accuracy, probably due to some differences inherent to the training framework used. However, the MAX78000 outperforms the other MCUs in terms of power and energy consumption and inference time. In particular, the power consumption is ~ 20 times smaller than the STM32H7 and ~ 70 times smaller than the Raspberry Pi 4, which makes this MCU the most suitable choice in scenarios with limited or sporadic power availability such as the miniature mobile robot application. We highlight that the inference time obtained on the MAX78000 is comparable to a Tesla T4 GPU.

Table 1. Performance comparison of the CNN-based model on different embedded platforms.

	MAX78000	Raspberry Pi 4	STM32H7	RP2040 [16]
Accuracy	96.02	98.07	98.07	91.80
Power (mW)	12.54	869.12	223.72	108.35
Energy (μ J)	0.66	1,544	132	3,685
Inference time (μ s)	53	177	590	34,000

5 Conclusions

The MAX78000 MCU has shown significant promise in the TinyML domain. In the presented experiment, despite a slightly lower accuracy, it outperformed other mainstream embedded platforms (i.e., the STM32H7 and the Raspberry Pi 4) in terms of inference time and power and energy consumption. This makes it an excellent choice in power-constrained applications like miniature mobile robot detection. Future works will include experiments in other embedded domains under real-time execution constraints (e.g., [21]).

References

1. Abadade, Y., Temouden, A., Bamoumen, H., Benamar, N., Chtouki, Y., Hafid, A.S.: A comprehensive survey on TinyML. *IEEE Access* **11**, 96892–96922 (2023). <https://doi.org/10.1109/ACCESS.2023.3294111>
2. Dabbous, A., Fresta, M., Bellotti, F., Berta, R.: Neural architecture for tennis shot classification on embedded system. In: Bellotti, F., Grammatikakis, M.D., Mansour, A., Ruo Roch, M., Seepold, R., Solanas, A., Berta, R. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 97–102. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_14
3. Khalife, R., Mrad, R., Dabbous, A., Ibrahim, A.: Real-time implementation of tiny machine learning models for hand motion classification. In: Bellotti, F., Grammatikakis, M.D., Mansour, A., Ruo Roch, M., Seepold, R., Solanas, A., Berta, R. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 487–492. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_70
4. Falaschetti, L., et al.: A low-cost, low-power and real-time image detector for grape leaf esca disease based on a compressed CNN. *IEEE J. Emerg. Select. Topi. Circ. Sys.* **11**, 468–481 (2021). <https://doi.org/10.1109/JETCAS.2021.3098454>
5. Dabbous, A., Fresta, M., Bellotti, F., Berta, R.: Arduino nano-based system for tennis shot classification. In: Ciofi, C., Limiti, E. (eds.) *Proceedings of SIE 2023*, pp. 357–362. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48711-8_43
6. Nardello, M., Caronti, L., Brunelli, D.: Intermittent Intelligent Camera with LEO sensor-to-satellite Connectivity. In: *Proceedings of the 11th International Workshop on Energy Harvesting & Energy-Neutral Sensing Systems*, pp. 79–85. Association for Computing Machinery, New York, NY, USA (2023). <https://doi.org/10.1145/3628353.3628550>
7. Fresta, M., et al.: End-to-end dataset collection system for sport activities. *Electronics* **13**, 1286 (2024). <https://doi.org/10.3390/electronics13071286>
8. Lazzaroni, L., Mazzara, A., Bellotti, F., De Gloria, A., Berta, R.: Employing an IoT framework as a generic serious games analytics engine. In: Marfisi-Schottman, I., Bellotti, F., Hamon, L., Klemke, R. (eds.) *Games and Learning Alliance*, pp. 79–88. Springer International Publishing, Cham (2020). https://doi.org/10.1007/978-3-030-63464-3_8
9. Caronti, L., Akhunov, K., Nardello, M., Yıldırım, K.S., Brunelli, D.: Fine-grained hardware acceleration for efficient Batteryless intermittent inference on the edge. *ACM Trans. Embed. Comput. Syst.* **22**, 82:1–82:19 (2023). <https://doi.org/10.1145/3608475>
10. Berta, R., Bellotti, F., De Gloria, A., Lazzaroni, L.: Assessing versatility of a generic end-to-end platform for IoT ecosystem applications. *Sensors* **22**, 713 (2022). <https://doi.org/10.3390/s22030713>
11. Han, S., Mao, H., Dally, W.J.: Deep Compression: Compressing Deep Neural Networks with Pruning, Trained Quantization and Huffman Coding. <http://arxiv.org/abs/1510.00149> (2016). <https://doi.org/10.48550/arXiv.1510.00149>
12. Sakr, F., et al.: CBin-NN: an inference engine for Binarized neural networks. *Electronics* **13**, 1624 (2024). <https://doi.org/10.3390/electronics13091624>
13. Antonini, M., Pincheira, M., Vecchio, M., Antonelli, F.: An adaptable and unsupervised TinyML anomaly detection system for extreme industrial environments. *Sensors* **23**, 2344 (2023). <https://doi.org/10.3390/s23042344>
14. Clay, M., Grecos, C., Shirvaikar, M., Richey, B.: Benchmarking the MAX78000 artificial intelligence microcontroller for deep learning applications. In: *Real-Time Image Processing and Deep Learning 2022*, pp. 47–52. SPIE (2022). <https://doi.org/10.1117/12.2622390>
15. Moss, A., et al.: Ultra-low power DNN accelerators for IoT: resource characterization of the MAX78000. In: *Proceedings of the 20th ACM Conference on Embedded Networked Sensor*

- Systems, pp. 934–940. Association for Computing Machinery, New York, NY, USA (2023). <https://doi.org/10.1145/3560905.3568300>
- 16. Pleterski, J., Škulj, G., Esnault, C., Puc, J., Vrabič, R., Podržaj, P.: Miniature mobile robot detection using an ultralow-resolution time-of-flight sensor. *IEEE Trans. Instrum. Meas.* **72**, 1–9 (2023). <https://doi.org/10.1109/TIM.2023.3318710>
 - 17. Nagel, M., et al.: A White Paper on Neural Network Quantization, <http://arxiv.org/abs/2106.08295> (2021). <https://doi.org/10.48550/arXiv.2106.08295>
 - 18. Analog Devices AI: <https://github.com/MaximIntegratedAI>. Last accessed 06 May 2024
 - 19. TensorFlow: <https://www.tensorflow.org/>. Last accessed 07 May 2024
 - 20. TensorFlow Lite | ML for Mobile and Edge Devices, <https://www.tensorflow.org/lite>. Last accessed 18 December 2021
 - 21. Fresta, M., et al.: Low-Cost, Edge-Cloud, End-to-End System Architecture for Human Activity Data Collection. In: Bellotti, F., Grammatikakis, M.D., Mansour, A., Ruo Roch, M., Seepold, R., Solanas, A., Berta, R. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 444–449. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_64



Classification of Skiing Techniques on Embedded System

Matteo Fresta^(✉), Francesco Bellotti, Alessio Capello, Marianna Cossu, Luca Forneris, and Riccardo Berta

Department of Electrical, Electronic and Telecommunication Engineering (DITEN), University of Genoa, Via Opera Pia 11a, 16145 Genoa, Italy
matteo.fresta@edu.unige.it

Abstract. Wearable technology has emerged as a key focus in both academic research and industry applications, especially in sports, where data gathering and analysis are crucial for enhancing athletic performance. This study proposes a 1D Convolutional Neural Network (1D-CNN) designed for real-time classification of skiing techniques using the Arduino Nano 33 BLE Sense, an embedded system that is both cost-effective and compact. The goal is to facilitate immediate feedback for athletes, aiding in performance enhancement and injury prevention.

Time-series data from 6-axis accelerometer and gyroscope were collected to represent four skiing techniques: drifting, snowplow-steering, push-off, and tuck. Data was captured at 20 Hz from an amateur skier wearing the Arduino device on the chest.

Model performance was assessed on a test set, reaching a good classification accuracy. Inference time and power consumption were measured considering TensorflowLite models deployed on the Arduino Nano 33 BLE Sense, both with and without 8-bit integer quantization for weights, showing promising results.

This approach underscores the potential of using compact neural networks on embedded systems for sports analytics, promising further advancements in real-time, field-based athlete monitoring and feedback systems.

Keywords: Skiing techniques classification · 1D-CNN · Time series · Inertial Measurement Unit (IMU) · Embedded device · Arduino Nano 33 BLE Sense

1 Introduction

Advancements in sensor technology and machine learning have led to significant innovations in sports analytics, particularly in sports like football [1], tennis [2], and also skiing [3], where technique refinement is critical for performance enhancement and injury prevention. Athletes are provided with real-time performance feedback tracked via wearable sensors. This research focus on the classification of skiing techniques, which are specific movements and postures used by skiers to navigate slopes efficiently and safely. While existing literature extensively covers data collection using various sensor placements, including on skis and different body parts, these methods often involve significant costs and complexity [4, 5].

Our study differs by utilizing a cost-effective and compact solution based on an Arduino Nano 33 BLE Sense, which has been validated in other studies [6]. Positioned on the chest, this device gathers comprehensive inertial measurements. This placement provides a dataset capturing accelerometer, and gyroscope data across three axes, offering a different perspective compared to other methods. This research also aims to address machine learning classification directly on the device for advanced real-time data analysis, bypassing the need for cloud processing, which is prevalent in current approaches.

2 Related Works

Numerous prior studies have focused on classifying skiing techniques using a range of sensors, following the initial experiments of Marshland et al. with wearable sensors [7]. Stööggl et al. utilized accelerometer data from a mobile phone secured to a skier's chest belt and employed a Markov chain model for stroke classification [8]. Similarly, Rindal et al. integrated wearable inertial measurement units (IMUs) on the skiers' arms and chest, along with gyroscopes on the arms, to analyze ski strokes [9]. Sakurai et al. extended this approach by attaching multiple IMUs to both the skis and poles, using this data to develop a decision tree classifier for both classical and skating techniques [10]. More recently, Jang et al. carried out a study that utilized a total of 17 inertial motion trackers to distinguish between classical and skating techniques using a deep machine learning framework that combines CNN and LSTM layers [11].

In all the works mentioned, data are recorded and processed either in the cloud or on a desktop computer. On the other hand, the literature has much less examples using embedded device capable of handling AI models to provide real-time feedback to the athlete.

Considering this context, the proposed work aims to present a novel application of an embedded system for real-time classification of skiing techniques. By utilizing low-cost, low-power hardware combined with efficient machine learning algorithms, this study seeks to provide athletes with immediate feedback while maintaining high accuracy and low latency in technique classification.

3 Experiment Setup

3.1 Dataset

For this study a dataset composed of 6-axis time-series data (x, y, and z from both the accelerometer and gyroscope) has been collected representing four specific skiing techniques: drifting, snowplow-steering, push off, and tuck. To focus specifically on the performance of a single athlete and assess the validity of the data collection method [12], an amateur skier performed multiple ski slopes equipped with a custom device featuring an Arduino Nano 33 BLE Sense with a custom battery board [13]. The IMU (LSM9DS1) sensor on this device captured the time-series data for the duration of the descent on the ski slope. The data collected by the Arduino was transmitted via BLE to a mobile phone and uploaded as CSV files to the Measurify cloud platform [14, 15].

Measurify is a cloud-based, measurement-oriented platform designed to manage data from IoT ecosystems, and its versatility was assessed in different studies [16, 17]. To collect the dataset, the board was placed on the athlete's chest to gather IMU data on the movements during the descent. The data were collected towards two ski resorts with a total of 13 different ski slopes. In total, 39 slopes were gathered, with 85% used as the training set and 15% as validation set. Additionally, for testing purposes, 4 longer slopes were collected containing all the techniques in sequence.

The dataset was collected with 20 Hz sampling frequency and for the classification we considered windows of 40, 60, and 80 data points respectively.

3.2 1D Classifier Network Architecture

To identify optimal hyperparameter values of the 1D-CNN (particularly: number of convolutional layers, number of filters, number of neurons for the first dense, and learning rate), we employed Bayesian optimization (BO) using the Keras tuner library to assess 20 combinations of hyperparameters over 40 epochs. Through this method, we reach good accuracy with 80 data points, and we obtained as optimal configuration a network with 3 convolutional layers, 32 filters, 32 neurons, and a learning rate of 10e-3.

Figure 1 shows the resulting structure of 1D Convolutional Neural Network (1D-CNN) designed for classification. This network is composed of three 1D convolutional layers, interlined by a max pooling layer. This sequence is followed by two dense layers and a softmax output layer with four neurons, corresponding to the four classes.

The primary function of the convolutional layers is to extract features relevant for classification, whereas the max pooling layers, which have non-overlapping receptive fields, are designed to reduce the dimensionality of the data.

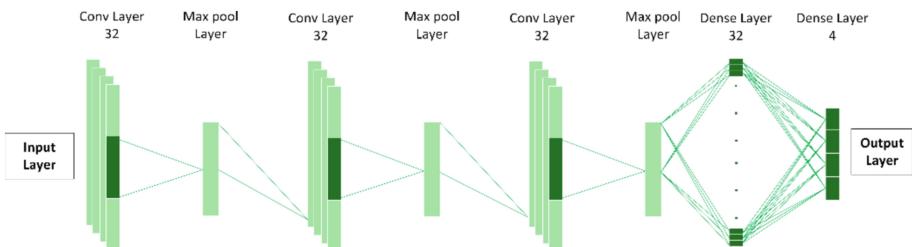


Fig. 1. 1D convolutional neural network.

4 Experimental Results

To evaluate the model's performance, we used the test set that includes more than 10 samples for each of the four techniques classified.

Figure 2 illustrates two key comparisons: on the left, it shows the comparison between the ground truth and the model's predictions for a segment of test sequence number 1; on the right, it presents the normalized confusion matrix of the best model.

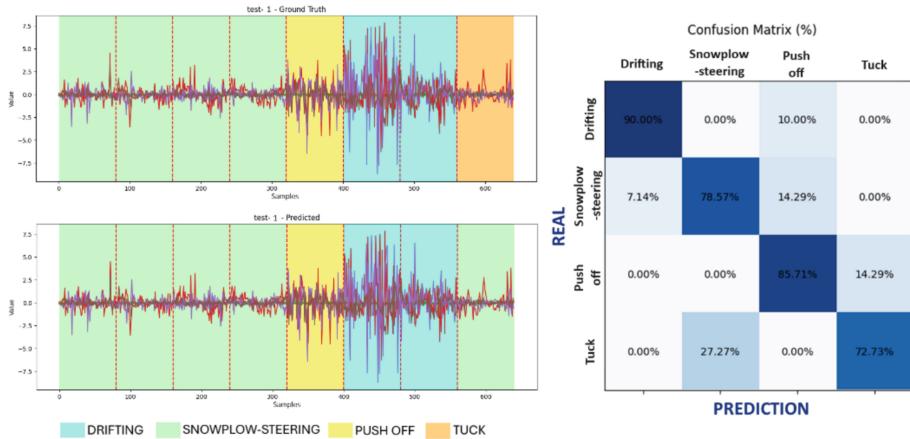


Fig. 2. (left) Comparison of ground truth and prediction, (right) Normalized confusion matrix of the 1D-CNN model.

The confusion matrix reveals that the drifting technique has the highest accuracy, while the tuck technique has the lowest.

Table 1 shows the performance of the trained models over the test set and the size of the models. For the deployability, the model was converted to TFLite with a decreasing in model size without a loss of accuracy. Additionally, to further reduce model size we also used the TFLite quantization of weights to 8-bit integers, but this led to a loss in accuracy as shown in Table 1.

Table 1. 1D-CNN model performance and size.

Model	Accuracy(%)	Precision(%)	Recall(%)	F1-score(%)	Size(KB)
1D-CNN(Baseline)	85.58	87.86	85.58	86.71	232.46
TFLite	85.58	87.86	85.58	86.71	66.50
Quantized	80.92	85.63	80.92	83.21	26.04

For the performance studies, the two models were deployed on the Arduino Nano 33 BLE Sense.

Table 2 demonstrates good performance in terms of inference time, power and energy consumption. In particular, power consumption was measured by observing the power variations during inference using a JT-UM120 USB Multimeter.

Table 2. Model performance on Arduino Nano 33 BLE Sense.

Model	Inference time (ms)	Power consumption (mW)	Energy consumption (mJ)
TFLite	78.130	15.200	1.188
Quantized	26.370	14.100	0.371

5 Conclusion

This paper presents the development of a 1D-CNN on an Arduino microcontroller to distinguish four different types of skiing techniques with high accuracy. This work has good performance, both in term of accuracy and power consumption, hence the concepts shown in the paper are applicable to real-world use cases. We will continue using basic computational techniques supported by low-power microelectronic devices to design compact and efficient end-to-end systems for analyzing sports activity signals in the field.

Future work may include expanding the dataset collection to involve more participants and exploring binary models to reduce memory usage and power consumption [18].

References

1. Yu, C., Huang, T.-Y., Ma, H.-P.: Motion analysis of football kick based on an IMU sensor. *Sensors* **22**, 6244 (2022). <https://doi.org/10.3390/s22166244>
2. Dabbous, A., Fresta, M., Bellotti, F., Berta, R.: Neural architecture for tennis shot classification on embedded system. In: Bellotti, F., et al. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 97–102. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_14
3. Azadi, B., Haslgrübler, M., Anzengruber-Tanase, B., Grünberger, S., Ferscha, A.: Alpine skiing activity recognition using smartphone's IMUs. *Sensors* **22**, 5922 (2022). <https://doi.org/10.3390/s22155922>
4. Neuwirth, C., Snyder, C., Kremser, W., Brunauer, R., Holzer, H., Stögg, T.: Classification of alpine skiing styles using GNSS and inertial measurement units. *Sensors* **20**, 4232 (2020). <https://doi.org/10.3390/s20154232>
5. Gløersen, Ø., Gilgien, M.: Classification of cross-country Ski skating sub-technique can be automated using carrier-phase differential GNSS measurements of the head's position. *Sensors* **21**, 2705 (2021). <https://doi.org/10.3390/s21082705>
6. Dabbous, A., Fresta, M., Bellotti, F., Berta, R.: Arduino nano-based system for tennis shot classification. In: Ciofi, C. and Limiti, E. (eds.) *Proceedings of SIE 2023*, pp. 357–362. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48711-8_43
7. Marsland, F., Lyons, K., Anson, J., Waddington, G., Macintosh, C., Chapman, D.: Identification of cross-country skiing movement patterns using micro. *Sensors* **12**, 5047–5066 (2012). <https://doi.org/10.3390/s120405047>
8. Stögg, T., et al.: Automatic classification of the sub-techniques (Gears) used in cross-country ski skating employing a mobile phone. *Sensors* **14**, 20589–20601 (2014). <https://doi.org/10.3390/s141120589>

9. Rindal, O.M.H., Seeberg, T.M., Tjønnås, J., Haugnes, P., Sandbakk, Ø.: Automatic classification of sub-techniques in classical cross-country skiing using a machine learning algorithm on micro-sensor data. *Sensors* **18**, 75 (2018). <https://doi.org/10.3390/s18010075>
10. Sakurai, Y., Fujita, Z., Ishige, Y.: Automatic identification of Subtechniques in skating-style roller skiing using inertial sensors. *Sensors* **16**, 473 (2016). <https://doi.org/10.3390/s16040473>
11. Jang, J., et al.: A unified deep-learning model for classifying the cross-country skiing techniques using wearable gyroscope sensors. *Sensors* **18**, 3819 (2018). <https://doi.org/10.3390/s18113819>
12. Fresta, M., et al.: Low-cost, edge-cloud, end-to-end system architecture for human activity data collection. In: Bellotti, F., et al. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 444–449. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_64
13. Fresta, M., et al.: End-to-end dataset collection system for sport activities. *Electronics (Switzerland)* **13** (2024). <https://doi.org/10.3390/electronics13071286>
14. Fresta, M., et al.: Efficient uploading of .Csv datasets into a non-relational database management system. In: Berta, R., De Gloria, A. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 9–15. Springer Nature Switzerland, Cham (2023). https://doi.org/10.1007/978-3-031-30333-3_2
15. Fresta, M., et al.: Supporting a .csv-based Workflow in MongoDB for Data Analysts. In: 2023 IEEE 32nd International Symposium on Industrial Electronics (ISIE), pp. 1–4 (2023). <https://doi.org/10.1109/ISIE51358.2023.10228044>
16. Berta, R., Bellotti, F., De Gloria, A., Lazzaroni, L.: Assessing versatility of a generic end-to-end platform for iot ecosystem applications. *Sensors* **22** (2022). <https://doi.org/10.3390/s22030713>
17. Capello, A., et al.: Exploiting big data for experiment reporting: the hi-drive collaborative research project case. *Sensors* **23**, 7866 (2023). <https://doi.org/10.3390/s23187866>
18. Sakr, F., et al.: CBin-NN: an inference engine for Binarized neural networks. *Electronics* **13**, 1624 (2024). <https://doi.org/10.3390/electronics13091624>



Enhancing μNAS for 1D CNNs on Microcontrollers

Alessio Capello^(✉), Riccardo Berta, Hadi Ballout, Matteo Fresta,
Vafali Soltanmuradov, and Francesco Bellotti

Department of Electrical, Electronic and Telecommunication Engineering (DITEN),
University of Genoa, Via Opera Pia 11a, 16145 Genoa, Italy
alessio.capello@edu.unige.it

Abstract. Deep Learning (DL) has proved effective in a variety of application domains. However, the computational and memory demand posed by deep neural models limits the spread of DL on resource-constrained devices such as microcontrollers. An opportunity to tailor DL models to specific hardware constraints is given by Neural Architecture Search (NAS), which automatically traverses a large search space, seeking for optimal architectures both in terms of hardware and performance, based on user specifications. State of the art open-source NAS tools for microcontrollers only support 2D Convolutional Neural Network (CNN) and Multi Layer Perceptron (MLP), but do not consider 1D convolution, which is key for time series analysis and signal processing. This study focuses on enhancing the state-of-the-art μNAS framework, by adding support for 1D CNN. Preliminary tests on a dummy dataset consisting of simple gaussian-distributed waveforms, demonstrate the system ability to find appropriate architectures to satisfy the specified constraints.

Keywords: Neural Architecture Search (NAS) · Microcontrollers · Optimization · 1D Convolutional Neural Network

1 Introduction

Deep Learning (DL) model effectiveness has led to a wide diffusion of neural architectures across a variety of tasks (e.g., automotive [1], medical [2], renewable energies [3], etc.). Convolutional Neural Networks (CNNs) are very effective in processing signals like images and time-series, and Recurrent Neural Networks (RNNs) provide models with short-term memory capabilities. These architectures are computationally and power expensive, which limits their use on microcontroller units (MCUs), that are typically characterized by significant constraints in terms of available resources [4]. This spurred a search for techniques able to adapt such DL models so to allow their execution on MCUs, particularly by reducing memory footprint and latency. This led to the definition of neural network (NN) model optimization techniques, such as pruning [5], quantization [6], and binarization [7]. A issue with this approach is that developers must manually identify the optimal models with an iterative approach, as shown in Fig. 1, which significantly increases their workload and the time to obtain the final model.

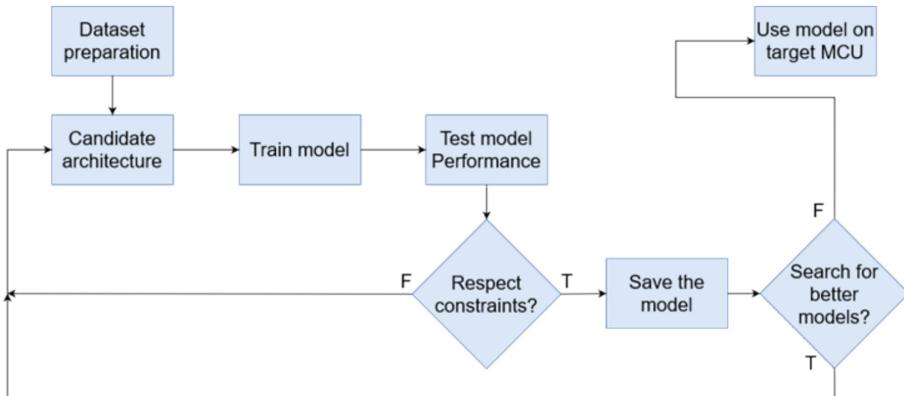


Fig. 1. Iterative workflow to manually find the best model respecting limited-resource constraints.

To overcome this issue, Neural Architecture Search (NAS) algorithms have been developed, which automatically iterate over a large search space to find the architectures (and hence the trained models) that satisfy the given constraints [8], such as memory footprint and latency. Figure 2 illustrates how the use of a NAS tool significantly simplifies the workflow of developers.



Fig. 2. NAS-enabled workflow.

Open-source NAS tools typically target standard benchmark 2D image datasets such as MNIST and CIFAR-10. Consequently, these solutions lack the support for 1D CNNs, focusing only on 2D CNNs and Multi Layer Perceptron (MLP).

The aim of this work is to enhance a state of the art MCU-oriented NAS tool so to make it able to manage 1D CNNs as well.

2 Related Works

The interest in NAS tools is shown by many state-of-the-art solutions available in literature, often targeting a particular domain or use case.

Lu et al. [9] provide a general multiobjective formulation of NAS and analysis from the optimization point of view. They also present an end-to-end pipeline, namely EvoXBench, to streamline the generation of benchmark test problems for evolutionary multiobjective optimization algorithms to run efficiently without requiring GPUs nor sophisticated software such as Pytorch/TensorFlow. Xue et al. [10], present a multi-objective evolutionary algorithm with a probability stack for NAS, which considers the two objectives of precision and time consumption. The authors report promising results

on 2D image benchmark datasets. Tan et al. [11], propose a factorized hierarchical search space method to encourage layer diversification throughout the network architecture, with a focus on mobile phones. Garavagno et al. [8] propose a NAS tool to develop and deploy 2D CNN models on the STM32 family MCUs. Liberis et al. [12], propose a tool, namely µNAS, to identify platform-independent NN architectures. This tool is presented in detail in the next section, as it is the foundation of our work.

MCUs serving as edge devices are often equipped with low-cost Inertial Measuring Unit (IMU) sensors, such as accelerometers and gyroscopes [13]. The onboard processing of these signals is relevant for applications like Gesture Recognition [14] and Sport Activity Recognition [15]. The optimal NN architecture for signal processing applications is 1D CNNs.

From the mentioned works, it emerges the interest in NAS tools to support Machine Learning developers with tools specifically tailored for a field application or domain of interest. On the other hand, there is a lack in the open-source community of NAS tools designed to support 1D CNN architectures, which motivated our work.

3 Methodology

Our work relies on the open-source tool µNAS [12], a robust NAS library developed in Python explicitly designed to identify architectures optimized for deployment on MCUs, considering factors such as Peak Memory Usage (PMU), model size, and latency. PMU, the maximum memory occupied by stored tensors, is assessed by evaluating the memory footprint of individual operators. Model size refers to the total number of bytes stored in the MCU's flash memory. To minimize model size, 32-bit floating point weights are usually quantized into 8-bit integers, which typically implies only a small decrease in accuracy [16]. Latency is essentially due to the number of Multiply Accumulate (MAC) operations [12], thus its estimation is approximated using the number of MAC operations as a proxy value.

µNAS generates and traverses the search space, tailored to the specified NN architecture type. Initially, random architectures are generated, and subsequent modifications are applied (i.e., layer addition or removal, number of unit adjustment, etc.). The search space is then explored using either Aging Evolution or Bayesian Optimization search strategies, aimed at identifying architectures that satisfy the specified requirements. Models found and trained with this tool are exported as TensorFlow Lite models, a common format in the DL community, directly supported by numerous MCUs.

While powerful, the current version of the tool is limited to MLP and 2D CNN architectures and lacks the support for other layers. The enhancement we propose for the µNAS tool involves the definition of a new search space dedicated to 1D CNNs, managed by modules that handle the generation of random architectures and their modifications, while also computing the PMU, model size, and MACs. This implementation seamlessly integrates with the existing µNAS library, leveraging identical optimization algorithms and multi-threading optimizations. Furthermore, consistent employment of the same handlers and configuration schema allows µNAS library users to seamlessly leverage the proposed extension.

4 Results

We test the enhanced μ NAS in a classification task with a custom-defined dummy dataset comprising of two classes of 2500 sine waves each. This dataset consists of signals resembling those collected by real-world sensors (e.g., gyroscopes, accelerometers) but characterized solely by frequency. The first class contains waves normally distributed around 250 Hz with a standard deviation of 130 Hz, while the second class has waves distributed around 650 Hz with the same standard deviation. All sine waves are sampled at a uniform frequency of 2 kHz. Frequency distributions are shown in Fig. 3.

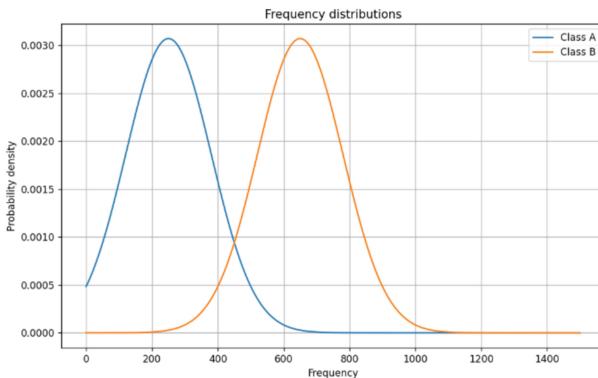


Fig. 3. Frequency distribution of two class dummy dataset.

Table 1 presents the results obtained by the enhanced μ NAS under the specified constraints in a single traversal of the search space using the Aging Evolution algorithm. The “Mean” row in the table represents the average values calculated across the 18 models identified by μ NAS, that met the constraints.

Table 1. Architectures found by μ NAS.

	Error rate	PMU (B)	Model size (B)	MACs
Constraints	0.2000	20 000	50 000	30 000
Mean	0.0499	353	3 603	5 170
Lowest error rate	0.0000	22	12 153	12 130
Lowest PMU	0.0140	20	10 131	10 110
Lowest size	0.0920	749	885	2 859
Lowest MACs	0.1580	177	1 691	2 682

This table demonstrates how this tool effectively identifies architectures not only within the given constraints, but also attempts to minimize them, allowing the user to

prioritize among different criteria. Table 1, in fact, highlights possible trade-offs between a low error rate, model size, and MACs. The model with the lowest error rate has a higher model size and MAC count compared to the mean value. Conversely, the model with the lowest size and the one with the lowest MAC count have a higher error rate. In this case, PMU does not appear to be closely correlated with the other quantities, warranting further investigation with real datasets.

5 Conclusion

Deploying NN models on MCUs is a complex task, which often involves a significant workload. To mitigate this complexity, developers can exploit NAS tools to identify NN models meeting the constraints set by the user keeping into account the characteristics of the target MCU and application. As state of the art open-source NAS tools do not support 1D CNN models, we have extended the well known µNAS tool to bridge this gap.

We tested the extended µNAS with a dummy dataset to assess its capability to find models within given constraints. The results are promising, as the extended tool identified various architectures, characterized by different performance metrics.

Future work should validate the extended tool's performance with real-work benchmarks, enabling comparisons with baseline models. Another research direction concerns expanding the tool to include other specific architectures, such as 3D-CNNs, MiniRocket, or hypernetworks designed to generate explainable networks.

References

1. Capello, A., et al.: Investigating high-level decision making for automated driving. In: Berta, R., De Gloria, A. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 307–311. Springer Nature Switzerland, Cham (2023). https://doi.org/10.1007/978-3-031-30333-3_41
2. Li, M., Jiang, Y., Zhang, Y., Zhu, H.: Medical image analysis using deep learning algorithms. *Front. Public Health* **11**, 1273253 (2023). <https://doi.org/10.3389/fpubh.2023.1273253>
3. Benti, N.E., Chaka, M.D., Semie, A.G.: Forecasting renewable energy generation with machine learning and deep learning: current advances and future prospects. *Sustainability* **15**, 7087 (2023). <https://doi.org/10.3390/su15097087>
4. Shuvo, M., Islam, S.K., Cheng, J., Morshed, B.I.: Efficient acceleration of deep learning inference on resource-constrained edge devices: a review. *Proc. IEEE* **111**, 42–91 (2023). <https://doi.org/10.1109/JPROC.2022.3226481>
5. Widmann, T., Merkle, F., Nocker, M., Schöttle, P.: Pruning for power: optimizing energy efficiency in IoT with neural network pruning. In: Iliadis, L., Maglogiannis, I., Alonso, S., Jayne, C., Pimenidis, E. (eds.) *Engineering Applications of Neural Networks*, pp. 251–263. Springer Nature Switzerland, Cham (2023). https://doi.org/10.1007/978-3-031-34204-2_22
6. Zhuso, S., et al.: An Empirical Study of Low Precision Quantization for TinyML (2022). <https://doi.org/10.48550/ARXIV.2203.05492>
7. Sakr, F., et al.: CBin-NN: an inference engine for Binarized neural networks. *Electronics* **13**, 1624 (2024). <https://doi.org/10.3390/electronics13091624>

8. Garavagno, A.M., Ragusa, E., Frisoli, A., Gastaldo, P.: An affordable hardware-aware neural architecture search for deploying convolutional neural networks on ultra-low-power computing platforms. *IEEE Sens. Lett.* **8**, 1–4 (2024). <https://doi.org/10.1109/LSENS.2024.3387056>
9. Lu, Z., Cheng, R., Jin, Y., Tan, K.C., Deb, K.: Neural architecture search as multiobjective optimization benchmarks: problem formulation and performance assessment. *IEEE Trans. Evol. Computat.* **28**, 323–337 (2024). <https://doi.org/10.1109/TEVC.2022.3233364>
10. Xue, Y., Chen, C., Stowik, A.: Neural architecture search based on a multi-objective evolutionary algorithm with probability stack. *IEEE Trans. Evol. Computat.* **27**, 778–786 (2023). <https://doi.org/10.1109/TEVC.2023.3252612>
11. Tan, M., et al.: MnasNet: Platform-Aware Neural Architecture Search for Mobile (2018). <https://doi.org/10.48550/ARXIV.1807.11626>
12. Liberis, E., Dudziak, Ł., Lane, N.D.: μNAS: Constrained Neural Architecture Search for Microcontrollers (2020). <https://doi.org/10.48550/ARXIV.2010.14246>
13. Fresta, M., et al.: Low-cost, edge-cloud, end-to-end system architecture for human activity data collection. In: Bellotti, F., Grammatikakis, M.D., Mansour, A., Ruo Roch, M., Seepold, R., Solanas, A., Berta, R. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 444–449. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_64
14. Khalife, R., Mrad, R., Dabbous, A., Ibrahim, A.: Real-time implementation of tiny machine learning models for hand motion classification. In: Bellotti, F., Grammatikakis, M.D., Mansour, A., Ruo Roch, M., Seepold, R., Solanas, A., and Berta, R. (eds.) *Applications in Electronics Pervading Industry, Environment and Society*, pp. 487–492. Springer Nature Switzerland, Cham (2024). https://doi.org/10.1007/978-3-031-48121-5_70
15. Dabbous, A., Fresta, M., Bellotti, F., Berta, R.: Arduino nano-based system for tennis shot classification. *Lecture Notes in Electrical Engineering*. 1113 LNEE, 357–362 (2024). https://doi.org/10.1007/978-3-031-48711-8_43
16. Lin, J., et al.: MCUNet: Tiny Deep Learning on IoT Devices (2020). <https://doi.org/10.48550/ARXIV.2007.10319>



Digital Low-Complexity Entropy Estimator Based on the Direct Assessment of Average Shannon Entropy

Tommaso Addabbo^(✉), Ada Fort, Filippo Spinelli, and Valerio Vignoli

Department of Information Engineering and Mathematics, University of Siena,
Via Roma 56, Siena, Italy

{tommaso.addabbo,ada.fort,valerio.vignoli}@unisi.it,
filippo.spinelli@student.unisi.it

Abstract. We present a methodology to design a new class of low-complexity entropy estimators, aimed at designing tunable True Random Number Generators (TRNGs). Our design approach is detailed for the typical scenario of non-IID ergodic sources, analyzing how source memory impacts estimation precision. Additionally, we have examined the refined hardware implementation of this estimator, specifically for a Xilinx Artix 7 FPGA.

Keywords: True Random Number Generators · Entropy Estimators

1 Introduction

We discuss the design of a low-complexity entropy estimator suitable for the design of tunable True Random Number Generators (TRNGs) in which the entropy sources are typically sensitive to PVT variations, and their tunability depends on parametric configurations allowing for the dynamical maximization of the entropy [1–6]. Entropy tuning is obtained by means of feedback based on entropy estimators [7–14]. In this work we discuss a method to design an entropy estimator that can be used to compare couples of random sources. The goal is to select the one with the highest entropy in a set.

2 Entropy Estimation

The Average Shannon Entropy (ASE) for an ergodic binary random source S is defined as

$$\mathcal{E}(S) = \lim_{n \rightarrow \infty} \mathcal{E}_n(S) = \lim_{n \rightarrow \infty} -\frac{1}{n} \sum_{\omega \in \Omega_n} P(\omega) \log_2(P(\omega)), \quad [\text{bit/sym.}], \quad (1)$$

where Ω_n is the set of all binary n -bit words, and $P(\omega)$ is the generation probability of the word $\omega \in \Omega_n$. Equation (1) holds for any ergodic source, regardless of its

memory. The computation of generation probabilities, $P(\omega)$, involves a counting process that tallies the frequencies of the 2^n words throughout an experimental observation. As a result, the practical implementation of (1) is only achievable by truncating the sequence to a suitable n value and monitoring the source for a limited duration. We denote with $\mathcal{E}_n^{(k)}(S)$ such a truncated entropy estimator, where the limit $\lim_{n,k \rightarrow \infty} \mathcal{E}_n^{(k)}(S) = \mathcal{E}(S)$ converges in probability.

3 Optimized Hardware Design

Let us focus on the low-complexity digital design of the expression

$$\mathcal{E}_n^{(k)}(S) = \sum_{\omega \in \Omega_n} \frac{f(P(\omega))}{n} = \sum_{\omega \in \Omega_n} \frac{-P(\omega) \log_2(P(\omega))}{n}. \quad (2)$$

The calculation of (2) involves one accumulator summing the repeated computation of the function $f : [0, 1] \rightarrow [0, \frac{1}{e \ln 2}]$, $f(x) = -x \log_2 x$. If n is a power of two, the ratio in (2) can be obtained with an hardware shift of the accumulator. Accordingly, the most expensive operation, in terms of computational resources, is the computation of the function f , that implies the multiplication of $-x$ by $\log_2(x)$. In literature, well known computation methods have been proposed to calculate the logarithm. However, since the considered application we need the direct calculation of f , specific optimizations can be investigated.

Table 1. HW Resource Consumption to Compute $f(x) = -x \log_2 x$

	LUTs	FFs	DSP48E1s	Latency
	#	#	#	(Clk Cycles)
Original	1034	1182	9	43
Cubic Approx.	328	565	10	23
Quadratic Approx.	187	337	6	19
Piecewise Linear Approx.	262	288	4	13

To establish a first reference implementation benchmark we implemented the function f resorting to High Level Synthesis (HLS). The function f has been described in C, encoding the input x and the function result as a IEEE 754 half-precision binary floating-point number, that provides a total significand precision of 11 bits. The solution has been carefully designed to minimize the hardware consumption, using Xilinx Vitis HLS optimized libraries, targeting a Xilinx Artix 7 FPGA running at 100 MHz clock frequency. Obtained implementation results are reported in the first row of Table 1. It is worth noting that the choice to represent data as half-precision floating-point numbers has been made

targeting the most efficient and optimized implementation achievable with standard computation techniques. The circuit synthesis has been carefully verified to ensure that no further optimizations could be made with this architecture.

As an alternative approach, we investigated the direct calculation of the function f , exploring cubic, quadratic and piecewise linear approximations.

3.1 Cubic Approximation

The function f can be approximated by a cubic polynomial of the form $\tilde{f}(x) = ax^3 + bx^2 + cx + d$. The parameters a, b, c, d can be estimated adopting any fitting strategy (e.g., a nonlinear least square method). In principle, the calculation of the cubic expression requires five linear multiply-and-add (MA) blocks, that can be implemented by properly combining DSP48E1 elements available in Xilinx FPGAs, depending on the numerical representation of x , as shown in Fig. 1. As reported in Table 1 the required amount of hardware resources is significantly reduced. However, the obtained approximation error $\delta(x) = \tilde{f}(x) - f(x)$ can be relevant for values of $x \rightarrow 1$, as reported in Fig. 2.

3.2 Quadratic Approximation

The function f can be approximated by a quadratic polynomial of the form $\tilde{f}(x) = bx^2 + cx + d$. Also in this case the constant parameters b, c, d can be estimated adopting a nonlinear least square fitting strategy. In principle, the calculation of the quadratic expression requires three MA blocks, as shown in Fig. 1. As reported in Table 1 the required amount of hardware resources is even more reduced and the obtained approximation error $\delta(x)$ is worsened in most part of the domain, as reported in Fig. 2.

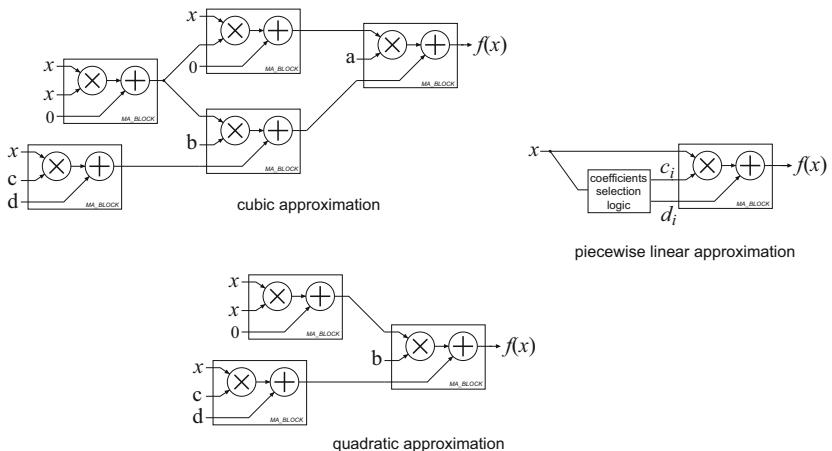


Fig. 1. Digital architectures to calculate the approximations of the function $f(x)$.

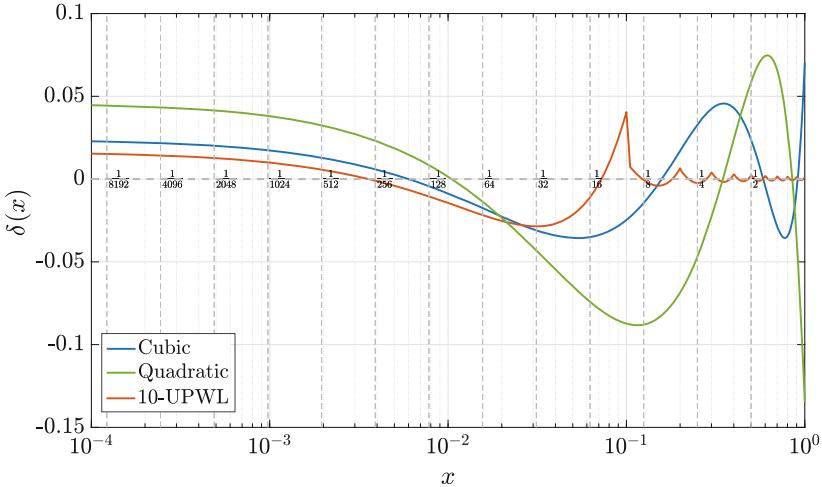


Fig. 2. Approximation errors $\delta(x) = \tilde{f}(x) - f(x)$ for the different approximation strategies.

3.3 Piecewise Linear Approximation

In this case, we considered a finite uniform partition $\Lambda = \{I_i \subset [0, 1] : \cup_i I_i = [0, 1], i \neq j \Rightarrow I_i \cap I_j = \emptyset\}$ of the interval $[0, 1]$ and approximated f as

$$x \in I_i \Rightarrow \tilde{f}(x) = c_i x + d_i \approx f(x). \quad (3)$$

In principle, the implementation of this solution requires just one MA block, but a coefficient selection logic is necessary to choose the values of the coefficients c_i and d_i in (3), as shown in Fig. 1. The complexity of this latter block depends on the number of partitions. The related approximation error $\delta(x)$ for a solution using ten intervals is reported in Fig. 2. As it can be seen, in this case the approximation error is lower than the cubic approximation in most part of the domain. The required amount of hardware resources is significantly reduced with respect to the cubic or quadratic polynomial approximations.

4 Experimental Results

We have compared the results obtained implementing the estimator $\mathcal{E}_8^{9765}(S)$ using the original function $f(x) = -x \log_2(x)$ and $\tilde{f}(x)$ obtained using a 10 intervals piecewise linear approximation. The experiment considered 1000 Markovian sources with entropy greater than 0.8 bit/sym. As shown in Fig. 3 when the entropy of the source tends to 1 bit/sym. The error of the estimator is significantly reduced (lower than 2% relative error for entropy greater than 0.94 bit/sym.). This is because for high entropy levels most 8-bit symbols have a generation probability $P(\omega)$ close to 1/256, that is a value of x around which

the approximation error is almost zero. This result can be generalized for any n , aiming at optimizing the implementation of the estimator $\mathcal{E}_n^{(k)}$, designing the partition such to make the approximation $\delta(x)$ close to zero for $x \approx \frac{1}{2^n}$. As a consequence, the proposed approximation provides results with high accuracy for high levels of entropy. This makes the estimator suitable for the design of best-source selectors embedded in the feedback controller of a tunable TRNG to be more accurate during fine-tuning phases, aiming at the maximization of the source entropy.

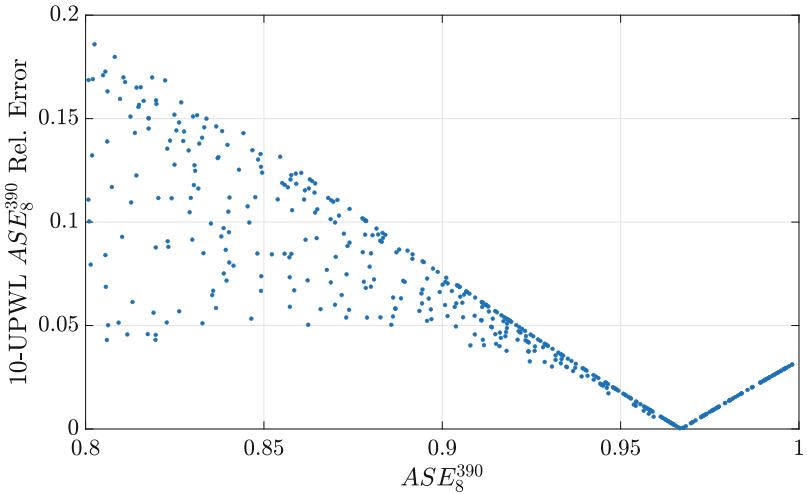


Fig. 3. Experimental results comparing.

5 Conclusion

We have presented a methodology to design a novel class of low-complexity entropy estimators, suitable for the design of tunable True Random Number Generators (TRNGs). The analysis considered different kinds of approximations, proposing a technique to design an approximating piece-wise linear function that can be implemented in a FPGA with low-complexity architectures, guaranteeing adjustable estimation errors that are reduced for increasing entropy levels, allowing for the fine-tuning of cryptographic TRNG. The optimized hardware implementation of the estimator has been investigated targeting a Xilinx Artix 7 FPGA.

References

1. Wang, X., et al.: High-throughput portable true random number generator based on jitter-latch structure. *IEEE Trans. Circuits Syst. I Regul. Pap.* **68**(2), 741–750 (2021)

2. Luo, Y., Wang, W., Best, S., Wang, Y., Xu, X.: A high-performance and secure TRNG based on chaotic cellular automata topology. *IEEE Trans. Circuits Syst. I Regul. Pap.* **67**(12), 4970–4983 (2020)
3. Zhao, Q., Zheng, W., Zhao, X., Cao, Y., Zhang, F., Law, M.-K.: A 108 F2/bit fully reconfigurable RRAM PUF based on truly random dynamic entropy of jitter noise. *IEEE Trans. Circ. Syst. I Regul. Pap.* **67**(11), 3866–3879 (2020)
4. Wieczorek, P.Z., Golofit, K.: True random number generator based on flip-flop resolve time instability boosted by random chaotic source. *IEEE Trans. Circ. Syst. I: Regul. Pap.* **65**(4), 1279–1292 (2018)
5. Liu, Y., Cheung, R.C.C., Wong, H.: A bias-bounded digital true random number generator architecture. *IEEE Trans. Circ. Syst. I Regul. Pap.* **64**(1), 133–144 (2017)
6. Wieczorek, P.Z.: Lightweight trng based on multiphase timing of bistables. *IEEE Trans. Circ. Syst. I Regul. Pap.* **63**(7), 1043–1054 (2016)
7. Addabbo, T., Fort, A., Moretti, R., Mugnaini, M., Papini, D., Vignoli, V.: A stochastic algorithm to design min-entropy tuning controllers for true random number generators. *IEEE Trans. Circ. Syst. I Regul. Pap.* **69**(5), 2084–2094 (2022)
8. Johnson, A.P., Chakraborty, R.S., Mukhopadyay, D.: An improved DCM-based tunable true random number generator for Xilinx FPGA. *IEEE Trans. Circ. Syst. II Express Briefs* **64**(4), 452–456 (2016)
9. Mathew, S.K., et al.: 2.4 Gbps, 7 mw all-digital PVT-variation tolerant true random number generator for 45 nm CMOS high-performance microprocessors. *IEEE J. Solid-State Circ.* **47**(11), 2807–2821 (2012)
10. Xu, X., et al.: An all-digital and jitter-quantizing true random number generator in SRAM-based FPGAs. In: IEEE 27th Asian Test Symposium (ATS 2018), pp. 59–62. IEEE (2018)
11. Rahman, M.T., Xiao, K., Forte, D., Zhang, X., Shi, J., Tehranipoor, M.: TI-TRNG: technology independent true random number generator. In: 51st ACM/EDAC/IEEE Design Automation Conference (DAC 2014), pp. 1–6. IEEE (2014)
12. Suresh, V., Burleson, W.: Entropy and energy bounds for metastability based TRNG with lightweight post-processing. *IEEE Trans. Circ. Syst. I Regul. Pap.* **62**(7), 1785–1793 (2015)
13. Addabbo, T., Fort, A., Mugnaini, M., Petra, N., Takaloo, H., Vignoli, V.: Self-tunable chaotic true random bit generator in current-mode CMOS circuit with nonlinear distortion analysis. *Int. J. Circ. Theory Appl.* **47**(12), 1877–1892 (2019)
14. Addabbo, T., Fort, A., Moretti, R., Spinelli, F., Vignoli, V.: Complex dynamics in digital nonlinear oscillators: experimental analysis and verification. *Electronics* **12**(11), 2459 (2023)

Author Index

A

- Abbass, Yahya 238, 456
Addabbo, Tommaso 487
Aiello, Orazio 35, 41
Ali, Haydar Al Haj 456, 462
Alimenti, Federico 142
Altana, Antonio 244
Amadori, Mattia 3
Antolini, Alessio 413
Antoniou, M. 369

B

- Baccarani, Giorgio 61
Ballout, Hadi 481
Barbaro, Massimo 448
Barile, Gianluca 163
Barsotti, Agata 94
Bartoli, Pietro 441
Basso, Giovanni 351
Bellotti, Francesco 468, 475, 481
Benini, Luca 21
Bernardini, Ethan 142
Berruti, G. M. 292
Berselli, Giovanni 251
Berta, Riccardo 468, 475, 481
Bertuccio, Giuseppe 170
Boccarossa, M. 369
Boni, E. 435
Borghese, A. 369
Borghi, Giacomo 3
Boschi, Marco 213
Bossi, Federica 213
Botrugno, Chiara 429
Brancali, Giulio 142
Breglio, G. 369
Breglio, Giovanni 274, 328
Buffoli, Andrea 189
Buontempo, Salvatore 274
Burla, Maurizio 142
Busatto, Giovanni 375
Bzeih, Fatima 35

C

- Camarchia, Vittorio 121, 132
Campagna, Riccardo 170
Campanella, Sara 177
Campopiano, Stefania 328, 335
Capello, Alessio 475, 481
Caputo, Domenico 199
Carminati, Marco 3
Carrano, Vincenzo 316
Casadei, Benedetta Caterina 213
Casalino, Silvia 199
Catalano, A. P. 369
Catalano, Antonio Pio 362
Caviglia, Daniele D. 41
Chiara Capelli, 221
Chiari, Marcella 221
Chibli, Hussein 462
Ciaramelletti, Carola 94
Ciccognani, Walter 105, 113
Colaiuda, Davide 163
Colalongo, Luigi 48
Colangeli, Sergio 105, 113
Collu, Riccardo 448
Consales, M. 292
Cossettu, Piero 448
Cossu, Marianna 475
Costa Angeli, Martina Aurora 244
Cova, Paolo 382
Crescitelli, Alessio 308
Crico, Monica 301
Crupi, Ilaria 441
Cuomo, Mariaconsiglia 328
Cusano, A. 292

D

- d'Alessandro, V. 369
d'Alessandro, Vincenzo 362
Dabbous, Ali 468
Damin, Francesco 221
De Ambroggi, Fabio 21
De Carlo, Martino 341

de Cesare, Giampiero 199
 De Gaetano, Samuele 301
 De Lellis, Giovanni 274
 De Leonardis, Francesco 341
 De Marchi, Luca 422
 de Oliveira Figares, Cainã 221
 De Vecchi, Arianna 213, 441
 De Vita, Elena 328
 Dedolli, Irisa 170
 Del Monte, Ettore 170
 Dell'Olio, Francesco 285, 429
 Della Sala, Riccardo 29
 Delmonte, Nicola 382
 Di Benedetto, Luigi 71
 Di Crescenzo, Antonia 274
 Di Giacomo, Susanna 3
 Di Meo, Valentina 308
 Dini, Pierpaolo 351

E

Esposito, Emanuela 308
 Esposito, Flavio 335
 Evangelista, Yuri 170

F

Faustini, Paolo 48
 Feroci, Marco 170
 Ferrari, Giorgio 221, 301, 322
 Ferrazzano, Elena 448
 Ferri, Giuseppe 163
 Fienga, Francesco 274
 Fiori, Franco 12
 Fiorini, Carlo 3
 Forneris, Luca 475
 Fort, Ada 487
 Franchi Scarselli, Eleonora 413
 Fresta, Matteo 475, 481
 Frisoli, Antonio 407
 Frroku, Saimir 390

G

Galdi, Vincenzo 308
 Gandola, Massimo 228
 Gasparini, Leonardo 228
 Gastaldo, Paolo 407, 422
 Gervasoni, Giacomo 441
 Gianoglio, Christian 238, 258, 456
 Gianoglio, christian 462
 Giordano, Michele 335

Giudici, Andrea 441
 Gnani, Elena 61
 Gnudi, Antonio 85
 Goldoni, Daniele 266
 Grassi, Marco 170
 Grillotti, Filippo 21
 Guidetti, Elio 21
 Guidoni, Leonardo 94
 Guillén, Mariano José 266

H

Hijazi, Zeinab 35
 Hübner, Martin 142
 Huesgen, Till 390

I

Iaccarino, Emanuela 308
 Iadicicco, Agostino 328, 335
 Ibba, Pietro 244
 Ibrahim, Ali 35
 Irace, A. 369
 Irace, Andrea 274, 390

K

Khalifeh, Razan 238
 Kunst, Marinus 316
 Kutteeri, Rahuldas 341

L

Lagonigro, F. 435
 Lai, Stefano 448
 Laita, Gabriele 189
 Lange, Sebastian 142
 Langfelder, Giacomo 189, 205
 Lazzaroni, Luca 468
 Leogrande, Elisabetta 429
 Leone, M. 292
 Leoni, Alfiero 163
 Licciardo, Gian Domenico 71
 Liguori, Rosalba 71
 Limiti, Ernesto 77, 105, 113
 Longhi, Patrick E. 113
 Longhi, Patrick Ettore 105
 Lophitis, N. 369
 Lovecchio, Nicola 199
 Lugli, Paolo 244

M

Macucci, Massimo 94

- Madrid, Rossana 266
Malcovati, Piero 170
Manuzzato, Enrico 228
Marchi, Luca De 413
Marconcini, Paolo 94
Maresca, L. 369
Marrazzo, Vincenzo Romano 274, 328
Martano, Emanuele 375
Martinelli, Daniele 413
Mascia, Antonello 448
Mattia Garavagno, Andrea 407
Maurina, Arianna Adelaide 221
Meacci, V. 435
Mele, Filippo 170
Melloni, Andrea 322
Melnyk, K. 369
Micheli, Chiara 251
Moccia, Massimo 308
Morichetti, Francesco 322
Moslemi, Amin 335
- N**
Nadalini, Alessandro 21
Namdari, Ali 41
Nascetti, Augusto 199
Natale, Teresa 285, 429
Neitzert, Heinz-Christoph 316
Nicolini, Jacopo 266
Nistor, I. 369
Nkembi, Armel Asongu 382
- O**
Orecchini, Giulia 142
- P**
Paganelli, Simone 94
Palazzi, Valentina 142
Palazzo, Simone 375
Palma, Lorenzo 177
Pan, Leidan 121
Paolini, Roberto 448
Parand, Peiman 105
Pasotti, Marco 413
Passaro, Vittorio M. N. 341
Passerone, Roberto 228
Perenzoni, Matteo 228
Persiano, G. V. 292
Petrelli, Mattia 244
Petti, Luisa 244
- Piacibello, Anna 121, 132
Pighetti, Alessandro 468
Pileri, Luca 205
Ploner, Moritz 244
Presentación, Sara Muñoz 468
Prinz, Timo S. 142
Procissi, Gregorio 94
- R**
Ragusa, Edoardo 407, 422
Rahimo, M. 369
Ramalli, A. 435
Raschi, Lorenzo 85
Reale, Andrea 77
Rendina, Ivo 308
Riccio, M. 369
Riccio, Michele 274
Richelli, Anna 48
Rinaldi, Nicola 71
Romano, Claudio 351
Ronchi, Michele 3
Rosa, Andrea 48
Rossi, Davide 21
Rubino, Alfredo 71
Ruvo, Menotti 308
- S**
Sacchi, Emanuele 322
Salvatore, Giovanni A. 390
Sampietro, Marco 221, 301, 322
Sandomenico, Annamaria 308
Sannino, Diana 316
Sanseverino, Annunziata 375
Sansone, Lucia 335
Santoro, Danilo 382
Saponara, Sergio 351
Scandelli, Alice 213, 441
Schiavolini, Giacomo 142
Scognamillo, C. 369
Scognamillo, Ciro 362
Scotti, Giuseppe 29
Selmi, Luca 266
Seminara, Lucia 251
Serino, Antonio 105
Serra, Jacopo 12
Shalby, Hazem Hesham Yousef 213
Sharma, Ankit Bhushan 390
Shebly, Daniella 462
Shkodra, Bajramshahe 244

Singh, Arpana 316
Sola, Laura 221
Soltanmuradov, Vafali 481
Soref, Richard A. 341
Speranza, Vito 316
Spinelli, Filippo 487
Srour, Oussama 35
Stornelli, Vincenzo 163

T

Tagliaferri, Anna 244
Tedeschi, Riccardo 21
Terracciano, V. 369
Testa, Riccardo 258
Tortoli, P. 435
Trojaniello, Diana 441

U

Ugolini, Tommaso 61

V

Vaiano, P. 292
Valle, Maurizio 238, 258, 456, 462

Velardi, Francesco 375
Verdi, P. 435
Vignoli, A. 435
Vignoli, Valerio 487
Villa, Federica 213, 441

W

Wang, Weimin 121
Westerhof, Camille C. A. 142
Wu, Yongle 121

Y

Yaacoub, Mohamad 258, 462

Z

Zanetto, Francesco 221, 301, 322
Zarotti, Francesca 77
Zavalloni, Francesco 413
Zhang, Zhifan 132
Zollo, Loredana 448
Zonzini, Federica 413, 422
Zunino, Rodolfo 407, 422