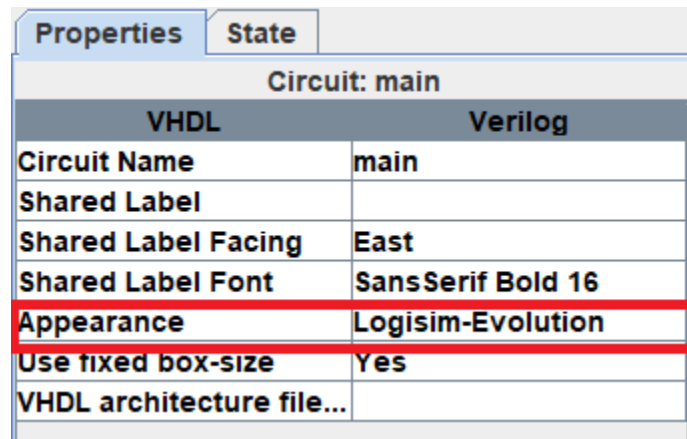


# ECS 154A: Homework 4

## Logisim

1. Use the [version from the class Google Drive of Logisim Evolution](#). Other versions may not work correctly.
2. Do not rename the files you receive. If you do so you will automatically fail the tester when you submit.
3. Put your solution for each problem into implementation subcircuit
4. Do not rename the implementation subcircuit anything else. If you do so you will automatically fail the tester when you submit.
5. Do not change the appearance of the implementation subcircuit from what it is set as. Doing so will cause you to automatically fail the tester when you submit.
  - a. That is this field right here



Properties		State
Circuit: main		
VHDL		Verilog
Circuit Name	main	
Shared Label		
Shared Label Facing	East	
Shared Label Font	SansSerif Bold 16	
Appearance	Logisim-Evolution	
Use fixed box-size	Yes	
VHDL architecture file...		

6. Do not move the pins inside of the implementation subcircuit as that affects the appearance of the circuit on the outside as you saw in discussion. Doing so will cause you to automatically fail the tester when you submit.
  - a. If you want to “move the pins” instead connect tunnels to the pins and move the tunnels around.
7. Do not name any of the subcircuits in your solution main. Doing so will cause you to automatically fail the tester when you submit.
8. You **can** create as many other subcircuits as you want in your solution. Just make sure your solution ends up in the implementation subcircuit

# Restrictions

For all problems in this homework, you may only use

- All of the components under Wiring
- All of the components under Gates **EXCEPT** for Controlled Buffer, Controlled Inverter, PLA
- All of the components under Plexers
- All of the components under Arithmetic
- All of the components under Memory **EXCEPT** for **RAM**, **ROM**, and **Random** Generator

Unless a problem specifies otherwise.

You have been provided a Register File circuit in the starting circuit. The **only outputs** of the register file that you are allowed to use are A\_Out and B\_Out. The rest are for testing purposes and **should not be used**. Using them will result in a 50% penalty in your grade.

## Problem 1: CPU.circ (100 points)

Build a 4-bit single cycle CPU that can implement the given instructions.

### Instruction Format

Our CPU will be using fixed length instructions. Our CPU will also have two types of instruction formats: R-type and I-type. In R-type instructions both operands come from registers. In I-type instructions, the first operand comes from a register and the second will be contained within the instruction.

#### R-Type

Name	Bits	Description
OpCode	15 - 12	Determines what operation should be performed
C	11 - 8	The destination register. The C in $\text{Reg}_C = \text{Reg}_A \text{ OP } \text{Reg}_B$
A	7 - 4	The first source register. The A in $\text{Reg}_C = \text{Reg}_A \text{ OP } \text{Reg}_B$
B	3 - 0	The second source register. The B in $\text{Reg}_C = \text{Reg}_A \text{ OP } \text{Reg}_B$

## I-Type

Name	Bits	Description
OpCode	15 - 12	Determines what operation should be performed
C	11 - 8	The destination register. The C in $\text{Reg}_C = \text{Reg}_A \text{ OP Imm}$
A	7 - 4	The first source register. The A in $\text{Reg}_C = \text{Reg}_A \text{ OP Imm}$
Immediate	3 - 0	The second source register. The Imm in $\text{Reg}_C = \text{Reg}_A \text{ OP Imm}$

## Instructions

Operation	Encoding (The value in the OpCodeField)	Description
STOP	0000	The CPU ceases execution
NOP	0001	Do nothing
LOAD	0010	$\text{Reg}_C = \text{Immediate}$
MOVE	0011	$\text{Reg}_C = \text{Reg}_A$
ANDR	0100	$\text{Reg}_C = \text{Reg}_A \text{ AND } \text{Reg}_B$
ANDI	0101	$\text{Reg}_C = \text{Reg}_A \text{ AND Immediate}$
ORR	0110	$\text{Reg}_C = \text{Reg}_A \text{ OR } \text{Reg}_B$
ORI	0111	$\text{Reg}_C = \text{Reg}_A \text{ OR Immediate}$
XORR	1000	$\text{Reg}_C = \text{Reg}_A \text{ XOR } \text{Reg}_B$
XORI	1001	$\text{Reg}_C = \text{Reg}_A \text{ XOR Immediate}$
NOT	1010	$\text{Reg}_C = \text{NOT } \text{Reg}_A$
NEGATE	1011	$\text{Reg}_C = -\text{Reg}_A$
ADDR	1100	$\text{Reg}_C = \text{Reg}_A + \text{Reg}_B$
ADDI	1101	$\text{Reg}_C = \text{Reg}_A + \text{Immediate}$
SUBR	1110	$\text{Reg}_C = \text{Reg}_A - \text{Reg}_B$
SUBI	1111	$\text{Reg}_C = \text{Reg}_A - \text{Immediate}$

## Inputs

Pin	Size (in bits)	Explanation
Instruction	16	The instruction located at Instruction_Address
ClkIn	1	The Clock. Connect this to the clock ports of your registers/flip-flops. Do nothing else with this.

## Outputs

Pin	Size (in bits)	Explanation
Instruction_Address_Out	5	The address of the instruction you want to execute
Reg0-15	4	The values in the register file. This has already been connected for you

## CPU Components

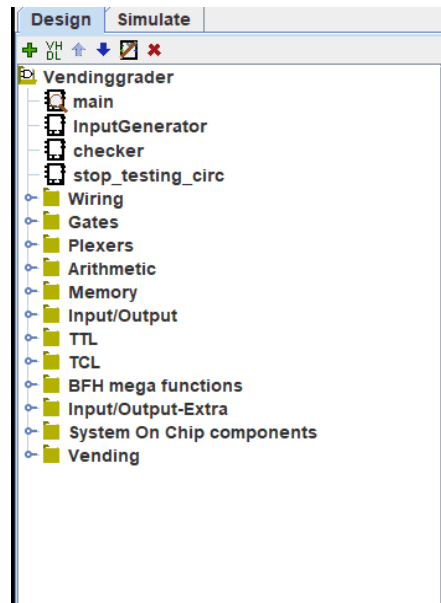
Your CPU should have

- A Program Counter (PC)
  - This stores and keeps track of what instruction you are on
- Instruction Decoder
  - This is a bunch of combinational logic that sets the control signals inside of your CPU
- Register File
  - A bunch of registers as well as ways to specify which ones you want. This has already been created for you.
  - The **only outputs** of the register file that you are allowed to use are A\_Out and B\_Out. The rest are for testing purposes and **should not be used**. Using them will result in a 50% penalty in your grade.

# Testing

Testing for this problem is different than for previous assignments but is more similar to sequential circuits than combinational circuits. After you finish building your circuit and are ready to test it

1. Open the associated grader circuit
2. Scroll down on the left and side until you find your circuit. Right-click on it and select Reload Library



- a.
3. Use ctrl+t to tick the clock and check that the outputs of the registers are what they are supposed to be as based on the test program below.

## The Test Program

Instruction	Meaning	Result
LOAD REG <sub>0</sub> , 3	Reg <sub>0</sub> = 3	Reg <sub>0</sub> = <b>3</b>
LOAD REG <sub>1</sub> , 6	Reg <sub>1</sub> = 6	Reg <sub>1</sub> = <b>6</b>
NOP	Do Nothing	No Change
MOVE REG <sub>2</sub> , Reg <sub>1</sub>	Reg <sub>2</sub> = Reg <sub>1</sub>	Reg <sub>2</sub> = <b>6</b>
ANDR REG <sub>3</sub> , REG <sub>0</sub> , REG <sub>1</sub>	REG <sub>3</sub> = REG <sub>0</sub> AND REG <sub>1</sub>	REG <sub>3</sub> = 3 & 6 = <b>2</b>
ANDI REG <sub>4</sub> , REG <sub>3</sub> , 3	REG <sub>4</sub> = REG <sub>3</sub> AND 3	REG <sub>4</sub> = 2 & 3 = <b>2</b>
ORR REG <sub>5</sub> , Reg <sub>2</sub> , REG <sub>0</sub>	REG <sub>5</sub> = Reg <sub>2</sub> OR REG <sub>0</sub>	REG <sub>5</sub> = 6   3 = <b>7</b>
ORI REG <sub>6</sub> , Reg <sub>3</sub> , 12	REG <sub>6</sub> = Reg <sub>3</sub> OR 12	REG <sub>6</sub> = 2 OR 12 = <b>14</b>
XORR REG <sub>7</sub> , Reg <sub>2</sub> , REG <sub>0</sub>	REG <sub>7</sub> = Reg <sub>2</sub> XOR REG <sub>0</sub>	REG <sub>7</sub> = 6 ^ 3 = <b>5</b>
XORI REG <sub>8</sub> , Reg <sub>6</sub> , 15	REG <sub>8</sub> = Reg <sub>6</sub> XOR 15	REG <sub>8</sub> = 14 ^ 15 = <b>1</b>
NEG REG <sub>9</sub> , REG <sub>3</sub>	REG <sub>9</sub> = -REG <sub>3</sub>	REG <sub>9</sub> = <b>-2</b>
ADDR REG <sub>10</sub> , Reg <sub>7</sub> , REG <sub>7</sub>	REG <sub>10</sub> = Reg <sub>7</sub> + REG <sub>7</sub>	REG <sub>10</sub> = 5 + 5 = <b>10</b>
ADDI REG <sub>11</sub> , Reg <sub>1</sub> , 3	REG <sub>11</sub> = Reg <sub>1</sub> + 3	REG <sub>11</sub> = 6 + 3 = <b>9</b>
SUBR REG <sub>12</sub> , Reg <sub>6</sub> , REG <sub>2</sub>	REG <sub>12</sub> = Reg <sub>6</sub> - REG <sub>2</sub>	REG <sub>12</sub> = 14 - 6 = <b>8</b>
SUBI REG <sub>13</sub> , Reg <sub>8</sub> , 5	REG <sub>13</sub> = Reg <sub>8</sub> - 5	REG <sub>13</sub> = 1 - 5 = <b>-4</b>
NOT REG <sub>15</sub> , REG <sub>8</sub>	REG <sub>15</sub> = NOT REG <sub>8</sub>	REG <sub>15</sub> = ~1 = <b>14</b>
ANDR REG <sub>1</sub> , REG <sub>12</sub> , REG <sub>13</sub>	REG <sub>1</sub> = REG <sub>12</sub> AND REG <sub>13</sub>	REG <sub>1</sub> = 8 & 12 = <b>8</b>
NEG REG <sub>5</sub> , REG <sub>5</sub>	REG <sub>5</sub> = -REG <sub>5</sub>	REG <sub>5</sub> = <b>-7</b>
NOP	Do Nothing	No Change
ADDR REG <sub>14</sub> , REG <sub>5</sub> , REG <sub>2</sub>	REG <sub>14</sub> = Reg <sub>5</sub> + REG <sub>2</sub>	REG <sub>14</sub> = -7 + 6 = <b>-1</b>
XORR REG <sub>7</sub> , REG <sub>7</sub> , REG <sub>14</sub>	REG <sub>7</sub> = Reg <sub>7</sub> ^ REG <sub>14</sub>	REG <sub>7</sub> = 5 ^ -1 = <b>10</b>
ORI REG <sub>2</sub> , REG <sub>2</sub> , 3	REG <sub>2</sub> = Reg <sub>2</sub>   3	REG <sub>2</sub> = 6   3 = <b>7</b>
SUBI REG <sub>13</sub> , REG <sub>13</sub> , 12	REG <sub>13</sub> = REG <sub>13</sub> - 12	REG <sub>13</sub> = 12 - 12 = <b>0</b>
STOP	CPU should cease execution	CPU should cease execution

LOAD REG <sub>15</sub> , 13	This line should not be executed because the CPU should have STOPped already	This line should not be executed because the CPU should have STOPped already
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The test program is just an **example program**. Your CPU should function on **any program** given to it.

## Making Fixes to Your Solution

After you make changes to your solution you will need to reload your circuit in the grader circuit. If you don't it won't see the updates. To reload your circuit, select your circuit in the grader, right-click it and select Reload Library.

## Submitting

### Submit to

Logisim Homework 3 on GradeScope.

### What to Submit

Submit a zip file that contains the following .circ files

1. CPU.circ

Inside of each .circ file leave a comment with you and your partner's names.

Make sure that you submit a zip that contains the files and **NOT** the **folder containing the files**. Check out the animation below for what to submit.



