CS51 – Homework #10

1. Given the following sequence of memory references to an empty eight-block direct mapped cache, fill in the table for the cache:

Word Addr	Binary Addr
27	11 011
9	01 001
30	11 110
19	10 011
9	01 001
23	10 111
27	11 011

Index	V	Tag	Data	Hit or Miss?
000	N			
001	Y	01	Mem[01001]	Hit
010	N			
011	Y	11	Mem[11011]	Miss
100	N			
101	N			
110	Y	11	Mem[11110]	Miss
111	Y	11	Mem[11111]	Miss

2. Suppose a CPU has a base CPI of 1, a clock rate of 3.6 GHz, a main memory access time of 220 ns, and a miss rate per instruction at primary (L1) cache is 3%.

   NOTE: For this problem, round all miss penalties to the nearest integer and all CPIs to one decimal place.

   Assuming the CPU has only primary (L1) cache:
   What is the miss penalty? ___792___
   What is the new total CPI? ___32.7___

   Now assume secondary (L2) cache is present, with an access time of 15 ns that reduces the miss rate to main memory by 0.6%.
   What is the miss penalty for a primary miss with an L2 hit? ___54___
   What is the miss penalty for a primary miss with an L2 miss? ___846___
   What is the new total CPI? ___7.9___