```
// ====== Chip_Select (Addres decoder) ========
             0xFF00
                           always @*
 Other
                            begin
                               case (j1_io_addr[15:8]) // direcciones - chip_select
             0x7000
                                 8'h67: cs= 3'b100;
                                                                 //mult
                                 8'h68: cs= 3'b010;
                                                                 //div
 UART
                                 8'h69: cs= 3'b001;
                                                                 //uart
             0x6900
                                 default: cs= 3'b000;
 Divider
                               endcase
             0x6800
                            end
                            // ====== Chip_Select (Addres decoder) ========
Multiplier
             0x6700
 BRAM
             0x0000
                                                                      cs1
                                                               Address cs2
                                                               decoder
                                                                      cs3
                                                                              d_in[15:0]
                                                                           cs1<sub>▶</sub> cs
                      io_din[15:0]
                                                                                 addr
                                                                                                d_out[15:0]
                     io_dout[15:0]
                                                                               ► rd
                     io_addr[15:0]
                                                                                                multiplier.v
                                                                               → wr
             J1.v
                            io_rd
                            io_wr
                                                                                 d_in[15:0]
                                                                                                                       100
                                                                           cs2 cs
                            uart.v
                                                                                                                       010
                                                                                 addr
                                                                                                 d_out[15:0]
                                                                                rd
                                                                                                                       001
                                                                                                   divider.v
                                                                               wr
                                                                                 d_in[15:0]
                                                                           cs3<sub>▶</sub>
                                                                                 CS
                                                                                                                       cs[1:3]
                                                                                 addr
                                                                                                 d_out[15:0]
                                                                                                                                      uart_tx
                                                                                 rd
                                                                               → wr
                                                                                                      uart.v
                                                                                                                                      led_out
```







