Verification of the VHDL Description with Spyglass 5.2 of Atrenta

1) Introduction

Document Used: Spyglass 5.2.0 UserGuide

a) Objective:

Solve various design issues in the early stages of the design development process.
For that it provides a pre-packaged set of goals and methodologies called GuideWare.

b) Goal (definition): is a pre-packaged set of rules that detects specific types of design issues. Example: simulation goal contains rules that checks for basic simulation issues in a design. When you run a goal after specifying design files in Atrenta Console qll rules of that goal are run. Once the run is complete, appropriate violations messages are reported to indicate design issues.

c) Methodology (definition): A collection of sub-methologies or a collection of goals. GuideWare is the methodology used by Atrenta - it provides guidance to designers to address various design issues by running a set of goals that are fine-tuned for high-quality and low noise.

2) Launch the SpyGlass

a) Launch SpyGlass 5.2

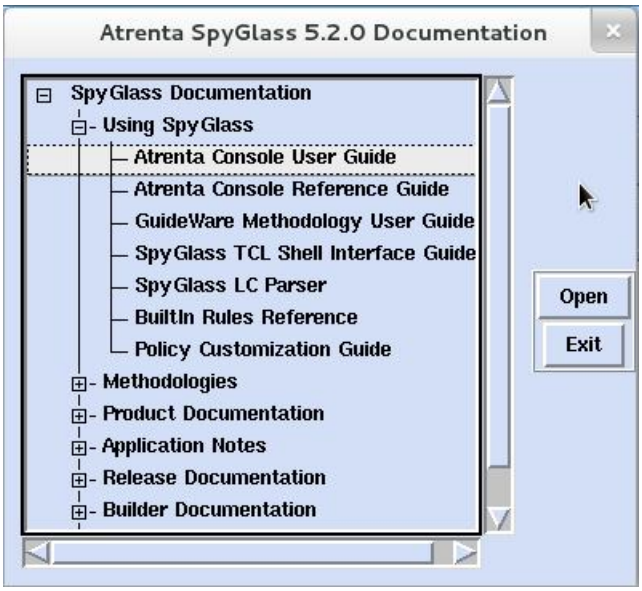
- Open the diretory that has the file ".bashrc_spyglass5_2_0".

- Commands to initialize Spyglass:
  -". ./.bashrc_spyglass5_2_0"
- Launch :
  -"spyglass"

```
:~/projet_atrenta$ . ./.bashrc_spyglass5_2_0
:~/projet_atrenta$ spyglass &
```

- It is possible to access the pdfs of UserGuide by the graphic interface of Spyglass

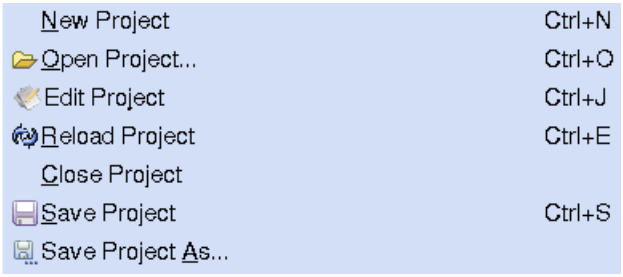
- Console_User_Guide.pdf can be accessed by "Help-> Spyglass Manuals-> Using Spyglass-> Atrenta Console UserGuide



- GUI Spyglass - Pages 24 and 25

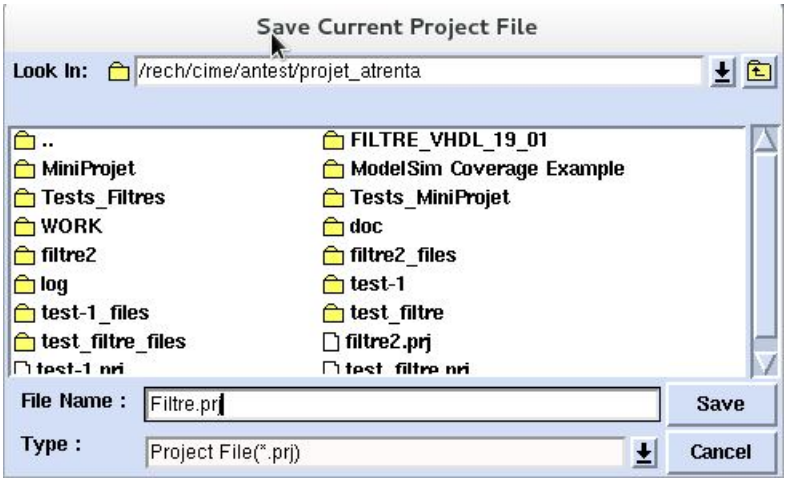
b) Creating your project

- In the top-left : "File -> New Project" to create one
- "File -> Save Project (Ctrl + S)" to save one.



- Project will be saved as a file ".prj", a directory "name of the project" and another directory "name of the project files".

- Create a New Project. It will receive a standard name, spyglass-1, from the software. Change the name of the projet for one that better suits it, par example “Filtre”, with the command "File -> Save Project as ..."



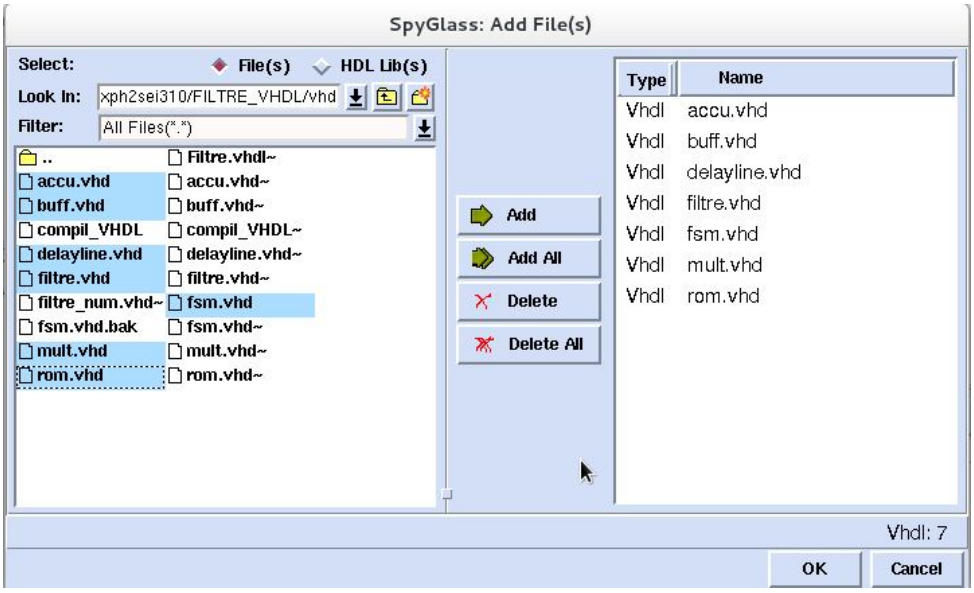
- Verify the file “Filtre.prj” and the directories “Filtre” and “Filtre_files” were created in the directory that you launched the software.

3) Adding your Files and Running DesignRead Verification

a) Add your Files

- Click "Add File(s)" at the "Add Design Files" Tab and select your VHDL files of the Filtre (files *.vhd). They are located in *${TP_PATH} / vhd* directory.

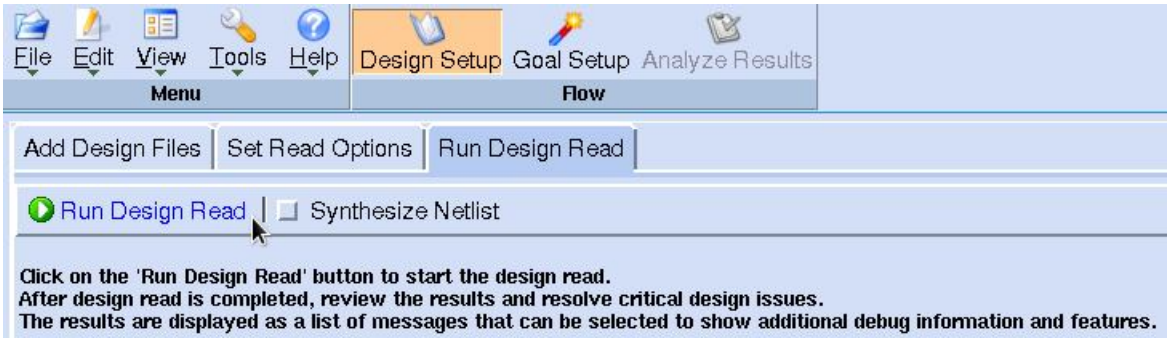
- There are 7 files to be added as shown in the picture above:



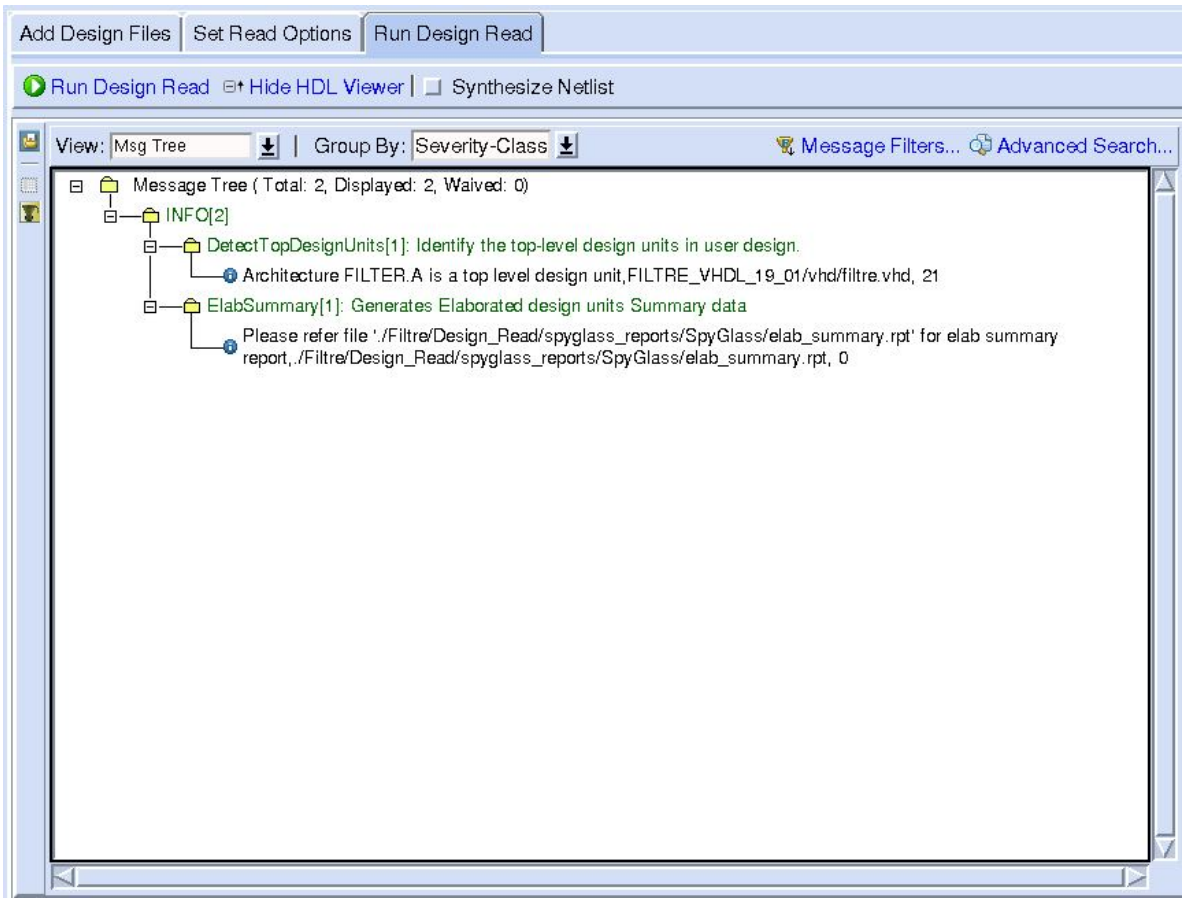
- After adding them, the window “HDL Files”, at the left-side, will show the files.
- You can delete a file by Right Click -> Delete or Select the file and push the button "Delete";
- You can edit a file by Right Click -> Edit and it will open with the VI editor;

b) Run DesignRead

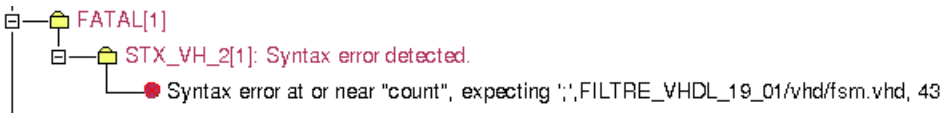
- Select the "Run Design Read" Tab and click at "Run Design Read".



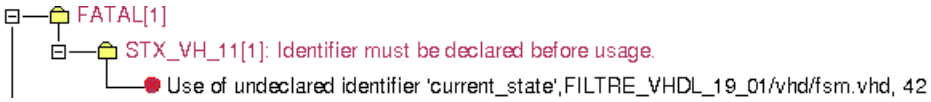
- After the “Run Design Read”, a window will show the messages about the verification.



- Examples of Errors and Warnings:
    - Syntax FATALs :



    - Identifier Must be Declared Before Usage FATAL:



    - New File Warning: If you edited a file and redo the “Run Design Read” there will be a warning.

- Its highly recommended that you corrected all errors detected and verify the warnings before passing to the next phase.

- Save your project

4) Running LINT and ADV_LINT Goals and Analysing Results

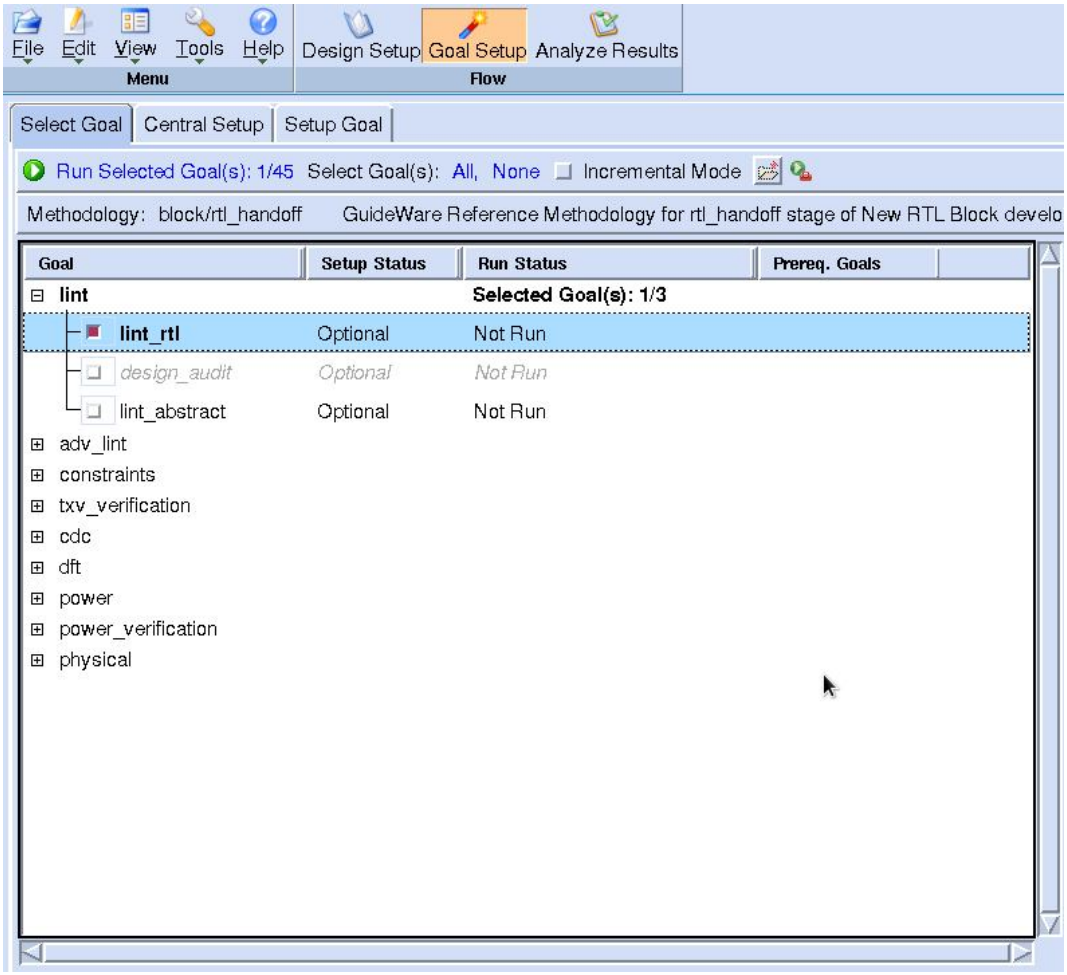
- Now, to run the other verifications, you need to change your main tab (top-middle) from “Design Setup” to “Goal Setup”

a) Running LINT

- You are now at the “Goal Setup -> Select Goal” tab and, as you can see, there are many goals that can be run to verify specific characteristics of your VHDL description.

- As you click in the name of a goal, the window “Help” at the right-side will display some informations about it (what the goal tests and can reveal of your description).

- Select the Goal LINT/LINT_RTL as shown in the figure above:



- Run it by clicking “Run Selected Goals” in the top-left.

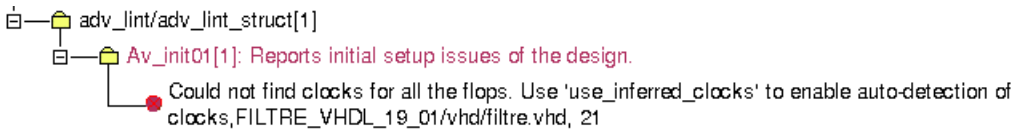
- Examples of Errors and Warnings:
    - Latchs
    - Code Non Synthesizable

- Run the others Goals of LINT and correct theirs errors as well.

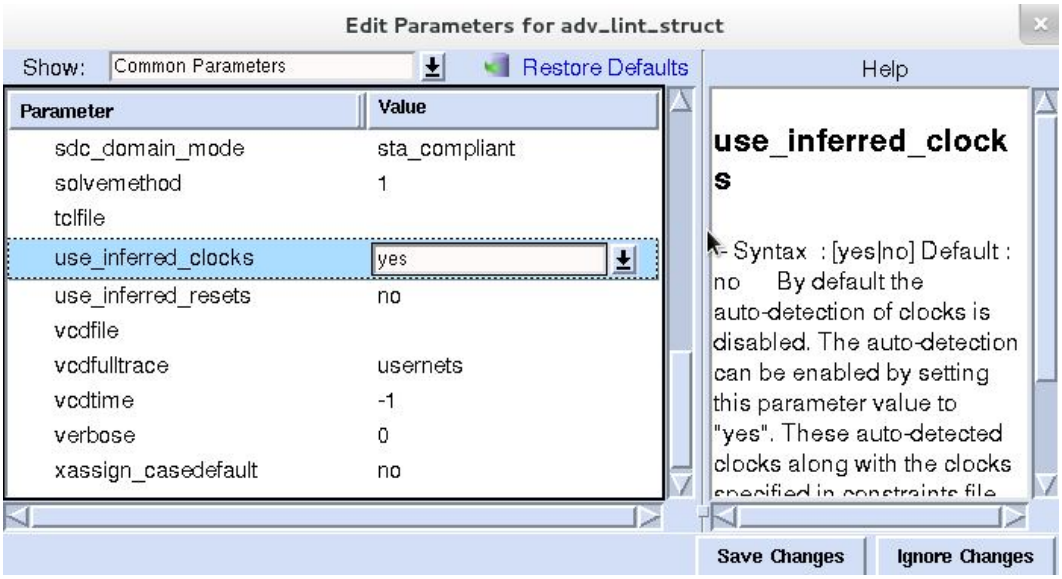
b) Running ADV_LINT

- After correcting the errors of LINT, you can run the goals of ADV_LINT. The main ones are ADV_LINT_STRUCT and ADV_CONNECTIVITY

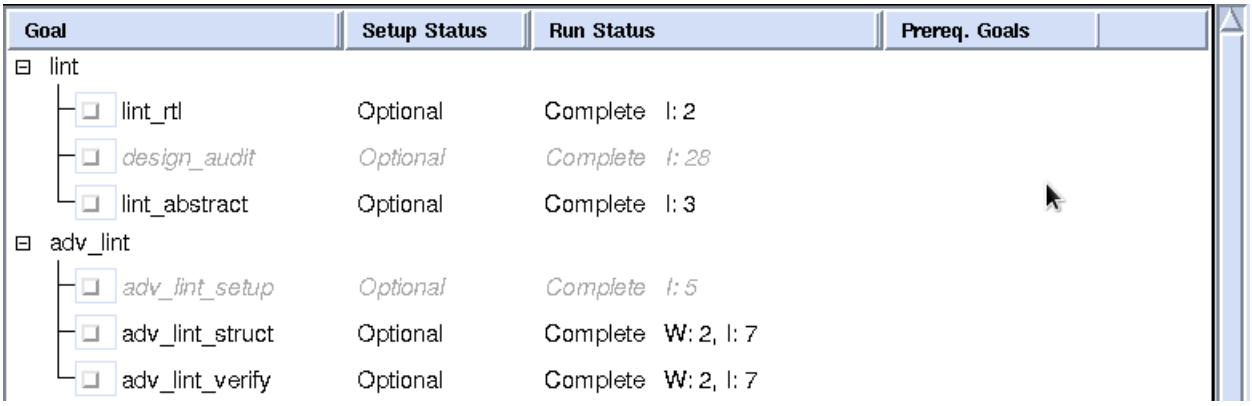
- You will propably find one FATAL error about a intial setup design. The software suggest to change the “use_inferred_clock” parameter of the goal.



- To edit the parameter Right-Click the goal in the “Select Goal” tab and choose “Edit Parameter”.
Search the parameter and change it to “Yes”. Save the changes.



- After running all the goals, you should have something like this in your “Select Goals” Tab.



Congratulations, You have ended your Verifications with Spyglass