

REFERENCIA Examen02Comp

Signals	RST	selRst	LPC	selPC	selComp	checkMode	LMAR	LIR	WE	RW	LB	LA	LO	LFZ	selBSrc<1>	selBSrc<0>	aluOp<1>	aluOp<0>	SV	endOfCode
States	cw19	cw18	cw17	cw16	cw15	cw14	cw13	cw12	cw11	cw10	cw9	cw8	cw7	cw6	cw5	cw4	cw3	cw2	cw1	cw0
Idle	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CheckPC	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
EndCodeSegment	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
LoadInst	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Decode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
CheckDir	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
WritePC	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SegmentViolationException	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
LoadAddress	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0
MovB	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0
LoadA	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
MovA	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
WBMem	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
ReadRegisters	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
Add	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
WBReg	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Sub	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0
ReadImm	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0

ALU OPERATION	AluOp<1>	AluOp<0>
MOV A	0	0
MOV B	0	1
ADD	1	0
SUB	1	1

Test data

RAM Address	Instruction	RAM Data
0x0	LD 12, R3	000 1100 011
0x1	LD 15, R4	000 1111 100
0x2	ADD R3, R4	010 0011 100
0x3	ST 13, R4	001 1101 100
0x4	INC 6, R4	100 0110 100
0x5	DEC 10, R4	101 1010 100
0x6	BEQ 10	110 1010 000
0x7	-	000 0000 000
0x8	-	000 0000 000
0x9	-	000 0000 000
0xA	-	000 0000 000
0xB	Data segment	000 0000 010
0xC	Data segment	000 0000 011
0xD	Data segment	000 0000 000
0xE	Data segment	000 0000 000
0xF	Data segment	000 0000 001



