Nyks TriPi Development Kit

User Manual

Product Information	Code	Name
Product	KFM-E-T20-144	Nyks TriPi Development Kit

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Approval Information	Name	Position	Date
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Verified by	Çağdaş Çelebi	Quality Admin.	30.11.2023
Approved by			

Document History

Version	Date	Author	Comment
01	26.10.2023	Abdulsamet Aldaş	Version 01
Explanations	First revision of the document.		

Purpose

The purpose of this document is to present characteristics of Nyks TriPi Development Kit to the user, and to provide the user with a comprehensive guide to understanding and using the Nyks TriPi Development Kit.

Summary

This document first gives an overview of the Nyks TriPi Development Kit followed by a detailed description of its features and configuration options. In addition, references to other useful documents are included.

Table of Contents

1 Overview

1.1 General

1.1.1 Introduction

TriPi is a ready-to-use, low-cost FPGA development platform based on the Trion T20 FPGA from EFINIX. TriPi is designed specifically for makers and students. The board can be programmed via USB. Raspberry Pi HATs and Digilent PMOD add-on boards are supported via dedicated interfaces. The combination of the Sapphire SoC and logic allows for the customization of software-defined peripherals and controllers tailored for the target application. With onboard 100Mbit/s Ethernet and an ESP32-C3 Wi-Fi/Bluetooth module, TriPi is suitable for IoT applications in addition to the other peripherals.

1.1.2 Warranty

Please refer to the General Business Conditions, available on the KuanTek website.

Warning!
Please note that the warranty of an KuanTek module is voided if the FPGA fuses are blown. This operation is done at own risk, as it is irreversible. KuanTek cannot test the module in case of a warranty product return.

1.1.3 RoHS

The Nyks TriPi Development Kit is designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.1.4 Disposal and WEEE

The Nyks TriPi Development Kit must be properly disposed of at the end of its life. The Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable for the Nyks TriPi Development Kit.

1.1.5 Safety Recommendations and Warnings

Board can be backpowered from 5V pins but not from 3.3V pins. Do not try to power the board from 3.3V pins.

1.1.6 Electrostatic Discharge

Electronic boards are sensitive to electrostatic discharge (ESD). Please ensure that the product is handled with care and only in an ESD-protected environment.

1.1.7 Abbreviations

Abbreviation	Explanation
PMOD	Peripheral Module Interface
GPIO	General-Purpose Input/Output
LVDS	Low-Voltage Differential Signalling
RoHS	Restriction of Hazardous Substances
WEEE	Waste Electrical and Electronic Equipment
ESD	Electrostatic Discharge
SPI	Serial Peripheral Interface
NOR	Not-OR (type of flash memory)
UART	Universal Asynchronous Receiver-Transmitter
FTDI	Future Technology Devices International
LED	Light Emitting Diode
PLL	Phase-Locked Loop
QSPI	Quad Serial Peripheral Interface
SD	Secure Digital
ESP32	Espressif Systems 32-bit microcontroller
RMII	Reduced Media Independent Interface
PHY	Physical Layer (networking)
MDIO	Management Data Input/Output
FPGA	Field-Programmable Gate Array
JTAG	Joint Test Action Group
TMS	Test Mode State
TCK	Test Clock
TDO	Test Data Out
TDI	Test Data In
C_RESET	Chip Reset
VCC_IO	Voltage Common Collector Input/Output
Mbit	Megabit
MHz	Megahertz
CRESET_N	Chip Reset, Active Low
GPIOL	General-Purpose Input/Output Left

Abbreviation	Explanation
GPIOR	General-Purpose Input/Output Right
CBSEL	Configuration Bit Select
CDI	Configuration Data Input
CTRL	Control
MDC	Management Data Clock
NC	Not Connected
SHLD	Shield
VDD	Voltage Drain Supply (Power Supply)
VSS	Voltage Source Supply (Ground)
GND	Ground
VREG_OUT	Voltage Regulator Output
RPI	Raspberry Pi
T20Q144C3	Model of Trion T20 FPGA
USB	Universal Serial Bus
Wi-Fi	Wireless Fidelity
SD-CARD	Secure Digital Card
PMOD-1	Peripheral Module Interface 1
PMOD-2	Peripheral Module Interface 2
Efinix	Name of the FPGA vendor

1.2 Features

- Efinix Trion T20Q144C3 FPGA
- 128 Mbit SPI NOR flash memory
- FTDI FT4232H chipset with USB controller
- Dedicated UART interface through USB
- USB type C receptacle
- 2x 12-pin PMOD-compatible GPIO socket
- Raspberry Pi compatible GPIO header
- User LEDs and buttons
    - 4 LEDs on T20Q144C3 bank 1E and 3E
    - 2 pushbuttons (connected to 1E and 3E I/O pins)
    - 33.33 MHz and 50 MHz oscillator for T20Q144C3 PLL input
- Power:

  - Power source: USB – 5V
- Micro-SD card slot
- Wi-Fi/Bluetooth module (ESP32-C3-MINI)

1.3 Deliverables

- Nyks TriPi Development Kit
- Nyks TriPi Development Kit documentation, available via download:
  - Nyks TriPi Development Kit User Manual (this document)
  - Nyks TriPi Development Kit User Schematics (PDF)
  - Nyks TriPi Development Kit Reference Design

1.4 Accessories

1.4.1 Reference Design

Nyks TriPi Development Kit reference design features an example configuration for T20 device, together with an example top level Verilog file for the user logic. Several software applications are available for the reference design, that show how to initialize the peripheral controllers, create a Sapphire SoC, and how to access the external devices. Pre-compiled binaries are included in the archive, so that users can easily check that the hardware is functional. The reference design can be downloaded from GitHub: [KuanTek's Official GitHub Page]

1.5 Efinity Tool Support

The Nyks TriPi Development Kit is supported by the Efinity Software and Efinity RISC-V Embedded Software IDE, which is available free of charge. Please contact Efinix for further information.

2 Module Description

2.1 Block Diagram

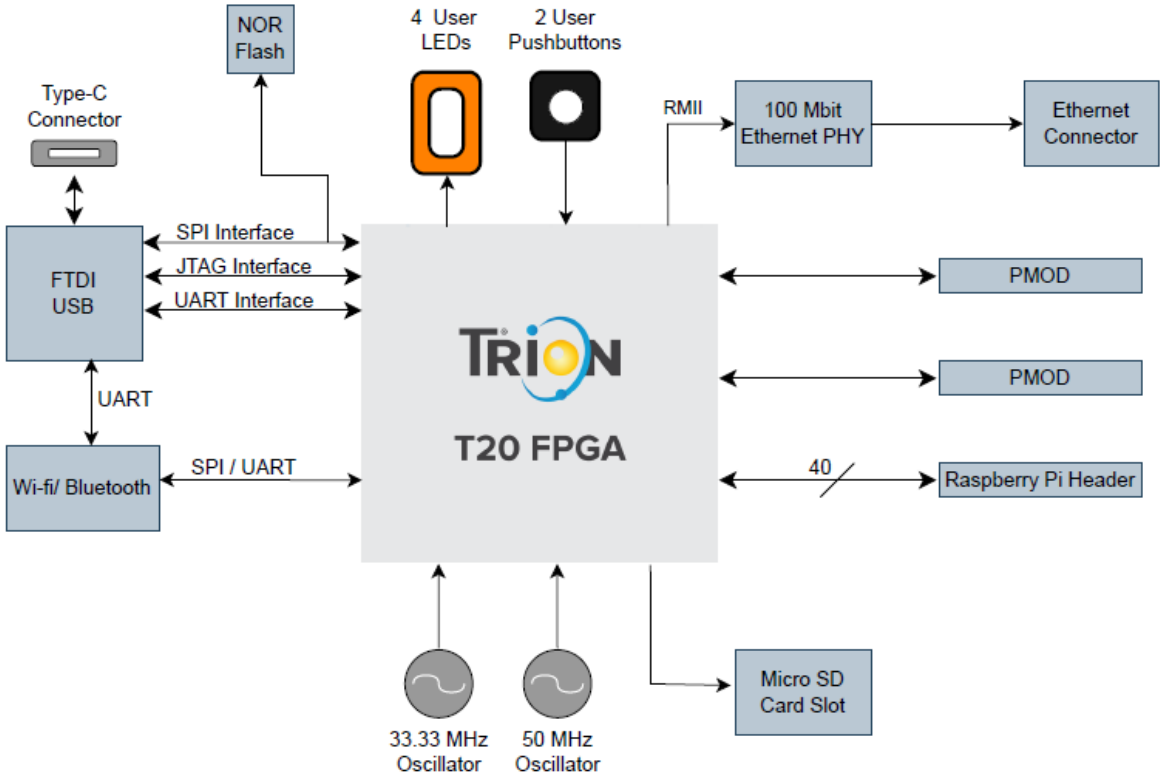

Figure 1: Module Block Diagram

2.2 Module Configuration and Product Codes

Table describes the available standard module configurations. Custom configurations are available; please contact KuanTek for further information.

Table 1: Product Code

Product Code	FPGA VENDOR	FPGA	PIN
KFM-E-T20-144	Efinix	T20	144

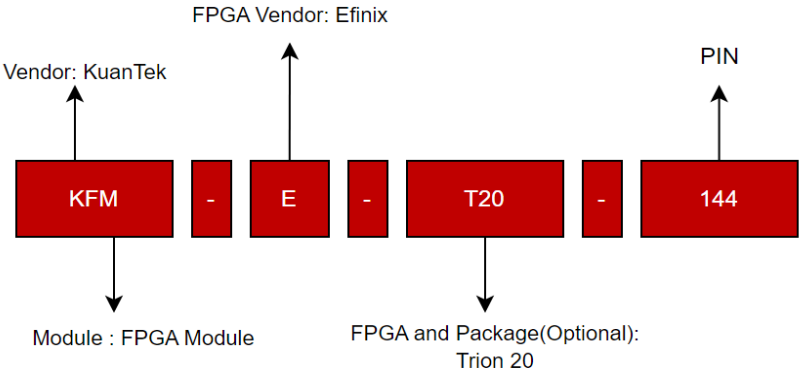

Figure 2: Product Code Fields

2.3 Top and Bottom Views

2.3.1 Top View

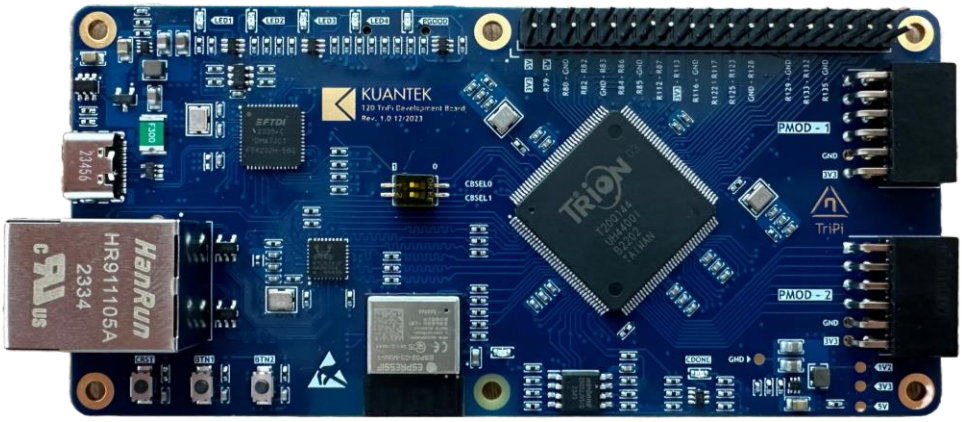

Figure 2: Module Top View

2.3.2 Bottom View

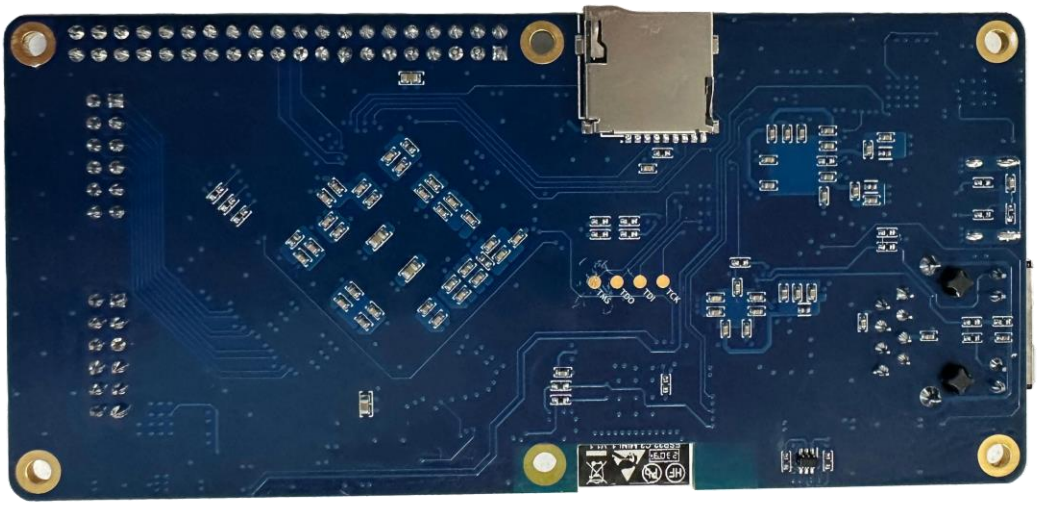

Figure 3: Module Bottom View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.4 Top and Bottom Assembly Drawings

2.4.1 Top Assembly Drawing

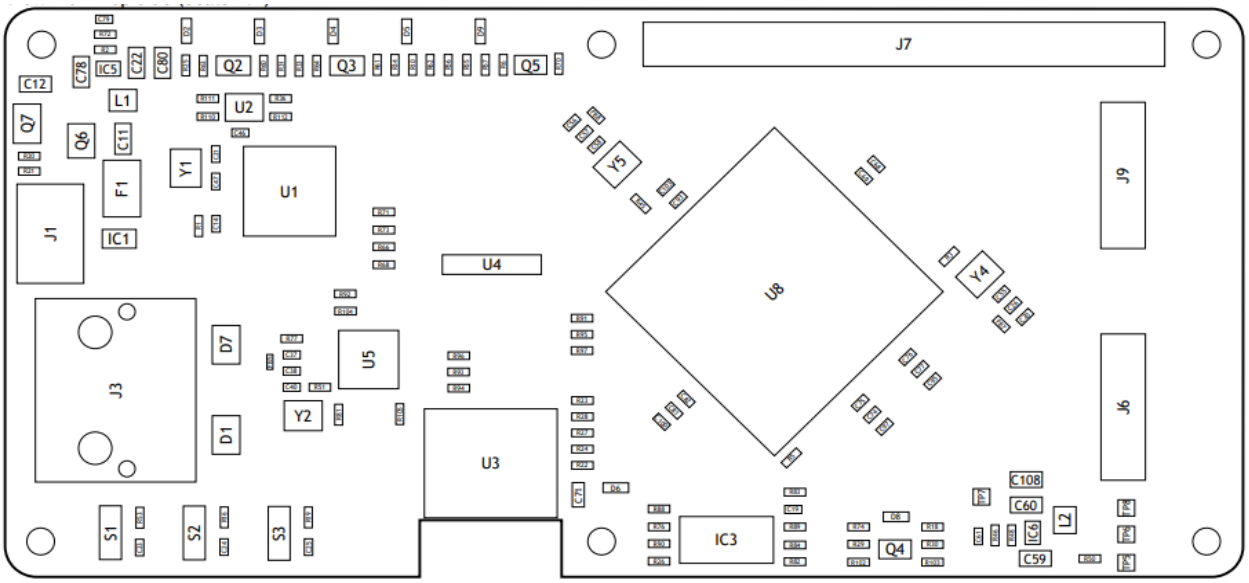

Figure 4: Module Top Assembly Drawing

2.4.2 Bottom Assembly Drawing

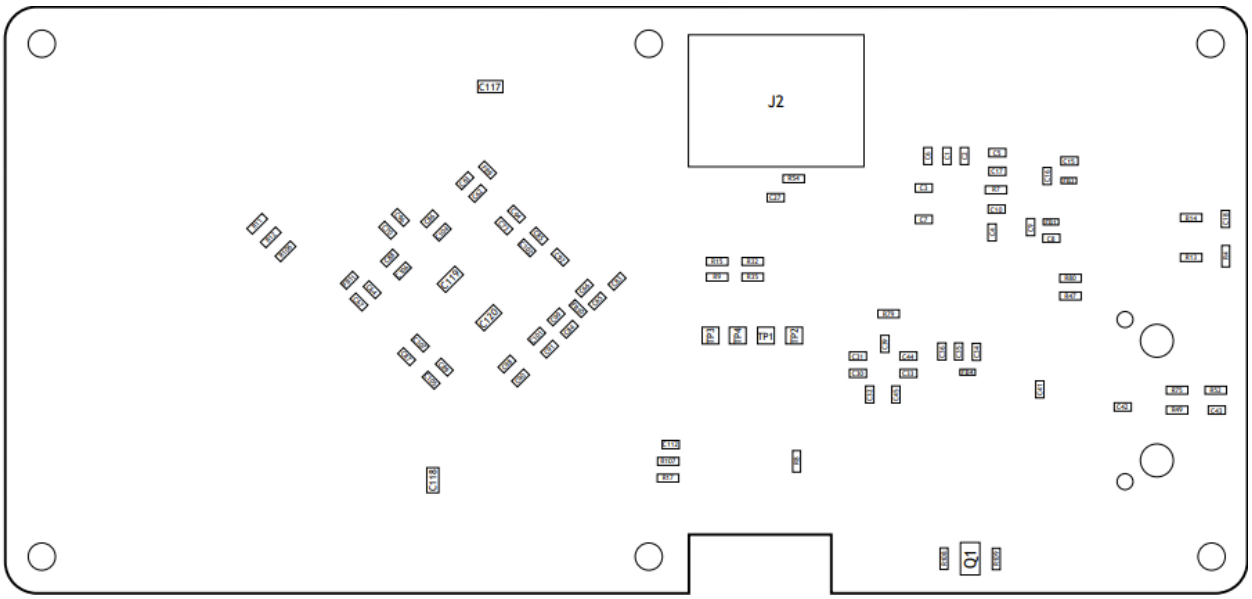

Figure 5: Module Bottom Assembly Drawing

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.5 Module Mechanical View

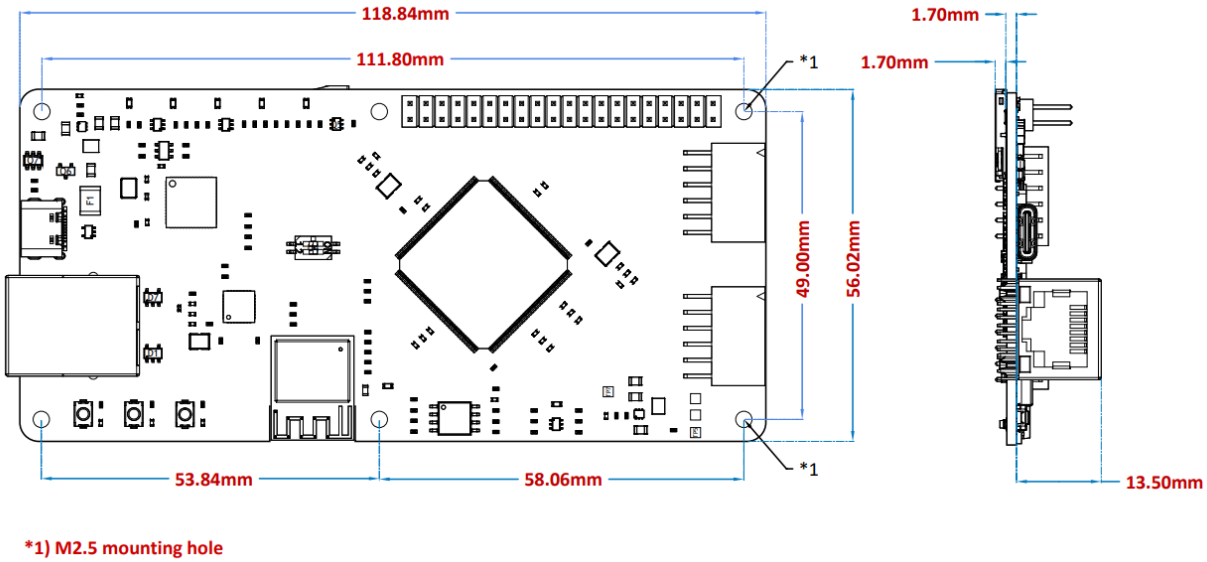

Figure 6: Module Footprint - Top View

Please note that depending on the hardware revision and configuration, the module may look slightly different than shown in this document.

2.6 Mechanical Data

Table 2 describes the mechanical characteristics of the Nyks TriPi Development Kit.

Table 2: Mechanical Data

Symbol	Value
Size	118.384 x 56 mm
Component height top	13.5 mm
Component height bottom	1.7 mm
Weight	120gr

2.7 User I/O

2.7.1 Pinout

The board contains a variety of headers to provide power, inputs, and outputs, and to communicate with external devices or boards.

Table 3*: User I/*Os

Pin Number	Module Connector	Description
Pin 1	RPI	3V3
Pin 2	RPI	5V
Pin 3	RPI	GPIOR_79_EXTFB1_CDI30
Pin 4	RPI	5V
Pin 5	RPI	GPIOR_80
Pin 6	RPI	GND
Pin 7	RPI	GPIOR_82
Pin 8	RPI	GPIOR_81_MREFCLK
Pin 9	RPI	GND
Pin 10	RPI	GPIOR_83
Pin 11	RPI	GND
Pin 12	RPI	GPIOR_86
Pin 13	RPI	GPIOR_85
Pin 14	RPI	GND
Pin 15	RPI	GPIOR_112_CDI23
Pin 16	RPI	GPIOR_87_CDI29
Pin 17	RPI	3V3
Pin 18	RPI	GPIOR_113_CDI22
Pin 19	RPI	GPIOR_116_CTRL15
Pin 20	RPI	GND
Pin 21	RPI	GPIOR_122_CLK13_CDI21
Pin 22	RPI	GPIOR_117_CTRL14
Pin 23	RPI	GPIOR_125_CLK10
Pin 24	RPI	GPIOR_123_CLK12_CDI20
Pin 25	RPI	GND
Pin 26	RPI	GPIOR_128_CTRL11
Pin 27	RPI	NC
Pin 28	RPI	NC

Pin 29	RPI	GPIOR_129_CTRL10
Pin 30	RPI	GND
Pin 31	RPI	GPIOR_133_CDI18
Pin 32	RPI	GPIOR_132_CDI19
Pin 33	RPI	GPIOR_135_CDI17
Pin 34	RPI	GND
Pin 35	RPI	GPIOR_138
Pin 36	RPI	GPIOR_136_CDI16
Pin 37	RPI	GPIOR_154
Pin 38	RPI	GPIOR_139
Pin 39	RPI	GND
Pin 40	RPI	GPIOR_155

Table 4: PMOD-1 I/O

Pin Number	Module Connector	Description
Pin 1	PMOD-1	GPIOB_RXN10
Pin 2	PMOD-1	GPIOB_RXP07
Pin 3	PMOD-1	GPIOB_RXP03
Pin 4	PMOD-1	GPIOB_RXN02
Pin 5	PMOD-1	GND
Pin 6	PMOD-1	3V3
Pin 7	PMOD-1	GPIOB_RXP10
Pin 8	PMOD-1	GPIOB_RXN07
Pin 9	PMOD-1	GPIOB_RXN03
Pin 10	PMOD-1	GPIOB_RXP02
Pin 11	PMOD-1	GND
Pin 12	PMOD-1	3V3

Table 5: PMOD-2 I/O

Pin Number	Module Connector	Description
Pin 1	PMOD-2	GPIOB_TXN09
Pin 2	PMOD-2	GPIOB_TXN06
Pin 3	PMOD-2	GPIOB_TXN04
Pin 4	PMOD-2	GPIOB_TXN02

Pin 5	PMOD-2	GND
Pin 6	PMOD-2	3V3
Pin 7	PMOD-2	GPIOB_TXP09
Pin 8	PMOD-2	GPIOB_TXP06
Pin 9	PMOD-2	GPIOB_TXP04
Pin 10	PMOD-2	GPIOB_TXP02
Pin 11	PMOD-2	GND
Pin 12	PMOD-2	3V3

2.7.2 I/O Banks

Table 6 describes the main attributes of the FPGA I/O banks, and indicates which peripherals are connected to each I/O bank.

Table 6: I/O Banks

	Bank	Connectivity	VCC_IO
FPGA	Bank 1A	Configuration	3.3V
FPGA	Bank 1B	ESP32-SPI/ ETH-RMII	3.3V
FPGA	Bank 1C	ETH-RMII	3.3V
FPGA	Bank 1D	ETH-RMII	3.3V
FPGA	Bank 1E	CBSEL/UART/PLL/BUTTON	3.3V
FPGA	Bank 3A	PI-HEADER/SD-CARD	3.3V
FPGA	Bank 3B	SD-CARD	3.3V
FPGA	Bank 3C	PI-HEADER	3.3V
FPGA	Bank 3D	PI-HEADER	3.3V
FPGA	Bank 3E	MISC/BUTTON/LEDS/PLL	3.3V
FPGA	Bank 4A	PMOD-1	3.3V
FPGA	Bank 4B	PMOD-2	3.3V

2.8 Power

2.8.1 Power Generation Overview

The Nyks TriPi Development Kit uses 5.0 V DC power input for generating the on-board supply voltages (1.2V,3.3V). Board can be powered from either USB port or RPI connector 5V pins.

Table 7: Power Generation

Voltage Supply Name	Voltage Value	Rated Current	Voltage Source
3V3	3.3 V	2A	5V
1V2	1.2 V	2A	5V

2.8.2 Voltage Supply Outputs

Table 8: Voltage Supply Inputs

Pin Name	Connector Pins	Voltage	Maximum Current
5V	2,4	5V	3A
3V3	Raspberry and PMOD header	3.3 V	2A

2.8.3 Power Consumption

Please note that the power consumption of any FPGA device strongly depends on the application (on the configured bitstream and I/O activity.)

Each Trion® FPGA has its own unique power profile. Therefore, Efinix provides a power estimator for each family member. These tools are Excel spreadsheets with macros. You can select the desired Trion® FPGA power estimator file, add information about your design, and the estimator calculates the projected power consumption. However, you need a license to obtain the Power Estimator Excel file from Efinix Support Center.

2.9 Clock Generation

Two on-board oscillators (33.33MHz and 50 MHz) are available to drive the T20Q144C3 PLL input pin and clock input.

Table 9: Module Clock Resources

Clock Source	PLL Input Pin Resources	PLL	External Clock
33.33 MHz oscillator	GPIOL_75_PLLIN1	PLL_TL0	External Clock 1
50 MHz oscillator	GPIOR_157_PLLIN	PLL_BR0	External Clock 1

2.10 Reset

The board reset signal (C_RESET) of the Nyks TriPi Development Kit is available on the button at the bottom left corner. Pushing the button pulls C_RESET low and resets the board.

2.11 LEDs

The board has 4 yellow user LEDs that are connected to I/O pins in T20Q144C3 banks 3E and 1E. By default, the T20Q144C3 I/O connected to these LEDs are set as active high. To turn a given LED on, pull the corresponding I/O signal high.

Table 10: Led Resources

Reference Designator	T20Q144C3 Pin Name	Active
LED1	GPIOL_71_NSTATUS	High
LED2	GPIOR_158_TEST_N	High
LED3	GPIOR_150_CBUS1	High
LED4	GPIOR_149_CBUS2	High

2.12 QSPI Flash Memory

The Nyks TriPi Development Kit has external QSPI flash memory. The QSPI flash memory has a density of 32 Mbits and a clock rate of up to 133 MHz. In active configuration mode, the FPGA is configured using the configuration bitstream in the SPI flash memory.

Table 11: Module QSPI Flash Memory

Signal Name	Direction	Description
SPI_SCLK	Input	Clock output to SPI flash memory.
SPI_MOSI	Input	Data output to SPI flash memory.
SPI_SS	Input	Active-low SPI flash memory chip select.
HOLD	Input	Active-low hold signal.
SPI_MISO	Output	Data input from SPI flash memory.

2.13 SD Card

The Nyks TriPi Development Kit includes a micro-SD card slot. SD card connects to GPIO pins in bank 3A and 3B. The micro-SD supports data rate of up-to 25 MB/s.

Table 12: Module SD-Card

Pin Name	Signal Name	T20Q144C3 Pin Name
1	DATA 2	NC
2	CD/DAT3	GPIOR_105_CDI24
3	CMD	GPIOR_104_CDI25
4	VDD	3V3
5	CLK	GPIOR_95_CDI26
6	VSS	GND
7	DAT0	GPIOR_94_CDI27
8	DAT1	NC
9	CD	GPIOR_88_CDI28
10	SHLD1	GND
11	SHLD2	GND
12	SHLD3	GND
13	SHLD4	GND

2.14 Ethernet

A 10/100 Mbit Ethernet PHY is available on the Nyks TriPi Development Kit, connected to PL via RMII interface. The RMII interface is connected directly to FPGA pins.

2.14.1 Ethernet PHY Type

Table 13 describes the equipped Ethernet PHY device type on the Nyks TriPi Development Kit.

Table 13: Ethernet PHY Type

PHY Type	Manufacturer	Type
RTL8201F-VB-CG	Realtek	10/100 Mbit

2.14.2 Signal Description

The RMII interface is connected to FPGA pins. The Ethernet connections are presented in Table 14. All listed pins are operated at 3.3V voltage.

Table 14: Signal Description

Signal Name	FPGA Pin
RMII RX 1	GPIOL_25_CLK1
RMII RX 0	GPIOL_24_CLK0
RMII_REF_CLK	GPIOL_31_CLK7_CDI6
RMII TX 1	GPIOL_40_CDI8
RMII TX 0	GPIOL_32_CTRL4_CDI7
RMII TXEN	GPIOL_41_CDI9
ETH MDC	GPIOL_46
RMII CRS DV	GPIOL_53_CDI10
ETH MDIO	GPIOL_54_CDI11
RXER	GPIOL_64
PHYRSTB	GPIOL_73_EXTFB1_CDI15

2.14.3 MDIO Address

The MDIO address assigned to the Ethernet PHY is 2. The MDIO interface is connected directly to FPGA pins.

2.14.4 PHY Configuration

The configuration of the Ethernet PHY is bootstrapped when the PHY is released with driver code. For extra information please contact KuanTek.

Table 15: PHY Configuration

Pin	Description
MODE	RMII mode: advertise all capabilities (10/100, half/full duplex)
PHYAD	MDIO address 0x2
RMII_REF_CLK	Output
LED0 (Pulled Down)	LINK
LED1 (Pulled Up)	ACT

3 Device Configuration

3.1 Configuration Signals

Table 16 describes the most important configuration pins and their location on the module connector.

Table 16: Configuration Signals

Signal Name	SoC Pin Type	FPA Pin	Description	Comment
TMS	TP & FPGA	TMS	Test Mode State pin	10 k pull-up to VREG_OUT_3.3V
TCK	TP & FPGA	TCK	Test Clock pin	10 k pull-up to VREG_OUT_3.3V
TDO	TP & FPGA	TDO	Test Data Out pin.	10 k pull-up to VREG_OUT_3.3V
TDI	TP & FPGA	TDI	Test Data In pin	10 k pull-up to VREG_OUT_3.3V

3.2 Boot Mode

The TriPi Development Kit supports three different configuration modes: SPI passive mode, SPI active mode, and JTAG mode. In SPI active and passive mode, you can choose which image to load from the SPI flash by pulling the CBSEL0 and CBSEL1 pins high or low.

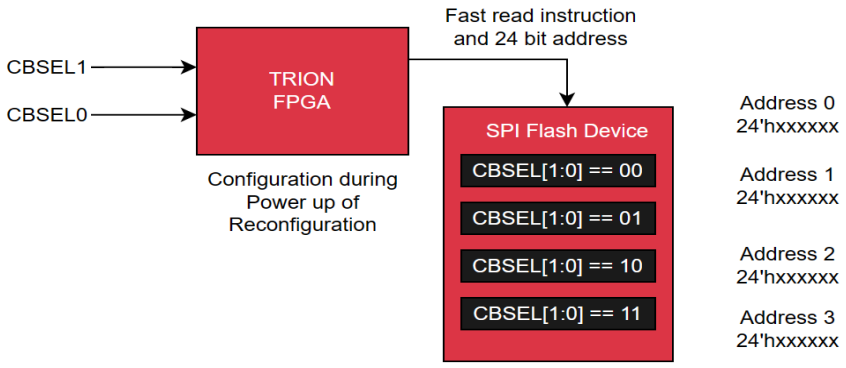

Figure 8: Module Boot Mode

3.3 QSPI Flash Programming via JTAG

The Efinix Efinity and SDK software offer QSPI flash programming support via JTAG. For more information, please refer to the Efinix Documentation and JTAG SPI Flash Loader IP.

4 Operating Conditions

4.1 Absolute Maximum Ratings

Table 17 indicates the absolute maximum ratings for the Nyks TriPi Development Kit. The values provided are for reference only.

Table 17: Absolute Maximum Ratings

Symbol	Description	Rating	Unit
5V	Supply voltage relative to GND	0 to 6	V
3.3V	I/O input voltage relative to GND	0 to 3,6	V
Temperature	Temperature range for commercial modules	0 to 85	◦C

4.2 Recommended Operating Conditions

Table 18 indicates the recommended operating conditions for the Nyks TriPi Development Kit. The values given are for reference only.

Table 18: Recommended Operating Conditions

Symbol	Description	Rating	Unit
5V	Supply voltage relative to GND	4.5 to 6	V
3.3V	I/O input voltage relative to GND	2,45 to 3,6	V
Temperature	Temperature range for commercial modules	0 to 85	◦C

5 Ordering and Support

5.1 Ordering

Please use the KuanTek online request/order form for ordering or requesting information:
https://www.kuantek.com.tr/contact

5.2 Support

Please follow the instructions on the KuanTek online support site: *https://www.kuantek.com.tr/contact*