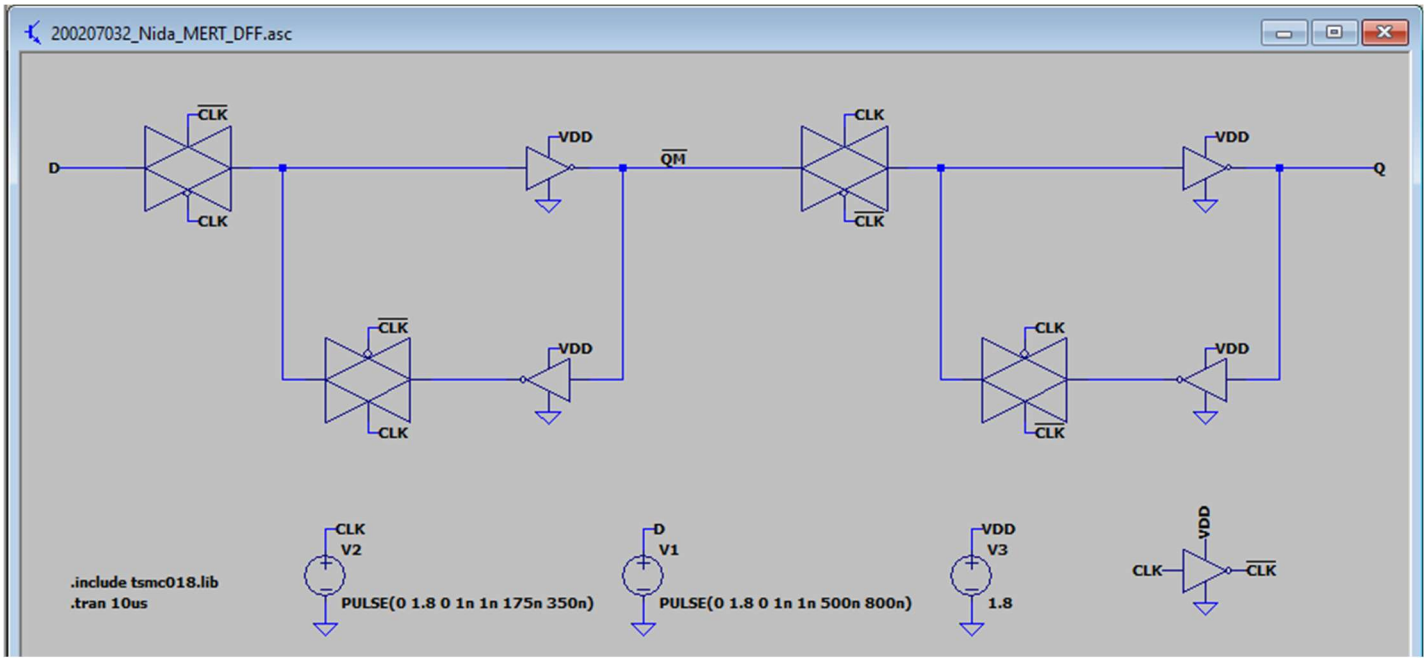
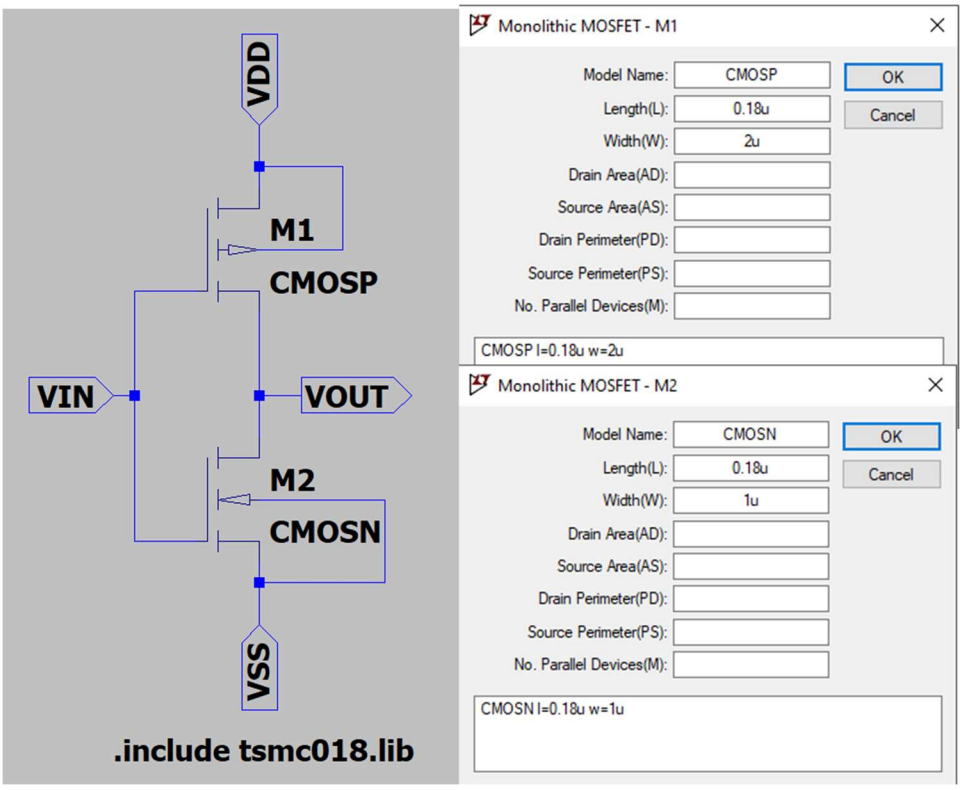
# Designing a Master-Slave D Flip-Flop in Ltspice



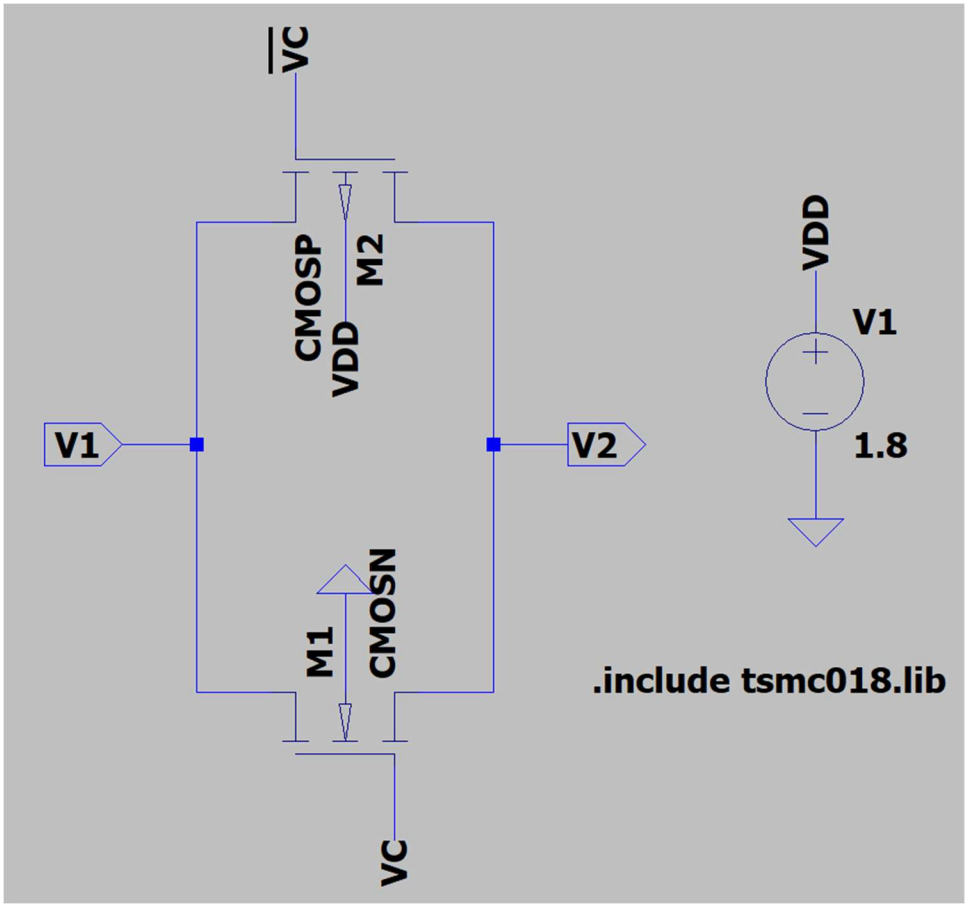

In this homework, we implement a Master-Slave D flip-flop (DFF) design and it operates as a positive-edge triggered flip-flop. This means that when the clock signal (CLK) transitions from low (0V) to high (1.8V), the input D data is captured and transferred to the output (Q).

## Inverter and Transmission Gate Design with Symbols



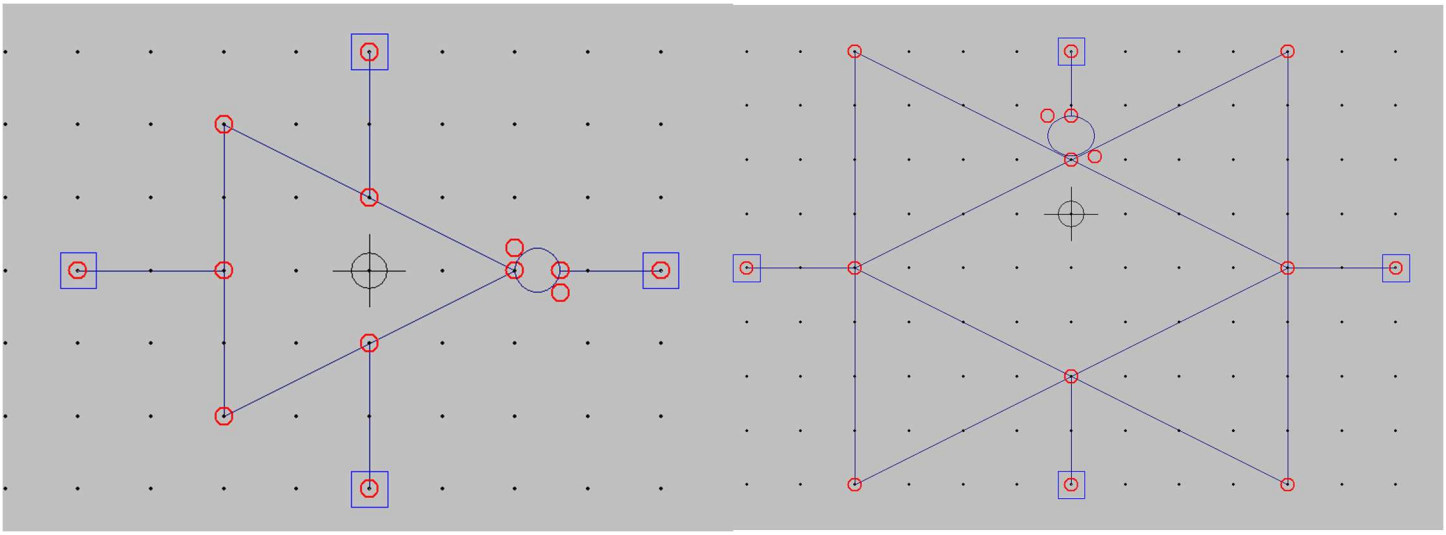

PMOS transistors are often two times wider than NMOS transistors because holes move more slowly than electrons so the transistor has to be wider in PMOS to deliver the same current.

For the inverter and transmission gate design, a length of 0.18µm was chosen. For the widths, PMOS4 was selected as 2µm, while NMOS4 was set to 1µm.

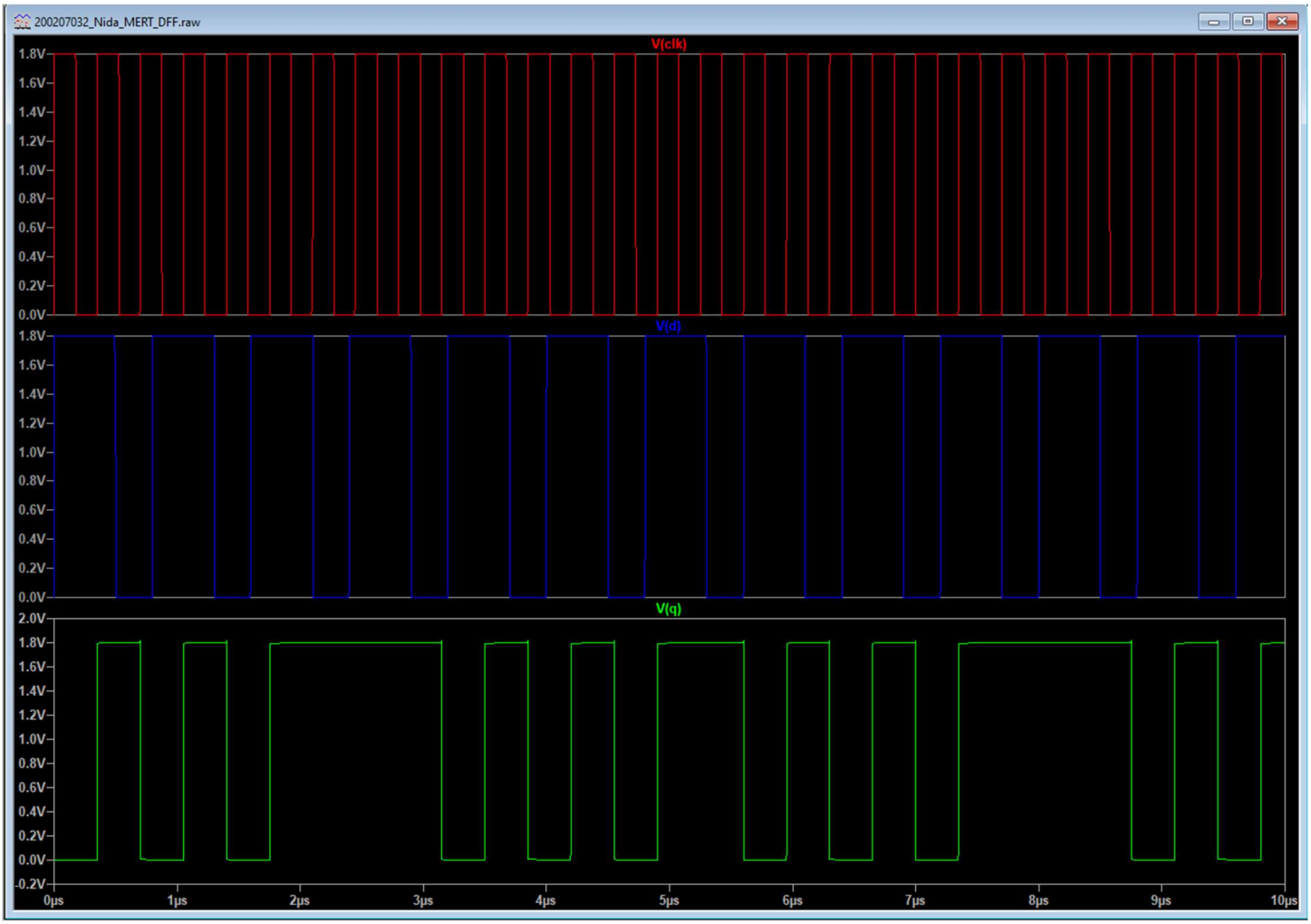



When an NMOS or PMOS transistor is used alone as a switch, it behaves as a pass transistor, but it does not efficiently pass both logic levels. In this design, by combining M1 (CMOSN) and M2 (CMOSP) in parallel, we create a transmission gate, which is controlled by the signal VC. When VC = 1, both transistors conduct, allowing the input V1 to pass through to the output V2. when VC = 0, both transistors turn off, isolating the output.

Here you can see the symbols of both inverter and transmission gate;



## Simulation Results of Positive Edge Trigerred Master-Slave D Flip-Flop Circuit




The simulation runs for 10µs. We generate a pulsed clock signal that starts at 0V, rises to 1.8V with a rise time of 1 nanosecond, stays at 1.8V for 175 nanoseconds, then falls back to 0V in 1 nanosecond, and repeats the cycle every 350 nanoseconds. Also, we generate a pulsed D input signal that starts at 0V, rises to 1.8V with a rise time of 1 nanosecond, stays at 1.8V for 500 nanoseconds, then falls back to 0V in 1 nanosecond, and repeats the cycle every 800 nanoseconds. We can see these parameters works as expected in the simulation results.

From the simulation results, it can be observed that the red signal represents the clock (CLK), the blue signal represents the input data (D), and the green signal represents the output data (Q). The Q output only changes on the rising edge of the clock, it captures the value of D at that moment, indicating that the flip-flop is working correctly.