A BCD Counter

In this laboratory assignment, we would like to construct and demonstrate a BCD counter. A generic 4-bit binary counter generates a sequence of numbers from 0 trough 15, and returns to zero afterwards. A BCD counter, on the other hand, runs up to 9 and then goes back to zero.

Pre-lab assignment

The file *counter4test.dig* is a simplified test bench for a 4-bit binary counter. The plot on the left side of Fig. 1 shows this circuit. The block labeled *cnt4* incorporates a 4-bit digital counter. The CLK signal is driven by a 1 Hz clock, so that the count increments every second, going through all hexadecimal digits, wrapping back to 0 after F.

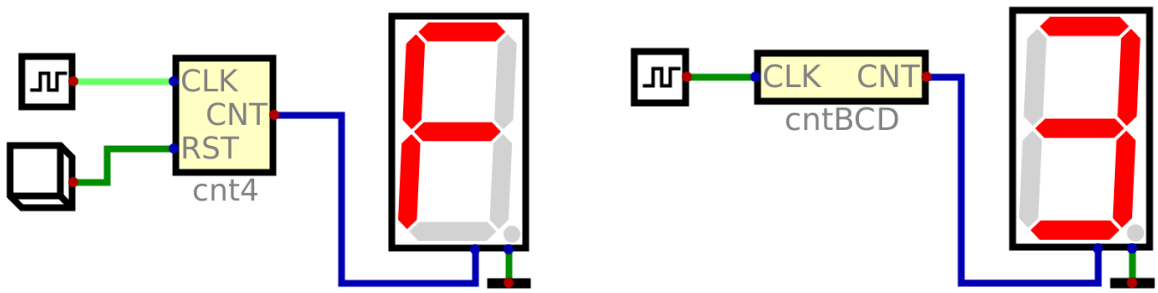

Fig. 1: Test bench for a binary counter (left), test bench for the circuit to be designed (right).

The counter circuit has an additional input labeled RST. Implied by the name, this input can be used to *reset* the counter, i.e., move it to zero. Run this circuit to observe the behavior of RST. Especially note when the counter gets reset with respect to the clock signal.

You are expected to modify *cnt4.dig* so that you get a BCD counter. The newly designed circuit, which can be named as *cntBCD.dig*, will use the RST input of *cnt4.dig* to make the count to roll to 0 after 9. Note that, *cntBCD.dig* does not have a RST input anymore; it has been used internally.

Design *cntBCD.dig*, test it, and upload it to SUcourse by the deadline.

On SUcourse, you are provided with the test bench *counter4test.dig*, and the counter *cnt4.dig*.

In-lab

During the laboratory session, you will be then asked to make a modification to the circuit to implement a different function.

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