CS 303 Logic and Digital System Design Assigned : 05/05/2023
Laboratory Assignment #04 Sessions : 15/05–18/05

A Tally Counter

You are provided with a up-down decimal counter in *cntDECud.dig*. Using two instances of this, and,

- two push buttons,
- two seven-segment hex displays (with the dot inputs grounded),
- a real time clock running at 100 Hz, and
- a 1-bit input to control the reset inputs of counters

design an up/down tally counter. The counter is expected to count the sequence ...-98-99-00-01-02-... in either direction, i.e., it should roll over 00 from 99, and vice versa. The expected behavior is demonstrated in *lab4_demo.mp4*.

Requirements:

- Full synchronous design: all FFs to be driven with the 100 Hz clock, and no clock gating.
- Full schematic design.

Submit your top level design as a single .dig file. Do not create any subcircuits (other than *cntDECud.dig*).

In-lab

During the laboratory session, you will be then asked to make a modification to the circuit.

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