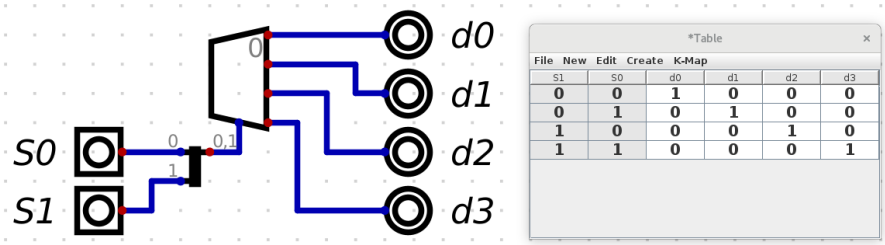
CS 303 Logic and Digital System Design Assigned : 13/04/2023
Homework #03 Due : 19/04/2023

The **Components** → **Plexers** menu of *Digital* provides multiplexers, demultiplexers and decoders. Using these,

1. Construct a 3-to-8 decoder using two 2-to-4 demultiplexers and an inverter,
2. Construct an 8-to-1 MUX using 2-to-1 mutiplexers (as many as needed),
3. Implement $F(x, y, z) = \sum(0, 1, 4, 5, 7)$ using a 3-to-8 decoder and the **minimum** number of 2-input OR/NOR gates,
4. Implement a full adder using two 4-to-1 MUXes.

Digital has an analysis tool (under **Analysis** → **Analysis**) that can be utilized to visualize the truth table of a circuit. For each design (in the above list), clearly get the truth table of the circuit, place it by the circuit schematic, and take a screenshot. To demonstrate, this has been done for *hw3_decoder_template.dig* (which is a template file for demonstrating the functionality of a 2-to-4 decoder, an is provided in SUcourse), and the result is shown in Fig. 1.



S1	S0	d0	d1	d2	d3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig. 1: The truth table of a 2-to-4 decoder generated by the Analysis tool of *Digital*.

Submit: A single .pdf file combining all of your four screenshots.

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