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الـــهـــيـــنة الملـــكـــية بـينبع
قـــطـــاع الـكـــــلـيات والـمـعـاهد

كـــلية ينبع الجـــــــامـــــعية
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قسم تقنية المعلومات والحاسب الآلي

PROJECT

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PRINCIPLES OF VLSI
CSE354

CMOS EXCESS-3-TO-BINARY CONVERTER

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FOR INSTRUCTOR USE ONLY				
Q. No.	CLOs	MAX MARK	MARKS OBTAINED	
	1.03, 2.01	15		
TOTAL MARKS		15		

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Table of Contents

1. Introduction

This report highlights the concept of excess-3 code and its representation, and how to convert an excess-3 code back to its original BCD form by implementing it as a circuit using Verilog. Excess-3 code or sometimes referred to as Tibitz code. The name Stibitz code refers to George Stibitz, who built a relay-based adding machine in 1937. [1]

1.2 Literature Review

1.2.1 Excess-3 Concept

It is a non-weighted code generated to express decimal numbers when you simply add decimal 3 to a number. It is also a self-complementary binary-coded decimal (BCD) code and numeral system. This means that the 1's complement of an excess-3 number is the excess-3 code for the 9's complement. [2]

1.2.2 Excess-3 Representation

Biased codes are a way to represent values with a balanced number of positive and negative numbers using a pre-specified number *N* as a biasing value. Biased codes (and Gray codes) are non-weighted codes. In excess-3 code, numbers are represented as decimal digits, and each digit is represented by four bits as the digit value plus 3 (the "excess" amount). For example:

Decimal digit 5:

BCD: 0 1 0 1 (+ 0 0 1 1) >>> Excess-3: 1 0 0 0

To convert an Excess-3 code back to its original BCD form, we subtract 3 from it. For example:

Excess-3 code: 1 0 0 0

When 1 0 0 0 – 0 0 1 1 >>> BCD: 0 1 0 1

1.2.3 Usage of Excess-3

It is particularly significant for arithmetic operations as it overcomes the shortcomings encountered while using the 8421 BCD code to add two decimal digits whose sum exceeds 9. This code is used in some old computers as well as in cash registers and hand-held portable electronic calculators of the 1970s, among other uses. [3]

2. Description of Circuit (Excess-3 to binary converter)

2.1 Truth Table and K-map of a 4-bit input:

Truth Table:

Inputs				Outputs			
W	X	Y	Z	A	B	C	D
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

K-map for each output:

WX \ YZ	00	01	11	10
00	x	x	0	x
01	0	0	0	0
11	1	x	x	x
10	0	0	1	0

A= WX+WYZ

WX \ YZ	00	01	11	10
00	x	x	0	x
01	0	0	1	0
11	0	x	x	x
10	1	1	0	1

B= X'Y'+XYZ+X'Z'

WX \ YZ	00	01	11	10
00	x	x	0	x
01	0	1	0	1
11	0	x	x	x
10	0	1	0	1

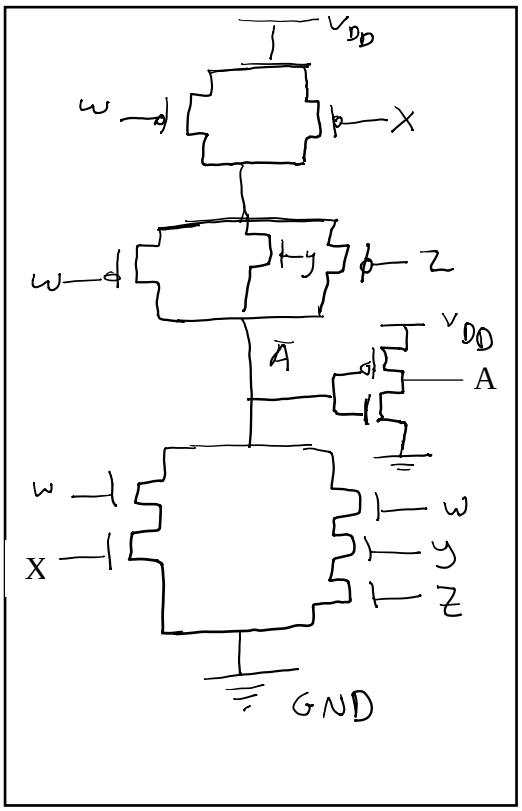
C= Y'Z + YZ' or Y XOR Z

WX \ YZ	00	01	11	10
00	x	x	0	x
01	1	0	0	1
11	1	x	x	x
10	1	0	0	1

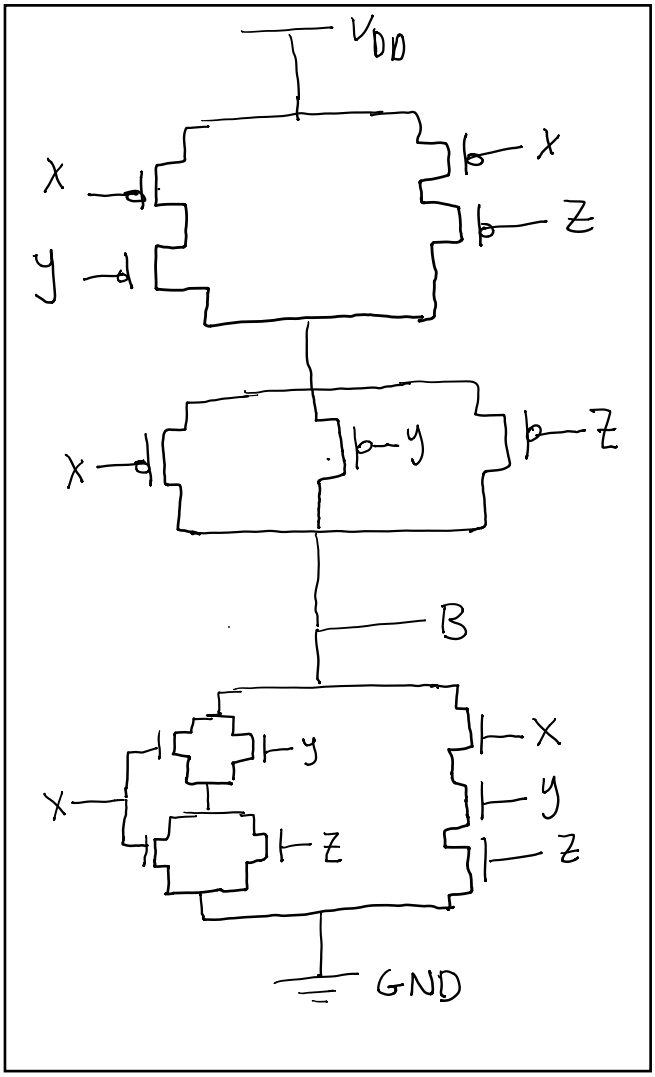
D= Z'

2.2 CMOS Circuit Diagram

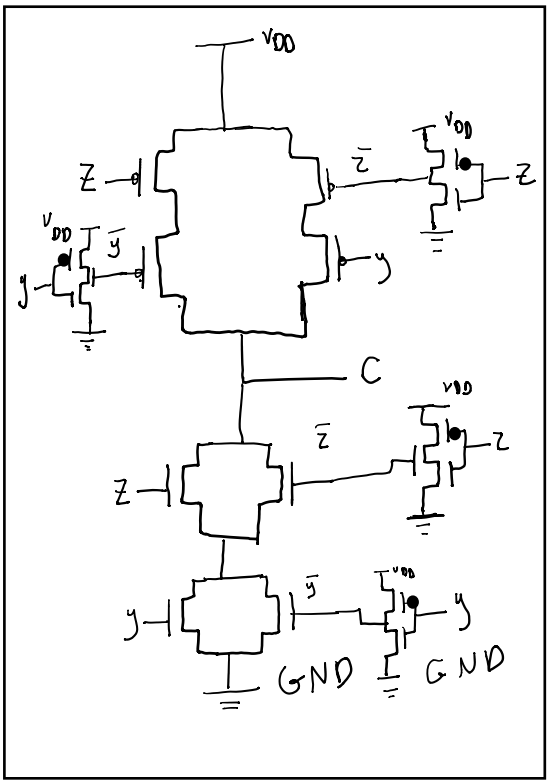
1. A = WX+WYZ



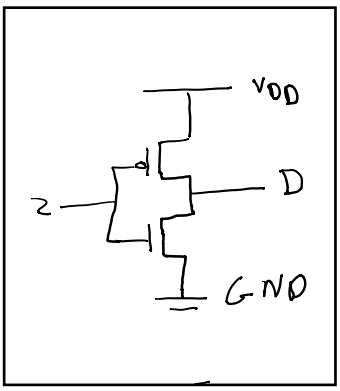
2. B = X'Y'+X'Z'+XYZ
=(X'Y'+X'Z')(X'+Y'+Z')



3. C = Y'Z+YZ'



4. D = Z'



2.3 Verilog Code

Module1

```
module converter1 (W,X,Y,Z,A);
input W, X, Y, Z;
output A;
supply1 V;
supply0 G;
wire Ap0, Ap1,An0, An1, An2;
  pmos (Ap0, V, W), (Ap0, V, X), (Ap1, Ap0, W), (Ap1, Ap0, Y), (Ap1, Ap0, Z), (A, V,
Ap1);
  nmos (Ap1, An0, W), (An0, G, X), (Ap1, An1, W), (An1, An2, Y), (An2, G, Z), (A, G,
Ap1);
endmodule
```

Module2

```
module converter2 (X,Y,Z,B);
input X, Y, Z;
output B;
supply1 V;
supply0 G;
wire Bp0, Bp1, Bp2, Bn0, Bn1, Bn2;
pmos (Bp0,V, X), (Bp1,V, X), (Bp2, Bp0, Y), (Bp2, Bp1, Z), (B, Bp2, X), (B, Bp2,Y),
(B, Bp2, Z);
nmos (Bn0, B, X), (Bn1, Bn0, Y), (G, Bn1, Z), (Bn2, B, Y), ( G, Bn2, Z), (Bn2, B, X),
(G, Bn2, X);
endmodule
```

Module3

```
module converter3 (Y,Z,C);
input Y, Z;
output C;
supply1 V;
supply0 G;
wire Cp0, Cp1,Cno ;
  pmos (Cp0, V, Z), (Cp1, V, ~Z), (C, Cp0, ~Y), (C, Cp1, Y), ( ~Z, V, Z), (~Y, V, Y),
  (~Z, V, Z), (~Y, V, Y);
  nmos (Cn0, C, Z), (Cn0, C, ~Z), (G, ~Z, Z), (G, Cn0, Y), (G, Cn0, ~Y), (G, ~Y, Y),
  (G, ~Z, Z), (G, ~Y, Y);
endmodule
```

Module4

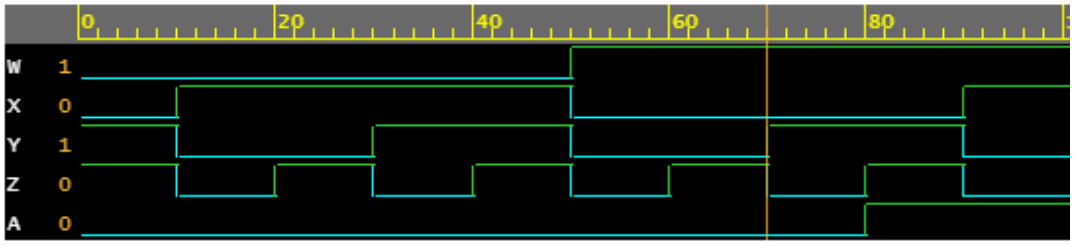
```
module converter4 (Z, D);
input Z;
output D;
supply1 V;
supply0 G;
  pmos (D, V, Z);
  nmos (G, D, Z);
endmodule
```

Testbench:

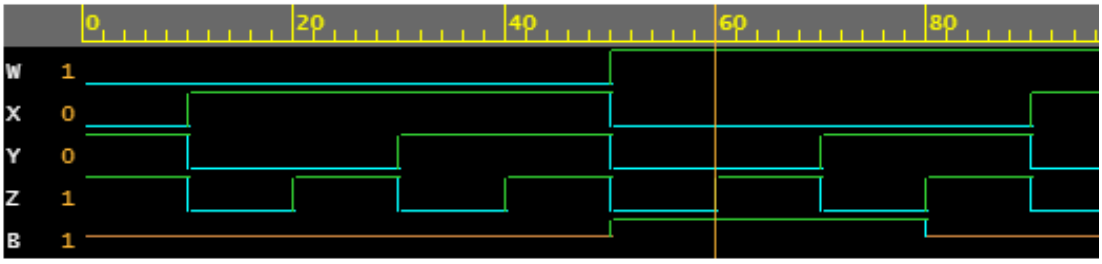
```
module testbench;
reg W, X, Y, Z;
wire A, B, C, D;
converter1 C1 (W,X,Y,Z,A);
converter2 C2 (X,Y,Z,B);
converter3 C3 (Y,Z,C);
converter4 C4 (Z,D);
initial
begin
  $dumpfile("dump.vcd");
  $dumpvars;
W =1'b0 ; X =1'b0 ; Y =1'b1 ; Z =1'b1 ;
#10;
 W =1'b0 ; X =1'b1 ; Y =1'b0 ; Z =1'b0;
#10;
  W =1'b0 ; X =1'b1 ; Y =1'b0 ; Z =1'b1;
#10;
  W =1'b0 ; X =1'b1 ; Y =1'b1 ; Z =1'b0;
#10;
  W =1'b0 ; X =1'b1 ; Y =1'b1 ; Z =1'b1;
#10 ;
  W =1'b1 ; X =1'b0 ; Y =1'b0 ; Z =1'b0 ;
#10;
  W =1'b1 ; X =1'b0 ; Y =1'b0 ; Z =1'b1;
#10 ;
  W =1'b1 ; X =1'b0 ; Y =1'b1 ; Z =1'b0;  #10;
  W =1'b1 ; X =1'b0 ; Y =1'b1 ; Z =1'b1;  #10 ;
  W =1'b1 ; X =1'b1 ; Y =1'b0 ; Z =1'b0;  #10;
end
initial
#250 $finish;
endmodule
```

3. Results

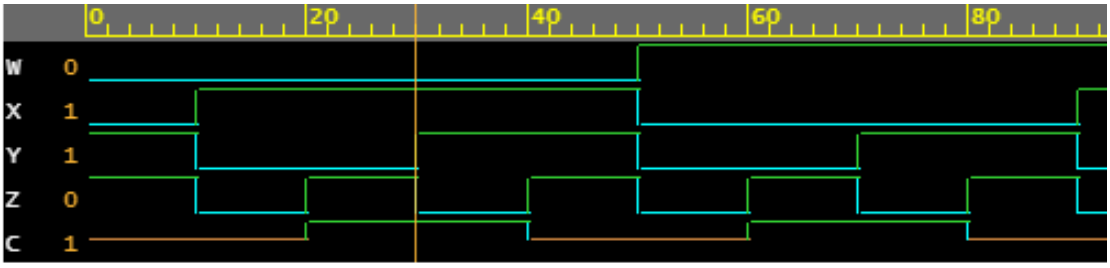
A: when input WXYZ (1010) >> output ABCD (**0**111)



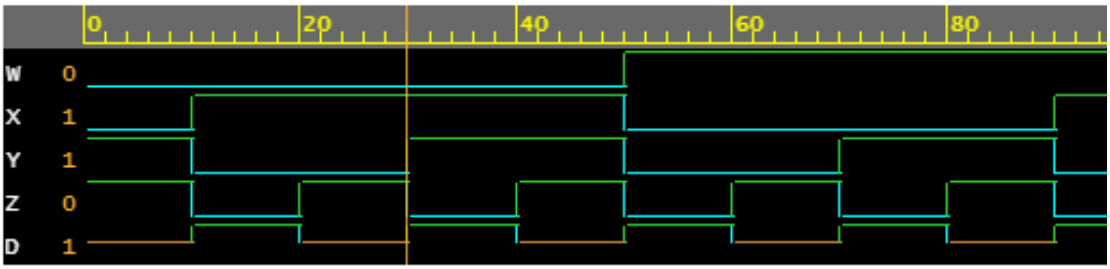
B: when input WXYZ (1001) >> output ABCD (0**1**10)



C: when input WXYZ (0110) >> output ABCD (00**1**1)



D: when input WXYZ (0110) >> output ABCD (001**1**)



4. Discussion and Comments

This report explains successful design of cmos excess-3-to-binary converter. We have implemented it as a circuit using Verilog to convert an excess-3 code back to its original BCD form. That can be done by simply deducting 3 or adding -3. As 4 bit excess-3 code start from 3 and end at 12 (input 0,1,2,13,14,15 not possible for obvious reason). For impossible inputs of 4 bit Excess-3 code we use output as Don’t care conditions.

References

[1]. “Excess-3 Code.” Wikipedia. 12 April. 2018. Web. Article. Reviewed on April 13. 2018. <https://en.wikipedia.org/wiki/Excess-3>

[2]. “Excess-3 code to BCD.” Quora. 31 May. 2017. Web. Article. Reviewed on April 13. 2018. <https://www.quora.com/How-do-I-convert-Excess-3-code-to-BCD-code>

[3]. Dinesh Thakur. “Excess-3 Code (XS3).” Ecomputer Notes. (n.d.). Web. Article. Reviewed on April 15. 2018. <http://ecomputernotes.com/digital-electronics/binary/excess-3>

[4]. “Binary-coded decimal.” Wikipedia. 30 March. 2018. Web. Article. Reviewed on April 15. 2018. <https://en.wikipedia.org/wiki/Binary-coded_decimal>