Ultra low power integer-N ADPLL

Master's thesis project - meeting 3

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Overview

For this week...

1. Estimation of loop filter logic power.
2. Criteria to push envelope versus state of art.
3. Ideal Virtuoso PLL setup with Verilog(-ams) models of components.

Digital loop filter power estimate.

Assumptions

— Arising from *paranoia* about digital loop filter power consumption (target < 10μW).

— Estimate equivalent number ($\mathrm{N_{NAND2}}$) of NAND2 gates for (a) 4x N-bit Baugh-Wooley array multipliers, (b) 3x N-bit Brent-Kung tree adders. Also, account for DFFs ($\mathrm{N_{DFF}}$) in 3x N-bit registers.

— Assume E_{op} = 1 fJ per NAND2 or DFF operation. Stian Østerhus' thesis from 2018 with 22-FDX found 139.37-239.42 aJ/operation for NAND, and 396.91-418.27 aJ/operation for DFF depending on with/without body bias with 0.35V supply (post layout).

— Activity factor α of loop filter logic is uncertain... In steady state (BB-PD feedback), loop filter input will change by ca. 1 LSB per cycle so I expect α is low.

$$\mathrm{P}_{logic} = \alpha(\mathrm{N_{NAND2}} + \mathrm{N_{DFF}})\mathrm{E}_{op} f_{clk} \tag{1}$$

Note: Only considering dynamic power here.

Digital loop filter power estimate.

Component-level specs

— Given 22-FDX yields ca. 5.5 MGates/mm^2, assume α = 0.1, f_{clk} = 16 MHz:

Datapath bits	Gates+DFFs	Area [μm^2]	Square side [μm]	Power [μW], α = 0.1
8	2652	521	22.8	4.24
9	3390	660	25.7	5.42
10	4213	815	28.5	6.74
11	5127	986	31.4	8.20
12	6126	1172	34.2	9.80
13	7216	1375	37.1	11.5
14	8391	1594	39.9	13.4
15	9657	1829	42.8	15.5
16	11008	2080	45.6	17.6

— Power in line with the naive 10μW goal. May require low supply V_{DD}, however.

— Logic under 50 μm x 50 μm. **Target whole PLL under 100 μm x 100 μm (0.01 mm^2??**

Pushing performance envelope.

State of art

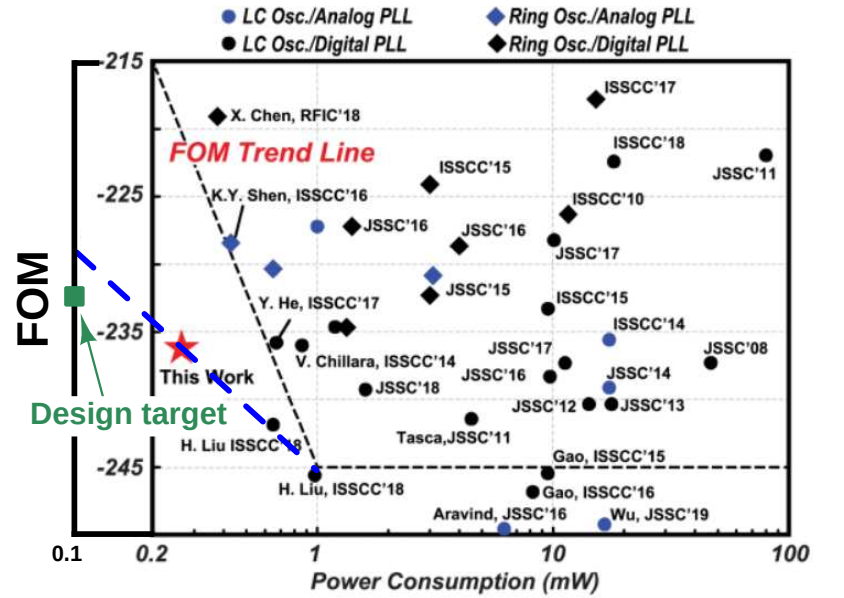
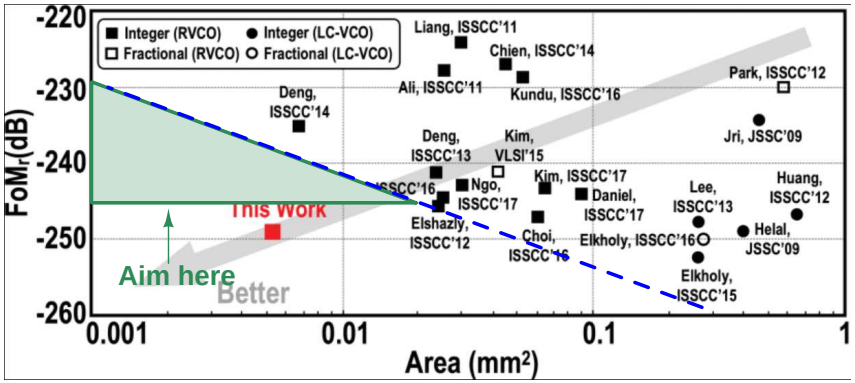


Figure from 2019 JSSC paper [1].

$$\mathrm{FOM}_{\mathrm{jitter}} = 10\log_{10}\left(\left(\frac{\sigma_{t_{jitter}}}{1\ \mathrm{s}}\right)^2 \cdot \frac{\mathrm{P}}{1\ \mathrm{mW}}\right) \qquad (2)$$

If CNR = 20 dBc @ 2.4GHz $\rightarrow$ $\sigma_{t_{jitter}}$ = 6.5 ps $\rightarrow$ FOM = -233 dB.



— Figure from 2018 JSSC paper [2].

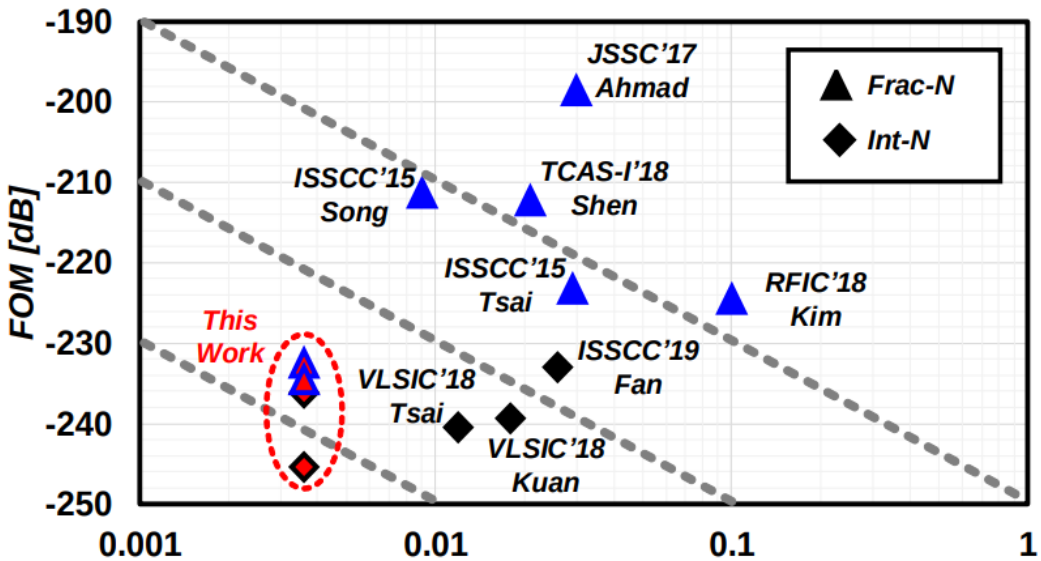
— FOM_r is with normalization to a 200 MHz reference oscillator. The PLL target for this project translates to FOM_r =-245 dB with a 16 MHz reference.

— **If phase noise can be maintaied with CNR $>$ 20 dBc, and PLL size $<$ 0.01 mm^2, design will be state of art.**

Pushing performance envelope.

Ultra-state of art for size (5 nm)

- This is from a sythesized PLL in TSMC 5nm FinFET [3], that *has* been fabricated. The paper is an early release from SSCL. Area is 0.0036 mm^2, or 50 μm x 72 μm.
- Targeting $FOM_{jitter} \approx$ -233 dB and < 0.01 mm^2 is fairly competitive with the 5nm design.
- Paper claims ring oscillator jitter degrades in sub-20nm regime, so 22-FDX may be very advantageous from an analog perspective.



Pushing performance envelope.

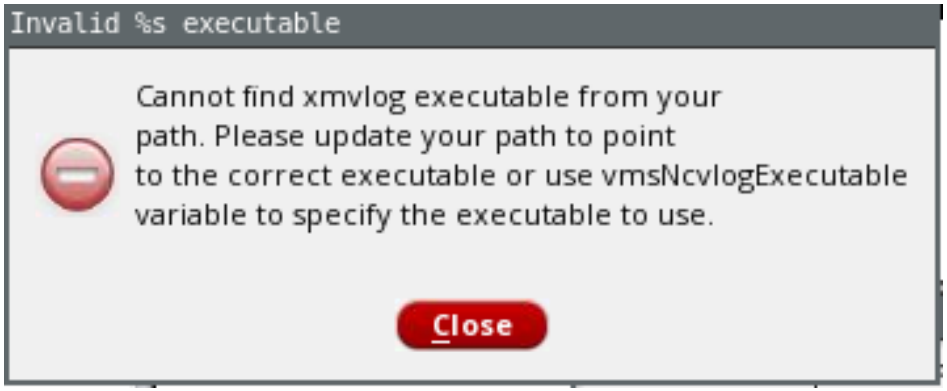
To be competitive versus current state of art the following design constraints are being imposed:

Parameter	Value	Unit
CNR	$\geq$ 16.5	dBc
FOM$_{\text{jitter}}$	$\leq$ -230	dB
Power	$\leq$ 100	μW
Area	$<$ 0.01	mm^2

Ideal PLL Testbench in Virtuoso

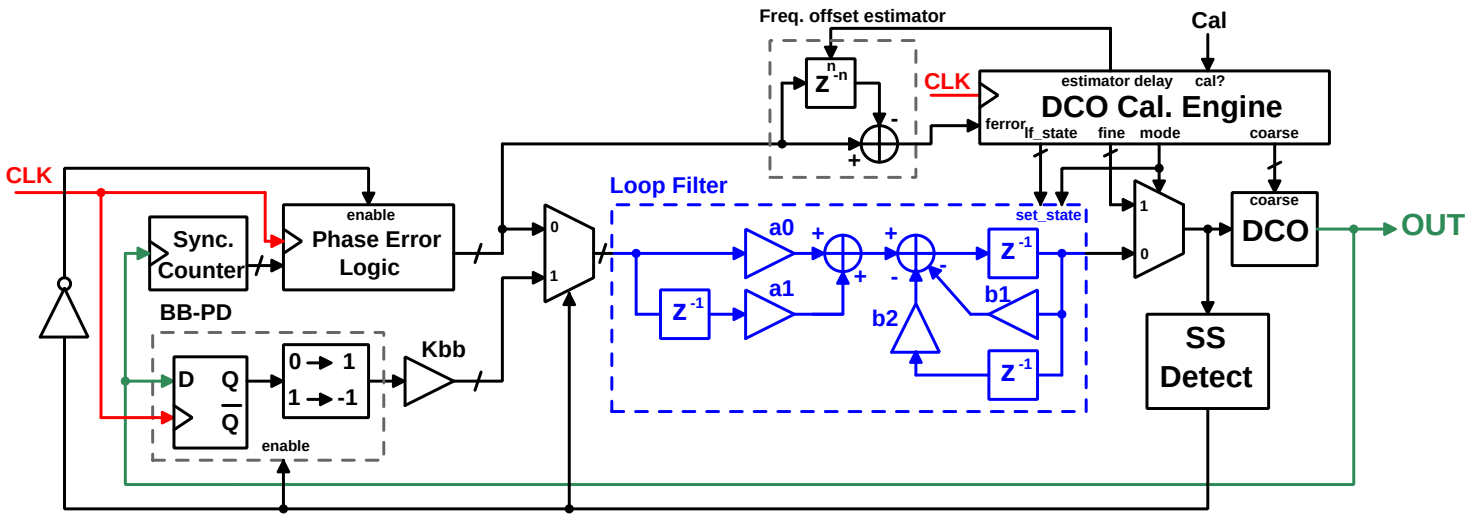
Verilog(-AMS) Models

- Wrote Verilog models for BB-PD, divider, loop filter. Wrote Verilog-AMS models for oscillator and TDC.
- Issue with Verilog-AMS: missing executable for xmvlog compiler?



Architecture

Block Diagram



Power Targets

DCO	Phase detector	Divider	Digital (LF)	Other	SUM
50 μW	10 μW	10 μW	10 μW	$<<$ 10 μW	$<$ 100 μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100	μW	minimize!
FSK BER	$\leq$ 1e-2		GFSK* with f_{dev}=$\pm$250 KHz
CNR	$>$ 16.5	dBc	Yields -233 dB FOM_{jitter}
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby
Lock Δf tolerance	10^5	Hz	
FOM_{jitter}	$\leq$ -230	dB	
Area	$<$ 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
TDC resolution	$\geq$ 155	steps/reference cycle
DCO gain K_{DCO}	10^4	Hz/LSB
DCO Phase noise	$<$ -80	dBc/Hz at $\Delta f = 10^6$ Hz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	$\leq$ 16	bits

Table: System-level specifications

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Schem. design: oscillator	LC DCO
12	16.3 - 22.3	Schem. design: divider	TSPC + pulse swallow or sync counter?
13	23.3 - 29.3	Schem. design: Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

References

[1] Liu, H., Shirane, A., Okada, K., Sun, Z., Huang, H., Deng, W., Siriburanon, T., Pang, J., Wang, Y., Wu, R. and Someya, T. (2019). A 265-μ W Fractional-*N* Digital PLL With Seamless Automatic Switching Sub-Sampling/Sampling Feedback Path and Duty-Cycled Frequency-Locked Loop in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 54(12), pp.3478-3492.

[2] Yang, S., Yin, J., Mak, P. and Martins, R. (2019). A 0.0056-mm2 -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs. IEEE Journal of Solid-State Circuits, 54(1), pp.88-98.

[3] Liu, B., Li, Z., Fu, X., Shirane, A., Kurosu, H., Nakane, Y., Masaki, S., Okada, K., Zhang, Y., Qiu, J., Huang, H., Sun, Z., Xu, D., Zhang, H., Wang, Y. and Pang, J. (2020). A Fully-Synthesizable Fractional-N Injection-Locked PLL for Digital Clocking with Triangle/Sawtooth Spread-Spectrum Modulation Capability in 5 nm CMOS. IEEE Solid-State Circuits Letters, pp.1-1.