Ultra low power integer-N ADPLL

Master's thesis project - meeting 1

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Timeline Tasks

Project description

— An ultra low power phase locked loop (PLL) frequency synthesizer shall be developed in 22nm FDSOI technology for application to 2.4 GHz ISM band wake up radio receivers. The project shall be undertaken with the following activities:

- Identification of an appropriate PLL architecture for ultra-low power consumption.
- Modeling of PLL to develop satisfactory specifications for PLL components.
- Transistor level implementation of design, including layout.
- Yield improvement/optimization if time allows.

Time plan

High level breakdown

— **Modeling/test bench creation** (2 weeks)
  - Finish high level modeling in Python to establish final component-level specifications.
  - Finish ideal PLL model in Virtuoso (Verilog modeling?), create set of test benches.

— **Schematic/RTL design** (8 weeks)
  - Schematic design for phase detector, oscillator, divider, calibration circuits
  - RTL/synthesis/place&route for digital loop filter and calibration circuits.

— **Layout** (4 weeks)
  - Layout for phase detector, oscillator divider, calibration circuits.

— **Flex weeks** (2 weeks)
  - One extra week for schematic design/layout respectively.

— **Report** (4 weeks)

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Schem. design: oscillator	LC DCO
12	16.3 - 22.3	Schem. design: divider	TSPC + pulse swallow or sync counter?
13	23.3 - 29.3	Schem. design: Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

State of the Art

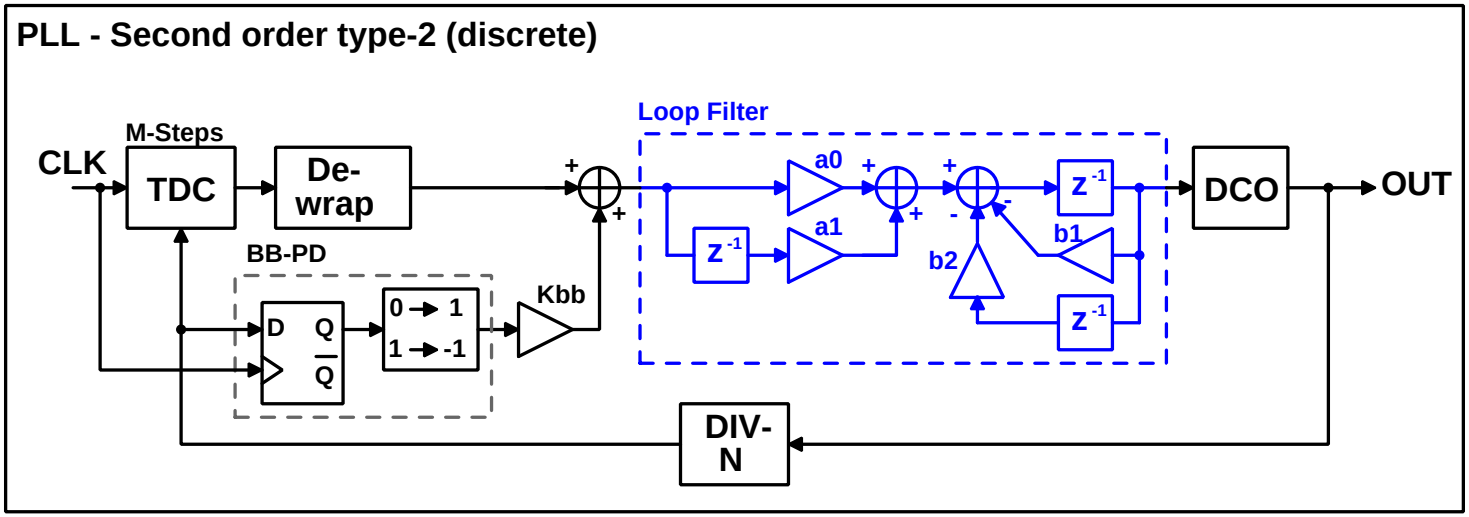
Sub 1-mW PLLS

Application is niche, so comparable PLLs hard to find. Sub 100μW is a reasonable target for low-power state of art in 2.4 GHz PLLs.

Type	P_{PLL} [μW]	P_{osc} [μW]	Freq [MHz]	PN@Δf [dBc/Hz]	t_{lock}* [μs]	Osc.	Ref Freq
Dig. Frac-N	650	304	2400	-110@0.5M	15/4	LC	26M
Ana. Int-N	680	510	2400	-110@1M	130/70	LC	1M
Ana. Int-N	128		500	-94@1M		Ring	31.25M
Ana. Int-N	570		800	-92.6@0.1M	200	LC	0.2M
Dig. Frac-N	250	173	2448		22/1	Ring	9M
Ana. Int-N	950		5500	-106@1M		IL-LC	

Architecture

Block Diagram



Power Targets

DCO	Phase detector	Divider	Digital (LF)	Other	SUM
50 μW	10 μW	10 μW	10 μW	$<<$ 10 μW	$<$ 100 μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100	μW	minimize!
FSK BER	$\leq$ 1e-2		2FSK with f_{dev}=$\pm$250 KHz
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby

Additionally: PLL output should support IQ sampling at LO frequency.