Ultra low power integer-N ADPLL

Master's thesis project - meeting 5

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Overview

For this week...

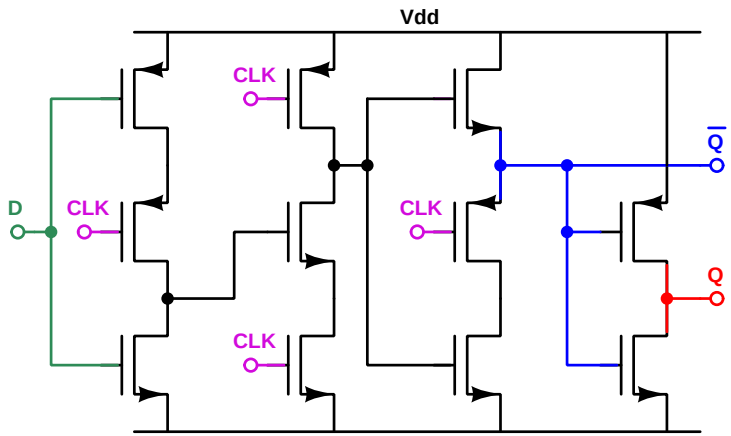
1. Some more with synchronous counter.
2. Bang bang phase detector.
3. New Github repo for presentations.

DFF Architectures

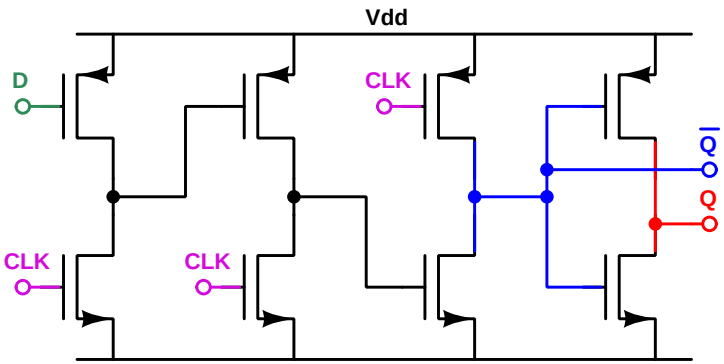
True single phase clock.

— True single phase clock (TSPC) advantageous for low power.

— If TSPC is too slow, enhanced TSPC (e-TSPC) is essentially the fastest possible DFF architecture in CMOS. However, power consumption is horrendous as it results in direct conduction paths from rail to rail on the order of 25% of the time if used as BB-PD.



(a) TSPC DFF

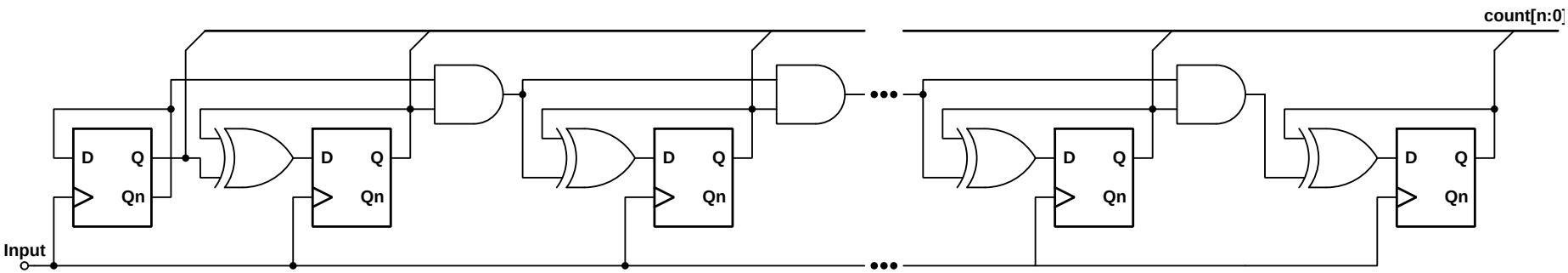


(b) e-TSPC DFF

Synchronous counter architecture

For real this time.

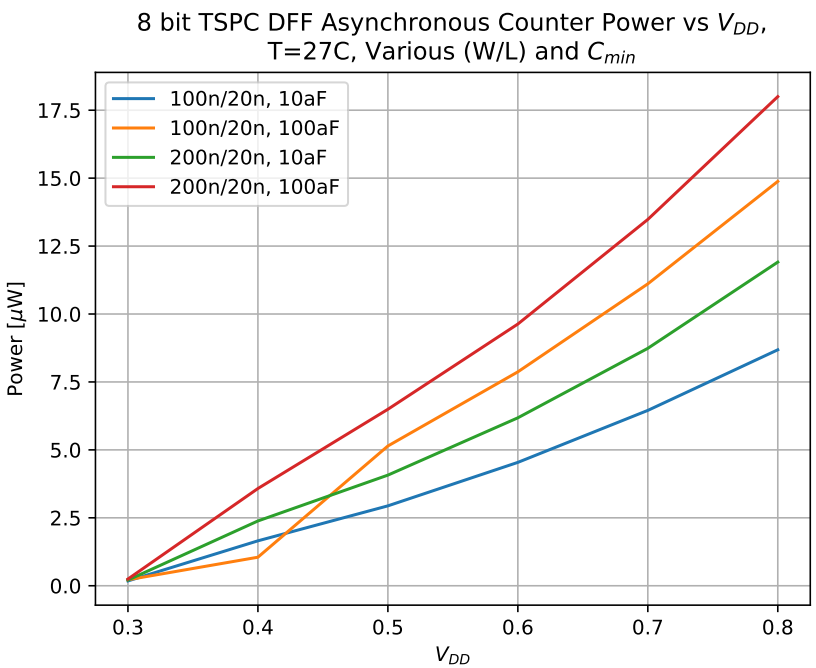
- Only tested ripple (asynchronous) counter last time.
- Implement T flip-flop with XOR gate, AND carry logic. Logic implemented as NAND2 only, with all FETS 200nm/20nm.
- Necessary to ensure that incorrect value isn't sampled, which is possible with asynchronous during ripple period. Penalty: 50 NAND2 gates, all FF's must be clocked every input cycle, i.e. more power than async.

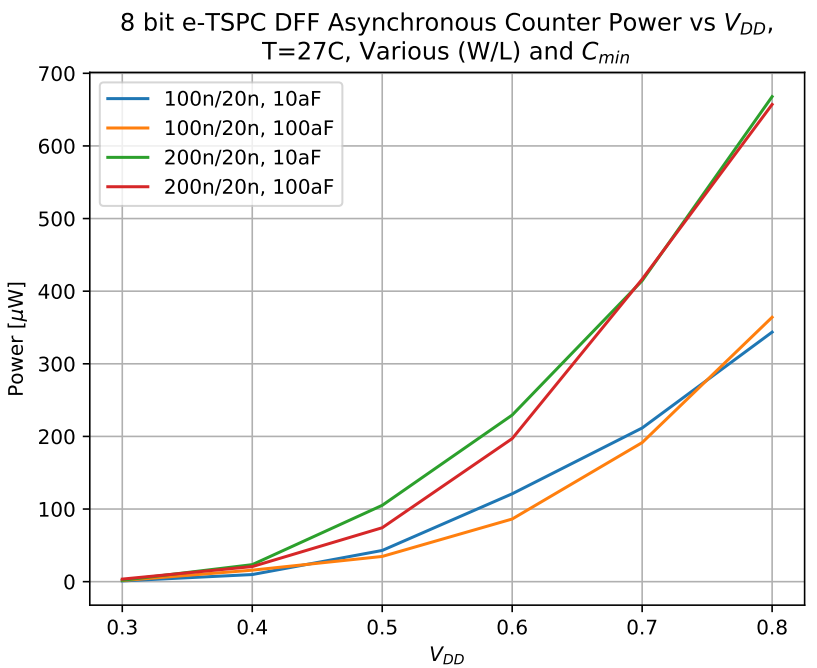


8 bit ripple async. counter power

Power consumption under swept conditions.

- Chain of 8 DFFs whose output clocks the next respective FF in the chain.
- Tested (W/L) = {100n/20, 200n/20}, C_{min} = {10, 100} aF, $V_{dd} \in [0.3, 0.8]$ V.
- TSPC has favorable power consumption. e-TSPC is terrible on the other hand, but is less sensitive to loading.

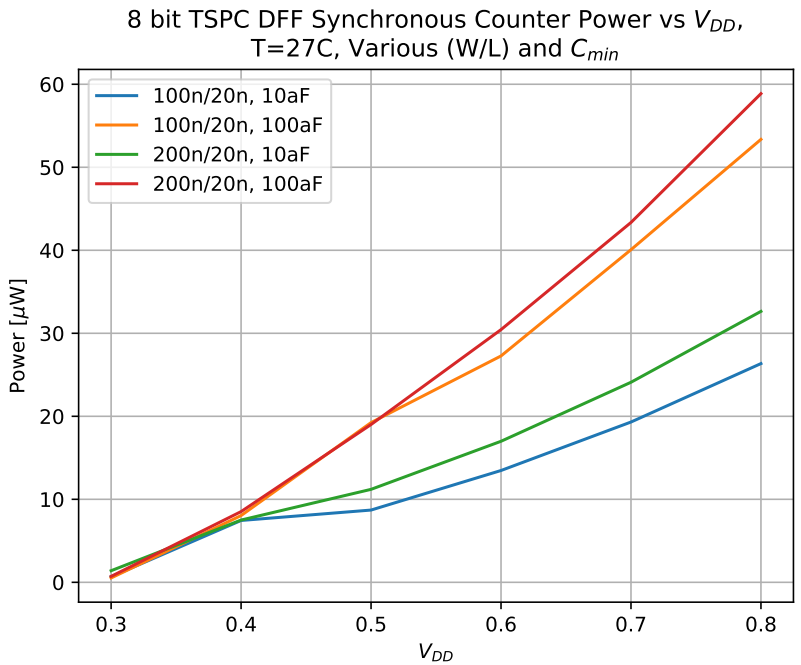




8 bit synchronous counter power

Power consumption under swept conditions.

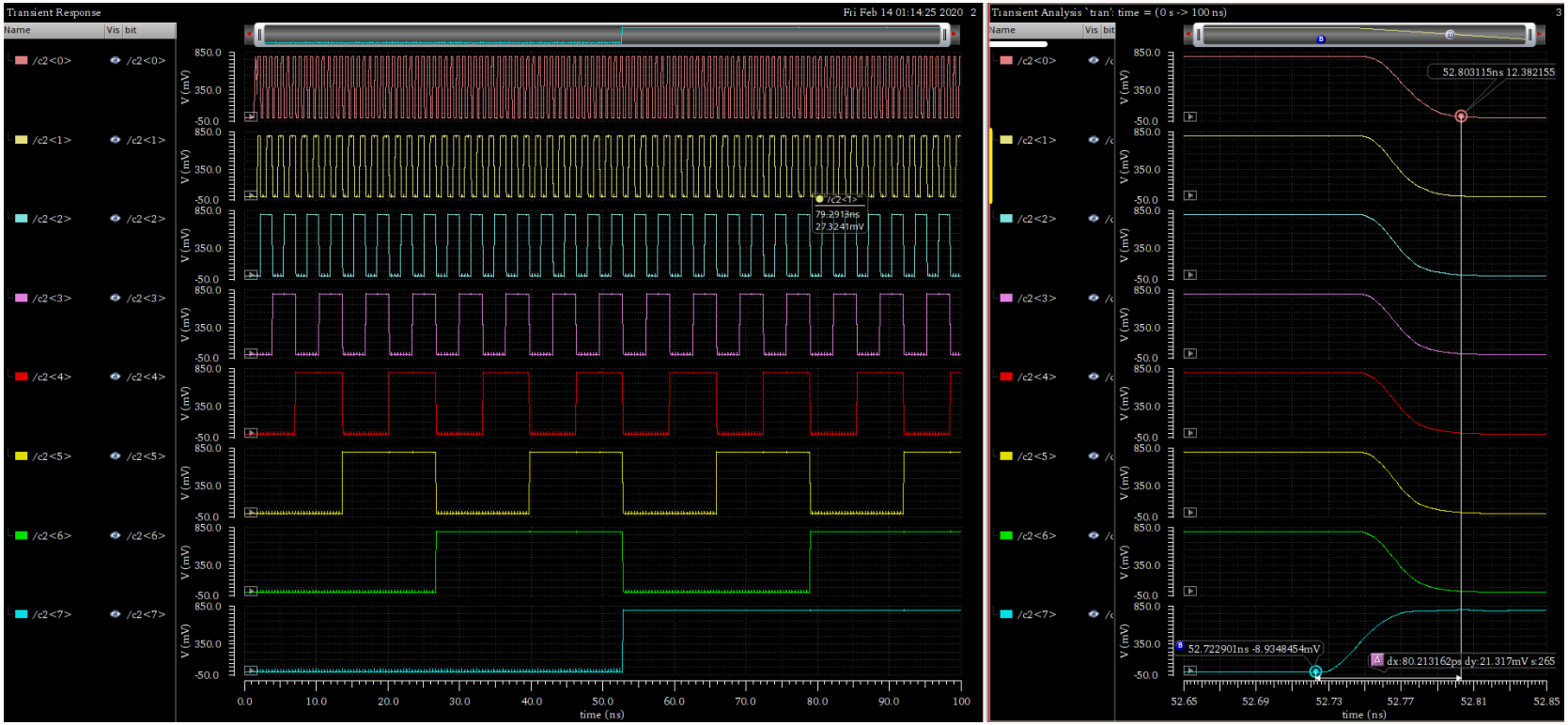
- Tested (W/L) = {100n/20, 200n/20}, C_{min} = {10, 100} aF, $V_{dd} \in [0.3, 0.8]$ V.
- Minimizing capacitance is most favorable for power. However, it is expected that 50 μW of counter power will only increase average power by $<<$ 1μW. So all circumstance tested here appear acceptable.



Synchronous counter output

800 mV Vdd

All edges occur within a time interval of 80ps. 54 μW power with 100 aF C_{min}

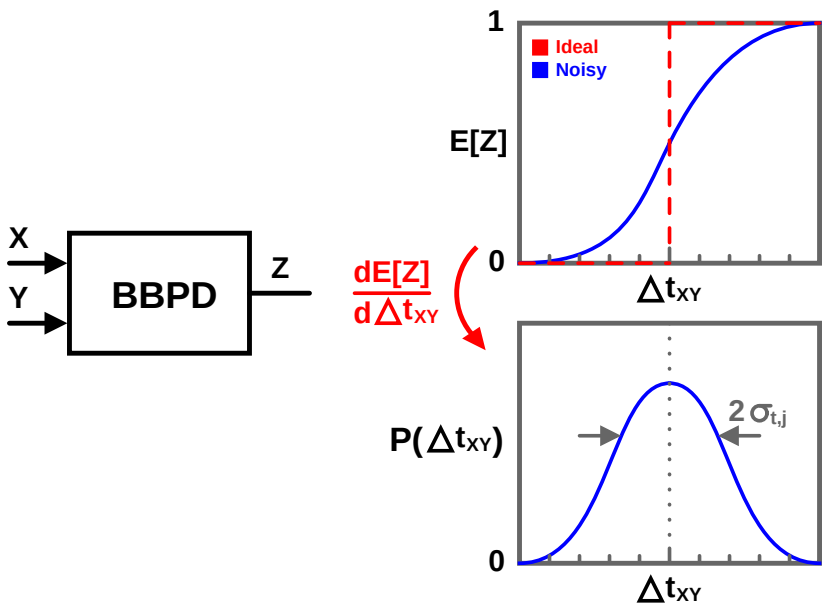


Noisy BB-PD Model.

Introduction of timing jitter to model.

— Uncorrelated / stochastic processes in a BB-PD result in the $\mathbb{E}[Z]$ with respect to input timing difference Δt_{xy} to deviate from an ideal step response.

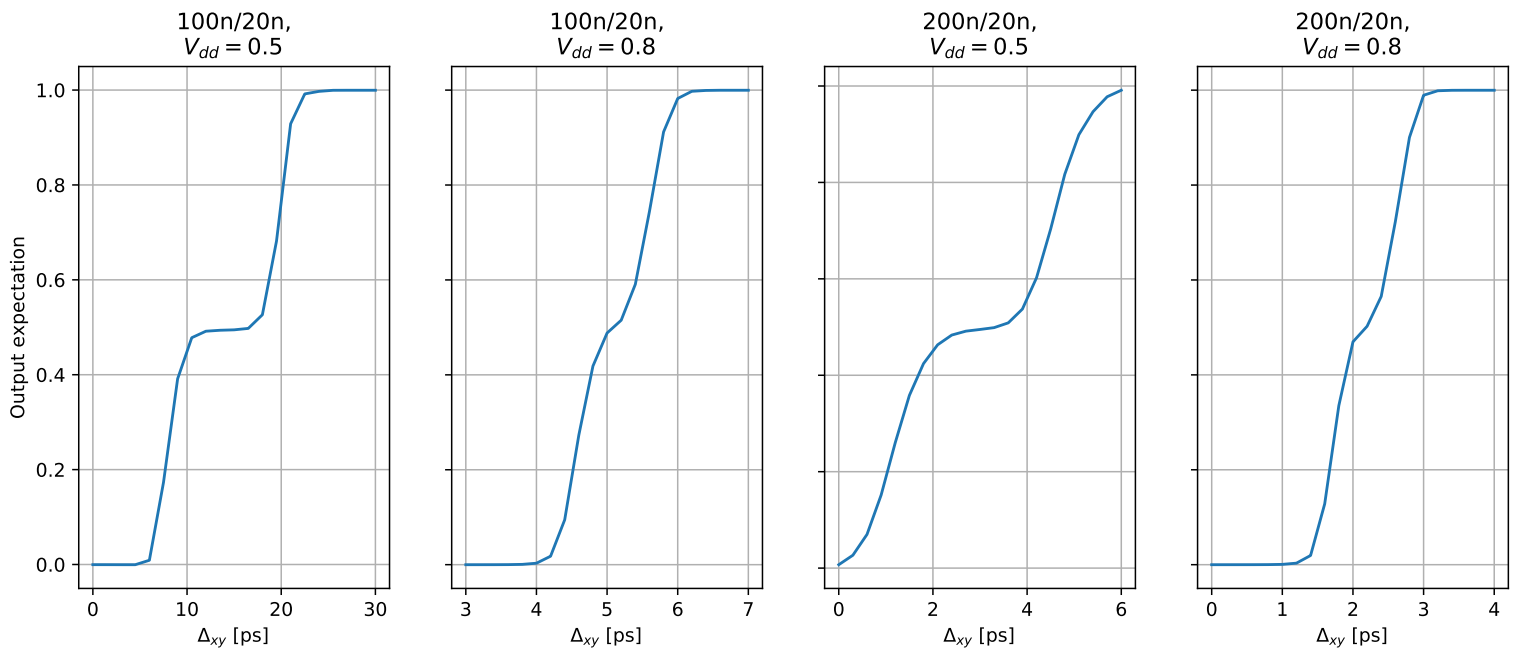
— $d\mathbb{E}[Z]/d\Delta t_{xy}$ results in a timing jitter probability distribution P(T=Δt_{xy}). The variance of this distribution on random jitter variable T, $\mathrm{Var}[T] = \sigma^2_{t,j}$, is the jitter power.



Simulation of BB-PD.

Simulation with TSPC DFF - Output expectation vs input delta.

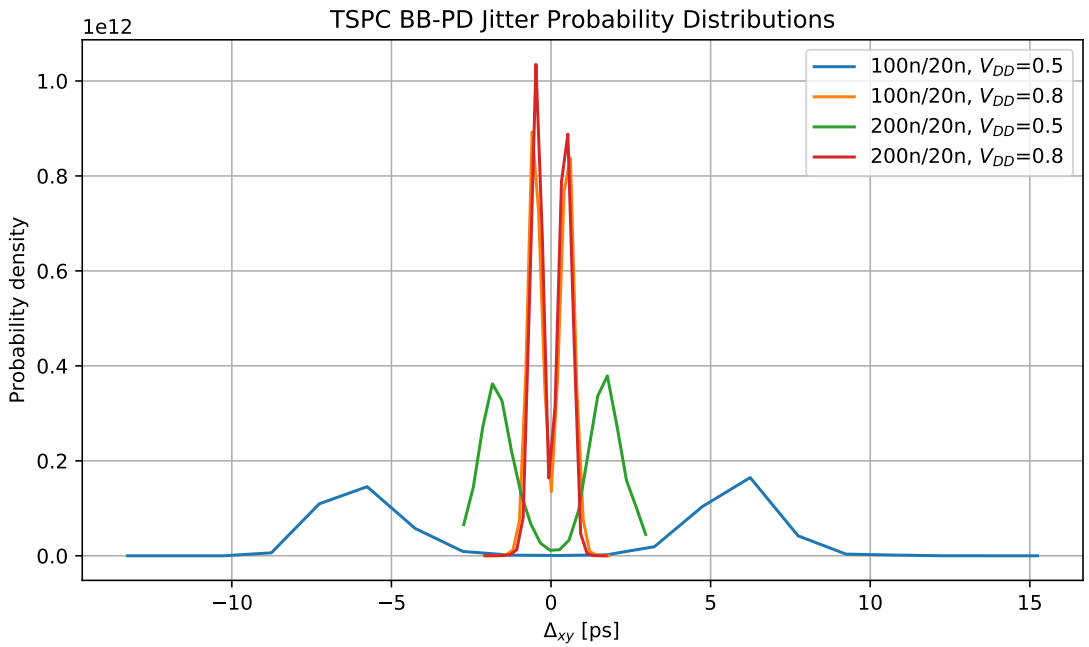
- Utilized TSPC DFF, with inverter buffers (FETs sized 200n/20n) for clock and data buffers.
- Sweep delay between inputs, calculating the expect value of the output for 100 bits. Transient noise simulated (up to 100 GHz), and the inital state of the FF is set to be high 50x and low 50x to include hysteresis effects.
- $V_{DD} \in \{0.5, 0.8\}$ V and (W/L) $\in$ {100n/20n, 200n/20n} tested. 100 aF added to every node.
- **Resulting CDFs of the input time delta versus output expectation are below.**



Simulation of BB-PD.

Simulation with TSPC DFF - Jitter distributions.

- Jitter PDFs are bimodal from hysteresis of DFF.
- Increasing (W/L) or V_{DD} both impact jitter favorably.
- **The jitter PDF (computed from the CDFs) of the input time delta versus output expectation are below. (Delays are removed)**



Simulation of BB-PD.

Tabularized results.

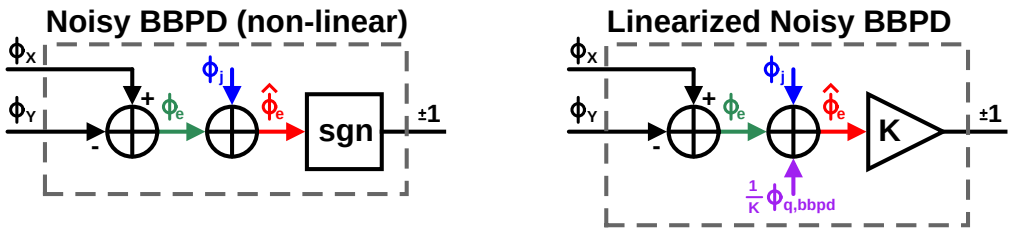
Requirements were $<$ 10 μW for the BB-PD, and its RMS jitter to be <12 ps for 17 dB CNR or < 8 ps for 20 dB CNR.

(W/L)	Supply [V]	RMS jitter [ps]	Delay [ps]	DFF [μW]	Buffer [μW]	Total Power [μW]
100n/20n	0.5	6.01	13.3	1.64	1.595	3.236
100n/20n	0.8	0.832	4.99	3.942	4.195	8.136
200n/20n	0.5	1.776	2.73	2.215	1.81	4.025
200n/20n	0.8	0.496	2.072	4.591	4.518	9.109

All four scenarios tested here pass the requirements. This will have to be re-evaluated post layout and with supply noise, however.

Noisy BB-PD Model. RECAP

Linearized noisy BB-PD model.



— BB-PD is non-linear, however with a stationary input ϕ_e with power $\sigma^2_{\phi_e}$, its gain can be linearized [1] as:

$$K = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\phi_e}} \tag{1}$$

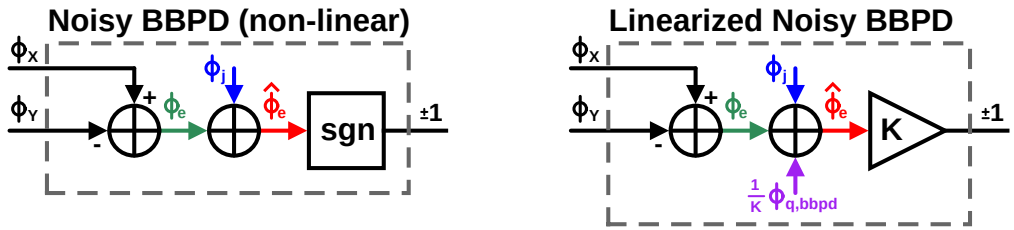
— The output has power $\sigma^2_{\phi_Z} = 1 = K^2\sigma^2_{\phi_e} + \sigma^2_{\phi_{q,bbpd}}$

— $\phi_{q,bbpd}$ is a error noise power inherent to the BB-PD.

$$\sigma^2_{\phi_{q,bbpd}} = 1 - \frac{2}{\pi} \tag{2}$$

Noisy BB-PD Model. RECAP

Linearized noisy BB-PD model (continued).



— Referring $\phi_{q,bbpd}$ to be before gain K, results in a total phase noise power for the BB-PD (assuming all noise sources uncorrelated):

$$\sigma^2_{\phi n,BBPD} = \left(\frac{\pi}{2} - 1\right)\sigma^2_{\phi e} + \frac{\pi}{2}\sigma^2_{\phi j} \tag{3}$$

— If the BB-PD is connected directly to oscillator output, $\sigma^2_{\phi e} = \sigma^2_{\phi n}$, i.e. the PLL output phase noise. The spectral density of the BB-PD phase noise is then:

$$S_{\phi n,BBPD} = \frac{\sigma^2_{\phi n,BBPD}}{f_{ref}} = \frac{\left(\frac{\pi}{2} - 1\right)\sigma^2_{\phi n} + \frac{\pi}{2}\sigma^2_{\phi j}}{f_{ref}} \tag{4}$$

BB-PD PLL Optimization. RECAP

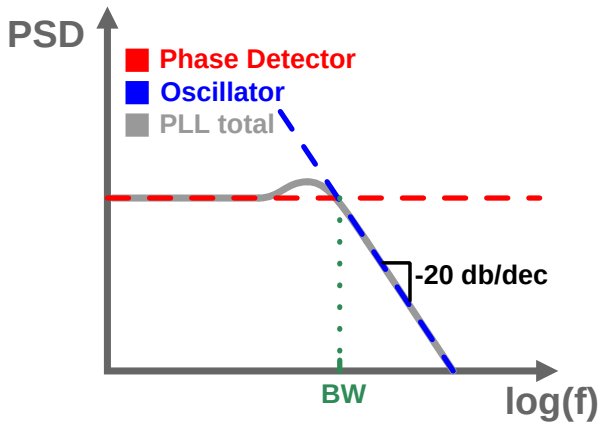
Approximate model for phase noise and optimal bandwidth.

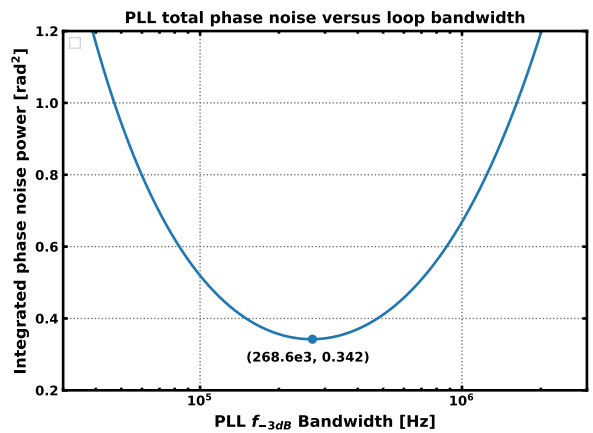
— It is observed that PLL phase noise spectrum is approximately Lorentzian (except for peaking and flicker noise components). Given BB-PD noise PSD of $S_{\phi n,BBPD}$, and an oscillator with noise PSD $S_{\phi n,osc}(\Delta f)$, the optimal bandwidth for minimum noise power is:

$$BW_{opt} = \sqrt{\frac{S_{\phi n,osc}(\Delta f)}{S_{\phi n,BBPD}}}\Delta f \tag{5}$$

— The total PLL output phase noise with optimal bandwidth is then:

$$\sigma^2_{\phi n,opt} = \pi\sqrt{\phi n,osc(\Delta f)S_{\phi n,BBPD}}\Delta f \tag{6}$$





BB-PD PLL Optimization. RECAP

BB-PD Jitter constraint with fixed BW and f_{ref} relationship.

— Using the findings for BB-PD noise PSD, assumption of Lorentzian spectrum, and constraint that BW = αf_{ref} (recommended $\alpha < 0.1$ [2], rule of thumb since ancient PLL days). Given oscillator center frequency f_c, BB-PD jitter is constrained:

$$\sigma_{t_j} \leq \frac{\sigma_{\Phi_n}}{2\pi f_c}\sqrt{\frac{2}{\pi}\left(\frac{1}{\pi\alpha} - \frac{\pi}{2} + 1\right)} = \frac{\sigma_{\Phi_n}}{2\pi f_c}\beta(\alpha) \tag{7}$$

— $\beta(\alpha = 0.1) = 1.28$, $\beta(\alpha = 0.05) = 1.92$.

— Using my PLL specifications (f_c = 2.448 GHz, CNR = $-\sigma_{\Phi_n}$ = 17 dB, $\alpha = 0.1$), $\sigma_{t,j} \leq 11.8$ **ps**

BB-PD optimal Jitter.

— With an unconstrained relationship for BW and f_{ref}, and the optimal bandwidth finding, it is determined that the optimal value of $\sigma_{t,j}$ for minimum phase noise is:

$$\sigma_{t_j,opt} = \frac{\sigma_{\Phi_n}}{2\pi f_c}\sqrt{\frac{2}{\pi}\left[\frac{\sigma_{\Phi_n}^4 f_{ref}}{\pi^2 S_{\phi n,osc}(\Delta f)\Delta f^2} - \left(\frac{\pi}{2} - 1\right)\sigma_{\Phi_n}^2\right]} \tag{8}$$

BB-PD PLL Optimization. RECAP

Optimal parameter selection.

— Setting the two jitter equations of the last side equal, it is found that optimal phase noise power is:

$$\sigma^2_{\Phi n,opt} = \frac{\pi S_{\phi n,osc}(\Delta f)\Delta f^2}{\alpha f_{ref}} \tag{9}$$

— The optimal reference frequency ($\sigma_{\Phi_n} = 2\pi f_c \sigma_{t_n}$ = CNR):

$$f_{ref} = \frac{\pi S_{\phi n,osc}(\Delta f)\Delta f^2}{\alpha \sigma^2_{\Phi n}} \tag{10}$$

— The optimal oscillator phase noise at offset Δf:

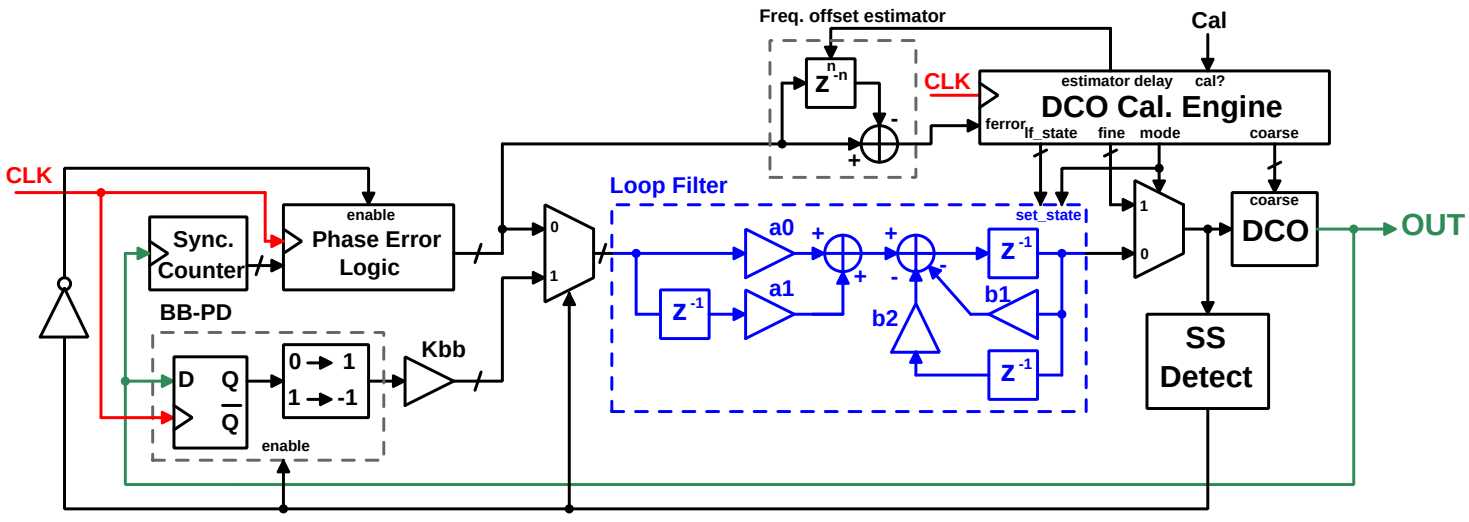
$$S_{\phi n,osc}(\Delta f) = \frac{\alpha f_{ref}\sigma^2_{\Phi n}}{\pi \Delta f^2} \tag{11}$$

— For CNR = 17 dB, $S_{\phi n,osc}(\Delta f = 1MHz)$ = -80 dBc/Hz, α = 0.1, the optimal f_{ref} = 15.7 MHz.

— For CNR = 20 dB, $S_{\phi n,osc}(\Delta f = 1MHz)$ = -80 dBc/Hz, α = 0.1, the optimal f_{ref} = 31.4 MHz.

Architecture

Block Diagram



Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Divider	Digital (LF)	Other	SUM
50 μW	10 μW	**N/A** ~~10 μW~~	10 μW	$\leq$ **5** ~~10~~ μW	$\leq$ **75** ~~100~~ μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ **75** ~~100~~ μW	μW	Minimize!
FSK BER	$\leq$ 1e-2		GFSK* with f_{dev}=$\pm$250 KHz
CNR	$>$ 20	dBc	Yields **-235** ~~-233~~ dB FOM_{jitter} ideally
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby, f_{error} $<$ **1 MHz**
Lock Δf tolerance	100	kHz	
FOM_{jitter}	$\leq$ -230	dB	**For state of art in size/power**
Area	$<$ 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
~~**TDC resolution**~~	~~$\geq$ 155~~	~~steps/reference cycle~~
DCO gain K_{DCO}	10^4	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	$<$ -80	dBc/Hz @ $\Delta f = 10^6$ Hz, f_c = 2.448 GHz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	$\leq$ 16	bits (power grows as $\mathcal{O}(n^2)$)
BB-PD jitter	$\leq$ 12	ps_{rms}

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Schem. design: oscillator	LC DCO
12	16.3 - 22.3	Schem. design: divider	TSPC + pulse swallow or sync counter?
13	23.3 - 29.3	Schem. design: Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

References

[1] H. Xu and A. A. Abidi, “Design Methodology for Phase-Locked Loops Using Binary (Bang-Bang) Phase Detectors,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 1637–1650, Jul. 2017.

[2] F. Gardner, “Charge-Pump Phase-Lock Loops,” IEEE Transactions on Communications, vol. 28, no. 11, pp. 1849–1858, Nov. 1980, doi: 10.1109/tcom.1980.1094619.