Ultra low power integer-N ADPLL

Master's thesis project - meeting 13

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Overview

For this week...

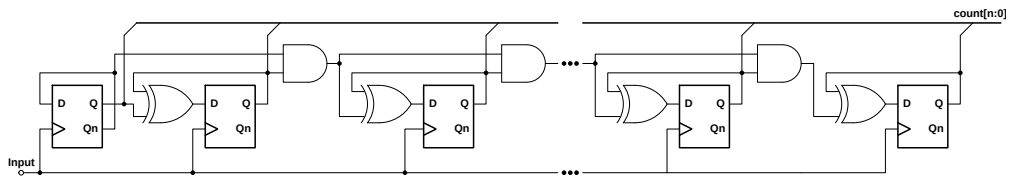
1. Calibration, control logic.
2. Phase detectors (BBPD, sync. counter).

Synchronous counter phase detector (SCPD).

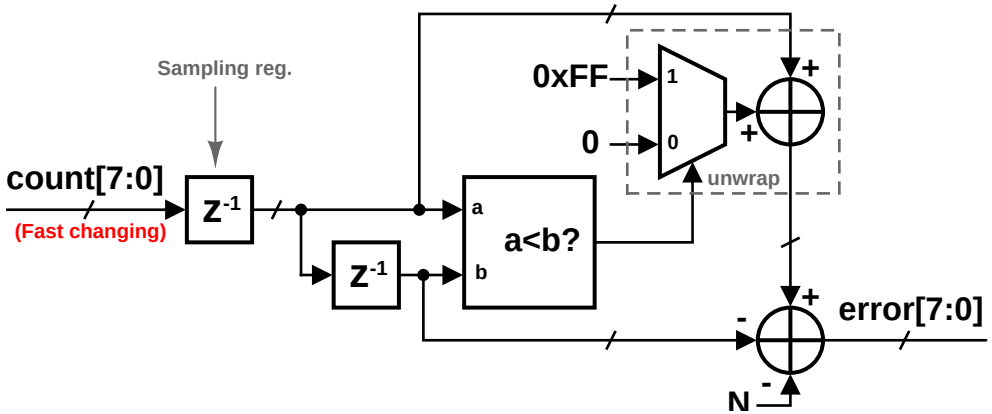
Implementation.

- Implemented completely with synthesized Verilog.
- Noise and power not crucial at all, only used for start up and calibration.
- Count is converted to phase error by taking Δ of count in one ref. cycle (with unwrapping)
- Low resolution, equiv. TDC steps = divider modulus N. Sufficient for start up.

Synchronous counter



Count to phase error decoder

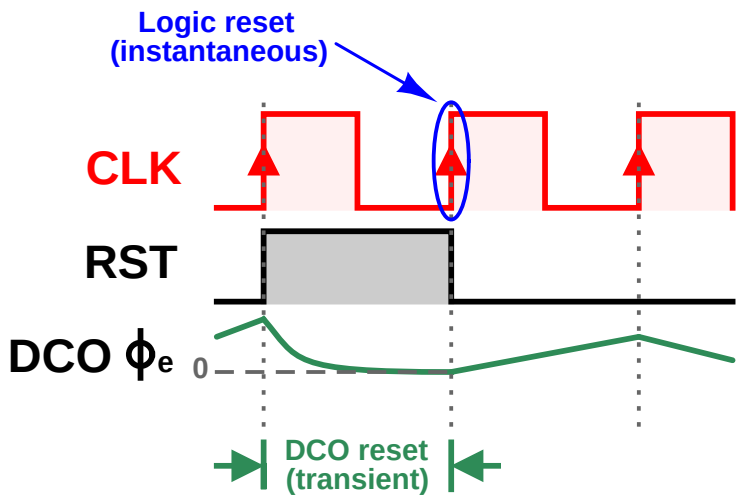


DCO reset scheme.

Implementation.

- Phase error zeroing reset implemented.
- Reset asserted (synchronously) for single cycle
  - DCO reset is at de-assertion of RST
  - Logic is reset at clock edge at end of RST assertion
- Allows for physical oscillator phase and digital phase error variable to be simulataneously set to zero.
  - Also BBPD doesn't work with BOTH phase/frequency error.
- Should enable faster lock (only initial unknown is frequency).
- Really only possible with the ring oscillator (LC can't start instantly)

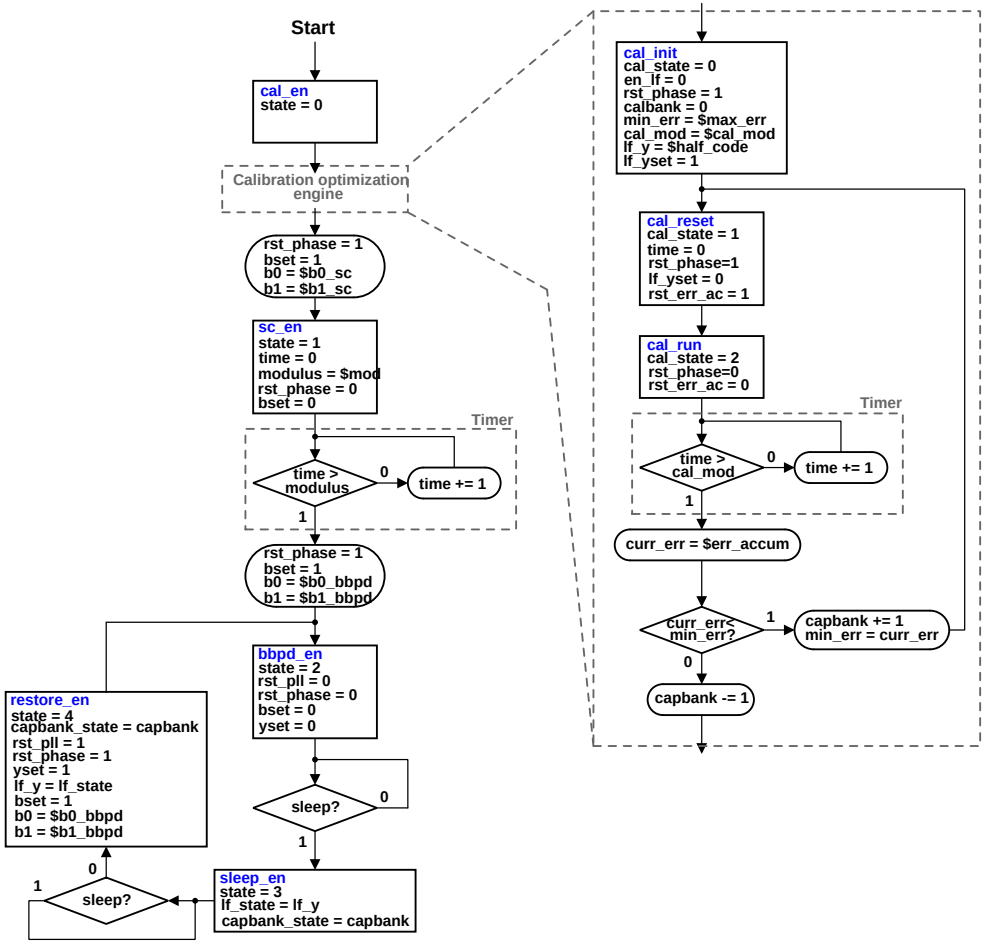
Reset scheme



PLL control state machine.

ASM chart

- Controller consists of 5 state FSM
  1. Calibration
  2. Run PLL, synchronous counter (timed start-up)
  3. **Run PLL, BBPD**
  4. Sleep (triggered externally)
  5. PLL restore (when sleep de-asserted)
- Calibration also has FSM, which implements a frequency-error minimizing algorithm
  - Starts at lowest capbank code, increments until argmin.
  - Frequency error by integrating error out over a number of cycles
  - Freq. resolution = f_{ref}/N_{cycles}
  - N_{cycles} = 4 yields 0.5% fractional resolution (vs cap bank resolution of 1.2%)



DCO control.

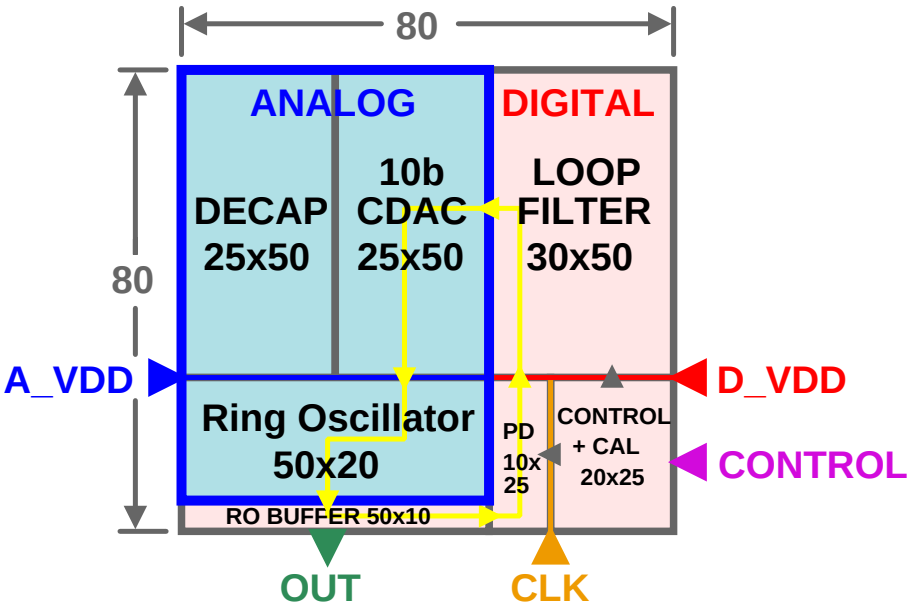
Continuity of fine/medium ranges.

- Originally planned to have PLL calibration state to tune medium DCO range.
- Decided it is easier to have both tuned simultaneously in the regular BBPD state.
  - Use 13 bit loop filter output (lf_out[12:0])
  - Fine range tapped off of lowest 10 bits (lf_out[9:0])
  - Medium range tapped off highest 3 bits (lf_out[12:10])
- Tuning range of fine/med ranges is 0.8 and 3.8 % respectively.
- MSB of fine range is 0.4%, LSB of medium range is 0.48%
  - Results in non-linearity during transient settling (LSB of medium range would ideally be 0.8%)
  - Steady state should be largely unaffected

Floor plan

Updated version

— **Original**

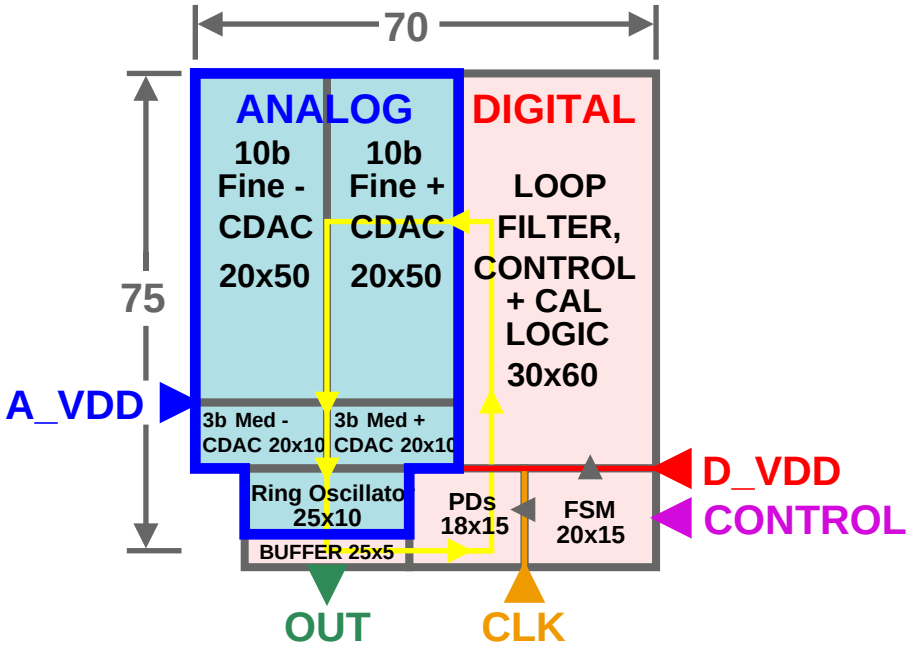


— **New**

— Merged majority of logic into one synthesized area.

— PLL control FSM and state retention registers in separate area (things that cannot be lost in sleep).

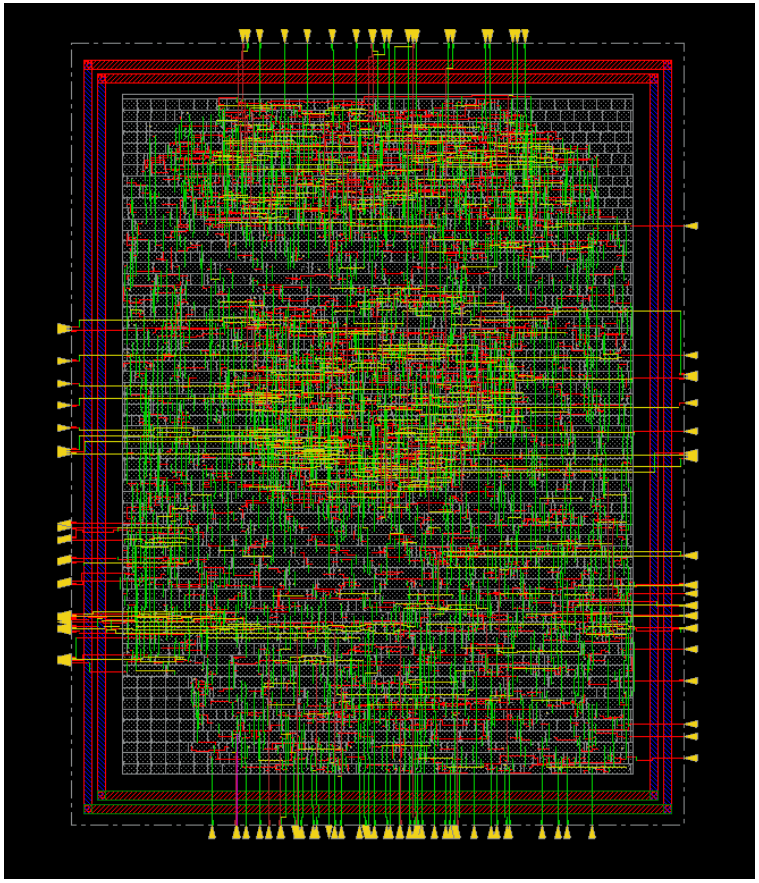
— During sleep, can cut power to bulk of logic to reduce leakage power.



LF/Calibration/control logic.

Synthesized.

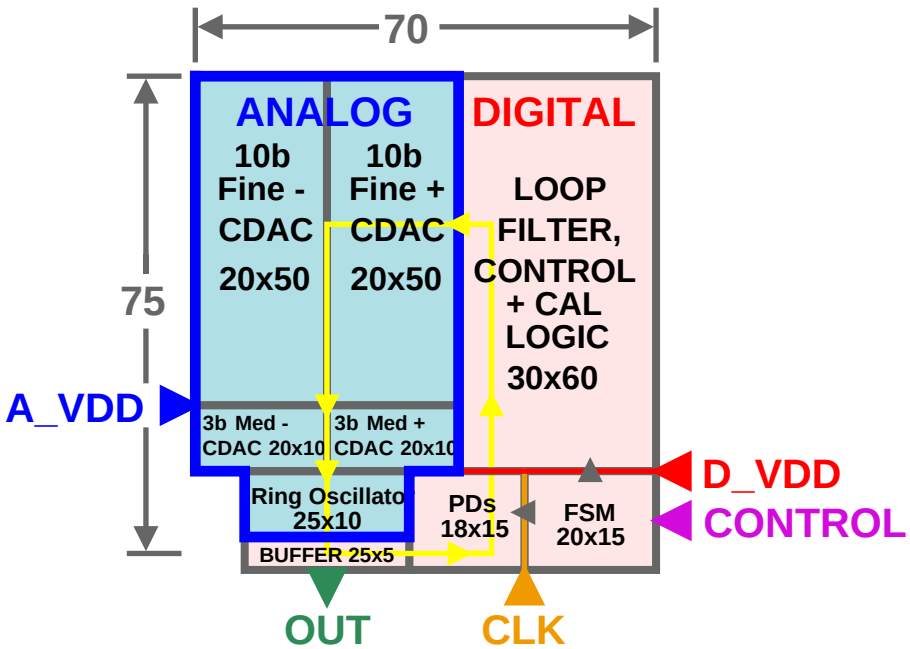
- Total area for logic = 716μm^2.
- Layout in 30 x 40 μm, ca. 50 % density.
- Power = 31.4 μW at 0.65V (82% leakage).
- Need to test at 0.5V, should be acceptable
- Need to replace pins (when fully decided)



PLL components

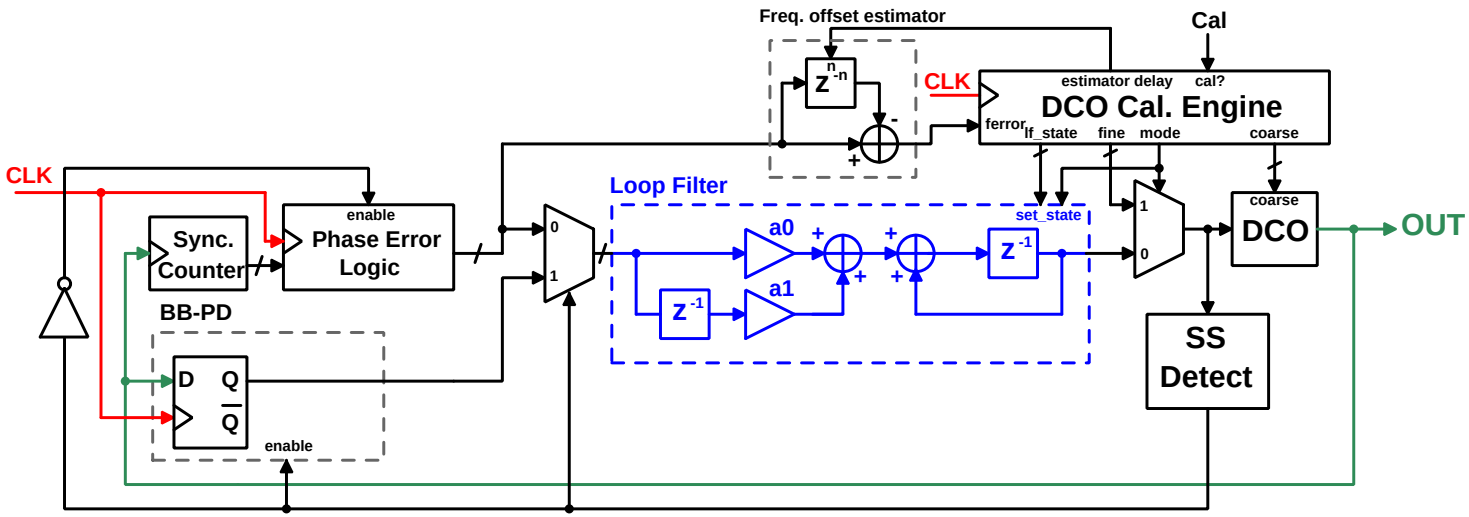
Loop filter

- Loop filter
- Control/calibration logic
  - Lock detect, gear switching
  - PVT cal
  - Estimate initial DCO control word
- Phase detectors
  - BBPD
  - Synchronous counter (7-8 bit)
  - Counter phase error decoder
- Level shifter (0.5V → 0.8V)
- CDACs
  - 5 bit coarse
  - 10 bit fine
- Ring oscillator
- RO buffer



Architecture

Block Diagram



Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Digital (LF)	Other	SUM
70 μW	10 μW	10 μW	**0** ~~≤ 5~~ μW	$\leq$ **90** ~~100~~ μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100 μW	μW	Minimize!
FSK BER	$\leq$ 1e-2		GFSK* with f_{dev}=$\pm$250 KHz
CNR	$>$ 20	dBc	Yields **-235** dB FOM_{jitter} ideally
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby, f_{error} $<$ **1 MHz**
Lock Δf tolerance	100	kHz	
FOM_{jitter}	$\leq$ -230	dB	**For state of art in size/power**
Area	$<$ 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
DCO gain K_{DCO}	10^4	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	$<$ -80	dBc/Hz @ $\Delta f = 10^6$ Hz, f_c = 2.448 GHz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	$\leq$ 16	bits (power grows as $\mathcal{O}(n^2)$)
BB-PD jitter	$\leq$ 12	ps_{rms}

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Layout: oscillator	
12	16.3 - 22.3	Layout: oscillator	
13	23.3 - 29.3	CDAC/Ring oscillator	
14	30.3 - 5.4	CDAC	
15	6.4 - 12.4	**(Easter)** Calibration/control logic	RTL, synth, PnR for calibration
16	13.4 - 19.4	Layout	Phase detectors
17	20.4 - 26.4	Layout/Integration	RO buffer, level shifter, whole PLL

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout/Integation	Finalization/system integration
19	4.5 - 10.5	Flex week (layout) OR yield improvement	Depending on progress
20	11.5 - 17.5	**Report writing**	
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

References

[1] L. Dai and R. Harjani, "Analysis and design of low-phase-noise ring oscillators," ISLPED'00: Proceedings of the 2000 International Symposium on Low Power Electronics and Design (Cat. No.00TH8514), Rapallo, Italy, 2000, pp. 289-294. doi: 10.1145/344166.344639

[2] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998.

[3] G. Jacquemod et al., "Study and reduction of variability in 28 nm FDSOI technology," 2015 International Workshop on CMOS Variability (VARI), Salvador, 2015, pp. 19-22.