Ultra low power integer-N ADPLL

Master's thesis project - meeting 9

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13 March 2020 (calendar week 11)

Overview

For this week...

1. Revised PVT scheme

Revised PVT tuning scheme.

MOS cap based solution.

— Originally planned for differentially attached APMOM caps. Still want differentially connected w/ symmetric configuration.

— Difficult to get small enough granularity (was seeing >10% per cap, needed ca. 2%)

— Now use MOS caps implemented with combination of minimum size RVT NMOS+PMOS, in symmetric configuration.

— Enabled through single T-gate.

Overall revised design.

Specs/performance.

— Now implementing only 6 stage differential at 816 MHz (eq. to quadrature at 2.448 GHz), due to challenge with meeting power, phase noise, frequency and tuning requirements.

— M1=M5 = 800n/80n, M2=M6=100n/80n, M3=M4= 400n/80n. All PVT bank caps 80n/20n.

— Power = 57.5 μW at 816 MHz (200 aF node cap, 6x PVT caps), FOM = -162 dB.
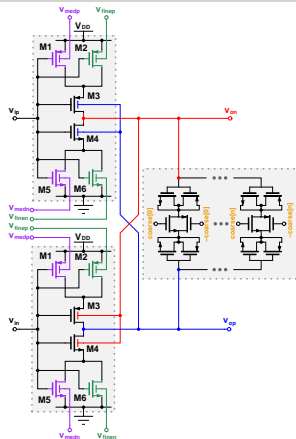
Implementation.

Simulation of revised PVT scheme.

— **Observed FOM = -162 dB**

— **Fine tuning = 0.8% fractional (19 MHz at 2.448 GHz).**

— **Medium tuning = 3.7% fractional (90.5 MHz at 2.448 GHz).**

— **Coarse tuning = 2.1% fractional per diff. mos cap cell.**

— All ranges overlap and final K_{DCO} is acceptable.

— 15% tuning range with 7 bit PVT bank.
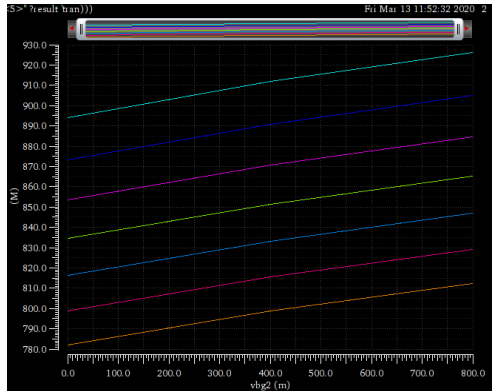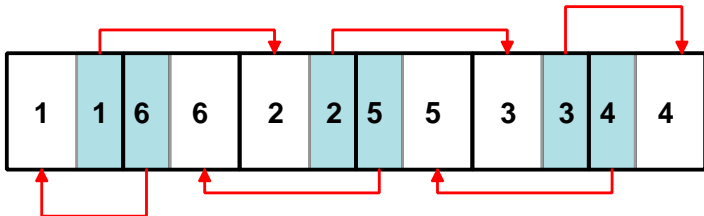
Implementation.

Fine tuning.

— Fine range almost completely linear with back gate voltage from 0-supply voltage, which is very good.
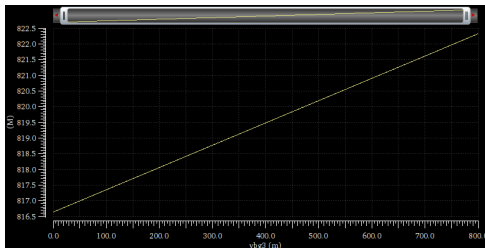
# Ring oscillator floorplan

For equal wire length

Blue is PVT calibration bank, white is delay cell.
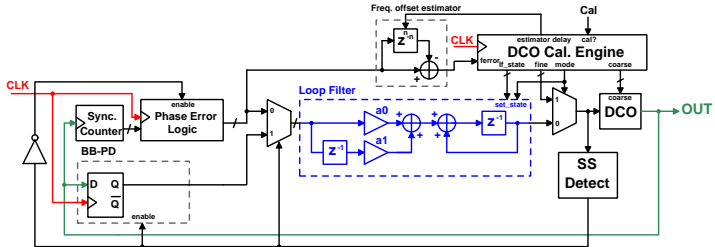
PLL components

Loop filter

— Loop filter
— Control/calibration logic
  • Lock detect, gear switching
  • PVT cal
  • Estimate initial DCO control word
— Phase detectors
  • BBPD
  • Synchronous counter (7-8 bit)
  • Counter phase error decoder
— Level shifter (0.5V → 0.8V)
— CDACs
  • 5 bit coarse
  • 10 bit fine
— Ring oscillator
— RO buffer
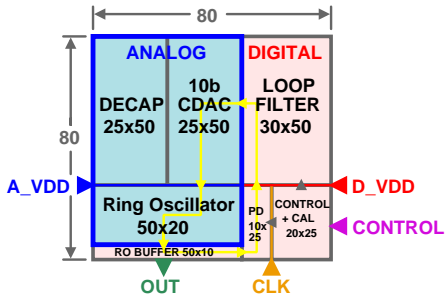
Architecture

Block Diagram

Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Digital (LF)	Other	SUM
50 μW	10 μW	10 μW	**0** ~~5~~ μW	$\leq$ **70** ~~100~~ μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ **70** ~~75~~ μW	μW	Minimize!
FSK BER	$\leq$ 1e-2		GFSK* with $f_{dev}=\pm250$ KHz
CNR	> 20	dBc	Yields **-235** dB FOM$_{jitter}$ ideally
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby, f_{error} < **1 MHz**
Lock Δf tolerance	100	kHz	
FOM$_{jitter}$	$\leq$ -230	dB	**For state of art in size/power**
Area	< 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
~~**TDC resolution**~~	~~$\geq$ 155~~	~~steps/reference cycle~~
DCO gain K_{DCO}	10^4	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	< -80	dBc/Hz @ $\Delta f = 10^6$ Hz, f_c = 2.448 GHz
DCO Power	≤ 50	μW
Digital filter word resolution	≤ 16	bits (power grows as $\mathcal{O}(n^2)$)
BB-PD jitter	≤ 12	ps$_{rms}$

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Layout: oscillator	
12	16.3 - 22.3	CDAC/Ring oscillator	Layout
13	23.3 - 29.3	Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: Done Current Revised

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: `Done` `Current` `Revised`

References

[1] L. Dai and R. Harjani, "Analysis and design of low-phase-noise ring oscillators," ISLPED'00: Proceedings of the 2000 International Symposium on Low Power Electronics and Design (Cat. No.00TH8514), Rapallo, Italy, 2000, pp. 289-294. doi: 10.1145/344166.344639

[2] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998.

[3] G. Jacquemod et al., "Study and reduction of variability in 28 nm FDSOI technology," 2015 International Workshop on CMOS Variability (VARI), Salvador, 2015, pp. 19-22.