Ultra low power integer-N ADPLL

Master's thesis project - meeting 8

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Overview

For this week...

1. Some ring oscillator theory
2. Oscillator topologies tested
3. Final topology.
4. Buffer/new BBPD topology

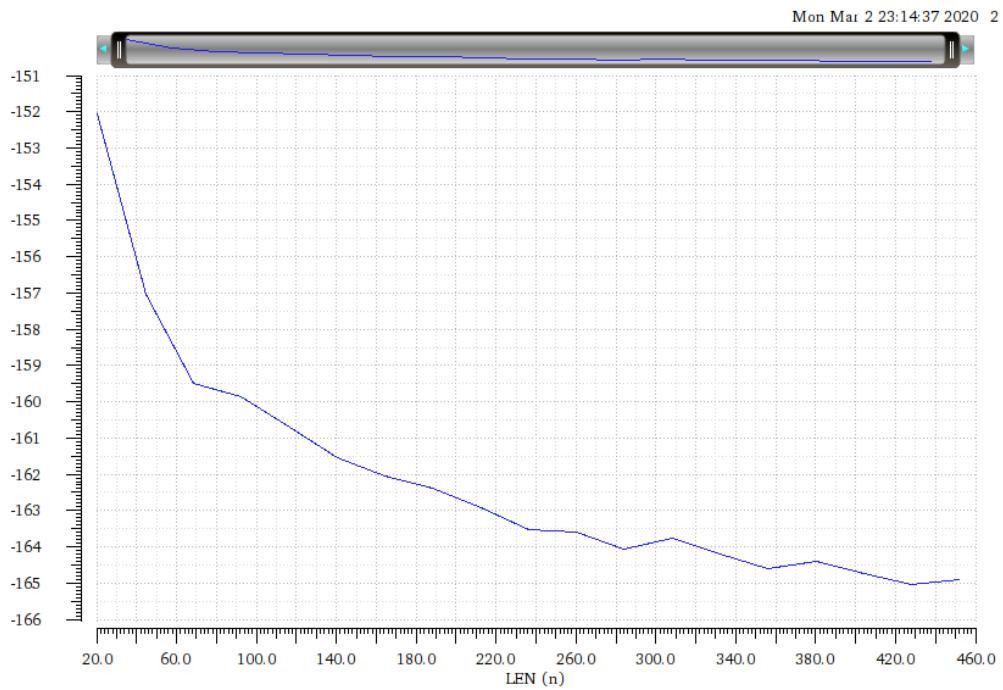
Ring oscillator phase noise

Channel length

- Simulated 5 stage ring oscillator.
- RVT devices, W/L = 5.
- Ran pss/pnoise.
- Computed FOM vs channel length (lower is better):

$$\text{FOM} = 10\log_{10}\left(\left(\frac{\Delta f}{f_0}\right)^2 \cdot \frac{P_{total}}{1\text{ mW}}\right) \quad \text{[dB]} \tag{1}$$

- It is seen that FOM improves asymptotically to $\sim$ -165 with longer L.
- FOM < -160 dB $\rightarrow$ L $\geq$ 100 nm.
- L should be set as long as possible, while mantaining appropriate speed.
  - This is actually recommended in Razavi's new book.



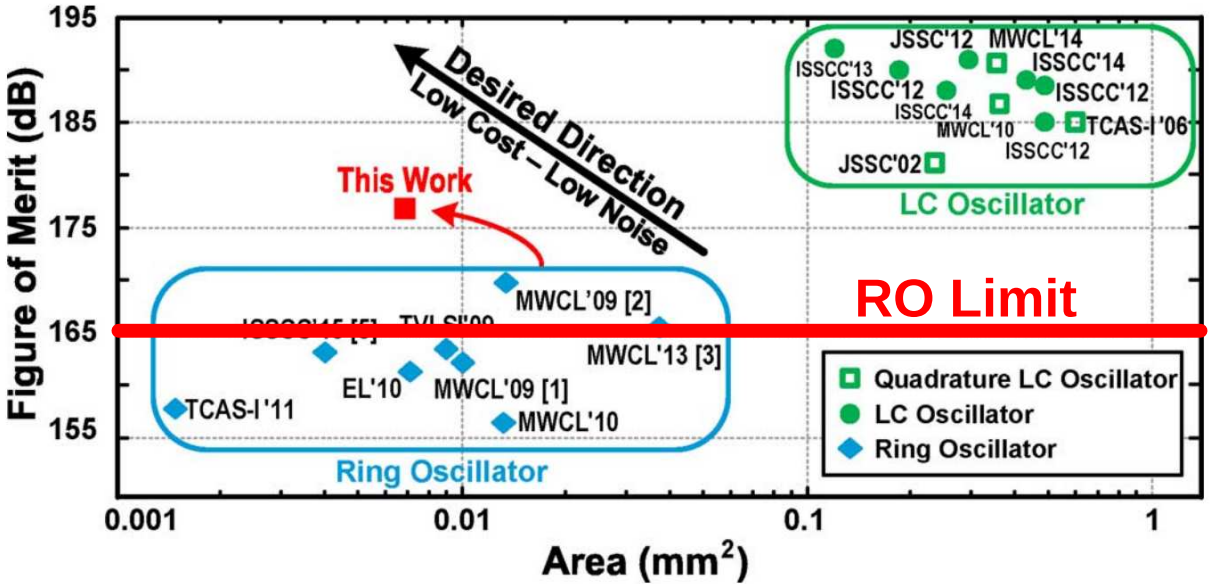
Ring oscillator phase noise

Theoretical limit applied

Ring oscillator phase noise limit from "Minimum Achievable Phase Noise of RC Oscillators", Navid et al. 2005:

$$PN_{min}(\Delta f) = 10 \log 10 \left(\frac{7.33 k_B T}{P} \left(\frac{f_0}{\Delta f} \right)^2 \right) \quad (2)$$

If f_0 = 2.4 GHz, P = 50 μW, Δf= 1 MHz, T = 293 K, $\rightarrow$ **PN_{min} = -84.7 dBc/Hz**
– This limit applied to the below FOM comparison (FOM PN=165 dB):



Ring oscillator model

Assumptions.

- Inverters modeled with ideal switches and lumped R and C components. R = $\langle g_{ch} \rangle^{-1}$, where $\langle g_{ch} \rangle$ is the average channel conductance during the propagation period t_{pd}
- Square law is valid ($L >> L_{min}$).
- In saturation during period of propagtion delay. Requires that $0.25 \cdot V_{DD} < V_{th} < 0.5 \cdot V_{DD}$.

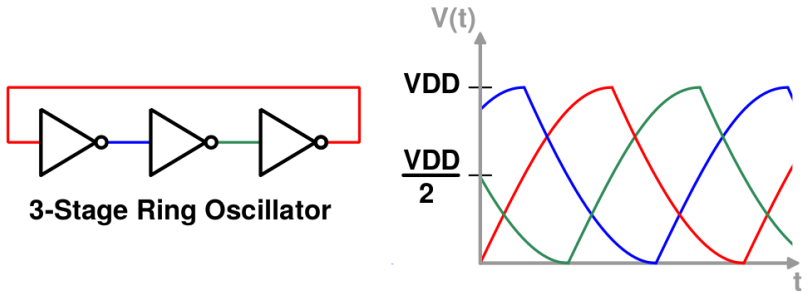
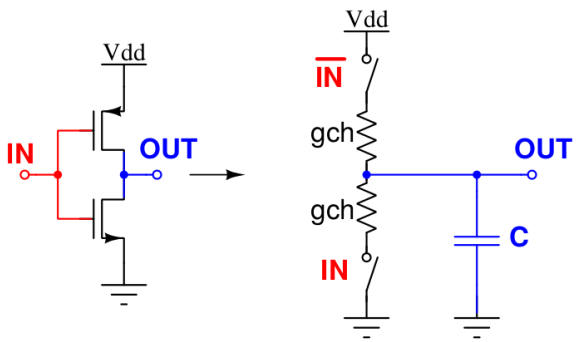
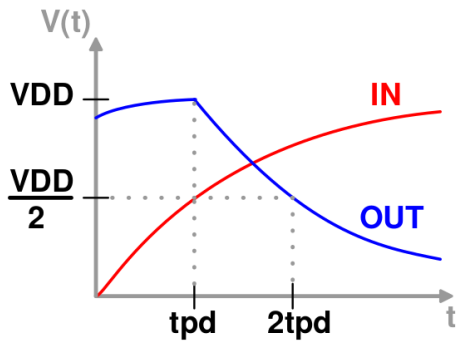


Figure 1: Model for ring oscillator.



(a) Inverter approximate model.



(b) Inverter waveforms in ring oscillator.

Ring oscillator model

Ring oscillator model - equations 1

Define current and voltage exponentials for active device

$$I_{out}(t) = \frac{k_n}{2}\left(\frac{W}{L}\right)_n\left[(V_{in}(t) - V_t)^2\right] - I_{short} = \frac{k_n}{2}\left(\frac{W}{L}\right)_n\left[\left(V_{DD}\left(1 - e^{-t/\tau}\right) - V_t\right)^2 - \left(\frac{V_{DD}}{2} - V_t\right)^2\right] \quad (3)$$

$$V_{out} = V_{DD}e^{-(t-t_{pd})/\tau} \quad (4)$$

Compute average transconductance

$$\langle g_{ch}\rangle = \frac{1}{t_{pd}}\int_0^{t_{pd}} \frac{I_{out}(t)}{V_{out}(t)}\,dt \quad (5)$$

$$\langle g_{ch}\rangle = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n\left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_t\left(\frac{1}{\ln 2} - 1\right)\right] \quad (6)$$

Define node capacitance

$$C = C_{ox}\left(W_N L_N + W_P L_N\right) + C_L \quad (7)$$

Define oscillator frequency

$$f_{osc}^{-1} = 2Nt_{pd} = \frac{2\ln(2)NC}{\langle g_{ch}\rangle} \quad (8)$$

Ring oscillator model

Unequal V_t for NMOS and PMOS

In the case of different threshold voltages for NMOS and PMOS:

$$f_{osc}^{-1} = N(t_{pdn} + t_{pdp}) = \ln(2)NC\left(\frac{1}{\langle g_{ch}\rangle_n} + \frac{1}{\langle g_{ch}\rangle_p}\right) = \frac{2\ln(2)NC}{\langle g_{ch}\rangle'} \tag{9}$$

Enforcing $\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$ **results in:**

$$\langle g_{ch}\rangle' = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \frac{2\alpha_n\alpha_p}{\alpha_n + \alpha_p} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \alpha' \tag{10}$$

Thus α_n **and** α_p **are found for the according threshold voltages and then** $\langle g_{ch}\rangle$ **can be found.**

$$\alpha' = \frac{2\alpha_n\alpha_p}{\alpha_n + \alpha_p}, \quad \alpha_x = \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{tx}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{11}$$

Ring oscillator model

Frequency and power.

Solving for oscillator frequency:

$$f_{osc} = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8 \ln 2} - 1\right) - V_t\left(\frac{1}{\ln 2} - 1\right)\right] \tag{12}$$

If capacitance is strictly proportional to gate area, and PMOS/NMOS are equal sized $C = 2WLC_{ox}$:

$$f_{osc} = \frac{\mu_n}{8 \ln 2 N} \cdot \frac{1}{L^2} \left[V_{DD}\left(\frac{7}{8 \ln 2} - 1\right) - V_t\left(\frac{1}{\ln 2} - 1\right)\right] \tag{13}$$

Power is $P = fC_\Sigma V_{DD}^2$, where C_Σ is the total active capacitance. Thus:

$$P_{osc} = N f_{osc} C V_{DD}^2 = \frac{\mu_n C_{ox}}{4 \ln 2} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8 \ln 2} - 1\right) - V_t\left(\frac{1}{\ln 2} - 1\right)\right] \tag{14}$$

It should be noted that the power consumption is proportional to FET aspect ratio (W/L).

Ring oscillator model

Back gate tuning

In FDSOI, the body effected is manifested as:

$$V_t = V_{t0} - \gamma V_{BG} \tag{15}$$

Using this in the ring oscillator frequency equation, if $\gamma_n \approx \gamma_p$ and $V_{t0n} \approx V_{t0p}$:

$$f_{osc} = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8 \ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right) + \gamma V_{BG}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{16}$$

Equivalently, defining $f_{osc} = f_{0,osc} + \Delta f_{osc}(V_{BG})$, where:

$$\Delta f_{osc}(V_{BG}) = \gamma V_{BG} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{17}$$

Ring oscillator model

Ring oscillator model - equations 3

Constraining backgate voltage to [0, V_{DD}], the center frequency f_c in the tuning range of the oscillator are then:

$$f_c = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1 + \frac{\gamma}{2\ln 2} - \frac{\gamma}{2}\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{18}$$

$$\Delta f = \gamma V_{DD} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{19}$$

The fractional tuning range of the oscillator is:

$$\frac{\Delta f}{f_c} = \frac{\gamma V_{DD}(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}(1 - \ln 2)} \tag{20}$$

If a N-bit DAC is used to control the oscillator, the resulting DCO gain is therefore:

$$K_{DCO} = \frac{f_c}{2^{N_{DAC}}} \cdot \frac{\gamma V_{DD}(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}(1 - \ln 2)} \tag{21}$$

V_{t0} = 0.3V, V_{DD}=0.8, γ = 0.07 yields 27.7% tuning range. I need ca 0.5%. Higher V_{DD} = smaller $\frac{\Delta f}{f_c}$.

Good oscillator characteristics

Hajimiri's phase noise theory

— Hajimiri's famous paper [2] introduces the concept of the impulse sensitivity function (ISF).

$$\Gamma_i(x) = \frac{f_i'}{|\,\vec{f}\,'|^2} = \frac{f_i'}{\sum_{j=1}^{n} f_j'^2}.$$

— ISF defines phase shift of oscillator with unit impulse applied to different parts of the oscillator cycle.

— Transition periods most sensitive to noise.

— Differing rise/fall time results in net DC component in ISF

- This increases oscillator noise susceptibility.

— **Good rise/fall symmetry required in design**.

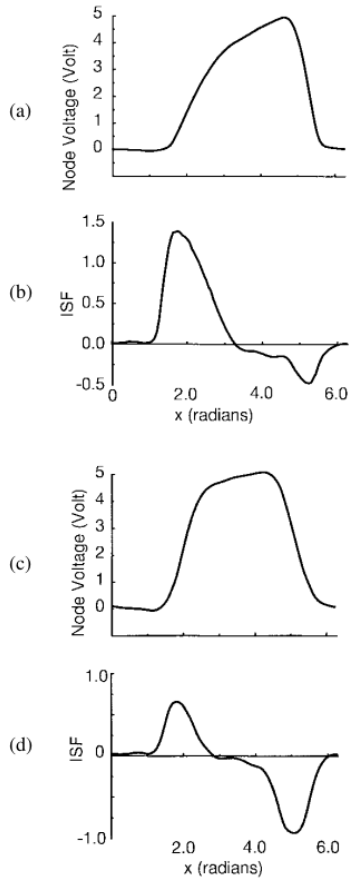
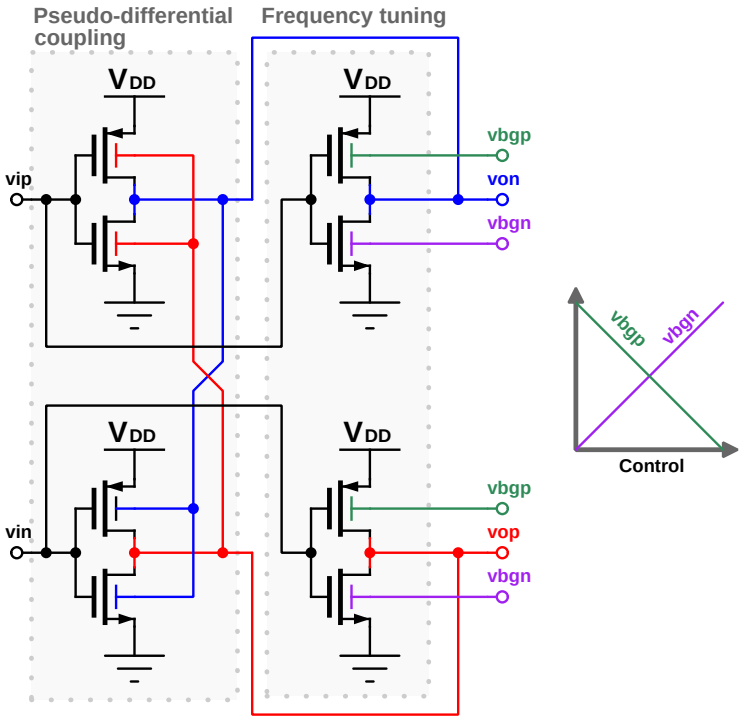


Fig. 16. (a) Waveform and (b) ISF for the asymmetrical node. (c) Waveform and (d) ISF for one of the symmetrical nodes.

Implementation

Parallel topology

- Utilize pseudo-differential inverter stage [3], in parallel with back gate tuned inverter.
  - Pseudo-differential stage couples oscillators, forcing crossing voltage $V_{DD}/2$.
  - Back gate tuned oscillator used to adjust frequency.
- Ratioing the sizes two types of inverters can be used to adjust the VCO gain. A ratio of 1:1 should reduce the K_{VCO} in half from what is expected from theory, a ratio of 3:1 (with pseudo-diff inverters being larger) will reduce K_{VCO} by 4.
- **Requires complementary control of backgate voltage for tuning.**
- **Allows for 0-V_{DD} control range.**



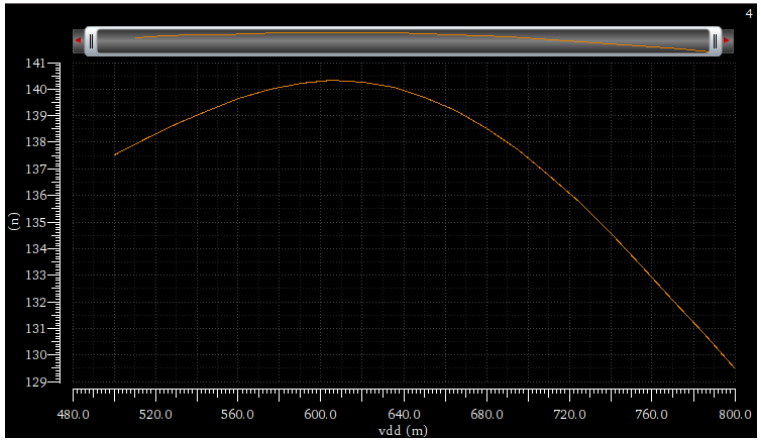
Implementation

Device selection

— Must use devices in N well (PFET, HVTPFET, SLVTN-FET, LVTNFET) to not forward bias substrate diode.

— To achieve $V_m = V_{DD}/2$, PFET + LVTNFET give most reasonable W_P/W_N, ca 1.2-1.4.

- SLVTNFET + PFET needs $W_P/W_N \approx 8$.

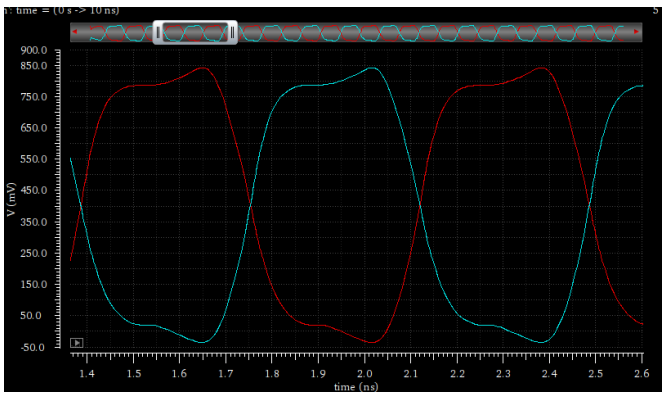


Implementation

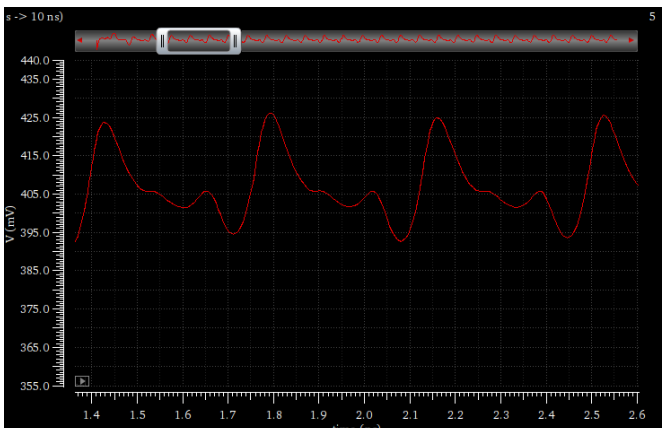
Simulation

- Good symmetry of rise time observed, with V_{cm} close to $V_{DD}/2$ over the full oscillation cycle.
- **Observed 10.3% fractional frequency tuning with L=150nm, FOM=-161 dB, 1:1 ratio of inverters.**
- I require $<$ 1% fractional tuning range to achieve my K_{DCO} with a 10b DAC, this will not work. The (W/L) becomes large to achieve a high inverter ratio, thus increases power too much.

Single ended outputs:



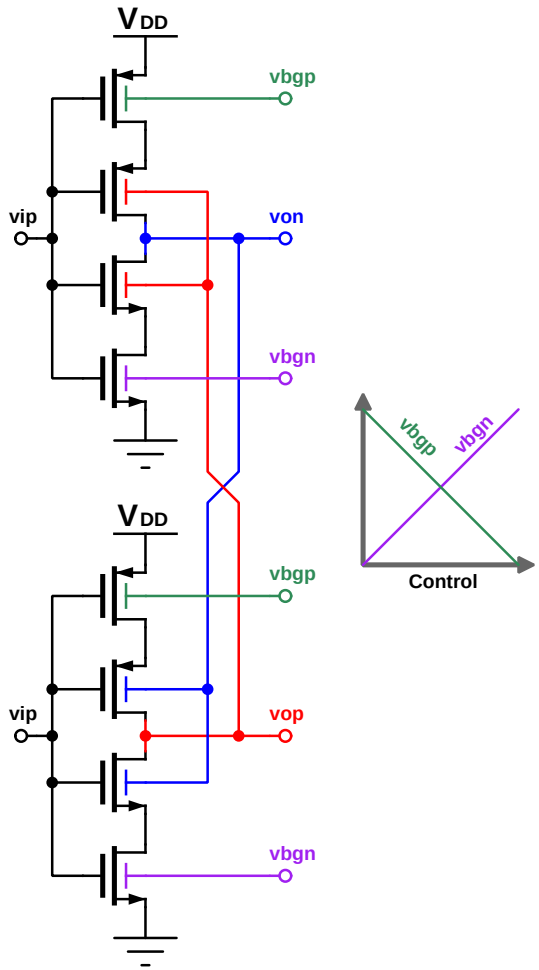
Common mode voltage:



Implementation

Telescopic topology

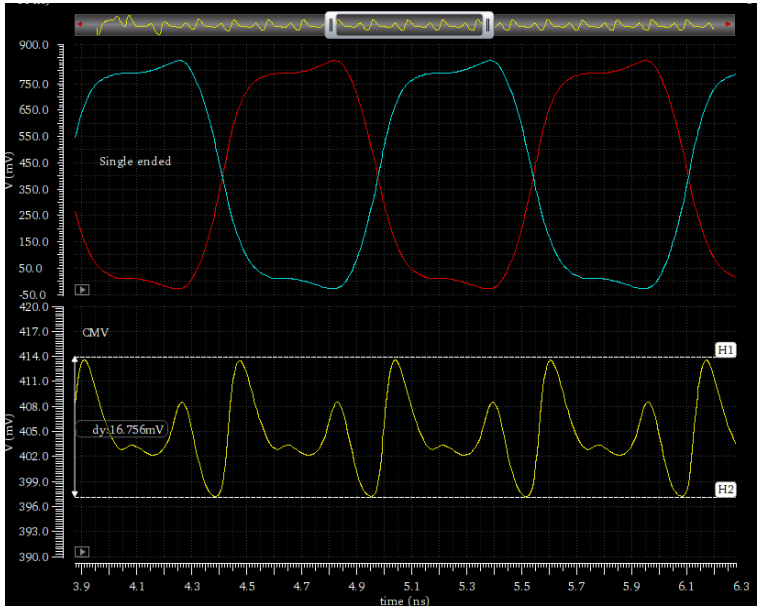
- Modify the pseudo-differential cell to have header/footer transistors with back gate control.
  - Cross-coupled devices force differential operation
  - Header/footer devices used to adjust frequency.
- Ratioing the size of the header/footer devices to the size of the cross-coupling devices tunes K_{VCO}
- **Requires complementary control of backgate voltage for tuning.**



Implementation

Telescopic design - simulation

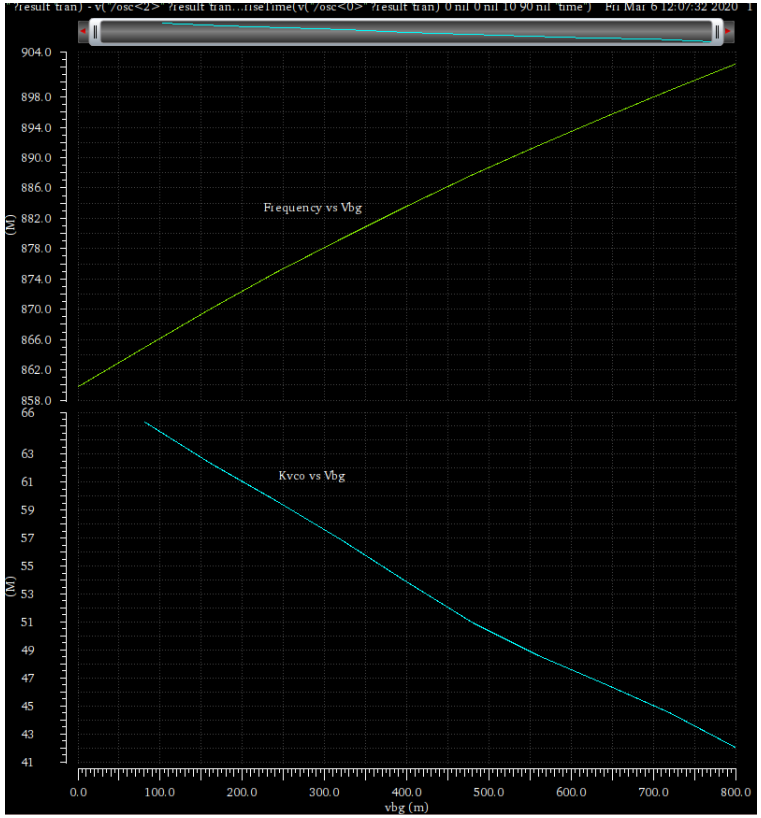
- Good symmetry of rise time observed, with V_{cm} close to $V_{DD}/2$ over the full oscillation cycle.
- W_p/W_n = 1.25. Nominal $(W/N)_n$ = 400n/150n
- **1:1 ratioing: Observed 10.0% fractional frequency tuning with L=150nm, FOM=-162.6 dB.**
- **1:2 ratioing (header/footer larger): Observed 4.8% fractional frequency tuning with L=150nm.**
- Still hard to get required $<$ 1% fractional frequency tuning.



Implementation

Telescopic design K_{VCO} - simulation

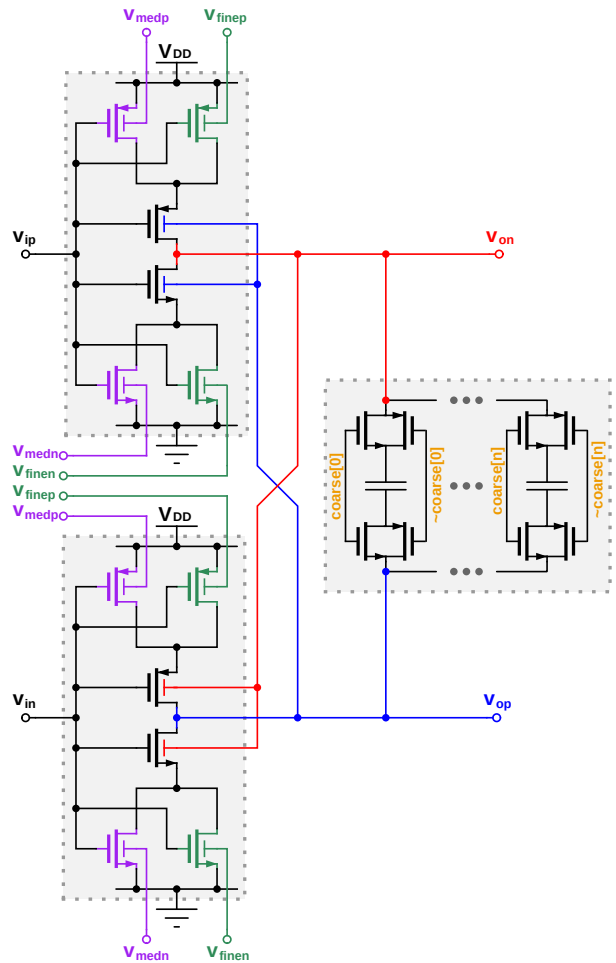
- Not as linear as I had hoped, K_{VCO} decreases by -33% when V_{DD} is swept [0, 0.8] V.
- I have observed a decease in γ at higher back gate biases, this and mobility degredation(??) might explain this trend.



Final delay stage topology.

Telescopic with fine/medium tuning ranges.

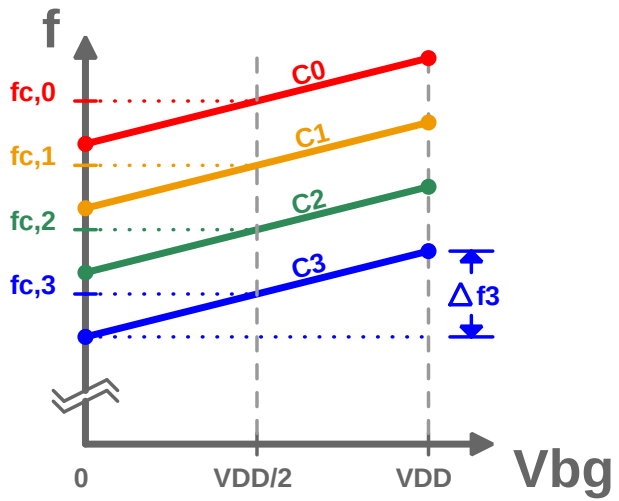
- PVT (coarse), medium and fine tuning all need to coexist (overlap in frequency).
- PVT tuning achieved with bank of differentially connected capacitors
- Fine/medium tuning achieved with parallel combination of header/footer transistors. The ratio of these devices affects the difference of the ranges.



PVT calibration.

Schema.

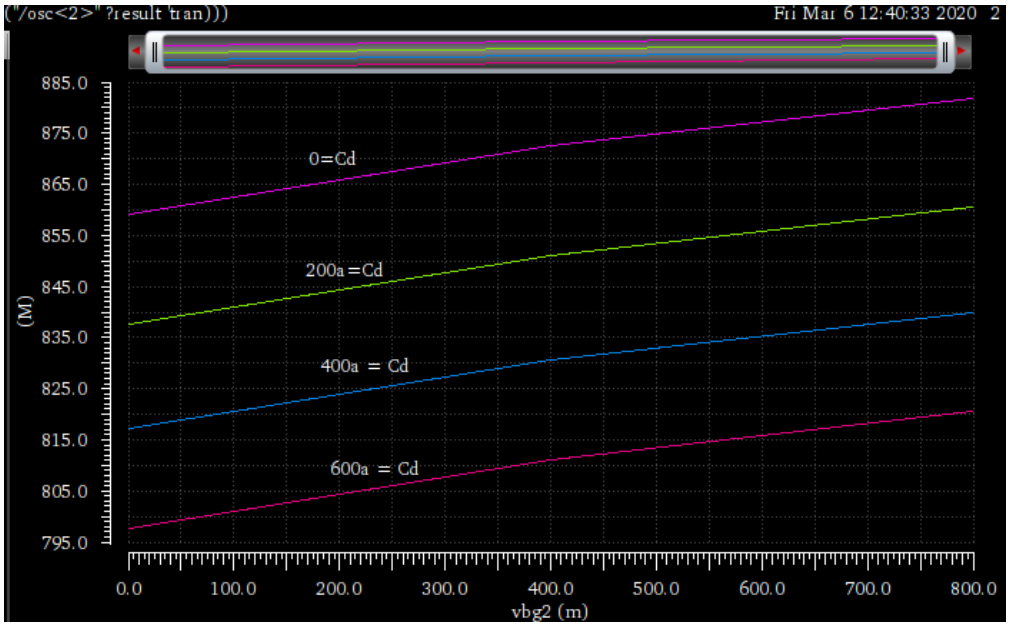
- Will have small number (4-8?) of unit differential capacitors to tune frequency range due to PVT variation.
- Final count will be motivated from post layout monte-carlo and corner simulation.
- Selection of capacitance will be made to ensure that there is overlap between frequency ranges.



Implementation.

Simulation of final delay cell.

- Implemented with 2:1 ratio of header/footer:cross-coupled transistors, 10:1 ratio between fine/medium tuning header/footer transistors.
- L=150 nm, nominal transistor size (W/L) = 500n/150n.
- **Observed FOM = -162.3 dB.**
- **Fine tuning = 0.6% fractional (16 MHz at 2.448 GHz)**, K_{DCO} = 16 kHz/LSB.
- **Medium tuning = 2.6% fractional (63 MHz at 2.448 GHz)**
- **Coarse tuning = 2.2% fractional per 200 aF cap.**
- All ranges overlap and final K_{DCO} is acceptable.



Ring oscillator buffer

Pseudo-differential implementation

— **Edge time out of ring oscillator is slow.** Slow edge time allows noise to couple to phase:

$$\Delta\Phi = 2\pi f_{osc} \left(\frac{dV}{dT} \right)^{-1} \cdot \Delta V \qquad (22)$$

— For good phase detector performance and to avoid effects of external loading, buffers are needed.

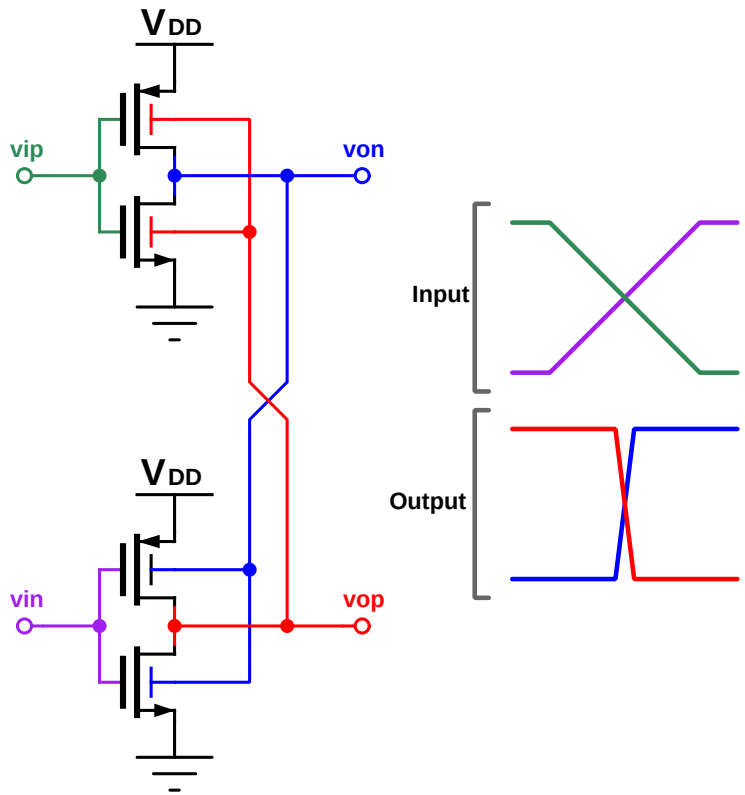
— Highest noise susceptibility when crossing V_{CM}.

— If A_i is the inverter gain at V_{CM}, the pseudodifferential buffer stage here will provide the following CMRR:

$$CMRR = \left| \frac{1 + \gamma A_i}{1 - \gamma A_i} \right| \qquad (23)$$

— Conveniently in 22FDX, $\gamma = 0.075$ and $A_i \approx 14$ with min. length PFET+LVTNFET at $V_{DD} = 0.8$. **Thus CMRR = 26 dB.** This should help reject supply noise.

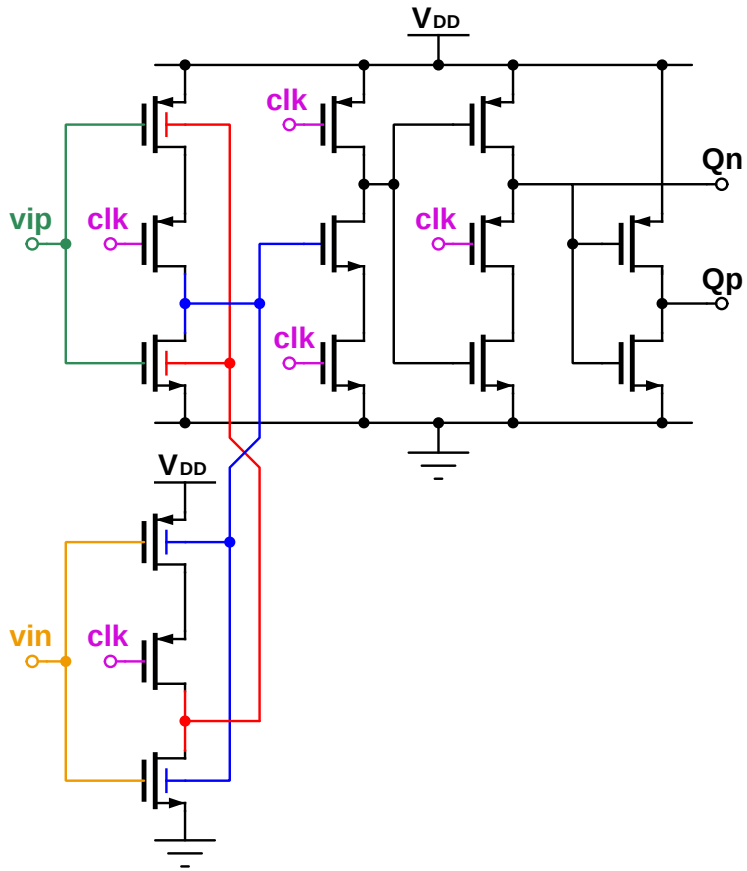
— Longer L yield essentially 0 dB CMRR.



Bang-bang phase detector

Pseudo-differential implementation

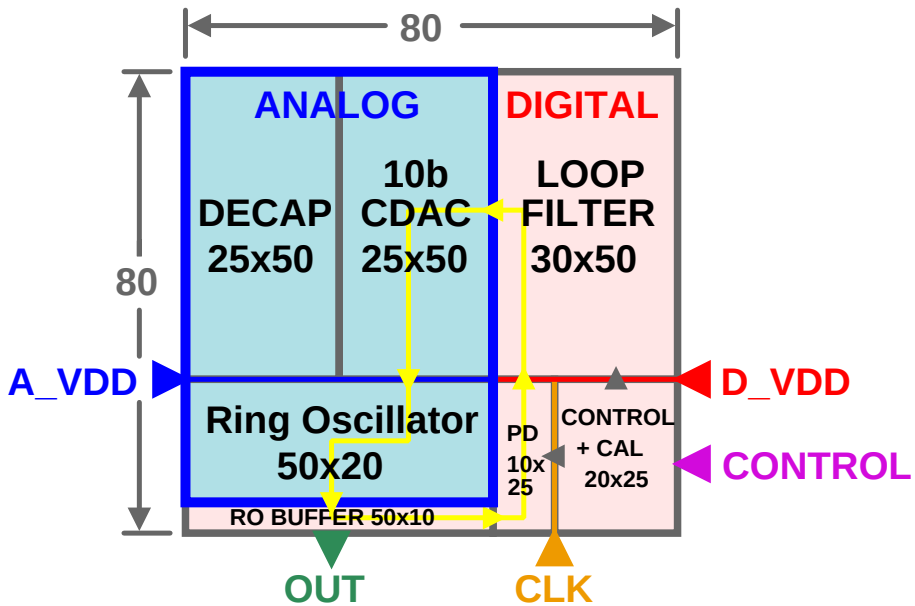
- Can also integrate buffer directly into the TSPC DFF bang-bang phase detector.
- First stage of the DFF is substituted with pseudo-differential inverter.
- Can connect direct to ring oscillator and have common mode (supply noise) rejection if minimum length used.



PLL components

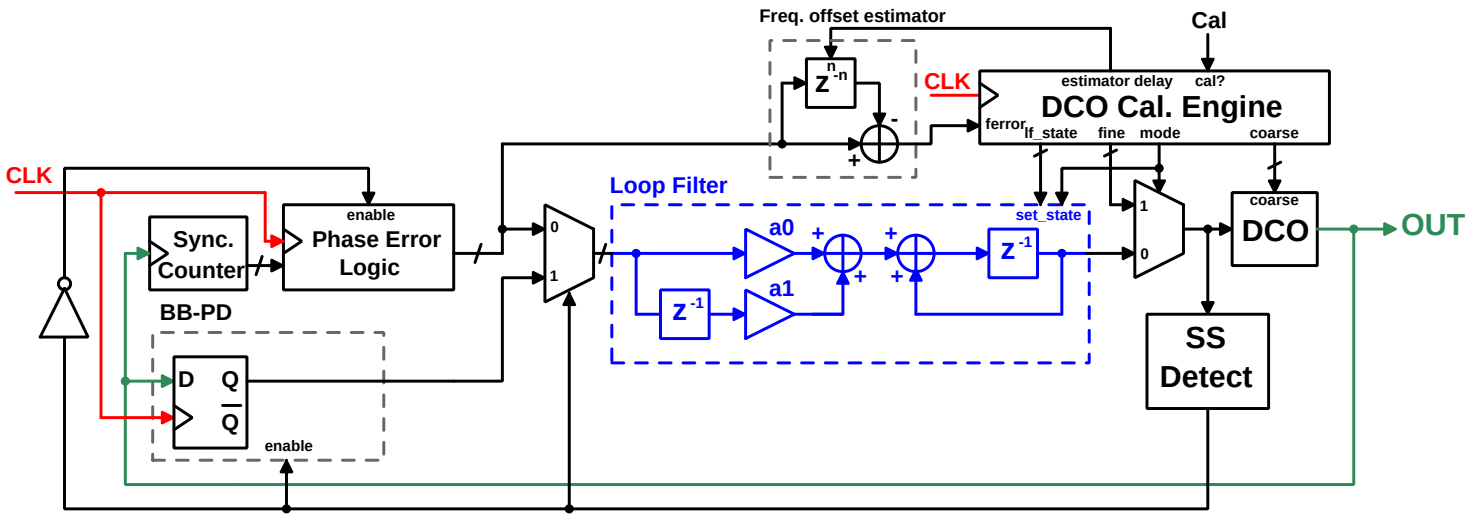
Loop filter

- Loop filter
- Control/calibration logic
  - Lock detect, gear switching
  - PVT cal
  - Estimate initial DCO control word
- Phase detectors
  - BBPD
  - Synchronous counter (7-8 bit)
  - Counter phase error decoder
- Level shifter (0.5V → 0.8V)
- CDACs
  - 5 bit coarse
  - 10 bit fine
- Ring oscillator
- RO buffer



Architecture

Block Diagram



Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Digital (LF)	Other	SUM
50 μW	10 μW	10 μW	**0** ~~≤ 5~~ μW	$\leq$ **70** ~~100~~ μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ **70** ~~75~~ μW	μW	Minimize!
FSK BER	$\leq$ 1e-2		GFSK* with f_{dev}=$\pm$250 KHz
CNR	$>$ 20	dBc	Yields **-235** dB FOM_{jitter} ideally
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby, f_{error} $<$ **1 MHz**
Lock Δf tolerance	100	kHz	
FOM_{jitter}	$\leq$ -230	dB	**For state of art in size/power**
Area	$<$ 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
~~**TDC resolution**~~	~~$\geq$ 155~~	~~steps/reference cycle~~
DCO gain K_{DCO}	10^4	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	$<$ -80	dBc/Hz @ $\Delta f = 10^6$ Hz, f_c = 2.448 GHz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	$\leq$ 16	bits (power grows as $\mathcal{O}(n^2)$)
BB-PD jitter	$\leq$ 12	ps_{rms}

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Layout: oscillator	
12	16.3 - 22.3	CDAC	Schem+layout
13	23.3 - 29.3	Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

References

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