Ultra low power integer-N ADPLL

Master's thesis project - meeting 2

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24 January 2020 (calendar week 4)

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Schem. design: oscillator	LC DCO
12	16.3 - 22.3	Schem. design: divider	TSPC + pulse swallow or sync counter?
13	23.3 - 29.3	Schem. design: Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

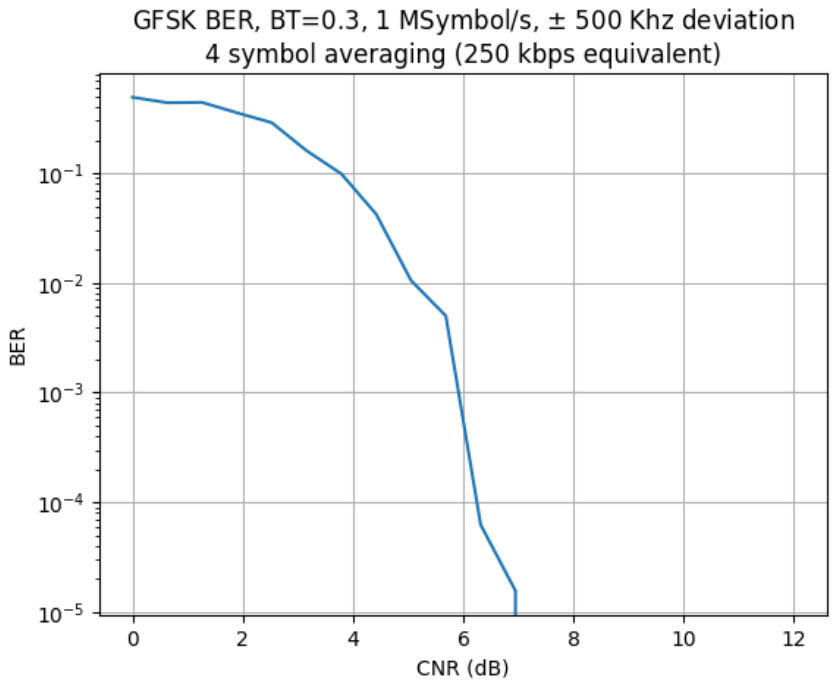
Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

Defining PLL Requirements

Radio application BER requirements.

- Simulated BER of GFSK radio with BT=0.3, 1 MSymbols/s, $\pm$ 250 kHz frequency deviation, 4 bit averaging in receiver for effective 250 kbps rate.
- Carrier to noise ratio (CNR) of the signal entering the demodulator greatly decreases after 6 dB (BER = 10^{-2} is at 5.1 dB). THUS targeting > 6 dB CNR.
- CNR $\approx$ Residual phase modulation (i.e. integrated phase noise power).



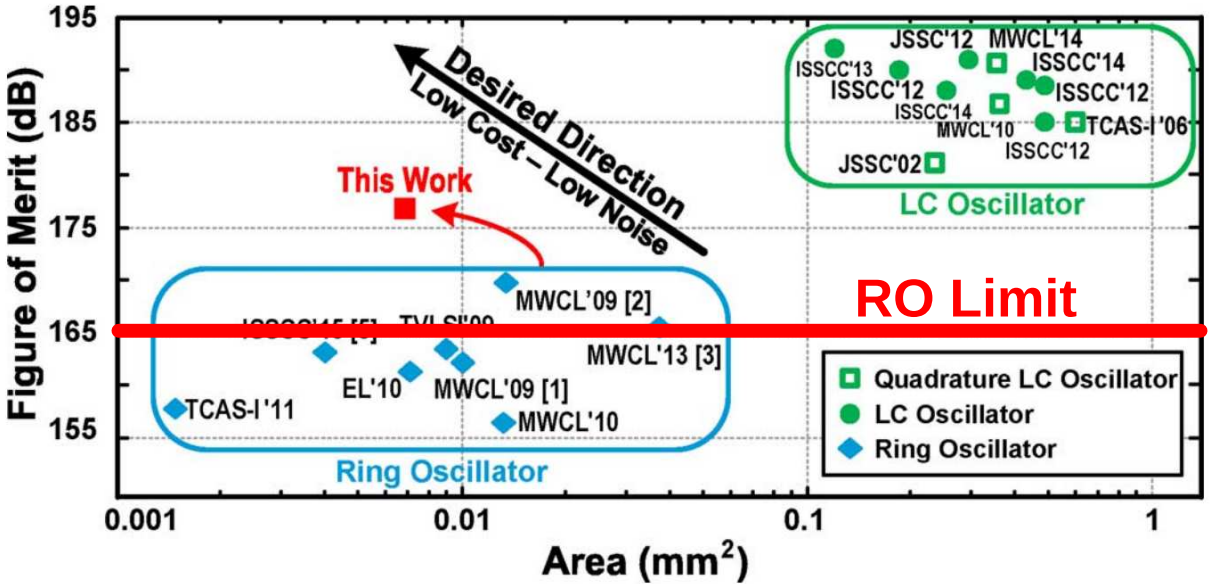
Ring oscillator phase noise

Theoretical limit applied

Ring oscillator phase noise limit from "Minimum Achievable Phase Noise of RC Oscillators", Navid et al. 2005:

$$PN_{min}(\Delta f) = 10 \log 10 \left(\frac{7.33 k_B T}{P} \left(\frac{f_0}{\Delta f} \right)^2 \right) \quad (1)$$

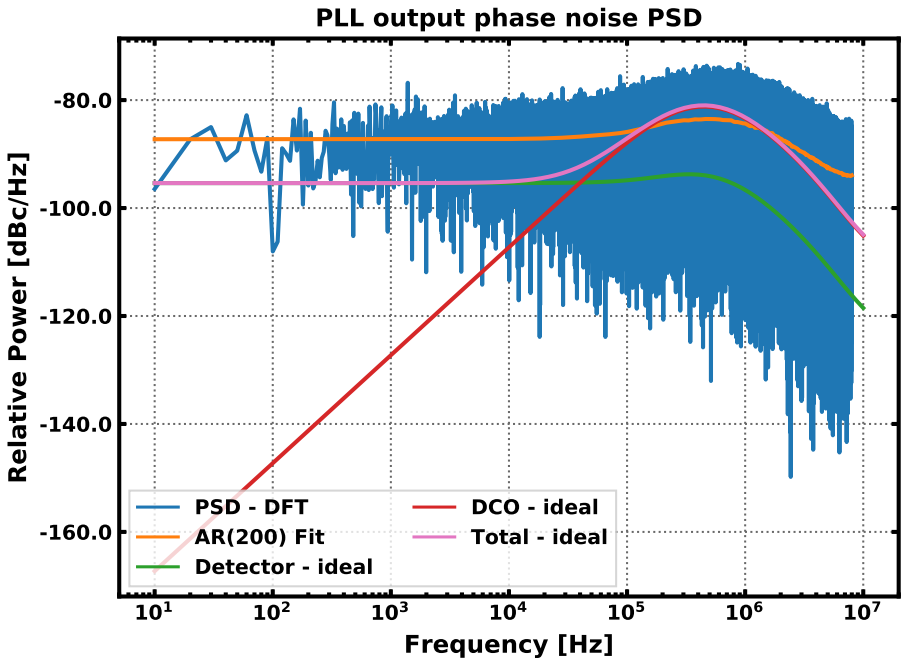
If f_0 = 2.4 GHz, P = 50 μW, Δf= 1 MHz, T = 293 K, $\rightarrow$ **PN_{min} = -84.7 dBc/Hz**
– This limit applied to the below FOM comparison (FOM PN=165 dB):



Simulated BER

BBPD-optimized (total phase noise minimized).

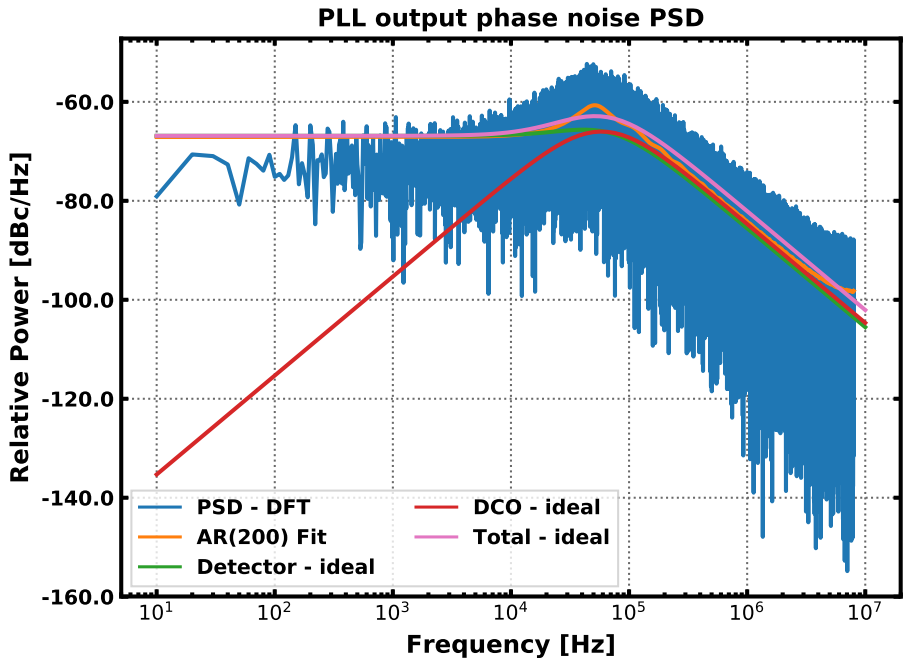
- f_0 = 2.4 GHz, P = 50 μW, clock freq = 16 MHz.
- Optimized for minimum phase noise with BBPD. Closed loop BW = 911 kHz.
- **CNR = 26 dB**, low BER expected.
- Simulation recorded 0 BER (with 64000 bits)



Simulated BER

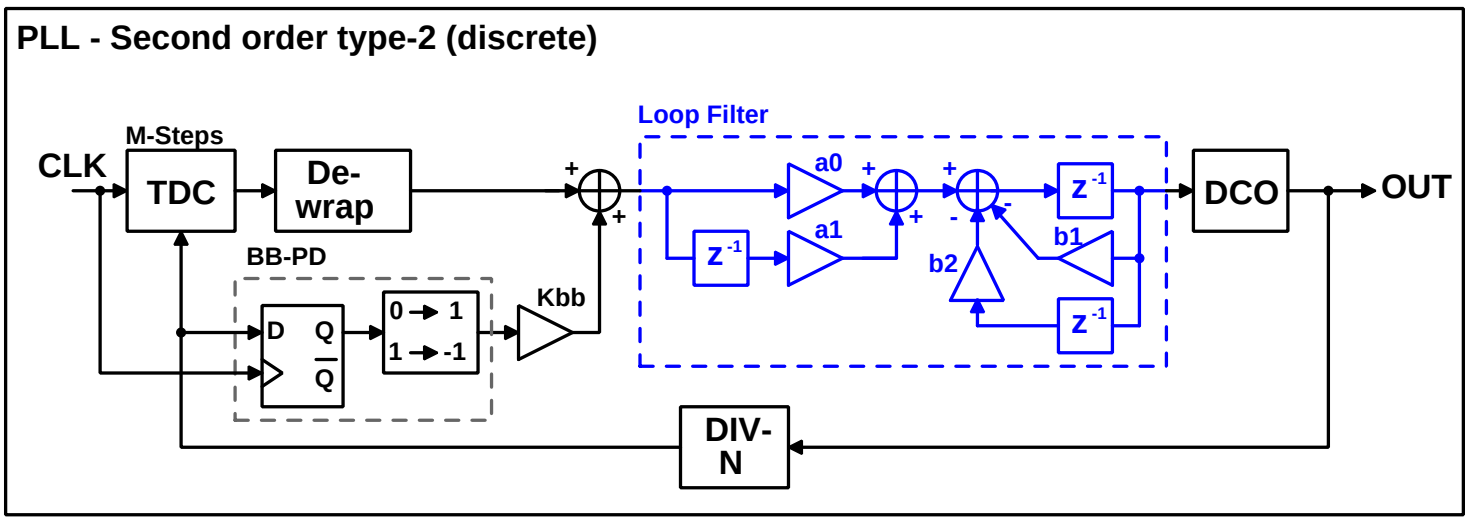
Sub-optimal phase noise.

- f_0 = 2.4 GHz, P = 50 μW, clock freq = 16 MHz.
- Closed loop BW = 145 kHz.
- **CNR = 17 dB**
- Simulation recorded 0 BER (with 64000 bits)
- Even under non-optimal conditions, 50 μW provides >10 dB margin if 6 dB CNR is assumed limit.



Architecture

Block Diagram



Power Targets

DCO	Phase detector	Divider	Digital (LF)	Other	SUM
50 μW	10 μW	10 μW	10 μW	$<<$ 10 μW	$<$ 100 μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	≤ 100	μW	minimize!
FSK BER	$\leq$ 1e-2		2FSK with $f_{dev}=\pm 250$ KHz
CNR	$<< 6$	dB	
Initial Lock Time	≤ 10	μs	Upon cold start
Re-lock Time	≤ 5	μs	Coming out of standby
Lock Δf tolerance	10^5	Hz	

Additionally: PLL output should support IQ sampling at LO frequency.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
TDC resolution	$\geq$ 155	steps/reference cycle
DCO gain K_{DCO}	10^4	Hz/LSB
DCO Phase noise	$<$ -80	dBc/Hz at $\Delta f = 10^6$ Hz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	13	bits

Table: System-level specifications