Ultra low power integer-N ADPLL

Master's thesis project - meeting 6

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Overview

For this week...

1. Figure out synthesis, place and route with Genus and Innovus
2. Tested with BBPD, Loop filter

Invecas model

Generating new Invecas models???

- The GF22FDX models used for synthesis (from `\eda\kits\invecas\...`) have sort of odd voltages defined, i.e. V_{dd} = {0.59, 0.65}, body bias = {0.45, 0.8} for TT corner.
- Also, only SLVT is available.
- These library files say they are generated from Cadence Liberate, is this something I can also use to generate new .lib files with V_{dd}/body bias closer to my needs?

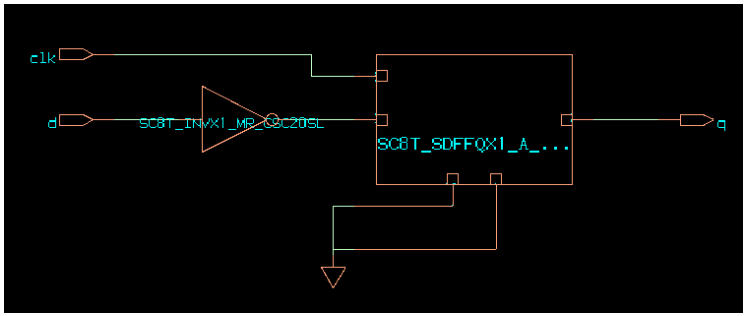
```
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_FFG_0P72V_0P00V_0P45V_M0P45V_125C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_FFG_0P72V_0P00V_0P45V_M0P45V_M40C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_FFG_0P72V_0P00V_0P80V_M0P80V_125C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_FFG_0P72V_0P00V_0P80V_M0P80V_M40C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_SSG_0P59V_0P00V_0P45V_M0P45V_125C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_SSG_0P59V_0P00V_0P45V_M0P45V_M40C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_SSG_0P59V_0P00V_0P80V_M0P80V_125C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_SSG_0P59V_0P00V_0P80V_M0P80V_M40C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_TT_0P59V_0P00V_0P45V_M0P45V_125C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_TT_0P59V_0P00V_0P45V_M0P45V_M40C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_TT_0P65V_0P00V_0P45V_M0P45V_25C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_TT_0P65V_0P00V_0P45V_M0P45V_85C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_TT_0P65V_0P00V_0P80V_M0P80V_25C.lib
2019 GF22FDX_SC8T_104CPP_BASE_CSC20SL_TT_0P65V_0P00V_0P80V_M0P80V_85C.lib
```

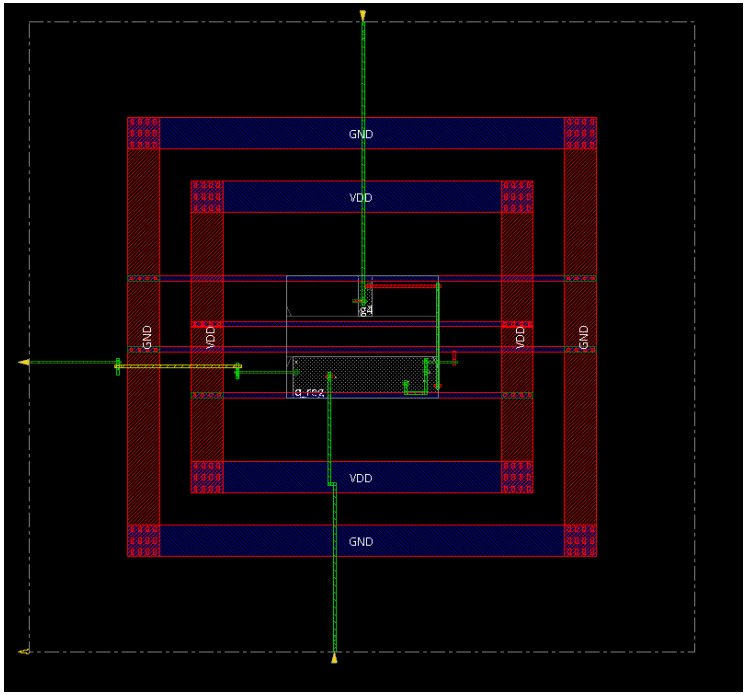
```
voltage_map (VDD, 0.65);
voltage_map (VNW_N, 0.45);
voltage_map (VPW_P, -0.45);
voltage_map (VSS, 0);
voltage_map (GND, 0);
voltage_map (VSSSUB, 0);
```

Synthesis/place and route

Attempt 1: BBPD.

— Tried simple test first...

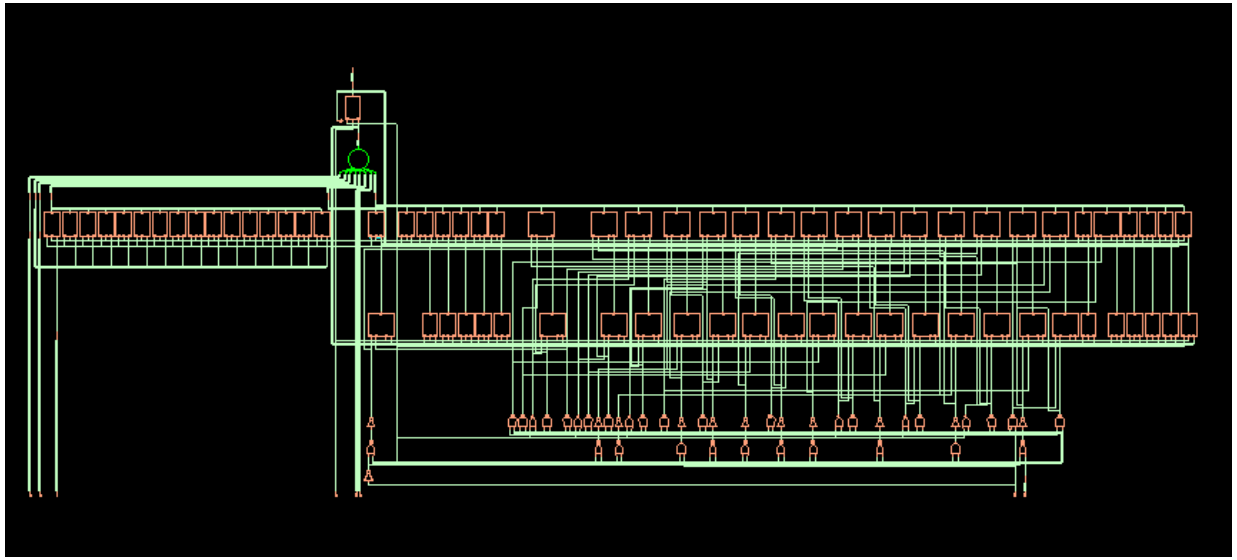




Synthesis/place and route

Loop filter

— Constructed using 16 bit width for all parts of datapath (3x adders, 4x multipliers).



Synthesis/place and route

Power estimate

- 117.6 μW with V_{DD} = 0.65, 0.45V body bias, TT corner, 25C.
- Probably is lower if I reduce the supply (0.5V?).
- Can reduce the design to PI controller only, removed 2 multipliers (should reduce power $\sim$2x?)

```
Instance: /lf_test
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     6.10866e-06  2.90116e-06  9.92165e-07  1.00020e-05   8.51%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     8.00500e-05  1.39195e-05  1.32609e-05  1.07230e-04  91.20%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  3.40704e-07  3.40704e-07   0.29%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     8.61587e-05  1.68207e-05  1.45938e-05  1.17573e-04 100.00%
  Percentage          73.28%       14.31%       12.41%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Synthesis/place and route

Area estimate

— Area of 1891 μm^2. Equal to 43.5x43.5 μm

Type	Instances	Area	Area %
sequential	72	132.588	7.0
inverter	234	31.150	1.6
logic	2439	1727.631	91.3
physical_cells	0	0.000	0.0
total	2745	1891.369	100.0

Original estimates...

Component-level specs

— Given 22-FDX yields ca. 5.5 MGates/mm^2, assume α = 0.1, f_{clk} = 16 MHz:

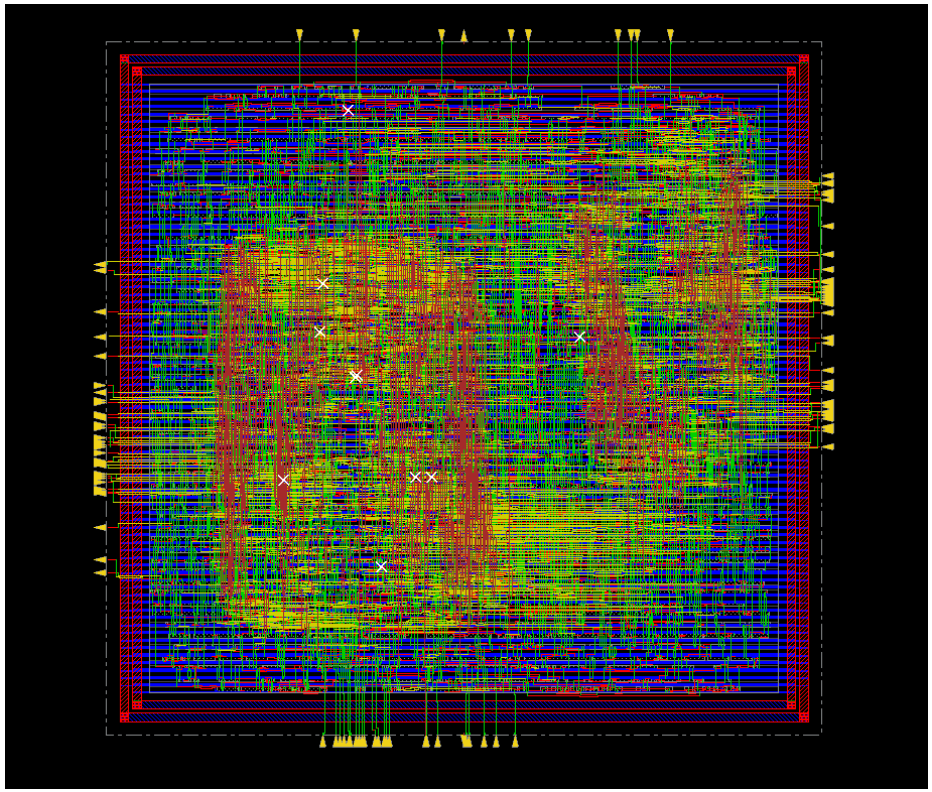
Datapath bits	Gates+DFFs	Area [μm^2]	Square side [μm]	Power [μW], α = 0.1
8	2652	521	22.8	4.24
9	3390	660	25.7	5.42
10	4213	815	28.5	6.74
11	5127	986	31.4	8.20
12	6126	1172	34.2	9.80
13	7216	1375	37.1	11.5
14	8391	1594	39.9	13.4
15	9657	1829	42.8	15.5
16	11008	2080	45.6	17.6

— **Area is close**. Power is off, however it was based on a guess based relative to values obtained at 0.35V.

Synthesis/place and route

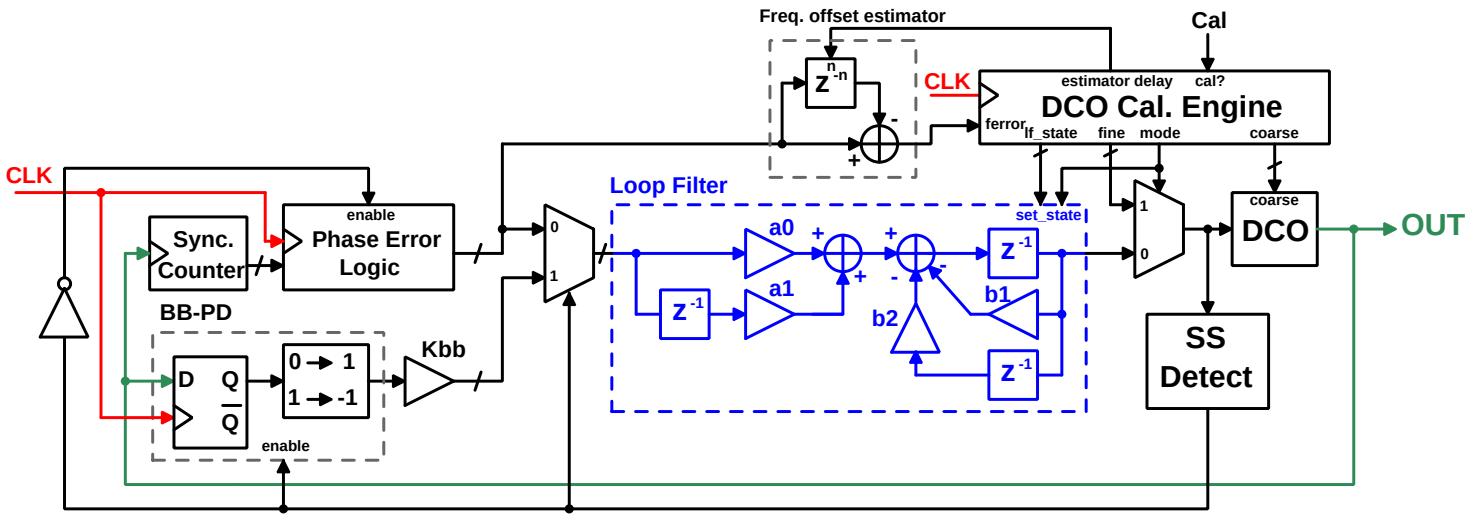
Loop filter layout.

— First iteration at loop filter layout... still need to extract the circuit/LVS etc...



Architecture

Block Diagram



Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Divider	Digital (LF)	Other	SUM
50 μW	10 μW	**N/A** ~~10 μW~~	10 μW	$\leq$ **5** ~~10~~ μW	$\leq$ **75** ~~100~~ μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ **75** ~~100~~ μW	μW	Minimize!
FSK BER	$\leq$ 1e-2		GFSK* with f_{dev}=$\pm$250 KHz
CNR	$>$ 20	dBc	Yields **-235** ~~-233~~ dB FOM_{jitter} ideally
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby, f_{error} $<$ **1 MHz**
Lock Δf tolerance	100	kHz	
FOM_{jitter}	$\leq$ -230	dB	**For state of art in size/power**
Area	$<$ 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
~~**TDC resolution**~~	~~$\geq$ 155~~	~~steps/reference cycle~~
DCO gain K_{DCO}	10^4	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	$<$ -80	dBc/Hz @ $\Delta f = 10^6$ Hz, f_c = 2.448 GHz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	$\leq$ 16	bits (power grows as $\mathcal{O}(n^2)$)
BB-PD jitter	$\leq$ 12	ps_{rms}

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Schem. design: oscillator	LC DCO
12	16.3 - 22.3	Schem. design: divider	TSPC + pulse swallow or sync counter?
13	23.3 - 29.3	Schem. design: Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

References

[1] H. Xu and A. A. Abidi, “Design Methodology for Phase-Locked Loops Using Binary (Bang-Bang) Phase Detectors,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 1637–1650, Jul. 2017.

[2] F. Gardner, “Charge-Pump Phase-Lock Loops,” IEEE Transactions on Communications, vol. 28, no. 11, pp. 1849–1858, Nov. 1980, doi: 10.1109/tcom.1980.1094619.