Ultra low power integer-N ADPLL

Master's thesis project - meeting 4

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Overview

For this week...

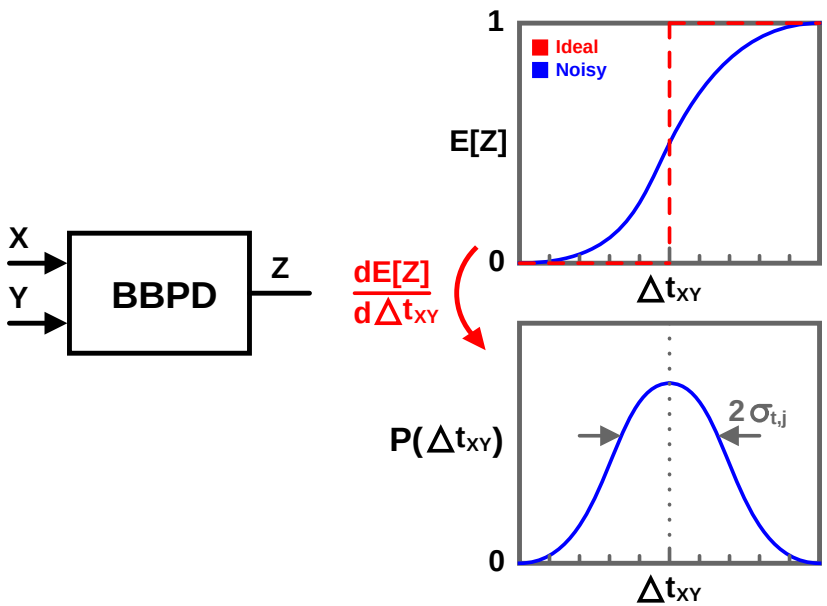
1. Theory for optimal PLL using BB-PD.
2. Linear phase detector
   - Delay line methods waste of time, need calibration, complexity increases with resolution
   - Counter TDC is viable.

Noisy BB-PD Model.

Introduction of timing jitter to model.

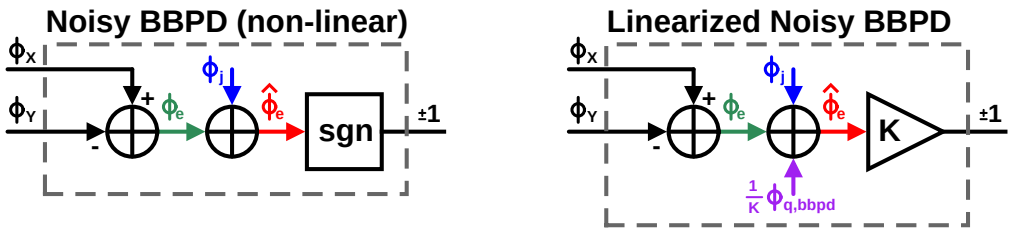
— Uncorrelated / stochastic processes in a BB-PD result in the $\mathbb{E}[Z]$ with respect to input timing difference Δt_{xy} to deviate from an ideal step response.

— $d\mathbb{E}[Z]/d\Delta t_{xy}$ results in a timing jitter probability distribution P(T=Δt_{xy}). The variance of this distribution on random jitter variable T, $\mathrm{Var}[T] = \sigma^2_{t,j}$, is the jitter power.



Noisy BB-PD Model.

Linearized noisy BB-PD model.



— BB-PD is non-linear, however with a stationary input ϕ_e with power $\sigma^2_{\phi_e}$, its gain can be linearized [1] as:

$$K = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\phi_e}} \tag{1}$$

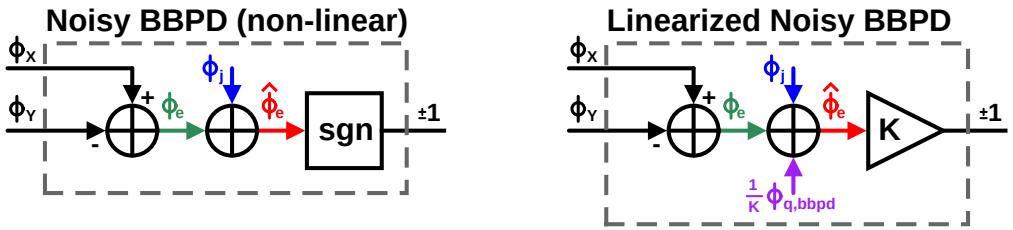
— The output has power $\sigma^2_{\phi_Z} = 1 = K^2\sigma^2_{\phi_e} + \sigma^2_{\phi_{q,bbpd}}$

— $\phi_{q,bbpd}$ is a error noise power inherent to the BB-PD.

$$\sigma^2_{\phi_{q,bbpd}} = 1 - \frac{2}{\pi} \tag{2}$$

Noisy BB-PD Model.

Linearized noisy BB-PD model (continued).



— Referring $\phi_{q,bbpd}$ to be before gain K, results in a total phase noise power for the BB-PD (assuming all noise sources uncorrelated):

$$\sigma^2_{\phi n,BBPD} = \left(\frac{\pi}{2} - 1\right)\sigma^2_{\phi e} + \frac{\pi}{2}\sigma^2_{\phi j} \tag{3}$$

— If the BB-PD is connected directly to oscillator output, $\sigma^2_{\phi e} = \sigma^2_{\phi n}$, i.e. the PLL output phase noise. The spectral density of the BB-PD phase noise is then:

$$S_{\phi n,BBPD} = \frac{\sigma^2_{\phi n,BBPD}}{f_{ref}} = \frac{\left(\frac{\pi}{2} - 1\right)\sigma^2_{\phi n} + \frac{\pi}{2}\sigma^2_{\phi j}}{f_{ref}} \tag{4}$$

BB-PD PLL Optimization.

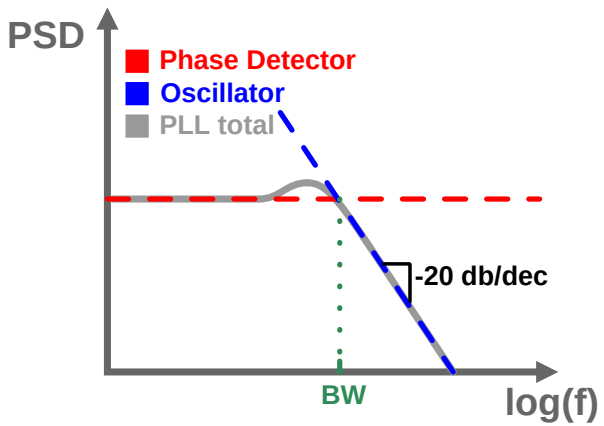
Approximate model for phase noise and optimal bandwidth.

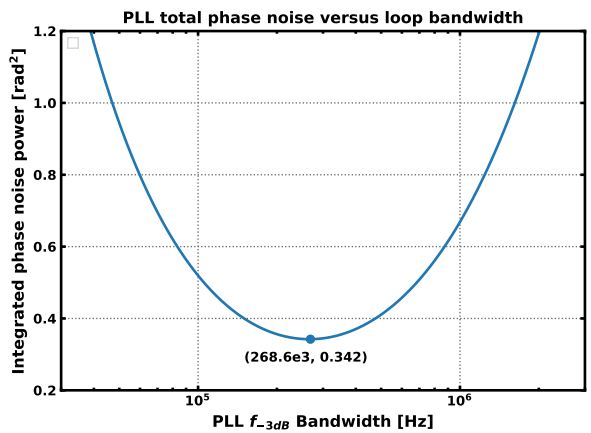
— It is observed that PLL phase noise spectrum is approximately Lorentzian (except for peaking and flicker noise components). Given BB-PD noise PSD of $S_{\phi n,BBPD}$, and an oscillator with noise PSD $S_{\phi n,osc}(\Delta f)$, the optimal bandwidth for minimum noise power is:

$$BW_{opt} = \sqrt{\frac{S_{\phi n,osc}(\Delta f)}{S_{\phi n,BBPD}}}\Delta f \tag{5}$$

— The total PLL output phase noise with optimal bandwidth is then:

$$\sigma^2_{\phi n,opt} = \pi\sqrt{\phi n,osc(\Delta f)S_{\phi n,BBPD}}\Delta f \tag{6}$$





BB-PD PLL Optimization.

BB-PD Jitter constraint with fixed BW and f_{ref} relationship.

— Using the findings for BB-PD noise PSD, assumption of Lorentzian spectrum, and constraint that BW = αf_{ref} (recommended α<0.1 [2], rule of thumb since ancient PLL days). Given oscillator center frequency f_c, BB-PD jitter is constrained:

$$\sigma_{t_j} \leq \frac{\sigma_{\Phi_n}}{2\pi f_c}\sqrt{\frac{2}{\pi}\left(\frac{1}{\pi\alpha}-\frac{\pi}{2}+1\right)} = \frac{\sigma_{\Phi_n}}{2\pi f_c}\beta(\alpha) \tag{7}$$

— $\beta(\alpha = 0.1)$ = 1.28, $\beta(\alpha = 0.05)$ = 1.92.

— Using my PLL specifications (f_c = 2.448 GHz, CNR = -σ_{Φ_n} = 17 dB, $\alpha = 0.1$), $\sigma_{t,j} \leq$ 11.8 **ps**

BB-PD optimal Jitter.

— With an unconstrained relationship for BW and f_{ref}, and the optimal bandwidth finding, it is determined that the optimal value of $\sigma_{t,j}$ for minimum phase noise is:

$$\sigma_{t_j,opt} = \frac{\sigma_{\Phi_n}}{2\pi f_c}\sqrt{\frac{2}{\pi}\left[\frac{\sigma_{\Phi_n}^4 f_{ref}}{\pi^2 S_{\phi n,osc}(\Delta f)\Delta f^2}-\left(\frac{\pi}{2}-1\right)\sigma_{\Phi_n}^2\right]} \tag{8}$$

BB-PD PLL Optimization.

Optimal parameter selection.

— Setting the two jitter equations of the last side equal, it is found that optimal phase noise power is:

$$\sigma^2_{\Phi n,opt} = \frac{\pi S_{\phi n,osc}(\Delta f)\Delta f^2}{\alpha f_{ref}} \tag{9}$$

— The optimal reference frequency ($\sigma_{\Phi_n} = 2\pi f_c \sigma_{t_n}$ = CNR):

$$f_{ref} = \frac{\pi S_{\phi n,osc}(\Delta f)\Delta f^2}{\alpha \sigma^2_{\Phi n}} \tag{10}$$

— The optimal oscillator phase noise at offset Δf:

$$S_{\phi n,osc}(\Delta f) = \frac{\alpha f_{ref}\sigma^2_{\Phi n}}{\pi \Delta f^2} \tag{11}$$

— For CNR = 17 dB, $S_{\phi n,osc}(\Delta f = 1MHz)$ = -80 dBc/Hz, α = 0.1, the optimal f_{ref} = 15.7 MHz.

— For CNR = 20 dB, $S_{\phi n,osc}(\Delta f = 1MHz)$ = -80 dBc/Hz, α = 0.1, the optimal f_{ref} = 31.4 MHz.

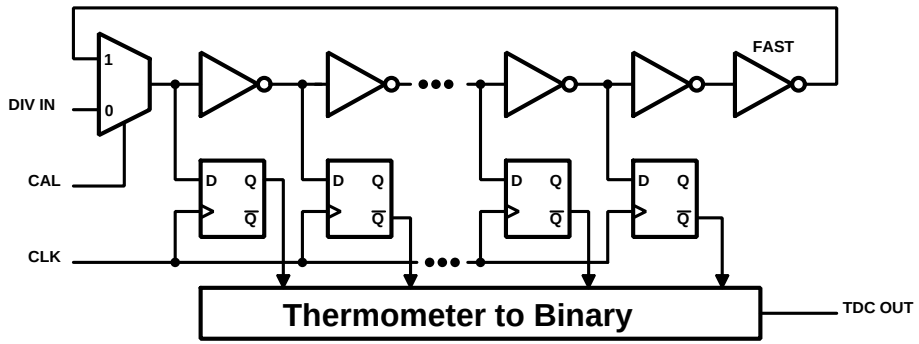
TDC implementation

Architectures

- Two choices for coarse linear phase detector, delay line TDC or synchronous counter.
- **Coarse delay line TDC**
  - **(-)** Complexity grows as $\mathcal{O}(n)$.
  - **(-)** Requires calibration of delay cells (possibly slow).
  - **(-)** Linearity issues, with poor calibration, gain accuracy is a problem.
  - **(-)** Needs divider.
- **Synchronous counter**
  - **(+)** Complexity grows as $\mathcal{O}(log(n))$.
  - **(+)** No calibration, no linearity issues.
  - **(+)** Divider not needed (reduces noise, power?).
  - **(-)** High power, must run as oscillator frequency.
  - **(-)** Resolution limited be to equal to divider modulus.
- Counter approach has *significant* advantages for PLL start up. Will switch of counter after initial lock to save power.

Digital TDC

Coarse Delay line (BAD)



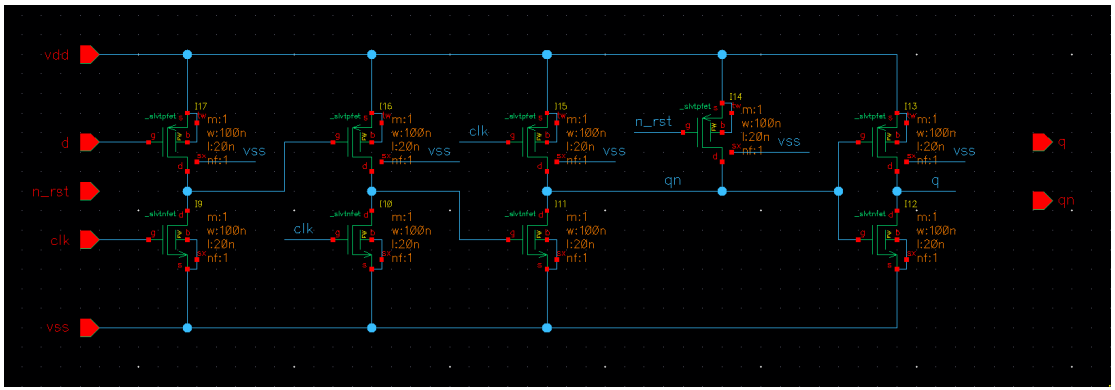
- Standard N-stage inverter-based delay line.
- Complexity is problematic, $\mathcal{O}$(n).
- Use mux to allow for delay line to operate as ring oscillator for calibration.
- Over N reference cycles in ring oscillator mode, a delta in the output word of ΔTDC corresponds to the following gain accuracy of the TDC (use to calibrate):

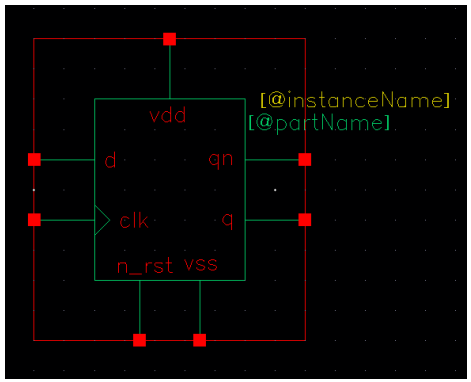
$$\frac{\Delta t_{line}}{T_{ref}} = \frac{\Delta TDC(N_{CYCLES})}{M \cdot N_{CYCLES}} \tag{12}$$

Flip flop for counter schematic

True single phase circuits

- I have implemented the divider using enhanced true single phase clock circuit (E-TSPC) DFFs. These are preferred in PLLs as they provide good energy-delay characteristics, but are not used in logic as the signal quality isn't perfect/limited retention time.
- These are implemented in minimum size for DFM ruleset (100nm/20nm) in SLVT.
- e-TSPC DFF is typically 6 transistors, I have added 1 transistor to implement asynchronous reset and one inverter to get an inverted output.

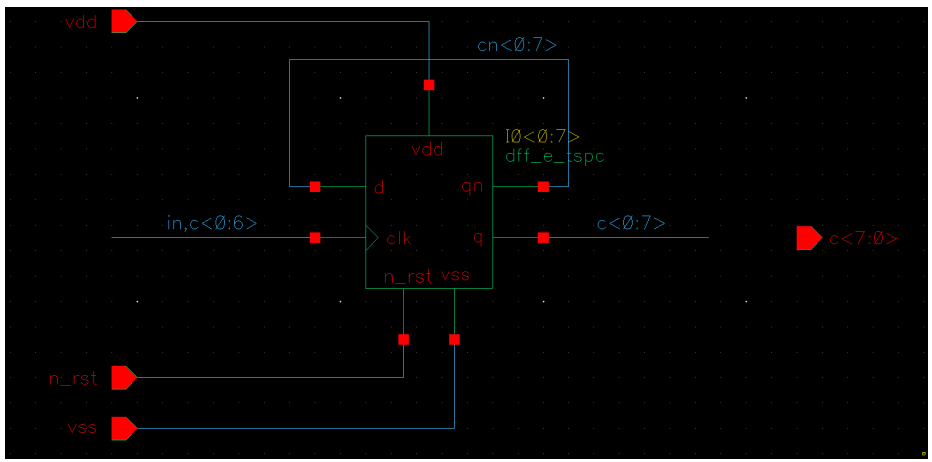




Synchronous counter schematic

Chained DFF's

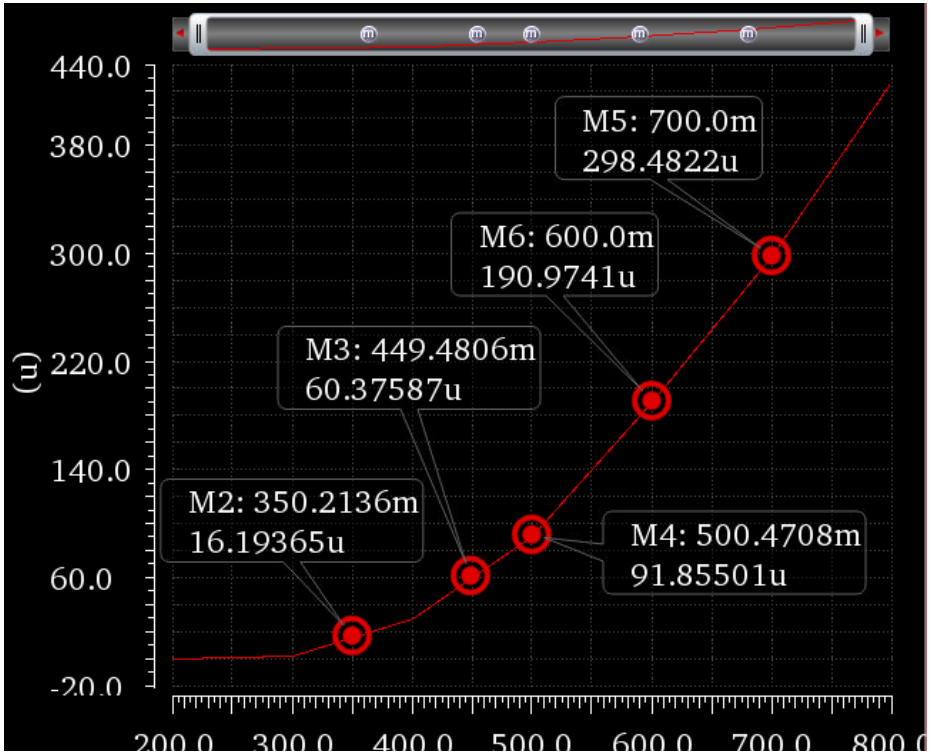
— I require an N=8 bit counter, so this is simply a chain of N e-TSPC DFFs with the output Q of a given stage clocking the next stage. The data input of each DFF is connected to the inverted output Qn so that the output toggles every clock edge.



Synchronous counter power

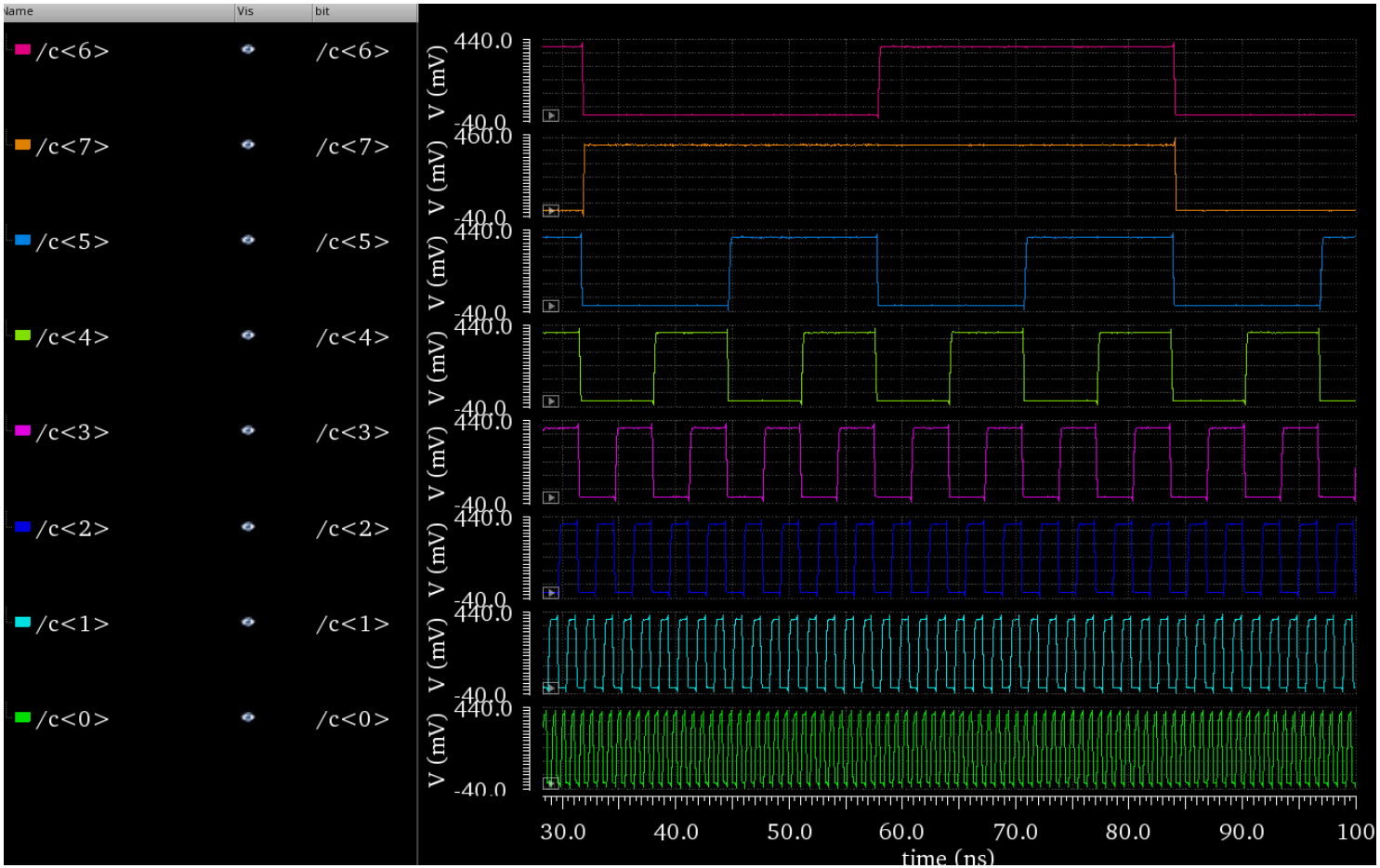
Sweeped Vdd

- Power grows rapidly with Vdd. For < 50 μW, should keep Vdd < 430 mV.
- Cmin = 10 aF.



Synchronous counter output

400 mV Vdd

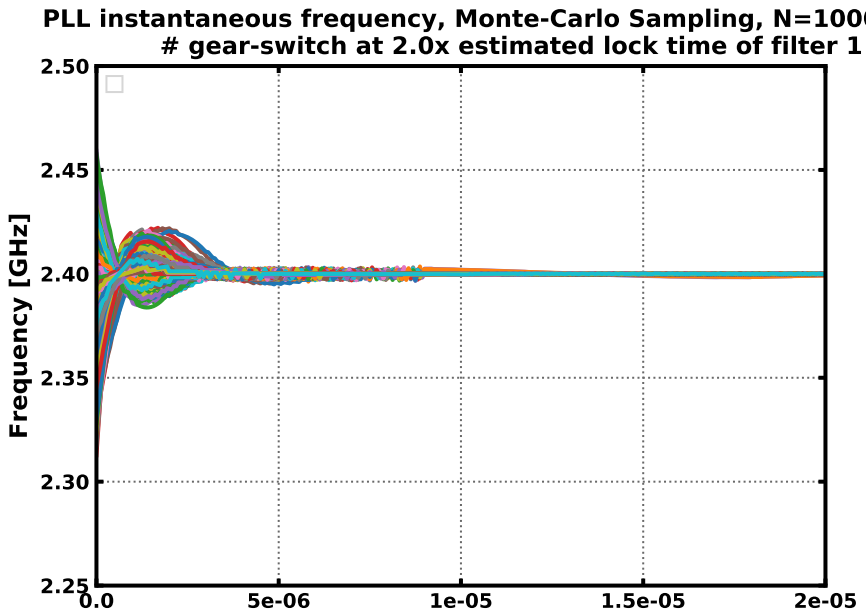


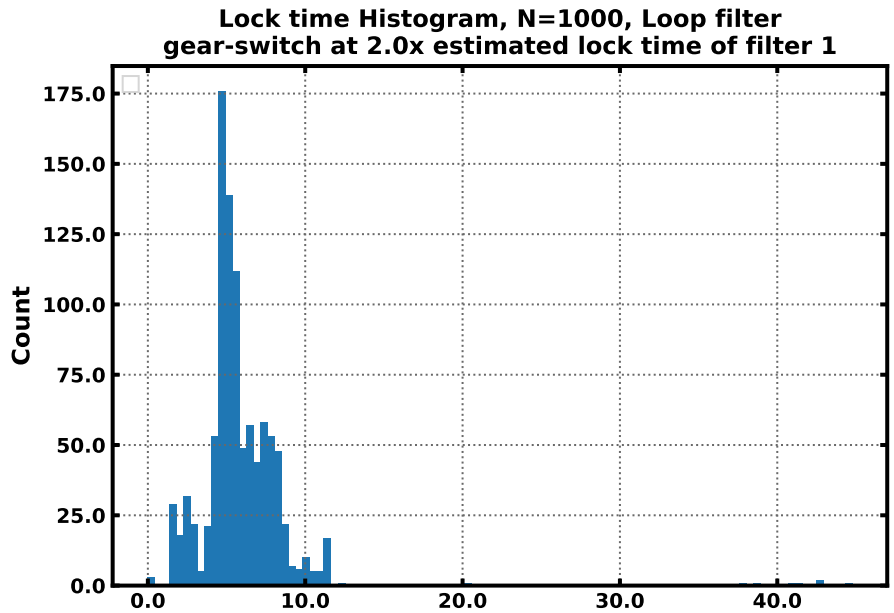
Importance of counter power.

Monte-Carlo simulation of lock time.

— Monte-Carlo simulation with 1000 samples, 20% RMS deviation in K_{DCO}, and 60 MHz (2.5% of nominal) RMS deviation in initial frequency error. Gear switch used for fast locking. **Mean lock time of 6 μs.**

— **High counter power consumption is not problematic**. If PLL on time = 256 μs, counter power is 5x the BB-PD, and the counter is disabled after gear 1 lock, averaged power increases only 9% versus BB-PD alone (i.e. 10 μW $\rightarrow$ 11 μW).





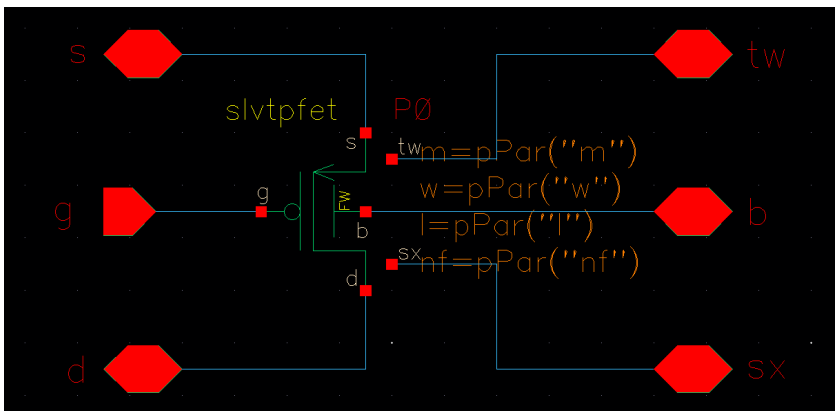
Wrapper for transistors?

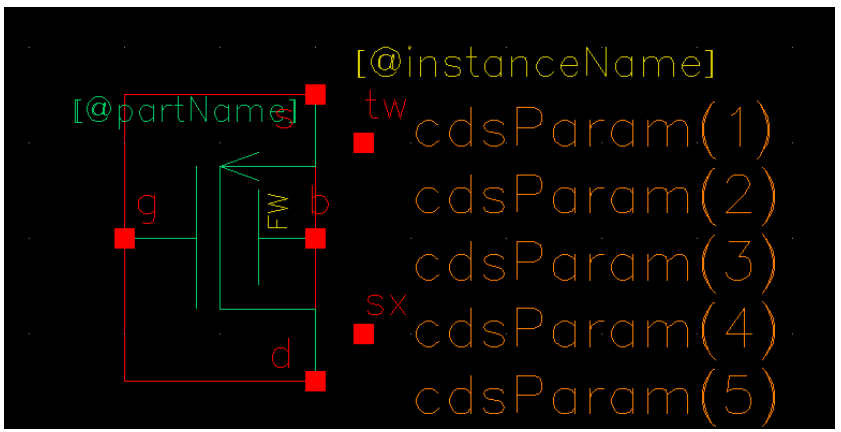
Attempt...

— Trond mentioned before that for a master's project, we should create a sort of wrapper for the transistors to improve portability.

— Should this be fixed unit size device, or can I implement it with pass-through of parameters to the symbol from the technology library (as I have currently done)?

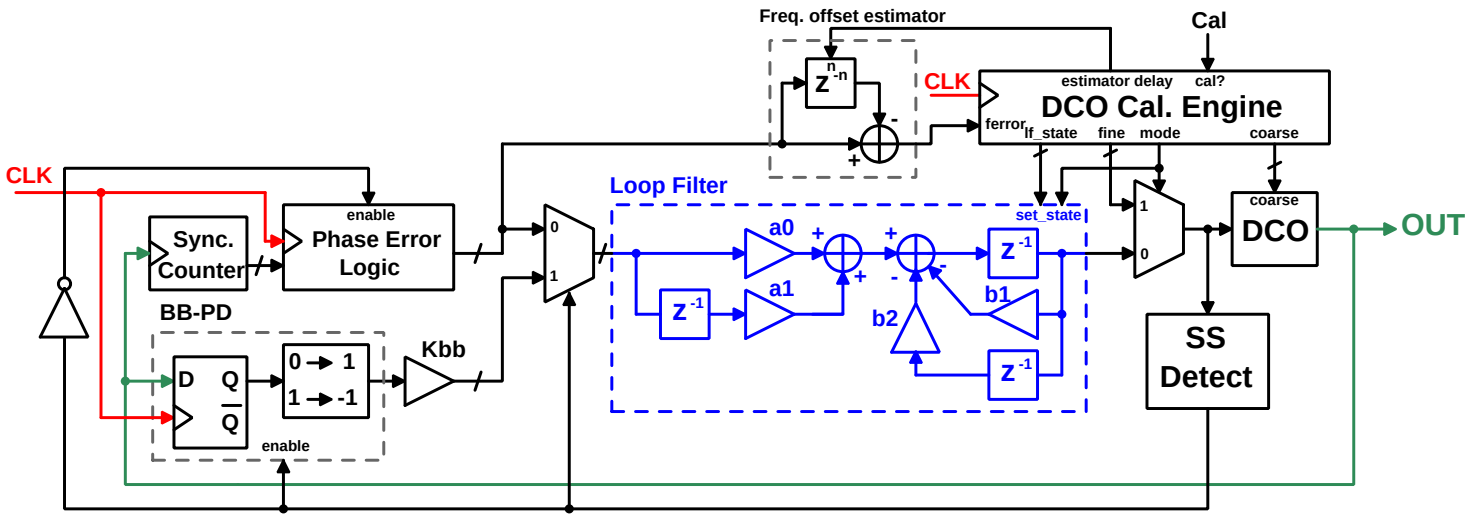
— Also, I will use the 5/6 terminal devices in my schematics (with parasitic diodes for the wells).





Architecture

Block Diagram



Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Divider	Digital (LF)	Other	SUM
50 μW	10 μW	**N/A** ~~10 μW~~	10 μW	$\leq$ **5** ~~10~~ μW	$\leq$ **75** ~~100~~ μW

Specification

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ **75** ~~100~~ μW	μW	Minimize!
FSK BER	$\leq$ 1e-2		GFSK* with f_{dev}=$\pm$250 KHz
CNR	$>$ 20	dBc	Yields **-235** ~~-233~~ dB FOM_{jitter} ideally
Initial Lock Time	$\leq$ 10	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby, f_{error} $<$ **1 MHz**
Lock Δf tolerance	100	kHz	
FOM_{jitter}	$\leq$ -230	dB	**For state of art in size/power**
Area	$<$ 0.01	mm^2	

* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

Specification

Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
~~**TDC resolution**~~	~~$\geq$ 155~~	~~steps/reference cycle~~
DCO gain K_{DCO}	10^4	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	$<$ -80	dBc/Hz @ $\Delta f = 10^6$ Hz, f_c = 2.448 GHz
DCO Power	$\leq$ 50	μW
Digital filter word resolution	$\leq$ 16	bits (power grows as $\mathcal{O}(n^2)$)
BB-PD jitter	$\leq$ 12	ps_{rms}

Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Schem. design: oscillator	LC DCO
12	16.3 - 22.3	Schem. design: divider	TSPC + pulse swallow or sync counter?
13	23.3 - 29.3	Schem. design: Calibration	RTL/schem. for calibration
14	30.3 - 5.4	Flex week - schem. design	Finalize schematic level design
15	6.4 - 12.4	**Easter**	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: **Done** **Current** **Revised**

Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	**Report writing**	
22	25.5 - 31.5	**Report writing**	
23	1.6 - 7.6	**Report writing**	**Deadline 8.6**

Legend: **Done** **Current** **Revised**

References

[1] H. Xu and A. A. Abidi, “Design Methodology for Phase-Locked Loops Using Binary (Bang-Bang) Phase Detectors,” IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 1637–1650, Jul. 2017.

[2] F. Gardner, “Charge-Pump Phase-Lock Loops,” IEEE Transactions on Communications, vol. 28, no. 11, pp. 1849–1858, Nov. 1980, doi: 10.1109/tcom.1980.1094619.