

# **Ultra low power integer-N ADPLL**

## **Master's thesis project - meeting 11**

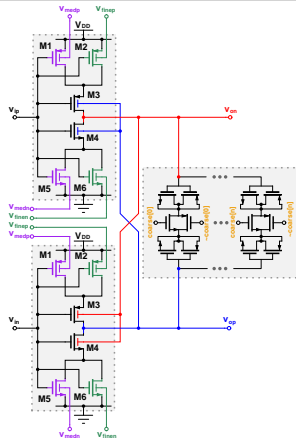
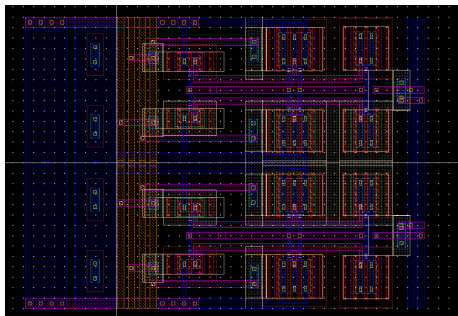
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27 March 2020 (calendar week 13)

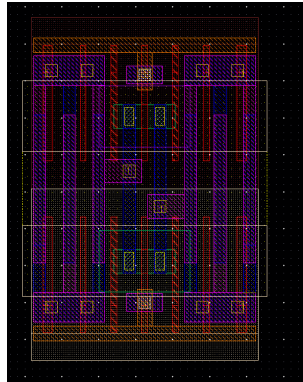
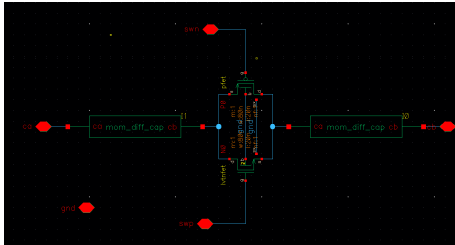
# Layout.

## 816 MHz Pseudo-differential delay cell.



# Layout.

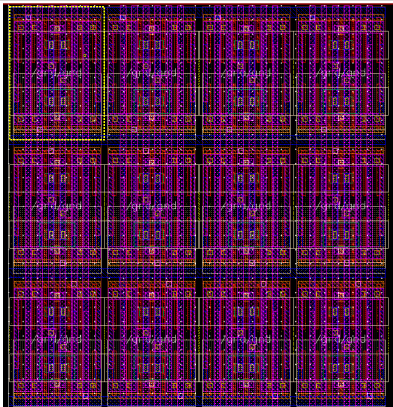
## PVT tuning unit cell.



# Layout.

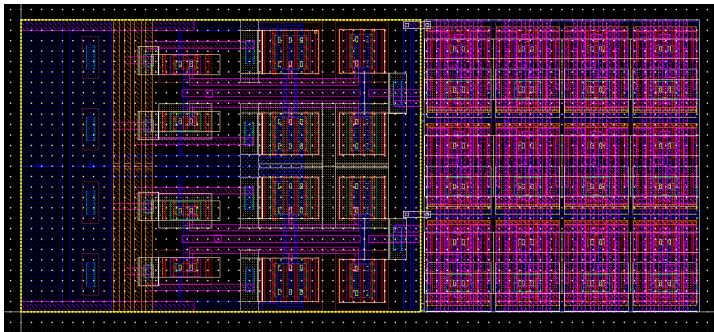
## PVT tuning bank.

- PVT bank comprised of array of 12 (3x4) PVT tuning unit cells.
- Results in approx 15% tuning range (ca 1.2% per unit cell).
- 24 control wires run vertically to the cell boundaries for enabling capacitors.
- $3\mu\text{m} \times 3.5\mu\text{m}$  (WxL)



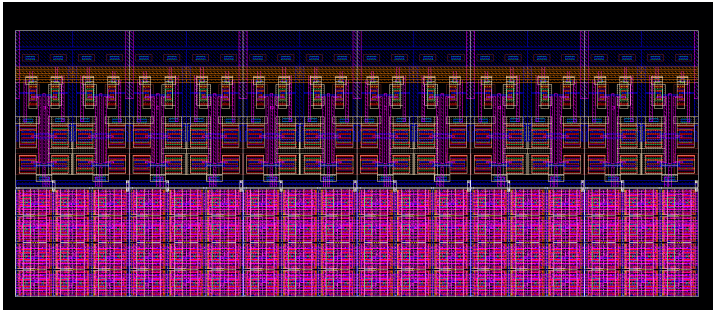
# Layout.

## Full ring oscillator slice layout.



# Layout.

## Full ring oscillator layout.

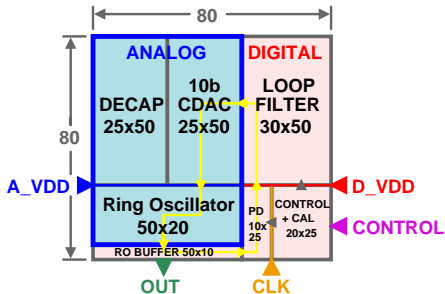


— 78  $\mu$ W, -160.2 dB FOM

# PLL components

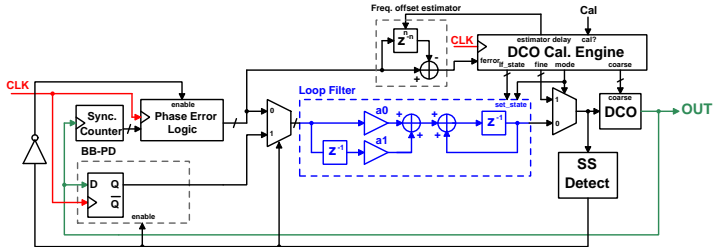
## Loop filter

- Loop filter
- Control/calibration logic
  - Lock detect, gear switching
  - PVT cal
  - Estimate initial DCO control word
- Phase detectors
  - BBPD
  - Synchronous counter (7-8 bit)
  - Counter phase error decoder
- Level shifter (0.5V  $\rightarrow$  0.8V)
- CDACs
  - 5 bit coarse
  - 10 bit fine
- Ring oscillator
- RO buffer



# Architecture

## Block Diagram



## Power Targets (revised)

(Divider not necessary)

DCO	Phase detector	Digital (LF)	Other	SUM
50 $\mu$ W	10 $\mu$ W	10 $\mu$ W	$0 \leq 5 \mu$ W	$\leq 70 + 100 \mu$ W



# Specification

## System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq 70$ <del>75</del> $\mu\text{W}$	$\mu\text{W}$	Minimize!
FSK BER	$\leq 1\text{e-}2$		GFSK* with $f_{dev} = \pm 250$ KHz
CNR	$> 20$	dBc	Yields <b>-235</b> dB FOM <sub>jitter</sub> ideally
Initial Lock Time	$\leq 10$	$\mu\text{s}$	Upon cold start
Re-lock Time	$\leq 5$	$\mu\text{s}$	Coming out of standby, $f_{error} < 1$ MHz
Lock $\Delta f$ tolerance	100	kHz	
FOM <sub>jitter</sub>	$\leq -230$	dB	<b>For state of art in size/power</b>
Area	$< 0.01$	$\text{mm}^2$	

\* Using BT=0.3, 1 MSymbols/s, 4 demodulated symbols averaged per bit to yield 250 kbps.

# Specification

## Component-level specs

Parameter	Value	Unit
Counter range	256 steps	coverage of 150-155
Divider ratio	150-155	(For non-counter based)
<b>TDC-resolution</b>	<b><math>\geq 155</math></b>	<b>steps/reference cycle</b>
DCO gain $K_{DCO}$	$10^4$	Hz/LSB
DCO tuning range	10	MHz
DCO DAC resolution	10	bit
DCO Phase noise	$< -80$	dBc/Hz @ $\Delta f = 10^6$ Hz, $f_c = 2.448$ GHz
DCO Power	$\leq 50$	$\mu W$
Digital filter word resolution	$\leq 16$	bits (power grows as $\mathcal{O}(n^2)$ )
BB-PD jitter	$\leq 12$	ps <sub>rms</sub>

# Time plan (pt. 1)

Week #	Dates	Tasks	Outcomes
4	20.1 - 26.1	Finalize high level modeling	Component level specification
5	27.1 - 2.2	Establish test bench in Virtuoso	With ideal PLL implementation
6	3.2 - 9.2	Schem. design: phase detector	TDC - flash and counter based
7	10.2 - 16.2	Schem. design: phase detector	Bang-bang phase detector
8	17.2 - 23.2	RTL, synthesis, place&route	Digital loop filter
9	24.2 - 1.3	RTL, synthesis, place&route	Digital loop filter
10	2.3 - 8.3	Schem. design: oscillator	Ring DCO
11	9.3 - 15.3	Layout: oscillator	
12	16.3 - 22.3	CDAC/Ring oscillator	Layout
13	23.3 - 29.3	CDAC/Ring oscillator	Layout
14	30.3 - 5.4	Calibration/control logic	RTL, synth, PnR for calibration
15	6.4 - 12.4	Easter	-
16	13.4 - 19.4	Layout	Phase detector
17	20.4 - 26.4	Layout	Oscillator

Legend: Done Current Revised

# Time plan (pt. 2)

Week #	Dates	Tasks	Outcomes
18	27.4 - 3.5	Layout	Divider/calibration
19	4.5 - 10.5	Layout	Finalization/system integration
20	11.5 - 17.5	Flex week (layout) OR yield improvement	Depending on progress
21	18.5 - 24.5	Report writing	
22	25.5 - 31.5	Report writing	
23	1.6 - 7.6	Report writing	Deadline 8.6

Legend: Done Current Revised

# References

- [1] L. Dai and R. Harjani, "Analysis and design of low-phase-noise ring oscillators," ISLPED'00: Proceedings of the 2000 International Symposium on Low Power Electronics and Design (Cat. No.00TH8514), Rapallo, Italy, 2000, pp. 289-294. doi: 10.1145/344166.344639
- [2] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," in IEEE Journal of Solid-State Circuits, vol. 33, no. 2, pp. 179-194, Feb. 1998.
- [3] G. Jacquemod et al., "Study and reduction of variability in 28 nm FDSOI technology," 2015 International Workshop on CMOS Variability (VARI), Salvador, 2015, pp. 19-22.