

Ultra-Low Power PLL for Wake-up Receiver Applications

Specialization Project Progress - 2nd Week

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6 September 2019 (Week 36)

This Week

Timeline Tasks

- **Primary:** Review PLL literature/theory to get up to speed on project.
 - Main topic of interest is design of digital PLLs.
 - Decide starting point for modeling based from this.
 - Reviewed Texts:
 - "Phase Locked Loops: Design, Simulation and Applications", 6th Edition, R.E. Best.
 - "PLL Performance, Simulation and Design", 5th Edition, D. Banerjee.

System Modeling/Simulation

Initial Approach

- Started writing Python code to simulate digital PLL.
 - Most familiar for me (I have modelled CDRs in Python before).
 - Simple to implement digital filters with Python Control Systems Library.
 - Also - Convenient stability analysis.
- Decided starting point:
 - Model DCO based on physical phase-noise limit of ring-oscillators.
 - Model loop filter as digital IIR second-order LPF (approximate second-order type-II analog PLL).
 - Ideal divider and TDC.
- Investigate (to determine component requirements):
 - Loop-BW to achieve PN requirements. Closed-loop sensitivity analysis:
 - TDC phase noise significant at $f < BW$, determine limits for this.

System Modeling/Simulation

Initial Approach (continued)

- Investigate (continued):
 - Quantization, linearity impact of TDC & DCO on phase noise.
 - Determine number of bits required for each, and non-linearity limits.
 - Loop filter implementations (IIR vs FIR), order & type.
 - Evaluate stability, lock time, operating region to meet requirements.
 - Digital data path requirements to implement filter.
 - Algorithm/state machine for handling continuity of fine/coarse DCO ranging.
 - Previous two lead to Verilog description.
- **Final Outcomes:**
 - Full design constraints for PLL components, sufficient to allow schematic-level implementation.

System Modeling/Simulation

Implementation in Cadence

- When initial modeling/simulation satisfactory, translate design into a setup within Cadence.
 - Implement using Verilog-A, ahdlLib components?
- Will act as known-good test bench for testing transistor-level implementations of components in future design stages.
 - Replace element by element until fully functioning at transistor level.

Specification (unchanged)

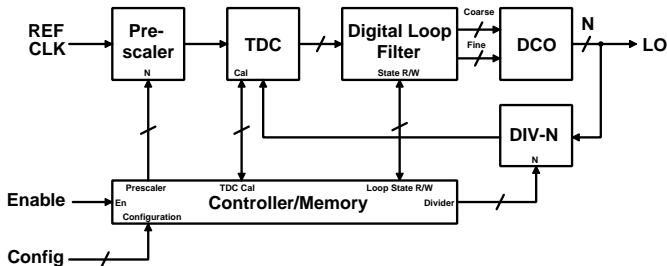
Preliminary Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	≤ 100	μW	
Residual FM	≤ 107	kHz_{RMS}	$\text{BER} \leq 1\text{e-}2$, $f_{\text{dev}} = \pm 250 \text{ KHz}$
Initial Lock Time	≤ 50	μs	Upon cold start
Re-lock Time	≤ 5	μs	Coming out of standby
Bandwidth	100	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

Architecture (unchanged)

Block Diagram



Power Targets

DCO	TDC	Divider	Other	SUM
70 μ W	20 μ W	10 μ W	$\ll 1$ μ W	100 μ W

Autumn Timeline

Week Number	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	Ideal (ahdlLib?) implementation in Cadence of PLL
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Circuit Implementation	Digital logic (schematic)
44	28.10 - 3.11	Circuit Implementation	DCO (schematic)
45	4.11 - 10.11	Circuit Implementation	Divider/other (schematic)
46	11.11 - 17.11	Circuit Implementation (TDC)	
47	18.11 - 24.11	Circuit Implementation (TDC)	TDC (schematic)
48	25.11 - 1.12	Full Circuit testing	Testbenches, find bugs, design fixes
49	2.12 - 8.12	Full Circuit testing	Design Fixes/iteration
50	9.12 - 15.12	–	–

*I will write the report simultaneously with the work.

Project Phases

Autumn 2019

- System modeling and simulation.
 - Learn PLL theory in detail
 - Evaluate feasibility of PLL architectures (counter, TDC-based)
 - Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
 - Determine digital logic for loop filter, validate stability and lock time performance.
- Research ultra-low power circuit topologies to implement system components that will meet determined requirements.
- Translate component-level specifications into schematic-level circuit designs.
 - Try, fail, try again until functional at schematic level.
 - I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

- Finalize schematic-level design.
- Establish thorough tests for PLL performance (automated?) to help in layout.
- Layout of PLL.
 - Design iteration until design specs met.
 - Probably very time consuming.
- Full characterization/validation of design performance.
 - Comprehensive Corners/Monte-Carlo testing (time consuming??)
 - More design iteration if new issues crop up...
- Thesis paper writing.