Ultra-Low Power PLL for Wake-up Receiver Applications

Specialization Project Progress - 10th Week

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Timeline

Week	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	Loop filter, DCO, TDC, calibration
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Spur analysis, filter automation	
44	28.10 - 3.11	Filter automation, SNR estimation	
45	4.11 - 10.11	Variation analysis, flicker noise	Histograms/yield estimates
46	11.11 - 17.11	Real DCO sensitivity, TDC/divider jitter	Simlate ring-DCO in Virtuoso
47	18.11 - 24.11	PLL + Radio simulation	BER estimate
48	25.11 - 1.12	Agglomerate into cohesive framework	(I have an Exam on 30.11)
49	2.12 - 8.12	Finish framework, report writing	
50	9.12 - 15.12	Report writing	Complete before 15.12

Legend: **Done** **Current** **Revised**

Timeline Tasks

This week

- **Filter design automation:**
  - Was very slow, changed gradient-descent optimization approach.
- **Baseband SNR estimation**:
  - Thought of way to estimate SNR of radio based on PLL phase noise and modulation PSD.
    - Can determine BER based on radio system (modulation, bitrate and thus Eb/No)
  - Utilize SNR estimate in optimization of PLL loop filter.
    - Design to maximize received SNR.
- **Variation analysis:**
  - Moved to next week due to SNR work.

Filter automation

Gradient descent optimization

— Old approach used stepping method which tried to select optimal step size.
  - Computing optimal step size is computationally expensive
  - This method is actually slow than methods that use sub-optimal step size

— Came across different method for selecting step size based *only* on the gradient and cost function independent variables for current and previous iterations.

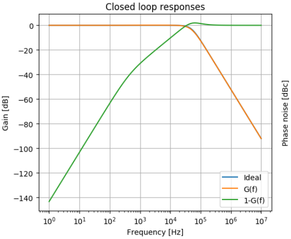
$$\gamma_n = \frac{\left|(\mathbf{x}_n - \mathbf{x}_{n-1})^T \left[\nabla F(\mathbf{x}_n) - \nabla F(\mathbf{x}_{n-1})\right]\right|}{\left\|\nabla F(\mathbf{x}_n) - \nabla F(\mathbf{x}_{n-1})\right\|^2}$$

  - Very fast, despite using sub-optimal step size.
  - Ca. 100x speed up in filter optimizer

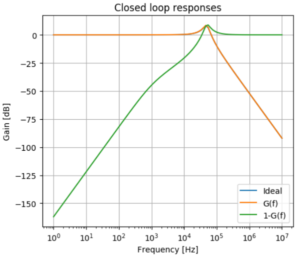
Filter automation

Gradient descent optimization

— Now can optimize with many more iterations, matched closed loop response now is very close.



(a) $\zeta = 0.707$



(b) $\zeta = 0.2$

SNR estimation of radio with PLL

Theory

- Considering generalized PSK/FSK modulation in the phase domain, the phase of such a signal after direct-to-DC downconversion with local oscillator with phase noise $\phi_n(t)$ is:

$$\phi(t) = \phi_{mod}(t) + \phi_n(t) \tag{1}$$

- Given the mean of the phase noise $\langle \phi_n(t) \rangle = 0$ and $|\phi_n(t)| << 1$, the amplitude of the signal can be approximated as:

$$\Re\{e^{\phi(t)}\} = \Re\{e^{\phi_{mod}(t)} e^{\phi_n(t)}\} \approx \Re\{e^{\phi_{mod}(t)}(1 + j\phi_n(t))\} \tag{2}$$

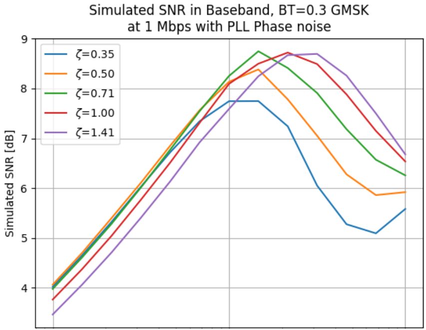
$$= \cos(\phi_{mod}(t)) - \phi_n(t)\sin(\phi_{mod}(t)) \tag{3}$$

- We can treat the downconverted signal in two parts, the main signal, $\cos(\phi_{mod}(t))$ (which is unchanged), and an orthogonal noise component that is the phase noise signal multiplied with a phase shifted version of the modulated signal ($\sin(\phi_{mod}(t))$).

SNR estimation of radio with PLL

Application

- In the frequency domain, the noise can be calculated as convolution of the modulated signal with the PLL phase noise
- The in band power then can be calculated for both the signal and noise to yield SNR:



Specification (unchanged)

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100	μW	
FSK BER	$\leq$ 1e-2		2FSK with f_{dev}=$\pm$250 KHz
Initial Lock Time	$\leq$ 50	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby
Bandwidth	50	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

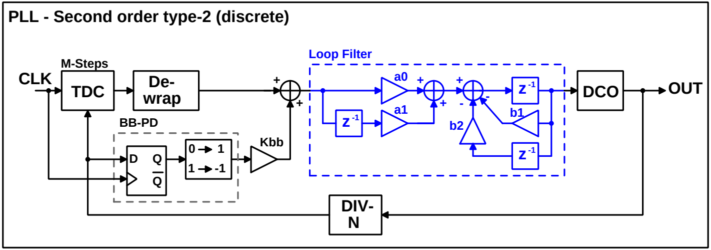
Specification (unchanged)

PLL Component Performance Targets

Parameter	Value	Unit	Notes
DCO LSB Resolution	≤ 50	kHz	Determined from quantization noise.
DCO DNL	< 1	LSB	Ensures monotonicity
TDC Resolution	0.95	ns	
TDC Resolution (bits)	6	bits	

Architecture (updated)

Block Diagram



Power Targets

DCO	TDC	Divider	Other	SUM
70 μW	20 μW	10 μW	$<<$ 1 μW	100 μW

Project Phases

Autumn 2019

— System modeling and simulation.

- Learn PLL theory in detail
- Evaluate feasability of PLL architectures (counter, TDC-based)
- Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
- Determine digital logic for loop filter, validate stability and lock time performance.

— Research ultra-low power circuit topologies to implement system components that will meet determined requirements.

— Translate component-level specifications into schematic-level circuit designs.

- Try, fail, try again until functional at schematic level.
    — I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

- — Finalize schematic-level design.
- — Estabilish thorough tests for PLL performance (automated?) to help in layout.
- — Layout of PLL.
  - Design iteration until design specs met.
  - Probably very time consuming.
- — Full characterization/validation of design performance.
  - Comprehensive Corners/Monte-Carlo testing (time consuming??)
  - More design iteration if new issues crop up...
- — Thesis paper writing.

References

[1] "Ultra-Low Power Wake-Up Receivers for Wireless Sensor Networks", N. Pletcher, J.M Rabaey, 2008.
`http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-59.html`