Ultra-Low Power PLL for Wake-up Receiver Applications

Specialization Project Progress - 5th Week

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27 September 2019 (Week 39)

Autumn Timeline

Week Number	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	**Loop filter,** Ideal implementation in Cadence
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Circuit Implementation	Digital logic (schematic)
44	28.10 - 3.11	Circuit Implementation	DCO (schematic)
45	4.11 - 10.11	Circuit Implementation	Divider/other (schematic)
46	11.11 - 17.11	Circuit Implementation (TDC)	
47	18.11 - 24.11	Circuit Implementation (TDC)	TDC (schematic)
48	25.11 - 1.12	Full Circuit testing	Testbenches, find bugs, design fixes
49	2.12 - 8.12	Full Circuit testing	Design Fixes/iteration
50	9.12 - 15.12	–	–

Legend: **Done** **Current** **Revised**

Timeline Tasks

This week

— **Primary:** Loop analysis, requirements definition

- Design open loop filter design to meet closed loop requirements.
  - — Dependent on DCO properties (k_{DCO}, f_0, tuning range).
  - — Difference equation implementing discrete time 2nd order IIR filter.
- Datapath requirements (fixed-point resolution)

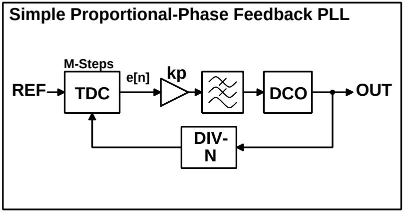
Next week - Revised

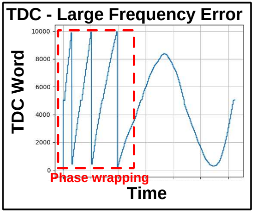
— **Primary:** Ideal component PLL implementation in Cadence, continue loop filter work.

- Ideal component PLL implementation is not a lot of work.
- Loop filter very critical, spend more time on this.
  - — Need to make Verilog description of loop filter for simulation in Cadence.

Loop Filter

Original Attempt





— Started with simple PLL loop with proportional-phase fed into loop filter (LF).

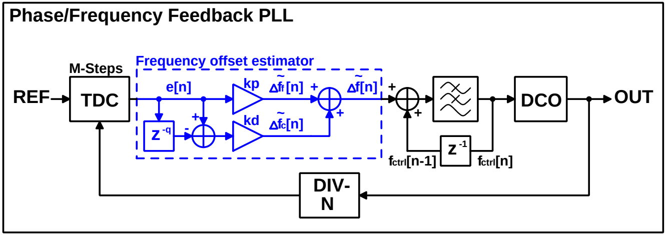
- Not stable at large frequency offset, due to frequency wrapping. At the TDC:

$$\Delta\phi = \frac{2\pi\Delta f T}{N} \rightarrow T_{wrap} = \frac{N}{\Delta f} \tag{1}$$

- Upon cold start, Δf is expected to be up to 100 MHz, N=150 $\rightarrow T_{wrap} = 1.5\ \mu$s
  — $f_{wrap} \sim 600$ kHz, this is unstable with a loop bandwidth of 100 kHz.
- Must opt for alternate loop structure.

Loop Filter

New Approach



— Two-fold approach: utilize propotional-phase and coarse frequency offset estimation in feedback.

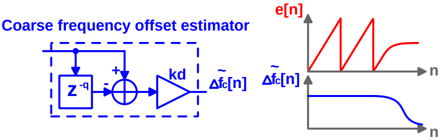
- Coarse frequency estimator to handle high frequency offset (e.g. cold start-up).
- Proportional-phase for near steady state. Acts like fine frequency estimator.

— Offset estimates are summed with previous oscillator tuning word (OTW, also f_{ctrl} here), then low passed filtered to yield new OTW.

- Low pass filter loop keeps steady state.

Loop Filter

Coarse frequency offset estimation



— **Coarse frequency estimation:** Given M-step TDC, outputting phase error signal e_ϕ[n], and a divider modulus N

$$\Delta\phi_{DCO}[n;q] = N\cdot\Delta\phi_{REF}[n] = 2\pi\frac{N}{M}\left(e_\phi[n]-e_\phi[n-q]\right), \qquad \Delta\phi_{DCO}[n;q] = \Delta\omega_{DCO}[n]qT_{ref} = 2\pi q\frac{\Delta f_{DCO}}{f_{ref}} \tag{2}$$

$$\Delta f_{DCO} = \frac{f_{ref}}{q}\frac{N}{M}\left(e_\phi[n]-e_\phi[n-q]\right) \tag{3}$$

— Is a discrete differentiator, with gain coeficient to convert $d\phi/dt$ to frequency.

- Design logic to handle phase wrapping.
- Useful in coarse frequency range calibration. Can detect fast if frequency offset too large.
- Delay q is used to increase frequency resolution.

Loop Filter

Coarse frequency offset estimation - continued

— Given DCO gain K_{DCO}, the gain K_d of the filter is:

$$K_d = \frac{f_{ref}}{qK_{DCO}} \frac{N}{M} \left(e_\phi[n] - e_\phi[n-q]\right) \tag{4}$$

— Disable the coarse estimator off if $e_\phi[n] - e_\phi[n-q]$ < some threshold:

- Offset small enough, allow to run as classical phase-detector mode.

Fine frequency offset estimation

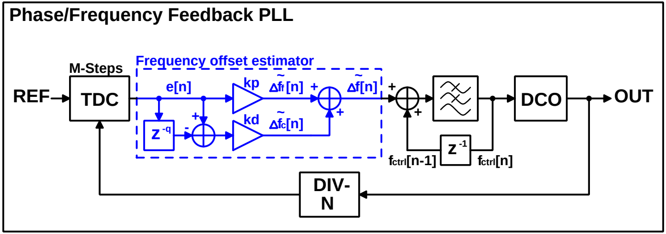
— Proportional signal of phase error to estimate frequency error.

— Used in near-steady state. Loop will regulate to keep phase locked.

— Classical PLL operating mode.

Loop Filter

Loop Filter Gain Coefficients



— When running in proportional-only feedback mode, the open loop gain $A(f)$ is:

$$A(f) = K_p \frac{M}{N} \frac{K_{LPF}}{s + \omega_{LPF} - K_{LPF}} \frac{2\pi K_{DCO}}{s} \tag{5}$$

— The closed loop gain is therefore (continuous):

$$G(f) = \frac{A(f)}{1 + A(f)} = \frac{2\pi M K_p K_{LPF} K_{DCO}/N}{s^2 + s(\omega_{LPF-K_{LPF}})/N + 2\pi M K_p K_{LPF} K_{DCO}/N} \tag{6}$$

Loop Filter

Loop Filter Gain Coefficients

— The form of a second order low pass filter is, with natural frequency ω_n and damping coefficient ζ:

$$H_{LPF}(f) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{7}$$

— Setting $H_{LPF}(f) = G(f)$, equivalencies for ω_n and ζ are found:

$$\omega_n = \sqrt{2\pi M K_p K_{LPF} K_{DCO}/N} \tag{8}$$

$$\zeta = \frac{\omega_{LPF-K_{LPF}}}{2\sqrt{2\pi M N K_p K_{LPF} K_{DCO}}} \tag{9}$$

— The Butterworth closed loop response with 100 kHz bandwidth, $\omega_n \sim 2\pi \cdot 100Khz$, $\zeta = 0.707$.

— Coefficients K_{LPF}, K_p, ω_n can be solved computationally.

— Need to reformulate in Z-domain.

Frequency Calibration

Coarse frequency calibration algorithm

- Ring oscillator DCO will have large variations in frequency due to PVT variation.
- Will have bank of coarse capacitance values to adjust range of oscillator.
- Utilize coarse frequency estimator in tuning.
- DCO is has a tuning range of Δf.

Coarse tuning state machine (as loop pseudo-code)

1. Set $C_{coarse} = 0$
2. Reset PLL
3. Estimate Frequency offset $\rightarrow f_{offset}$
4. **If** $f_{offset} > \Delta f/4$ **and** $f_{offset} \leq 3\Delta f/2$: **break**
5. C_{coarse} += 1
6. **Goto** 2

Specification (unchanged)

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100	μW	
Residual FM	$\leq$ 107	kHz_{RMS}	BER $\leq$ 1e-2, f_{dev}=$\pm$250 KHz
Initial Lock Time	$\leq$ 50	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby
Bandwidth	100	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

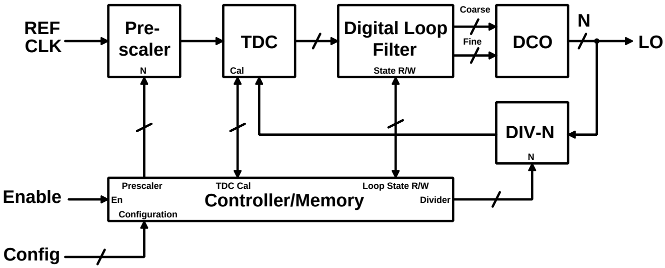
Specification (new)

PLL Component Performance Targets

Parameter	Value	Unit	Notes
DCO LSB Resolution	≤ 50	kHz	Determined from quantization noise.
DCO DNL	< 1	LSB	Ensures monotonicity
TDC Resolution	≤ 3.8	ns	
TDC Resolution (bits)	≥ 4.03	bits	

Architecture (unchanged)

Block Diagram



Power Targets

DCO	TDC	Divider	Other	SUM
70 μW	20 μW	10 μW	$<<$ 1 μW	100 μW

Project Phases

Autumn 2019

— System modeling and simulation.

- Learn PLL theory in detail
- Evaluate feasability of PLL architectures (counter, TDC-based)
- Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
- Determine digital logic for loop filter, validate stability and lock time performance.

— Research ultra-low power circuit topologies to implement system components that will meet determined requirements.

— Translate component-level specifications into schematic-level circuit designs.

- Try, fail, try again until functional at schematic level.
  - — I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

- — Finalize schematic-level design.
- — Estabilish thorough tests for PLL performance (automated?) to help in layout.
- — Layout of PLL.
  - Design iteration until design specs met.
  - Probably very time consuming.
- — Full characterization/validation of design performance.
  - Comprehensive Corners/Monte-Carlo testing (time consuming??)
  - More design iteration if new issues crop up...
- — Thesis paper writing.