Ultra-Low Power PLL for Wake-up Receiver Applications

Specialization Project Progress - 8th Week

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Autumn Timeline

Week	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	Loop filter, DCO, TDC, calibration
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies, Ideal Virtuoso implementation
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Circuit Implementation	Digital logic (schematic)
44	28.10 - 3.11	Circuit Implementation	DCO (schematic)
45	4.11 - 10.11	Circuit Implementation	Divider/other (schematic)
46	11.11 - 17.11	Circuit Implementation (TDC)	
47	18.11 - 24.11	Circuit Implementation (TDC)	TDC (schematic)
48	25.11 - 1.12	Full Circuit testing	Testbenches, find bugs, design fixes
49	2.12 - 8.12	Full Circuit testing	Design Fixes/iteration
50	9.12 - 15.12	–	–

Legend: **Done** **Current** **Revised**

Timeline Tasks

This week

— **TDC/Phase detector**

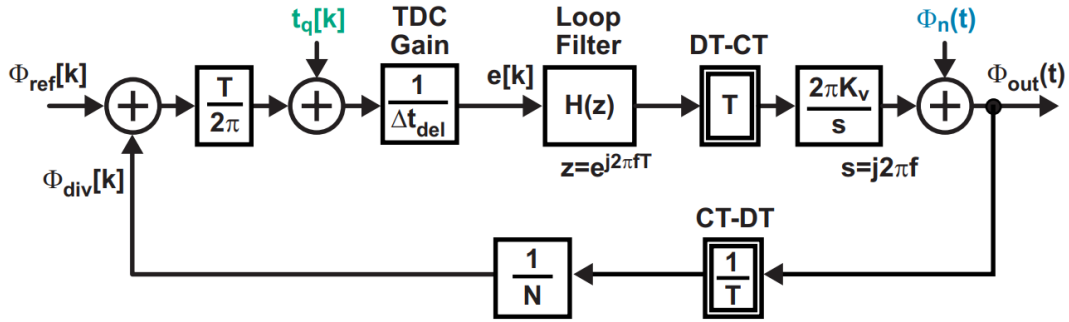
- New hybrid architecture using TDC and digital bang-bang phase detector to overcome resolution deficiencies.
- Already talked about topologies two weeks ago.

— **Python Simulation**:

- Variance of K_{DCO} to analyze stability and effects on start-up.
- Added quantization to loop filter model.
- Added in hybrid TDC and digital bang-bang phase detector.

TDC model limitations

Continuous approximation model



— Have been using continuous approximation of PLL loop to model phase noise dynamics.

— Phase error here is *instantly* available with added quantization noise.

— **Reality:** Low TDC resolution not manifested accurately.

- There is latency - Phase error must accumalate over many reference cycles until it is large enough to increment TDC by 1 LSB.

— Time to increment 1 LSB for a frequency error Δf is below. E.g. Δf = 50 kHz, M=64, N=150 yields 47 μs latency, or 750 reference cycles at 16 MHz.

$$t = \frac{N}{M \cdot \Delta f} \tag{1}$$

Overcoming TDC limitations

Issue of low TDC resolution

— Low TDC resolution limits ability to track random phase walk (principal phase noise component).

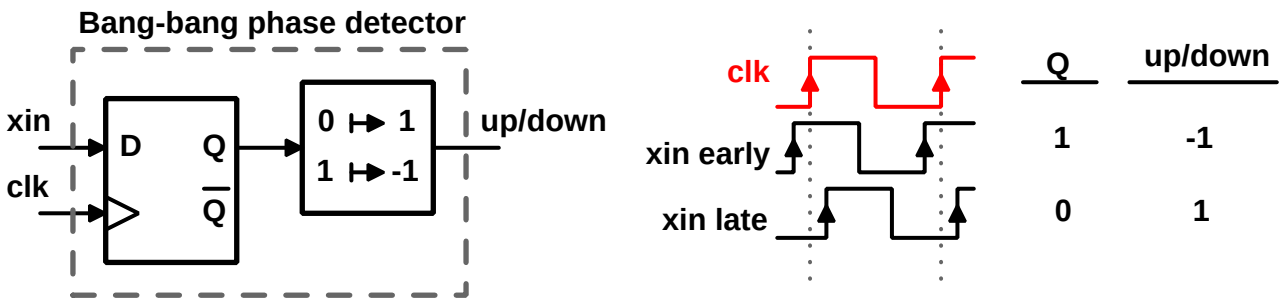
— **TDC steps M** $>>$ **Divider N** for TDC response time to frequency error Δf to be much less than period of Δf. This allows for the frequency error due to phase walk to be corrected before it contributes to the phase noise spectrum.

— If N=150, TDC bits $>>$ 7.2.

- This is impractical.
- Delay line TDC with ca. 150 stages would be problematic.
- Counter based TDC limited to exactly M=N.

Overcoming TDC limitations

Bang-bang phase detector



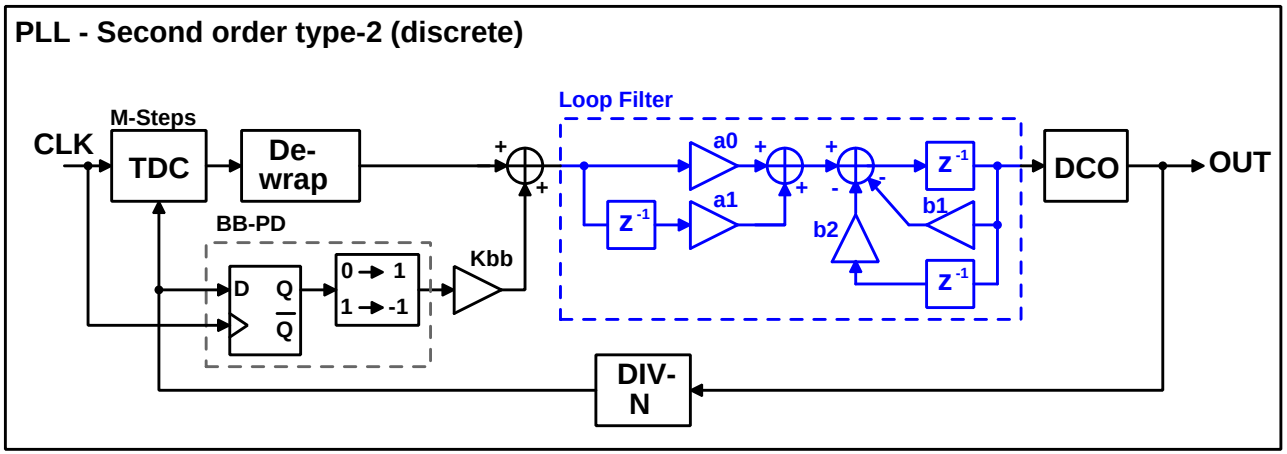
— Need a way to incorporate more instantaneous phase feedback, enter the **bang-bang phase detector** (BB-PD).
  - Bang-bang detector samples every cycle, measuring if the input edge is late or early relative to the clock.

— Basic implementation is a D flip-flop.

— To correct phase error (if small in magnitude):
  - Early input $\rightarrow$ decrement oscillator frequency
  - Late input $\rightarrow$ incremenent oscillator frequency

Overcoming TDC limitations

Hybrid detector



— Combine TDC and bang-bang phase detector to yield better overall phase detector.
- TDC good for achieving fast lock with large frequency offset.
- Bang-bang good for steady-state tracking.

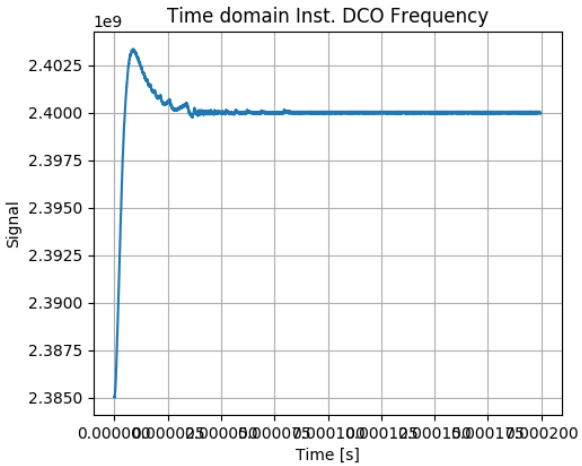
— In phase error signal, TDC sets integer part of signal, BB-PD is fractional.
- Near steady state, TDC signal is 0, so BB-PD dominates.

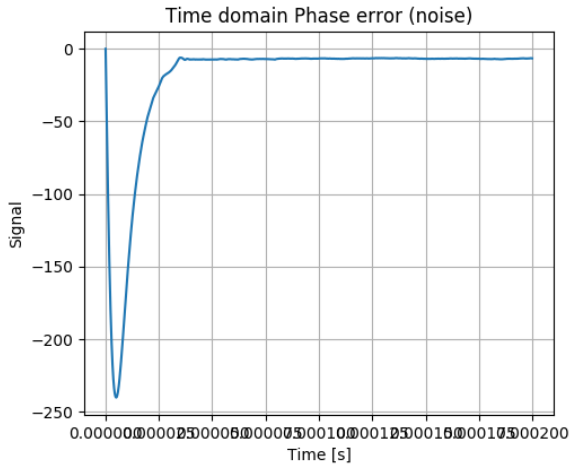
— Remainder of PLL is same as before.

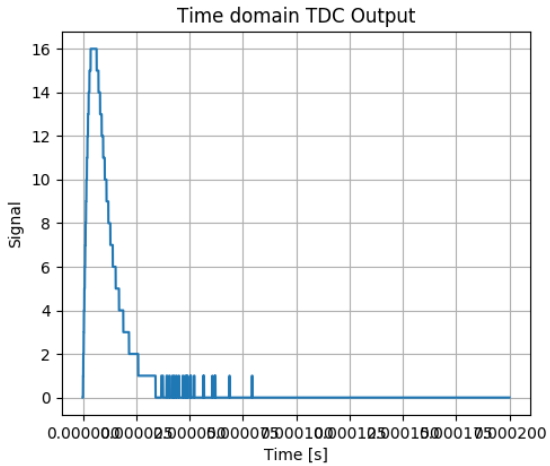
Overcoming TDC limitations

Example TDC out with low resolution.

- Simulated 2.4 GHz PLL, with 16 MHz reference, 50 kHz bandwidth, 64 TDC steps.
- Does a good job locking from large offset, bad phase error in steady state.
- Noticably no tracking of small phase variations (phase noise) in steady state.

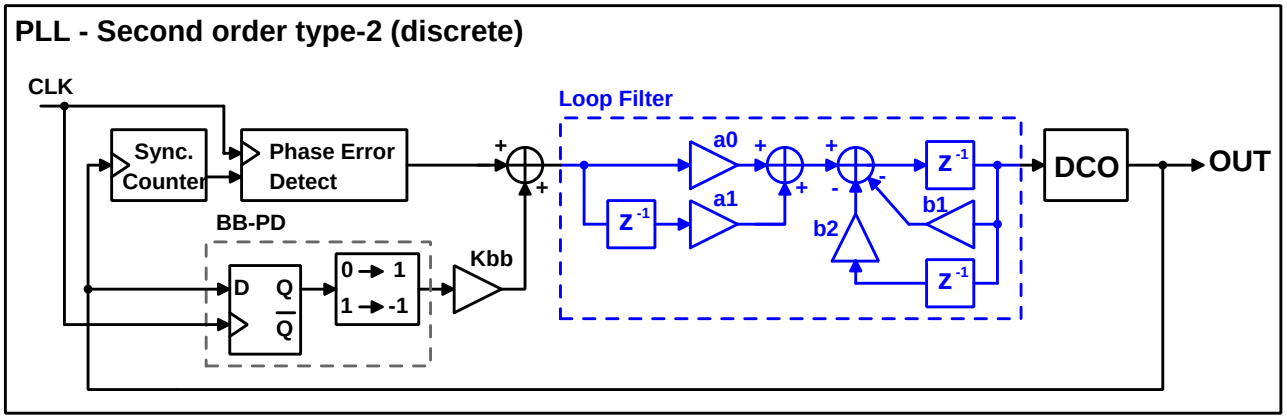






Overcoming TDC limitations

BB-PD with counter-based TDC

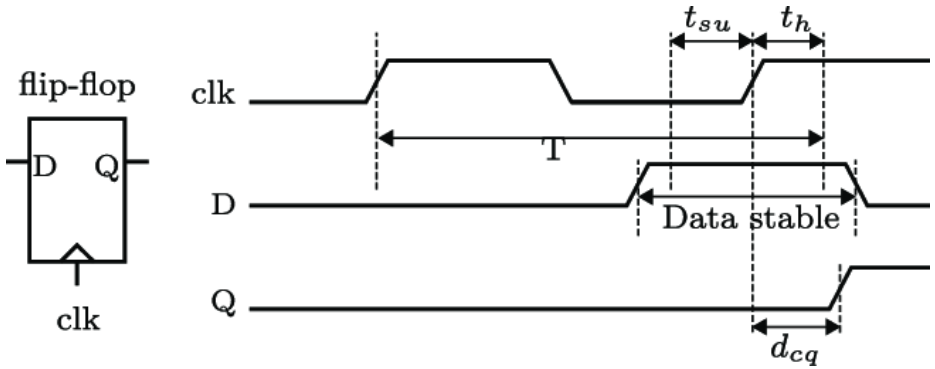


— Counter-based TDC has no divider, connect BB-PD direct to DCO output.

— Disable synchronous counter and only use BB-PD near lock to save power?

Overcoming TDC limitations

BB-PD gain selection



— Regardless of phase error magnitude, BB-PD output will be fixed magnitude. How do we set K_{BB}?

- To achieve maximum resolution (lowest phase noise), K_{BB} should be defined by the minimum time difference resolvable by the BB-PD.
- If faster settling is need, increase K_{BB}

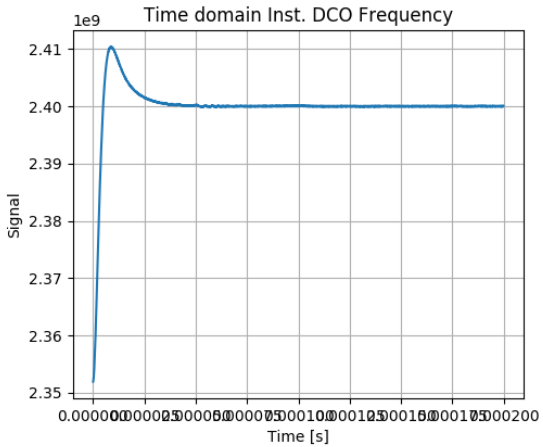
— Minimum effective temporal resolution of BB-PD is given by set-up and hold time requirements of flip-flop for deterministic output. So for use with a M-step TDC:

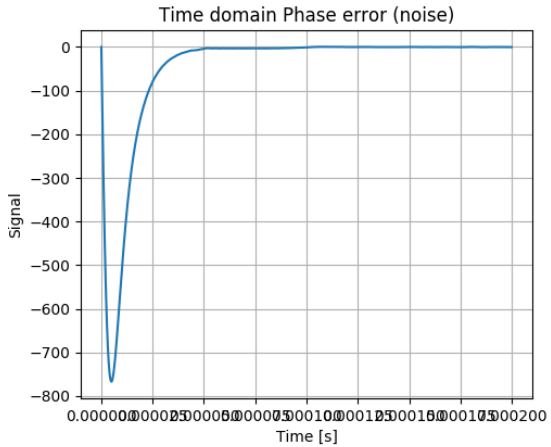
$$K_{BB} \geq M \cdot f_{clk}(t_{su} + t_h) \tag{2}$$

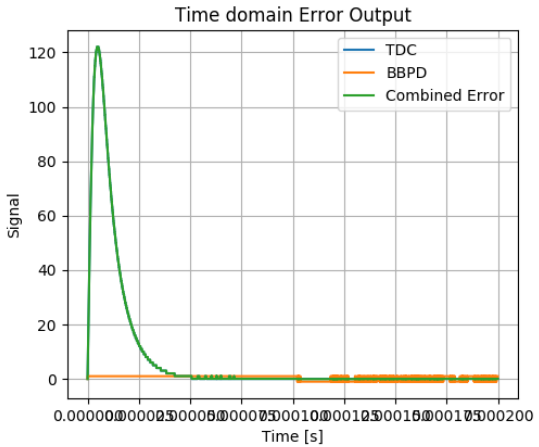
PLL Simulation with BB-PD

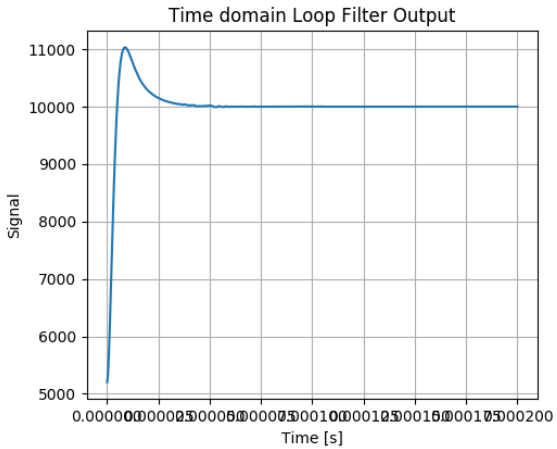
Counter based TDC/divider.

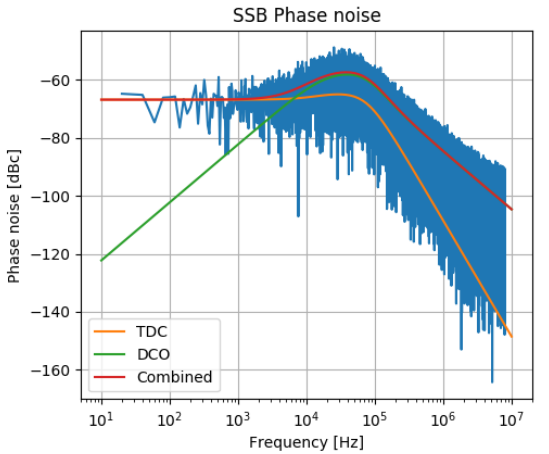
- f_{clk} = 16 MHz, N = 150 (2.4 GHz), 48 MHz initial offset, $t_{su} = t_h = 20ps$.









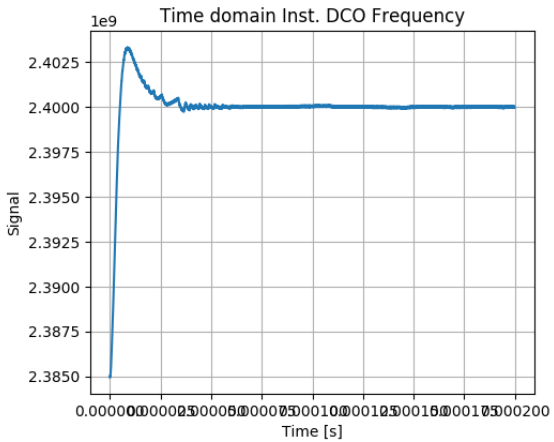


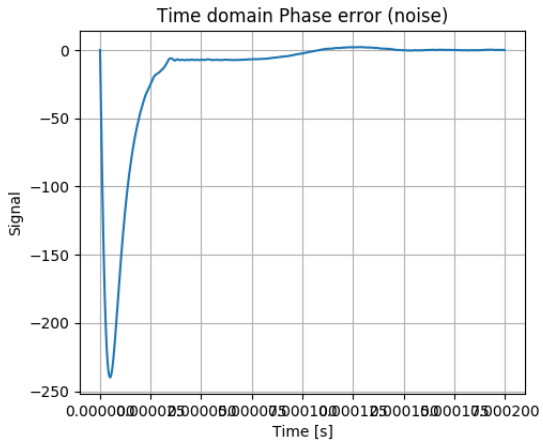
Phase noise matches model.

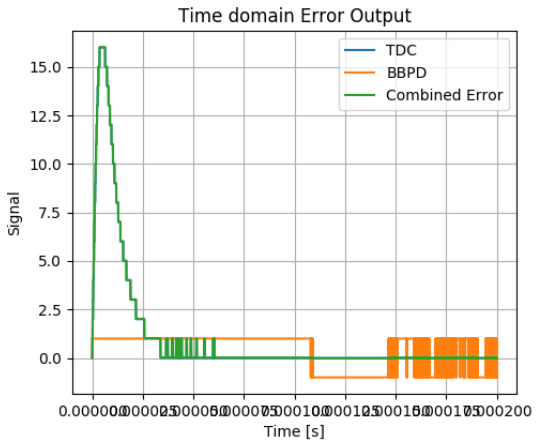
PLL Simulation with BB-PD

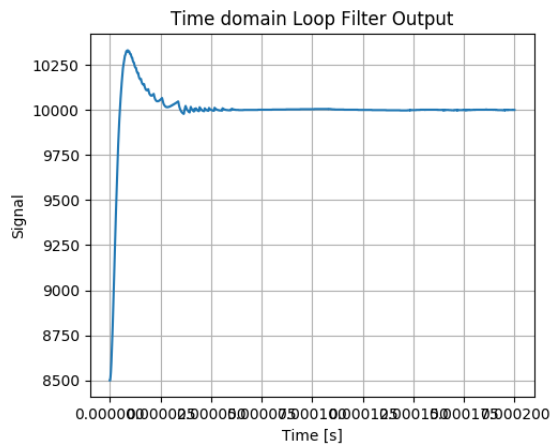
Delay line based TDC.

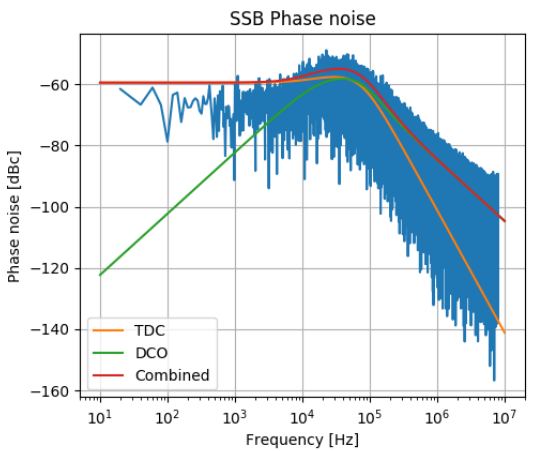
- TDC steps = 64, f_{clk} = 16 MHz, N = 150 (2.4 GHz), 15 MHz initial offset, $t_{su} = t_h = 20ps$.







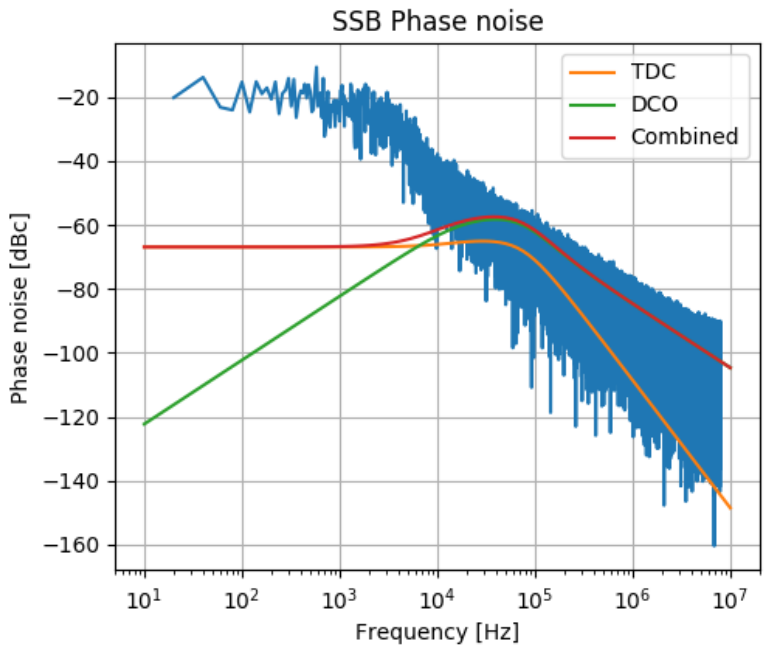




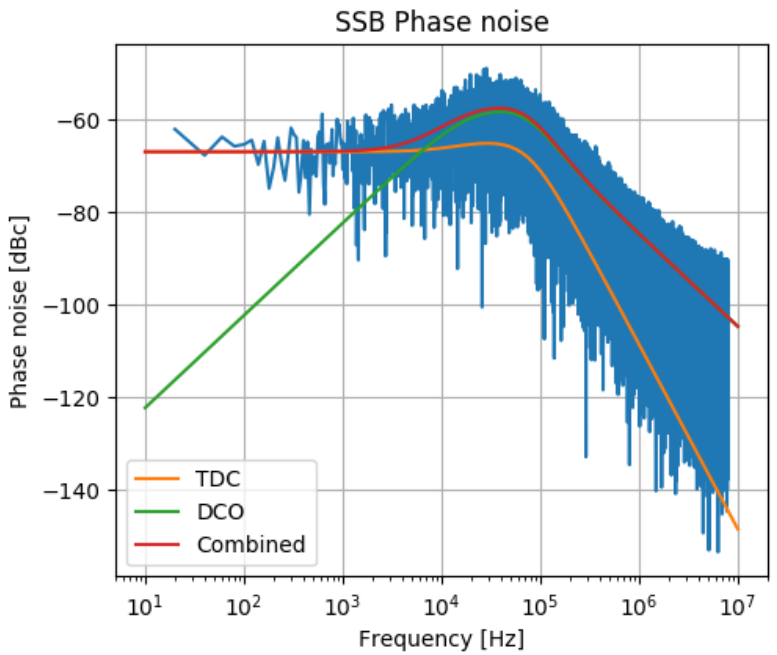
PLL Simulation with BB-PD

Phase noise comparison with and without BB-PD.

- The discrepencies I saw last week between model and simulation were from the phase detector, not a math error.



(a) Without BB-PD.

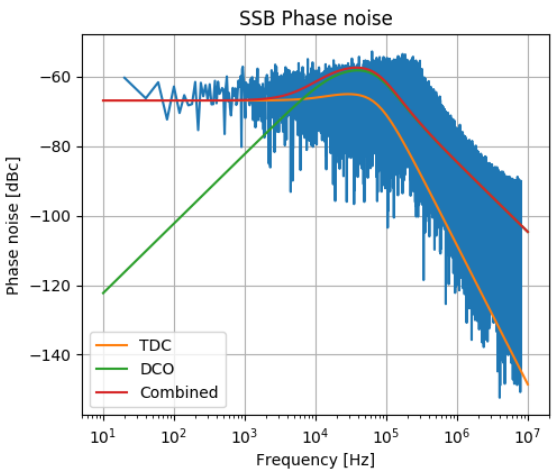


(b) With BB-PD.

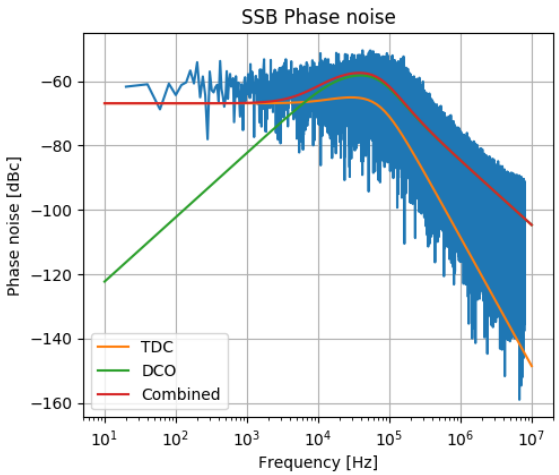
PLL Sim. - Datapath resolution

Comparison of Counter PLL with 6-10 fractional bits.

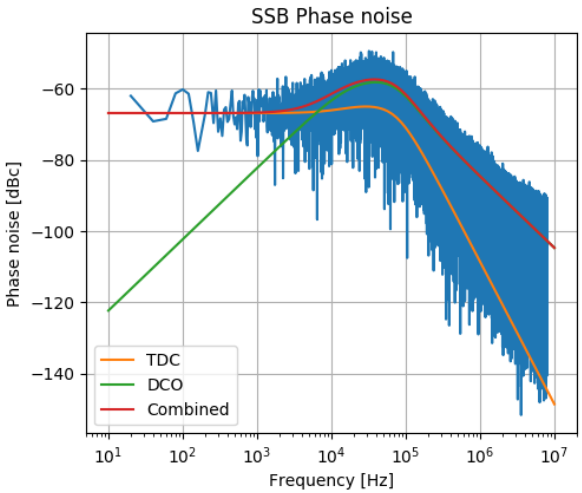
— Simulated PLL with various number of fractional bits in fixed point numeric representations. Number of integer bits varies.



(a) 6 Fractional bits.



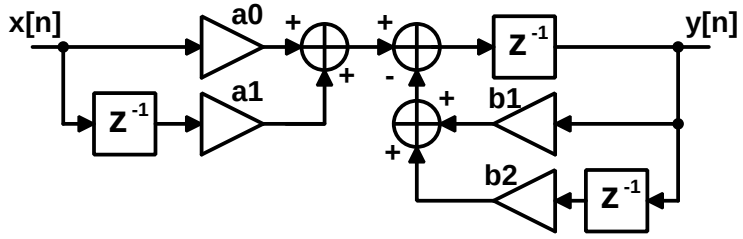
(b) 8 Fractional bits.



(c) 10 Fractional bits.

PLL Sim. - Datapath resolution

Resolution for fractional part from last week



— Last week came up with this expression based on the difference equation coefficients:

$$\text{\# Fractional bits} > \lceil -\log_2(a_0 + a_1) \rceil \tag{3}$$

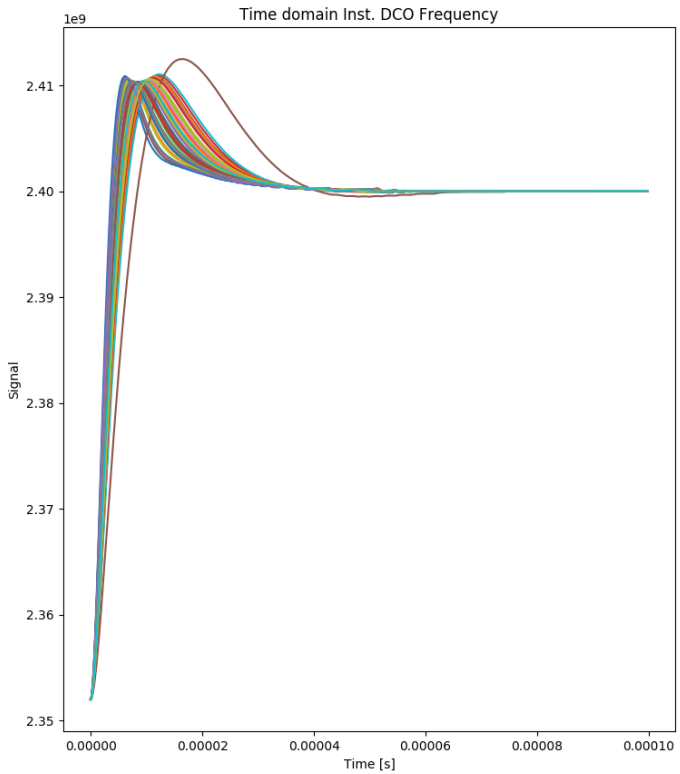
— For the configuration tested, 9 bits is the minimum based on the above equation. This seems to be in agreement with the simulation.

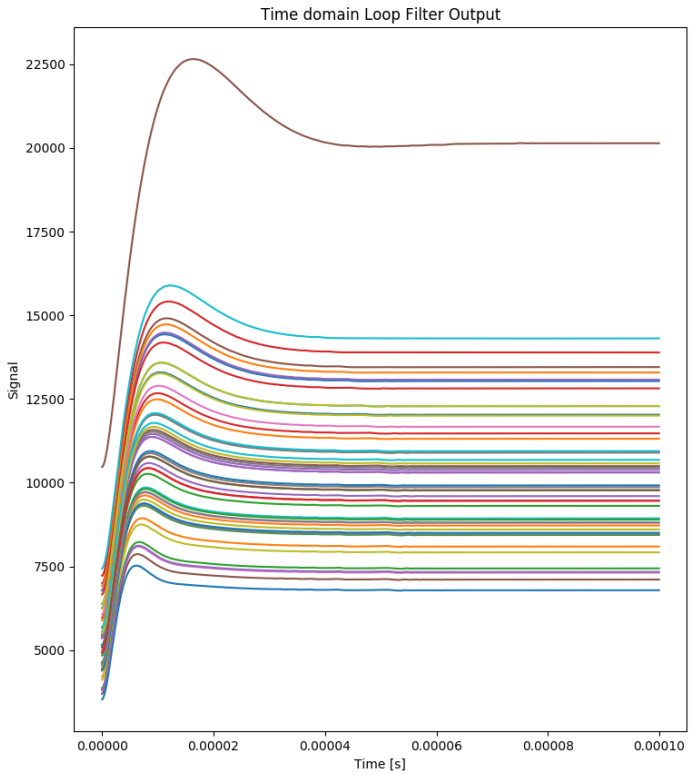
Simulation - Variation

KDCO variation.

— Simulated PLL with K_{DCO} subject to variance, where σ_{KDCO} is 20% of nominal K_{DCO}.

— Stable with 50 runs.

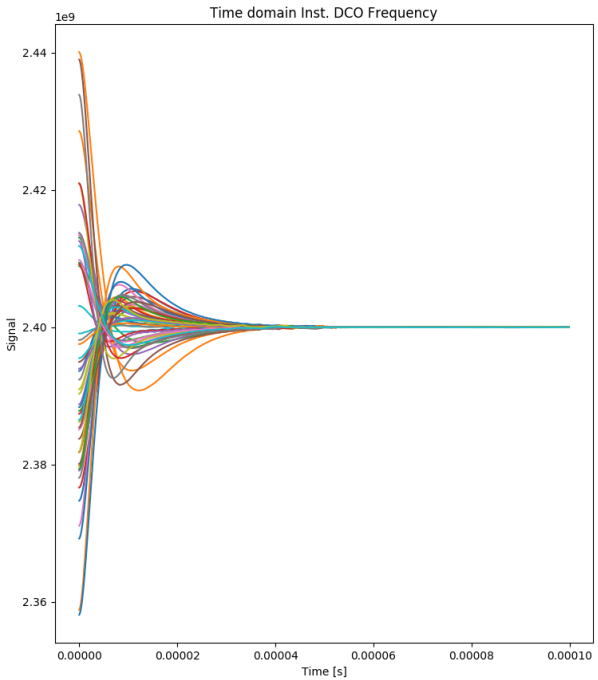


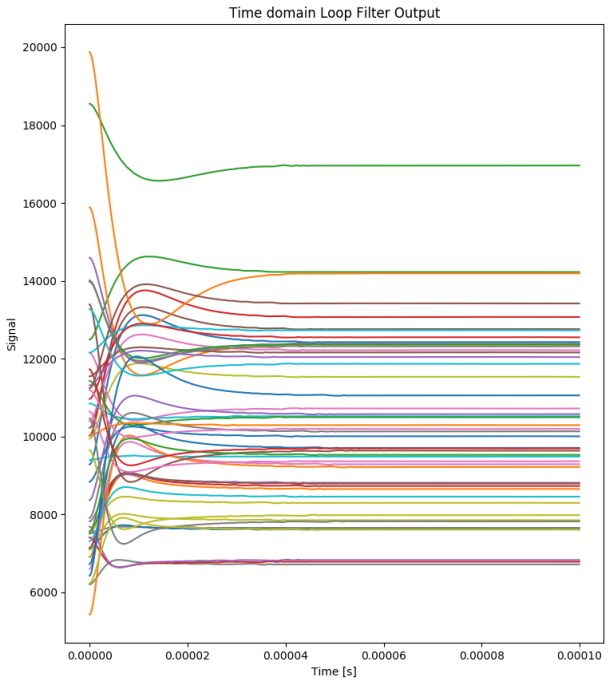


Simulation - Variation

KDCO and initial frequency variation.

- Simulated PLL with K_{DCO} subject to variance, where σ_{KDCO} is 20% of nominal K_{DCO}.
- $f_{initial} = f_0 - \Delta f$ is subject to variance, where $\sigma_{\Delta f}$ is 1% of nominal f_0.
- Stable with 50 runs.





Specification (unchanged)

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100	μW	
FSK BER	$\leq$ 1e-2		2FSK with f_{dev}=$\pm$250 KHz
Initial Lock Time	$\leq$ 50	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby
Bandwidth	50	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

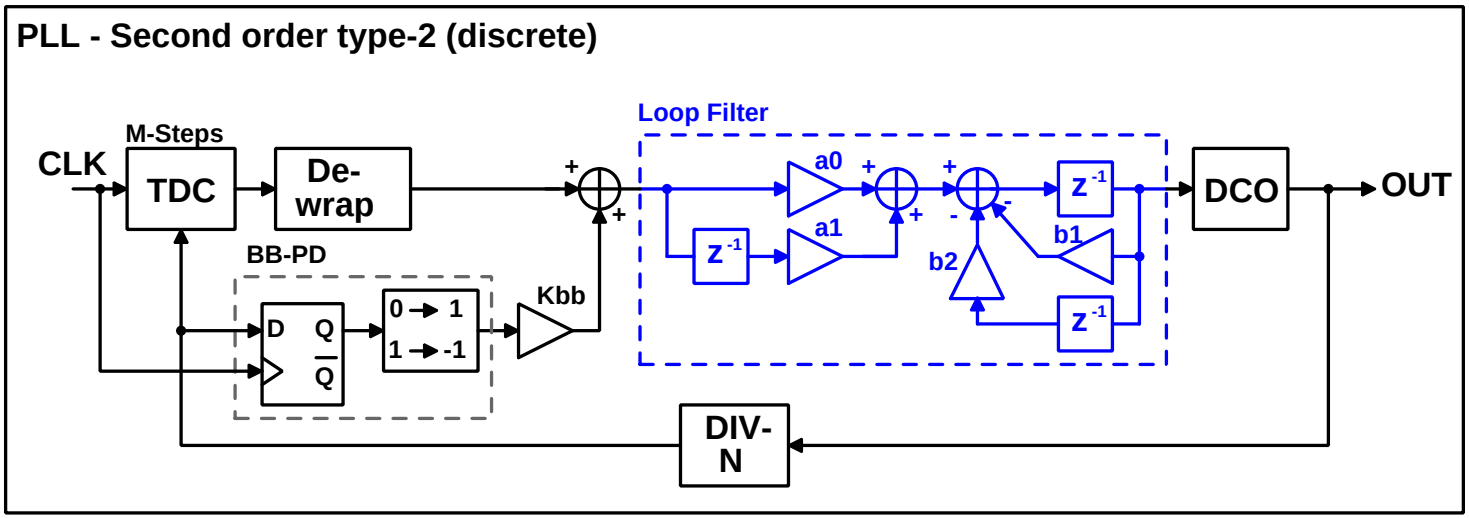
Specification (unchanged)

PLL Component Performance Targets

Parameter	Value	Unit	Notes
DCO LSB Resolution	≤ 50	kHz	Determined from quantization noise.
DCO DNL	< 1	LSB	Ensures monotonicity
TDC Resolution	0.95	ns	
TDC Resolution (bits)	6	bits	

Architecture (updated)

Block Diagram



Power Targets

DCO	TDC	Divider	Other	SUM
70 μW	20 μW	10 μW	$<<$ 1 μW	100 μW

Project Phases

Autumn 2019

- System modeling and simulation.
  - Learn PLL theory in detail
  - Evaluate feasability of PLL architectures (counter, TDC-based)
  - Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
  - Determine digital logic for loop filter, validate stability and lock time performance.
- Research ultra-low power circuit topologies to implement system components that will meet determined requirements.
- Translate component-level specifications into schematic-level circuit designs.
  - Try, fail, try again until functional at schematic level.
    - I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

- Finalize schematic-level design.
- Establish thorough tests for PLL performance (automated?) to help in layout.
- Layout of PLL.
  - Design iteration until design specs met.
  - Probably very time consuming.
- Full characterization/validation of design performance.
  - Comprehensive Corners/Monte-Carlo testing (time consuming??)
  - More design iteration if new issues crop up...
- Thesis paper writing.

References

[1] "Ultra-Low Power Wake-Up Receivers for Wireless Sensor Networks", N. Pletcher, J.M Rabaey, 2008.

`http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-59.html`