Ultra-Low Power PLL for Wake-up Receiver Applications

Specialization Project Progress - 5th Week

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Autumn Timeline

Week Number	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	**Loop filter,** Ideal implementation in Cadence
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Circuit Implementation	Digital logic (schematic)
44	28.10 - 3.11	Circuit Implementation	DCO (schematic)
45	4.11 - 10.11	Circuit Implementation	Divider/other (schematic)
46	11.11 - 17.11	Circuit Implementation (TDC)	
47	18.11 - 24.11	Circuit Implementation (TDC)	TDC (schematic)
48	25.11 - 1.12	Full Circuit testing	Testbenches, find bugs, design fixes
49	2.12 - 8.12	Full Circuit testing	Design Fixes/iteration
50	9.12 - 15.12	–	–

Legend: **Done** **Current** **Revised**

Timeline Tasks

This week

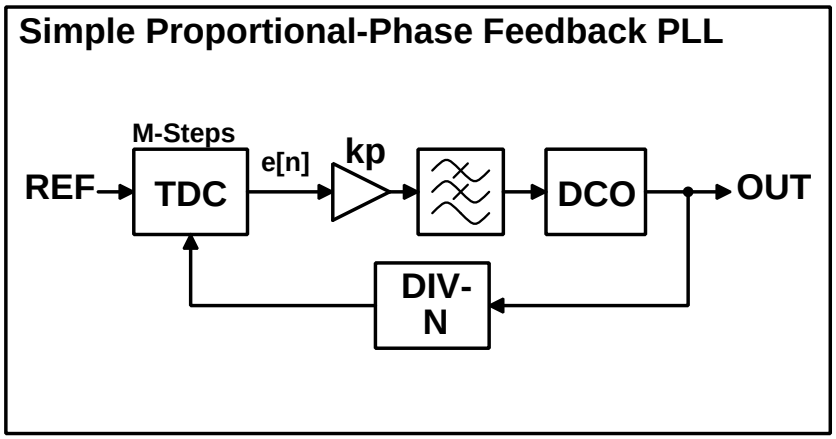
- **Primary:** Loop analysis, requirements definition
  - Design open loop filter design to meet closed loop requirements.
    - Dependent on DCO properties (k_{DCO}, f_0, tuning range).
    - Difference equation implementing discrete time 2nd order IIR filter.
  - Datapath requirements (fixed-point resolution)

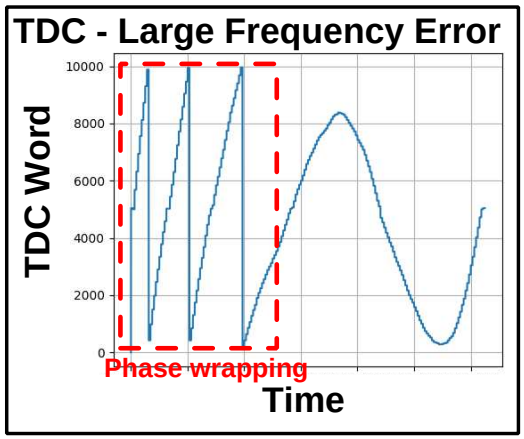
Next week - Revised

- **Primary:** Ideal component PLL implementation in Cadence, continue loop filter work.
  - Ideal component PLL implementation is not a lot of work.
  - Loop filter very critical, spend more time on this.
    - Need to make Verilog description of loop filter for simulation in Cadence.

Loop Filter

Original Attempt





— Started with simple PLL loop with proportional-phase fed into loop filter (LF).

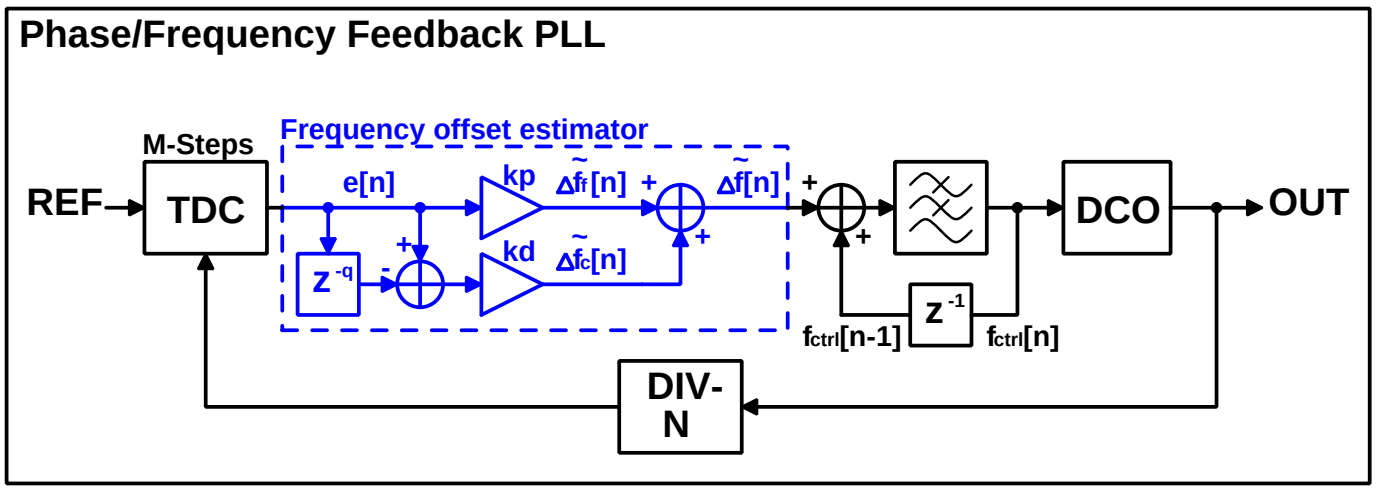
- Not stable at large frequency offset, due to frequency wrapping. At the TDC:

$$\Delta\phi = \frac{2\pi\Delta f T}{N} \rightarrow T_{wrap} = \frac{N}{\Delta f} \tag{1}$$

- Upon cold start, Δf is expected to be up to 100 MHz, N=150 $\rightarrow$ $T_{wrap} = 1.5\ \mu$s
  - $f_{wrap} \sim$ 600 kHz, this is unstable with a loop bandwidth of 100 kHz.
- Must opt for alternate loop structure.

Loop Filter

New Approach

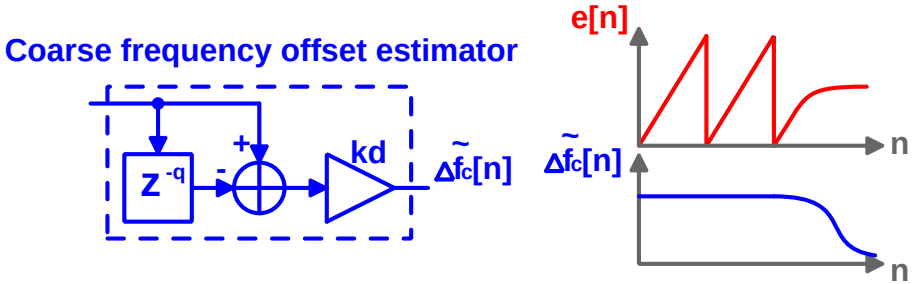


— Two-fold approach: utilize fine and coarse frequency offset estimation.
- Coarse frequency estimator to handle high frequency offset (e.g. cold start-up).
- Fine frequency estimator for near steady state.

— Offset estimates are summed with previous oscillator tuning word (OTW, also f_{ctrl} here), then low passed filtered to yield new OTW.
- Low pass filter loop keeps steady state.
- Frequency estimator updates if any changes detected.

Loop Filter

Coarse frequency offset estimation



— **Coarse frequency estimation:** Given M-step TDC, outputting phase error signal $e_\phi[n]$, and a divider modulus N

$$\Delta\phi_{DCO}[n;q] = N \cdot \Delta\phi_{REF}[n] = 2\pi \frac{N}{M} \left(e_\phi[n] - e_\phi[n-q]\right), \qquad \Delta\phi_{DCO}[n;q] = \Delta\omega_{DCO}[n] q T_{ref} = 2\pi q \frac{\Delta f_{DCO}}{f_{ref}} \tag{2}$$

$$\Delta f_{DCO} = \frac{f_{ref}}{q} \frac{N}{M} \left(e_\phi[n] - e_\phi[n-q]\right) \tag{3}$$

— Is a discrete differentiator, with gain coeficient to convert $d\phi/dt$ to frequency.

- Rejects phase wrapping.
- Useful in coarse frequency range calibration. Can detect fast if frequency offset too large.
- Delay q is used to increase frequency resolution.

Loop Filter

Coarse frequency offset estimation - continued

— Given DCO gain K_{DCO}, the gain K_d of the filter is:

$$K_d = \frac{f_{ref}}{qK_{DCO}} \frac{N}{M} \left(e_\phi[n] - e_\phi[n-q]\right) \tag{4}$$

— Gate the coarse estimator off if $e_\phi[n] - e_\phi[n-q] <$ some threshold:

- Offset small enough, allow to run as classical phase-detector mode.

Fine frequency offset estimation

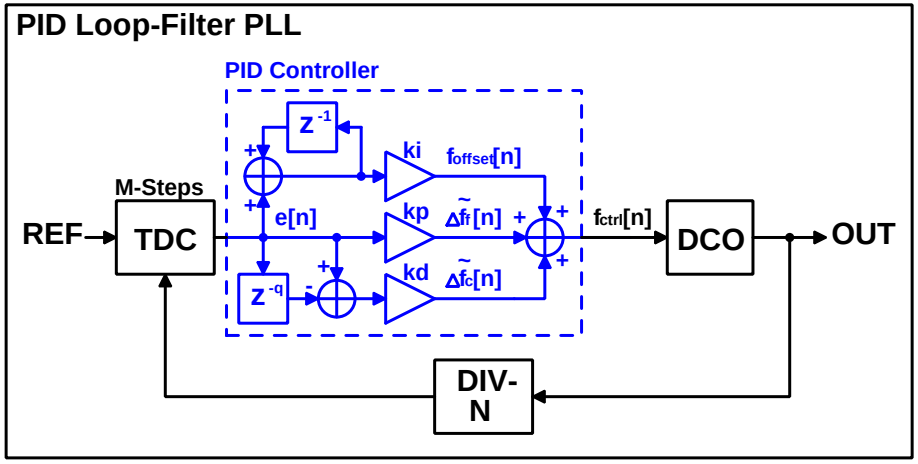
— Proportional signal of phase error to estimate frequency error.

— Used in near-steady state. Loop will regulate to keep phase locked.

— Classical PLL operating mode.

Loop Filter

Modified implementation - PID



— On the observation that the loop filter was basically a PID controller.

- Add integral term to complete PID. Integral term keeps track of steady state offset of OTW, ideally yields 0 steady state error.
- Derivative term *only* used to perform coarse adjustment.
- Near/in steady, behaves as **PI controller**.

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Loop Filter

Loop Filter Gain Coefficients

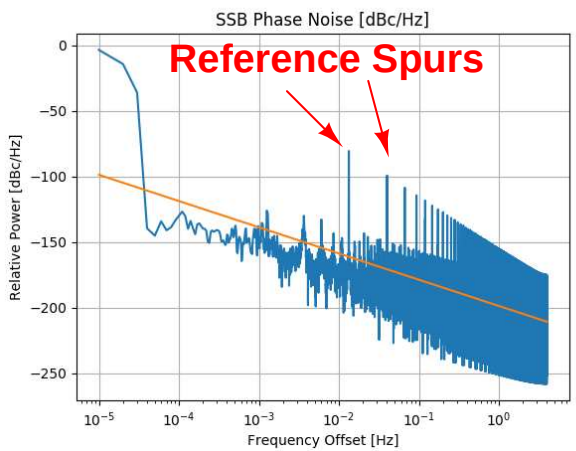
— On the observation that the loop filter was basically a PID controller.
  - Add integral term to complete PID. Integral term keeps track of steady state offset of OTW, ideally yields 0 steady state error.
  - Derivative term used to perform coarse adjustment.
  - Near/in steady, behaves as PI controller.

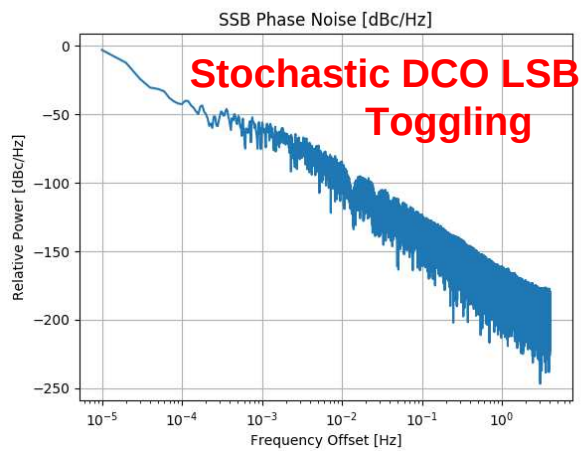
—

DCO

Performance criteria

- Resolution set by frequency accuracy requirements, quantization noise.
- Quantization noise is manifested here as:
  - Reference spurs resulting from deterministic components of signal.
  - A quasi-random noise signal when lock is achieved.
    - Results from stochastic toggling of $\sim$ 1 LSB of DCO tuning word to track low frequency variations.
    - Rolloff of -20 dB/decade at low frequency (same as ring oscillator), -40 dB/decade at high frequencies.



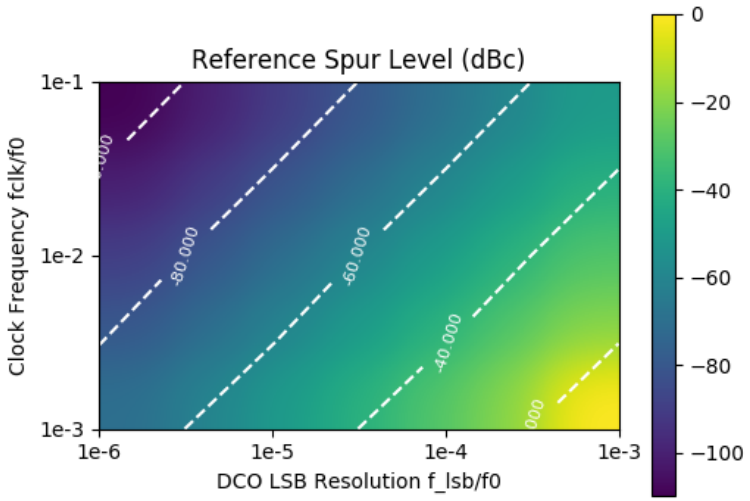


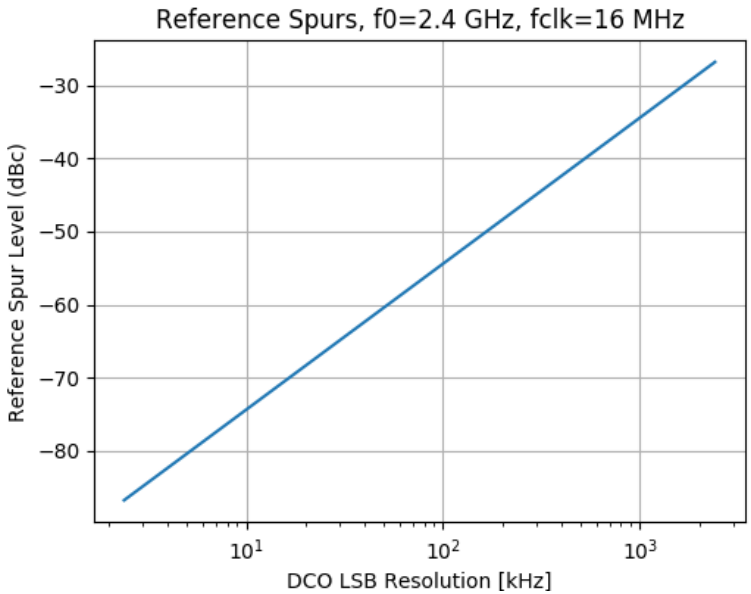
DCO

Requirements based on reference spurs

— Worst case reference spur level.
  - DCO tuning word toggling up/down 1 LSB every reference cycle.

— With f_0 = 2.4 GHz, f_{clk} = 16 MHz:
  - 52 kHz per LSB (i.e. K_{DCO}) is needed for a maximum -60 dBc reference spur level.





DCO

Requirements from steady state tracking of stochastic variation.

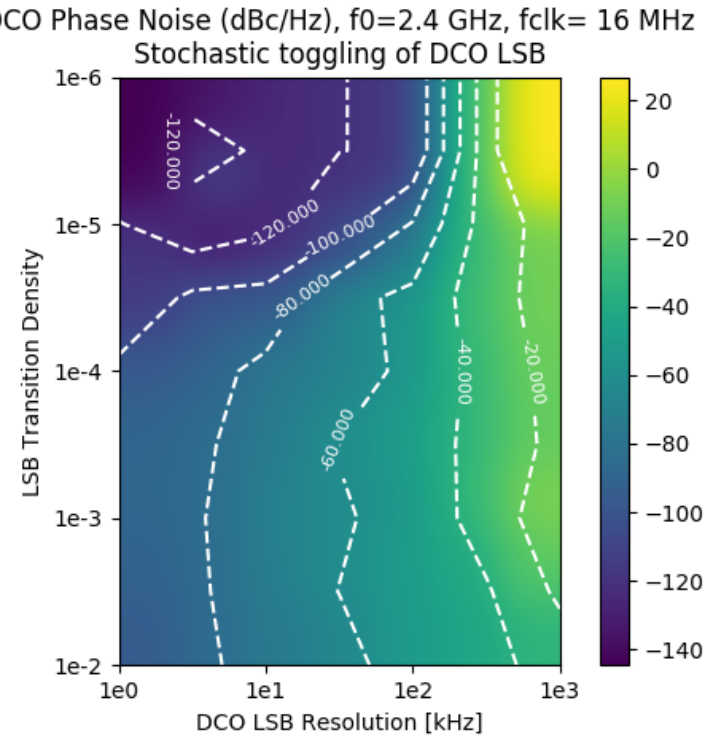
— In steady state, DCO tuning word will vary occassionaly by $\sim$ 1 LSB to track stochastic frequency changes.
  - This generates noise and should be less than the thermal phase noise of DCO.
  - Very pessimistic estimate here (assumes abrupt frequency change). Abrupt frequency steps contribute $1/\Delta f$ dependent component to phase noise.

— Theoretical ring oscillator phase noise limit from [2]:

$$PN_{min}(\Delta f) = 10 \log 10 \left(\frac{7.33 k_B T}{P} \left(\frac{f_0}{\Delta f} \right)^2 \right) \quad (5)$$

— If f_0 = 2.4 GHz, P = 50 μW, Δf= 1 MHz, T = 293K,

$\rightarrow$ **PN < -84.7 dBc/Hz** from this noise process.
  - LSB resolution of **50 kHz** seems feasible. Will have to verify with full PLL sim to account for loop dynamics.



DCO

Accuracy and Linearity

- Frequency accuracy.
  - Indeterminate IF assumed for wake up receivers, so accuracy not so critical.
  - If RF bandwidth of receiver > PLL bandwidth, reasonable assumption is maximum frequency offset (accuracy) should be < PLL bandwidth.
  - Current PLL bandwidth spec is 100 kHz, suggested 50 kHz LSB step from quantization noise analysis is sufficient?
    - This is assuming accuracy is tied to DCO resolution.
- Linearity:
  - Integral non-linearity over the tuning DCO range is not important, so no spec for INL is suggested. Should be locally linear (constrains DNL).
  - Monotonicity is essential, so must strictly have DNL < 1 LSB.

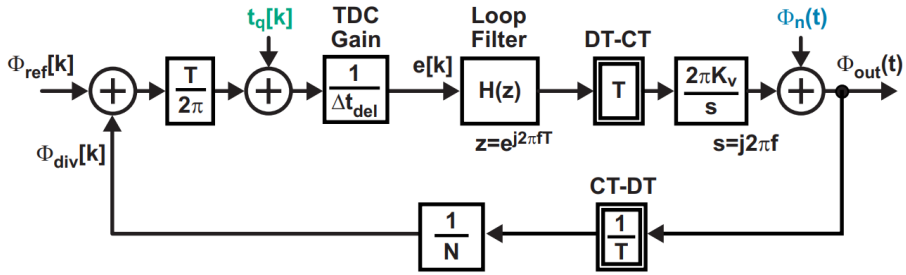
TDC

Phase Noise Modeling

— Based on a phase-domain model for PLL phase noise from Michael Perrot [1].

$$S_{\phi,out}(f) = f_{clk} \cdot |2\pi NG(f)|^2 \cdot \frac{\Delta t_{del}^2}{12} \quad (6)$$

$$G(f) = \frac{A(f)}{1 + A(f)} \quad (7)$$



— $S_{\phi,out}(f)$ is the TDC phase noise component, N is the divider modulus, G(f) is the closed loop PLL transfer function, A(f) is the open loop transfer function, Δt_{del} is the TDC time resolution.

— G(0) = 1, and G(f) $\approx$ 1 for f $\in$ [0, f_{CBW}], where f_{CBW} is the closed loop bandwidth.

TDC

Phase Noise Modeling

— Naive estimate for TDC time resolution:
- Phase noise flat within closed-loop bandwidth. This component dominates power of the integrated phase noise a PLL with low TDC-resolution.
- Use Residual frequency modulation equation and equation 2 (TDC phase noise) to estimate Δt_{del}. Integrate in f $\in$ [0, f_{CBW}]

$$\Delta f_{RFM} = 2 \int_{f_a}^{f_b} f^2 * PN(f) df \tag{8}$$

— With f_{clk} = 16 MHz, N = 150 (for 2.4 GHz synthesis), Δf_{RFM} < 107 kHz to meet BER requirement, and f_{CBW} = 100 kHz. (PLL presumed to have very low TDC resolution)
- Δt_{del} < 3.8 ns
- Phase noise of TDC below f_{CBW} is -47.7 dBc/Hz
- Equates to minimum of 16.4 quantization steps for TDC (4.03 bits).
- Assumptions of high phase noise and low resolution appear valid.

Specification (unchanged)

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	≤ 100	μW	
Residual FM	≤ 107	kHz_{RMS}	BER $\leq$ 1e-2, f_{dev}=$\pm$250 KHz
Initial Lock Time	≤ 50	μs	Upon cold start
Re-lock Time	≤ 5	μs	Coming out of standby
Bandwidth	100	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

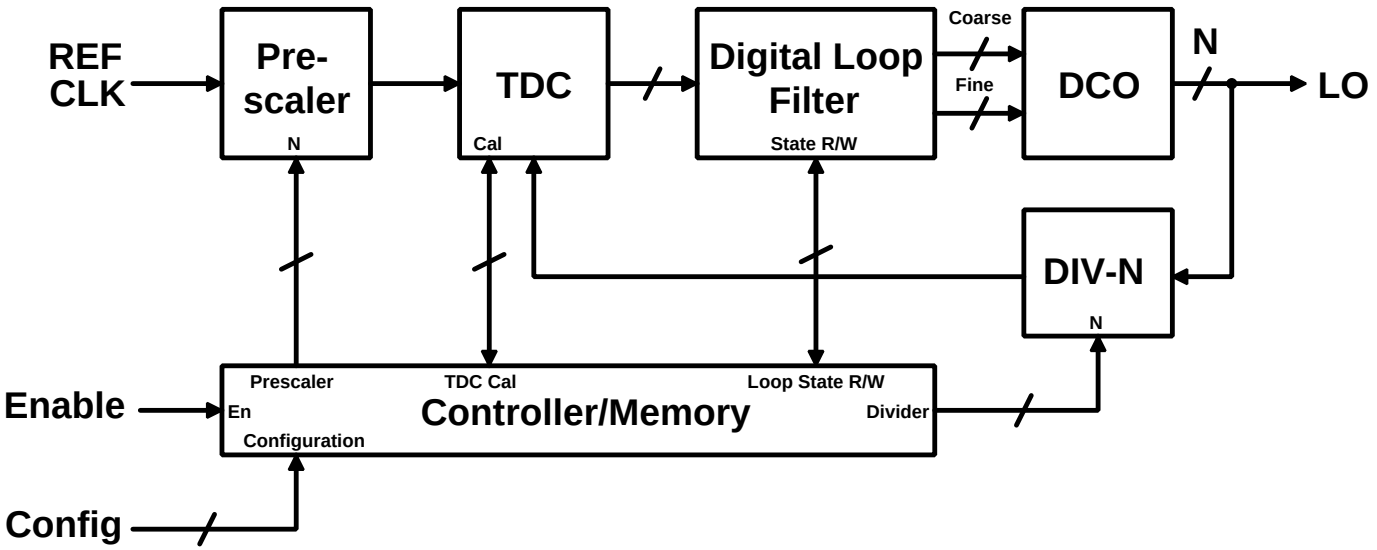
Specification (new)

PLL Component Performance Targets

Parameter	Value	Unit	Notes
DCO LSB Resolution	≤ 50	kHz	Determined from quantization noise.
DCO DNL	< 1	LSB	Ensures monotonicity
TDC Resolution	≤ 3.8	ns	
TDC Resolution (bits)	≥ 4.03	bits	

Architecture (unchanged)

Block Diagram



Power Targets

DCO	TDC	Divider	Other	SUM
70 μW	20 μW	10 μW	$<<$ 1 μW	100 μW

Project Phases

Autumn 2019

- System modeling and simulation.
  - Learn PLL theory in detail
  - Evaluate feasability of PLL architectures (counter, TDC-based)
  - Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
  - Determine digital logic for loop filter, validate stability and lock time performance.
- Research ultra-low power circuit topologies to implement system components that will meet determined requirements.
- Translate component-level specifications into schematic-level circuit designs.
  - Try, fail, try again until functional at schematic level.
    - I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

- Finalize schematic-level design.
- Establish thorough tests for PLL performance (automated?) to help in layout.
- Layout of PLL.
  - Design iteration until design specs met.
  - Probably very time consuming.
- Full characterization/validation of design performance.
  - Comprehensive Corners/Monte-Carlo testing (time consuming??)
  - More design iteration if new issues crop up...
- Thesis paper writing.

Project Phases (continued)

Spring 2020

[1] "Digital Frequency Synthesizers", Michael Perrott, 2019.
`http://www.cppsim.com/PLL_Lectures/day4_am.pdf`

[2] "Minimum Achievable Phase Noise of RC Oscillators", Navid et al. 2005