Ultra-Low Power PLL for Wake-up Receiver Applications

Specialization Project

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Motivation

Wireless Sensor Networks (WSNs) and IoT

— WSNs require ultra-low power circuits. A sensor should last for many years (>5) on a coin cell battery.

— With the below P_{avg} values, a CR2032 cell with 0.6 Wh capacity will last:
  - 1 μW $\rightarrow$ 70 years
  - 10 μW $\rightarrow$ 7 years
  - 100 μW $\rightarrow$ 0.7 years

— To save power, run devices with low duty cycle; activate remotely using wake up receiver (WuRx).
  - For 5 years of life, using 10% of battery energy for the WuRx, P_{WURX} **< 1.4 μW** on average is required.

— Main challenge for receiver is low power LO synthesis.
  - Synthesizer-free approaches (OOK receiver) lack robustness.
  - Advanced modulation schemes are too demanding with phase noise (PN).
  - Best option is FSK, using low power synthesizer with loose PN requirements to meet power target.

State of the Art

Wake Up Receivers

Performance averages based on sampling of 15 works published in IEEE:

Group	Count	Power [μW]	Freq [MHz]	RF BW [MHz]	Bitrate [kbps]	BER	Sens. [dBm]
All	15	96	1400	1.2	52	3e-3	-66
800/900M	6	138	887	0.95	15	4e-3	-68
All 2.4G	6	81	2400	2	60	2.8e-3	-67
2.4G FSK	2	190	2400	1.5	98	1e-3	-69
2.4G OOK	4	27	2400	2.5	41.5	4e-3	-66

— State of art of 2.4G WuRx:

- Active Power $\leq$ 100 μW
- RF BW $\approx$ 1 MHz
- Sensitivity = -70 dBm (BER 1e-3)
- Data Rate = 100 kbps

Objective

Synthesizer Goals

— Design ultra-low-power frequency synthesizer to meet requirements for *practical* wake up receivers.

- $\leq$**1** μ**W average consumption**
- Targeting **1% duty cycle** for $\leq$**100** μ**W active power**.
  - Fast locking to reduce on time/energy consumption.

— Synthesis range within **2.4 GHz ISM band**.

— Enable **wake up call detection within 1s** with 1e-3 miss rate.

- Achievable with 250 kbps data, BER $\leq$ 1e-2, 1% duty, 20% wake up call Tx density.
- Assuming 32-symbol wake up call used for false-alarm robustness.
- High BER inherent due to high PN, expect many misses before sucess.
- Use large FSK modulation index (m) to ease PN and power requirements.
  - m=2 $\rightarrow$ 2π phase shift per symbol or $\pm$250 kHz frequency deviation.
  - RMS Residual frequency modulation (RFM) of PLL should be $<<$ symbol frequency deviation to achieve desired BER.
  - **RFM is derived from phase noise integration; use to constrain PLL PN.**

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Specification

Preliminary Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	≤ 100	μW	
Residual FM	≤ 107	kHz$_{RMS}$	BER $\leq$ 1e-2, $f_{dev}=\pm250$ KHz
Initial Lock Time	≤ 50	μs	Upon cold start
Re-lock Time	≤ 5	μs	Coming out of standby
Bandwidth	100	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

Architecture

Concept

— Utilize **Digital PLL**.
  - Inherent feedback helps with PVT variation (yield).
  - Calibration easy in digital design, agains helps with PVT variation.
  - Can store state when PLL idle, allowing for faster lock times coming out of standby.

— Utilize low duty cycle to achieve power target.
  - Can exploit semi-frequent calibration to improve performance.
  - Possibly can run PLL open loop when lock is achieved to save power.

— Utilize oscillator running at 1/N subharmonic of target frequency.
  - Use 2N phases in oscillator to achieve equivalent IQ sampling.
  - Avoids having to run oscillator at 2x target frequency as done typically.
  - 1/3 subharmonic operation should allow for dual mode 2.4G and 915M operation.

— Employ subsampling to reduce divider noise and TDC power?

Architecture

Block Diagram
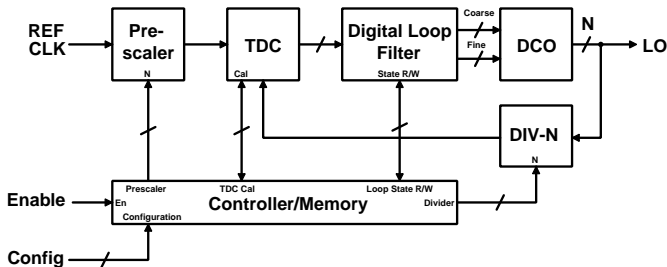
Power Targets

DCO	TDC	Divider	Other	SUM
70 μW	20 μW	10 μW	$<< 1$ μW	100 μW

State of the Art

Sub 1-mW PLLS

Application is niche, so comparable PLLs hard to find.

Type	P_{PLL} [μW]	P_{osc} [μW]	Freq [MHz]	PN@Δf [dBc/Hz]	t_{lock}* [μs]	Osc.	Ref Freq
Dig. Frac-N	650	304	2400	-110@0.5M	15/4	LC	26M
Ana. Int-N	680	510	2400	-110@1M	130/70	LC	1M
Ana. Int-N	128		500	-94@1M		Ring	31.25M
Ana. Int-N	570		800	-92.6@0.1M	200	LC	0.2M
Dig. Frac-N	250	173	2448		22/1	Ring	9M
Ana. Int-N	950		5500	-106@1M		IL-LC	

*Initial lock time and relock time

— Power limited by oscillator type. Scaling of LC-oscillator limited by gain requirements for self-starting. LC does not scale to low enough power.

— Current state of art for minimum power will be with ring oscillator, on the order of 200 μW for total PLL consumption.
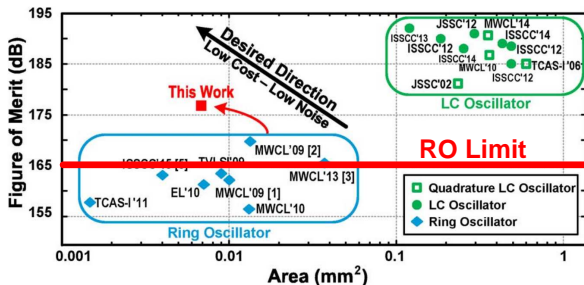
Physical limits

Ring Oscillator Phase Noise

Ring oscillator phase noise limit from "Minimum Achievable Phase Noise of RC Oscillators", Navid et al. 2005:

$$PN_{min}(\Delta f) = 10 \log 10 \left(\frac{7.33 k_B T}{P} \left(\frac{f_0}{\Delta f} \right)^2 \right) \tag{1}$$

If f_0 = 2.4 GHz, P = 50 μW, Δf = 1 MHz, T = 293 K, $\rightarrow$ **PN$_{min}$ = -84.7 dBc/Hz**
– This limit applied to the below FOM comparison (FOM PN=165 dB):

Project Phases

Autumn 2019

— System modeling and simulation.
- Learn PLL theory in detail
- Evaluate feasability of PLL architectures (counter, TDC-based)
- Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
- Determine digital logic for loop filter, validate stability and lock time performance.

— Research ultra-low power circuit topologies to implement system components that will meet determined requirements.

— Translate component-level specifications into schematic-level circuit designs.
- Try, fail, try again until functional at schematic level.
  - I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

— Finalize schematic-level design.
— Estabilish thorough tests for PLL performance (automated?) to help in layout.
— Layout of PLL.
  • Design iteration until design specs met.
  • Probably very time consuming.
— Full characterization/validation of design performance.
  • Comprehensive Corners/Monte-Carlo testing (time consuming??)
  • More design iteration if new issues crop up...
— Thesis paper writing.

Autumn Timeline

Week Number	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	Ideal (ahdlLib?) implementation in Cadence of PLL
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Circuit Implementation	Digital logic (schematic)
44	28.10 - 3.11	Circuit Implementation	DCO (schematic)
45	4.11 - 10.11	Circuit Implementation	Divider/other (schematic)
46	11.11 - 17.11	Circuit Implementation (TDC)	
47	18.11 - 24.11	Circuit Implementation (TDC)	TDC (schematic)
48	25.11 - 1.12	Full Circuit testing	Testbenches, find bugs, design fixes
49	2.12 - 8.12	Full Circuit testing	Design Fixes/iteration
50	9.12 - 15.12	–	–