Python Framework for Design and Analysis of Integer-N ADPLLs

Specialization Project Progress - 12th Week

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15 November 2019 (Calendar week 46)

Timeline

Week	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	Loop filter, DCO, TDC, calibration
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Spur analysis, filter automation	
44	28.10 - 3.11	Filter automation, SNR estimation	
45	4.11 - 10.11	Variation analysis, flicker noise	Histograms/yield estimates
46	11.11 - 17.11	Real DCO sensitivity, TDC/divider jitter	Simlate ring-DCO in Virtuoso
47	18.11 - 24.11	PLL + Radio simulation	BER estimate
48	25.11 - 1.12	Agglomerate into cohesive framework	(I have an Exam on 30.11)
49	2.12 - 8.12	Finish framework, report writing	
50	9.12 - 15.12	Report writing	Complete before 15.12

Legend: **Done** **Current** **Revised**

Timeline Tasks

This week

— **Include more sources of phase noise in PLL model:**
  - Added divider jitter, LF quantization noise, DCO quantization noise.

— **Simulation of Ring oscillator in 22FDX:**
  - Extracted values/variation for V_{th} and body effect coefficient γ for RVT/SLVT devices in various conditions.
  - Extracted data for frequency and current consumption for varied L, (W/L), load capacitance, temperature, supply voltage and RVT/SLVT devices.
  - Simulated variance of ring oscillator for comparison to model.

Phase noise model

Adding more components

- New loop filter optimizer is based on phase noise minimization, it is good to have a more complete phase noise model.
  - Previously only TDC noise and DCO noise (non-quantization) were considered.
- New phase noise components that were added:
  - Loop filter quantization noise.
  - DCO quantization noise
  - Divider jitter.
- These added components will allow for a more accurate estimate of the oscillator phase noise, and thus better loop filter optimization (i.e. phase noise minimizaton).

Phase noise model

Adding more components

— **Loop filter/DCO quantization noise**, where Q_{DCO} and Q_{LF} are the DCO and loop filter quantization noise signals. The noise transfer function is:

$$\frac{\Phi_{out}}{Q_{DCO}} = \frac{\Phi_{out}}{Q_{LF}} = 2\pi \frac{N_{DIV}}{M_{TDC}} \frac{G(s)}{H_{LF}(s)} \tag{1}$$

The PLL output phase noise spectral density from DCO quantization is as follows:

$$S_{\Phi_{out} Q_{DCO}} = \frac{1}{12 f_{clk}} \left| 2\pi \frac{N_{DIV}}{M_{TDC}} \frac{G(s)}{H_{LF}(s)} \right|^2 \tag{2}$$

The PLL output phase noise spectral density from loop filter quantization is as follows, where $\sigma^2_{Q_{LF}}$ is average power (in LSB^2) of the quantization noise. This is implementation dependent.

$$S_{\Phi_{out} Q_{LF}} = \sigma^2_{Q_{LF}} \left| 2\pi \frac{N_{DIV}}{M_{TDC}} \frac{G(s)}{H_{LF}(s)} \right|^2 \tag{3}$$

Phase noise model

Adding more components

— **Divider jitter**, where the noise transfer function is:

$$\frac{\Phi_{out}}{\Phi_{div}} = -N \cdot G(s) \tag{4}$$

If the divider is subject to jitter in time with variance $\sigma^2_{jit,div}$, the corresponding PLL output phase noise spectrum is:

$$S_{\Phi_{out}\Phi_{jit,div}} = \left|2\pi f_{clk} N_{DIV} \sigma_{jit,div} G(s)\right|^2 \tag{5}$$

This has the same dependence on G(s) as TDC quantization noise. To make divider noise less than TDC-related noise, we set $S_{\Phi_{out}\Phi_{jit,div}} < S_{\Phi_{out}\Phi_{Q_{TDC}}}$, this results in:

$$\sigma_{jit,div} < \frac{1}{M \cdot f_{clk}^{3/2}} \tag{6}$$

Ring oscillator in 22FDX

Extracting FET parameters

- Extracted V_{th} and body effect coefficient to use with model for comparison with simulation.
- Extracted for RVT and SLVT devices with L in {20n 100n, 500n}, W/L in {1, 10}.
- Short channel effects noticable in 20nm, $>=$ 100 nm it becomes less significant.
- For L=500nm, the below parameters were found. $\sigma_{V_{th}} < 0.036 V_{th}$, $\sigma_{\gamma} < 0.024\gamma$ (via Monte Carlo samping at T=-40, 25, 85).

Parameter	NFET	SLVTNFET	PFET	SLVTPFET
V_{th} [mV]	390-0.69T	340-0.67T	-387+0.88T	-312+0.77T
γ [V/V]	-0.072	-0.083	0.082	0.069

Ring oscillator in 22FDX

Ring oscillator model - assumptions

— Model ring oscillator with inverters modeled with ideal switches and lumped R and C components. The R is equivalent to the average channel resistance for the FETs.

— Square law ($L >> L_{min}$) and in saturation during period of propagtion delay. Requires $0.25V_{DD} < V_{th} < 0.5V_{DD}$.

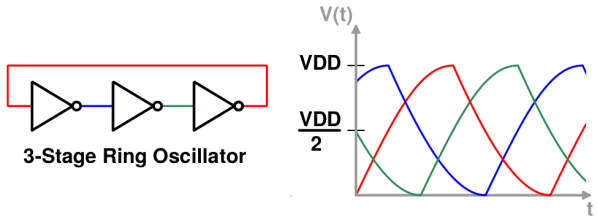
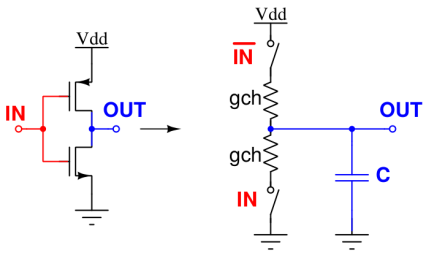
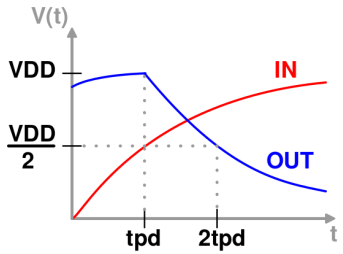


Figure 1: Model for ring oscillator.



(a) Inverter approximate model.



(b) Inverter waveforms in ring oscillator.

Ring oscillator in 22FDX

Ring oscillator model - equations

$$f_{osc} = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right) + \gamma V_{BG}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{7}$$

$$\Delta f_{osc}(V_{BG}) = \gamma V_{BG} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{8}$$

If backgate voltage is limited to the range of V_{DD}

$$f_c = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1 + \frac{\gamma}{2\ln 2} - \frac{\gamma}{2}\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{9}$$

$$\Delta f = \frac{\gamma V_{DD}}{2} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{10}$$

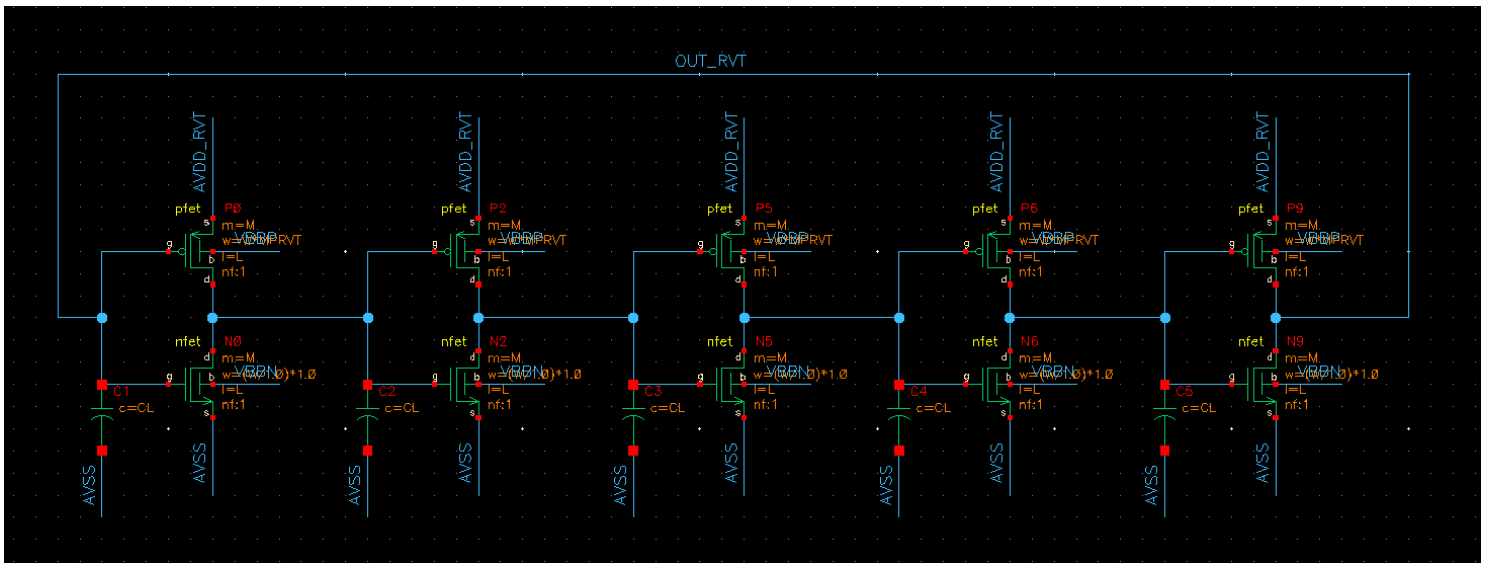
$$\frac{\Delta f}{f_c} = \frac{1}{2} \cdot \frac{\gamma V_{DD}(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}(1 - \ln 2)} \tag{11}$$

Ring oscillator in 22FDX

Ring oscillator simulation - schematic

— Simulated simple 5 stage ring oscillator with V_{DD} = 0.8.

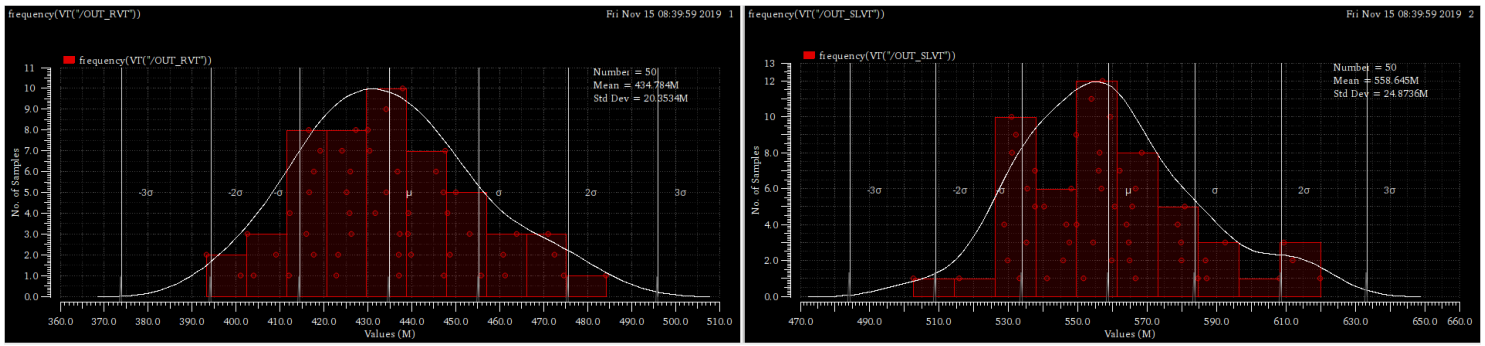
— Used RVT/SLVT devices, varied temp in {-40, 25, 85}, L in {100n, 500n}, W/L in {1, 10}, C_{load} in {0, 1f, 10f}, V_{BB} in {0, 0.8}



Ring oscillator in 22FDX

Ring oscillator simulation - variation

- Simulated simple 5 stage ring oscillator with V_{DD} = 0.8.
- Used RVT/SLVT devices, varied temp in {-40, 25, 85}, L in {100n, 500n}, W/L in: {1, 10}, C_{load} in {0, 1f, 10f}, V_{BB} in {0, 0.8}
- Also perfomed Monte-Carlo at 25C with L=500nm and W/L=1:
- Standard deviation for RVT is 4.7% of nominal value, for SLVT it is 4.5% of nominal.



Specification (unchanged)

System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq$ 100	μW	
FSK BER	$\leq$ 1e-2		2FSK with f_{dev}=$\pm$250 KHz
Initial Lock Time	$\leq$ 50	μs	Upon cold start
Re-lock Time	$\leq$ 5	μs	Coming out of standby
Bandwidth	50	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

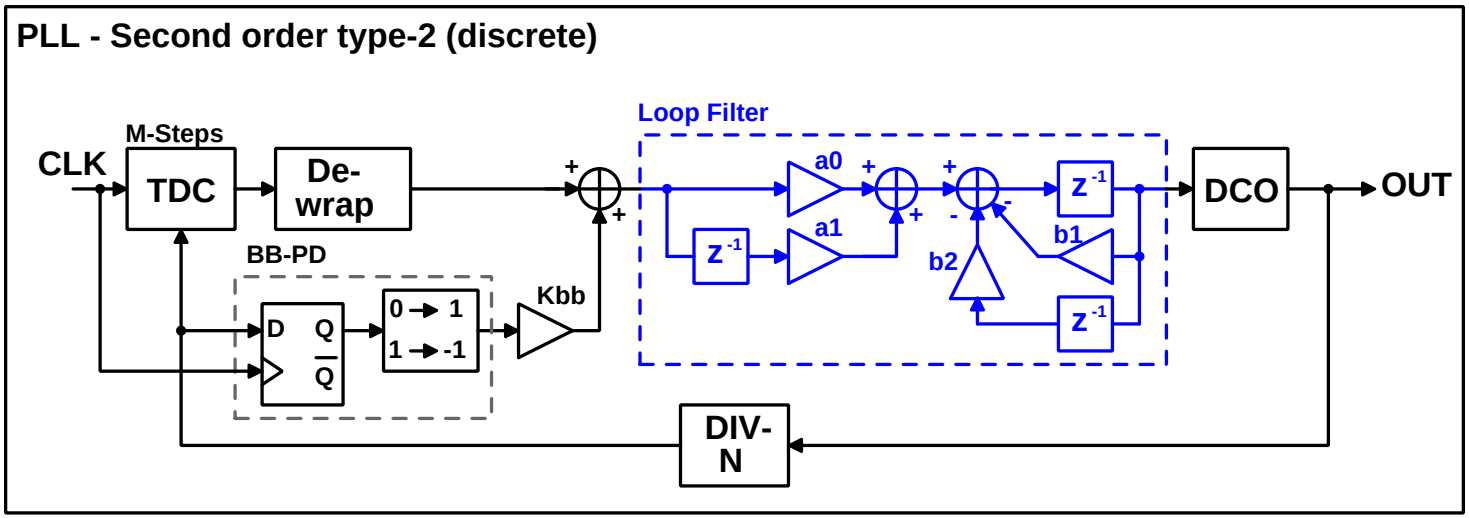
Specification (unchanged)

PLL Component Performance Targets

Parameter	Value	Unit	Notes
DCO LSB Resolution	≤ 50	kHz	Determined from quantization noise.
DCO DNL	< 1	LSB	Ensures monotonicity
TDC Resolution	0.95	ns	
TDC Resolution (bits)	6	bits	

Architecture (updated)

Block Diagram



Power Targets

DCO	TDC	Divider	Other	SUM
70 μW	20 μW	10 μW	$<<$ 1 μW	100 μW

Project Phases

Autumn 2019

— System modeling and simulation.
  - Learn PLL theory in detail
  - Evaluate feasability of PLL architectures (counter, TDC-based)
  - Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
  - Determine digital logic for loop filter, validate stability and lock time performance.

— Research ultra-low power circuit topologies to implement system components that will meet determined requirements.

— Translate component-level specifications into schematic-level circuit designs.
  - Try, fail, try again until functional at schematic level.
    — I expect the TDC to be difficult.

Project Phases (continued)

Spring 2020

- Finalize schematic-level design.
- Establish thorough tests for PLL performance (automated?) to help in layout.
- Layout of PLL.
  - Design iteration until design specs met.
  - Probably very time consuming.
- Full characterization/validation of design performance.
  - Comprehensive Corners/Monte-Carlo testing (time consuming??)
  - More design iteration if new issues crop up...
- Thesis paper writing.

References

[1] "Ultra-Low Power Wake-Up Receivers for Wireless Sensor Networks", N. Pletcher, J.M Rabaey, 2008.

`http://www.eecs.berkeley.edu/Pubs/TechRpts/2008/EECS-2008-59.html`