

# Ultra-Low Power PLL for Wake-up Receiver Applications

## Specialization Project Progress - 4th Week

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# This Week

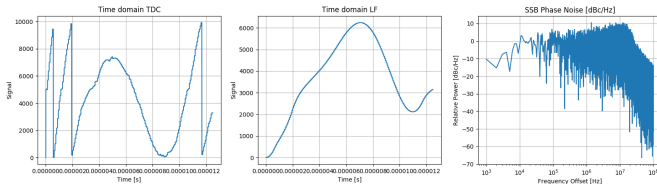
## Timeline Tasks

- **Primary:** Determine design requirements from modeling/simulation for Time to Digital Converter (TDC) and Digitally Controlled Oscillator (DCO).
  - For **TDC**:
    - Important criteria are resolution, linearity.
    - Quantization noise, dependent on resolution, is highly significant in PLL phase noise within loop bandwidth.
  - For **DCO**:
    - Important criteria are resolution, phase noise and monotonicity.

# Simulation/Modeling

## Approach

- My current full-PLL simulations are not generally stable.
  - Due to arbitrary choices for loop filter parameters not yielding a stable loop.
  - Next week plan is simulation / analysis / requirements definition of loop filter.
  - Will have to address issue of phase wrapping, fixed point resolution.

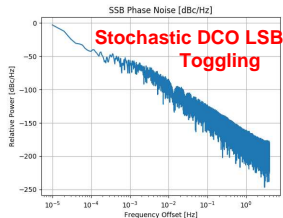
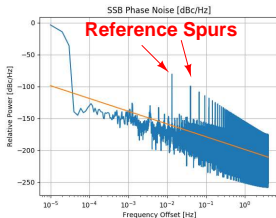


- Opted for mathematical-modelling of TDC, separate simulation of DCO.
  - Found straightforward model for TDC phase noise from Michael Perrott of MIT.
  - DCO simulation estimates quantization noise.
  - Will resume with full PLL simulation for loop filter and remainder of modeling.

# DCO

## Performance criteria

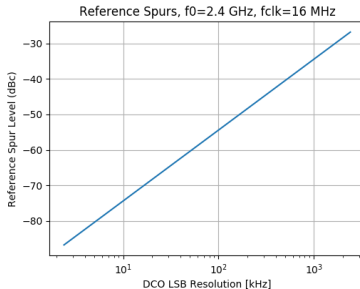
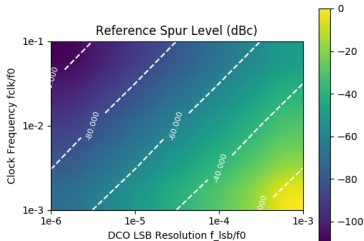
- Resolution set by frequency accuracy requirements, quantization noise.
- Quantization noise is manifested here as:
  - Reference spurs resulting from deterministic components of signal.
  - A quasi-random noise signal when lock is achieved.
    - Results from stochastic toggling of  $\sim 1$  LSB of DCO tuning word to track low frequency variations.
    - Rolloff of -20 dB/decade at low frequency (same as ring oscillator), -40 dB/decade at high frequencies.



# DCO

## Requirements based on reference spurs

- Worst case reference spur level.
  - DCO tuning word toggling up/down every reference cycle.
- With  $f_0 = 2.4$  GHz,  $f_{clk} = 16$  MHz:
  - 52 kHz per LSB (i.e.  $K_{DCO}$ ) is needed for a maximum -60 dBc reference spur level.



# DCO

## Requirements from steady state tracking of stochastic variation.

- Noise from toggling of  $\sim 1$  LSB of DCO tuning word in steady state tracking should be less than thermal phase noise of DCO.

- Very pessimistic estimate here (assumes abrupt frequency change).

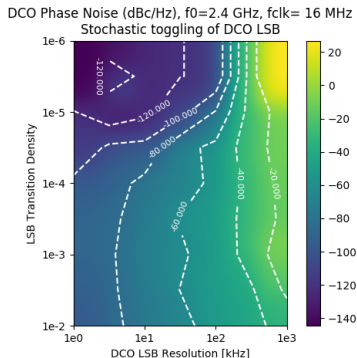
- Theoretical ring oscillator phase noise limit from [2]:

$$PN_{min}(\Delta f) = 10 \log 10 \left( \frac{7.33 k_B T}{P} \left( \frac{f_0}{\Delta f} \right)^2 \right) \quad (1)$$

- If  $f_0 = 2.4$  GHz,  $P = 50 \mu\text{W}$ ,  $\Delta f = 1$  MHz,  $T = 293\text{K}$ ,

→ **PN < -84.7 dBc/Hz**

- LSB resolution of **50 kHz** seems feasible.  
Will have to verify with full PLL sim to account for loop dynamics.



# DCO

## Accuracy and Linearity

### — Frequency accuracy.

- Indeterminate IF assumed for wake up receivers, so accuracy not so critical.
- If RF bandwidth of receiver > PLL bandwidth, reasonable assumption is maximum frequency offset (accuracy) should be < PLL bandwidth.
- Current PLL bandwidth spec is 100 kHz, suggested 50 kHz LSB step from quantization noise analysis is sufficient?

### — Linearity:

- Integral non-linearity over the tuning DCO range is not important, so no spec for INL is suggested.
- Monotonicity is essential, however, must strictly have  $DNL < 1 \text{ LSB}$ .

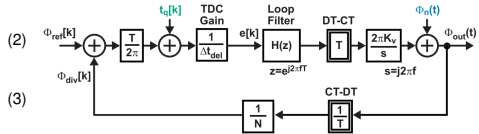
# TDC

## Phase Noise Modeling

- Based on a phase-domain model for PLL phase noise from Michael Perrot [1].

$$S_{\phi, out}(f) = f_{clk} \cdot |2\pi NG(f)|^2 \cdot \frac{\Delta t_{del}^2}{12}$$

$$G(f) = \frac{A(f)}{1 + A(f)}$$



- $S_{\phi, out}(f)$  is the phase noise,  $N$  is the divider modulus,  $G(f)$  is the closed loop PLL transfer function,  $A(f)$  is the open loop transfer function,  $\Delta t_{del}$  is the TDC time resolution.
- $G(0) = 1$ , and  $G(f) \approx 1$  for  $f \in [0, f_{CBW}]$ , where  $f_{CBW}$  is the closed loop bandwidth.



# TDC

## Phase Noise Modeling

— Naive estimate for TDC time resolution:

- Phase noise flat within closed-loop bandwidth. This component dominates power of integrated phase noise.
- Use Residual phase noise modulation equation and equation 2 to estimate  $\Delta t_{del}$ .

$$\Delta f_{RFM} = 2 \int_{f_a}^{f_b} f^2 * PN(f) df \quad (4)$$

— With  $f_{clk} = 16$  MHz,  $N = 150$  (for 2.4 GHz synthesis),  $\Delta f_{RFM} < 107$  kHz, and  $f_{CBW} = 100$  kHz

- $\Delta t_{del} = 3.8$  ns
- Phase noise of TDC below  $f_{CBW}$  is -47.7 dBc/Hz
- Equates to minimum of 16.4 quantization steps for TDC (4.03 bits).

# Specification (unchanged)

## System Performance Targets

Parameter	Value	Unit	Notes
Frequency	2.4-2.4835	GHz	2.4G ISM Band
Ref. frequency	16	MHz	Yields 6 channels
Power	$\leq 100$	$\mu\text{W}$	
Residual FM	$\leq 107$	$\text{kHz}_{RMS}$	$\text{BER} \leq 1\text{e-}2$ , $f_{dev} = \pm 250 \text{ KHz}$
Initial Lock Time	$\leq 50$	$\mu\text{s}$	Upon cold start
Re-lock Time	$\leq 5$	$\mu\text{s}$	Coming out of standby
Bandwidth	100	kHz	(nominally), tunable

Additionally: PLL output should support IQ sampling at LO frequency.

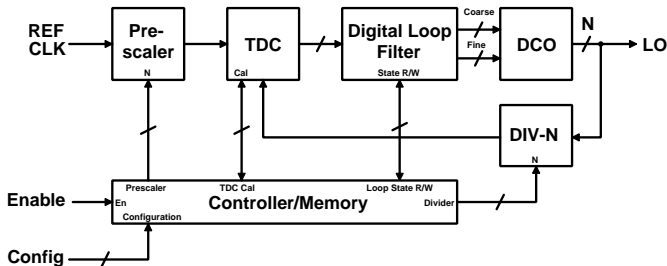
# Specification (new)

## PLL Component Performance Targets

Parameter	Value	Unit	Notes
DCO LSB Resolution	$\leq 50$	kHz	Determined from quantization noise.
DCO DNL	$< 1$	LSB	Ensures monotonicity
TDC Resolution	$\leq 3.8$	ns	
TDC Resolution (bits)	$\geq 4.03$	bits	

# Architecture (unchanged)

## Block Diagram



## Power Targets

DCO	TDC	Divider	Other	SUM
70 $\mu$ W	20 $\mu$ W	10 $\mu$ W	$\ll 1$ $\mu$ W	100 $\mu$ W

# Autumn Timeline

Week Number	Dates	Tasks	Outcomes
36	2.9 - 8.9	Review PLL Design	Refreshed Knowledge
37	9.9 - 15.9	Modeling/simulation (set up)	–
38	16.9 - 22.9	Modeling/simulation	TDC/DCO Requirements
39	23.9 - 29.9	Modeling/simulation	Loop Filter/Digital Algorithms
40	30.9 - 6.10	Modeling/simulation	Ideal (ahdlLib?) implementation in Cadence of PLL
41	7.10 - 13.10	Circuit Research	DCO/Divider topologies
42	14.10 - 20.10	Circuit Research	TDC/other topologies
43	21.10 - 27.10	Circuit Implementation	Digital logic (schematic)
44	28.10 - 3.11	Circuit Implementation	DCO (schematic)
45	4.11 - 10.11	Circuit Implementation	Divider/other (schematic)
46	11.11 - 17.11	Circuit Implementation (TDC)	
47	18.11 - 24.11	Circuit Implementation (TDC)	TDC (schematic)
48	25.11 - 1.12	Full Circuit testing	Testbenches, find bugs, design fixes
49	2.12 - 8.12	Full Circuit testing	Design Fixes/iteration
50	9.12 - 15.12	–	–

\*I will write the report simultaneously with the work.

# Project Phases

## Autumn 2019

- System modeling and simulation.
  - Learn PLL theory in detail
  - Evaluate feasibility of PLL architectures (counter, TDC-based)
  - Determine requirements for TDC/DCO/Divider/logic (bits of resolution, accuracy etc) to meet PLL performance specifications.
  - Determine digital logic for loop filter, validate stability and lock time performance.
- Research ultra-low power circuit topologies to implement system components that will meet determined requirements.
- Translate component-level specifications into schematic-level circuit designs.
  - Try, fail, try again until functional at schematic level.
    - I expect the TDC to be difficult.

# Project Phases (continued)

## Spring 2020

- Finalize schematic-level design.
- Establish thorough tests for PLL performance (automated?) to help in layout.
- Layout of PLL.
  - Design iteration until design specs met.
  - Probably very time consuming.
- Full characterization/validation of design performance.
  - Comprehensive Corners/Monte-Carlo testing (time consuming??)
  - More design iteration if new issues crop up...
- Thesis paper writing.

# Project Phases (continued)

## Spring 2020

[1] "Digital Frequency Synthesizers", Michael Perrott, 2019.

[http://www.cppsim.com/PLL\\_Lectures/day4\\_am.pdf](http://www.cppsim.com/PLL_Lectures/day4_am.pdf)

[2] "Minimum Achievable Phase Noise of RC Oscillators", Navid et al.  
2005