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Ultra Low Power Frequency Synthesizer

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Abstract.

An integer-N all digital phase locked loop (ADPLL) frequency synthesizer implemented 22nm FD-SOI (22FDX) technology is presented in this paper, achieving a power consumption of X μW at 2.448 GHz, a jitter FOM of X dB, and an active area of X mm^2. This design emphasizes power reducing architectural choices for application to low duty cyce wake up receivers (WURx), utiling low complexity, bias and reference free circuits. Included is a novel, pseudo-differential voltage controlled ring oscillator utilizing FD-SOI backgates to implement both frequency tuning and differential behavior. This oscillator achieves high oscillator tuning gain with rail-to-rail input range, whilst utilizing no current biasing. Capactive DACs are utilized to provide digital control to the oscillator with minimum power draw. A low complexity band-bang phase detector (BBPD) and all digital loop filter, with no divider in steady state implement the remaining portions of the PLL. Calibration of the PLL is implemented utilizing a synchronous counter-based frequency error detection scheme coupled with a coarse bank of tuning capacitors.

Preface.

Simplicity is the ultimate sophistication.

Leonardo da Vinci

I would like to thank my advisors Trond Ytterdal and Carsten Wulff for providing me the oppourtunities to futher my knowledge and experience in the dark arts of circuit design.

I also thank my family for their continual open support of my life endeavors.

Problem description.

The intent of this project is to develop an ultra low power, integer-N ADPLL frequency synthesizer for applications to wake up receiver (WURX) radio circuits. The target technology is Global Foundaries 22FDX fully-depeleted silicon on insulator (FD-SOI), a 22nm process node. The implemented PLL is intended for use in duty cycled wake up receiver WURX circuits applications, with on the order of 1% active time. Thus, the design must feature low power consumption in inactive (sleep) states, and rapid wake-up/resume. The required specifications for this PLL design are given in table 1

Parameter	Specification	Unit
Power	$\leq$ 100	μW
CNR[1]	$\geq$ 20	20 dBc
Reference frequency[2]	32	MHz
Synthesized frequency	2.448	MHz
Area	$\leq$ 0.01	mm^2
Lock time (cold-start)	$\leq$ 20	μs
Re-lock time (sleep-resume)	$\leq$ 5	μs
FOM$_{\Phi n}$[3]	$\leq$ -230	dB

Table 1: Design required specifications.

This work is in part a continuation of the author's previous work [1] on the optimization and simulation of integer-N ADPLL, which focused on automation of loop filter design. The architectural proceeded with in this work are motivated through findings of this work, particularly the usage of bang-bang phase detector with proportional-integral (PI) controller based loop filter. This architecture was found to be advantageous in terms of complexity and optimizability, providing for a known good starting point on this project.

[1] Carrier to noise ratio.

[2] Divided frequencies (powers of 2) are also acceptable.

[3] $\text{FOM}_{\Phi n} = 10\log_{10}\left(\frac{\sigma_{t_j}^2}{(1\,\text{s})^2}\cdot\frac{\text{Power}}{1\,\text{mW}}\right)$, where σ_{t_j} is the measured RMS timing jitter of the PLL.

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Abbreviations.

ADPLL	All digital phase locked loop
BBPD	Bang-bang phase detector
BOX	Burried-oxide
BW	Bandwidth
CDAC	Capacitive digital to analog converter
CDF	Cumulative distribution function
CI	Confidence interval
CLK	Clock
CM	Common mode
CMOS	Complementary metal oxide semiconductor
CMRR	Common mode rejection ratio
CNR	Carrier to noise ratio
DAC	Digital to analog converter
DC	Direct current
DCO	Digitally controlled oscillator
DFF	D flip flop
DIV	Divider
DNL	Differential non-linearity
FDSOI	Fully depleted silicon on insulator
FET	Field effect transistor
FOM	Figure of merit
FSK	Frequency shift keying
FSM	Finite state machine
HVTPFET	High threshold voltage PFET
IIR	Infinite impulse response
INL	Integral nonlinearity
ISF	Impulse sensitivity function
KDCO	DCO Gain
LC	Inductor-capacitor
LF	Loop filter
LO	Local oscillator
LSB	Least significant bit
LVTNFET	Low voltage threshold NFET
MMSE	Minimum mean squared error
MOSFET	Metal oxide semiconductor filed effect transistor

MSE	Mean squared error
NFET	N-channel field effect transistor
NMOS	N-channel metal oxide semiconductor
OOK	On-off keying
OTW	Oscillator tuning word
PD	Phase detector
PDF	Probability distribution function
PFET	P-channel FET
PI	Proportional-integral
PID	Proportional-integral-derivative
PLL	Phase locked loop
PMOS	P-channel metal oxide semiconductor
PN	Phase noise
PSD	Power spectral density
PSK	Phase shift keying
PVT	Process
RC	Resistor-capacitor
RMS	Root mean squared
RO	Ring oscillator
RST	Reset
RVT	Regular voltage threshold
SLVTNFET	Super-low voltage threshold NFET
SNR	Signal to noise ratio
SOI	Silicon on insulator
SSB	Single side band
TDC	Time to digital converter
TF	Transfer function
TSPC	True single phase circuit
UTBB	Ultra-thin body BOX
VCO	Voltage controlled oscillator
WUC	Wake up call
WUR	Wake up receiver

1 Introduction

Phase locked loops (PLLs) are the fundamental building block to virtually all wired and wireless communication systems of today. To meet industrial demands of continual and uncompromsing improvement of communication system performance, i.e. higher data rates, lower power, it is paramount that PLL performance is continually improved. The advent of battery powered mobile and IoT produces an accute need for power reduction. A recent approach to reducing power consumption of mobile and IoT devices is through usage of wake up receivers (WUR). These are ultra low power, low data rate radio receivers, which listen for requests (i.e. a ”wake up call”, or WUC) for activity of the aforementioned devices. Upon a WUC, the device activates a higher powered radio supporting higher data rates for only the time required. In devices which are inactive for large periods of time, waiting for requests for activity (e.g. as sensor networks or wireless headphones), such a scheme can enable great power reduction, achieving 4.5 nW in [2] and 365 nW in [3] for 2.4 GHz reception, compared to utilizing a full data rate receiver to poll the radio spectrum for activity requests.

Thus, in this work, low power PLL design which enables WUR design is to be considered. Ultra low power has been achieved with PLL-less OOK receivers, for example achieving 4.5 nW with 0.3 kbps of data at 2.4GHz [2]. However, this work will be catered to PLL-based designs that mantain backwards-compatibility with FSK, PSK modulation schemes supported by existing standards such as 802.15.4, Wifi, Bluetooth. The PLL design approached in this work will seek methods to reduce overall complexity (minimize current paths), whilst yielding high performance on a given power budget. A brief outline of the paper is as follows. An introduction to PLL and FD-SOI theory is in section 2. The undertaken PLL Design are discussed in section 3. Simulation results obtained of the design are in section 4. Comparisons to states of art and general discussion regarding this work is in section 5. Finally, section 6 concludes.

1.1 Main Contributions

1. Implementation of an ultra-low power, small area CMOS PLL in 22FDX FD-SOI technology.
2. Presentiation of a novel pseudodifferential ring oscillator circuit topology, utilizing FD-SOI backgates to implement both frequency tuning and differential coupling.
3. Realization of linear gain voltage controlled oscillator with rail to rail range.
4. Introduction of mathematical model of the aforementioned oscillator.
5. Implementation of low power CDACs, bang-bang phase detector.
6. Implementation of low power digital loop filter.
7. Demonstration of bias current and reference free PLL design.

2 Theory

2.1 Fully Depleted Silicon on Insulator (FD-SOI)

FD-SOI is a process technology that implements complementary metal oxide semiconductor (CMOS) transistors with an insulating layer of oxide, referred to as a burried oxide (BOX), between the channel of the transistors and the silicon substrate [4]. The addition of such an oxide reduces capacitances of the fabricated transistors to the silicon substrate, resulting in lower overall capacitance than in bulk CMOS technologies. Thus higher frequency of operating is possible versus similar sized bulk process nodes. A further feature introduced by FD-SOI technology is the ability to form isolated wells beneath fabricated devices [5], which remained electrically isolated from the transistors via the BOX and from the substrate due to PN junctions inherent in well formation. This opens the possibility to achieve biasing across a wide voltage range of the regions below individual transistors (both for PMOS and NMOS devices), which enables tuning of individual transistor threshold voltages by exploitation of the MOS body effect. The well beneath a FD-SOI transistor is referred to as the ”backgate”. The implementation these features in the Global Foundaries 22FDX process is shown in figure 1.

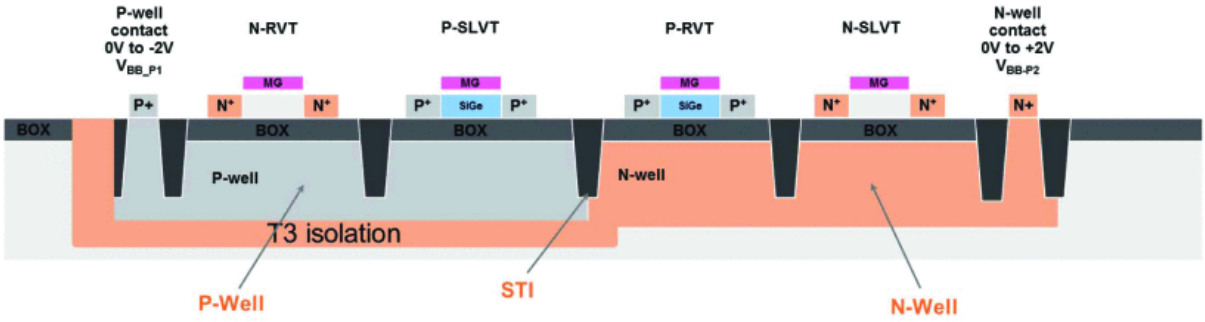


Figure 1: 22FDX cross-sectional construction of active devices [5].

2.2 MOSFET Models

2.2.1 I-V relations

Basic models that describe the large signal current-voltage relations of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) are introduced here, based wholy from [6]. For the purposes of this work, a MOSFET is schematically represented in the manner of figure 2, with gate (G), drain (D), source (S) and backgate (B) terminals. Several operating regimes occur depending on the relation of the terminal voltages. Relevant to the scope of this work, are the linear, saturated and velocity saturated regions of MOSFET operation. Nominally, it is expected that when configured as in figure 3, sweeping the gate-source voltage (V_{GS}), with the

drain-source voltage (V_{DS}) set greater than 0 in the case of a NFET, that an increasing amount of current will enter the MOSFET drain after crossing a threshold voltage (V_{TH}). V_{TH} is predominantly dependent of physical configuration of a FET (dimensions, doping, material), however is impacted by the backgate bias in what is termed "the body effect". A more detailed description of each operating regime will be given in the following discourse.

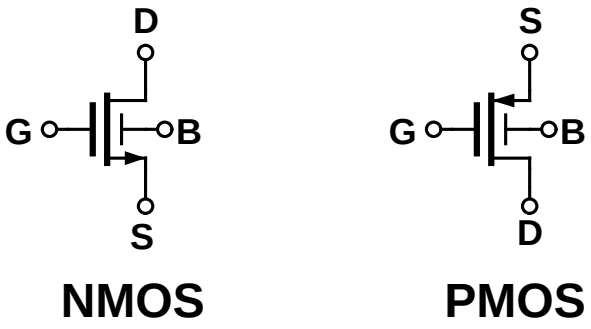


Figure 2: MOSFET symbols.

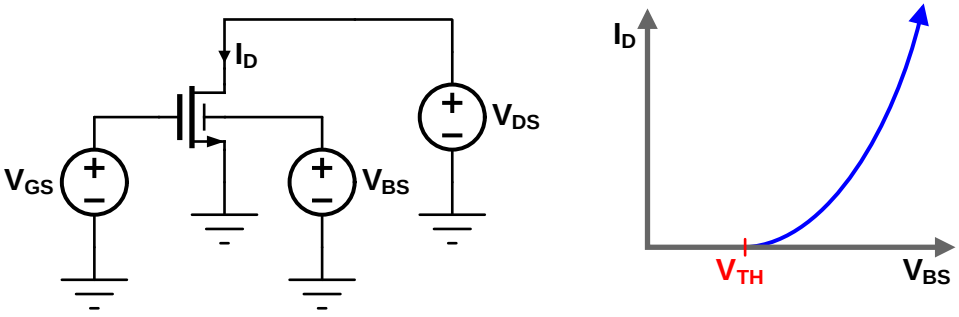


Figure 3: Drain current versus gate-source bias.

Linear Region Linear MOSFET operation occurs under the circumstances where $|V_{GS} - V_{TH}| > |V_{DS}|$. The following equation is the I-V relation in this regime, where μ_n represents the electron mobility of the semiconductor in use (within the FET channel), C_{ox} represents the MOS oxide capacitance.

$$I_D = \mu_x C_{ox} \left(\frac{W}{L}\right) \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \tag{1}$$

Saturation Region Saturation region occurs when $|V_{DS}| > |V_{GS} - V_{TH}|$. Notably, dependence of drain current on V_{DS} is reduced, and in the case of the ideal models considered here the effect of V_{DS} are completely negated.

$$I_D = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{TH})^2 \tag{2}$$

Velocity-saturation Region In the scenario of high applied fields which arise in a short MOSFET channels, carrier velocity can saturate to a limited velocity, v_{sat}. The point at which this effect takes place is device dependent. For approximate consideration it can be understood to

occur when $|V_{DS}/L > E_{crit}|$, where E_{crit} is the electric field which the carrier velocity-electric field relation ($v = \mu E$) of the channel semiconductor becomes sub-linear. Below is the MOSFET model under such circumstances.

$$I_D = WC_{ox}(V_{GS} - V_{TH})v_{sat} \tag{3}$$

2.2.2 Body Effect

Application of a bias to the substrate below a bulk MOSFET, or to the well below a FD-SOI MOSFET has a direct effect on the threshold voltage of a MOSFET. For a bulk MOSFET, change of body bias affects the width of source-drain and source-body depletions, which consequently can increase or decrease the magnitude of the channel inversion charge as seen by the gate terminal. This corresponds to a differential in the threshold voltage. The below equation [6] quantifies this effect for bulk devices. γ is the body effect coefficient, $2\Phi_F$ represents the MOS surface potential. V_{TH} is non-linearly related to the source-body voltage V_{SB}.

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\Phi_F + V_{SB}} - \sqrt{|2\Phi_F|}\right) \tag{4}$$

In the case of FD-SOI transistors, the nature of the body effect is modified due to the presence of the BOX. Thus, an approximate derivation for body effect will be provided here. In FD-SOI, the active channel region is thin, and under strong inversion, the entire channel region is depleted of charge. Supposing a channel height Z and doping N_A, the total inversion charge (i.e. to deplete the channel) is $Q_d = N_A Z$. With oxide capacitance $C_{ox,fg}$ associated with the front gate, the portion of the threshold voltage associated with total depletion of the channel is, from the front gate perspective:

$$V_{d,fg} = \frac{Q_d}{C_{ox,fg}} = \frac{N_A Z}{C_{ox,fg}} \tag{5}$$

Supposing that the back gate has capacitance of $C_{ox,bg}$, with bias applied V_{BS}, the back gate can be seen to "rob" the front gate of $Q_{bg} = C_{ox,bg}V_{BS}$ when in inversion. Thus results in a partial change of the front gate referred voltage required to obtain channel depletion:

$$V'_{d,fg} = \frac{Q_d - Q_{bg}}{C_{ox,fg}} = \frac{Q_d}{C_{ox,fg}} - \frac{C_{ox,bg}}{C_{ox,fg}}V_{BS} = V_{d,fg} - \Delta V_{th,bg} \tag{6}$$

It is noted that this can be writen as the nominal value of $V_{d,fg}$ minus a differential. This differential is the resulting change in threshold voltage due to back gate bias, $\Delta V_{th,bg}$:

$$\Delta V_{th,bg} = \frac{C_{ox,bg}}{C_{ox,fg}}V_{BS} \tag{7}$$

This is linear with applied back gate bias, and that the strength of the coupling is tunable by the ratio of front gate and back gate capacitances. Typically this ration is $<< 1$. If we define the

body effect coefficient γ as:

$$\gamma = \frac{C_{ox,bg}}{C_{ox,fg}} \tag{8}$$

Given a nominal threshold voltage of V_{TH0}, in FD-SOI, the threshold voltage can be calculated as:

$$V_{TH} = V_{TH0} - \gamma V_{BS} \tag{9}$$

2.3 Basic PLL

A phase locked loop (PLL) is a feedback system whose output tracks or maintains a fixed phase relationship to an input signal. PLLs are well suited for frequency synthesis, which is the process of generating derivative frequencies from some reference frequency. Given a reference signal with phase trajectory Φ_{ref} and output signal with phase Φ_{out}, a PLL can be modeled as in figure 4 using an elementary feedback system, with feedforward and feedback networks A(s) and B(s).

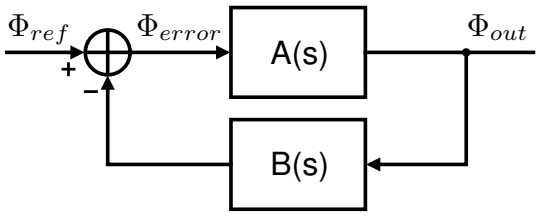


Figure 4: Phase locked loop as elementary feedback system.

The closed loop phase response for Φ_{ref} to Φ_{out} is therefore:

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{A(s)}{1 + A(s)B(s)} \tag{10}$$

A case of interest is when B(s) = 1/N, where N is a constant, and the loop gain L(s) = A(s)B(s) $>>$ 1. The closed loop response for this case is:

$$\frac{\Phi_{out}(s)}{\Phi_{ref}(s)} \approx \frac{A(s)}{A(s)B(s)} = \frac{1}{B(s)} = N \tag{11}$$

We see that the phase through the PLL is multiplied by a factor of N. If the input phase signal is sinusoidal with frequency ω_{ref}, and likewise the output with ω_{out}, then $\phi_{ref}(t) = \omega_{ref}t$ and $\phi_{out}(t) = \omega_{out}t$. Accordingly:

$$\frac{\Phi_{out}(t)}{\Phi_{ref}(t)} = \frac{\omega_{out}t}{\omega_{ref}t} \approx N \quad \rightarrow \quad \omega_{out} \approx N\omega_{ref} \tag{12}$$

Therefore, it is observed that a PLL allows for the generation of a new frequency from a refer-

ence frequency signal, which is termed as ”frequency synthesis”. With a feedback division ratio of 1/N, the PLL multiplies the reference frequency by a factor of N. Hereon, the B(s) portion of a PLL feedback network is referred to as a divider, with associated division raito N.

2.4 PLL Synthesizer Architecture

A typical architecture for implementing a physically realizable PLL frequency synthesizer [7] is shown in figure 5. This PLL is comprised of four components: (1) a phase detector, herein PD, (2) a loop filter, herein $H_{LF}(s)$, (3) a voltage controlled oscillator, herein VCO, and (4) a divider, indicated as ”÷ N” in figure 5. In control systems parlance, the loop filter corresponds to a controller, the VCO an actuator, and the divider as feedback.

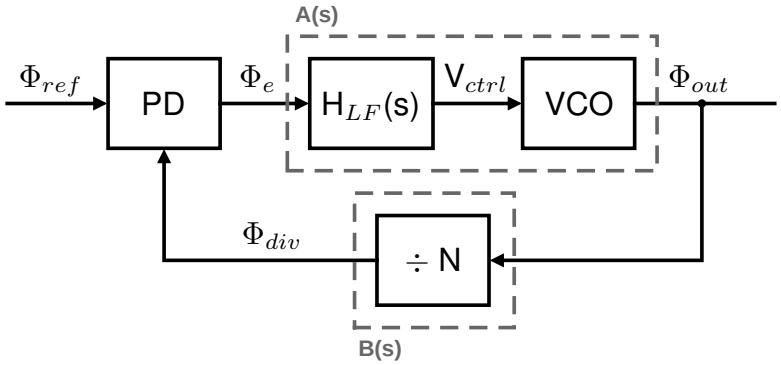


Figure 5: High-level PLL Synthesizer Architecture.

Further explaination of these components will be hereafter made.

2.4.1 Phase Detector

A phase detector acts as the summation point of figure 4, which measures the phase error Φ_e between the reference signal and the output of the PLL. The phase error then is then used by the controller, which is implemented as the loop filter. Such a phase detector may also have intrinsic gain, given by K_{PD}.

$$\Phi_e(s) = K_{PD}(\Phi_{ref}(s) - \Phi_{div}(s)) \tag{13}$$

2.4.2 Bang-bang phase detector

A simple implementation of a phase detector is a bang-bang phase detector (BBPD) [8]. As exhibited in figure 6, a BBPD outputs a value of 1 if the input Φ_Y is late relative to the reference

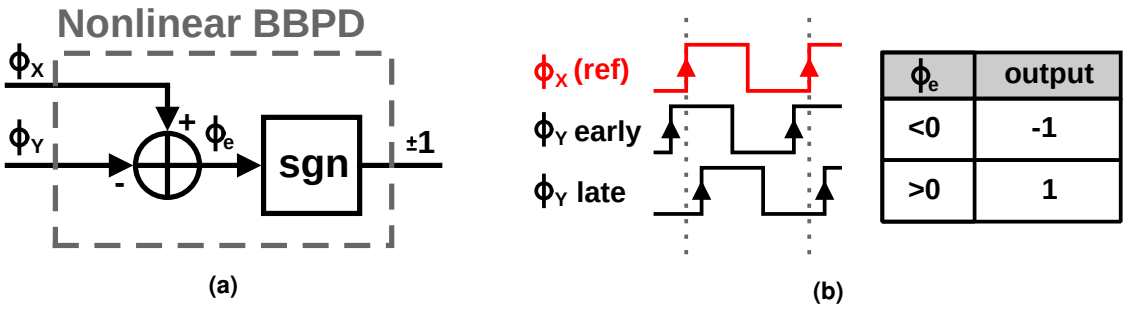


Figure 6: (a) BBPD schematic, **(b)** BBPD timing.

Φ_X (representing a clock signal), and -1 if it is early. A BBPD shows abrupt nonlinearity in its transfer characteristics. If the error signal variance $\sigma^2_{\Phi_e}$ is constant, which is expected in steady-state PLL operation, a linearized model for phase detector gain can be established [9], given in equation 14.

A linearized version of the BBPD is illustrated in figure 7. The output z valued as ± 1 (its variance σ^2_y=1).

$$K_{BBPD} = \frac{\mathbb{E}[\Phi_e(t) \cdot \mathrm{z}(t)]}{\mathbb{E}[\Phi_e^2(t)]} = \sqrt{\frac{2}{\pi}} \frac{1}{\sigma_{\Phi_e}} \tag{14}$$

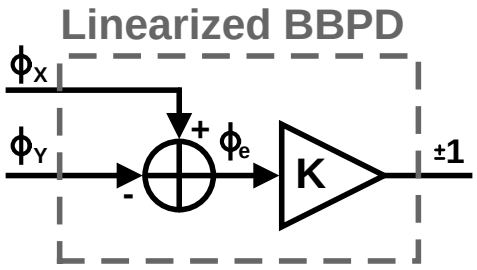


Figure 7: Linearized bang-bang phase detector.

2.4.3 BBPD Noise

Given the output of the BBPD is of fixed power σ_z^2 = 1, a linearized gain of K_{BBPD}, a phase error power of $\mathrm{Var}[\Phi_e(t)] = \sigma^2_{\Phi_e}$, and $\mathbb{E}[\Phi_e(t)] = 0$, the noise power $\sigma^2_{n_{BBPD}}$ out of the BBPD is in equation 15. $K^2_{BBPD}\sigma^2_{\Phi_e}$ represents the power of the phase error signal component post-detector, and it is assumed that noise power and signal power are uncorrelated.

$$\sigma^2_{n_{BBPD}} = \sigma_z^2 - K^2_{BBPD}\sigma^2_{\Phi_e} = 1 - \frac{2}{\pi} \tag{15}$$

Observe that the BBPD noise power is constant. If the reference signal is a clock signal with

frequency f_{ref}, the BBPD noise spectral density is in equation 16.

$$S_{n_{BBPD}(f)} = \frac{\sigma^2_{n_{BBPD}}}{\Delta f} = \frac{\left(1 - \frac{2}{\pi}\right)}{f_{ref}} \tag{16}$$

2.4.4 Divider

A divider is used as the feedback path in the PLL, where the division ratio N controls the frequency multiplication of a PLL synthesizer. The transfer function of the divider is:

$$\mathrm{H}_{div}(s) = \frac{\Phi_{div}(s)}{\Phi_{out}(s)} = \frac{1}{\mathrm{N}} \tag{17}$$

Dividers are commonly realized as digital modulo-N counters that count oscillation cycles [10]. With a division ratio of N, the output of the divider will have an active edge transition (considered to be rising edge as shown in figure 8) every N input cycles. Phase information is inferred from the output edge timing, which occurs with time interval N/f_{osc}, and is equal to the point at which output phase equals a multiple of 2π. Thus a digital divider does not provider continuous phase information, but rather a sampled phase signal with rate f_{osc}/N.

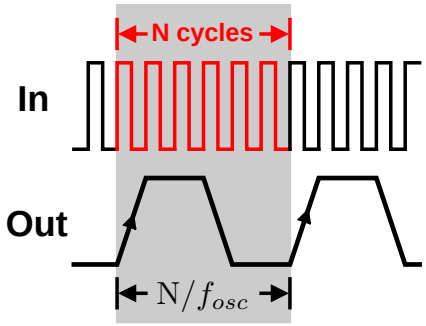


Figure 8: Digital divider signals.

2.4.5 Loop Filter

A loop filter behaves as the controller of a PLL, namely controlling the phase-frequency response of PLL. The choice of loop filter transfer function significatly affects transient PLL behavior, as well as phase noise performance, as is later described. Here, a pole-zero based controller is defined for use in this work. This is designed to have P poles and Z zeros, and can be represented in the canonical form of equation 18 as a rational function of polynomials of s

with coefficients given with $\{a_0, ..., a_P\}$ and $\{b_0, ..., b_Z\}$.

$$\mathrm{H}_{LF}(s) = \frac{\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^k} \tag{18}$$

2.4.6 Loop Filter Discretization and Digitization

In PLLs which sample on a fixed interval, defined by a reference clock frequency f_{ref}, derivation of a discrete time controller model is necessary. This is derived from the continuous canonical loop filter (equation 18) via application of a continous s-domain to discrete z-domain transformation. Strictly speaking, $z^{-1} = e^{-s\Delta T_s}$ for values on the unit circle, i.e. r=1 [11]. However, if the PLL sampling rate f_s=f_{ref} is constrained to be sufficiently higher than the implemented filter bandwidth (i.e. PLL loop bandwidth, BW_{loop}), a simpler transformation using a truncated Taylor series approximation is applicable. Given the $1/\Delta T_s$=f_s as the relation for sampling rate, then:

$$\begin{aligned}
z^{-1} &= e^{-s\Delta T_s} && \text{(definition of z on unit circle)} \\
&= \sum_{k=0}^{\infty} \frac{(-s\Delta T_s)^k}{k!} && \text{(exponential Taylor series)} \\
&\approx 1 - s\Delta T_s && \text{(if } |s\Delta T_s| = 2\pi \mathrm{BW}_{loop} \cdot \Delta T_s << 1)
\end{aligned}$$

Thus the s-to-z and z-to-s identities for the approximate transform are:

$$z^{-1} = 1 - s\Delta T_s \tag{19}$$

$$s = \frac{1}{\Delta T_s}(1 - z^{-1}) \tag{20}$$

Applying equation 20 to the general loop filter of equation 18 yields the z-domain loop filter:

$$\mathrm{H}_{LF}(z) = \mathrm{H}_{LF}(s)|_{s=\frac{1}{\Delta T_s}(1-z^{-1})} = \left.\frac{\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^k}\right|_{s=\frac{1}{\Delta T_s}(1-z^{-1})} \tag{21}$$

$$= \frac{\sum_{j=0}^{Z} \frac{b_j}{\Delta T_s^j}(1 - z^{-1})^j}{\sum_{k=0}^{P} \frac{a_k}{\Delta T_k}(1 - z^{-1})^k} \tag{22}$$

Equation 22 is transformed into a digitally implementable form by reorganizing into the canonical representation of equation 23, which then determines the tap coefficients for the sampled-

time difference equation in equation 24.

$$\mathrm{H}_{LF}(z) = \frac{\sum_{j=0}^{P} b_j' z^{-j}}{1 + \sum_{k=1}^{Z} a_k' z^{-k}} \tag{23}$$

$$y[n] = -\sum_{k=1}^{P} a_k' y[n-k] + \sum_{j=0}^{Z} b_j' x[n-j] \tag{24}$$

The obtained difference equation is directly implementable in digital hardware with a direct form-I IIR filter [12] shown in figure 9. Such a design is a cantidate for automatic synthesis of digital logic. The filter coefficients $\{a_1', ..., a_P'\}$ and $\{b_0', ..., b_Z'\}$ must be quantized into finite resolution fixed point words for a complete digital implementation. The delay elements (z^{-1} blocks) are implementable digitally as registers, the coefficient gains are implementable with array multipliers, and the adders are implementable with digital adders.

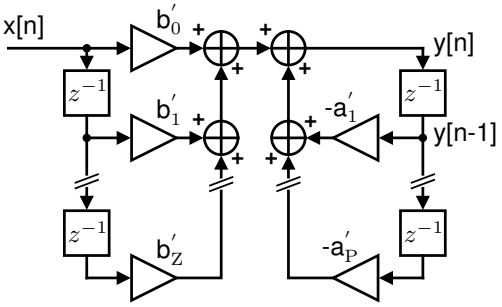


Figure 9: Direct form I implementation of IIR filter.

2.4.7 Voltage/Digitally Controlled Oscillator

A controlled oscillator is an oscillator with frequency controlled by an input signal. When this input signal takes the form of an analog voltage V_{ctrl}, it is referred to as a voltage controlled oscillator (VCO). Otherwise, when controlled digitally with an oscillator tuning work (OTW) u[n], it is referred to as a digitally controlled oscillator (DCO). Nominally, a controlled oscillator is characterized by its gain, in the case of a VCO is $K_{VCO} = \partial f / \partial \mathrm{V}_{ctrl}$. With a DCO, the gain is $K_{DCO} = \Delta f / LSB$, that is the change in frequency per least significant bit. Analyzed in terms of phase (for the VCO case), an oscillator can be seen as a time-phase integrator, provided a nominal oscillator frequency of f_0:

$$\Phi_{VCO}(t) = \Phi_{out}(t) = \int 2\pi(K_{VCO}\mathrm{V}_{ctrl}(t) + f_0)\mathrm{dt} \tag{25}$$

In the s-domain, the transfer function for a VCO is in equation 26 and equation 27 for a DCO.

$$\mathrm{H}_{VCO}(s) = \frac{\Phi_{VCO}(s)}{\mathrm{V}_{ctrl}(s)} = \frac{2\pi K_{VCO}}{s} \tag{26}$$

$$\mathrm{H}_{DCO}(s) = \frac{\Phi_{VCO}(s)}{\mathrm{u}(s)} = \frac{2\pi K_{DCO}}{s} \tag{27}$$

By application of discretization and conversion to difference equations, the sampled-time oscillator phase signals are equation 28 for a VCO and equation 29 for a DCO.

$$\Phi_{out}[n] = \Phi_{out}[n-1] + 2\pi K_{VCO}\Delta T_s \mathrm{V}_{ctrl}[n] \tag{28}$$

$$\Phi_{out}[n] = \Phi_{out}[n-1] + 2\pi K_{DCO}\Delta T_s u[n] \tag{29}$$

2.4.8 Closed Loop PLL Transfer Function

With a PLL described at the component level, the closed loop dynamics of the PLL can be computed. A PLL loop gain L(s) can be first determined (using BBPD definition for phase detector gain).

$$\mathrm{L}(s) = K_{PD}\mathrm{H}_{LF}(s)\mathrm{H}_{DCO}(s)\mathrm{H}_{div}(s) = \frac{2\pi K_{PD}K_{DCO}}{\mathrm{N}}\frac{1}{s}\frac{\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^k} \tag{30}$$

Closing the loop with the phase detector as the feedback summation point, the response of the PLL from reference to output is in equation 31.

$$\mathrm{T}(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{2\pi K_{PD}K_{DCO}\sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^{k+1} + \frac{2\pi K_{PD}K_{DCO}}{\mathrm{N}}\sum_{j=0}^{Z} b_j s^j} = \mathrm{N}\frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} \tag{31}$$

2.5 Phase noise

Phase noise can be described as undesired variation in an oscillator's phase trajectory from ideal. If an oscillator's frequency is ω_{osc}, then with additive phase noise, the phase of an oscillator is in 32.

$$\Phi_{osc}(t) = \omega_{osc}t + \Phi_n(t) \tag{32}$$

This is composed of a linear phase component $\omega_{osc}t$ and a noise component $\Phi_n(t)$. In the frequency domain, the effect of phase noise is that it broadens the tone of the oscillator, as shown in figure 10. Phase noise can be viewed as instability in terms of oscillator frequency.

2.5.1 Relation to Power spectral density

An oscillator's voltage waveform can be described in terms of a phase trajectory function $\Phi_{osc}(t)$ and amplitude A_0 in the following manner (ignoring higher harmonics):

$$V_{osc}(t) = \Re\left\{A_0 e^{j\Phi_{osc}(t)}\right\} \tag{33}$$

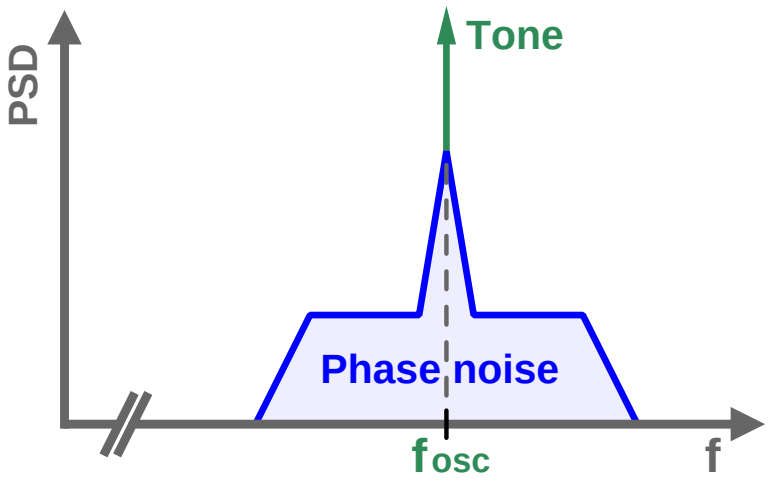


Figure 10: Effect of phase noise on frequency tone.

In an oscillator, it is desirable for phase noise to be small, and zero mean ($\mathbb{E}[\Phi_n(t)] = 0$). Using a constraint $\mathrm{Var}[\Phi_n(t)] << 1$ the following approximations can be applied to determine the oscillators spectral density in terms of the phase noise component $\Phi_n(t)$.

$$V_{osc}(t) = \Re\left\{A_0 e^{j\omega_{osc}t} e^{j\Phi_n(t)}\right\} \quad \text{(oscillator waveform)} \tag{34}$$

$$= \Re\left\{A_0 e^{j\omega_{osc}t} \sum_{k=0}^{\infty} \frac{(j\Phi_n(t))^k}{k!}\right\} \quad \text{(apply exponential Taylor series)} \tag{35}$$

$$\approx \Re\left\{A_0 e^{j\omega_{osc}t} + j\Phi_n(t) A_0 e^{j\omega_{osc}t}\right\} \quad \text{(truncate series at k=1 given } \mathrm{Var}[\Phi_n(t)] << 1) \tag{36}$$

$$= A_0 \cos(\omega_{osc}t) - \Phi_n(t) A_0 \sin(\omega_{osc}t) \quad \text{(taking real component)} \tag{37}$$

$$\tag{38}$$

The result is a carrier cosine signal, and an orthogonal sine signal modulated by the phase noise Φ_n. From this, the spectral density of the phase noise relative to the carrier can be estimated. The power spectral density $S_{V_{osc}}$ is computed in equations 39-41. Due to orthogonality of the sine/cosine components of equation 37, the cross terms that appear in the PSD computation are zero.

$$S_{V_{out}}(f) = \lim_{\Delta T \to \infty} \frac{1}{\Delta T} |\mathcal{F}\{V_{out}(t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \tag{39}$$

$$= \lim_{\Delta T \to \infty} \frac{A_0^2}{\Delta T} |\mathcal{F}\{\cos(\omega_{osc}t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \tag{40}$$

$$+ \lim_{\Delta T \to \infty} \frac{A_0^2}{\Delta T} |\mathcal{F}\{\Phi_n(t) \cdot \mathrm{rect}(t/\Delta T)\} * \mathcal{F}\{\sin(\omega_{osc}t) \cdot \mathrm{rect}(t/\Delta T)\}|^2 \tag{41}$$

$$\tag{42}$$

The noise power spectral density function of the output waveform $\mathcal{L}(\Delta f)$ is defined as the noise PSD at offset Δf from the carrier frequency f_{osc}, normalized to the carrier power. Here the PSD of the carrier component is given by equation 40, and the noise component by equation

41. Shifting equation 41 by $-\omega_{osc}$ and performing normalization for carrier power results in:

$$\mathcal{L}(\Delta f) = \lim_{\Delta T \to \infty} \frac{1}{\Delta T} |\mathcal{F}\{\Phi_n(t) \cdot \text{rect}(t/\Delta T)\}|^2 \Big|_{f=\Delta f} = S_{\Phi_n}(\Delta f) \tag{43}$$

Thus, the noise PSD $\mathcal{L}(\Delta f)$ of the PLL output waveform relative to the carrier is equal to the PSD of the phase noise signal $\Phi_n(t)$, provided Var$[\Phi_n(t)] << 1$. The PSD of $\Phi_n(t)$ is notated as $S_{\Phi_n}(\Delta f)$.

2.5.2 Leeson's model

Oscillator noise from thermal and stochastic sources is typical represented mathematically using Leeson's model for oscillator phase noise [13]. Leeson's model considers noise power density at an offset Δf from the oscillator tone (carrier). Noise power density is represented with the function $\mathcal{L}(\Delta f)$, which is the noise power density normalized to the power of the oscillator carrier tone, in other words in units of dBc/Hz. Leeson's model divides phase noise into three regions, illustrated in figure 11: (1) flicker-noise dominated, with a slope of -30 dB/decade, (2) white frequency-noise dominated, with -20 dB per decade, and (3) a flat region, limited by the thermal noise floor or amplitude noise. It is noted that phase noise components are at frequencies different than the carrier, hence are orthogonal, and can be treated as independent components that are added to the main oscillator tone signal for analysis.

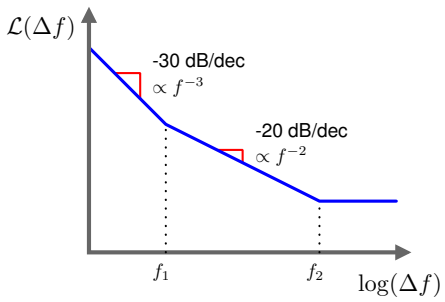


Figure 11: Phase noise regions of Leeson's model.

The equation for $\mathcal{L}(\Delta f)$ (from [14]) is in equation 44, and is dependent on temperature T, excess noise factor F, oscillator power P, oscillator Q factor, and the transition frequencies f_1 and f_2 that separate the different noise regions. It is of interest to note that the phase noise relative to the carrier will increase as power decreases, which provides challenge for creating low power oscillators with acceptable phase noise characteristics.

$$\mathcal{L}(\Delta f) = 10 \log_{10} \left[\frac{2\text{F}k_B\text{T}}{\text{P}} \left(1 + \left(\frac{f_2}{2Q\Delta f} \right)^2 \right) \left(1 + \frac{f_1}{|\Delta f|} \right) \right] = S_{\Phi n_{DCO}}(\Delta f) \tag{44}$$

For notational consistency, the following redefinition is used in the remainder of this paper: $S_{\Phi n_{DCO}}(f) = \mathcal{L}(\Delta f)|_{\Delta f = f}$

2.5.3 Phase Noise Figures of Merit

A common method to assign a figure of merit (FOM) to oscillator phase noise performance is to utilize the below relation [15]. Such a model assumes linear tradeoffs between power, frequency, and phase noise, and assumes that the rolloff of phase noise will occur with -20 dB/decade. A Lower FOM here is better.

$$\text{FOM}_{\text{pn}} = 10\log_{10}\left(\frac{\text{Power}}{1\text{ mW}}\cdot\left(\frac{\Delta f}{f_0}\right)^2\right) + \mathcal{L}(\Delta f) \tag{45}$$

Another FOM applied to PLLs is provided below, based on the RMS jitter of the PLL [16]. Here, RMS jitter is used as the phase spectrum of a PLL is often more complicated than a simple oscillator, containing spurs, in-band phase noise supression, and peaking resulting from the PLL loop filter. It should be noted that RMS jitter (in time) is tied directly to total phase noise power, as expected by Parseval's theorem [17]. Lower is better again with this FOM.

$$\text{FOM}_{\text{jitter}} = 10\log_{10}\left(\frac{\sigma_{t_j}^2}{(1\text{ s})^2}\cdot\frac{\text{Power}}{1\text{ mW}}\right) \tag{46}$$

$$\sigma_{t_j}^2 = \frac{\text{Var}[\Phi_n(t)]}{\omega_0^2} \tag{47}$$

In general, a good figure of merit is arrived to be decreasing power and/or minimizing total phase noise power.

2.5.4 Ring Oscillator Phase Noise

Oscillator phase noise for ring oscillators has a well defined limit as determined by analysis of noise of ideal RC circuits [18], which is provided in equation 48. Note that his model is limited to analyzing the-20 dB/decade part of an oscillator's spectrum as seen by Leeson's model.

$$\mathcal{L}_{min}(\Delta f) = 10\log 10\left(\frac{7.33k_BT}{P}\left(\frac{f_0}{\Delta f}\right)^2\right) \tag{48}$$

Applying this to the phase noise FOM equation 45, a limit for ring oscillator phase noise FOM is determined in equation 49.

$$\text{FOM}_{\text{jitter}}(T) = 10\log 10\,(7330k_BT) \tag{49}$$

At 300K, it is then expected that the jitter FOM for a ring oscillator should approach -165.2 dB. An example state of art comparison figure in 12 shows clustering by oscillator type of jitter FOM calculated in various published works in [19]. It is seen the FOM value calculated from theory is close to that seen implemented hardware.

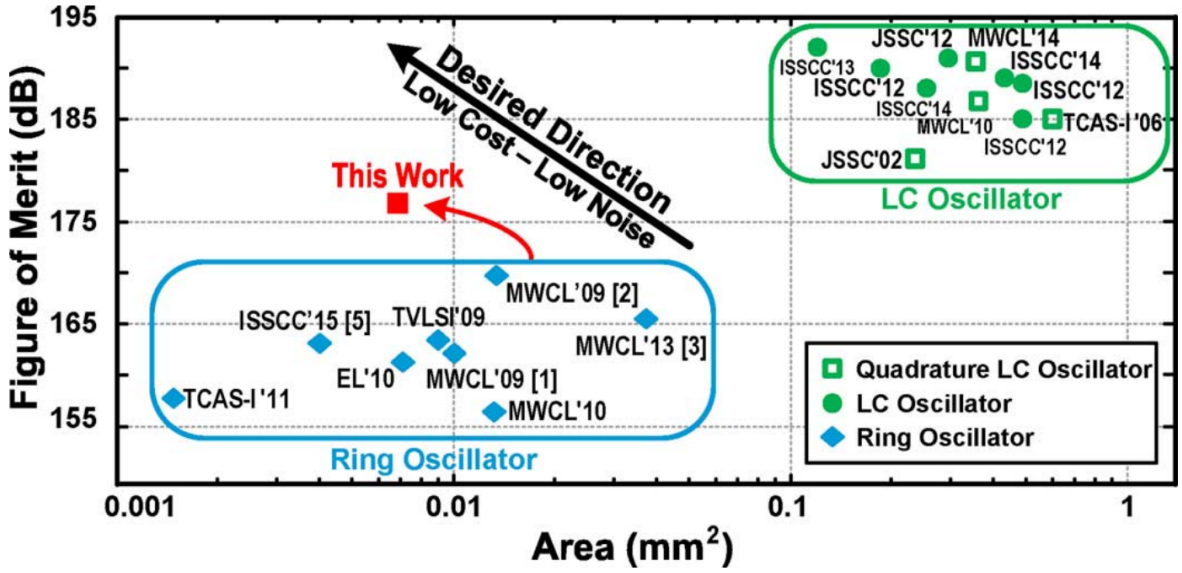


Figure 12: FOM$_{jitter}$ of various LC and ring oscillators [19].

2.6 PLL Phase Noise

Having an understanding of PLL theory, individual PLL component characteristics, and phase noise, a model for PLL phase noise can be constructed. To begin, noise sensitivity transfer functions are defined to refer each noise source to the PLL output. Here, all noise sources have been defined as additive signal components to each PLL component output. The full system noise model is in figure 13.

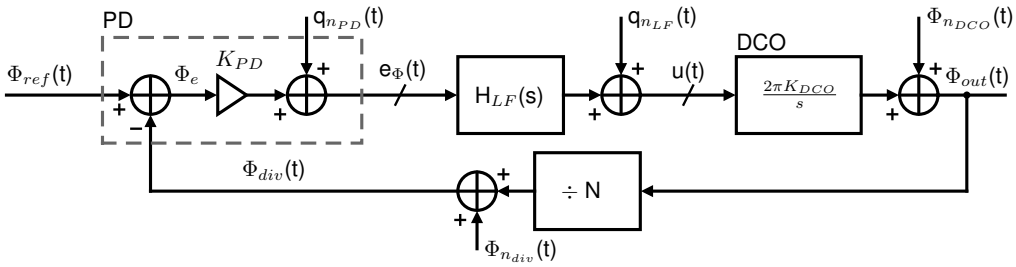


Figure 13: Full PLL additive noise model.

2.6.1 PLL Noise Transfer Functions

Following the approach of [20], a transfer function $\hat{\mathrm{T}}(s)$ is defined in equation 50 which characterizes the normalized closed loop phase response from reference input to output of the PLL.

$L(s)$ is the PLL loop gain and $T(s)$ is the PLL closed loop transfer function.

$$\hat{\mathrm{T}}(s) = \frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} \quad \text{s.t.} \quad \mathrm{T}(s) = \frac{\Phi_{out}}{\Phi_{ref}} = \mathrm{N}\hat{\mathrm{T}}(s) \tag{50}$$

Solving for the closed transfer functions between each noise source ($q_{n_{BBPD}}$, $q_{n_{LF}}$, $\Phi_{n_{DCO}}$ and $\Phi_{n_{div}}$) to the output Φ_{out} in the s-domain yields equations 51-54.

$$\frac{\Phi_{out}(s)}{q_{n_{PD}}(s)} = \frac{2\pi\frac{K_{DCO}}{s}\mathrm{H}_{LF}(s)}{1+\mathrm{L}(s)} = \frac{\mathrm{N}}{\mathrm{K_{PD}}}\frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} = \frac{\mathrm{N}}{\mathrm{K_{PD}}}\hat{\mathrm{T}}(s) \tag{51}$$

$$\frac{\Phi_{out}(s)}{\Phi_{n_{DCO}}(s)} = \frac{1}{1+\mathrm{L}(s)} = 1-\hat{\mathrm{T}}(s) \tag{52}$$

$$\frac{\Phi_{out}(s)}{q_{n_{LF}}(s)} = \frac{2\pi\frac{K_{DCO}}{s}}{1+\mathrm{L}(s)} = 2\pi\frac{K_{DCO}}{s}(1-\hat{\mathrm{T}}(s)) \tag{53}$$

$$\frac{\Phi_{out}(s)}{\Phi_{n_{div}}(s)} = \frac{K_{BBPD}2\pi\frac{K_{DCO}}{s}\mathrm{H}_{LF}(s)}{1+\mathrm{L}(s)} = \mathrm{N}\frac{\mathrm{L}(s)}{1+\mathrm{L}(s)} = \mathrm{N}\hat{\mathrm{T}}(s) \tag{54}$$

2.6.2 PLL Output-referred Noise

Using the noise transfer functions, the expressions for noise power spectrum of the BBPD (equation 16) and the noise spectrum of a ring oscillator (equation 48), the PLL output phase noise spectrum of each component is determined by multiply the respective noise transfer function with the respective noise spectral density. Here it is found that the BBPD noise component out of the PLL is given in equation 55, and the oscillator component is given in equation 56. The loop filter and divider components are here ignored, as they will be shown not be relevant in this work.

$$S_{\Phi n_{BBPD,out}}(f) = S_{n_{BBPD}}(f)\left|\frac{\Phi_{out}(f)}{q_{n_{BBPD}}(f)}\right|^2 = \frac{\left(\frac{\pi}{2}-1\right)}{f_{ref}}\left|\sigma_{\Phi_e}\mathrm{N}\hat{\mathrm{T}}(f)\right|^2 \tag{55}$$

$$S_{\Phi n_{DCO,out}}(f) = \mathcal{L}_{min}(f)\left|\frac{\Phi_{out}(f)}{q_{n_{DCO}}(f)}\right|^2 = \frac{7.33k_BT}{P}\left(\frac{f_0}{\Delta f}\right)^2|1-\hat{\mathrm{T}}(\Delta f)|^2 \tag{56}$$

The total output noise power spectral density is given as the sum of the components, presuming independence of all noise sources. Following the results of section 2.5.1, which determined that oscillator power spectrum is equivalent to the phase noise power spectrum for zero mean phase noise with low power, the final oscillator power spectrum at Δf from the carrier is in equation

57.

$$S_{n_{PLL}}(f_{osc}+\Delta f) = S_{\Phi n_{BBPD,out}}(\Delta f) + S_{\Phi n_{DCO,out}}(\Delta f) \tag{57}$$

$$= \frac{\left(\frac{\pi}{2}-1\right)}{f_{ref}}\left|\sigma_{\Phi_e}\mathrm{N}\hat{\mathrm{T}}(\Delta f)\right|^2 + \frac{7.33k_BT}{P}\left(\frac{f_0}{\Delta f}\right)^2 |1-\hat{\mathrm{T}}(\Delta f)|^2 \tag{58}$$

A complexity arises in equation 57 due to the fact that the power spectum is a function of the root mean squared (RMS) phase error, σ_{Φ_e}. σ_{Φ_e} may be calculated as equation 59. Computation of the power spectrum therefore requires derivation of a closed form solution for σ_{Φ_e} accounting for the PLL transfer function, which coupled with PLL power spectral density equation can be solved in a system of equations to result in a closed form solution of the power spectral density.

$$\sigma_{\Phi_e} = \sqrt{2\int_0^\infty S_{n_{PLL}}(f_{osc}+\Delta f)d\Delta f} \tag{59}$$

3 Design

The primary objective in this work is to obtain a very low 100μW power consumption for a 2.448 GHz PLL frequency synthesizer, while achieving a carrier-to-noise ratio for the synthesized signal of >20 dB. Consequently, the design philosophy adhered to in this work is pursue simplicity wherever possible, in order to reduce number of sources of power draw and noise. Furthermore, this design is targeted to allow duty cycled operation to further reduce power. Thus, an all-digital architecture has been selected to enable the possibility to save the PLL state, enter an ultra-low-power sleep state, and then resume from the stored state rapidly, without requiring relocking of the PLL.

3.1 Proposed Architecture - ADPLL

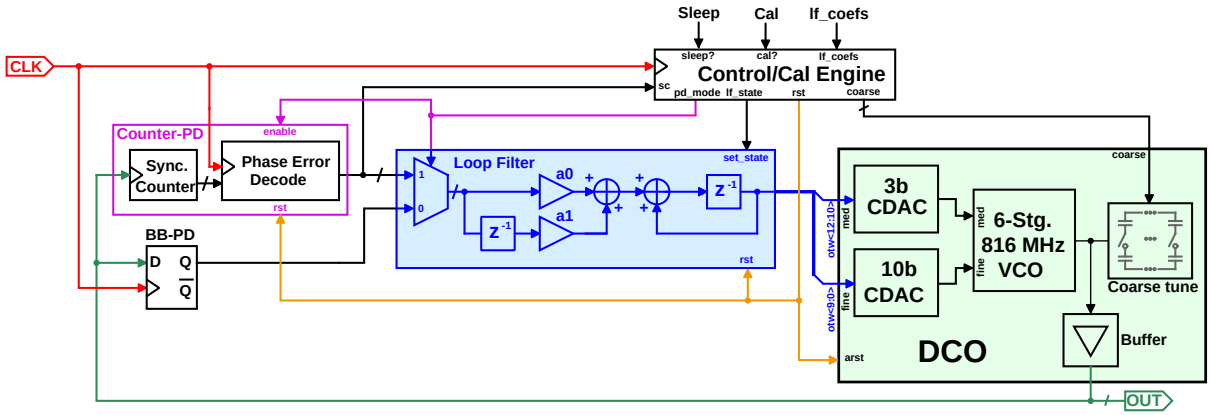


Figure 14: ADPLL Architecture.

The undertaken PLL architecture is in figure 14. It comprises primarily of five components: (1) counter-based phase detector for initial start up, (2) bang-bang phase detector for steady state feedback, (3) proportional-integral controller loop filter, (4) DCO implemented as a VCO plus capacitive DACs, and (5) a control and calibration engine, consisting of digital logic. This design was achieved via minimization of complexity. First, the need of a divider is removed from the design by the usage of both the counter phase detector and BBPD. For initial cold start up of the PLL from an unknown state, the counter-based phase detector functions as a low-resolution replacement for a divider and linear phase detector. When near steady state, the counter-PD is disabled and replaced by BBPD feedback, which will maintain the PLL at steady state. The removal of a divider results in lower power consumption, and less noise added in-loop. The usage of only a BBPD in steady state further reduces power, as it is a minimum complexity phase detector. This is expected without significant performance degredation, as with proper optimization, BBPD PLLs can obtain comparable perform to linear charge-pump style PLLs [9]. Additional power improvements are obtained in the usage of digital logic to implement the loop filter, using a simple PI-controller architecture. The final power saving move

is implemented in a DCO based on the combination of several CDACs with a voltage controlled ring oscillator. This reduces to near zero the static curent draw associated with control of the VCO. The overall design is implemented with no static current paths, other than that associated with leakage, achieved by favoring static logic derived components throughout the PLL.

A further feature gained in the proposed all-digital architecture is the ability to abruptly save the state of the PLL digitally and place it into an ultra low power sleep mode, and then later resume the PLL from the saved state. Figure 15 demonstrate such operation, where t_{l1} is the lock time from cold start, and t_{l2} is the time to relock from a resume. This functionality enables the ability to rapidly duty cycle the PLL between active and sleep states, with minimal time to relock. Power consumption of the PLL is reduced by a factor that is the duty cycle which it is operated, and in this design can enable as low as 1μW power consumption as 1% duty cycle.

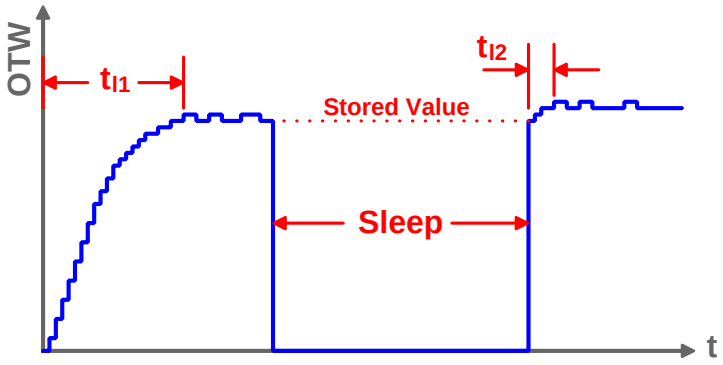


Figure 15: PLL sleep and resume operation.

The proposed digital architecture also enables a form of fast-locking via gear switching of the loop filter [21]. In this work, the counter-based TDC is initially used for large frequency and phase errors with a loop filter optimized for speed, which after locking can be changed (gear-switched) to a BBPD optimized loop filter chosen to minimize total phase-noise. Design of optimal filters will be discused later on.

3.1.1 Power budget

The below power budget was used in the design process to divide up the 100 μW allotment between the different PLL components. In order to minimize oscillator phase noise, as large of a portion was allotted to the oscillator, being 80%.

DCO	Phase detector	Digital (LF)	Other	SUM
80 μW	10 μW	10 μW	0 μW	$\leq$ 100 μW

3.1.2 Floorplan

The below floor plan (dimensions in microns) has been devised to meet the area requirement of $< 0.01\ \text{mm}^2$.

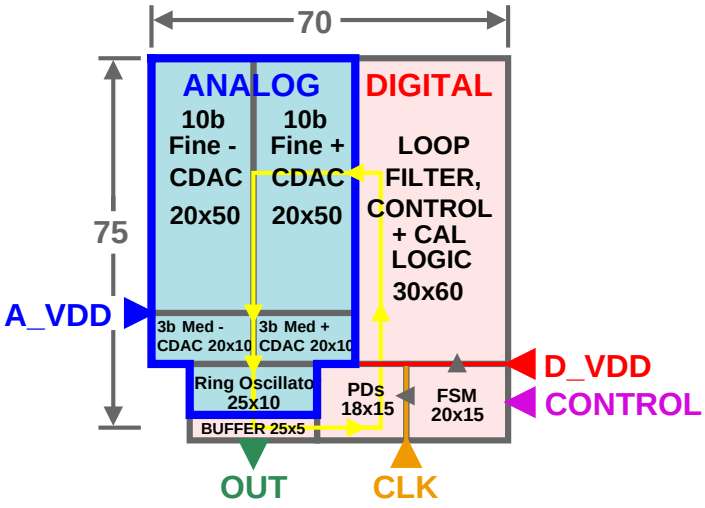


Figure 16: PLL floorplan.

3.1.3 Dividerless PLL

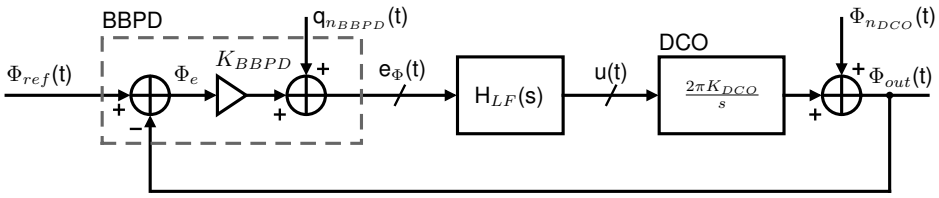


Figure 17: BBPD-PLL full noise model.

In the PLL theory (section 2.6.2), the derived PLL detector phase noise component (equation 55) contains a term proportional to N^2, that is the detector noise will grow with the square of the PLL divider ratio. It is, however, possible to remove this N^2 dependency by usage of oscillator sub-sampling within the PLL [22]. This is achieved by directly sampling the PLL output at a rate equivalent to the reference frequency. This is equivalent to removing the divider from the PLL loop and directly connecting the PLL output to the phase detector, which has been employed in this work (see figure 14). To lock to the desired frequency, though, it must be guaranteed that the PLL frequency at the start of sub-sampling operation be within $f_{ref}/2$ of the target frequency (the PLL will lock to the nearest multiple of the reference frequency). In this work, this is achieved through sequencing at startup through two phase detectors. A synchronous counter phase detector (which emulates both a divider and phase detector) initially locks the PLL within $f_{ref}/2$ of the target frequency, after which the PLL is operated in sub-sampling bang-bang phase detector.

In accordance to the change to a dividerless operation, the PLL closed loop transfer function has been rederived in equation 60. Furthermore, new expressions for PLL output phase noise with a BBPD is given in equation 61, and PLL output oscillator noise with a ring oscillator is given in equation 62, for the noise model in figure 17. Noise due to the loop filter here is ignored, as it will be possible to adjust the loop filter datapath resolution to make digital quantizaiton noise effects negligible.

$$\mathrm{T}(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{2\pi K_{BBPD} K_{DCO} \sum_{j=0}^{Z} b_j s^j}{\sum_{k=0}^{P} a_k s^{k+1} + 2\pi K_{BBPD} K_{DCO} \sum_{j=0}^{Z} b_j s^j} = \frac{\mathrm{L}(s)}{1 + \mathrm{L}(s)} \tag{60}$$

$$S_{\Phi n_{BBPD,out}}(f) = S_{n_{BBPD}}(f) \left| \frac{\Phi_{out}(f)}{q_{n_{BBPD}}(f)} \right|^2 = \frac{\left(\frac{\pi}{2} - 1\right)}{f_{ref}} \left| \sigma_{\Phi_e} \mathrm{T}(f) \right|^2 \tag{61}$$

$$S_{\Phi n_{DCO,out}}(f) = \mathcal{L}_{min}(f) \left| \frac{\Phi_{out}(f)}{q_{n_{DCO}}(f)} \right|^2 = \frac{7.33 k_B T}{P} \left(\frac{f_0}{f} \right)^2 |1 - \mathrm{T}(f)|^2 \tag{62}$$

3.2 Bang-Bang Phase Detector

A bang-bang phase detector, as introduced in section 2.4.2, can be implemented physically with a D flip-flop [23] and logic to map the logical state to a signed ± 1 value that may be passed into a digital loop filter. This is shown in figure 18.

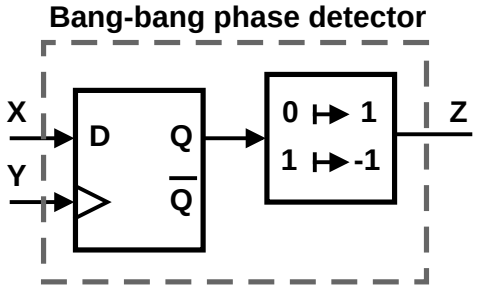


Figure 18: Bang-bang phase detector with D flip-flop.

The realization of a BBPD using a digital flip flop introduces additional noise to the system in the form of jitter. Jitter arises as an artifact of circuit and supply noise. For small time differentials between the BBPD inputs X and Y, the output can be stochatically corrupted due to the presence of noise. Furthermore, physical D flip flop implementations exhibit set-up and hold time requirements for data to be stable (to allow internal nodes to settle), so deterministic corruption of phase detection can be imparted if the inputs violate physical timing requirements. These sources of corruption cause BB-PD transfer characteristics in terms of output expectation, $\mathbb{E}[Z]$, with respect to input timing difference Δt_{XY} to deviate from an ideal step response, demonstrated in figure 19. Analytically, the corruption of the transfer characteristic can be viewed as being caused by an additive phase noise component before the signum operation in

the BBPD, as shown in figure 20a. The expectation $\mathbb{E}[Z(\Delta t_{XY})]$ acts as a cumulative distribution function (CDF) for this phase noise component. Thus, differentiation of $\mathbb{E}[Z(\Delta t_{XY})]$ results in a probability distribution function (PDF) P(T=Δt_{xy}) of this phase noise signal. Statistical analysis of variance of the PDF provides an RMS value for timing jitter of this additive noise source, $\sqrt{\mathrm{Var}[T]} = \sigma_{t,j}$. The RMS timing jitter may be converted to RMS phase error of the noise source as $\sigma_{\Phi_j} = 2\pi f_{osc}\sigma_{t_j}$. This analysis approach is applied in this work to evaluate BBPD performance.

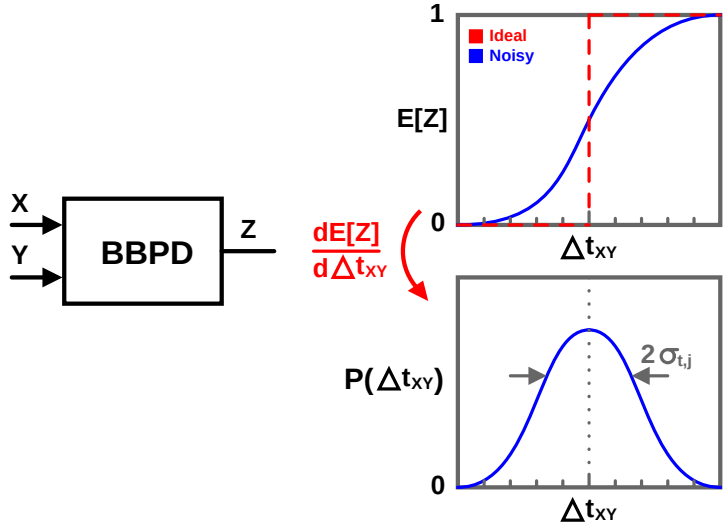


Figure 19: BBPD output expectation and jitter PDF versus input time differential.

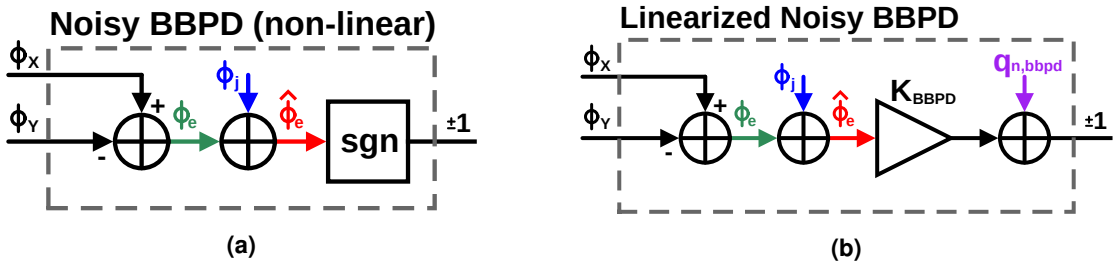


Figure 20: (a) Noisy BBPD nonlinear model **(b)** Noisy BBPD linearized model

With a model for BBPD noise due to implementation non-idealities, a modified linearized model for the BBPD will be established here. This model will reconcile the ideal BBPD noise introduced in section 2.4.3 with the noise due to the new additive jitter component just described. First, a component representing the non-ideal jitter component, Φ_j, is added into noise model from figure 17. The result is the linearized model of figure 20b. We then define a modified phase error, $\hat{\Phi}_e$, which includes the nominal Φ_e and the jitter corruption:

$$\hat{\Phi}_e = \Phi_e + \Phi_j. \tag{63}$$

$\hat{\Phi}_e$ has a variance defined as $\sigma^2_{\hat{\Phi}_e} = \sigma^2_{\Phi_e} + \sigma^2_{\Phi_j}$, assuming Φ_e and Φ_j are uncorrelated. Defining

BBPD gain in terms of $\sigma_{\hat{\Phi}_e}$:

$$K_{BBPD} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sigma_{\hat{\Phi}_e}} = \sqrt{\frac{2}{\pi}} \cdot \frac{1}{\sqrt{\sigma^2_{\Phi_e} + \sigma^2_{\Phi_j}}} \tag{64}$$

It is then observed that the output Z is valued ± 1, thus its power is always σ^2_Z=1. Furthermore:

$$\sigma^2_Z = 1 = K^2_{BBPD}(\sigma^2_{\phi_e} + \sigma^2_{\phi_j}) + \sigma^2_{q_{n,BBPD}} \tag{65}$$

As determined in section 2.4.3, it is inherent that $\sigma^2_{q_{n,BBPD}} = 1 - \frac{2}{\pi}$. If the total output noise

$$\sigma^2_{\phi_{n,BBPD}} = \sigma^2_{q_{n,BBPD}} + K^2_{BBPD}\sigma^2_{\phi_j} = 1 - \frac{2}{\pi}\frac{\sigma^2_{\phi_e}}{\sigma^2_{\phi_j} + \sigma^2_{\phi_e}} \tag{66}$$

If the BB-PD is connected directly to oscillator output, $\sigma^2_{\phi_e} = \sigma^2_{\phi_n}$, i.e. the PLL output phase noise. The spectral density of the BB-PD phase noise is then:

$$S_{\phi_{n,BBPD}} = \frac{\sigma^2_{\phi_{n,BBPD}}}{f_{ref}} = \frac{1 - \frac{2}{\pi}\frac{\sigma^2_{\phi_n}}{\sigma^2_{\phi_j}+\sigma^2_{\phi_n}}}{f_{ref}} \tag{67}$$

$$S_{\Phi n_{BBPD,out}}(f) = S_{n_{BBPD}}(f)\left|\frac{\Phi_{out}(f)}{q_{n_{BBPD}}(f)}\right|^2 = \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}}\left|\mathrm{T}(f)\right|^2 \tag{68}$$

3.2.1 Circuit

The physcial implementation of the bang-bang phase detector has been selected to utilize a true single phase clock (TSPC) D-flip flop [24]. The positive-edge triggered variant of this circuit has been implemented as shown in figure 21. Selection of this topology was based on the desire for the usage of a single ended clock as a reference signal.

This TSPC design was validated in simulation with RVT devices with all devices set with (W/L) = {100n/20n, 200n/20n}, and with supply voltages of 0.5 and 0.8 volts. Results for jitter PDF are in figure 22, and the RMS jitter and power consumption are in table 2. For implementation (W/L) = 100n/20n was selected for all devices, as to ensure that the budgeted power of 10 μW is met with layout parasitics.

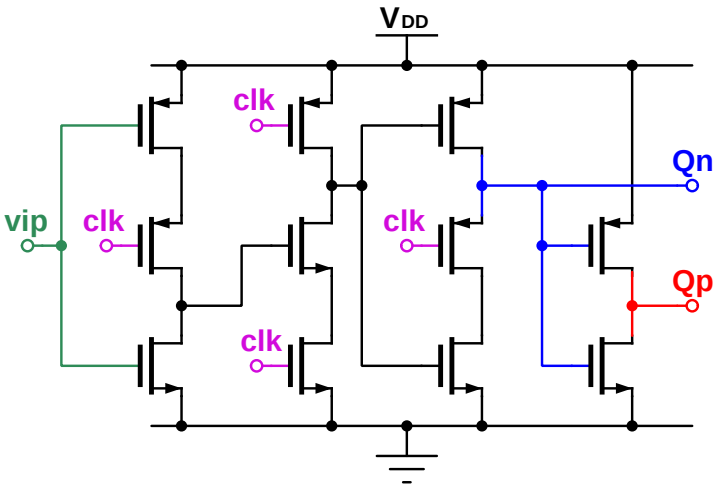


Figure 21: True single-phase clock (TSPC) D flip-flop, positive edge triggered.

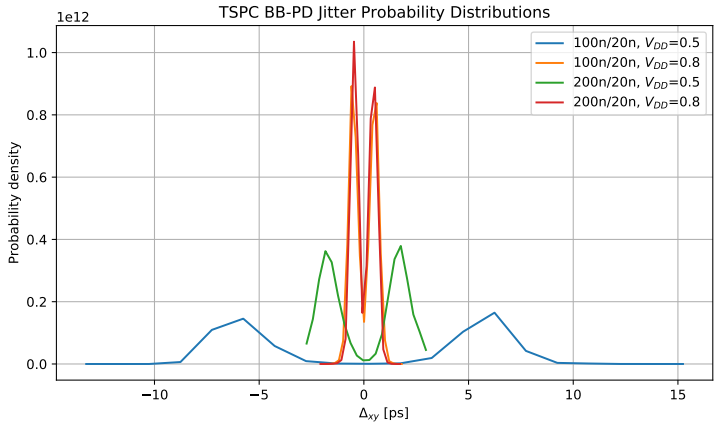


Figure 22: Jitter PDF from simulated TSPC DFFs.

(W/L)	Supply [V]	RMS jitter [ps]	Power [μW]
100n/20n	0.5	6.01	1.64
100n/20n	0.8	0.832	3.942
200n/20n	0.5	1.776	2.215
200n/20n	0.8	0.496	4.591

Table 2: Schematic simulation of TSPC DFF.

3.2.2 Layout

Area?

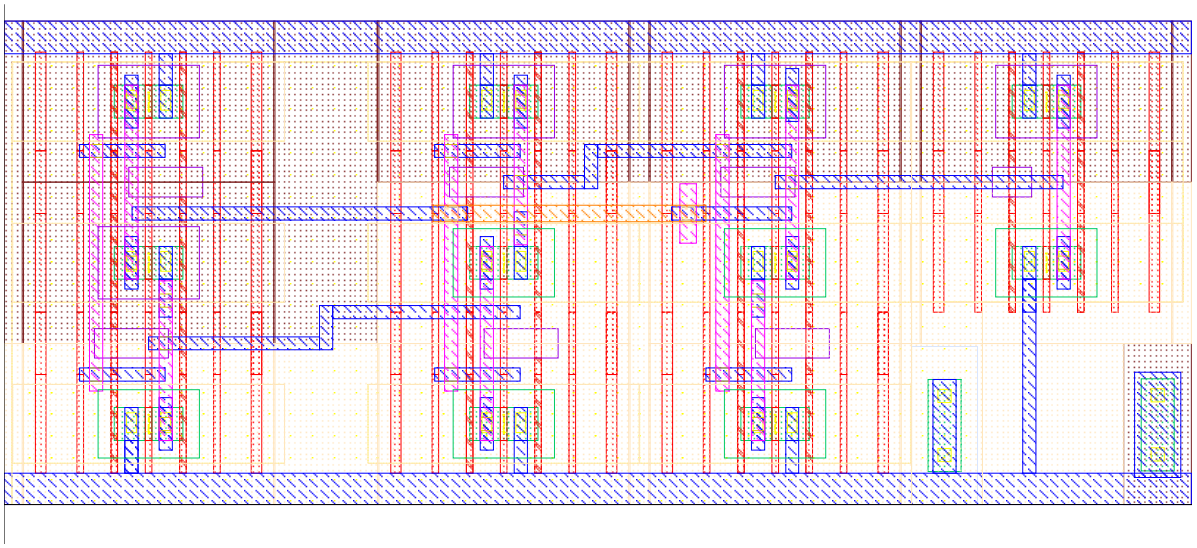


Figure 23: Single ended bang-bang phase detector.

3.3 Loop Filter

For selection of a loop filter, some basic criteria have been selected:

1. Zero steady state phase error, to ensure accuracy of synthesized frequency.
2. Minimize complexity of implemented logic, i.e. minimize the number of poles and zeros.
3. Low pass response of PLL in closed-loop.

From this author's previous work [1], it was established that the pole-zero filter satisfying these requirements is a proportional-integral controller.

3.3.1 Proportional-integral Loop Filter

A proportional-integral controller [25] is given in equation 69, containing an proportional gain term K_p, and an integral gain term K_p. This can be optionally represented using a pole at zero and a zero with $\omega_z = K_i/K_p$:

$$\mathrm{H}_{LF}(s) = K_p + \frac{K_i}{s} = \frac{K_i}{s}\left(\frac{s}{\omega_z} + 1\right) \tag{69}$$

Substitution of this controller into the PLL closed loop transfer function (equation 60) results in:

$$T(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{2\pi K_{BBPD} K_{DCO} K_i \left(\frac{s}{\omega_z} + 1\right)}{s^2 + 2\pi K_{BBPD} K_{DCO} K_i \left(\frac{s}{\omega_z} + 1\right)} \tag{70}$$

3.3.2 Optimal Filter Selection

Optimization of loop filter will be attempted to minimizing the total integrated phase noise power out of the PLL, while keeping the filter bandwidth low enough to acheive satisfactory oversampling for acceptable performance. A limit of loop bandwidth BW_{loop} = $0.1 f_{ref}$ is employed here, which is a figure commonly cited in PLL literature from [26]. Higher degrees of oversampling lead to deviations between continuous PLL models and real sampled-PLL performance.

First, some mathematical simplifications of the PLL model are introduced. Rewriting equation 70 with substitutions $\omega_z = K_i/K_p$ and K = $2\pi K_{BBPD} K_{DCO} K_i$:

$$T(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{s\frac{K}{\omega_z} + K}{s^2 + s\frac{K}{\omega_z} + K} \tag{71}$$

The denominator can be redefined in terms of a natural frequency ω_n and damping ratio ζ:

$$s^2 + s\frac{K}{\omega_z} + K = s^2 + s2\zeta\omega_n + \omega_n^2 \tag{72}$$

Thus, $\omega_n = \sqrt{K}$, and $\omega_z = \sqrt{K}/2\zeta$. The poles of equation 71 are then located at s = $\zeta\sqrt{K} \pm j\sqrt{K}\sqrt{1-\zeta^2}$. The settling time constant of the PLL is determined by the real portion of dominant pole of equation 71:

$$\tau = \frac{1}{|\min(\Re(\{s_{p1}, s_{p2}\}))|} \tag{73}$$

It is decidedly of interest to minimize settling time of the PLL (i.e. time constant), thus maximizing the frequency of the dominant pole of the PLL is of interest. Based on the pole-zero plot of figure 24, it is seen the dominant pole of equation 71 is maximized with $\zeta = 1$. The shown pole and zero loci are oriented based on increasing ζ values. According to Razavi [6], ζ is usually "chosen to be $> \sqrt{2}/2$ or even 1 to avoid excessive ringing." It has according been chosen to fix $\zeta = 1$ for the PI-controller.

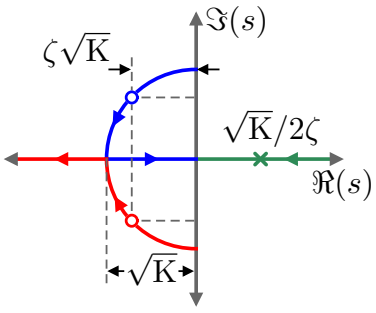


Figure 24: PI-controller PLL pole-zero locations.

To illustrate the effect of the damping ratio ζ, figure 25 illustratesexample frequency and step responses of a PI-controlled PLL. It is observed that increasing ringing and peaking is obtained with increasing values of ζ. This is undesirable from a stability standpoint, and increased peaking in the PLL transfer function will increase output phase noise contributions, also undesirable. Therefore, the selection of $\zeta = 1$ is solidified.

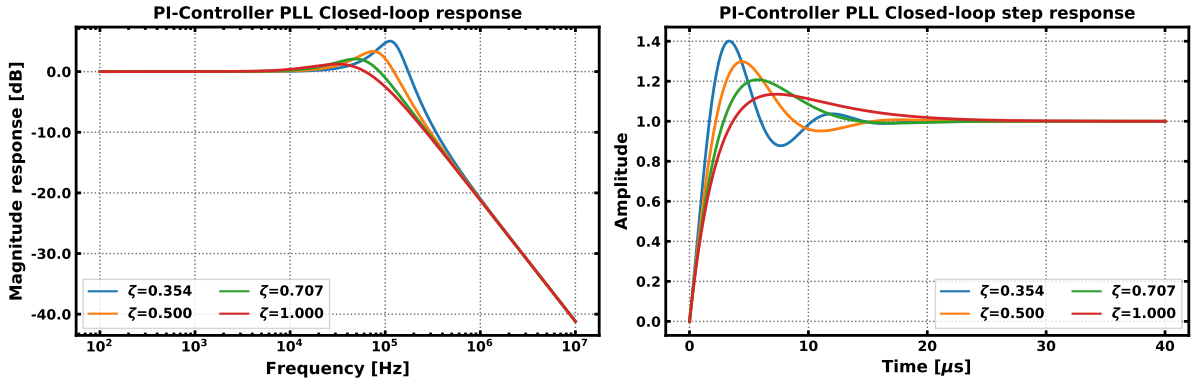


Figure 25: Example PI-PLL responses with varied ζ.

With ζ is constrained to 1, the final simplified PLL closed loop transfer function is in equation 74. The form of this equation is favorable for integration, due to the selection of ζ=1.

$$T(s) = \frac{2\sqrt{K}s + K}{s^2 + 2\sqrt{K}s + K} \tag{74}$$

Now, the PLL output referred noise power of the oscillator and BBPD may be calculated. First, if the PLL-less oscillator is defined as equation 75, where $S_{0_{osc}}$ is defined as the oscillator spectral density at 1 Hz frequency offset from the carrier.

$$\mathcal{L}(f) = \frac{S_{0_{osc}}}{f^2} \tag{75}$$

The PLL output spectum is then computed as:

$$S_{\Phi n_{DCO,out}}(f) = \frac{S_{0_{osc}}}{f^2}|1 - \mathrm{T}(f)|^2 \tag{76}$$

Now, $|1 - \mathrm{T}(f)|^2$ is found to be after much simplification:

$$|1 - \mathrm{T}(f)|^2 = \frac{f^4}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{77}$$

Thus, re-evaluating equation 76 yields:

$$S_{\Phi n_{DCO,out}}(f) = S_{0_{osc}} \frac{f^2}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{78}$$

The total PLL phase noise power associated with the oscillator, $\sigma^2_{\Phi_{n,DCO}}$ is achieved by integrating equation 79 with respect to frequency.

$$\sigma^2_{\Phi_{n,DCO}} = \int_{-\infty}^{\infty} S_{\Phi n_{DCO,out}}(f)df = S_{0_{osc}} \int_{-\infty}^{\infty} \frac{f^2}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} df \tag{79}$$

$$= S_{0_{osc}} \frac{\pi^2}{\sqrt{K}} \tag{80}$$

Next, the total BBPD noise at the PLL output is computed. The expression for BBPD noise density in equation 68 will be used, and for which $|\mathrm{T}(f)|^2$ must be computed. This is:

$$|\mathrm{T}(f)|^2 = \frac{4\frac{K}{(2\pi)^2}f^2 + \frac{K^2}{(2\pi)^4}}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{81}$$

The resulting BBPD spectral density equation is:

$$S_{\Phi n_{BBPD,out}}(f) = \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}} |\mathrm{T}(f)|^2 \tag{82}$$

$$= \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}} \cdot \frac{4\frac{K}{(2\pi)^2}f^2 + \frac{K^2}{(2\pi)^4}}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} \tag{83}$$

The total PLL phase noise power associated with the BBPD, $\sigma^2_{\Phi_{n,BBPD}}$ is achieved by integrating equation 84 with respect to frequency:

$$\sigma^2_{\Phi_{n,BBPD}} = \frac{\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}}{f_{ref}} \int_{-\infty}^{\infty} \frac{4\frac{K}{(2\pi)^2}f^2 + \frac{K^2}{(2\pi)^4}}{\left(f^2 + \frac{K}{(2\pi)^2}\right)^2} df \tag{84}$$

$$= \frac{5\sqrt{K}}{4f_{ref}} \cdot \left[\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}\right] \tag{85}$$

The total noise out of the PLL is therefore the sum of $\sigma^2_{\Phi_{n,BBPD}}$ and $\sigma^2_{\Phi_{n,DCO}}$:

$$\sigma^2_{\phi_n} = \sigma^2_{\Phi_{n,DCO}} + \sigma^2_{\Phi_{n,BBPD}} = S_{0_{osc}} \frac{\pi^2}{\sqrt{K}} + \frac{5\sqrt{K}}{4f_{ref}} \cdot \left[\frac{\pi}{2}(\sigma^2_{\phi_j} + \sigma^2_{\phi_n}) - \sigma^2_{\phi_n}\right] \tag{86}$$

Reorganization of equation 86 in terms of $\sigma^2_{\phi_n}$ yields:

$$\sigma^2_{\phi_n} = \frac{S_{0_{osc}} \frac{\pi^2}{\sqrt{K}} + \frac{5\pi\sqrt{K}}{8f_{ref}} \sigma^2_{\phi_j}}{1 - \frac{5\sqrt{K}}{4f_{ref}}(\frac{\pi}{2} - 1)} \tag{87}$$

In the special case of an ideal BBPD where $\sigma^2_{\phi_j}$ = 0, the optimal value of K that minimizes total phase noise can be determined by solving for $d\sigma^2_{\phi_n}/dK = 0$, yielding:

$$K_{opt} = \left(\frac{4}{5} \cdot \frac{f_{ref}}{\pi - 2} \right)^2 \tag{88}$$

The corresponding optimal value of $\sigma^2_{\phi_n}$ is in equation 89. This should be the absolute best case achievable with a BBPD PLL with a PI-controller. For this design, with 80μW oscillator power at 2.448 GHz, 16 MHz reference, and 300K ambient temperature, the theoretical best attainable phase noise is $\sigma^2_{\phi_{n,opt}} = 0.004$, or a CNR of 24 dB, above the desired 20 dB. Therefore, the current design targets are feasible.

$$\sigma^2_{\phi_{n,opt}} = \frac{5\pi^2 S_{0_{osc}}}{f_{ref}} \left(\frac{\pi}{2} - 1 \right) \tag{89}$$

In the presence of a non-ideal phase detector having phase noise power $\sigma^2_{\phi_j} = (2\pi f_{osc})^2 \sigma^2_{t_j}$, the optimal value K that minimizes phase noise is obtained as the root of $d\sigma^2_{\phi_n}/dK = 0$ in equation 90. The obtained result for K_{opt} may be substitued into equation 87 to determine the total noise power $\sigma^2_{\phi_n}$.

$$K_{opt} = \left[\frac{S_{0_{osc}} \pi(\pi - 2)}{\sigma^2_{\phi_j}} - \sqrt{\frac{S^2_{0_{osc}} \pi^2 (\pi - 2)^2}{\sigma^4_{\phi_j}} + \frac{S_{0_{osc}} 8\pi f_{ref}}{5\sigma^2_{\phi_j}}} \right]^2 \tag{90}$$

The parameter of K has a direct relationship to the closed loop bandwidth BW_{loop} of the PLL, which is determined by solving $|T(f)|^2 = 0.5$. The result is given in equation 91.

$$BW_{loop} = \frac{1}{2\pi} \sqrt{K} \sqrt{3 + \sqrt{10}} \tag{91}$$

As mentioned before, it is advisable to observe a limit of loop bandwidth BW_{loop} = $0.1 f_{ref}$. The coefficient α is defined here now to describe the loop bandwidth-reference frequency ratio, where $BW_{loop} = \alpha f_{ref}$. Interestingly, solving the system of equations given by equation 88 and equation 91 provides an ideal ratio of BW_{loop} and f_{ref}, being α=0.28, which exceeds the rule of thumb α=0.1. Thus, in the case that α must be constrained for sampling reasons, equation

92 is found to determine K. Thus with a 16 MHz referece, and α=1, $K = 1.64 \times 10^{13}$.

$$K_\alpha = \frac{(2\pi\alpha f_{ref})^2}{3+\sqrt{10}} \tag{92}$$

It is best to be as near to the optimal value of α as possible. Figure 26 demonstrates the effect of α on the phase noise power (normalized to the optimal value). It is seen that the total phase noise asymptotically grows to infinity as α approaches 0 and 0.55. In the case of α=0.1, the phase noise is expected to be 1.69 times the optimal value, resulting in a 2.3 dB degredation from optimal, implying that the best case CNR is 21.7 dB with 80μW oscillator power at 2.448 GHz, 16 MHz reference, and 300K ambient temperature.

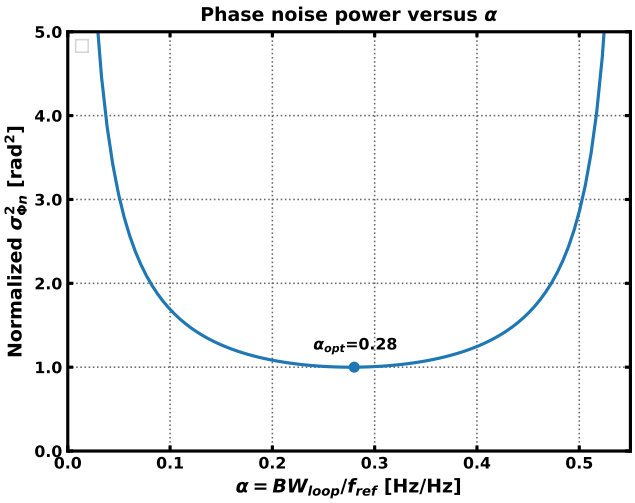


Figure 26: Phase noise power (normalized) versus α.

It is possible to derive a constraint for BBPD jitter $\sigma^2_{\phi_j}$ in terms of α and a target $\sigma^2_{\phi_n}$ (i.e. CNR value), which allows for the performance specification for the physical BBPD to be set. Equation 93 defines the maximum allowable phase noise power due to BBPD jitter, and equation 94 defines the maximum RMS timing jitter of the same detector. In the case of 2.448 GHz operation, with 20 dB of CNR, and α = 0.1, the maximum allowable RMS BBPD jitter is σ_{t_j} = 4.75 ps.

$$\sigma^2_{\phi_j} \leq \sigma^2_{\phi_n}\left[\frac{4\sqrt{3+\sqrt{10}}}{5\pi^2\alpha}+\frac{2}{\pi}-1\right]-\frac{2S_{0_{osc}}(3+\sqrt{10})}{5\pi\alpha^2 f_{ref}} \tag{93}$$

$$\sigma_{t_j} \leq \frac{1}{2\pi f_{osc}}\sqrt{\sigma^2_{\phi_n}\left[\frac{4\sqrt{3+\sqrt{10}}}{5\pi^2\alpha}+\frac{2}{\pi}-1\right]-\frac{2S_{0_{osc}}(3+\sqrt{10})}{5\pi\alpha^2 f_{ref}}} \tag{94}$$

Now with theory in place to optimize PLL performance, mapping of the optimal parameter K onto the loop filter of equation 69 will be considered. Recall that $\omega_z = K_i/K_p = \sqrt{K}/2\zeta$ and

$K = 2\pi K_{BBPD} K_{DCO} K_i$. The parameters K_i, K_p, and ω_z are thus provided in equations 95-97.

$$\omega_z = \frac{\sqrt{K}}{2} \tag{95}$$

$$K_p = \frac{\sqrt{K}}{\pi K_{BBPD} K_{DCO}} = \frac{\sqrt{K}\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{\sqrt{2\pi} K_{DCO}} \tag{96}$$

$$K_i = \frac{K}{2\pi K_{BBPD} K_{DCO}} = \frac{K\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{2\sqrt{2\pi} K_{DCO}} \tag{97}$$

3.3.3 Settling Time

If ζ is constrained to ≤ 1:

$$\tau = \frac{1}{|\min(\Re(\{s_{p1}, s_{p2}\}))|} = \frac{1}{\zeta\sqrt{K}} \tag{98}$$

Thus settling time is:

$$t_s = \frac{-\ln(\delta)}{\zeta\sqrt{K}} = \frac{-\ln\left(\frac{f_{tol}}{|f_i - N f_{ref}|}\right)}{\zeta\sqrt{K}} \tag{99}$$

3.3.4 Filter Design for Synchronous counter

WIP Use fixed damping=1, maximize loop bandwidth, use Kpd of synchronous counter. Estimate settling time.

3.3.5 PI-controller phase margin

The PI-PLL architecture of this work has a phase margin determined by the damping ratio ζ, given by equation 100. Figure 27 shows phase margin versus $0 \geq \zeta \geq 1$ of the PI-controller PLL. It is recommended to use at least 30-60 degrees in phase margin to achieve stability [27]. In this work, ζ = 1 has been used, so a phase margin of 76 degrees is expected, and accordingly stability should be expected.

$$\angle \mathrm{L}(\omega_{ug}) = \frac{180}{2\pi} \arctan\left(2\zeta\sqrt{2\zeta^2 + \sqrt{4\zeta^4 + 1}}\right) \quad \text{[degrees]} \tag{100}$$

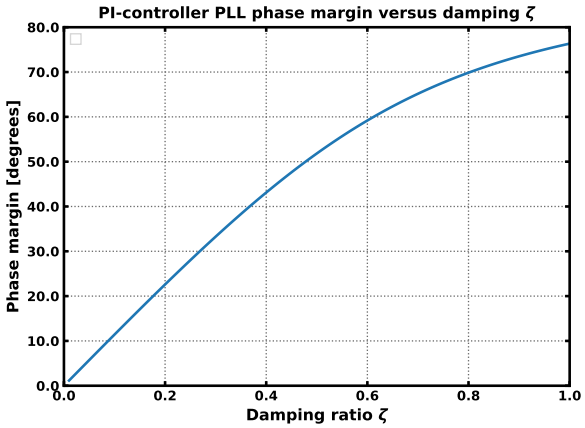


Figure 27: PI-controller PLL phase margin versus damping ratio.

3.3.6 Discretization of Loop Filter

Using the continuous filter discretization approach described in section 2.4.6 on the loop filter of equation 69 results in equation 101.

$$\mathrm{H}_{LF}(z) = \frac{K_i}{s}\left(\frac{s}{\omega_z}+1\right)\Bigg|_{s=\frac{1}{\Delta T_s}(1-z^{-1})} = K_p\frac{(1+\omega_z\Delta T_s)-z^{-1}}{1-z^{-2}} \tag{101}$$

The transformation of equation 101 into a digitally implementable design as a direct form 1 IIR filter shown in figure 28. Its filter coefficients given by equations 102 and 103.

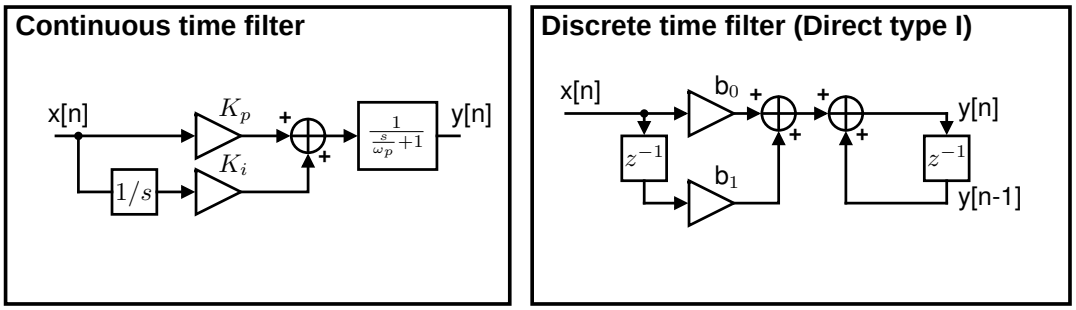


Figure 28: Implementation of filter.

$$b_0 = K_p(1+\omega_z\Delta T_s) = \frac{\sqrt{K}\sqrt{\sigma_{\phi_j}^2+\sigma_{\phi_n}^2}}{\sqrt{2\pi}K_{DCO}}\left(1+\frac{\sqrt{K}}{2f_{ref}}\right) \tag{102}$$

$$b_1 = -K_p = -\frac{\sqrt{K}\sqrt{\sigma_{\phi_j}^2+\sigma_{\phi_n}^2}}{\sqrt{2\pi}K_{DCO}} \tag{103}$$

If design of the PLL is with fixed target for $\sigma_{\phi_n}^2$ (CNR), has a known $\sigma_{\phi_j}^2$ for the BBPD, and α is selected to be constant (i.e. 0.1), the filter coefficients may be calculated as in equations 104 and 105.

$$b_0 = \frac{\alpha f_{ref}\sqrt{2\pi}\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{\sqrt{3+\sqrt{10}}K_{DCO}}\left(1 + \frac{\pi\alpha}{\sqrt{3+\sqrt{10}}}\right) \tag{104}$$

$$b_1 = -\frac{\alpha f_{ref}\sqrt{2\pi}\sqrt{\sigma_{\phi_j}^2 + \sigma_{\phi_n}^2}}{\sqrt{3+\sqrt{10}}K_{DCO}} \tag{105}$$

3.3.7 Implementation

The filter has been chosen to be implemented with separate parts to implement the feedforward parts for each phase detector of the PI-controller, but with a common integrator at the output, as shown in figure 29. This approach to reduce power in steady state operation (using the BBPD). The rationale is that the synchronous counter is a linear detector, thus requires multipliers in the datapath to implement the filter, whereas the BBPD only outputs two values, so the multipliers can be replaces with multiplexers that select between two products ($\pm b_0$ and $\pm b_1$) depending on the input. It is lower energy to operate a multiplexer than an array multiplier due to substantially lower complexity of logic, so the usage of two multiplexers in steady to implement the multipliers will result in substantial power savings. The usage of a common integrator used in both detector modes allows for continuity of output stage during transition between detector modes.

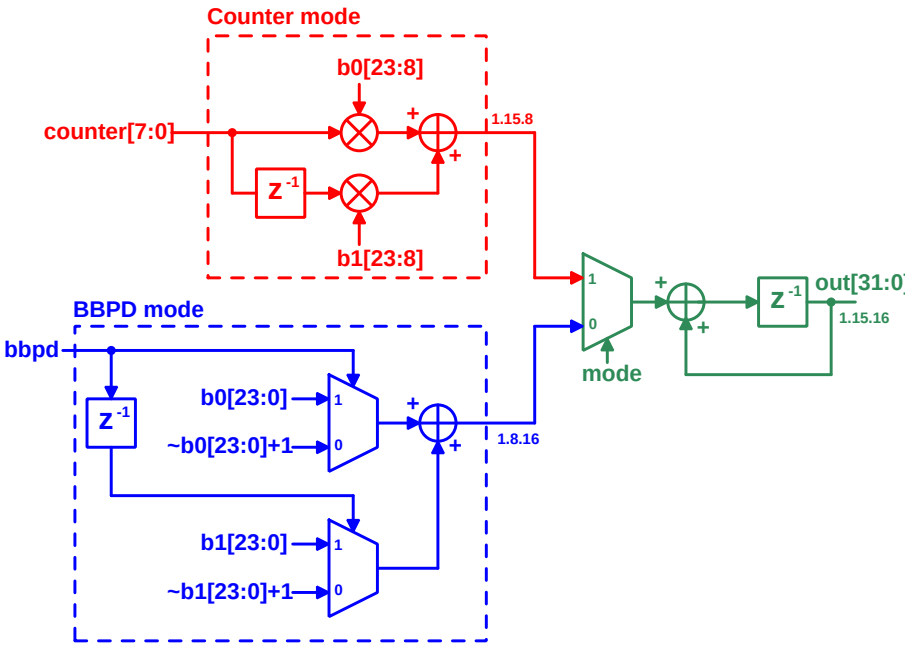


Figure 29: PI-controller implementation for combination of BBPD and synchronous counter usage.

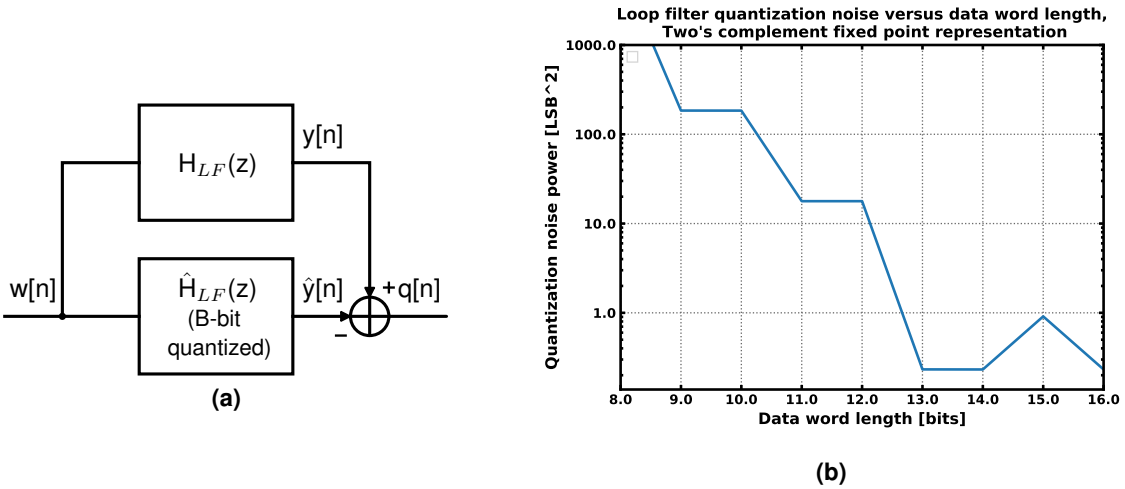


Figure 30: **(a)** Model for determining quantization noise of loop filter, **(b)** Quantization noise power power out of an example loop filter versus data word resolution.

3.3.8 Loop Filter Quantization Noise Optimization

3.3.9 Loop Filter Transfer Function Error Optimization

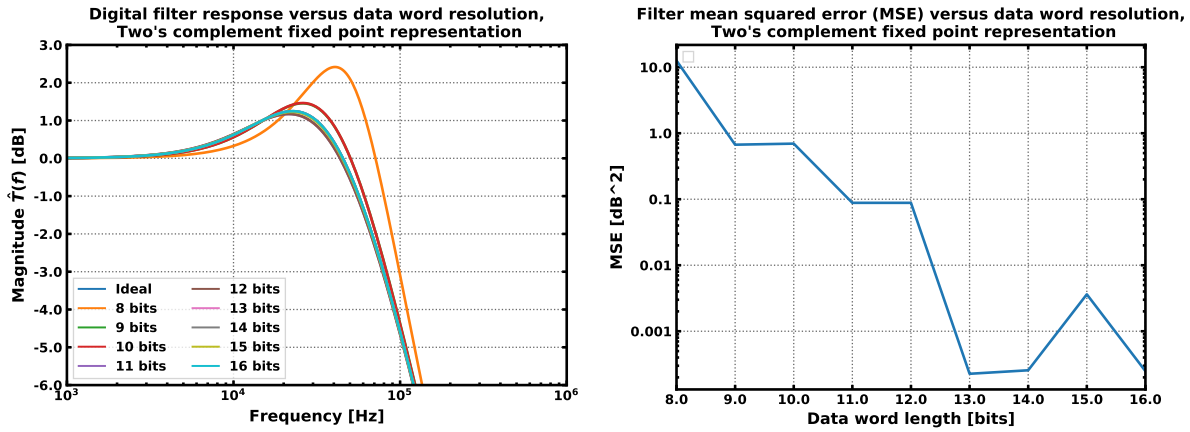


Figure 31: **(a)** Example filter error due to coefficient quantization, **(b)** Example MSE error of filter design due to coefficient quantization.

3.3.10 Approach 2: Results of Transient and Phase Noise Simulation

It is observed that the fast lock gear converges the PLL to steady state in approximately 6 μs as seen in the transient step simulation in figures 32a and 32b, where an initial frequency error of 0.5% 12 MHz is used. Figure 33a shows the output of the TDC and BBPD, it is seen that BBPD feedback has a high density at approximately 11 μs, implicating steady state conditions. Finally, the computed phase noise spectrum of figure 33b demonstrates that there is some discrepancy between the ideal designed response and that simulated, albeit the bandwidth appears correct.

The phase noise spectrum discrepancy is likely due to the model used in the optimization for the BBPD, which uses a linearized model of the BBPD with only idealized DCO and detector noise considered. This does not accurately account for all quantization and discretization emergent behaviors in the discrete time behavioral simulation possibly being manifested here.

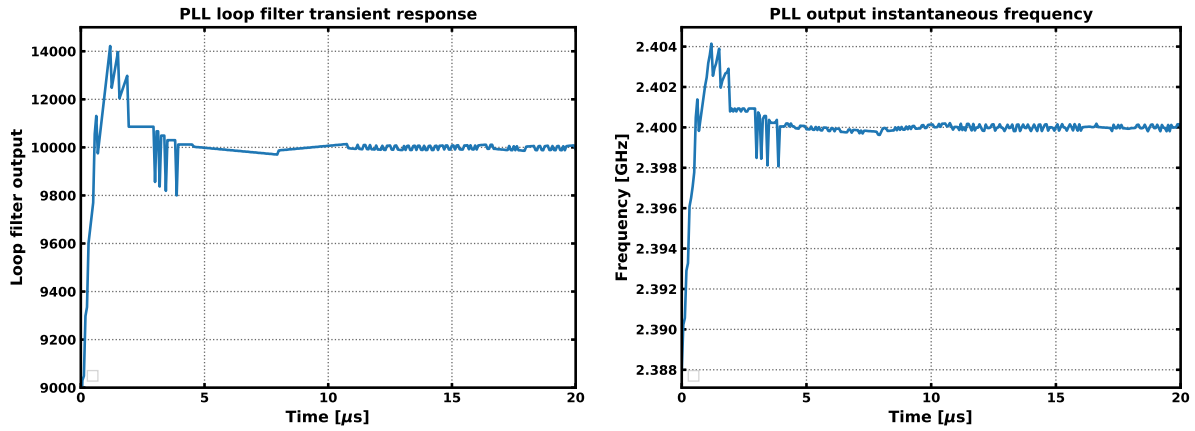


Figure 32: Simulation with 0.5% initial frequency error: **(a)** Loop filter transient response, **(b)** PLL output instantaneous frequency.

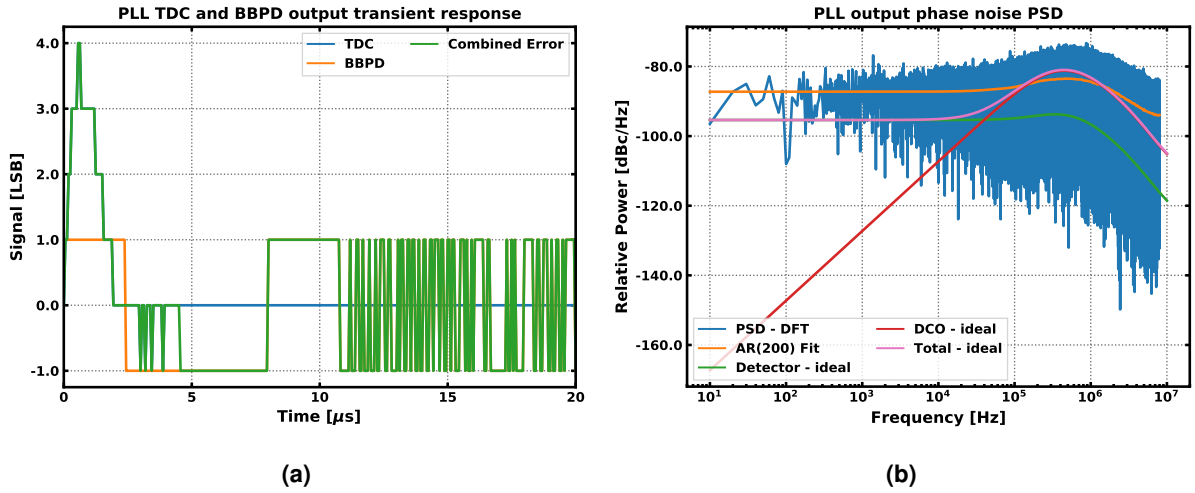
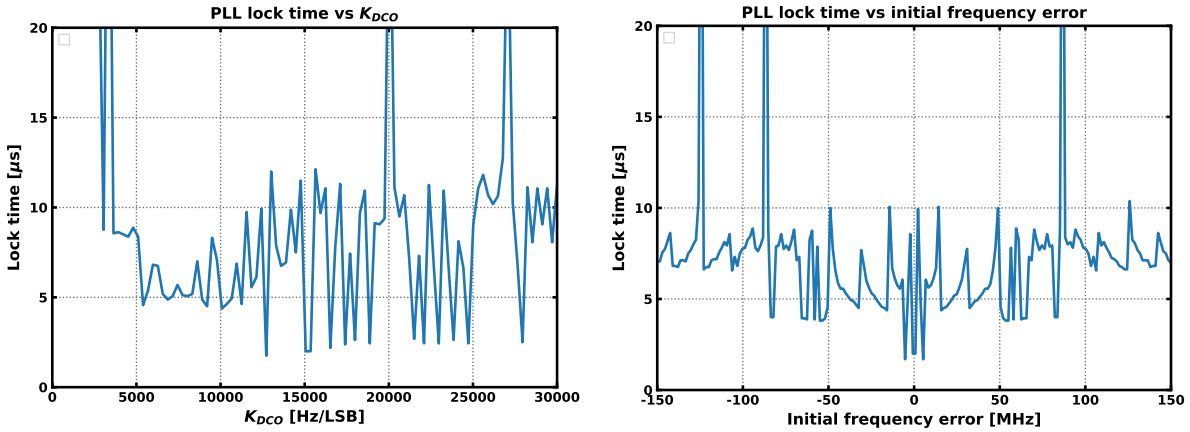


Figure 33: Simulation with 12 MHz (0.5%) initial frequency error: **(a)** BBPD/TDC detector responses, **(b)** PLL output phase noise power spectrum.

3.3.11 Approach 2: Results of Parameter Sweep and Variational Analysis

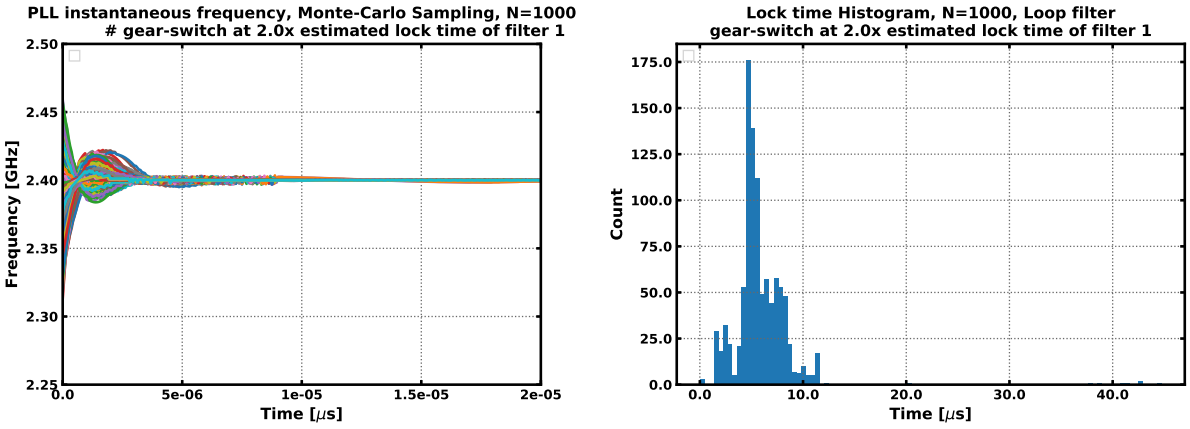
The same parameter sweeps for K_{DCO} and initial frequency error of approach 1 were applied here. In figures 34a and 34b, the results of these sweeps are shown. The loop filter gear switching mechanism as modeled in the simulation waits a fixed time interval before switching gears, in this case chosen to be 2.0 times the estimated lock time given in table 9. This interval has provided sufficient settling within the simulated parameter range of K_{DCO} and initial frequency error that lock time stability is observed under most conditions, except under high offset for

K_{DCO} and initial frequency error. It was established for this simulation results that tolerance range for K_{DCO} is -6950/+9750 Hz/LSB from the nominal 10000 Hz/LSB value, and the capture range is 168 MHz. Figures 35a and 35b demonstrate a variational simulation of the PLL using Monte-Carlo sampling, with 1000 samples. The simulation was configured to vary K_{DCO} with a standard deviation of 20 % of the nominal value, and to vary the initial starting frequency with a standard deviation of 60 MHz (2.5 % of the final frequency). It was observed that the PLL stably locked for all simulation instances, a mean lock time of 5.96 μs was achieved. This value correlates well with the estimate of 5.52 μs from the filter design process. The upper bound for a 99% confidence interval of lock time is 11.625 μs, thus meeting the 25μs lock time specification with considerable margin. The extracted PLL performance parameters from these simulations of this gear-switching PLL is in table 3.



(a) **(b)**

Figure 34: (a) PLL lock time simulation with KDCO swept, 12 MHz (0.5%) initial frequency error, **(b)** PLL lock time simulation with initial frequency error swept.

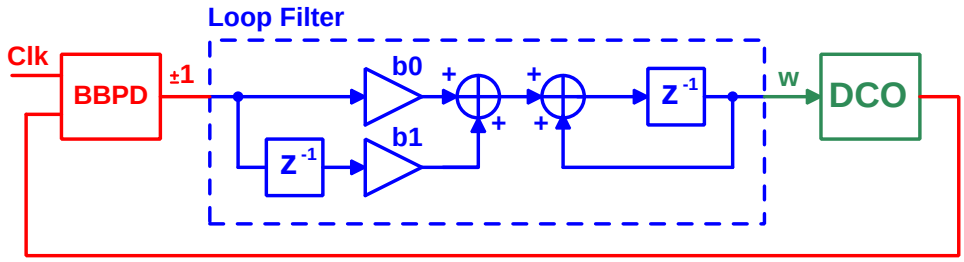


(a) **(b)**

Figure 35: Monte-Carlo simulation with 1000 samples, 20% RMS deviation in KDCO, and 60 MHz (2.5%) RMS deviation in initial frequency error **(a)** Frequency transient responses, **(b)** Lock time histogram.

Parameter	Value	Unit
K_{DCO} **Tolerance**	-6950/+9750	Hz/LSB
Capture range	168 ($\pm$84)	MHz
Mean lock time	5.961688	μs
Lock time σ	3.611130	μs
Lock time 99 % CI upper bound	11.625	μs
Residual phase modulation	4.367535×10^{-2}	rad^2

Table 3: PLL parameters extracted from variance and parameter sweep simulations.

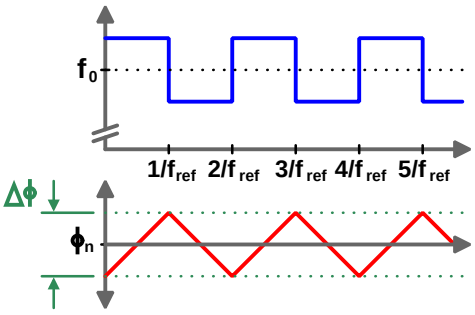


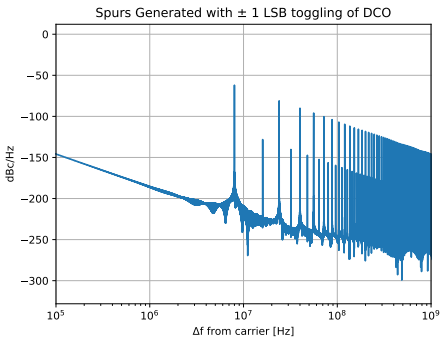
3.3.12 Cyclostationary nonsense

— Output of BBPD is quantized $\pm$ 1. With PI loop filter architecture, there are only 4 possible values that the output **w** can increment by: $\lfloor b_0 + b_1 \rfloor$, $\lfloor b_0 - b_1 \rfloor$, $\lfloor -b_0 + b_1 \rfloor$, $\lfloor -b_0 - b_1 \rfloor$.

— In steady state, with the BBPD outputting a worst case sequence of +1/-1/+1/-1... , the output will toggle betwwen $\lfloor b_0 - b_1 \rfloor$ and $\lfloor -b_0 + b_1 \rfloor$.

- Current optimization yields b_0 = 8.899856, b_1 = -8.301153
- Thus output **w** will increment by +17, -18, +17, -18 ...
- Essentially output will make large-ish jumps in frequency every reference cycle





— Worst case input sequence results in square wave frequency modulation, which in the phase domain creates a cyclostationary triangle wave with period f_{ref}/2. This creates

SPURS at $f_{ref}/2$.

— In general, $f_{ref} >> K_{DCO}|b_0 - b_1|$ (frequency deviation), so spurs are not generated at the deviation frequencies.

— With 1 LSB deviation per ref. cycle, a -62 dBc spur (SSB) is expected $f_{ref}/2$.

- Under my current b_0, b_1, this spur will be -37 dBc.

— **Cyclostationary (+1, -1, +1, -1, ...):**

- Under my system parameters, the total phase noise power from resolution effects is -34 dBc, essentially all of which is in the first spur at $f_{ref}/2$.

$$\Delta\Phi = \frac{2\pi|b_0 - b_1|K_{DCO}}{f_{ref}} \tag{106}$$

$$\sigma_{\Phi rj} = \frac{\pi|b_0 - b_1|K_{DCO}}{\sqrt{3}f_{ref}} \tag{107}$$

— **General note:** the phase noise from this source must << than target SNR for PLL application. Can use these relations to find limits for maximum K_{DCO} before resolution jitter is dominant.

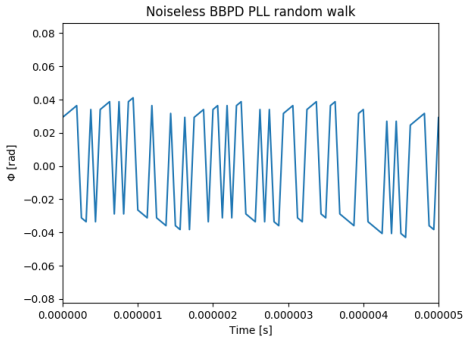
— **Average case:**

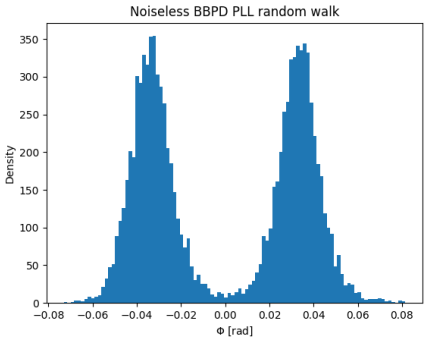
- All transitions equally likely out of BBPD.

- Under my system parameters, the total phase noise power from resolution effects is -29.4 dBc (simulated).

- Phase noise is bimodal. The total RMS phase noise power is approximately equal to the absolute value of the distribution means.

$$\mu = \pm\frac{\pi|b_0 - b_1|K_{DCO}}{f_{ref}}. \qquad \sigma_{\Phi rj} \approx |\mu| \tag{108}$$





— Found an interesting dissertation on BBPD PLLs [3], which shows that the linearized

BBPD gain model I have been using ($K_{BBPD} = 2/\sqrt{2\pi}\sigma_{\Phi_n}$) is not totally correct.

- Due to BBPF-PLL resolution jitter, varies depending if resolution jitter or if random noise is the dominant component.

— Need to account for this in my filter optimization code...

— An approximation, with random/uncorrelated noise with $\sigma_{\Phi uc}$, and resolution jitter $\sigma_{\Phi rj}$ (based on variable substitution of [3]'s theory):

$$K_{BBPD} = \frac{1}{\sqrt{2\pi}\sigma_{\Phi uc}}\left[1 + e^{-\frac{1}{2}\left(\frac{\sigma_{\Phi rj}}{\sigma_{\Phi uc}}\right)^2}\right] \tag{109}$$

$$\sigma_{\Phi rj} \approx \frac{\pi|b_0 - b_1|K_{DCO}}{f_{ref}} \tag{110}$$

— Currently, I should be well into the random noise dominated regime.

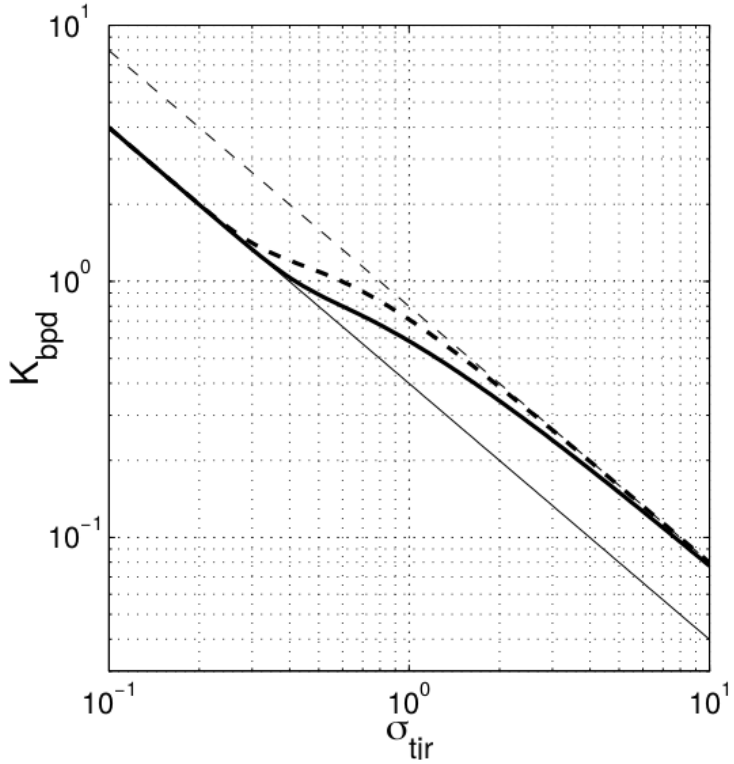


Figure 4.5: Plot of K_{bpd} versus σ_{tjr} (gaussian jitter, $N\beta K_T$ normalized to 1): K_{bpd} computed with a 101 states Markov Chain (thick solid), K_{bpd} approximated with a 3 states Markov Chain (thick dashed), asymptote $K_{bpd} = 1/(\sqrt{2\pi}\sigma_{t_{jr}})$ (thin solid), asymptote $K_{bpd} = 2/(\sqrt{2\pi}\sigma_{t_{jr}})$ (thin dashed).

3.3.13 Filter Design

Parameter	Value	Unit
K	2.982197×10^{12}	
K_i	2.982197×10^{8}	
K_p	2.115052×10^{2}	
f_z	2.244064×10^{5}	Hz
b_0	$2.3014397180 \times 10^{2}$	
b_1	$-2.1150524223 \times 10^{2}$	
a_0	1.0×10^{0}	
a_1	-1.0×10^{0}	
a_2	0.0×10^{0}	
Estimated bandwidth	5.333423×10^{5}	Hz
Estimated lock time	4.527067×10^{-6}	seconds

Table 4: PLL parameters determined from filter design and optimization process for fast lock speed with TDC feedback.

Parameter	Value	Unit
K	5.325862×12^{12}	
K_i	1.271456×10^{10}	
K_p	1.101813×10^{4}	
f_z	1.836596×10^{5}	Hz
b_0	$1.1812790734 \times 10^{4}$	
b_1	$-1.1018130778 \times 10^{4}$	
a_0	1.0×10^{0}	
a_1	-1.0×10^{0}	
a_2	0.0×10^{0}	
K_{bb}	1.0×10^{0}	
Estimated bandwidth	9.117332×10^{5}	Hz
Estimated lock time	9.978130×10^{-7}	seconds

Table 5: PLL parameters determined from filter design and optimization process for minimum phase noise with BBPD.

Parameter	Value	Value (digital)	Value Error
Total dataword bits	20		
Sign bits	1		
Integer bits	8		
Fractional bits	11		
b_0 (gear 1)	2.301440×10^2	0b01110011000100100111	$+7.116930 \times 10^{-5}$
b_1 (gear 1)	-2.115054×10^2	0b11110110001111110101	-1.288619×10^{-4}
a_0 (gear 1)	1.0×10^0	0b00000000100000000000	0.0×10^0
a_1 (gear 1)	-1.0×10^0	0b11111111100000000000	0.0×10^0
a_2 (gear 1)	0.0×10^0	0b00000000000000000000	0.0×10^0
K_{bb} (gear 1)	0.0×10^0	0b00000000000000000000	0.0×10^0
b_0 (gear 2)	8.899902×10^0	0b00000100011100110011	$+4.616306 \times 10^{-5}$
b_1 (gear 2)	-8.301270×10^0	0b11111011110110010111	-1.168639×10^{-4}
a_0 (gear 2)	1.0×10^0	0b00000000100000000000	0.0×10^0
a_1 (gear 2)	-1.0×10^0	0b11111111100000000000	0.0×10^0
a_2 (gear 2)	0.0×10^0	0b00000000000000000000	0.0×10^0
K_{bb} (gear 2)	1.0×10^0	0b00000000100000000000	1×10^0

Table 6: Loop filter parameters after digitization and optimization for data word length, gear 1 and gear 2.

3.4 Ring oscillator

Selected due to instantaneous start up capabilities, and associated ability to therefore reset phase to a known possition instantly.

Tuning of a FDSOI ring oscillator DCO through backgate terminal voltage and supply voltage will be considered. A general analysis of ring oscillator frequency will be made first to begin.

Hajimiri's oscillator impulse sensitivity function (ISF) paper [28] suggests that it is favorable for an oscillator to have as symmetric rise and fall time. Higher symmetry of waveform results in a lower corner frequency for flicker noise, thus low frequency phase noise will be improved.

3.4.1 Channel length consideration

Based on the 22FDX process: Notes, from the derived theory, it is expected that power should be fixed for fixed w/l (true except for small channel length), frequency to decrease. Increased phase noise is seen near 20nm according to the 5nm PLL, explain+cite. Recommened to avoid min. channel length.

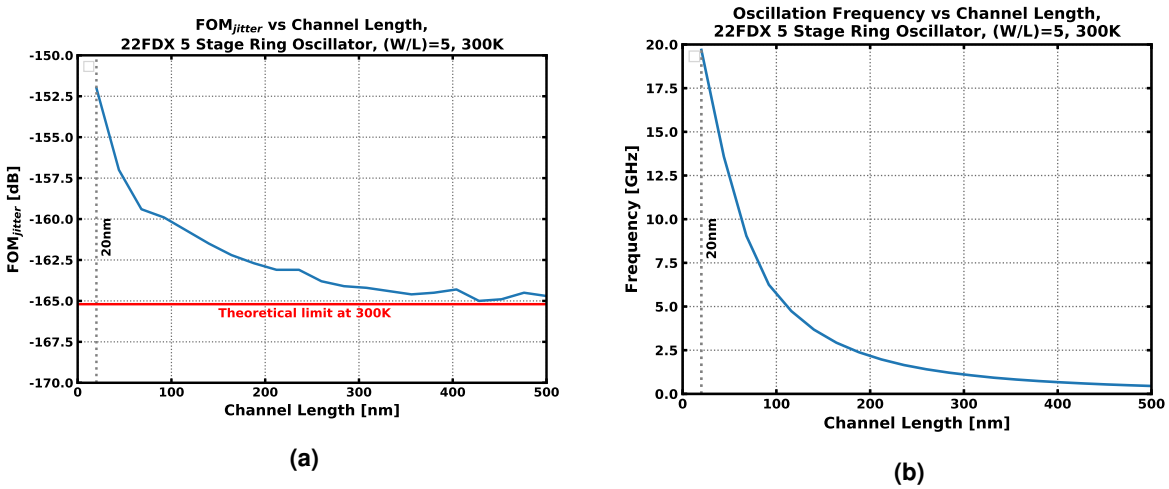


Figure 38: 22FDX ring oscillator channel length sweep versus **(a)** FOM, **(b)** Oscillation frequency.

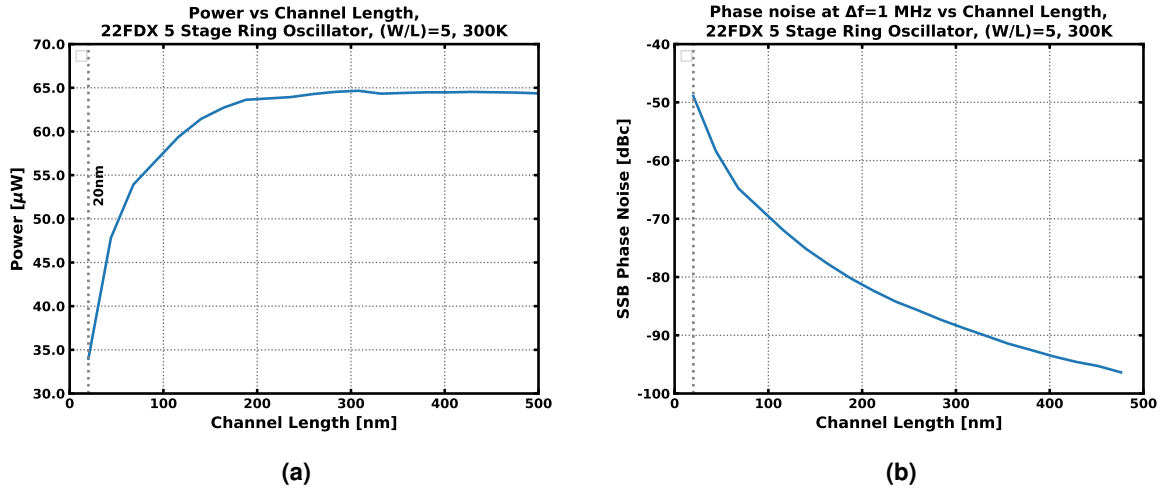


Figure 39: 2FDX ring oscillator channel length sweep versus **(a)** Power, **(b)** Phase noise at 1 MHz carrier offset (SSB).

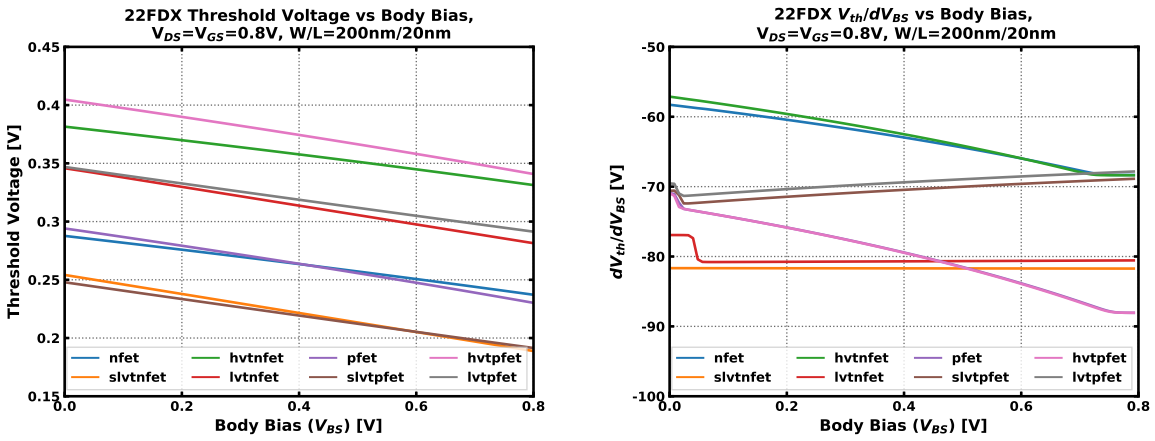
3.4.2 22FDX considerations

Idea: use backgates of FDSOI to tune frequency.. Vth is approximately linear with applied backgate bias, use approximate model $vth = vth0 + \gamma V_{BS}$ Derive that gmbs = γ gm with this assumption. Gmbs and gm are easily found with SPICE simulator, which results in the extracted data below.

Although the BSIM-IMG FD-SOI threshold voltage model is not perfectly linear, it is observed that the body-bias threshold is approximately linear, especially under semi-local conditions. Thus, for simplified analysis, a new model for body-effect coupled threshold voltage is introduced here. Body bias is here defined as the potential V_{BS} applied between the backgate contact and the source contact.

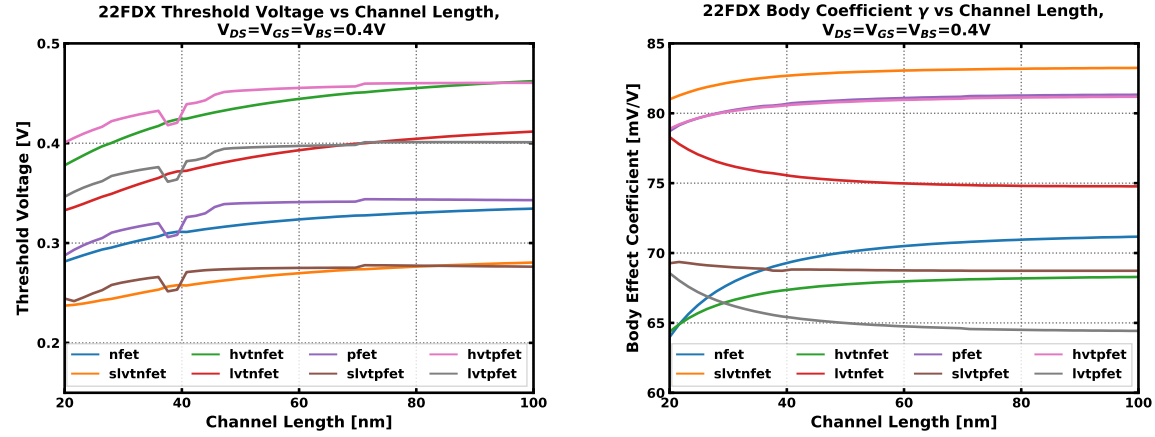
$$V_{th} = V_{th0} - \gamma V_{BS} \tag{111}$$

Might be challenging to achieve proper frequency and sufficient FOM, unfortunately....



(a) (b)

Figure 40: **(a)** 22 FDX threshold voltage versus body bias, **(b)** Rate of change of threshold voltage versus body bias.



(a) (b)

Figure 41: **(a)** 22 FDX Extracted threshold voltage versus channel length, **(b)** Extracted body effect coefficient.

Extracted vth and body effect coefficient (γ). Assuming gmbs = gamma*gm. Extracted for $V_{DD} = V_{GS} = 0.4$.

Device	L [nm]	W [nm]	V_{th} [mV]	γ [mV/V]
nfet	20	100	306.3	59.14
nfet	100	500	376.4	65.4
slvtnfet	20n	100	270.3	81.38
slvtnfet	100	500	326.7	83.23
hvtnfet	20n	100	402.4	58.85
hvtnfet	100	500	513.5	61.96
lvtnfet	20	100	364.9	77.72
lvtnfet	100	500	466.3	74.85

Table 7: 22FDX core NFET threshold voltage and body effect coefficient extraction.

Device	L [nm]	W [nm]	V_{th} [mV]	γ [mV/V]
pfet	20	100	317.7	71.51
pfet	100	500	366.8	74.32
slvtpfet	20n	100	272.6	71.09
slvtpfet	100	500	294.4	70.79
hvtpfet	20n	100	430.7	71.28
hvtpfet	100	500	488.4	74.23
lvtpfet	20	100	374.2	69.93
lvtpfet	100	500	422.8	66.43

Table 8: 22FDX core PFET threshold voltage and body effect coefficient extraction.

3.4.3 Ring oscillator frequency derivation

To analyze the oscillation frequency of a CMOS ring oscillator, an approximate model for a CMOS inverter will first be considered. A common model for delay in digital circuits [elmore delay model] is an RC circuit, where the MOSFET channels are approximated with an average conductance value $\langle g_{ch} \rangle$, and the output node is approximated to have a capacitance of C. With such a model, a ring oscillator would be assumed to have waveforms as decaying exponential, with time constant $\tau = \langle g_{ch} \rangle^{-1} C$, such as in Figure 42.

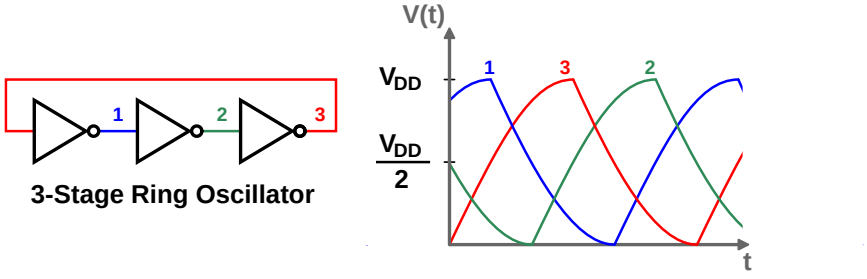
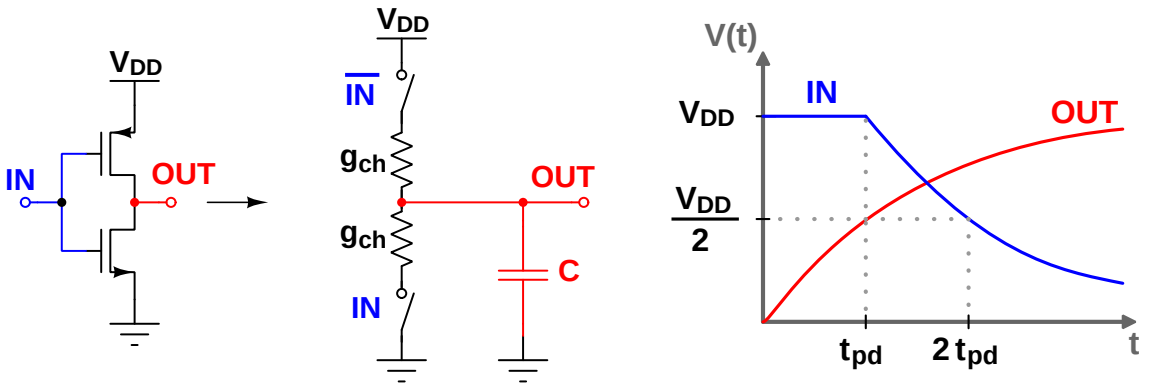


Figure 42: Model for ring oscillator.



(a) Inverter approximate model.

(b) Inverter waveforms in ring oscillator.

Figure 43: Approximate model for ring oscillator inverter delay cell.

To calculate oscillation frequency ring oscillator from the RC model, several inferences are made:

- The switching point V_M of the inverters is $V_{DD}/2$, based on the assumption that the NMOS and PMOS are of equal strength.
- The output of an inverter will have a decaying exponential which starts coincident with the passing of V_M at the input.
- The propagation delay t_{pd} for an inverter will be the time differential between the V_M crossing points on the input and output.
- The oscillator frequency will be $f_{osc} = 1/2Nt_{pd}$, where N is the number of stages (i.e. defined by 2N propagation delays).

Following the definition of V_M, it is trivial to find that $t_{pd} = \tau \ln 2$. It is therefore known that:

$$f_{osc}^{-1} = 2Nt_{pd} = \frac{2\ln(2)NC}{\langle g_{ch} \rangle} \tag{112}$$

3.4.4 Finding $\langle g_{ch} \rangle$ and C

The node capacitance C is trivial to find based on the inverter gate capacitance and a lumped load capacitance term C_L:

$$C = C_{ox}\left(W_N L_N + W_P L_N\right) + C_L \tag{113}$$

The average channel conductance $\langle g_{ch} \rangle$ is more involved to find. To do so, several assumptions are made:

- L >> L_{min}, so no velocity saturation, and therefore square law is applicable.

- NMOS and PMOS have equal V_t and transconducance.
- Output transition occur with the active FET in saturation during t_{pd}. This requires:
  - $V_{DD}/4 < V_t < V_{DD}/2$

Following those assumptions, $\langle g_{ch} \rangle$ can be computed via integral within the period t_{pd}:

$$\langle g_{ch} \rangle = \frac{1}{t_{pd}} \int_0^{t_{pd}} \frac{I_{out}(t)}{V_{out}(t)} dt \tag{114}$$

I_{out} is computed using the saturated MOSFET square law model an exponential waveforms assumptions. An I_{short} term is included to account for output current reduction from short-circuit conduction.

$$I_{out}(t) = \frac{k_n}{2} \left(\frac{W}{L}\right)_n \left[(V_{in}(t) - V_t)^2\right] - I_{short} = \frac{k_n}{2} \left(\frac{W}{L}\right)_n \left[\left(V_{DD}\left(1 - e^{-t/\tau}\right) - V_t\right)^2 - \left(\frac{V_{DD}}{2} - V_t\right)^2\right] \tag{115}$$

$k_n = \mu_n C_{ox}$, with the equal PMOS/NMOS assumption, $k_n \left(\frac{W}{L}\right)_n = k_p \left(\frac{W}{L}\right)_p$. V_{out} is simply a decaying exponential with a delay t_pd versus the input:

$$V_{out} = V_{DD} e^{-(t - t_{pd})/\tau} \tag{116}$$

Now, computing the integral for $\langle g_{ch} \rangle$ yields:

$$\langle g_{ch} \rangle = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_t\left(\frac{1}{\ln 2} - 1\right)\right] \tag{117}$$

As a simplification, α is defined as:

$$\alpha = \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_t\left(\frac{1}{\ln 2} - 1\right)\right] \tag{118}$$

3.4.5 Handling unequal NMOS/PMOS

In the case of different threshold voltages for NMOS and PMOS:

$$f_{osc}^{-1} = N(t_{pdn} + t_{pdp}) = \ln(2) NC \left(\frac{1}{\langle g_{ch} \rangle_n} + \frac{1}{\langle g_{ch} \rangle_p}\right) = \frac{2\ln(2) NC}{\langle g_{ch} \rangle'} \tag{119}$$

A modified $\langle g_{ch} \rangle'$ is defined:

$$\langle g_{ch} \rangle' = 2\left(\frac{1}{\langle g_{ch} \rangle_n} + \frac{1}{\langle g_{ch} \rangle_p}\right)^{-1} = 2\frac{\langle g_{ch} \rangle_n \langle g_{ch} \rangle_p}{\langle g_{ch} \rangle_n + \langle g_{ch} \rangle_p} = 2\frac{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \alpha_n \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \alpha_p}{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n \alpha_n + \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_p \alpha_p} \tag{120}$$

This is somewhat unmanagable, however enforcing $\mu_n C_{ox} \left(\frac{W}{L}\right)_n = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$ for V_M to equal $V_{DD}/2$ gives:

$$\langle g_{ch} \rangle' = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_n \frac{2\alpha_n \alpha_p}{\alpha_n + \alpha_p} = \frac{1}{2}\mu_n C_{ox} \left(\frac{W}{L}\right)_n \alpha' \tag{121}$$

Thus α_n and α_p are found for the according threshold voltages and then $\langle g_{ch} \rangle$ can be found.

$$\alpha' = \frac{2\alpha_n \alpha_p}{\alpha_n + \alpha_p} \tag{122}$$

3.4.6 Solving for oscillator frequency and power

Solving for oscillator frequency:

$$f_{osc} = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_t \left(\frac{1}{\ln 2} - 1\right)\right] \tag{123}$$

If gate capacitance is the dominant load component, and PMOS/NMOS are equal sized such that $C = 2WLC_{ox}$:

$$f_{osc} = \frac{\mu_n}{8 \ln 2 N} \cdot \frac{1}{L^2} \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_t \left(\frac{1}{\ln 2} - 1\right)\right] \tag{124}$$

Power can also be calculated, knowing in digital circuits $P = f C_\Sigma V_{DD}^2$, where C_Σ is the total active capacitance. Thus:

$$P_{osc} = N f_{osc} C V_{DD}^2 = \frac{\mu_n C_{ox}}{4 \ln 2} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_t \left(\frac{1}{\ln 2} - 1\right)\right] \tag{125}$$

It should be noted that the power consumption is proportional to FET aspect ratio (W/L).

3.4.7 Ring oscillator backgate tuning derivation

Using the basic expressions for ring oscillator frequency, the operature under backgate biasing can be found. In UTBB-FDSOI processes, the threshold voltage of a FET varies with linear dependence on the applied back gate bias V_{BG} (relative to source). Given the body effect coefficient of a process, γ, V_t is:

$$V_t = V_{t0} - \gamma V_{BG} \tag{126}$$

Using this in the ring oscillator frequency equation:

$$f_{osc} = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0} \left(\frac{1}{\ln 2} - 1\right) + \gamma V_{BG} \left(\frac{1}{\ln 2} - 1\right)\right] \tag{127}$$

Equivalently, $f_{osc} = f_{0,osc} + \Delta f_{osc}(V_{BG})$, where:

$$\Delta f_{osc}(V_{BG}) = \gamma V_{BG} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{128}$$

And $f_{0,osc}$ is the frequency with no backgate bias. If the backgate is swept from 0 to V_{DD}, and the node capacitance is increasingly varied (C0 to C3), Figure 44 is observed. Note that the change in frequency is linear with to backgate bias.

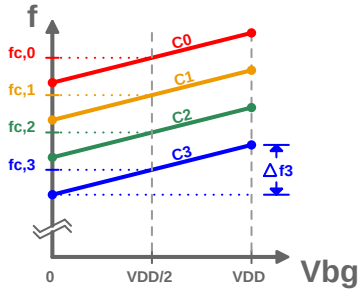


Figure 44: Backgate-tuned ring oscillator with coarse tuning capacitor bank.

If the backgate voltage is constrained in the range $[0, V_{DD}]$, the center frequency f_c in the tuning range of the oscillator is then:

$$f_c = \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[V_{DD}\left(\frac{7}{8 \ln 2} - 1 + \frac{\gamma}{2 \ln 2} - \frac{\gamma}{2}\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)\right] \tag{129}$$

The tuning range is also therefore:

$$\Delta f = \gamma V_{DD} \frac{\mu_n C_{ox}}{4 \ln 2 NC} \left(\frac{W}{L}\right)_n \left[\frac{1}{\ln 2} - 1\right] \tag{130}$$

The fractional tuning range of the oscillator is:

$$\frac{\Delta f}{f_c} = \frac{\gamma V_{DD}\,(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}\,(1 - \ln 2)} \tag{131}$$

If a N-bit DAC is used to control the oscillator, the resulting DCO gain is therefore:

$$K_{DCO} = \frac{\Delta f}{2^{N_{DAC}}} = \frac{f_c}{2^{N_{DAC}}} \cdot \frac{\gamma V_{DD}\,(1 - \ln 2)}{V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}\,(1 - \ln 2)} \tag{132}$$

3.4.8 DCO Gain Uncertainty

The DCO gain K_{DCO} is used in setting the loop filter coefficients, so the uncertainty of the DCO gain is of interest to allow for statistical analysis of the PLL across process variation. The uncertainty of K_{DCO} (normalized with nominal K_{DCO} value) as a function of V_{DD}, V_{t0} and γ

is:

$$\sigma_{KDCO} = \sqrt{\left(\frac{\partial K_{DCO}}{\partial V_{DD}} \cdot \frac{\sigma_{VDD}}{K_{DCO}}\right)^2 + \left(\frac{\partial K_{DCO}}{\partial V_{t0}} \cdot \frac{\sigma_{Vt0}}{K_{DCO}}\right)^2 + \left(\frac{\partial K_{DCO}}{\partial \gamma} \cdot \frac{\sigma_{\gamma}}{K_{DCO}}\right)^2} \tag{133}$$

$$\frac{\partial K_{DCO}}{\partial V_{DD}} = \frac{f_c}{2^{N_{DAC}+1}} \cdot \frac{-\gamma V_{t0}(1-\ln 2)^2}{\left[V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}\left(1-\ln 2\right)\right]^2} \tag{134}$$

$$\frac{\partial K_{DCO}}{\partial V_{t0}} = \frac{f_c}{2^{N_{DAC}+1}} \cdot \frac{\gamma V_{DD}(1-\ln 2)^2}{\left[V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}\left(1-\ln 2\right)\right]^2} \tag{135}$$

$$\frac{\partial K_{DCO}}{\partial \gamma} = \frac{f_c}{2^{N_{DAC}+1}} \cdot \frac{V_{DD}\cdot(1-\ln 2)\left[V_{DD}\left(\frac{7}{8} - \ln 2\right) - V_{t0}\left(1-\ln 2\right)\right]}{\left[V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}\left(1-\ln 2\right)\right]^2} \tag{136}$$

Simplified:

$$\sigma_{KDCO} = \frac{1}{\gamma V_{DD}\left[V_{DD}\left(\frac{7}{8} - \ln 2 + \frac{\gamma}{2} - \frac{\gamma}{2}\ln 2\right) - V_{t0}\left(1-\ln 2\right)\right]} \cdot \sqrt{\left(\gamma V_{t0}(1-\ln 2)\sigma_{VDD}\right)^2 + \left(\gamma V_{DD}(1-\ln 2)\sigma_{Vt0}\right)^2 + \left(V_{DD}\left[V_{DD}\left(\frac{7}{8} - \ln 2\right) - V_{t0}\left(1-\ln 2\right)\right]\sigma_{\gamma}\right)^2} \tag{137}$$

Motivate selection of fine backgate tuning and supply coarse tuning (as future extension?). I.e. what is df/dVdd vs df/dVbg? **TODO** - extract γ, V_{t0} variance for FETs in process kit, place in results?

3.4.9 DCO Sensitivity

The frequency tuning sensitivity of the ring oscillator for supply and backgate voltages will be compared. First the following is defined, following that the derived equations for oscillator frequency are linear.

$$f_{osc}(V_{DD} + \Delta V_{DD}) = f_{osc}(V_{DD}) + f_{osc}(\Delta V_{DD}) \tag{138}$$

$$f_{osc}(V_{DD}) = f_0 \tag{139}$$

$$f_{osc}(\Delta V_{DD}) = \Delta f \tag{140}$$

In the case of supply voltage tuning, the change (proportion) of frequency per voltage of applied extra bias is (evaluated at zero back-gate bias):

$$S_{V_{DD}}^{f_{osc}} = \frac{\Delta f}{f_0} \cdot \frac{1}{\Delta V_{DD}} = \frac{\left(\frac{7}{8\ln 2} - 1\right)}{V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)} \tag{141}$$

With V_{DD}=0.8, V_{t0}=0.3, it is expected 340% change in frequency will result per extra volt of applied bias (of course, this is linearized, one does not expect to apply an extra 1V). Realistically, the supply can be tuned $\pm$ 10%, which corresponds to a $\pm$27.2% tuning range of the oscillator. This is perhaps a good coarse tuning mechanism, but does not provide much for fine tuning. make note of supply noise sensitivity!

In the case of backgate tuning, the change (proportion) of frequency per volt of applied backgate bias is:

$$S_{V_{BG}}^{f_{osc}} = \frac{\Delta f}{f_0} \cdot \frac{1}{\Delta V_{BG}} = \frac{\gamma\left(\frac{1}{\ln 2} - 1\right)}{V_{DD}\left(\frac{7}{8\ln 2} - 1\right) - V_{t0}\left(\frac{1}{\ln 2} - 1\right)} \tag{142}$$

With γ=0.07, V_{DD}=0.8, V_{t0}=0.3, it is expected a 40% change in frequency will result per volt applied of backgate bias. This is much finer than achieved with supply voltage tuning. The ratio of frequency sensitivity to supply and backgate voltage tuning is:

$$\frac{S_{V_{DD}}^{f_{osc}}}{S_{V_{BG}}^{f_{osc}}} = \frac{\frac{7}{8\ln 2} - 1}{\gamma\left(\frac{1}{\ln 2} - 1\right)} \tag{143}$$

Under the aforementioned biasing conditions, it is expected that 8.4x finer control can be achieved with backgate tuning. The wide backgate voltage ranges allowed for with FDSOI technology permit for design of a voltage-DAC based controll scheme which will achieve far smaller frequency resolution than with supply voltage tuning.

3.4.10 temp

— Simulated 5 stage ring oscillator.

— RVT devices, W/L = 5.

— Ran pss/pnoise.

— Computed FOM vs channel length (lower is better):

$$\text{FOM} = 10\log_{10}\left(\left(\frac{\Delta f}{f_0}\right)^2 \cdot \frac{\text{P}_{total}}{1\text{ mW}}\right) \quad \text{[dB]} \tag{144}$$

— It is seen that FOM improves asymptotically to $\sim$ -165 with longer L.

— FOM ¡ -160 dB $\rightarrow$ L $\geq$ 100 nm.

— L should be set as long as possible, while mantaining appropriate speed.

- This is actually recommended in Razavi's new book [23].

3.4.11 Delay cell

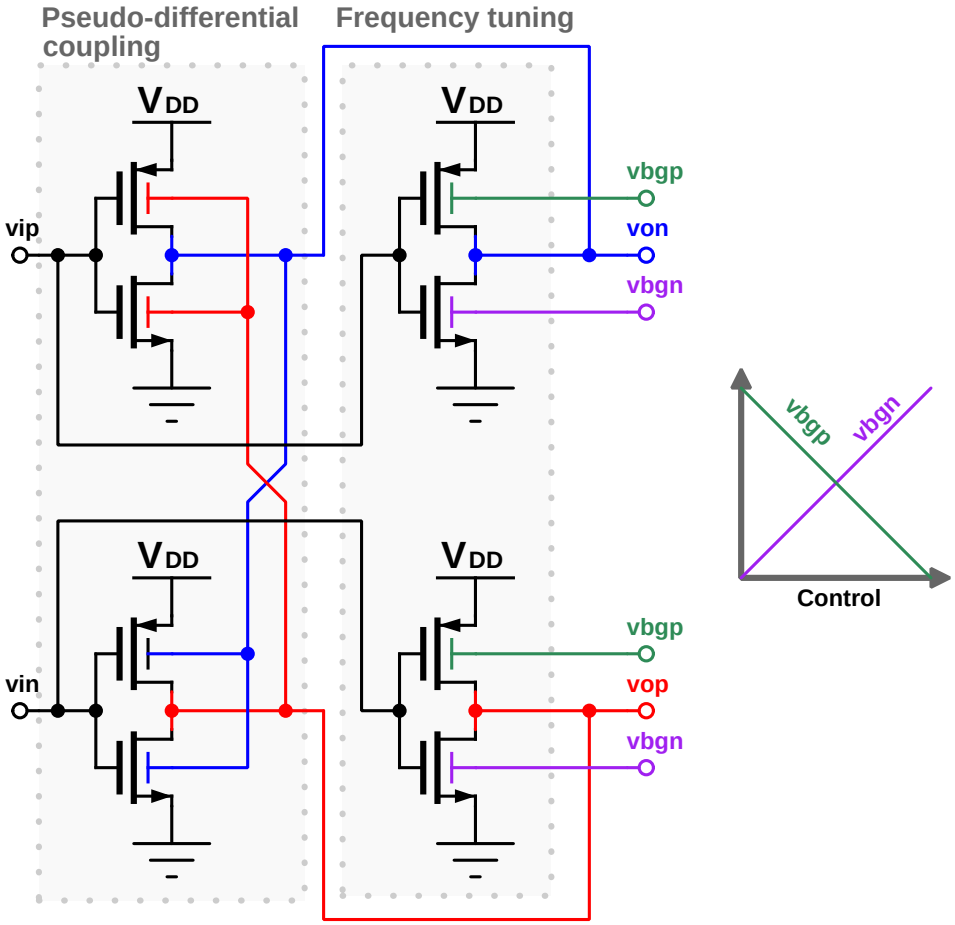
— Utilize pseudo-differential inverter stage [3], in parallel with back gate tuned inverter.

- Pseudo-differential stage couples oscillators, forcing crossing voltage $V_{DD}/2$.
- Back gate tuned oscillator used to adjust frequency.

— Ratioing the sizes two types of inverters can be used to adjust the VCO gain. A ratio of 1:1 should reduce the K_{VCO} in half from what is expected from theory, a ratio of 3:1 (with pseudo-diff inverters being larger) will reduce K_{VCO} by 4.

— **Requires complementary control of backgate voltage for tuning.**

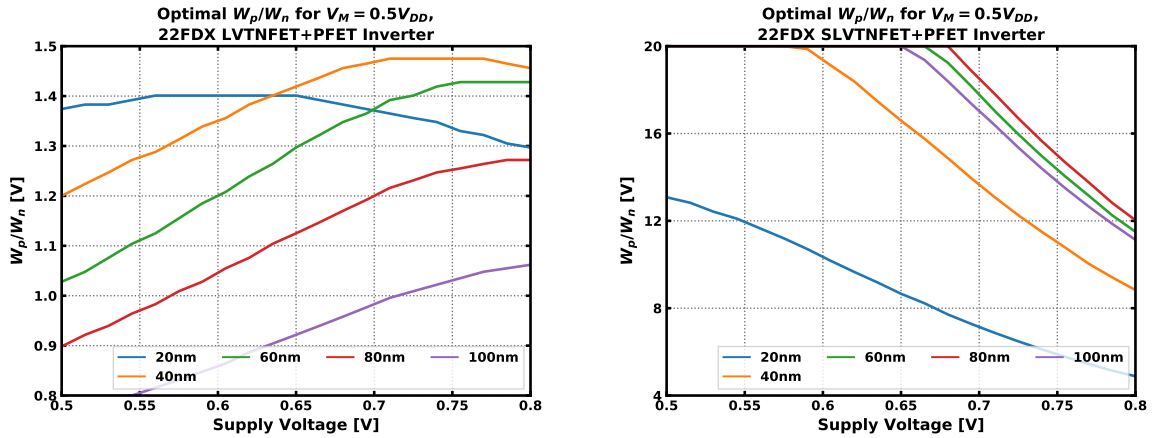
— **Allows for 0-V_{DD} control range.**



— Must use devices in N well (PFET, HVTPFET, SLVTNFET, LVTNFET) to not forward bias substrate diode.

— To achieve $V_m = V_{DD}/2$, PFET + LVTNFET give most reasonable W_P/W_N, ca 1.2-1.4.

- SLVTNFET + PFET needs $W_P/W_N \approx 8$.



(a) (b)

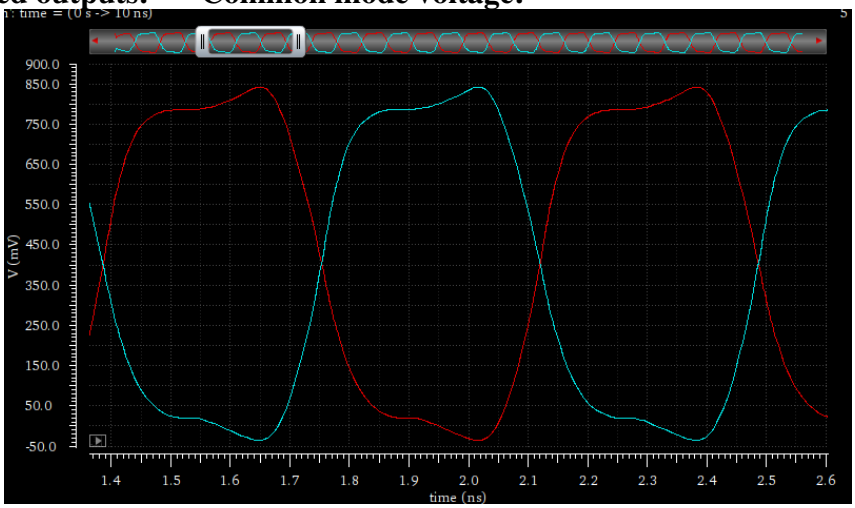
Figure 45: (a) Optimal width PFET/LVTNFET, **(b)** Optimal width PFET/SLVTNFET.

— Good symmetry of rise time observed, with V_{cm} close to $V_{DD}/2$ over the full oscillation cycle.

— **Observed 10.3% fractional frequency tuning with L=150nm, FOM=-161 dB, 1:1 ratio of inverters.**

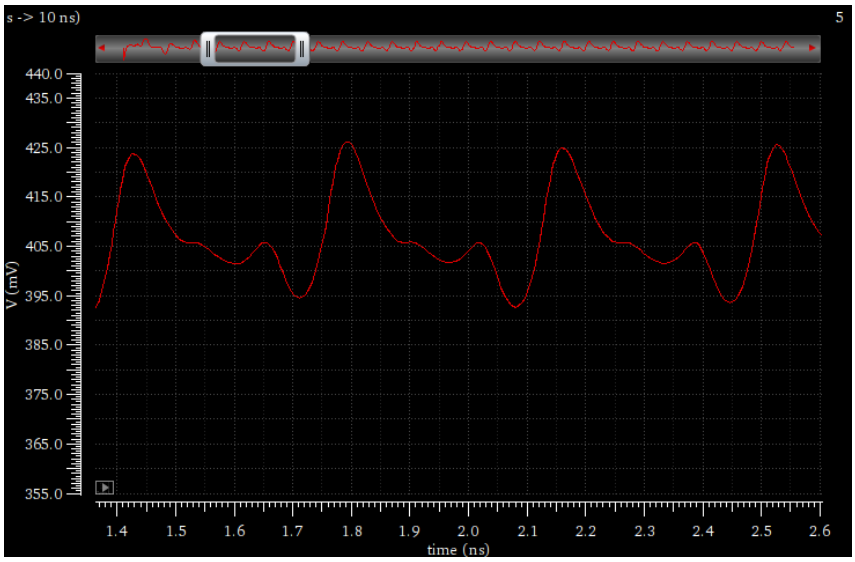
— I require $< 1\%$ fractional tuning range to achieve my K_{DCO} with a 10b DAC, this will not work. The (W/L) becomes large to achieve a high inverter ratio, thus increases power too much.

Single ended outputs: **Common mode voltage:**



— Modify the pseudo-differential cell to have header/footer transistors with back gate control.

- Cross-coupled devices force differential operation



- Header/footer devices used to adjust frequency.

— Ratioing the size of the header/footer devices to the size of the cross-coupling devices tunes K_{VCO}

— **Requires complementary control of backgate voltage for tuning.**

— Good symmetry of rise time observed, with V_{cm} close to $V_{DD}/2$ over the full oscillation cycle.

— W_p/W_n = 1.25. Nominal (W/N)$_n$ = 400n/150n

— **1:1 ratioing: Observed 10.0% fractional frequency tuning with L=150nm, FOM=-162.6 dB.**

— **1:2 ratioing (header/footer larger): Observed 4.8% fractional frequency tuning with L=150nm.**

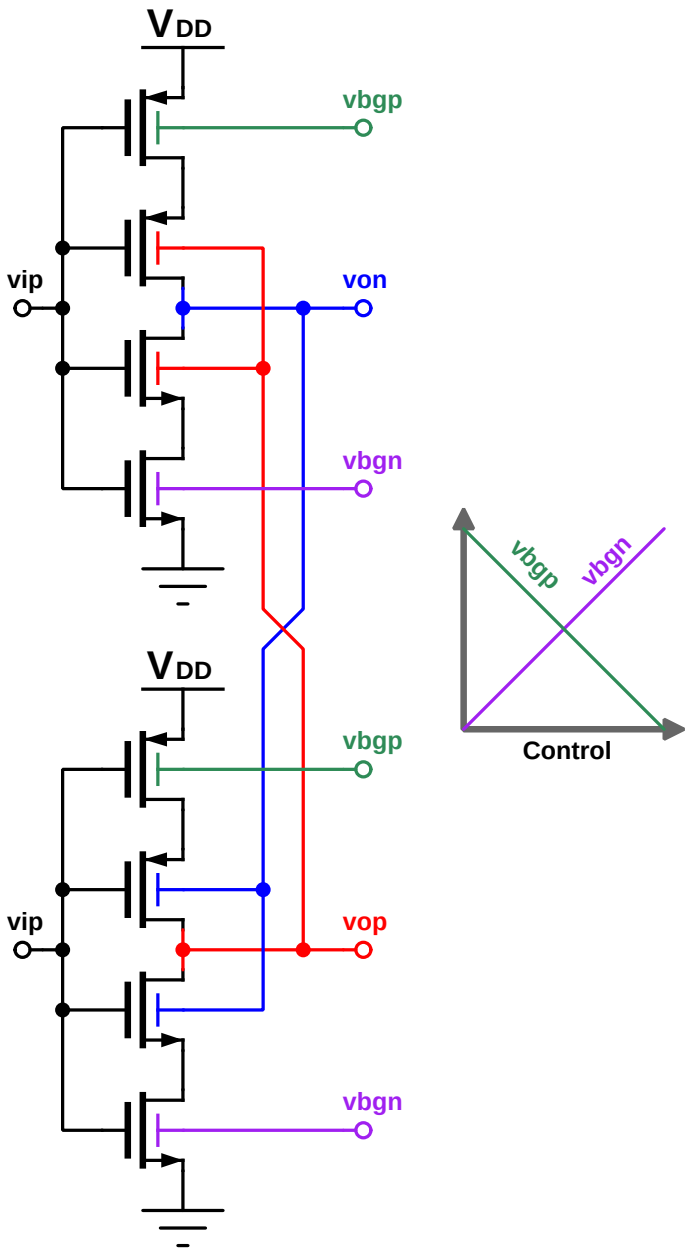
— Still hard to get required $< 1\%$ fractional frequency tuning.

— Not as linear as I had hoped, K_{VCO} decreases by -33% when V_{DD} is swept [0, 0.8] V.

— I have observed a decease in γ at higher back gate biases, this and mobility degredation(??) might explain this trend.

— PVT (coarse), medium and fine tuning all need to coexist (overlap in frequency).

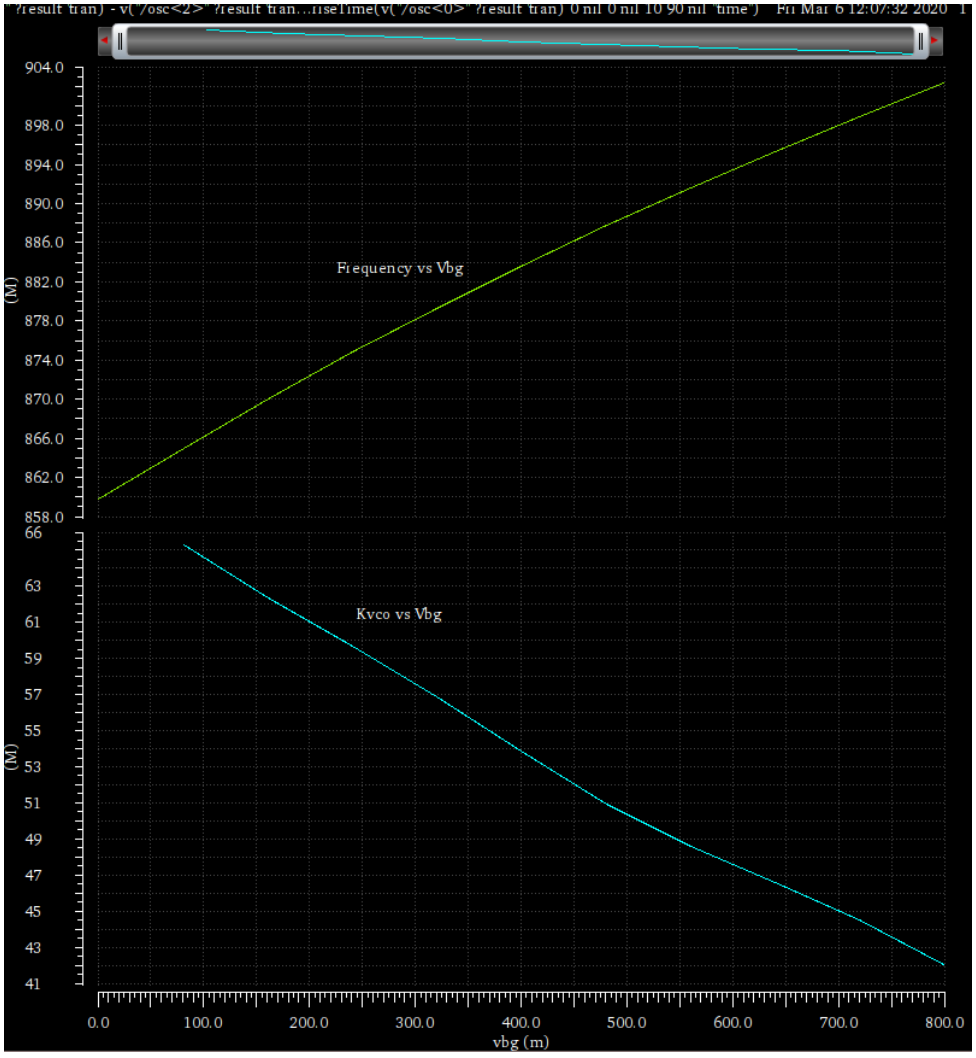
— PVT tuning achieved with bank of differentially connected capacitors



— Fine/medium tuning achieved with parallel combination of header/footer transistors. The ratio of these devices affects the difference of the ranges.

3.5 Full circuit

3.5.1 Layout


Frequency vs Vbg
Kvco vs Vbg
(M)
(M)
904.0
898.0
894.0
890.0
886.0
882.0
878.0
874.0
870.0
866.0
862.0
858.0
66
63
61
59
57
55
53
51
49
47
45
43
41
0.0
100.0
200.0
300.0
400.0
500.0
600.0
700.0
800.0
vbg (m)

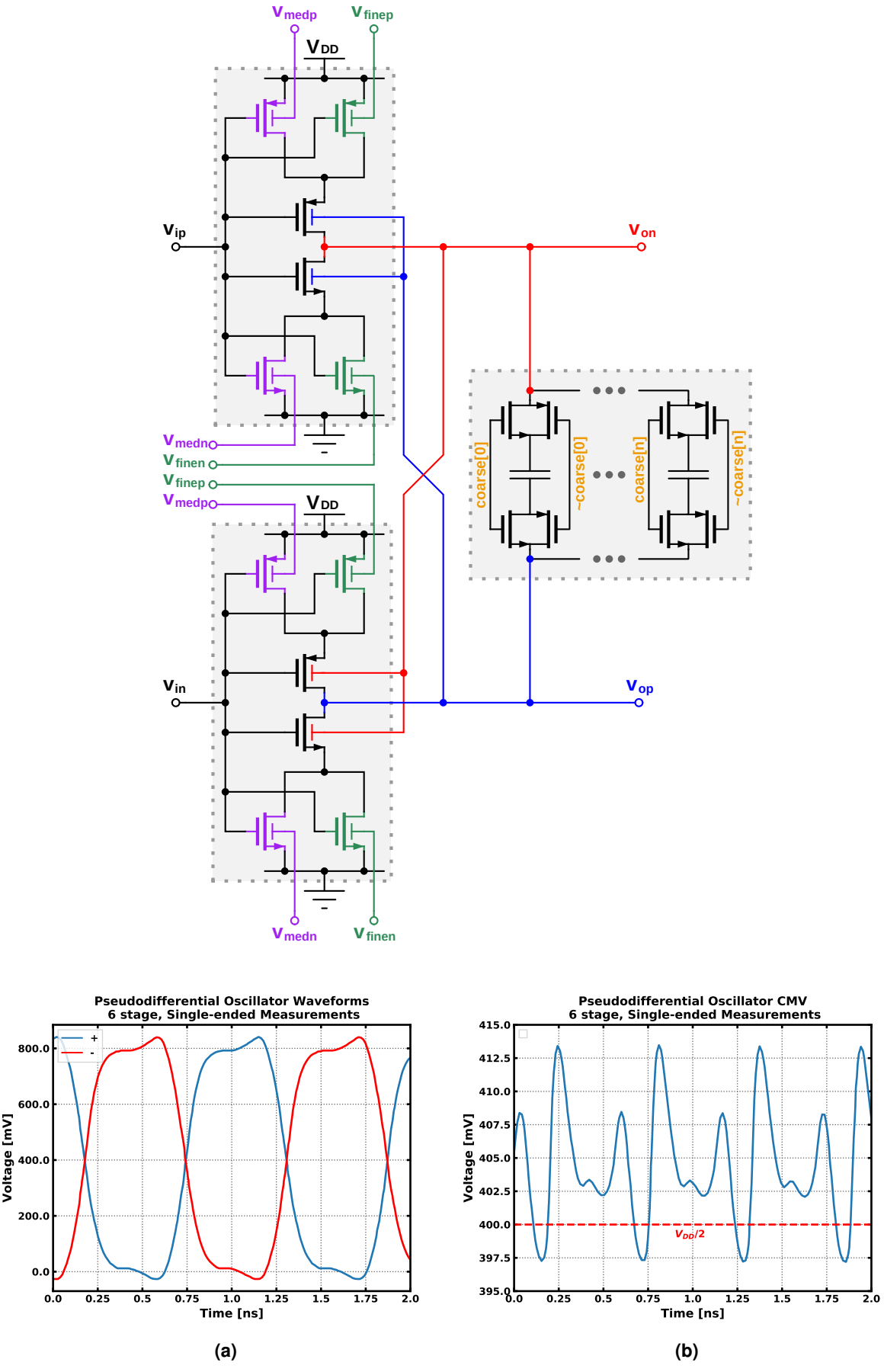
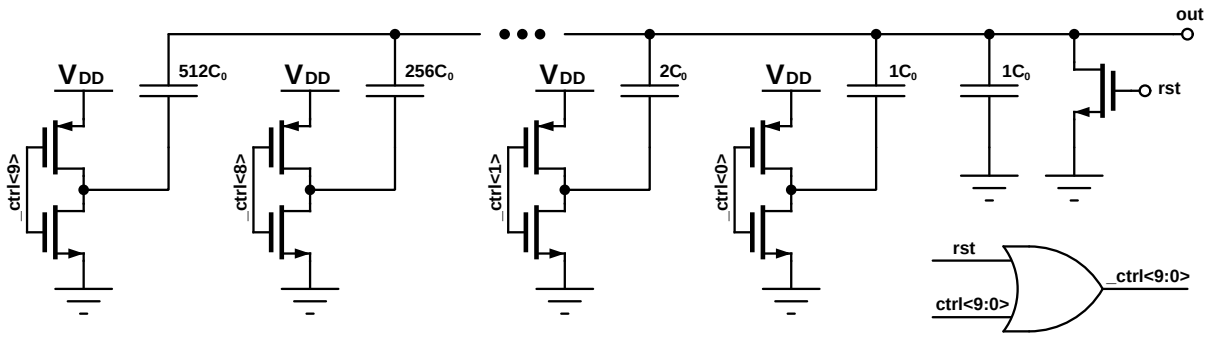


Figure 46: (a) Oscillator single-ended waveforms, **(b)** Oscillator common mode voltage waveform.

3.6 CDAC

3.6.1 Circuit



3.6.2 Layout

3.7 Logic

— Phase error zeroing reset implemented.

— Reset asserted (synchronously) for single cycle

- DCO reset is at de-assertion of RST
- Logic is reset at clock edge at end of RST assertion

— Allows for physical oscillator phase and digital phase error variable to be simulataneously set to zero.

- Also BBPD doesn't work with BOTH phase/frequency error.

— Should enable faster lock (only initial unknown is frequency).

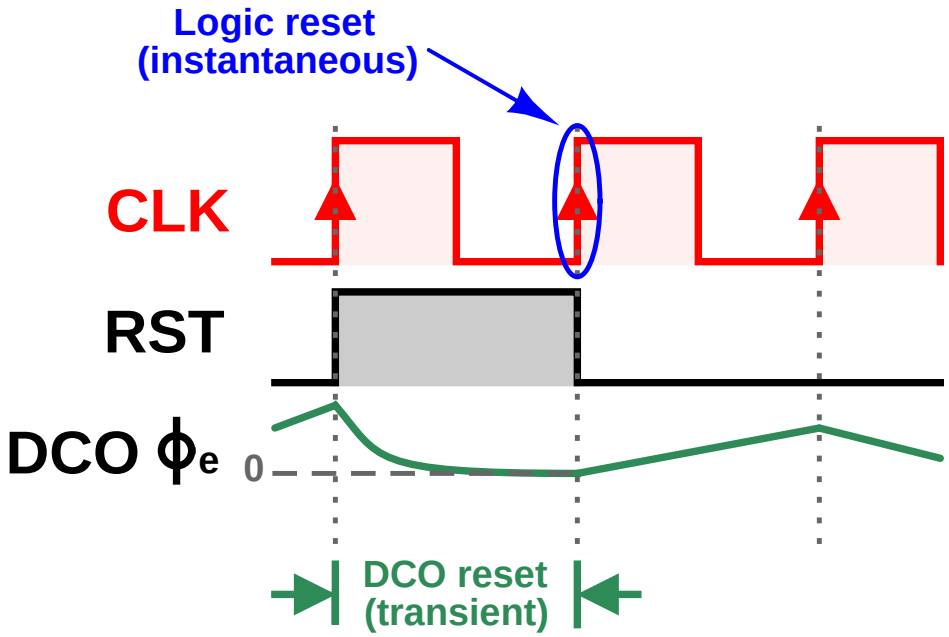
— Really only possible with the ring oscillator (LC can't start instantly)

Reset scheme

— Controller consists of 5 state FSM

1 Calibration

2 Run PLL, synchronous counter (timed start-up)



3 **Run PLL, BBPD**

4 Sleep (triggered externally)

5 PLL restore (when sleep de-asserted)

— Calibration also has FSM, which implements a frequency-error minimizing algorithm

- Starts at lowest capbank code, increments until argmin.
- Frequency error by integrating error out over a number of cycles
- Freq. resolution = f_{ref}/N_{cycles}
- N_{cycles} = 4 yields 0.5% fractional resolution (vs cap bank resolution of 1.2%)

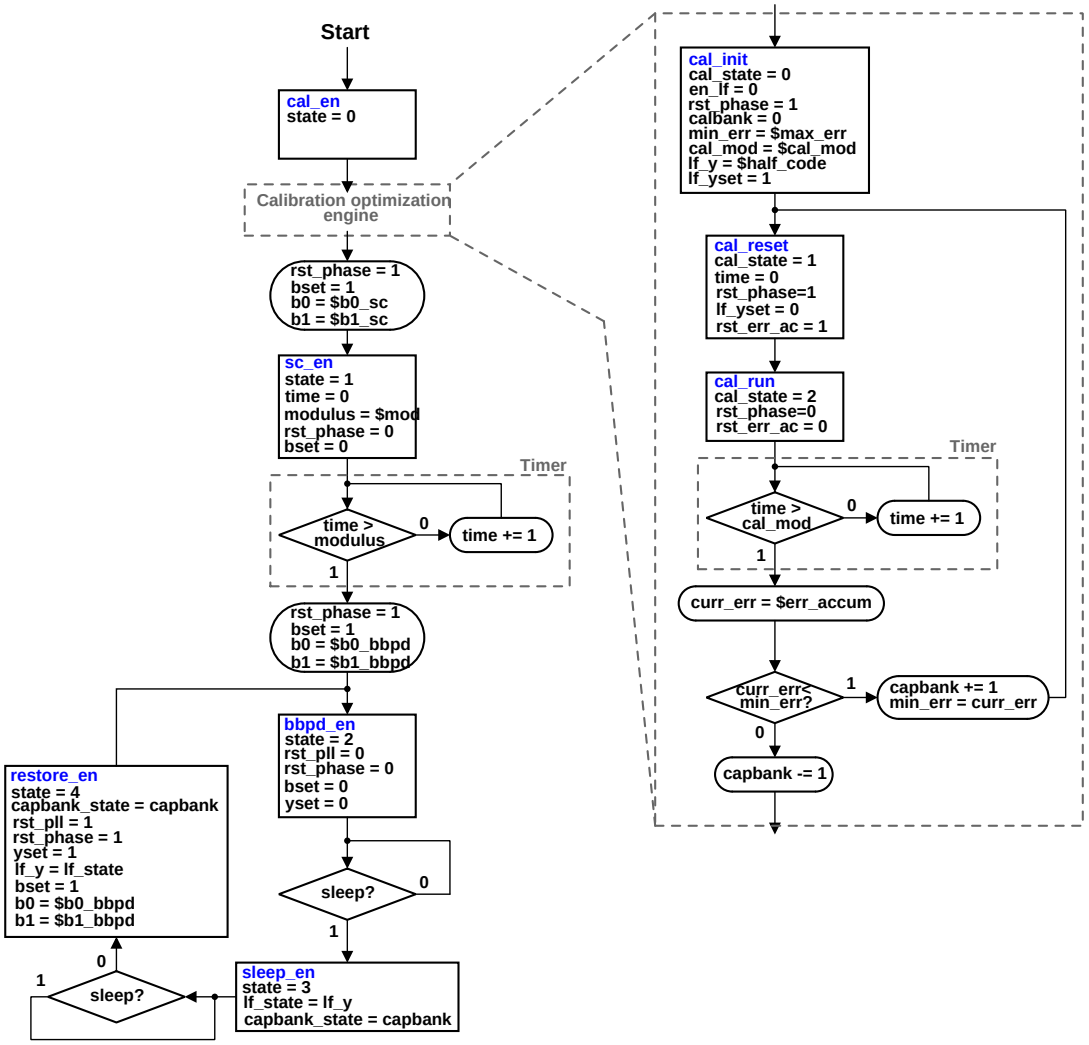
3.7.1 Circuit

3.7.2 Layout

— Total area for logic = 716μm^2.

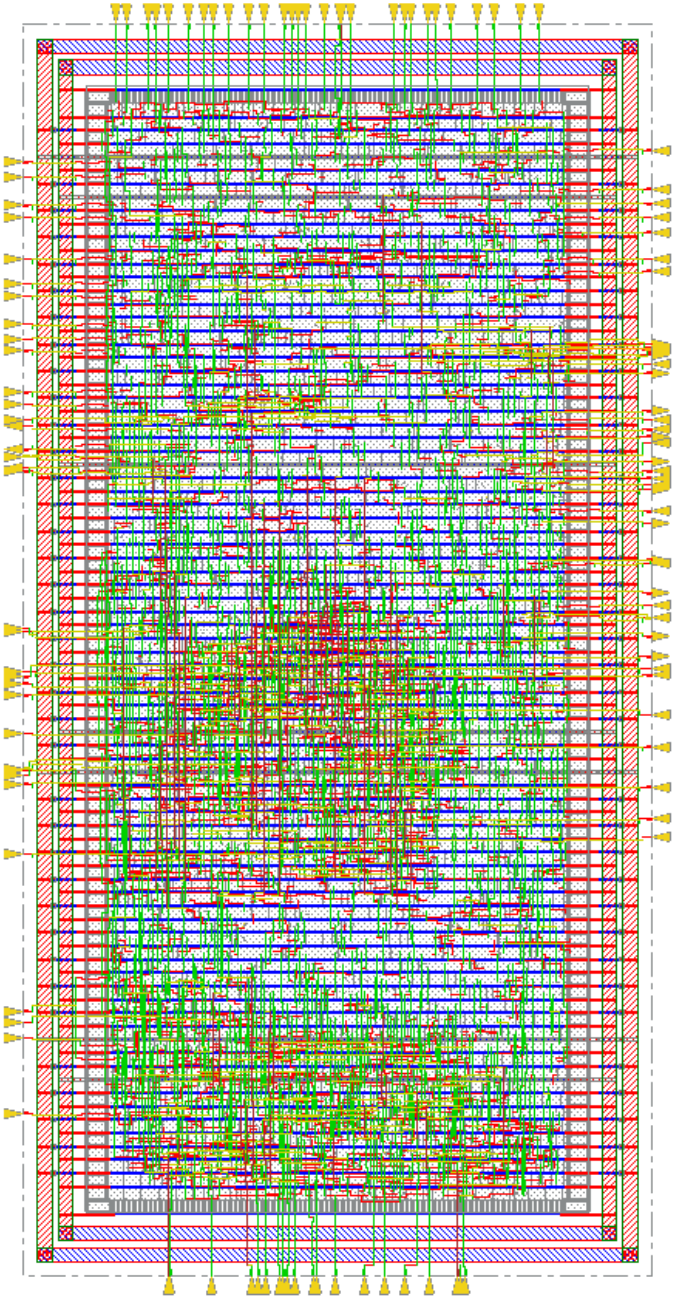
— Layout in 30 x 40 μm, ca. 50 % density.

— Power = 31.4 μW at 0.65V (82% leakage).



— Need to test at 0.5V, should be acceptable

— Need to replace pins (when fully decided)



3.8 Output buffer

3.8.1 Circuit

3.8.2 Layout

— **Edge time out of ring oscillator is slow.** Slow edge time allows noise to couple to phase:

$$\Delta\Phi = 2\pi f_{osc} \left(\frac{dV}{dT}\right)^{-1} \cdot \Delta V \tag{145}$$

— For good phase detector performance and to avoid effects of external loading, buffers are needed.

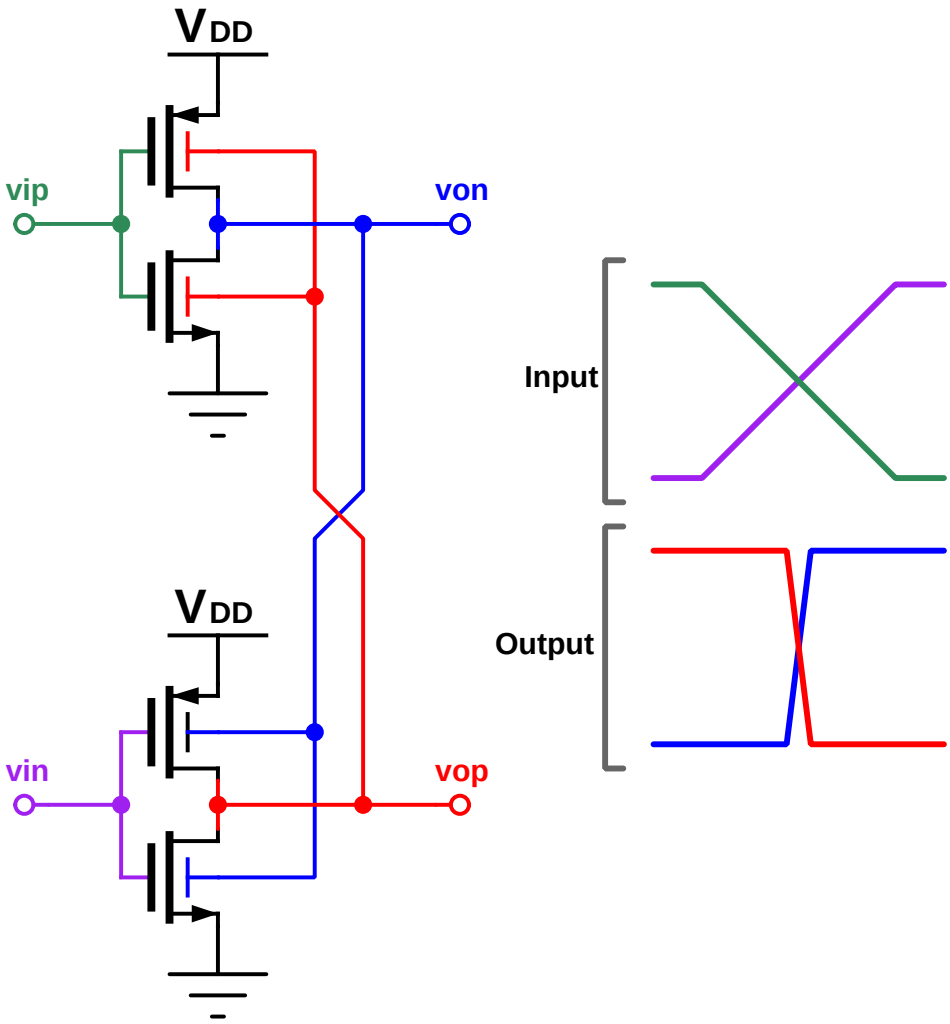
— Highest noise susceptibility when crossing V_{CM}.

— If A_i is the inverter gain at V_{CM}, the pseudodifferential buffer stage here will provide the following CMRR:

$$CMRR = \left|\frac{1+\gamma A_i}{1-\gamma A_i}\right| \tag{146}$$

— Conveniently in 22FDX, γ = 0.075 and $A_i \approx 14$ with min. length PFET+LVTNFET at $V_{DD} = 0.8$. **Thus CMRR = 26 dB.** This should help reject supply noise.

— Longer L yield essentially 0 dB CMRR.



3.9 Synchronous Counter

— Two choices for coarse linear phase detector, delay line TDC or synchronous counter.

— **Coarse delay line TDC**

– (-) Complexity grows as $\mathcal{O}(n)$.

– (-) Requires calibration of delay cells (possibly slow).

– (-) Linearity issues, with poor calibration, gain accuracy is a problem.

– (-) Needs divider.

— **Synchronous counter**

– (+) Complexity grows as $\mathcal{O}(log(n))$.

- (+) No calibration, no linearity issues.
- (+) Divider not needed (reduces noise, power?).
- (-) High power, must run as oscillator frequency.
- (-) Resolution limited be to equal to divider modulus.

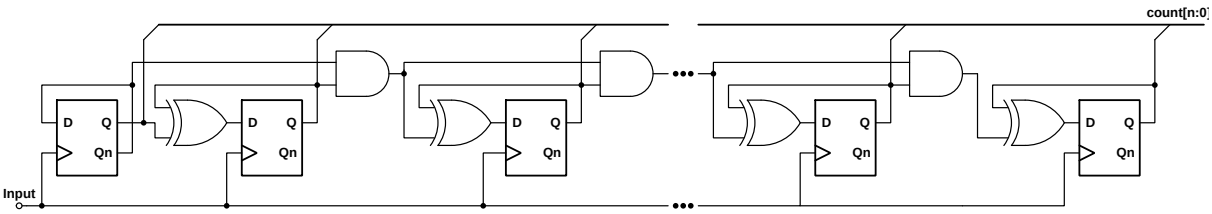
— Counter approach has *significant* advantages for PLL start up. Will switch of counter after initial lock to save power.

3.9.1 Circuit

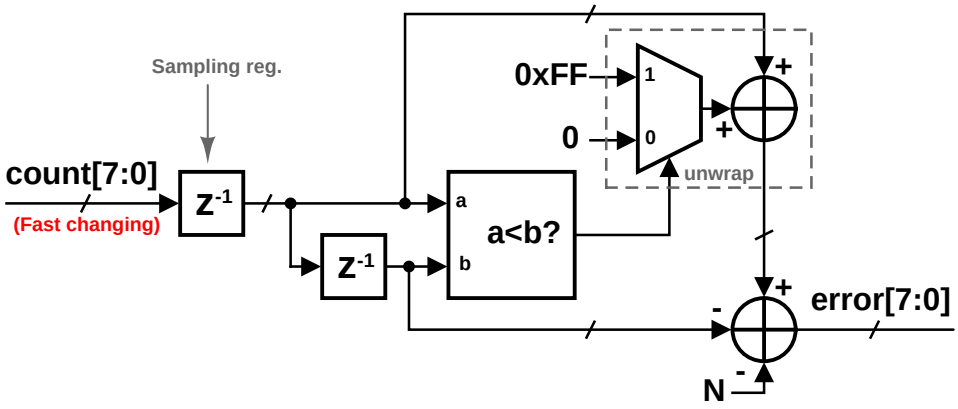
— Only tested ripple (asynchronous) counter last time.

— Implement T flip-flop with XOR gate, AND carry logic. Logic implemented as NAND2 only, with all FETS 200nm/20nm.

— Necessary to ensure that incorrect value isn't sampled, which is possible with asynchronous during ripple period. Penalty: 50 NAND2 gates, all FF's must be clocked every input cycle, i.e. more power than async.



Count to phase error decoder



3.9.2 Layout

4 Results

4.1 Power breakdown

4.2 Ring oscillator

FOM = -157.2, power = 79.06 μW at 816 MHz.

4.2.1 Phase Noise

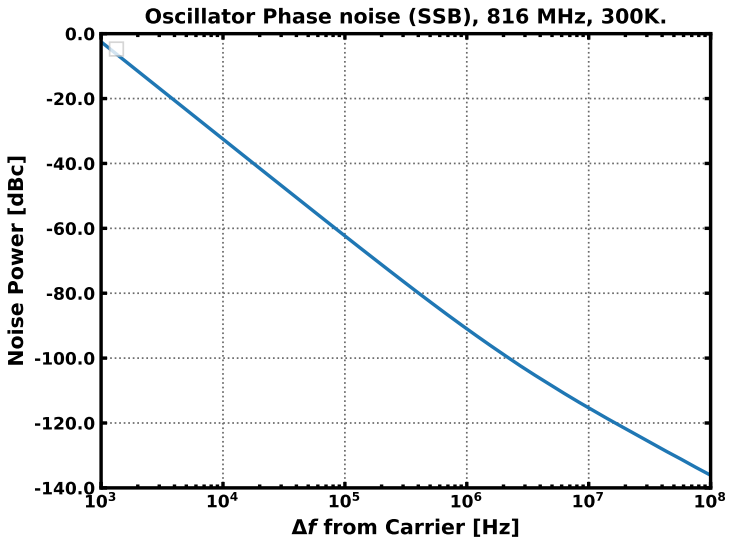
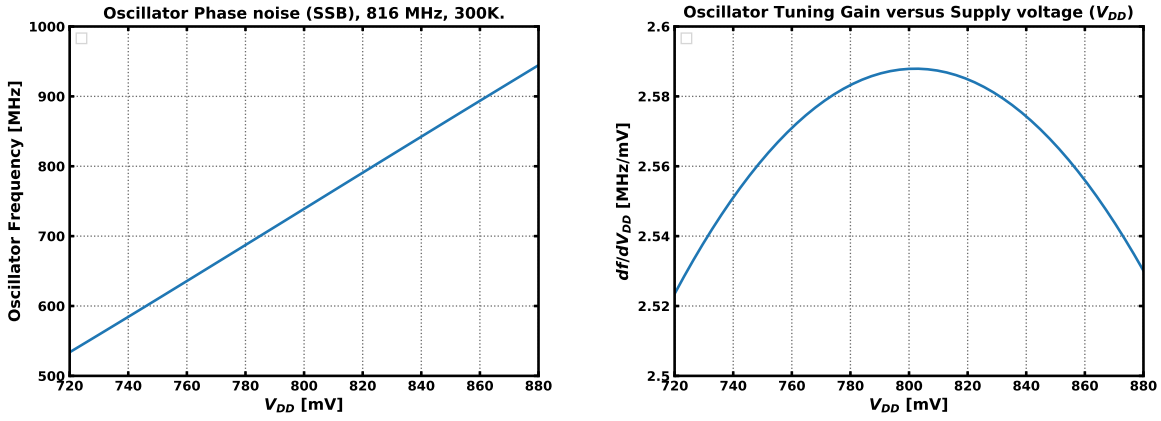


Figure 47: Ring oscillator phase noise (SSB).

4.2.2 Tuning

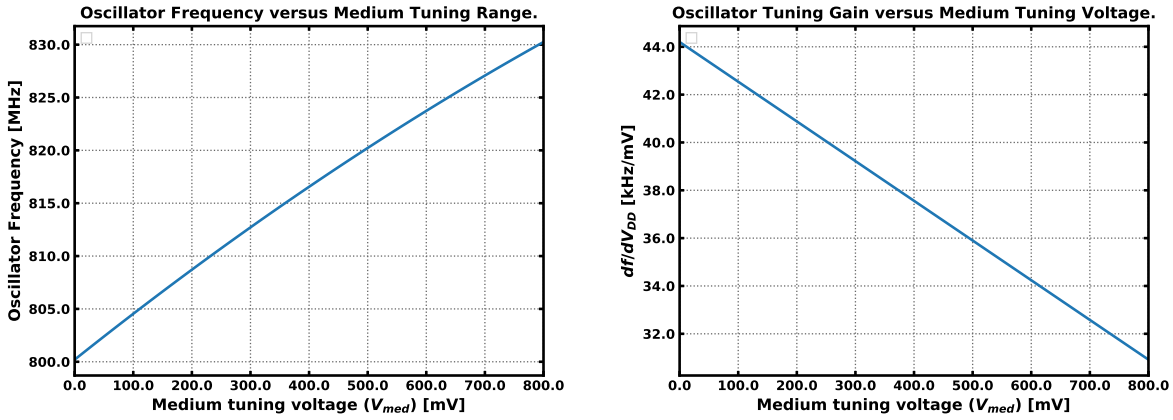
Mode	VCO Gain	Units	Normalized gain	Units
Supply tuning	2.588	MHz/mV	317.2	%/V
Medium tuning	30.92	kHz/mV	3.789	%/V
Fine tuning	5.378	kHz/mV	0.659	%/V
Capacitor tuning	9782	kHz/cap	1.19	%/cap

Table 9: PLL parameters determined from filter design and optimization process for fast lock speed with TDC feedback.



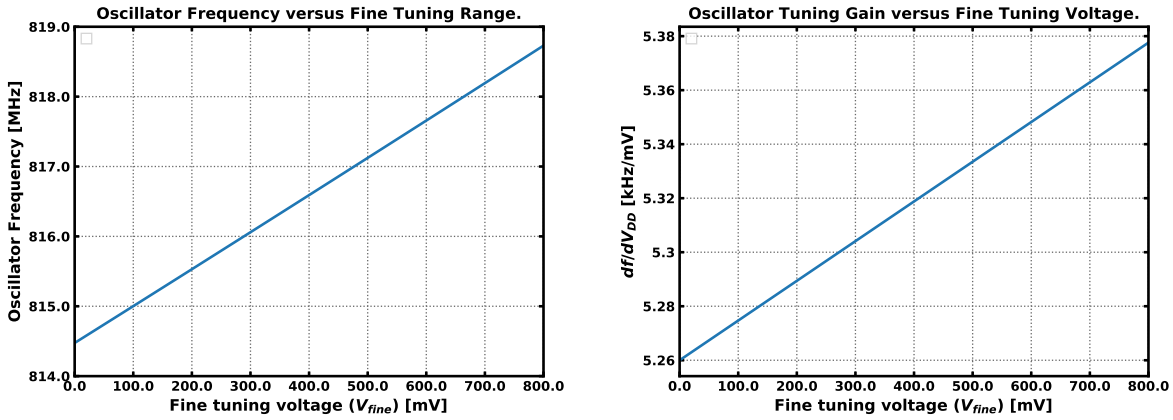
(a) **(b)**

Figure 48: Supply voltage versus ($\pm$ 10% from 0.8V) **(a)** Oscillation Frequency, **(b)** VCO gain.



(a) **(b)**

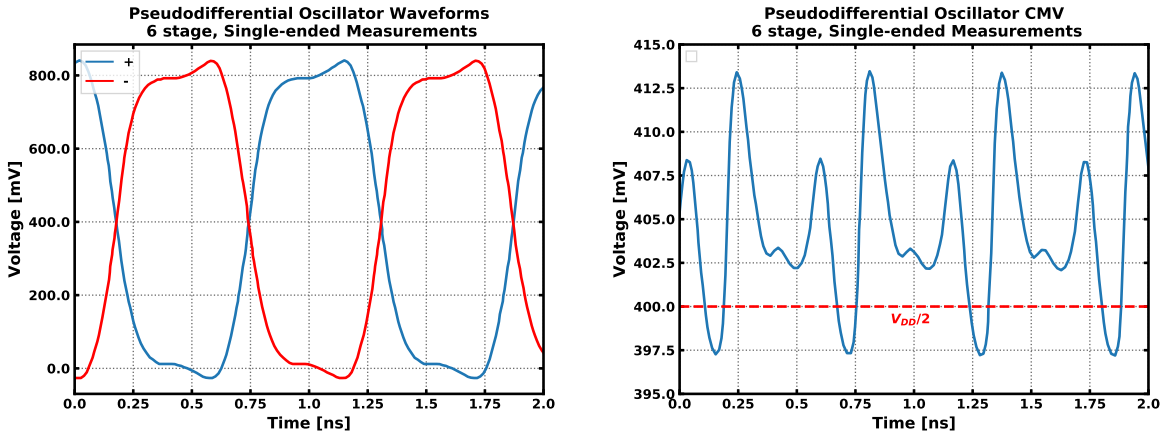
Figure 49: Medium tuning range versus **(a)** Oscillation Frequency, **(b)** VCO gain.



(a) **(b)**

Figure 50: Fine tuning range versus **(a)** Oscillation Frequency, **(b)** VCO gain.

4.2.3 Waveforms

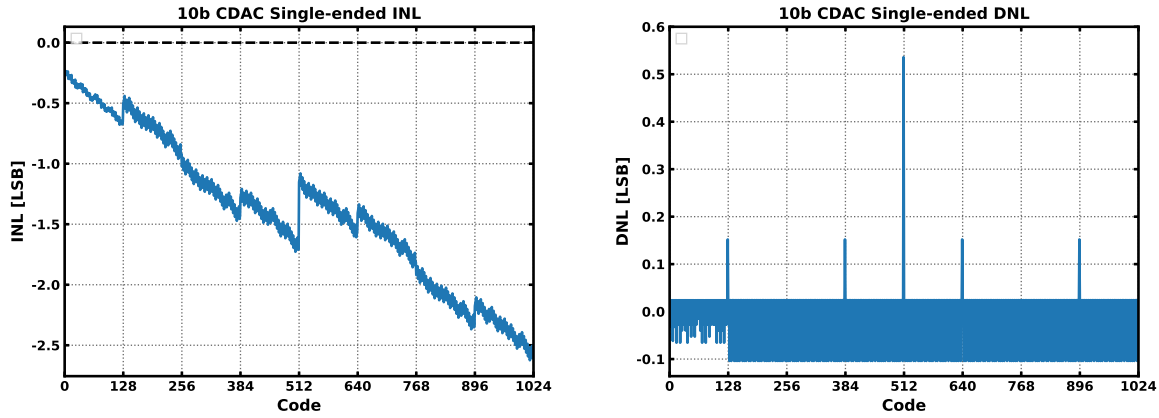


(a) (b)

Figure 51: (a) Oscillator single-ended waveforms, **(b)** Oscillator common mode voltage waveform.

4.3 10b CDAC

Unit cap = 2.185 fF, total= 2.24pF INL/DNL, unit cap, area



(a) (b)

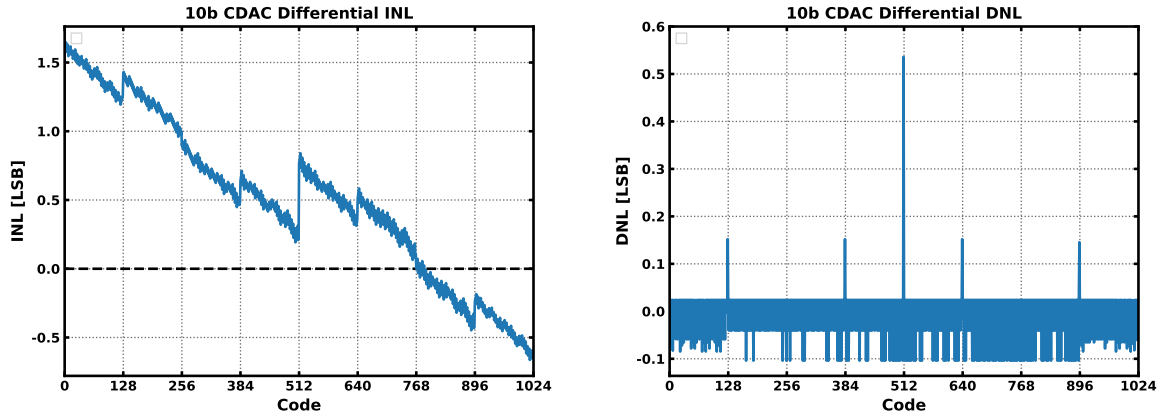
Figure 52: 10b CDAC single-ended **(a)** Integral Nonlinearity, **(b)** Differential Nonlinearity.

4.4 3b CDAC

Unit cap = 254fF, total = 2.032pF (tried to get approximately same as 10b CDAC) INL/DNL, unit cap, area

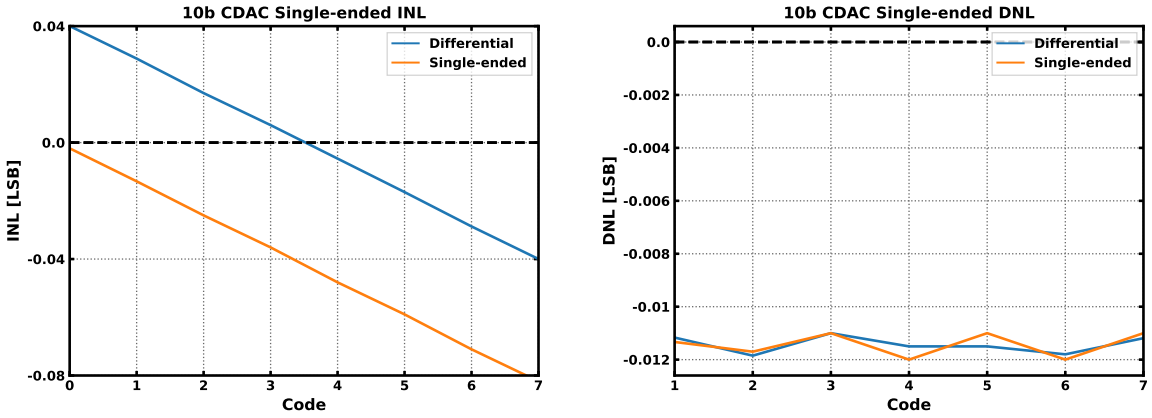
4.5 Bang-bang phase detector

Noise up to 20 GHz, 100 transitions averaged for 101 delay values, 0.8V, 1.342ps rms jitter added.



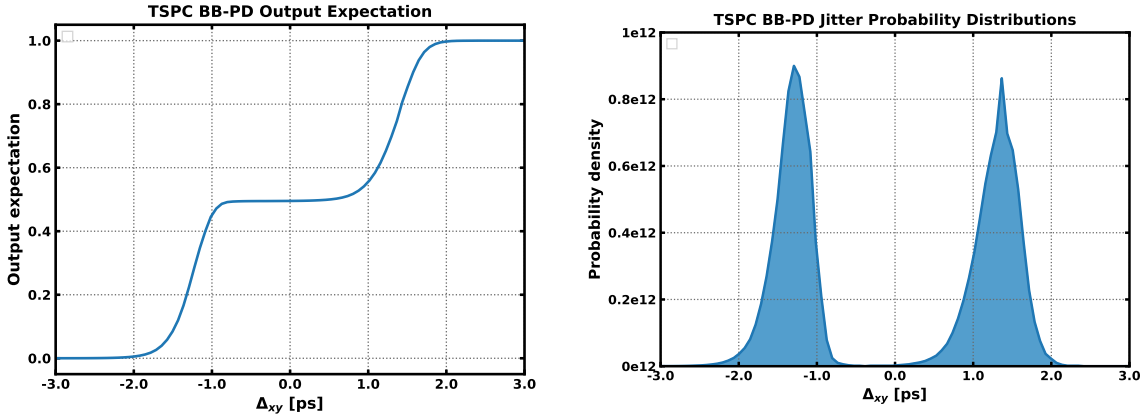
(a) (b)

Figure 53: 10b CDAC differential **(a)** Integral Nonlinearity, **(b)** Differential Nonlinearity.



(a) (b)

Figure 54: 3b CDAC differential **(a)** Integral Nonlinearity, **(b)** Differential Nonlinearity.



(a) (b)

Figure 55: BBPD extracted jitter **(a)** Cumulative Distribution Function, **(b)** Probability Distribution Function.

4.6 Logic

Power consumption

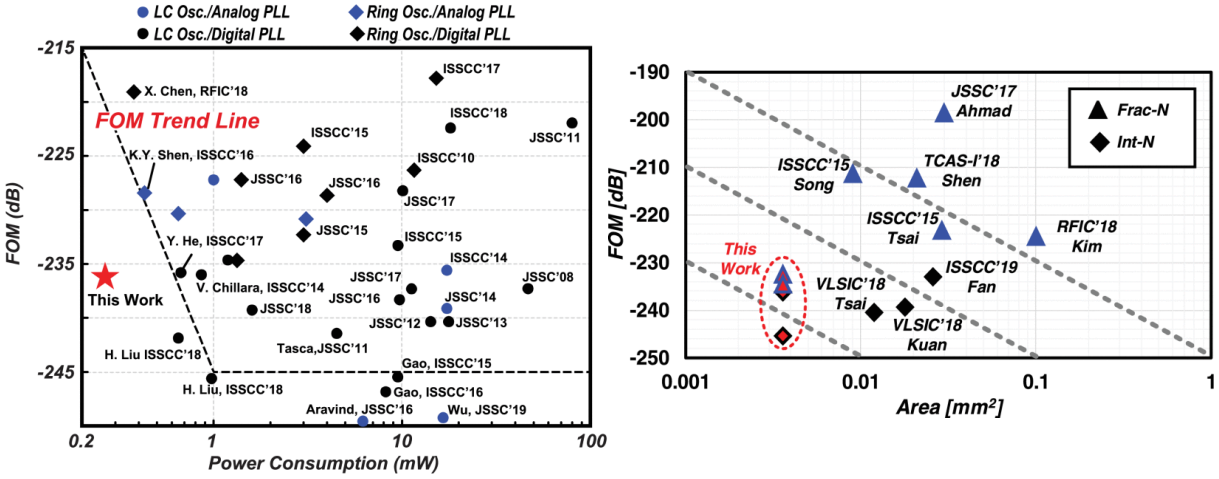
4.7 Synchronous counter

Power consumption

5 Discussion

In this discussion, the performance of the presented design solution will first be evaluated with a design example. Then, a comparison of the presented solution will be made to existing solutions in literature, pointing out advantages and disadvantages of this work. Finally, a general discussion will be made covering areas of improvement, reasoning for the central design choices made, and considerations for usage the framework.

5.1 State of art



5.1.1 Results Comparison of Design Approaches

A comparison of the two design approaches shows that the PLL utilizing the gear switching results in a superior result using the design automation framework of this work. The usage of gear switching results in lower phase noise than approach 1, with total phase noise power (residual phase modulation) of 4.36×10^{-2} rad^2 versus 3.37×10^{-1} rad^2. Additionally, the lock time is significantly lower in the PLL with gear switching, at an average of 5.96 μs versus 19.32 μs. Therefore it has been shown that this framework offers the capability to design gear-switching PLLs with performance advantages to static loop filter PLL designs.

5.2 Areas of Improvement

6 Conclusion

In this work, an automatic framework for the design and optimization of all digital PLL loop filters has been introduced. The framework allows for input of target PLL specifications, for which a digital implementation-ready filter design will be generated having (a) minimized lock time or (b) minimized phase noise in terms of integrated power, subject to specified lock time constraints. The framework additionally performs post-optimization on the generated loop filter design to ensure performance including effects of quantization in the digital loop filter. A time domain PLL simulation engine is included within the framework to verify the performance of the designed filters for acceptable phase noise, lock time and stability. It was shown in this work that the designed and optimized filters correlate with the results found with the implemented simulator. Furthermore, the design of a fast-locking and phase noise-minimized PLL using loop filter gear-shifting was demonstrated and shown to correlate with simulation.

This work will be applied in a later thesis project undertaken by the author of this work concerning the design of an ultra-low power ADPLL, in order to assist and accelerate the design process.

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A Layout

A.1 Ring Oscillator

A.1.1 Full oscillator layout

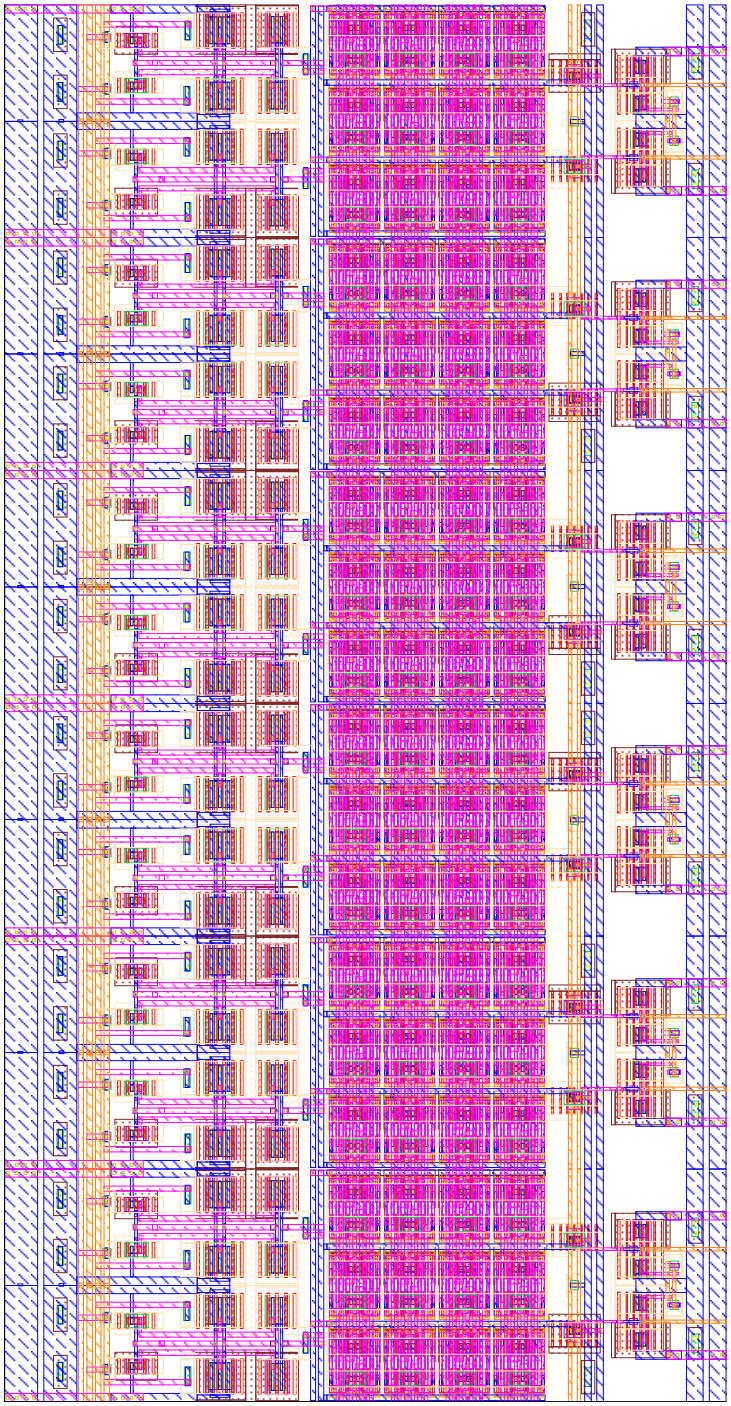

Figure 57: Full six stage oscillator layout with capacitor tuning bank, reset switches, and output buffer.

A.1.2 Pseudodifferential inverter delay cell

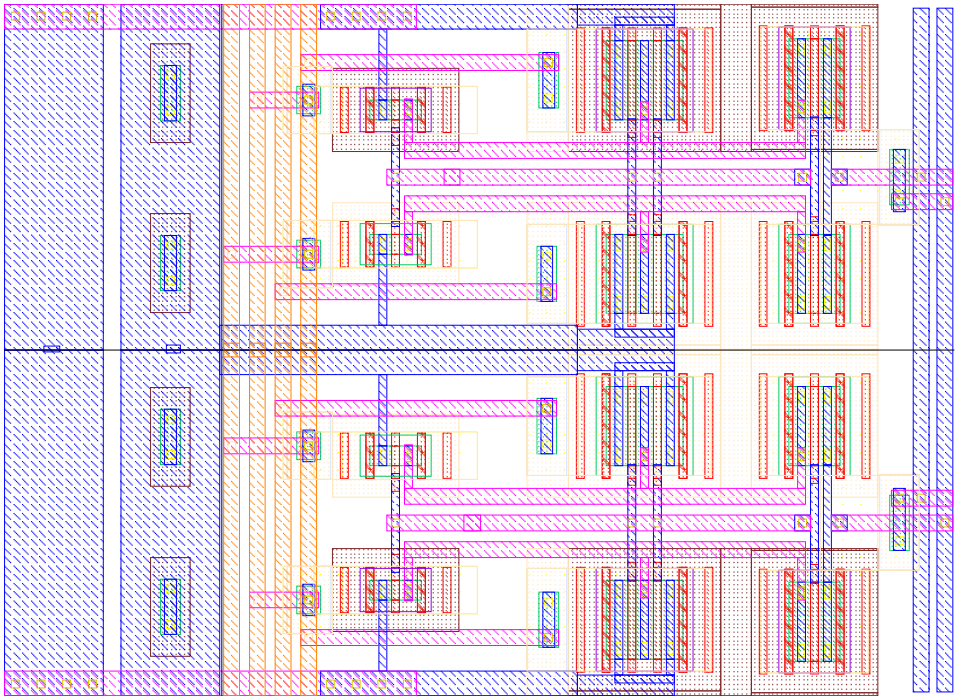

Figure 58: Unit delay stage pseudodifferential inverter.

A.1.3 Capaitor tuning bank

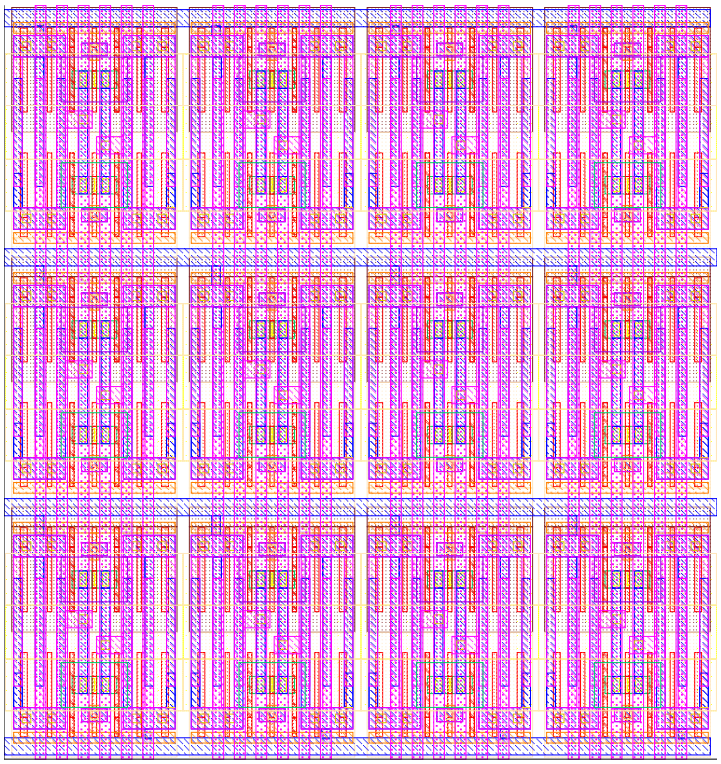

Figure 59: Capaitor tuning bank.

A.2 10b CDAC

A.2.1 Full CDAC Layout

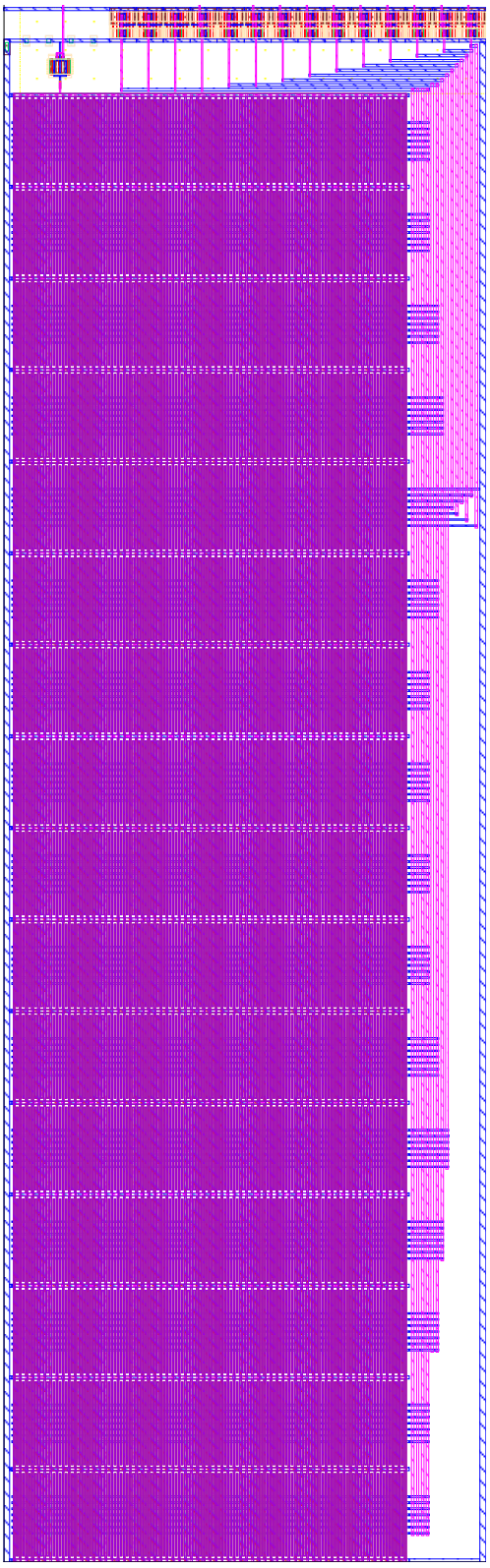

Figure 60: 10 bit CDAC layout.

A.2.2 64 unit capacitor sub-bank

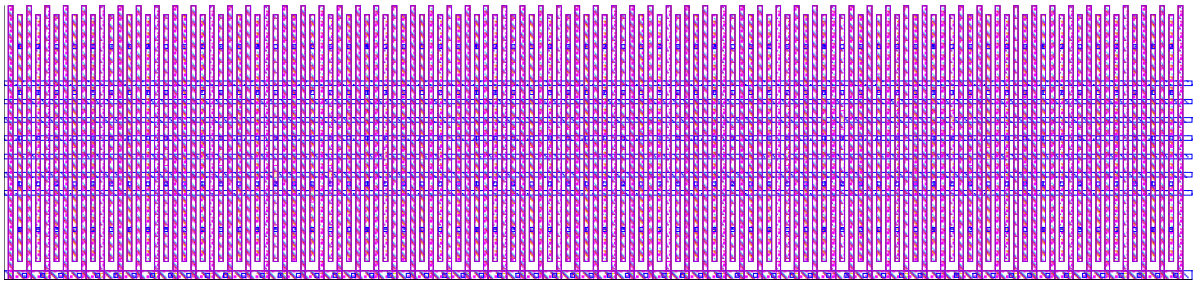

Figure 61: 64 unit capacitor bank.

A.3 CDAC unit switch

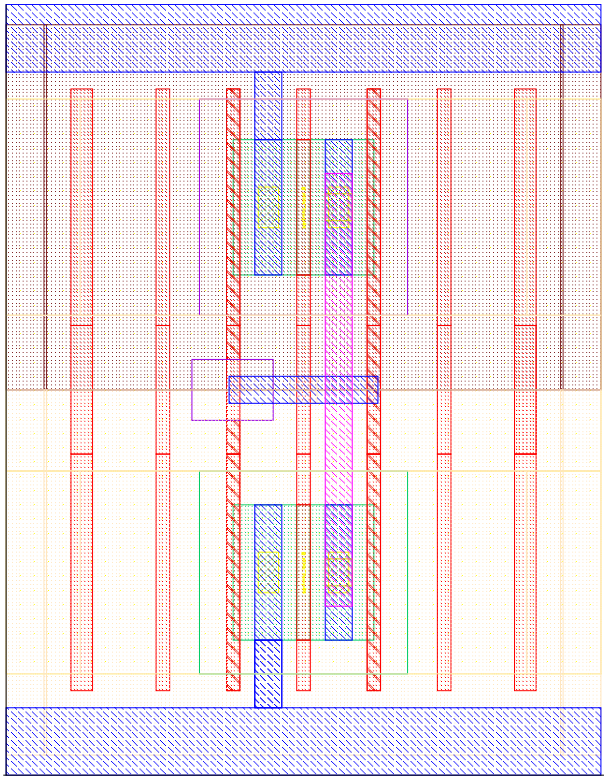

Figure 62: CDAC switch.

A.4 3b CDAC

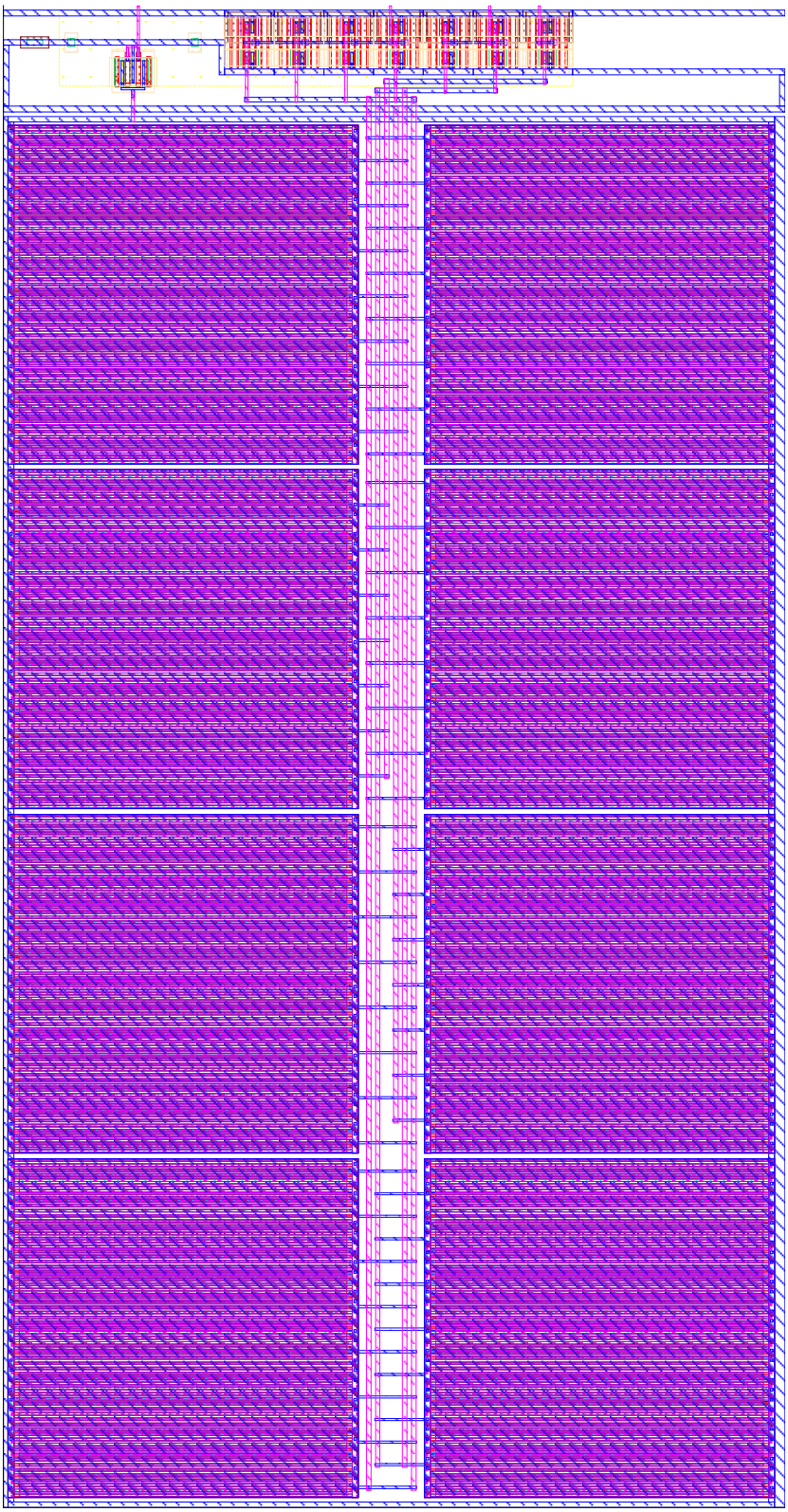

Figure 63: 3 bit CDAC layout.

A.5 Buffer

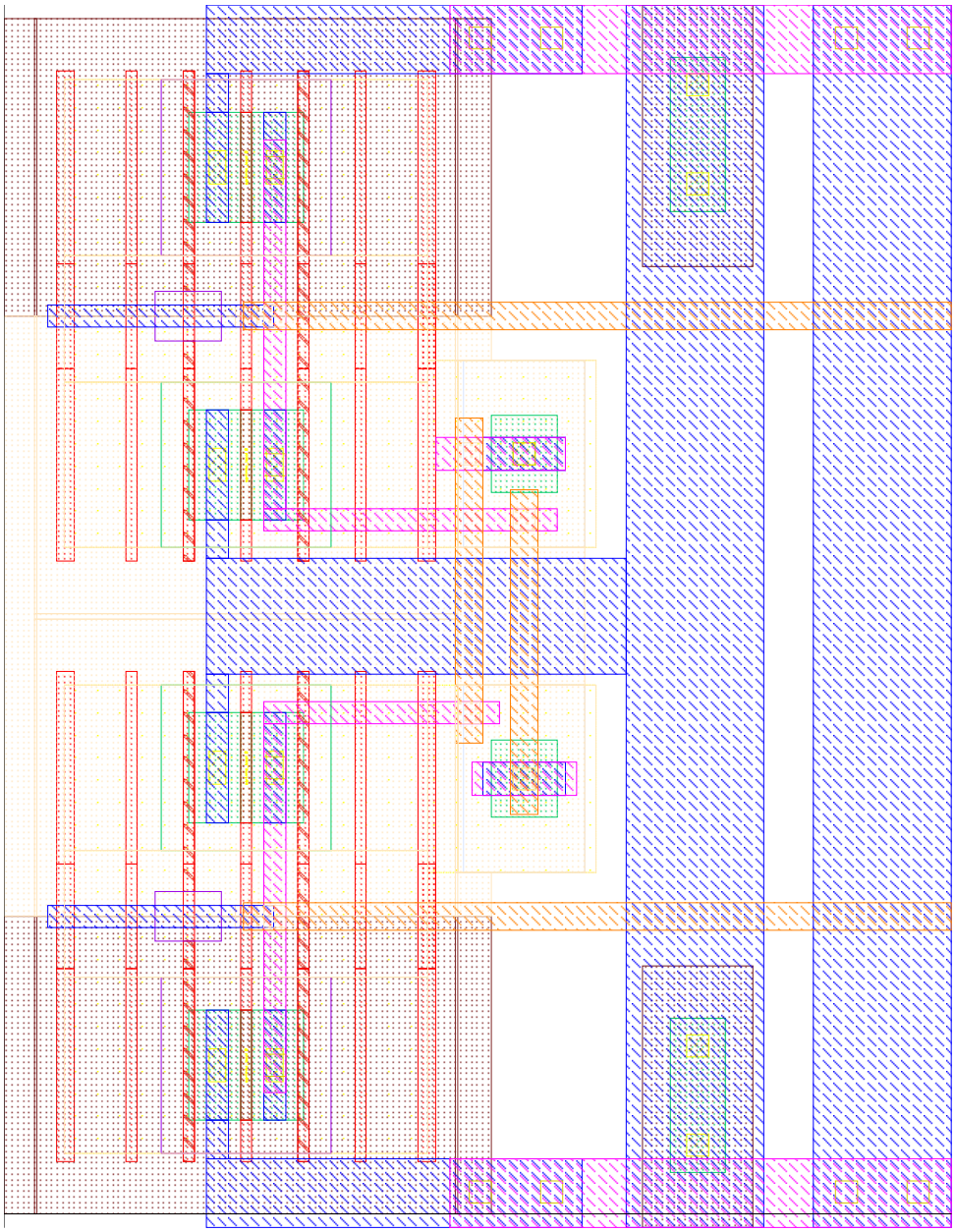

Figure 64: Pseudodifferential inverter buffer cell.

A.6 BBPD

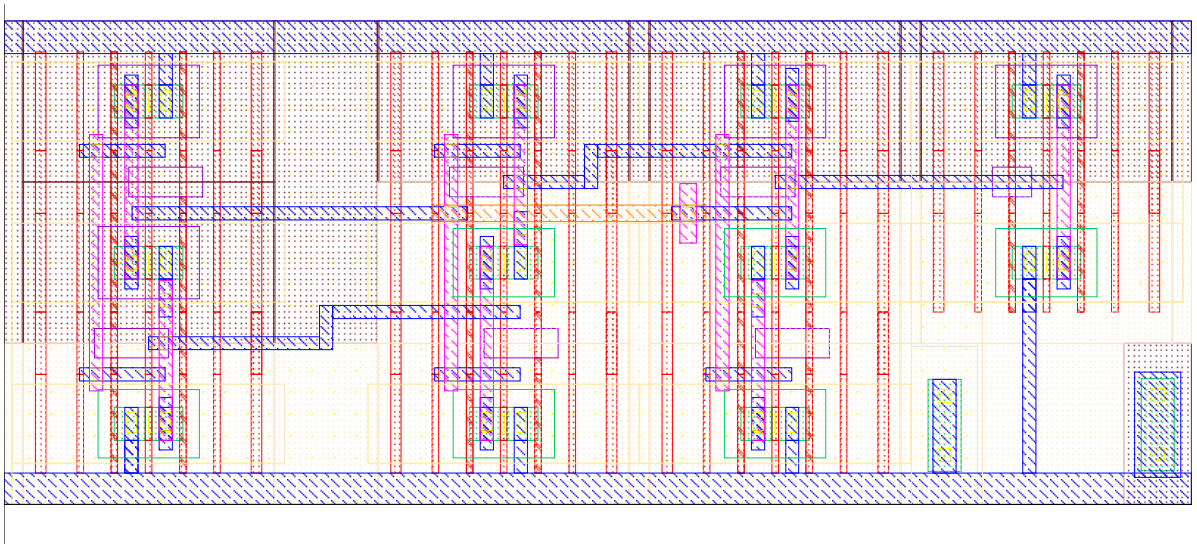

Figure 65: Single ended bang-bang phase detector.

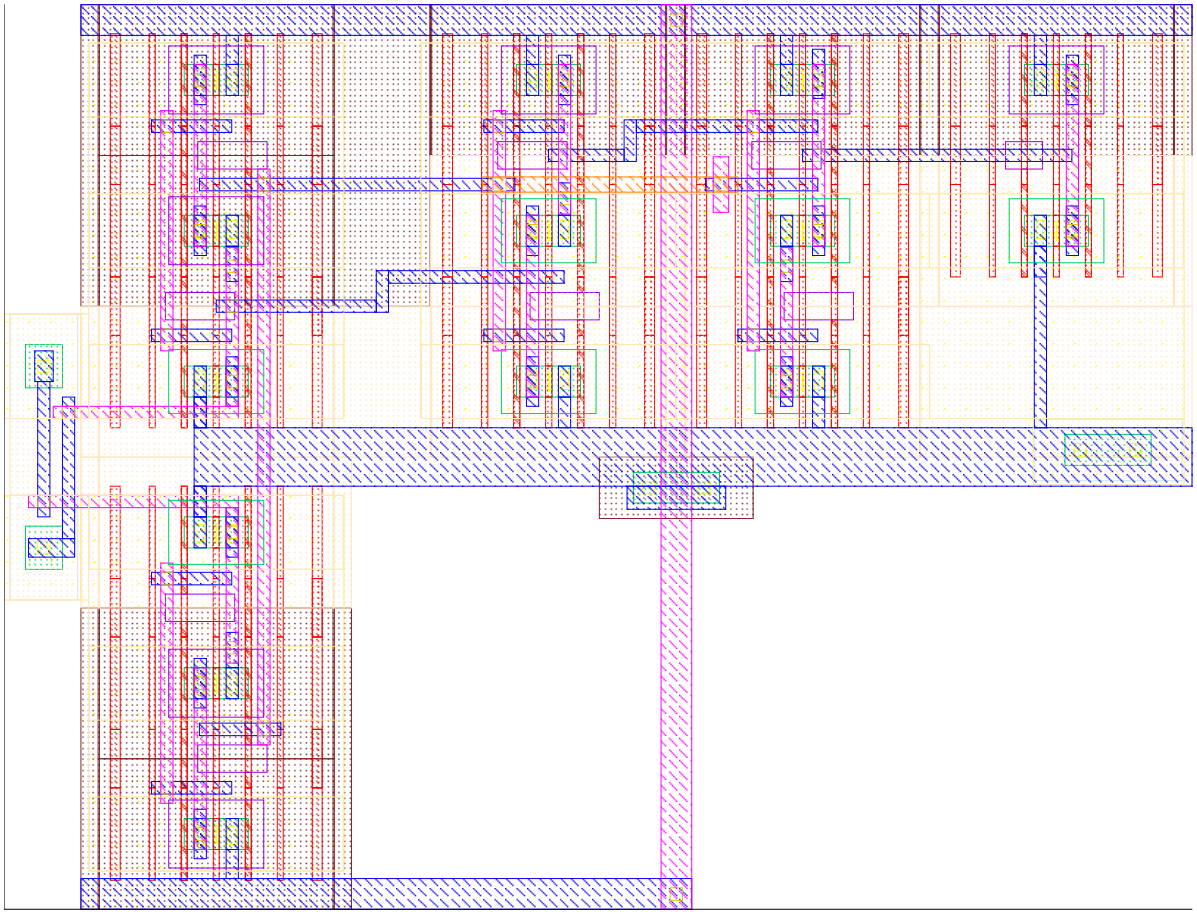

Figure 66: Pseudodifferential input bang-bang phase detector.

A.7 SPNR Logic

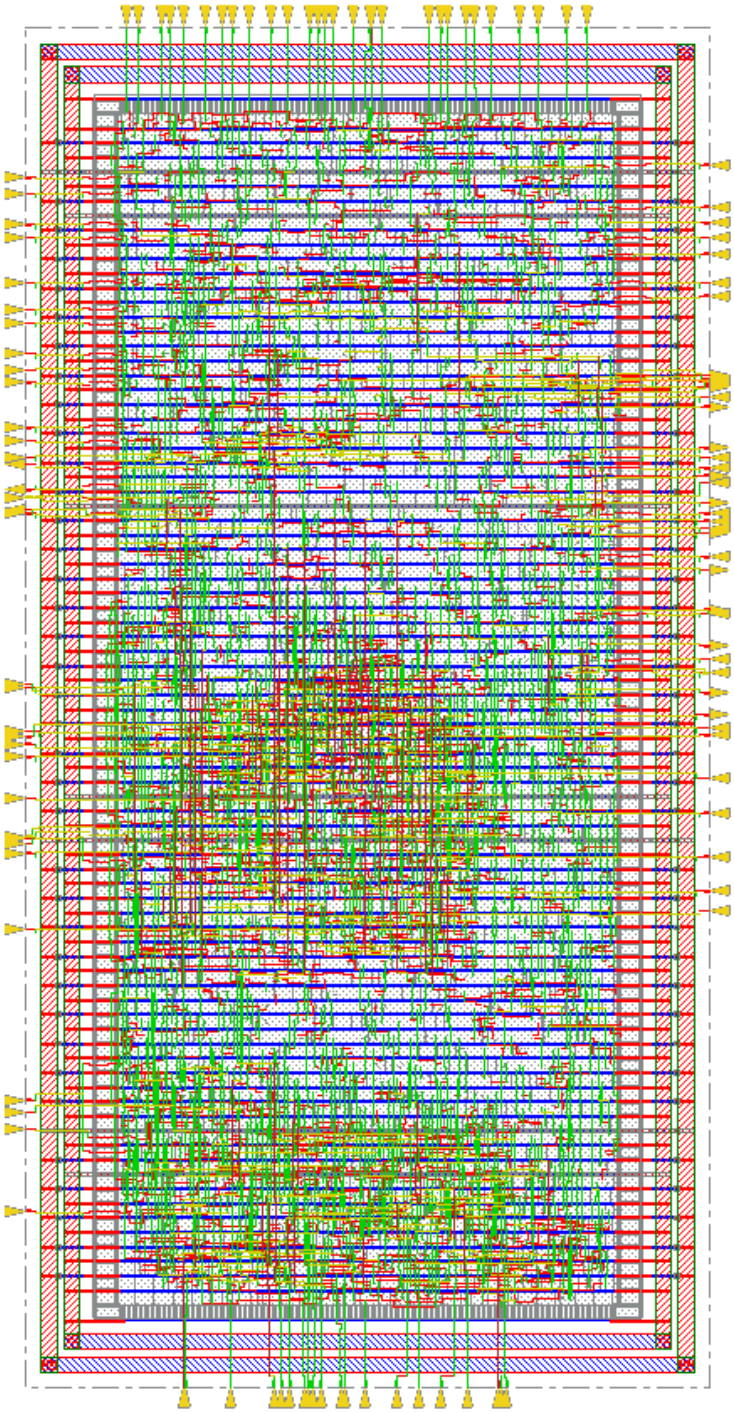

Figure 67: Place and route generated logic for PLL.

B Estimating PSD with Autoregressive Model

The following is based on [29]. Given a signal x[n] whose power spectrum should be estimated, its autocorrelation sequence $r_{xx}[l]$ with lag l must be computed:

$$r_{xx}[l] = \sum_{n=-\infty}^{\infty} x[n]x[n-l] \tag{147}$$

The autoregressive model for power spectrum, with p poles, that shall be fitted is given in 148

$$S_{XX}(f) = \frac{1}{|1 + \sum_{n=1}^{p} a_n z^{-1}|^2}\Bigg|_{z^{-1}=e^{-j2\pi f \Delta T}} \tag{148}$$

MMSE optimization of the distribution for coefficients $\{a_1, ..., a_p\}$ is done by solving the Yule-Walker equation in 149.

$$\begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ a_p \end{bmatrix} = -\mathbf{R}_{xx}^{-1}\mathbf{r}_{xx} = - \begin{bmatrix} r_{xx}[0] & r_{xx}[1] & \dots & r_{xx}[p-1] \\ r_{xx}[1] & r_{xx}[0] & \dots & r_{xx}[p-2] \\ \vdots & \vdots & & \\ r_{xx}[p-1] & r_{xx}[p-2] & & r_{xx}[0] \end{bmatrix}^{-1} \begin{bmatrix} r_{xx}[1] \\ r_{xx}[2] \\ \vdots \\ r_{xx}[p] \end{bmatrix} \tag{149}$$