Fast Switched-Capacitor Moving Average Filter for Direct Sampling Mixers

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***Abstract*—A moving average filter design utilizing a switched capacitor circuit is described. The moving average filter was implemented with a high gain and high-speed telescopic op amp with minimum channel lengths in the FreePDK45 process. The final design is able to drive up to 1pF of load to a gain bandwidth of 731 MHz with a phase margin of 89 degrees, making it very stable. The switched capacitor circuit failed to work as designed due to deficiencies with the common mode feedback of the OP amp design decgrading performance.**

I. Introduction

Recent industrial trends push for the continual reduction in size as well as power consumption of consumer electronic devices, essentially all of which contain some form of a wireless radio. At the core of these radios are mixers, used to upconvert and downconvert signals between frequencies. Conventional receiver architectures rely on one heterodyne receiver per band, which consumes large amounts of area and power for multi band systems. Direct sampled mixer approaches (e.g. MTDSM) offer a huge advantage where one mixer circuit can be used across a wide band (covering many bands), reducing die area and power usage simple by decreasing the number of circuits needed [2].

In lieu of the advantages of direct sampled mixers and their future prospect, a switched capacitor moving average filter was designed in for this project for application to direct sampling mixers. More specifically, a high performance telescopic op amp was designed as well as a switched capacitor network.

II. Design Architecture

A prototypical direct sampled mixer utilizing a switched capacitor is shown in figure 1 [7]. This circuit is the basis of this design project. This circuit features a LNTA, a mixer, and a SC moving average filter. As the mixer and LNTA designs are a different subject matter than that taught in 5333, only the SC part of the design was considered in this project. More specifically only the first stage of the SC cicuit was designed to avoid over complication the project.

A brief overview of the operation of the moving average filter is as follows: a current coming out of the RF section of the design is fed into the sampling portion of the circuit (at the caps labeled Cs). The input current contains the mixed RF signal to be filtered. The input of the MA filter then uses four switched sampling capacitors (2 per input) to convert the input

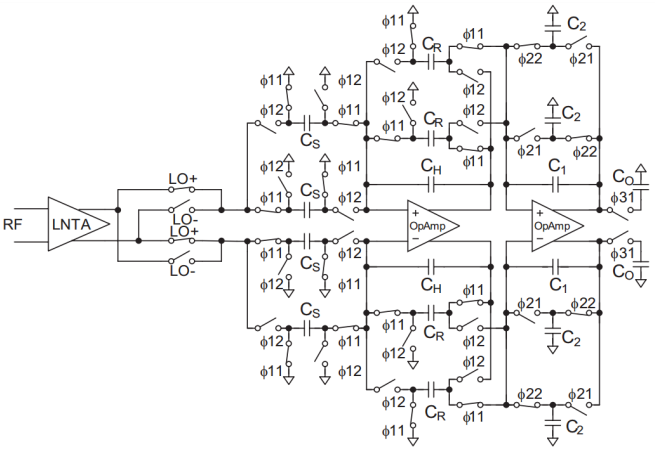

Fig. 1. Direct Sampling Mixer Architecture [7]

current to charge (sampling in this system works on charge), with each input having two samplers that alternate sampling twice a period to yield a continuous output signal (no gaps in the sampling). The charge of Cs is then shared with a history capacitor (Ch), larger then CS, on the time Cs is not being used to sample. This sharing of charge acts as a means of implementing a IIR filter, in this case a moving average filter. The output of the circuit is then shared onto an output cap Co for measing by an ADC. The output of the circuit ideally should smooth out an input signal, isolating a downconverted signal from higher harmonics if a mixed signal is fed into the circuit.

The architecture of the opamp was chosen to be high bandwidth and high speed. This is to ensure high speed filtering of input signals, as well as ensuring fast settling times. To meet these needs, a telescopic op amp design with gain boosting and common mode feedback was selected.Initially a folded cascode was selected for this project, however this was changed as the benefits in terms of gain, bandwidth, and power consumption of a telescopic topology was realized (specifically the 2x lower current consumption).

Operational Amplifier Design

Below is a table summarizing the performance of the designed telescopic op amp.

Parameter	Measured (target)
Voltage Gain	56dB (100db)
Unity Gain Bandwidth	731 MHz (1GHz)
Slew Rate	500 V/μs (750 V/μs)
Temperature Range	0-70°C
Load Capacitance	1pF
Phase Margin	89° (60°)
Supply Voltage	1.25V
Input Common Mode Voltage	0.55 - 0.9v
Output Common Mode Voltage	0.3 - 1.05V
Power	1650μW/1.31mA (1000μW)
FOM	0.558 GHz pF/mA

Fig. 2. OP amp Specifications

Some of the design specs were low, due to initially too aggressive targets.

The full design implemented is shown in the following figure. The circuit is a telescopic cascode with gain boosting and input common mode feedback. The starting point for this design was the gain bandwidth, load capacitance. From these numbers and the FOM for the project, 1mA bias current for the cascode was decided upon. From there, 0.1V Vds was chosen to allow for large output swing. Running several simulations sweeping the size of the cascode transistors showed 10u to be the optimal size for having the input common level be half Vdd. From there I sized the tail mosfet to twice the cascode ones, and the PFETS to also be 2x to lower the VGS. This design also has gain boosing, shown as the triangles, implemented as two stage op amps that take in a reference which sets the quiescent point to the node between the cascode transistors. There is also a CM input FB circuit. These will be discussed next.

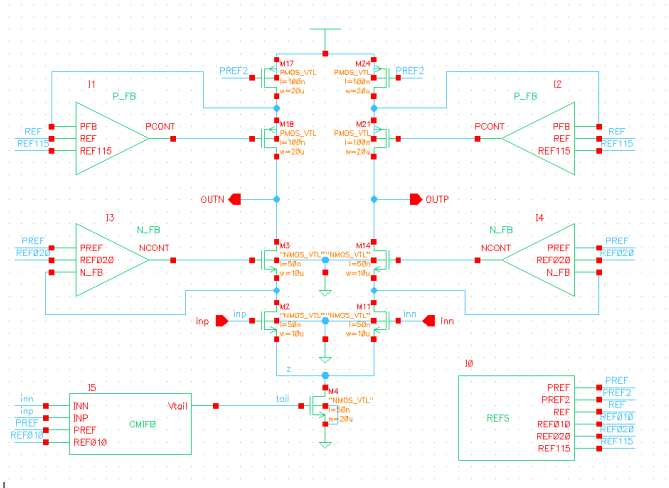

Fig. 3. Full Op Amp Schematic

The following is the gain boosting amplifier used on the lower half of the cascode. The design is a two stage op amp with p inputs in order to sense the low 0.1 V signal at the feedback node. This signal is compared to a 0.1V reference in the 5T pair and the output is then buffered through an inverting amplifier. The inv. amplifier output connects to the transistor being controlled by the gain boosting circuit. The sizes for this circuit were selected for 20uA bias and minimal size.

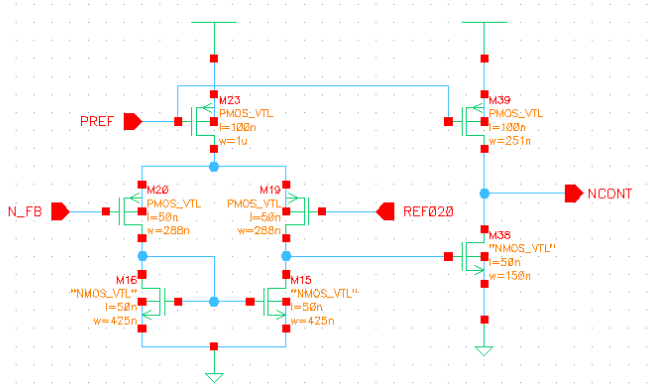

Fig. 4. Gain boosting amplifier for the bottom half of the cascode

The next circuit is the gain boosting amp for the P channel device half of the cascode. The operation is the same (complementary) to the previous one so I will not discuss it further. Design considerations were made for 10uA bias currents, minimal channel size, and channel length were found via simulation and selecting the optimal size.

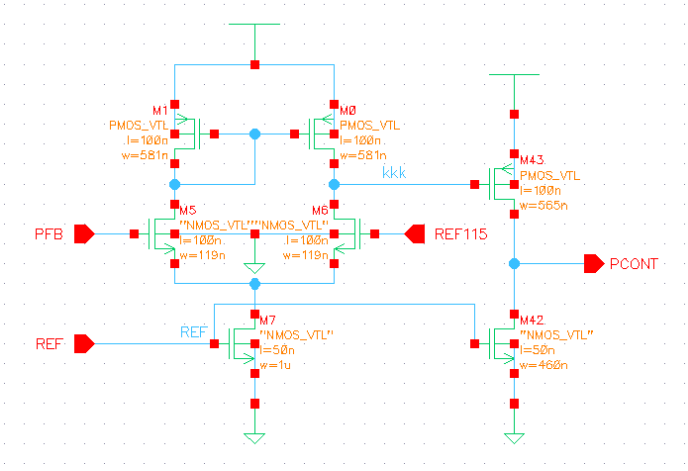

Fig. 5. Gain boosting amplifier for the top half of the cascode

The voltage reference for the opamp is shown below. It is implemented using a self-biasing threshold-referenced current referent, which has good supply rejection. This circuit works as the upper half is a current mirror, and the lower is a resistor with a different current transfer reletionship. The circuit operates stably at the intersection of the current transfer curves, with small deviations due to power supply variations. The voltage for the circuit is refered across the resistor as it has the best PSRR. All other bias voltages are generated from this reference voltage using complementry chains of P and NMOS tranistors sized to output the correct voltages when the NMOS is connected to the reference.

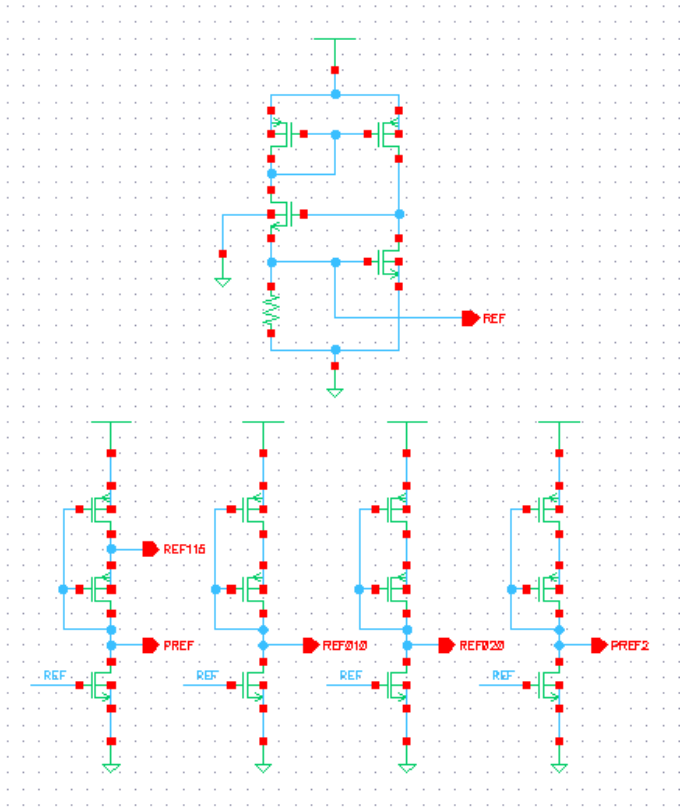

Fig. 6. Voltage reference generating circuit

The following graphic is a simulation of the voltage out of the reference vs a sweep on supply voltage. We see very little change in the output voltage, approximately a sensitivity of 0.1. This is far lower than what you would see with only using a resistor and a current mirror (0.1) for a reference.

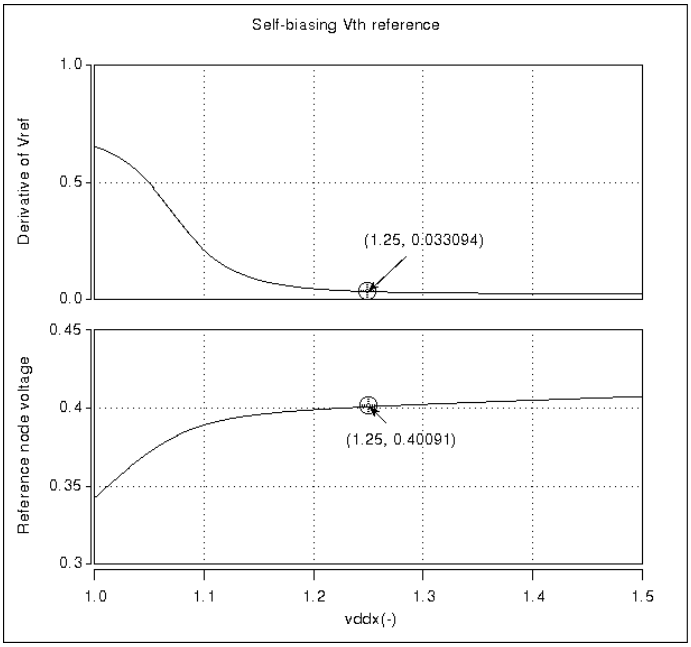

Fig. 7. Power supply sensitivity of Vth referenced voltage reference

This last circuit is the commom mode feedback circuit for the input. This works by sensing the common mode level with a differential pair connected at both the drain and source, using transistors 1/40 the size of the op amp input transistors, and biased at the same level. THe current from the diff pair is forced through a NMOS 1/40 of the size of the op amp tail transistor, which generates a reference level for the tail transistor that takes in common mode level. An opamp in used to try to force the VDS across the tail transistor to be 0.1 volts at all times to ensure high cascode impedance.

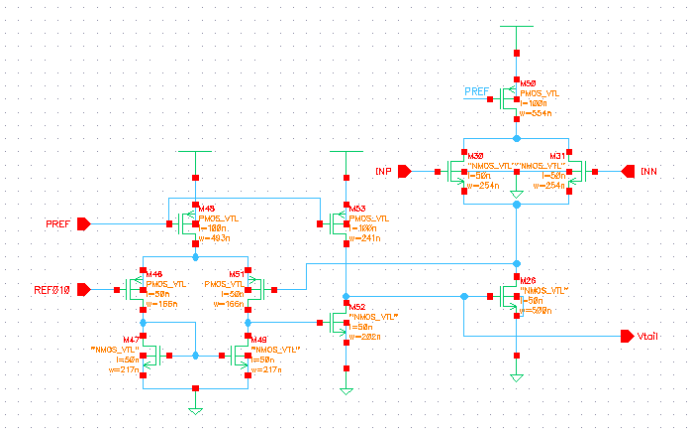

Fig. 8. Input Common mode feedback circuit

The following plot is a VTC for the designed op amp, swept from rail to rail to the input. The outputs cross as intended at half VDD for both output and input. The gain was also extracted by differentiating the curve. The observed gain is 681, or about 56dB, which is quite good. This is nearly 20db better than the design without the gain boosting (gain of 74). Therefore the gain boosting is deemed helpful. Also, the high gain value will help to give a fast rise time, as rise time is at a minimimum 1/GBWP, or 1.37ns.

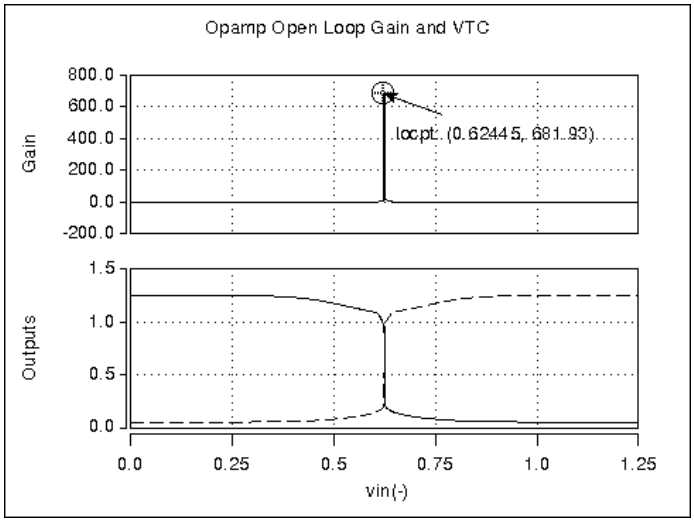

Fig. 9. Op amp VTC with full range sweep and gain extraction

The following is the bode plots for open loop performance of the opamp with 0.5pF of load on each output (1pF total). We see that the unity gain frequency is 731 MHz, with a phase margin of 89 degrees, meaning stablility is given, as well as no ringing.

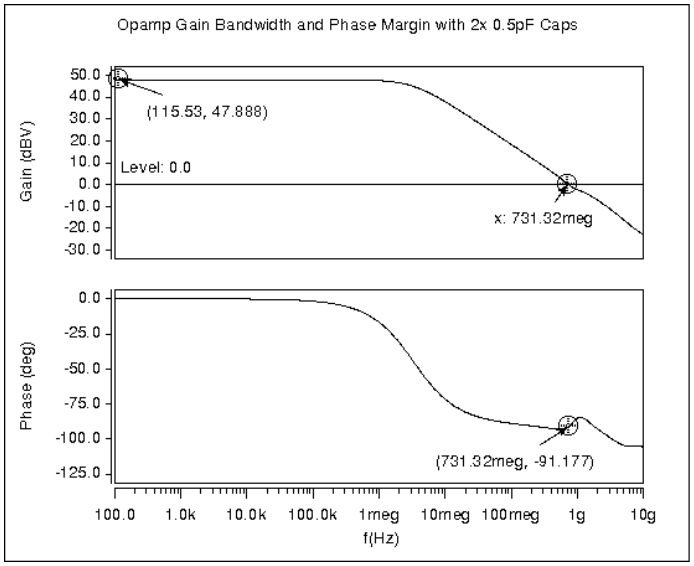

Fig. 10. Op Amp Open Loop Bode Plots

A. OP AMP Layout

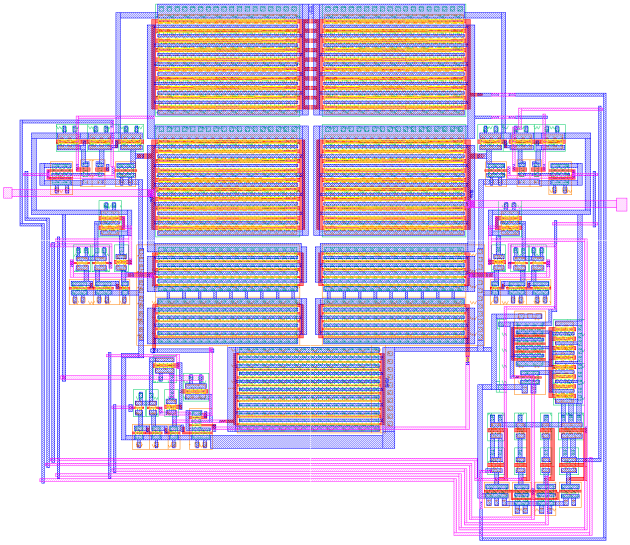

Fig. 11. Layout of the Telescopic Op amp

The following figure for the design shows the full layout for the opamp. The total size was approximately 17.5 by 15 microns, or 262 sq microns. The center region is the telescopic cascode, the right/left top circuit outside the cascode are the gain boosters, the lower left is the CMFB and the lower right is the ref generator.

B. SC Ciruit

The circuit designed is duplicated from the first stage of the moving average filter in figure 1's Direct sampling mixer. This is the right half of the schematic below. The left portion is the non-overlapping clock generation circuit, needed to prevent direct feedthrough of signal through the circuit.

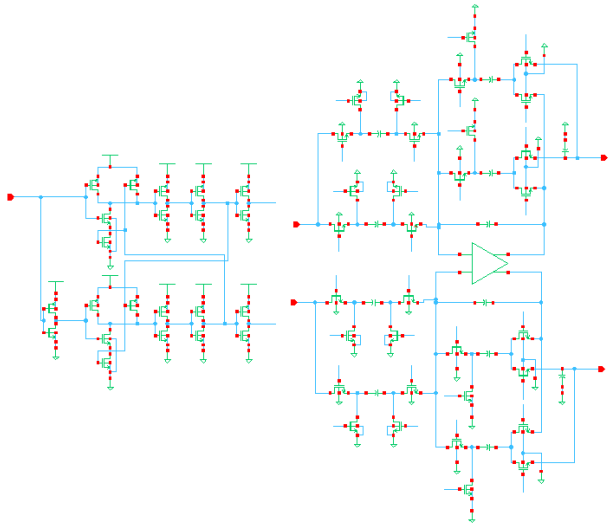

Fig. 12. SC Moving Average filter

Below is a gate level schematic of the non-overlapping clock generator. Any clock frequency up to approx 500MHz can be fed in with about 190ps of clock seperation coming out of the two clocks. This circuit was built using standard static CMOS gates.

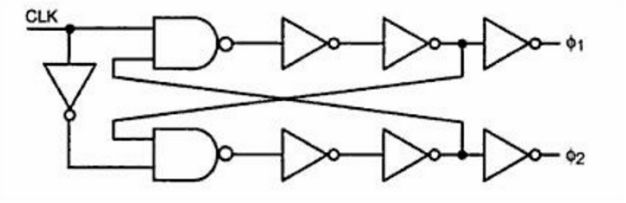

Fig. 13. Non-overlapping clock circuit

Below is a plot demonstrating the output of the non-overlapping clock with 200 MHz input. Notice the clock separation.

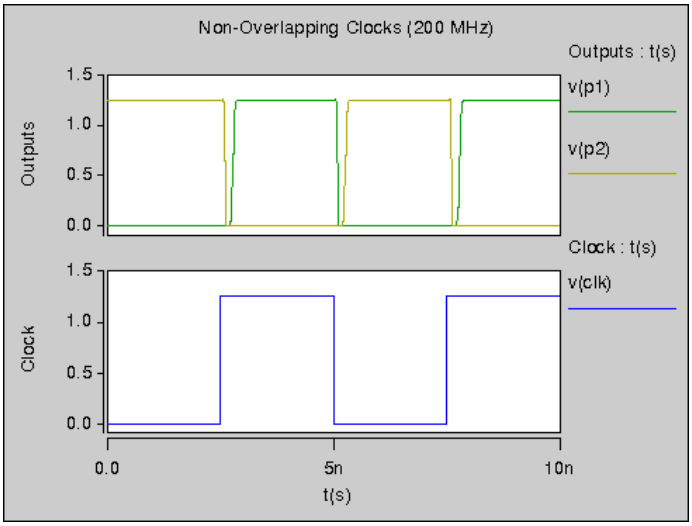

Fig. 14. Simulation of the non-overlapping clock generator

The following plot is the full layout of the design, having a size of 33 by 16.3 microns. This is about 574 microns squared.

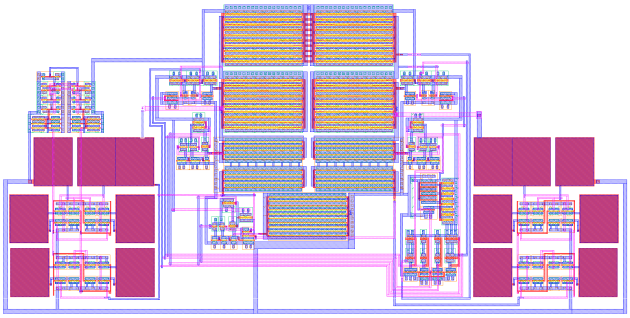

Fig. 15. Layout of SC circuit

These last two plots show the deficiencies of the opamp in simulation. With a 10MHz signal fed into the amplifier, the output common mode level of the opamp hit the top rail. This was not seen in the OP amp only simulation, so was hard to correct for after designing the op amp. The railing of the output causes the circuit to fail to output any signal (last plot). This would be fixed by implementing better common mode feedback, particularly on the output, however I didn't have time for this.

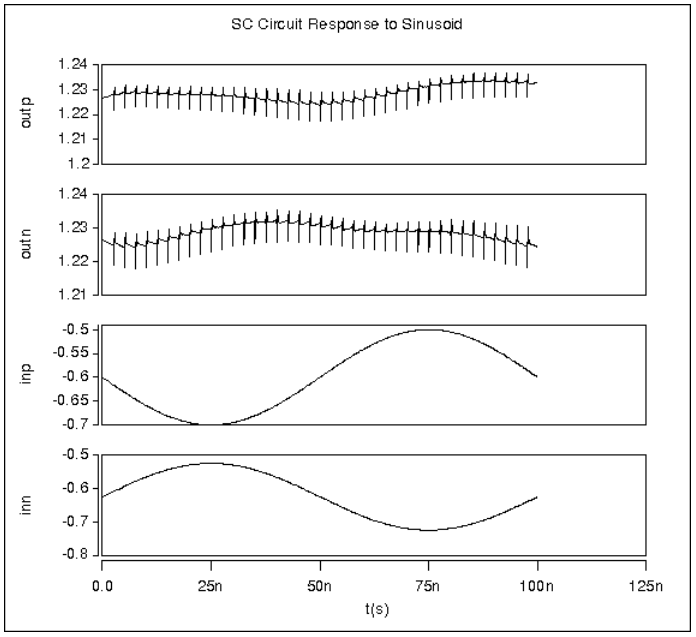

Fig. 16. SC circuit simulation output at opamp output nodes

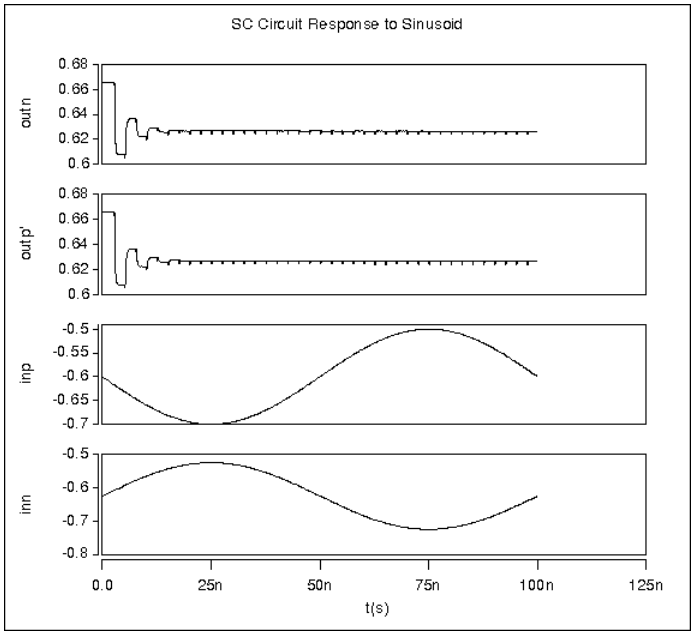

Fig. 17. Time Domain Simulation of SC Circuit

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