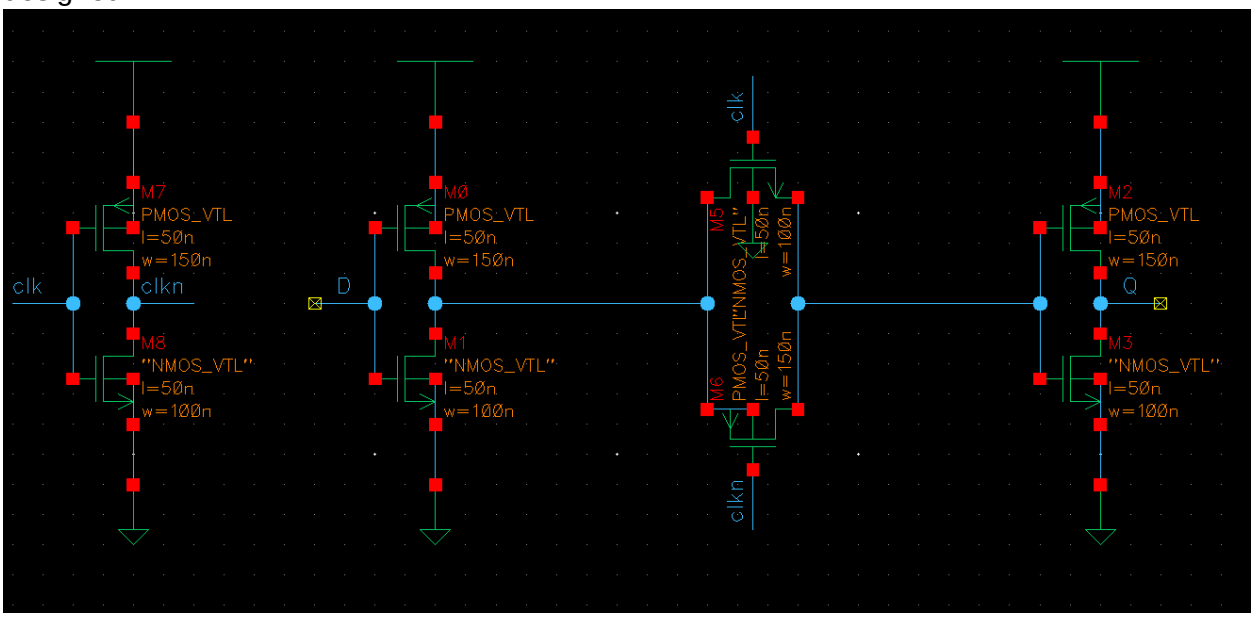
Standard Latch

I designed a standard latch to have minimal device dimensions while maintaining a PMOS to NMOS ratio of 1.5 for speed. Below is the schematic for the standard latch, containing an input and output inverters to achieve a non-inverter output while maintaining ability for reasonable fan out. An inverter is also used for the complementary clock generation. Below is the circuit designed.

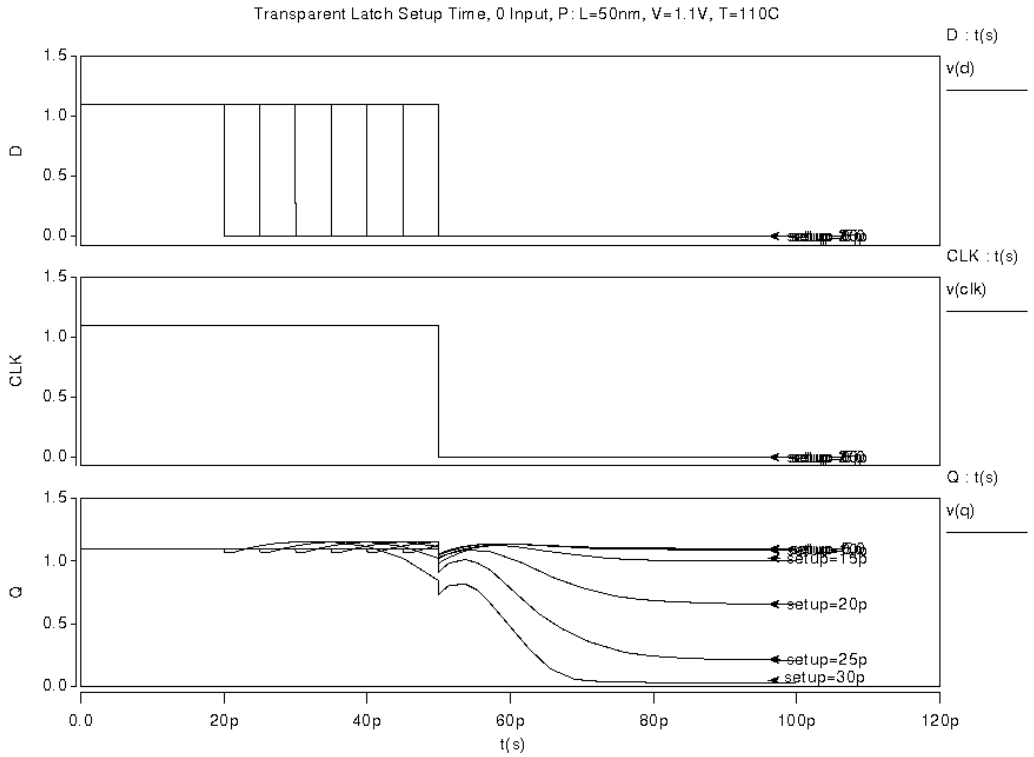


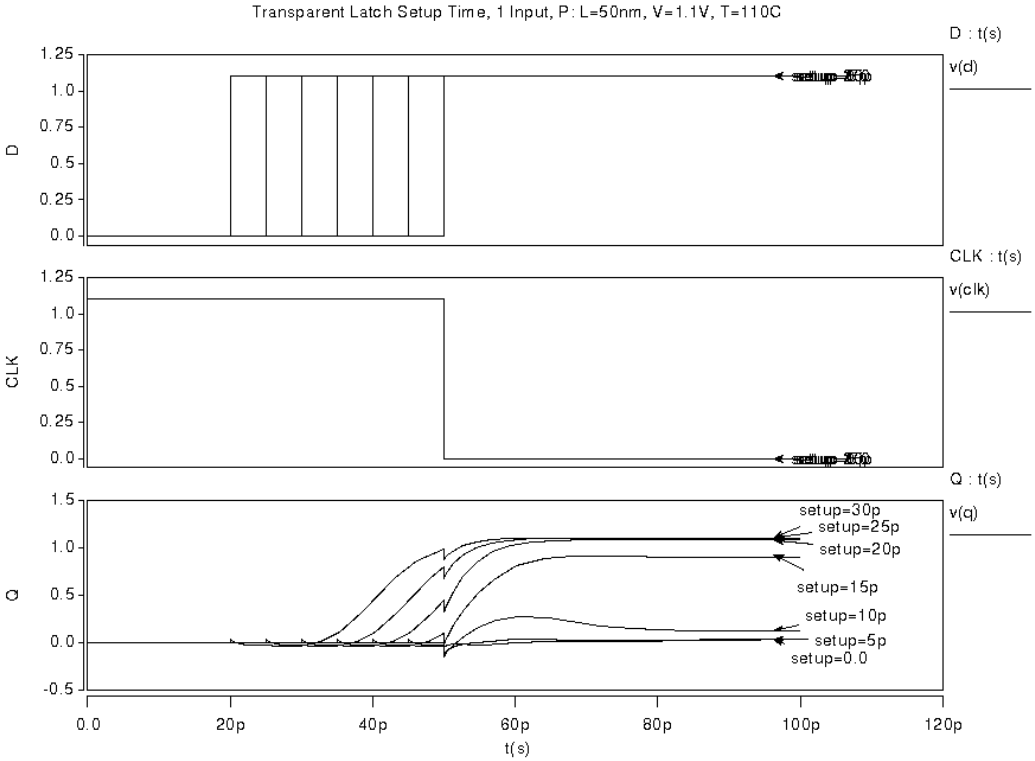
This circuit works by using a transmission gate to pass a signal when the clock in gating the latch, and when the clock is inactive the transmission gate becomes a high impedance, trapping charge on the output inverter's gate, thus storing a bit of data until leakage corrupts the state. Note this latch is fully transparent, so only the state that is presented at the end of the active clock period will be retained, if held for a long enough set up time.

The setup time for this latch was found by running several transient simulations where the data input was toggled to the desired value to be stored (for both 1/0) for several different time periods before the negative transition of the clock (active to inactive or transparent to opaque). The minimum time period that a signal needed to be asserted in order for a state to be properly retained after clock change was taken to be the setup time. The measured setup times for the latch were approximately:

Latch 0 setup : 20ps

Latch 1 setup : 30ps

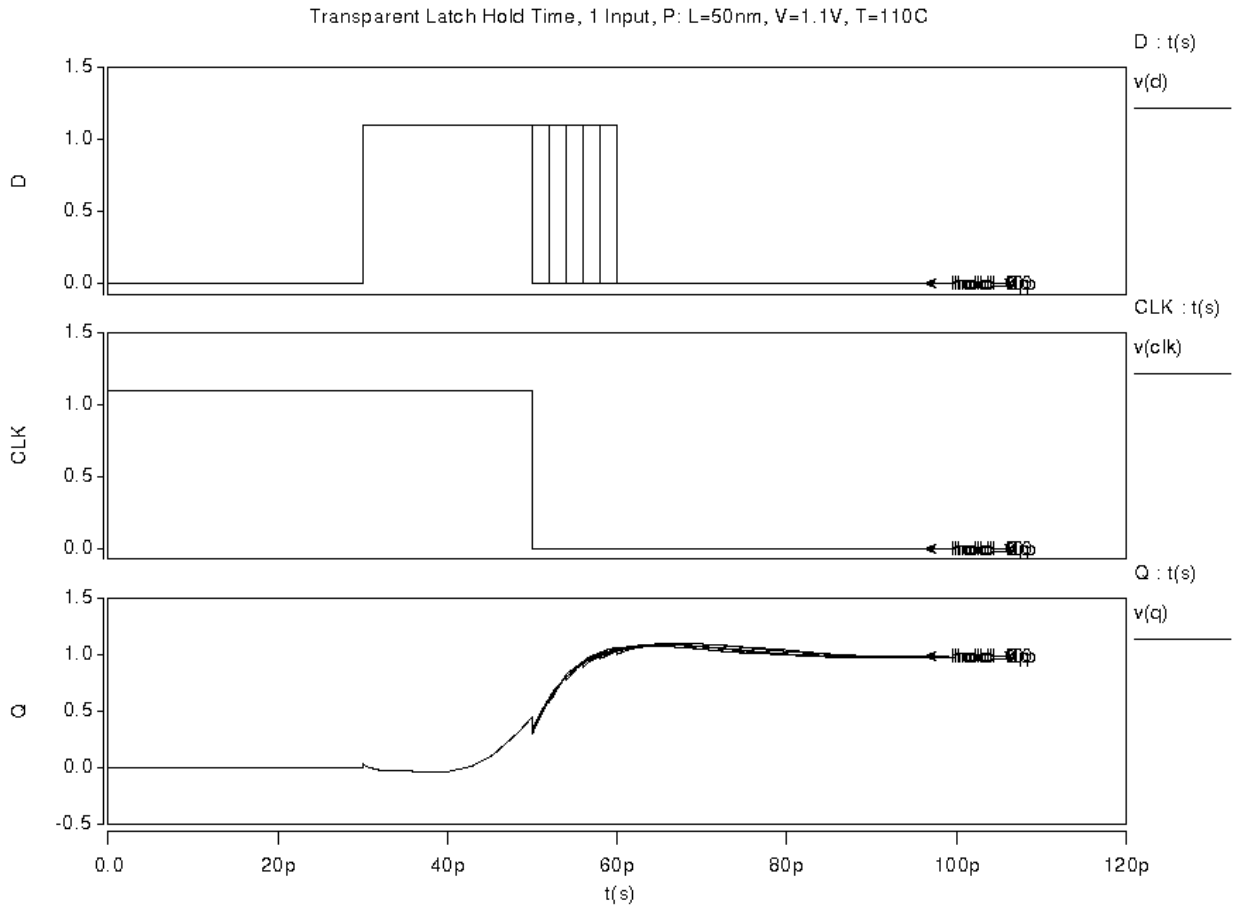

Transparent Latch Setup Time, 0 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Q : t(s)
v(q)
D
CLK
Q
1.5
1.0
0.5
0.0
setup=15p
setup=20p
setup=25p
setup=30p
0.0
20p
40p
60p
80p
100p
120p
t(s)

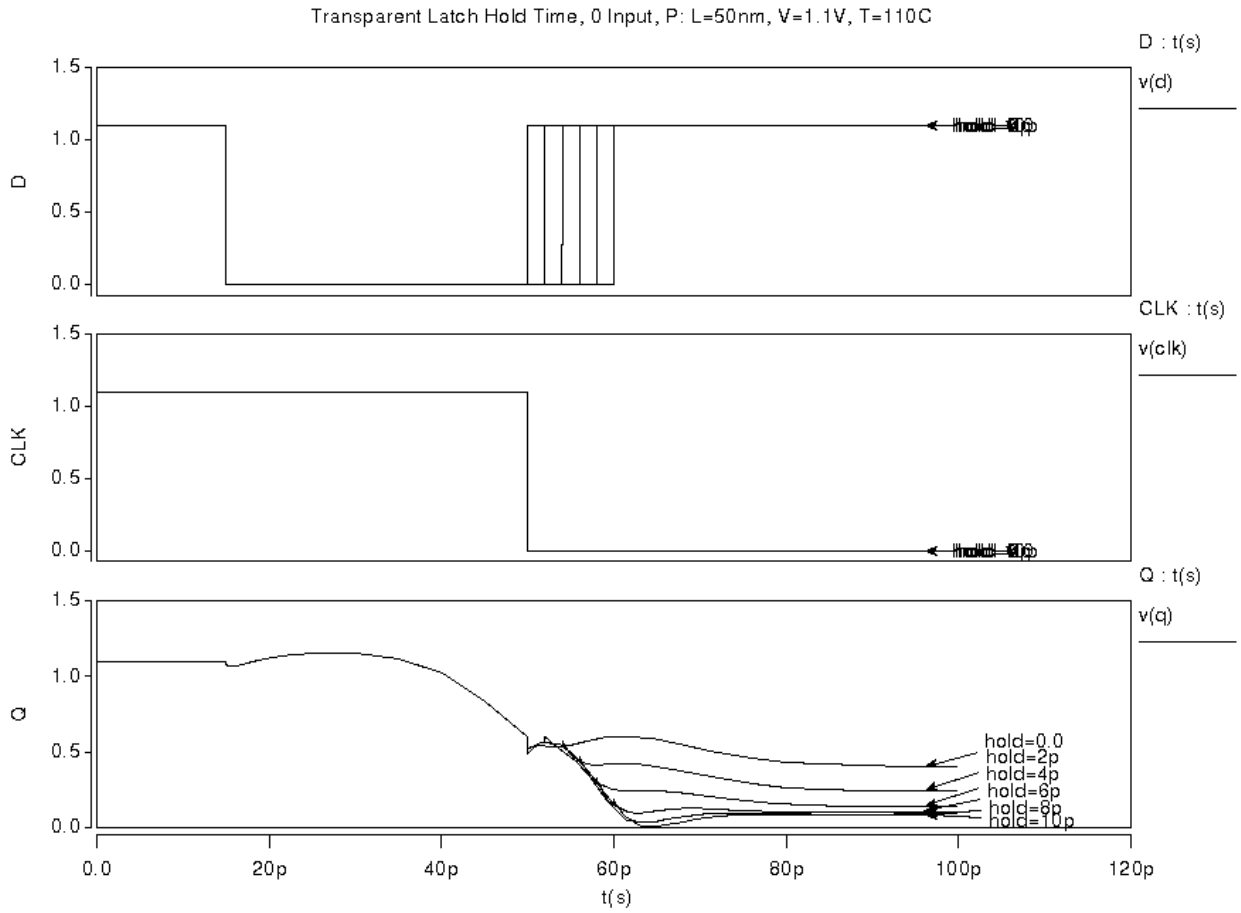

Transparent Latch Setup Time, 1 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Q : t(s)
v(q)
D
CLK
Q
1.25
1.0
0.75
0.5
0.25
0.0
-0.5
setup=30p
setup=25p
setup=20p
setup=15p
setup=10p
setup=5p
setup=0.0
0.0
20p
40p
60p
80p
100p
120p
t(s)

The hold time was found by asserting the desired data signal at the input of the flip flop for the minimal setup time, and then running several transient simulations with varying hold times after the high-low clock transition. The minimal seen time after the clock transition needed to retain a proper state was determined to be the hold time. The determined values for latch hold time were:

Latch 0 hold : 6ps

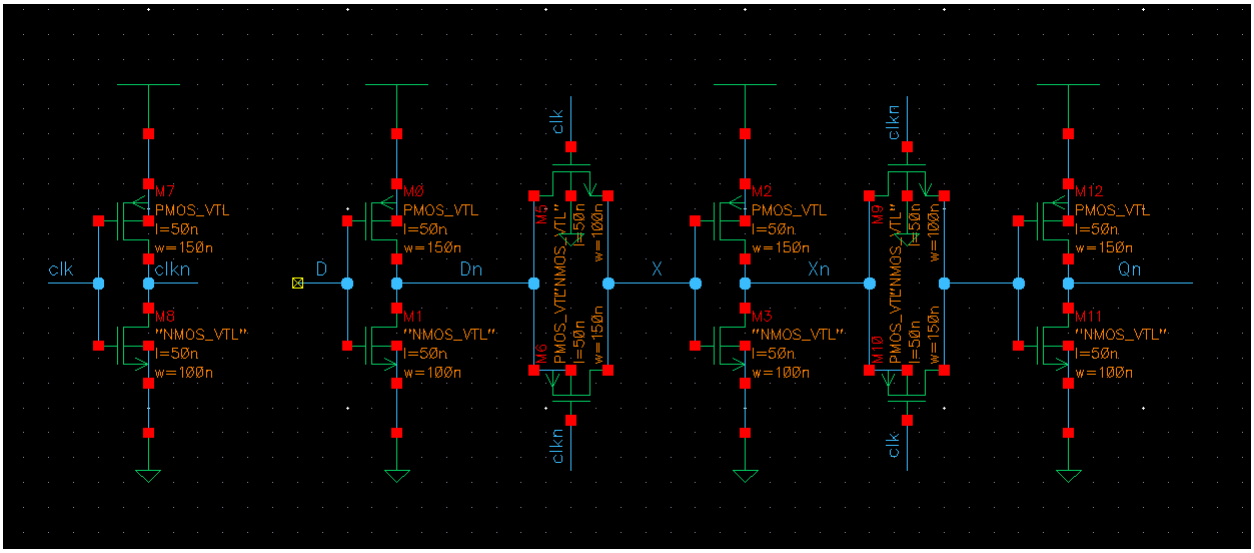
Latch 1 hold : 0ps




Transparent Latch Hold Time, 0 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Q : t(s)
v(q)
D
CLK
Q
1.5
1.0
0.5
0.0
hold=0.0
hold=2p
hold=4p
hold=6p
hold=8p
hold=10p
0.0
20p
40p
60p
80p
100p
120p
t(s)

Standard Flip-Flop

The standard flip flop is similar to the previous latch, except another transmission gate with flipped clocks and another inverter are added after the original latch design. This is shown as follows:



This design works by the input latch portion retaining a state up to the falling edge of the clock, and then the next stage immediately transferring that state to the output inverters gate as the second transmission gate goes active (opposite of the first trans. gate), without being affected by any further changes to the FF input. This makes the FF opaque, that it is only sensitive to change just at the clock transition where the state is transferred from the first to second latch. Setup and hold times were measured using the same method for the latch, the recorded values are shown below:

Latch 0 setup: 30ps

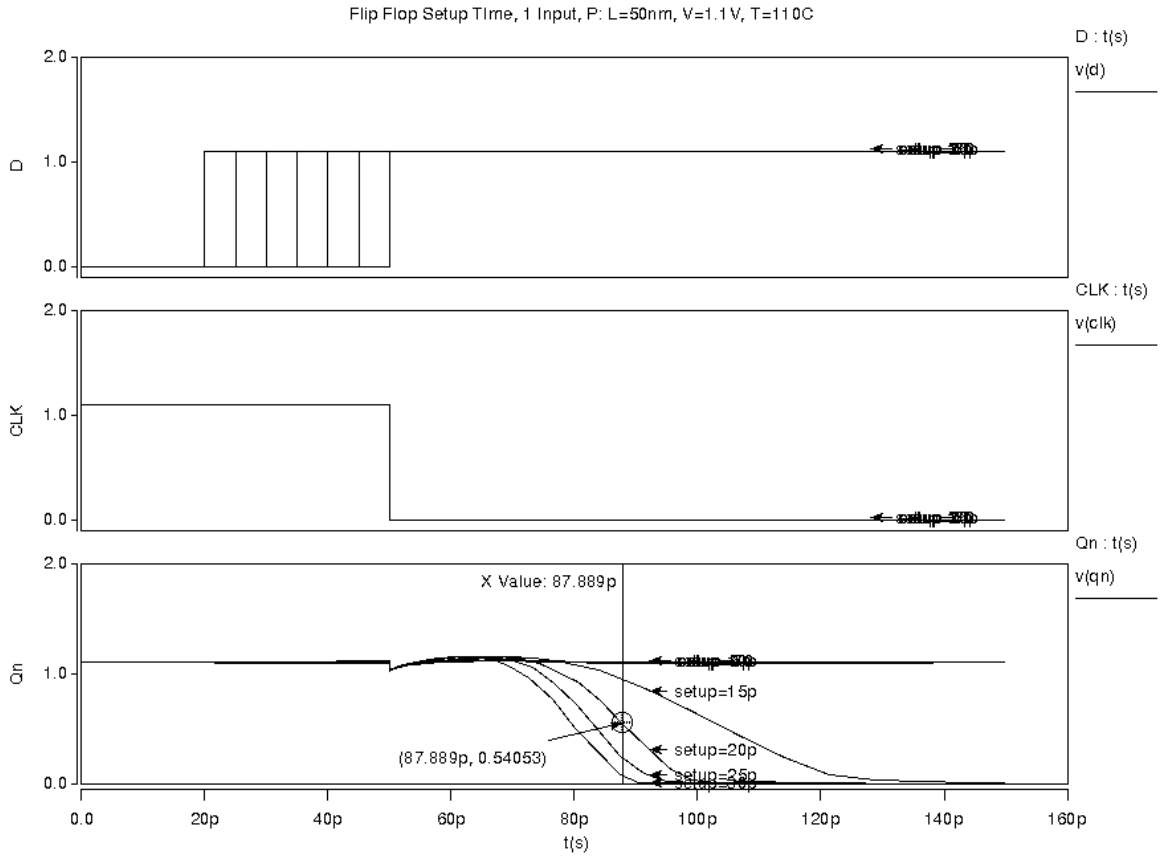
Latch 1 setup : 20ps

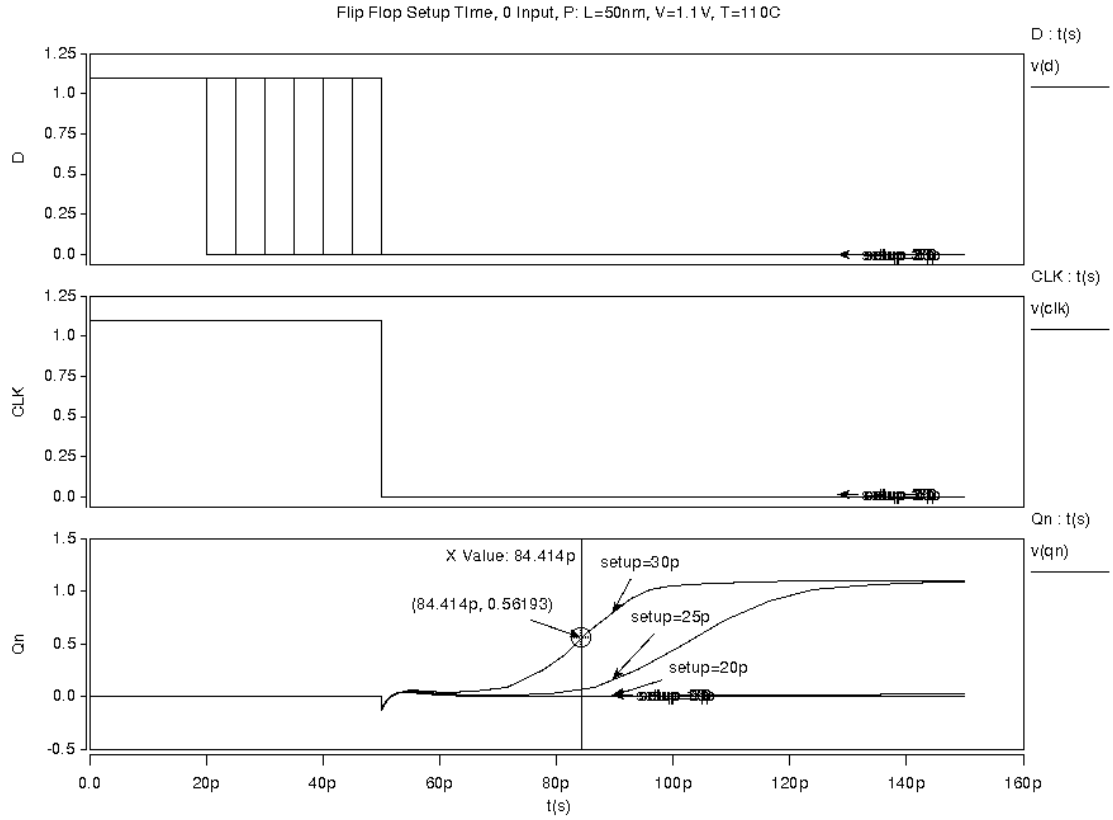
Latch 0 hold : 6ps

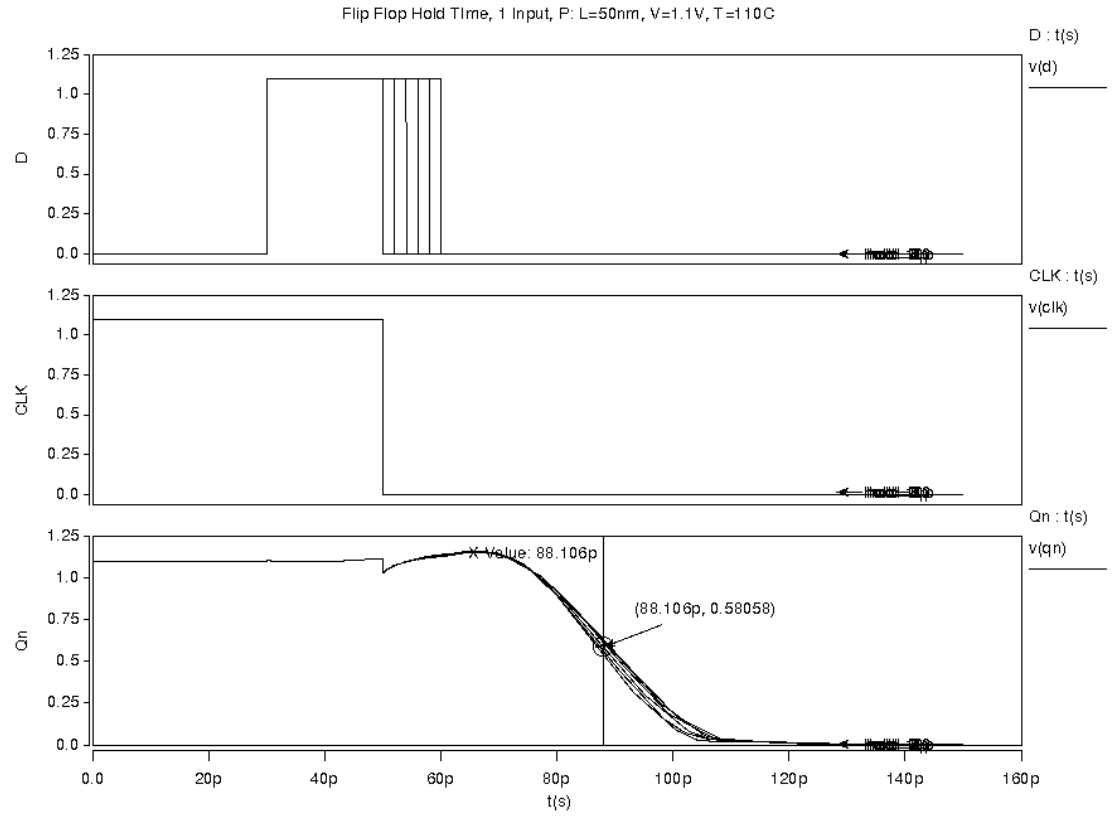
Latch 1 hold : 0ps

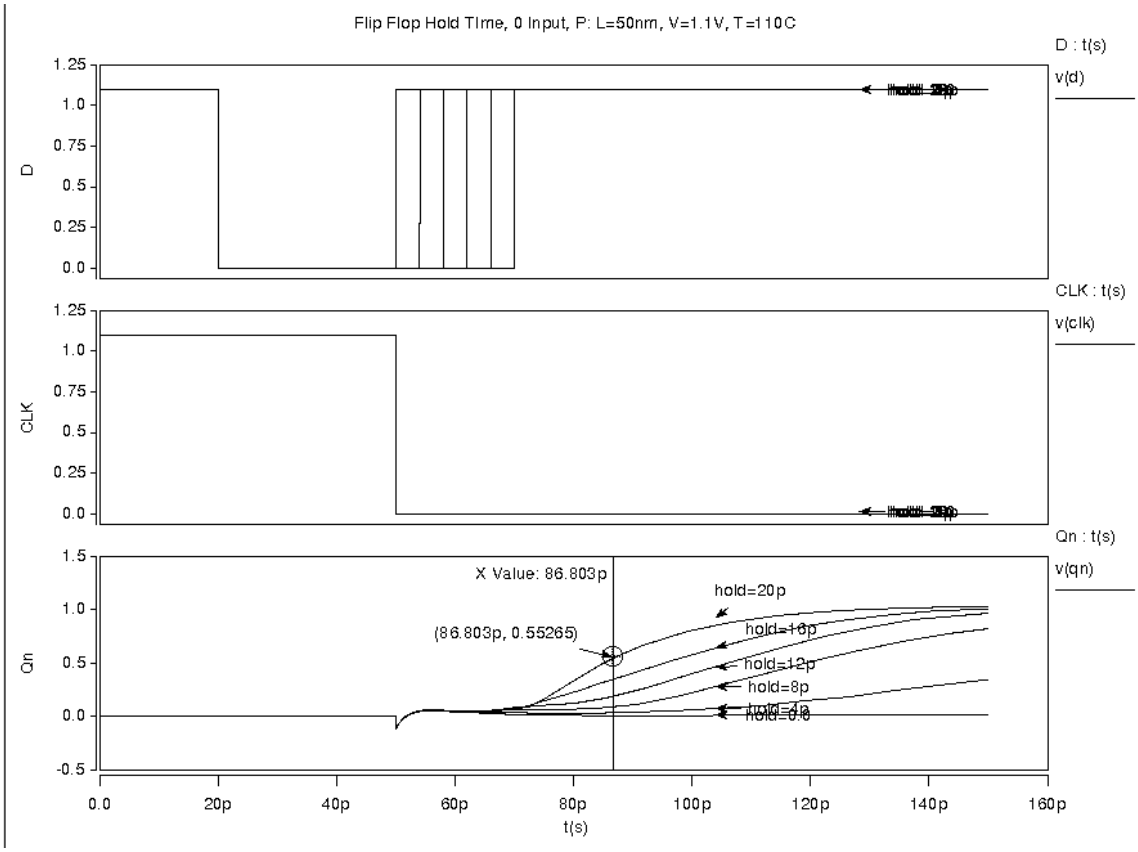
CLK to Q delay, 1 input: 0ps

CLK to Q delay, 0 input : 20ps


Flip Flop Setup TIme, 1 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Qn : t(s)
v(qn)
D
CLK
Qn
2.0
1.0
0.0
X Value: 87.889p
setup=15p
setup=20p
setup=25p
(87.889p, 0.54053)
0.0
20p
40p
60p
80p
100p
120p
140p
160p
t(s)


Flip Flop Setup TIme, 0 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Qn : t(s)
v(qn)
D
CLK
Qn
1.25
1.0
0.75
0.5
0.25
0.0
1.5
-0.5
X Value: 84.414p
setup=30p
(84.414p, 0.56193)
setup=25p
setup=20p
0.0
20p
40p
60p
80p
100p
120p
140p
160p
t(s)


Flip Flop Hold TIme, 1 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Qn : t(s)
v(qn)
D
CLK
Qn
X Value: 88.106p
(88.106p, 0.58058)
1.25
1.0
0.75
0.5
0.25
0.0
0.0
20p
40p
60p
80p
100p
120p
140p
160p
t(s)


Flip Flop Hold TIme, 0 Input, P: L=50nm, V=1.1V, T=110C
D : t(s)
v(d)
CLK : t(s)
v(clk)
Qn : t(s)
v(qn)
D
CLK
Qn
X Value: 86.803p
(86.803p, 0.55265)
hold=20p
hold=16p
hold=12p
hold=8p
hold=4p
hold=0.0
1.5
1.25
1.0
0.75
0.5
0.25
0.0
-0.5
0.0
20p
40p
60p
80p
100p
120p
140p
160p
t(s)