CHAPTER 19

19.1

(a) True

(b) (i) Severely distorted I_D–V_D characteristics. (Curves fail to saturate and $I_D \propto V_D^2$ curves observed for gate voltages below threshold.)

(ii) Subthreshold transfer characteristics which vary with V_D.

(iii) A threshold voltage which is a function of the gate dimensions and the applied biases.

(c) *differ* ...$|V_T|$ decreases with L but increases with Z.

alike ...Both effects have a similar cause; the gate charge required to achieve the threshold point changes because of the increasing importance of channel-edge charges.

(d) As noted in Subsection 19.1.1, L_{min} can be made smaller, and hence small-dimension effects minimized, by reducing the depth of the source/drain islands and by increasing the substrate doping.

(e) (i) punch-through

(ii) carrier multiplication and regenerative feedback

(f) In the vicinity of the drain under operational conditions, channel carriers, and carriers entering the drain depletion region from the substrate, periodically gain a sufficient amount of energy to surmount the Si–SiO_2 surface barrier and enter the oxide. Neutral centers in the oxide trap a portion of the injected charge and thereby cause a charge build-up within the oxide.

(g) Primarily because a larger percentage of the gated region is affected in the smaller devices. (However, the oxide charging is made worse by the common practice of using bias voltages that have not been scaled down in proportion to the device dimensions.)

(h) First, I_{Dsat} for a given V_G is significantly reduced. Second, the saturation current exhibits an almost linear dependence on V_G–V_T as opposed to the conventional square-law dependence.

(i) *ballistic transport* — the projectile-like motion of carriers through a semiconductor region where there is very little or no scattering.

(j) *velocity overshoot* — an average carrier velocity greater than v_{sat}.

(k) A lightly doped drain (LDD) region is introduced between the end of the channel and the drain proper.

(l) With a material lattice constant different than that of the underlying substrate, a pseudomorphic film is a thin layer of the material (typically $\lesssim$ 1000Å) that conforms to the lattice pattern of the substrate.

(m) (i) The SiGe enhanced-mobility MOSFET picture in Fig. 19.12 contains a strained pseudomorphic Si film that conforms to the larger lattice constant of the underlying $Si_{0.7}Ge_{0.3}$ layer.

(ii) The pseudomorphic MODFET or PHEMT pictured in Fig. 19.15 contains a pseudomorphic $In_xGa_{1-x}As$ layer positioned between the AlGaAs and GaAs.

(n) A high dose of oxygen is implanted into a silicon wafer and the wafer subsequently annealed to produce an oxide layer beneath the top surface of the wafer. An SOI layer is thereby created. (See Fig. 19.13.)

(o) There is no difference. MODFET and HEMT are just two different names for the same device.

19.2

LDD...*l*ightly *d*oped *d*rain

DMOS...*d*ouble-diffused *m*etal *o*xide *s*emiconductor

SOI...*s*ilicon *o*n *i*nsulator

SOS...*s*ilicon *o*n *s*apphire

ELO...*e*pitaxial *l*ayer *o*vergrowth

SIMOX...*s*eparation by *im*plantation of *ox*ygen

BESOI...*b*onded *s*ilicon *o*n *i*nsulator

BOX...*b*uried *o*xide *l*ayer

MODFET...*mo*dulation *d*oped *f*ield *e*ffect *t*ransistor

PHEMT...*p*seudomorphic *h*igh *e*lectron *m*obility *t*ransistor

19.3

(a) Given... $x_o = 0.028\mu m = 280\text{Å}$, $r_j = 1\mu m$, and

$$W = \left[\frac{2K_S\varepsilon_0}{qN_A}(V_{bi} - V_A)\right]^{1/2} \quad \text{with } V_{bi} = 0.915V \text{ (read from Fig. E5.1)}$$

$V_A \Rightarrow 0$ source junction

$V_A \Rightarrow -V_D = 0.125V$ drain junction

$$W_S = \left[\frac{(2)(11.8)(8.85\times10^{-14})}{(1.6\times10^{-19})(8\times10^{15})}(0.915)\right]^{1/2} = 0.386\mu m$$

$$W_D = \left[\frac{(2)(11.8)(8.85\times10^{-14})}{(1.6\times10^{-19})(8\times10^{15})}(0.915 + 0.125)\right]^{1/2} = 0.412\mu m$$

$$L_{min} = 0.4\left[r_j x_o (W_S + W_D)^2\right]^{1/3} = 0.4\left[(1)(280)(0.386+0.412)^2\right]^{1/3} = \mathbf{2.25\mu m}$$

The calculated L_{min} is right on target. The $V_D = 0.125V$ data in Fig. 19.3 show a significant change in the threshold voltage for $L \lesssim 2\mu m$. [It should be noted that $W_D = 0.896\mu m$ and $L_{min} = 3.09\mu m$ if one employs $V_D = 4V$. This L_{min} for $V_D = 4V$ appears to be decidedly too low. The V_D dependence noted in Fig. 19.3 is much stronger than that expected from the L_{min} dependence.]

(b) $\phi_F = (kT/q)\ln(N_A/n_i) = 0.0259\ln(8\times10^{15}/10^{10}) = 0.352V$

$$W_T = \left[\frac{2K_S\varepsilon_0}{qN_A}(2\phi_F)\right]^{1/2} = \left[\frac{(2)(11.8)(8.85\times10^{-14})}{(1.6\times10^{-19})(8\times10^{15})}(2)(0.352)\right]^{1/2} = 0.339\mu m$$

$$\Delta V_T = -\frac{qN_A W_T}{K_O\varepsilon_0} x_o \frac{r_j}{L}\left(\sqrt{1 + \frac{2W_T}{r_j}} - 1\right)$$

$$= -\frac{(1.6\times10^{-19})(8\times10^{15})(3.39\times10^{-5})(2.8\times10^{-6})(10^{-4})}{(3.9)(8.85\times10^{-14})(10^{-4})}\left\{\left[1 + \frac{(2)(0.339)}{1}\right]^{1/2} - 1\right\}$$

$$= \mathbf{-0.104V}$$

The computed result here is very close to the observed $\Delta V_T \cong -0.13V$.

(c) No...The Eq.(19.13) result is derived assuming $V_D \cong 0$.

19.4

(a) A lightly doped drain region (n^- versus n^+ of the drain proper) which lies between the end of the channel and the drain proper.

(b) A short channel length (~1μm) formed by the difference in the lateral distances diffused by two impurities. The short channel length can be achieved without using small-dimension lithographic masks.

(c) A surface layer beneath the gate with the same doping as the drain and source islands.

(d) The channel region of the MOSFET is a strained pseudomorphic Si layer with a higher carrier mobility than equivalently-doped bulk Si.

(e) Si device layers formed *over* an insulating film or substrate.