Lab 1 Report

EE 4111

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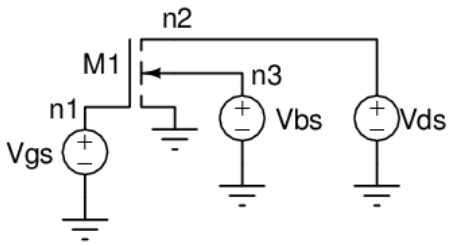
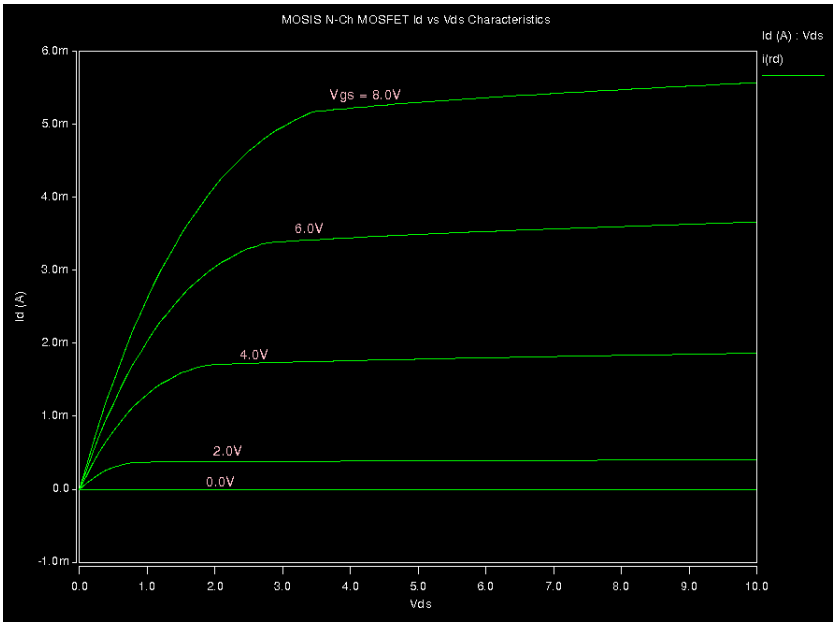
Task 2

The objective of this task was to make a family of I-V characteritic curves for the given MOSFET model. Below is the circuit used with labeled nodes. Underneath the circuit schematic is the netlist for this circuit (body effect is ignored for this part). The family of I-V curves were generated by sweeping the drain-to-source voltage (Vds) for five different gate to source voltages (Vgs), done with the .DC directive. The output was plotted in Cosmoscope.




```
mosfet i-v curve
.OPTIONS LIST NODE POST
.DC Vds 0V 10V 100mV Vgs 0 8V 2V
.PRINT DC V(3) I1(M1)

Vgs 1 0 DC 3
Vds 2 0 DC 1
M1 2 1 0 0 CMOSN W = 10U L = 1.5U

.MODEL CMOSN NMOS ( LEVEL = 3
+ TOX = 1.4E-8 NSUB  = 1E17 GAMMA = 0.5483559
+ PHI = 0.7 VTO = 0.7640855 DELTA = 3.0541177
+ UO = 662.6984452 ETA = 3.162045E-6 THETA = 0.1013999
+ KP  = 1.259355E-4 VMAX = 1.442228E5 KAPPA = 0.3
+ RSH = 7.513418E-3 NFS = 1E12   TPG   = 1
+ XJ    = 3E-7 LD  = 1E-13 WD = 2.334779E-7
+ CGD = 2.15E-10 CGSO = 2.15E-10 CGBO  = 1E-10
+ C = 4.258447E-4 PB = 0.914037 MJ    = 0.435903
+ CJSW  = 3.147465E-10  MJSW  = 0.1977689     )

.END
```

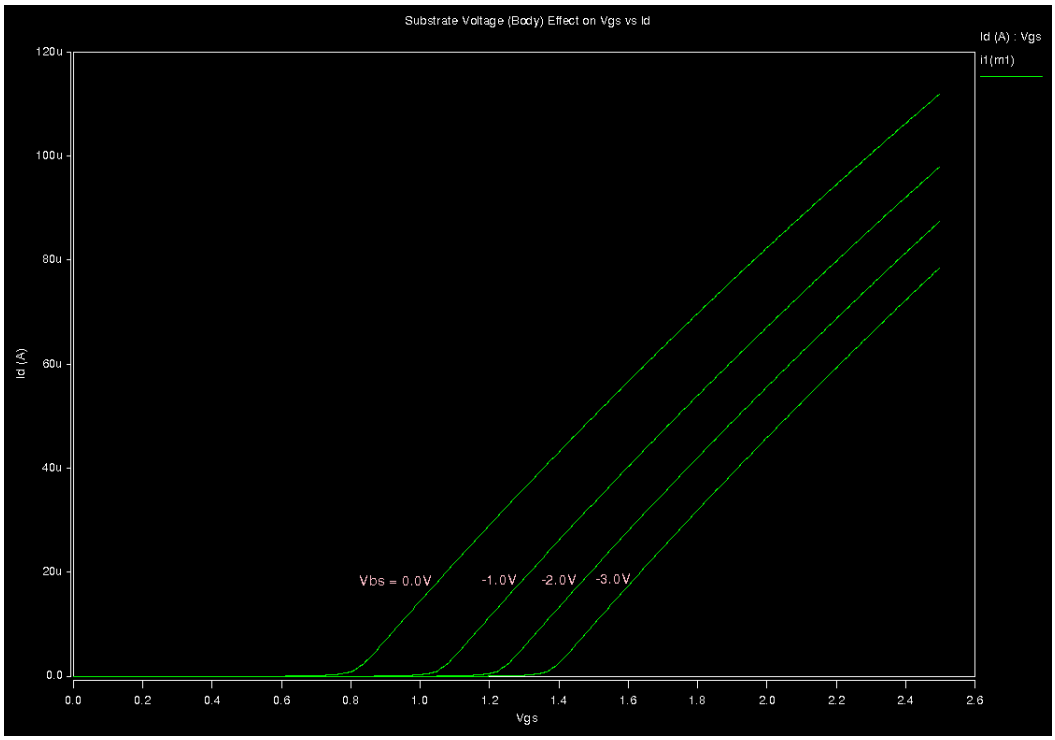
In the following plot notice the parabolic ($\propto V_{ov}^2$) growth of I_d, as well as the Early effect causing the saturation region to have a slope.



The second part of this task was to investigate how the body effect (gamma parameter) affects the I-V characteristic of a MOSFET. This was done by modififying the netlist to include a body to source voltage (Vbs) and then keeping Vds constant while sweeping Vbs. The body to source voltage is always kept at a negative potential to ground, as reversing the polarity would forward bias the source body junction.

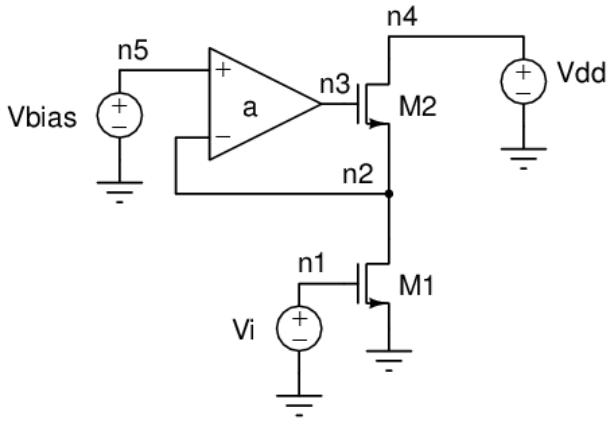
```
mosfet i-v curve
.OPTIONS LIST NODE POST
.DC Vgs 0V 2.5V 5mV Vbs 0 -3V 1V
.PRINT DC V(1) I1(M1)

Vgs 1 0 DC 3V
Vds 2 0 DC 0.1V
Vbs 3 0 DC 1V
M1 2 1 0 3 CMOSN W = 10U L = 1.5U

.MODEL CMOSN NMOS ( LEVEL = 3
+ TOX = 1.4E-8 NSUB  = 1E17 GAMMA = 0.5483559
+ PHI = 0.7 VTO = 0.7640855 DELTA = 3.0541177
+ UO = 662.6984452 ETA = 3.162045E-6 THETA = 0.1013999
+ KP  = 1.259355E-4 VMAX = 1.442228E5 KAPPA = 0.3
+ RSH = 7.513418E-3 NFS = 1E12    TPG    = 1
+ XJ    = 3E-7 LD  = 1E-13 WD = 2.334779E-7
+ CGD = 2.15E-10 CGSO = 2.15E-10 CGBO  = 1E-10
+ C = 4.258447E-4 PB = 0.914037 MJ    = 0.435903
+ CJSW  = 3.147465E-10  MJSW  = 0.1977689     )

.END
```

It should be noted that the body effect (gamma) affects the Id-Vgs characteristic by increasing the Vgs needed for a current with a greater Vbs. This is an important parameter to understand and to design for when designing microelectronics as it has a large impact on circuit behavior.



Task 3

The objective of this task was to create a netlist for the active cascode circuit of figure 3.41 in Grey and Meyer. The circuit is designed have Vbias and Vi set such that the drain current is approximately 500μA. The bodies of both transistors are connected to ground, and the OP AMP feedback amplifier is modeled by an ideal amplifier. The current was set to 500μA by approximately calculating the V_{ov} using $V_{ov} = \frac{1}{2}\text{KP} \times V_{ov}^2$, and then setting Vbias to that voltage. Vi was set to Vto plus Vov. This was then simulated using an DC operating point simulation. The values of Vbias and Vi were then tweaked for the drain current to be closer to 500μA. As follows is the circuit diagram and netlist.




```
active cascode
.OPTIONS LIST NODE POST
.OP
.PRINT DC V(n1) V(n4) I1(M2)

Vdd n4 0 DC 8V
Vbias n5 0 DC 1.6V
Vi n1 0 DC 2.25V
M1 n2 n1 0 0 CMOSN W = 10U L = 1.5U
M2 n4 n3 n2 0 CMOSN W = 10U L = 1.5U
Eopamp n3 0 OPAMP n5 n2

.MODEL CMOSN NMOS ( LEVEL = 3
+ TOX = 1.4E-8 NSUB  = 1E17 GAMMA = 0.5483559
+ PHI = 0.7 VTO = 0.7640855 DELTA = 3.0541177
+ UO = 662.6984452 ETA = 3.162045E-6 THETA = 0.1013999
+ KP  = 1.259355E-4 VMAX = 1.442228E5 KAPPA = 0.3
+ RSH = 7.513418E-3 NFS = 1E12    TPG    = 1
+ XJ    = 3E-7 LD  = 1E-13 WD = 2.334779E-7
+ CGD = 2.15E-10 CGSO = 2.15E-10  CGBO   = 1E-10
+ C = 4.258447E-4 PB = 0.914037 MJ    = 0.435903
+ CJSW  = 3.147465E-10  MJSW  = 0.1977689     )

.END
```

Below is the data from the output listing file of the DC operaing point of the two MOSFETS. The drain currents are both close to 500 μA and both devices are in saturation.

```
 subckt
 element 0:m1      0:m2
 model   0:cmosn   0:cmosn
 region    Saturati  Saturati
  id      508.1523u 503.0331u
```

```
ibs       0.       -16.0000f
ibd     -16.0000f -80.0000f
vgs       2.2500    2.5078
vds       1.6000    6.4000
vbs       0.       -1.6000
vth     750.7243m   1.1050
vdsat     1.0655    1.0611
vod       1.4993    1.4028
beta    541.3695u 545.4733u
gam eff 514.7031m 495.2495m
gm      561.4416u 601.1679u
gds       7.6704u   4.2889u
gmb       0.       95.8735u
cdtot     2.2252f   2.4510f
cgtot    28.1535f  28.3405f
cstot    25.6637f  25.6637f
cbtot   264.6000a 225.9071a
cgs      25.6637f  25.6637f
cgd       2.2252f   2.4510f
```

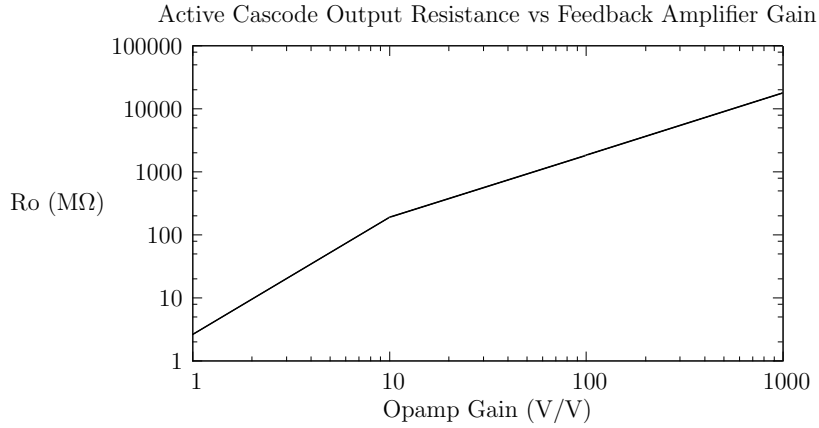
Task 4

Task 4 uses the same netlist as Task 3, however modified to have an adjustable gain. The objective of this part is to find the output resistance looking into the drain of M2. Since this is a cascode configuration, the output inpedence should be extremely high, especially if the drain to source voltage of M1 is held constant across M1 due to the feedback amplifier and Vi is held constant. Holding these voltages constant effectively negate the Early effect for M1, which essentially elimates the r_o term for that transistor in the small signal domain. It is expected that the high gain the opamp has, the better the Vds of M2 will stay constant, and the higher the output resistance will be. The output resistance was found by adding a AC voltage to the the supply voltage connected to the drain of M2. Running an AC simulation at a low frequency (to avoid capacitive effects) allows us to see the small signal current that flows into the active cascode, and the output resistance can therefore be calculated as the ration of the AC voltage to the AC current. Below is the netlist for this circuit.

```
active cascode
.OPTIONS LIST NODE POST
.PRINT AC V(n4) I1(M2) PAR('V(n4)/I1(M2)')
.AC DEC 1 10 100

Vdd n4 0 DC 8V AC 1 SIN (0 1 100)
Vbias n5 0 DC 1.6V
Vi n1 0 DC 2.25V
M1 n2 n1 0 0 CMOSN W = 10U L = 1.5U
M2 n4 n3 n2 0 CMOSN W = 10U L = 1.5U
```

```
E0 n3 0 n5 n2 1000

.MODEL CMOSN NMOS ( LEVEL = 3
+ TOX = 1.4E-8 NSUB  = 1E17 GAMMA = 0.5483559
+ PHI = 0.7 VTO = 0.7640855 DELTA = 3.0541177
+ UO = 662.6984452 ETA = 3.162045E-6 THETA = 0.1013999
+ KP  = 1.259355E-4 VMAX = 1.442228E5 KAPPA = 0.3
+ RSH = 7.513418E-3 NFS = 1E12    TPG    = 1
+ XJ    = 3E-7 LD  = 1E-13 WD = 2.334779E-7
+ CGD = 2.15E-10 CGSO = 2.15E-10 CGBO  = 1E-10
+ C = 4.258447E-4 PB = 0.914037 MJ    = 0.435903
+ CJSW  = 3.147465E-10  MJSW  = 0.1977689     )
*

.END
```

This circuit was simulated for feedback gain settings of 1, 10, 100 and 1000. Below are the results plotted in logscale. The impedence was extremely high as expected, topping off at 18 GΩ for $a = 1000$. As expected, output resistance grows with gain, almost exponentially. It should be noted that the active cascode was unable to mantain a drain current of 100μA with a gain setting of 1.

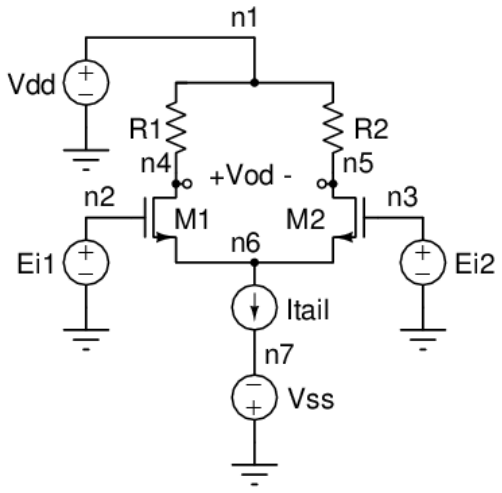


Below are the numerical values for gain extracted from the simulation output listing files:

a = 1	$R_o = 2.6399$ MΩ
a = 10	$R_o = 190.01$ MΩ
a = 100	$R_o = 1823.2$ MΩ
a = 1000	$R_o = 18132$ MΩ

Task 5

The objective of this part was to determine the linear input range of the below source coupled amplifier. The values for Rc and the supply voltages were adjusted to give a subjectively linear region between plus and minus 0.5 volts input differential. Itail was set to 200uA.




```
source coupled pair
.OPTIONS LIST NODE POST
.DC Vdiff -0.5 0.5 0.01 $differential voltage sweep
.PRINT DC PAR('V(n3)-V(n2)') PAR('V(n5) - V(n4)') I(Rd1) I(Rd2)

Vdd n1 0 DC 5
Vss 0 n7 DC 5
Vdiff n10 0 DC 0
Ei1 n2 0 VOL = '-1*V(n10)' $differential inputs
Ei2 n3 0 VOL = 'V(n10)'
Rd1 n1 n4 25000
Rd2 n1 n5 25000
M1 n4 n2 n6 n7 CMOSN W = 10U L = 1.5U
M2 n5 n3 n6 n7 CMOSN W = 10U L = 1.5U
Itail n6 n7 DC 200uA

.MODEL CMOSN NMOS ( LEVEL = 3
+ TOX = 1.4E-8 NSUB  = 1E17 GAMMA = 0.5483559
+ PHI = 0.7 VTO = 0.7640855 DELTA = 3.0541177
+ UO = 662.6984452 ETA = 3.162045E-6 THETA = 0.1013999
+ KP  = 1.259355E-4 VMAX = 1.442228E5 KAPPA = 0.3
+ RSH = 7.513418E-3 NFS = 1E12    TPG    = 1
+ XJ    = 3E-7 LD  = 1E-13 WD = 2.334779E-7
+ CGD = 2.15E-10 CGSO = 2.15E-10 CGBO  = 1E-10
+ C = 4.258447E-4 PB = 0.914037 MJ    = 0.435903
```

```
+ CJSW   = 3.147465E-10   MJSW   = 0.1977689      )
*

.END
```

This is the simulation output. We see fairly linear behavior for -0.5 to 0.5 volts as requested.