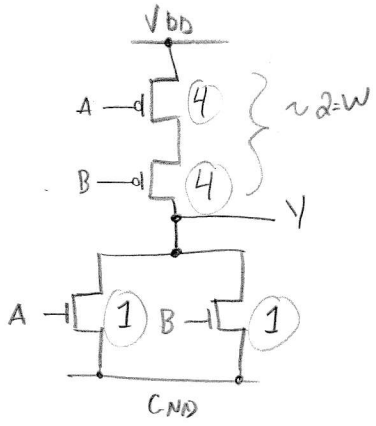
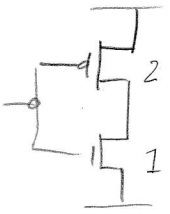
Cole Nielsen - 4971360 - EE 5323 HW No 5

1- 4.1)

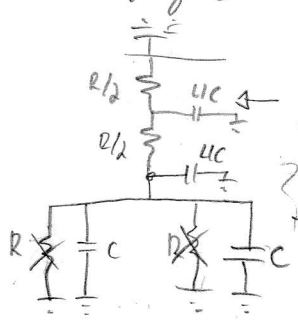


Same delay ⟷



* Alternatively top PMOS's W=3 for $\frac{W_p}{W_N} = 1.5$

capacitance: if $g=1$



Rising delay

$R/2 \cdot 4C$ ← self loading

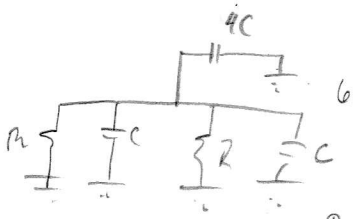
6C self loading, + each gate input is $4C + 1C = 5C$

So $t_{rise} = R/2 \cdot 4C + R(6C + 5Ch)$

$= 2RC + 6RC + 5RCh$

$= \boxed{8RC + 5RCh = T_{rise}}$

Falling =>



3C load per gate

$R_{PU} = R_2$

$t_{fall} = \frac{R}{2}(6C + 5Ch$

$\boxed{T_{fall} = (3RC + \frac{5}{2}RCh)}$

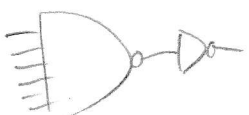
2 - 4.11) (a)

$G = \prod g_i$ NAND NOT

$G = (n+2)/3 \cdot 1 = (6+2)/3 \cdot 1 = \underline{8/3 = G}$

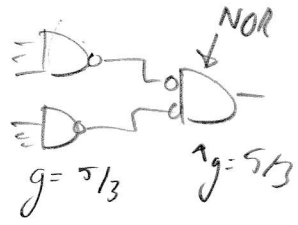
$\underline{N=2}$, $\underline{P = 6+1 = 7}$

$\Rightarrow D = N(GH)^{1/N}$,



$H = \frac{1}{\_} \quad \frac{5}{\_} \quad \frac{20}{\_}$

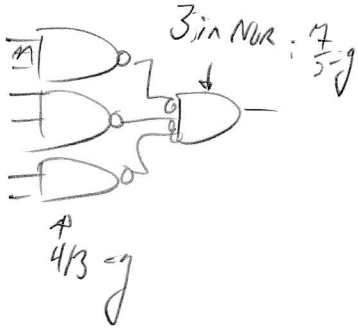
$D = 10.27 \quad 14.30 \quad 21.61$

b) 

$G = \frac{5}{3}\cdot\frac{5}{3} = \frac{25}{9} = 6$

$P = 3+2 = 5$ $\quad N = 2$

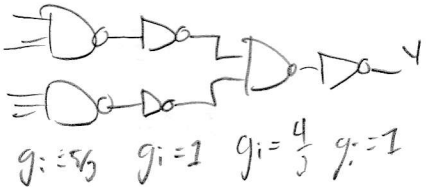
H =	1	5	20
D =	8.33	12.45	19.91

c) 

$Hg = \frac{7}{5}\cdot\frac{4}{3} = \frac{28}{9} = 6$

$P = 2+3$, $N = 2$

H =	1	5	20
D =	8.52	12.89	20.178

d) 

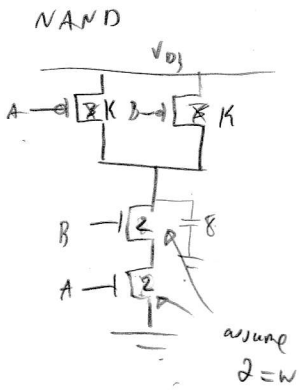
$Hg = \frac{5}{3}\cdot 1\cdot\frac{4}{3}\cdot 1 = \frac{20}{9}$

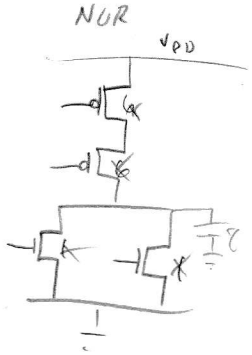
$P = 3+1+2+1 = 7$, $N = 2$

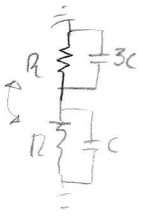
H = 1	5	20
D = 9.98	13.67	20.33

Design B is better for H = 1 & H = 5 as it has the lowest logical effort, design A is best for H = 20 as it has the lowest logical effort (probably due to long path allowing load to be spread/gradually increased)

3- 4.15

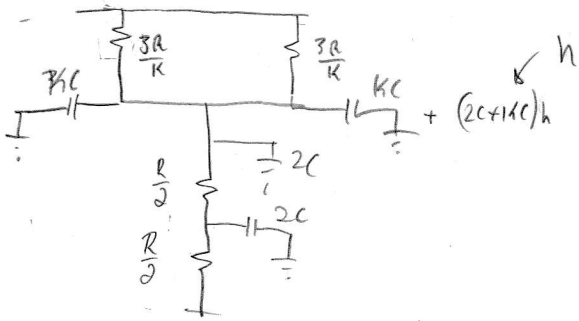




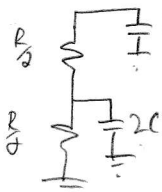


Fall = delay rise = $4RC + 4RCH$

$d = gh + p = \frac{C_{out}}{C_{in} g} + p$ =



Load

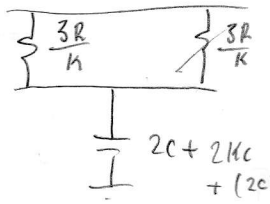


No Load $T_d = \frac{R}{2} 2C + R(2KC + 2C)$

$= RC + 2RCK + 2RC$

$= 3RC + 2RCK$

T_r



No load $t_r =$ $\frac{3R}{K}(2C + 2KC)$

$= \frac{6RC}{K} + 6RC$

$t_F = t_r$ (K.) $\left(\frac{6RC}{K} + 6RC\right) = (3RC + 2RCK)$ (K.)

$\Rightarrow 6RC + 6RC \cdot K = 3RC \cdot K + 2RCK^2$

$\Rightarrow 0 = 2RCK^2 - 3RC \cdot K - 6RC$

$0 = K^2 - \frac{3}{2}K - 3$ $\Rightarrow K = 2.64$ for equal delay

delay w/ load = $t = 3RC + 2RC \cdot 2.64 + (2C + \overset{2.064}{K}C)h$

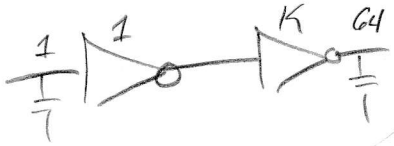
$= (8.28 + 4.64h)RC$

min $t_d = 4RC + 4rch$

$P = 2.07$, $g = 1.16$

4- 5.5) Minimum number of gates will consume lowest energy, or minimal capacitance will be created with min. gates;

so for a buffer this is 2 inverters = minimum



$g\left(\frac{C_{out}}{C_{in}}\right)$

effort

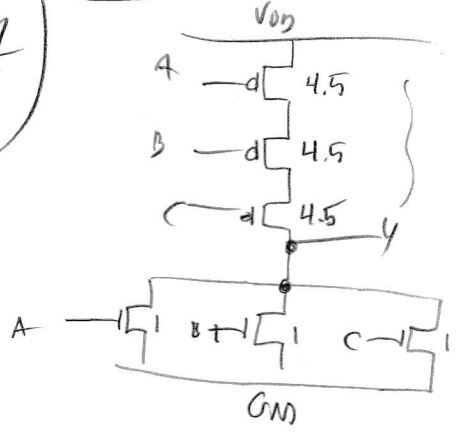
$$20 = d = gh + p = \left(K + \frac{64}{K}\right) + 2^{*}P$$

$$\Rightarrow 0 = K + \frac{64}{K} - 18 \Rightarrow 0 = K^2 - 19K + 64$$

K = 4.88 ← second

1 ← first (unit size)

5- 9.7) P: L=50nm V=1.1 T=110C



FROM HSPICE SIM

INPUT	G	P
A	2.895	4.19
B	2.519	4.19
C	1.85	2.69
Average	2.421	3.69

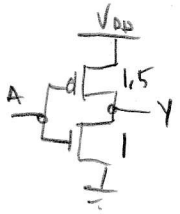
FROM BOOK
Ideal G = 7/3 = 2.33
Ideal P = 3

in A: τ_p unloaded = 11.94ps UNLoaded

t_{pOA} 17.343ps LOADED w/ 1 gate

$\rightarrow d = t_p = 11.94ps + 5.403h$

$P = \frac{11.94}{2.85} = 4.19 = P_A$, $\frac{5.403}{1.8658} = 2.895 = G_A$



$P_1 = 2.85ps$ (no load)

$d = t_d = P_1 + gh$

$4.7158 = 2.85 + g.1$

$g_i = 1.8658$

IN B: t_p unloaded = 11.95ps

t_p loaded = 16.65 ps (1 gate)

$d = \tau_p = 11.95 + 4.7h$

$P = \frac{11.95}{2.85} = 4.19 = P_B$, $\frac{4.7}{1.8658} = 2.519 = G_B$

INC t_p unloaded = 7.69ps

to loaded (1 gate) = 11.15ps

$d = \tau_p = 7.69 + 3.46h \Rightarrow$ $P_C = 2.69$ $G_C = 1.85$

CONCLUSION:

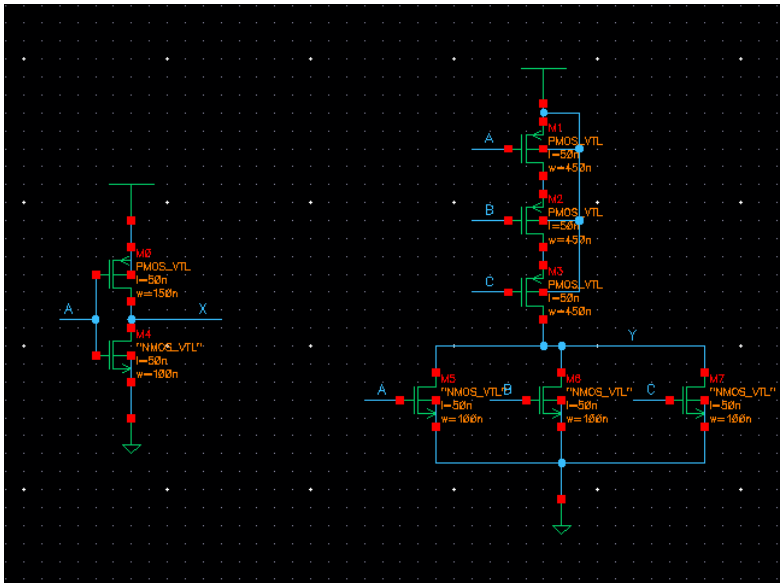
Average G = 2.421 close to ideal 7/3

Average P = 3.69 close to ideal 3

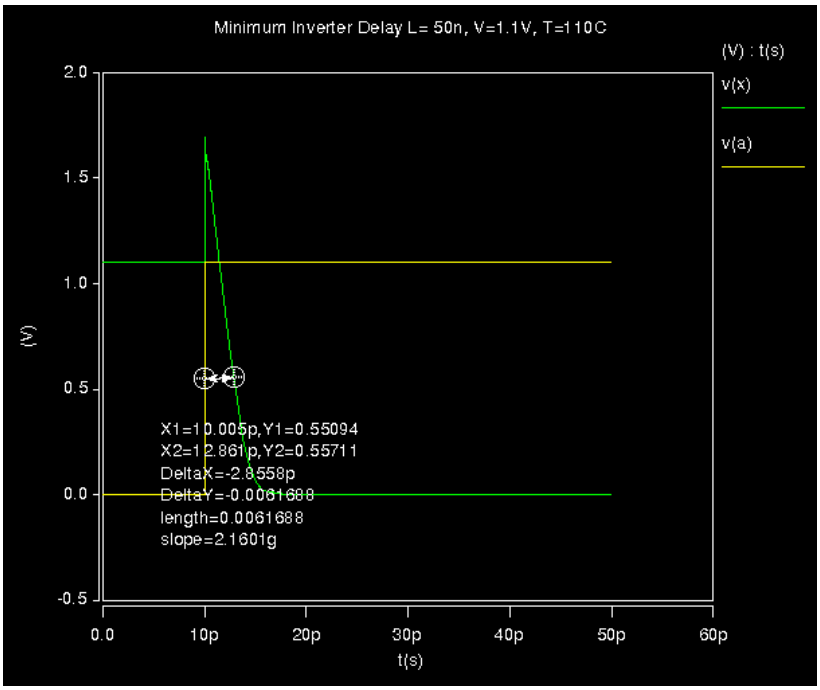
individual P/G

Problem 9.7)

To find the logical effort of a 3 IN NOR in FreePDK45, I made a HSPICE simulation with a minimal inverter where L=50nm and W=100nm for the NMOS and W=150nm for the PMOS. I also made a 3 in NOR gate that maintained the same overall ration of P width to Nwidth. This is shown below

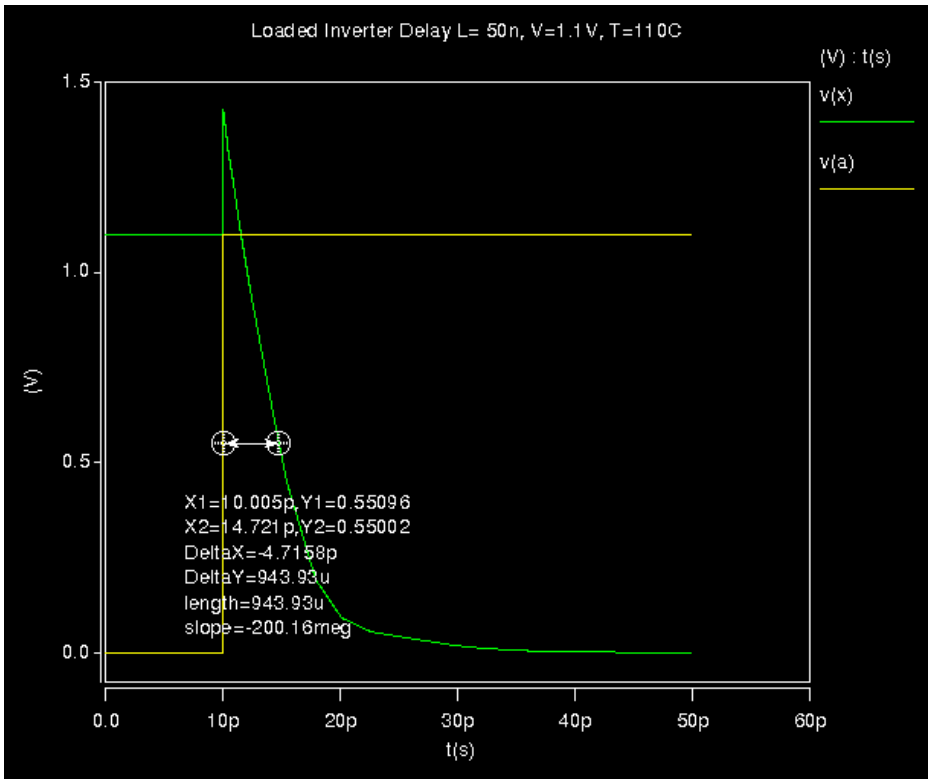


I then ran a simulation of the inverter (no loading) with T=110C and Vdd=1.1V to determine the minimal (intrinsic delay) for this process.

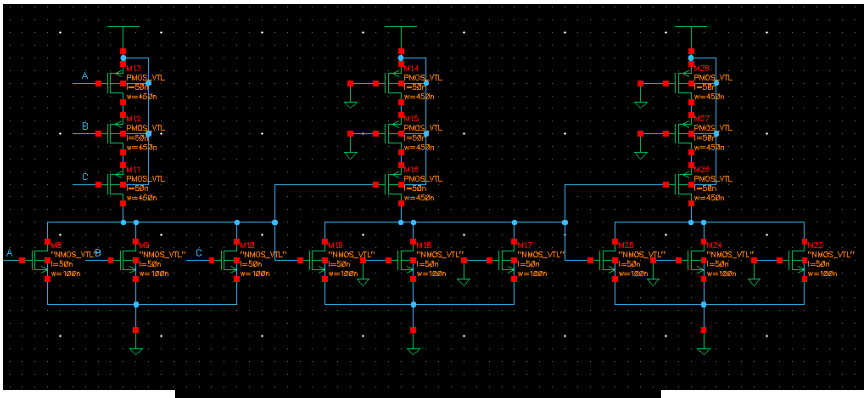


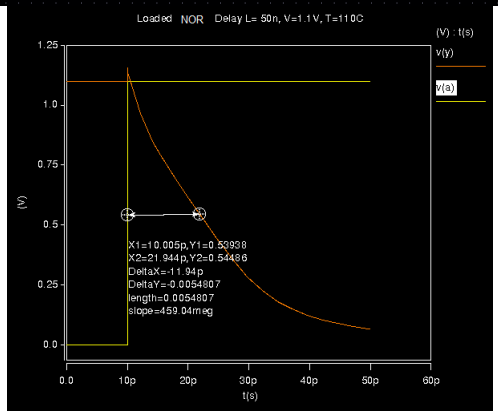
Doing this shows that the minimal propagation delay tp0 is 2.856ps

I ran another simulation with this gate loaded with a single inverter, shown below. The loaded delay is 4.72ps, therefore we can say the delay for this inverter with h gates loading it is tp = 2.85 + h*(4.72-2.85) = 2.85 + 1.87*h



The NOR gate was then simulated with no load on the output and a step was applied separately to each input to determine the unloaded delay for each input. The NOR gate was then loaded with a chain of NOR gates as shown below to determine the propagation delay for a single 3IN NOR load. From this a delay equation was derived for each input (on handwritten parts of assignment). The values for logical effort in terms of P and G were then found by dividing the p and g values for each input of the NOR by the minimal inverter p and g values. The found P and G values are listed on the hand written part of this assignment

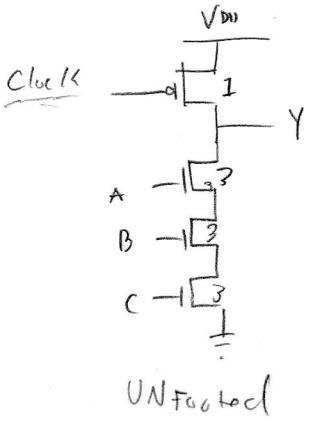




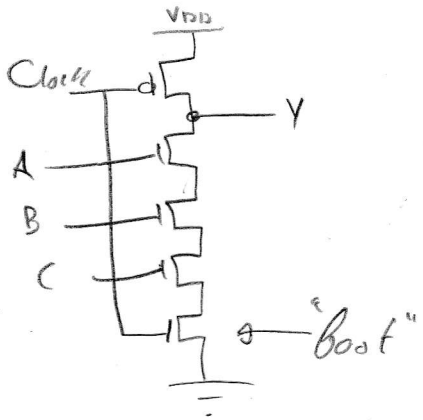
Above: example simulation of NOR delay for unloaded NOR gate and input A tested. I'm not going to show graphics of all the sims as it is redundant/waste of space. The measured values are given on the handwritten part of this problem

6 – 9.27)

NAND

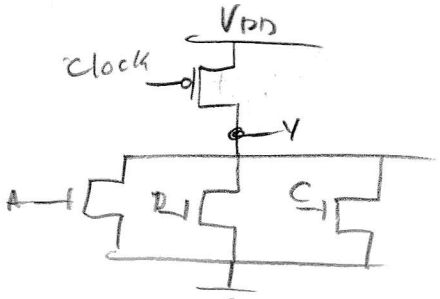


UNfooted

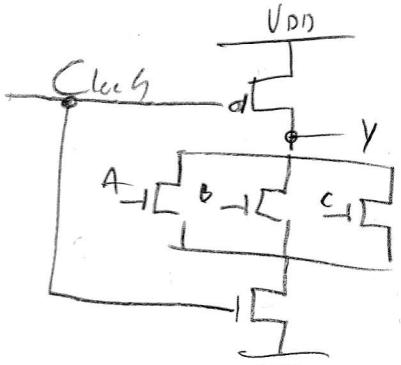


Footed

NOR



unfooted



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