CHAPTER R2

C1

(a) (iii)...A **wide**-base diode is assumed.

(b) (ii)...The R-G current is the dominant current component.

(c) (iv)...Avalanching is the dominant process causing breakdown if $V_{BR} > \sim 4.5$ V.

(d) (i)...C_J varies as $1/\sqrt{V_{bi}-V_A}$ **if one has a step junction.**

C2

(a) (i) forward biased...$p_n(x=x_n) > p_{n0} = n_i^2/N_D$. One has a carrier excess at the n-edge of the depletion region.

(b) (ii) the same as...Per the Eq. (6.18) boundary condition

$$\Delta p_n(x=x_n) = (n_i^2/N_D)(e^{qV_A/kT} - 1)$$

The n_i^2/N_D factor must be the same for both diodes since the minority carrier concentrations in the two diodes approach the same value as $x \rightarrow \infty$. Also, $\Delta p_n(x=x_n)$ is the same for both diodes. It therefore follows that V_A must be the same for both diodes.

(c) (i) significantly larger than...As emphasized in Subsection 8.1.2 (see Eq. 8.2), the current flowing in an ideal diode is directly proportional to $d\Delta p_n/dx|_{x=x_n}$. Inspecting the figure associated with the problem, we find the magnitude of $d\Delta p_n/dx|_{x=x_n} = dp_n/dx|_{x=x_n}$ is greater for Diode B.

(d) (ii) roughly the same as...If n_i^2/N_D is the same in two p^+-n Si diodes maintained at room temperature, then the N_D doping must be the same in the two diodes. Now, the V_{BR} of a p^+-n junction varies in an inverse manner with the n-side N_D doping. Thus, even though the p^+-side N_A doping may be different, having the same N_D doping, the diodes should exhibit roughly the same breakdown voltage.

C3

(a) Forward biased. There is an *excess* of minority carriers adjacent to the edges of the depletion region.

(b) Yes — low level injection does prevail. As required for low-level injection conditions to prevail, the majority carrier concentrations in the quasineutral regions are essentially unperturbed, and the minority carrier concentrations in these regions are much less than the majority carrier concentrations.

(c) The diffusion capacitance (C_D) results directly from the oscillation of minority carrier charge piled-up near the depletion region edges in response to an applied a.c. signal.

(d) In going from the forward-bias "on"-state to the reverse-bias "off"-state, the store of minority carriers adjacent to the edges of the depletion region must be removed. Since this cannot be accomplished instantaneously, there is a lag time known as the storage delay time (t_S) that is observed during the turn-off transient.

C4

(a–f) The required dashed-line or "no effect" answers are given in the figures on the next page. An explanation of the answers (which is not technically required) is provided below.

(a) The increase in N_D leads to two major modifications in the *I–V* characteristic. First, since V_{BR} is approximately proportional to $1/N_D$, increasing N_D by a factor of 2 decreases V_{BR} by about a factor of 2. Second, from the shape of the *I–V* characteristic, it is clear that the *R–G current dominates* in the given device. (This is also to be expected, since the characteristics were said to be derived from a Si diode maintained at room temperature.) For reverse biases greater than a few kT/q volts,

$$I_{R\text{-}G} = -\frac{qAn_i}{2\tau_0} W \qquad \text{... Eq. (6.43)}$$

where

$$W = \left[\frac{2K_S\varepsilon_0}{qN_D}(V_{bi} - V_A)\right]^{1/2} \qquad \text{... Eq. (5.38) for a } p^+\text{-}n$$

At biases where $-V_A >> V_{bi}$, $W \propto 1/\sqrt{N_D}$, and the factor of 2 increase in N_D reduces W and therfore $I_{R\text{-}G}$ by a factor of $\sqrt{2}$. At small $-V_A$, V_{bi}, which is slightly increased by increasing N_D, causes the decrease in W and $I_{R\text{-}G}$ to be slightly less than $\sqrt{2}$.

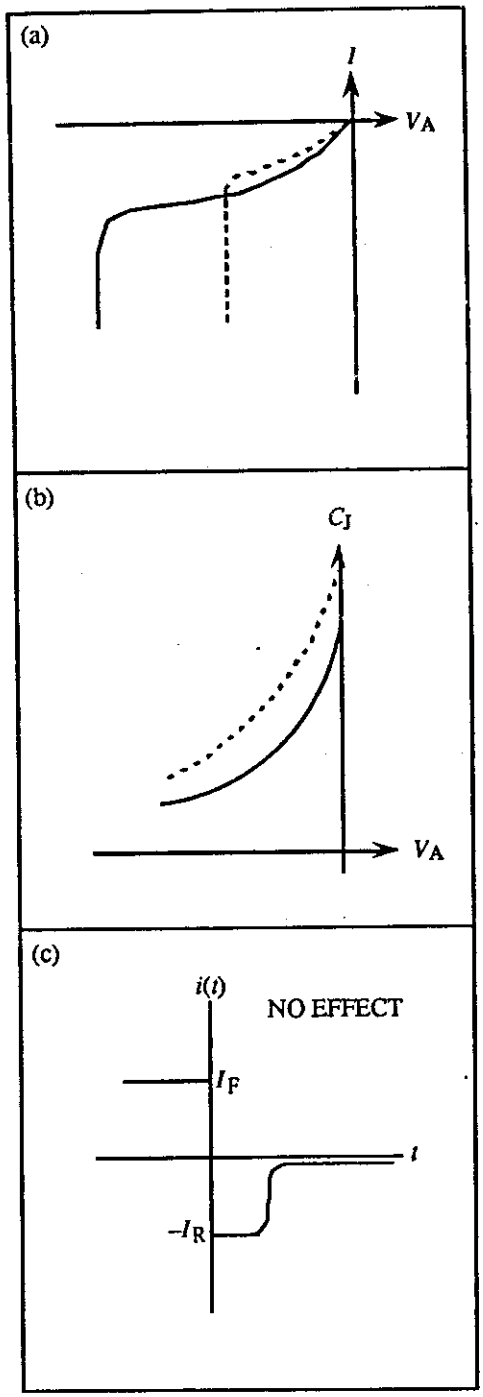
(b) Noting $C_J = K_S\varepsilon_0 A/W$, we conclude based on the discussion in part (a) that $C_J \propto 1/W$ will increase by a factor of $\sqrt{2}$ if $-V_A >> V_{bi}$. At small $-V_A$, the slight increase in V_{bi} with the increase in N_D will lead to an increase in C_J that is slightly less than $\sqrt{2}$.

(c) The storage delay time relationships developed and cited in Chapter 8 (Eqs. 8.8 and 8.9) are not a function of the semiconductor doping.

(d) As noted in the part (a) explanation, $I_{R\text{-}G} \propto 1/\tau_0$ is clearly the dominant current component. Thus, increasing τ_0 by a factor of 2 will decrease the observed current by a factor of 2.

(e) The junction capacitance is not a function of the τ_p and τ_0 carrier lifetimes.

(f) t_s as given by either Eq. (8.8) or (8.9) is directly proportional to τ_p. Thus, increasing τ_p by a factor of 2 causes t_s to increase by a factor of 2.


(a)
I
V_A
(b)
C_J
V_A
(c)
i(t)
NO EFFECT
I_F
t
$-I_R$
(d)
I
V_A
(e)
NO EFFECT
C_J
V_A
(f)
i(t)
I_F
t
$-I_R$