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UG Program in Electronics Engineering
(VLSI Design and Technology)

Design of a Modular Digital Data Monitoring Unit

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***Abstract*—Recent advances in embedded system technology have made real-time monitoring of sensor data increasingly important due to issues surrounding embedded system safety and embedded system efficiency. Although software polling typically occurs at much faster rates than electrical signals, it may not always capture event spikes that are of extremely brief duration. As a result, this project has developed an 8-Bit Data Register with user-defined thresholds for both signed and unsigned numeric types. The new design has additional features, such as a "Sticky Alarm" latch mechanism for storage of occurrences of extreme states (i.e., alarm conditions) and the ability to keep track of the actual data which caused the failure (i.e., fault capture register). This design was subjected to extensive simulation validation and can be applied to various application domains such as Industrial Automation and Healthcare, Environmental Monitoring, and has been tested against various related United Nations Sustainable Development Goals (UN SDGs).**

***Index Terms*—Digital Event Monitoring, Verilog HDL, Sticky Alarm, Fault Capture, FSM, SDGs.**

I. Introduction

The rapid development of the Internet of Things (IoT) and Industry 4.0 depends on Intelligent Hardware Sensors. Processor-based software may perform fine when a catastrophic failure occurs, but it may be busy doing other things. Intelligent monitoring of the sensor input must be through dedicated hardware logic. The project's objective is the creation of a re-usable Intellectual Property Core (IP Core) that will act as a "watchdog" to monitor sensor data continuously. The watchdog is implemented through state machine-based control logic for improved fault condition management when compared to, and in place of, using raw comparators. This will alleviate false alarms from the main processor while providing the main processor with additional useful diagnostic information.

II. Problem Statement

The newly implemented digital monitoring system's new features present a lot of benefits to businesses. However, there are still limitations to using digital monitoring tools today that are categorized into three areas of focus:

1) **Transitory Event Loss:** Sudden increases or decreases in a sensor's readings caused by conditions that are not considered normal (i.e., voltage transients), which might cause a loss of data before the data is analyzed through software.
2) **Insufficient Diagnostic Help From Alarm Systems:** A traditional alarm system will notify the user that there is an issue. Still, the diagnostic alarm system shows additional diagnostic data about the issues that have been classified and their severity.
3) **Device Management Programmed in Static Space:** The majority of current monitoring devices come programmed to respond to only certain specified signal types like unsigned integer types. Therefore, many monitoring devices are limited to being used in a single application and cannot be transferred to other applications that also require their use (e.g., temperature and audio).

We are developing a monitoring device that will have new capabilities; in addition to the above, we will also be adding:

1) Latching alarms;
2) Value capture mode;
3) Dynamic data mode selection.

III. System Architecture

This system design provides a modular Register Transfer Level (RTL) architecture that breaks the system into seven functional blocks to help make the code easier to read/debug/scalable.

A. Module Breakdown

The RTL Architecture consists of these seven submodules:

- **Sensor Register:** Provides clocking synchronization for the asynchronous input data from the sensor(s).
- **Threshold Register:** Contains the configurable maximum value.
- **MUX Selector:** Provides multiplexing and routing of the 8-bit data streams from the sensor(s).
- **Comparator:** Performs comparative arithmetic on the data based on the selected mode and value of the threshold register.
- **FSM Controller:** Provides a 3-state Moore Machine for controlling state changes.
- **Alarm Register:** Stores the alarm out signal.
- **Fault Capture Register:** Stores a sensor's value at the time of the threshold violation.

IV. Specifications

This design has normal FPGA Operating Clock Speeds along with the other following technical specifications:

TABLE I
SYSTEM SPECIFICATIONS

Parameter	Value / Description
Clock Frequency	50 MHz is (average) Maximum Processing Speed
Sample Latency	1 Cycle of Clock Time for producing an Alarm after Detection.
FSM States	Three States - IDLE, ALARM, COOLDOWN.
State Registers	Two Bits - To store the current state.
Reset Type	Asynchronous Reset Type Using Logic level zero - resets system immediately.
Data Width	Sensor and Threshold data both need an 8-bit width.
Interface Type	All operations are synchronized with help of 'clk'.

V. APPLICATIONS AND SDG MAPPING

The versatility of the Digital Event Monitoring Unit allows it to be deployed in diverse sectors. Table V maps specific use cases to the United Nations Sustainable Development Goals (SDGs).

Application Domain	Mapped SDG	Justification
Industrial Motor Overheat Protection	SDG 9	Innovation in resilient infrastructure.
Automotive Battery Management System	SDG 7	Promoting clean energy transport efficiency.
Medical Fever Detection / Infusion Pump	SDG 3	Ensuring good health and well-being via monitoring.
Environmental Flood Warning Systems	SDG 11	Safeguarding cities against climate disasters.
Agriculture Soil Moisture / Irrigation Control	SDG 6	Optimizing water usage efficiency.
Robotics Collision Detection (Current Surge)	SDG 9	Advanced manufacturing automation.
Consumer Smart Thermostat	SDG 12	Responsible consumption via energy saving.
Security Perimeter Intrusion Alarm	SDG 11	Creating safe public spaces.

VI. IMPLEMENTATION AND SIMULATION RESULTS

A. System Architecture Diagrams

Figure presents the DEMU (Digital Event Monitoring Unit) Architecture showing 7 different functions of the blocks: Sensor Register, Threshold Register, MUX Selector, Comparator, FSM Controller, Alarm Register and Fault Capture Register.

The control logic is managed by a Finite State Machine (FSM) as depicted in Figure 2. The diagram highlights the transition between IDLE, ALARM, and COOLDOWN states, ensuring sticky behavior and hysteresis.

Fig. 1. System architecture block diagram

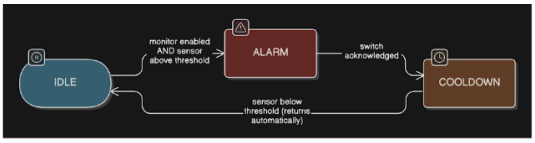

Fig. 2. Finite State Machine

B. Code Implementation

C. Simulation Results

Verification of the design was undertaken via eight different applicable scenarios, with confirmation of successful critical tests (Motor Overheat and Battery Overcharge) displayed in figure .

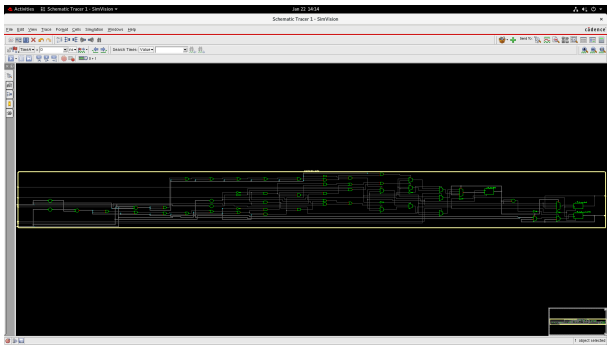

Fig. 3. Output from Cadence

The simulation output for the signal analysis is shown in Figure 4. It shows that the value of "ALARM OUT" holds HIGH and the value of the 'FAULT CAPTURE' register holds the trigger value even after the value for "SENSOR DATA" returns to its normal (safe) state, demonstrating a practical example of the sticky alarm.

VII. CONCLUSION

We created a Digital Event Monitor that can monitor digital events in real time with an 8-bit threshold. To do this, we

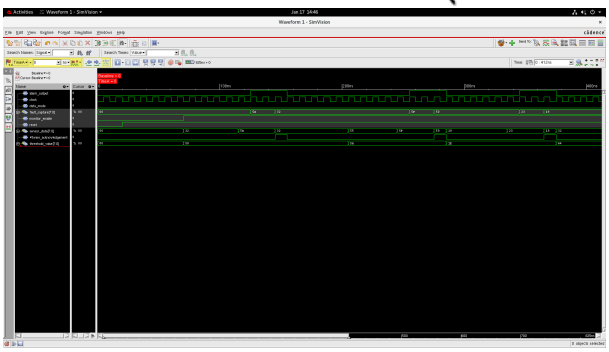

Fig. 4. Waveform Analysis

used a modular architecture and a specialized Finite State Machine (FSM). We can detect events with zero-latency software notification of those events. The Signed Data Mode and Snapshot Register provide the possibility of using the IP Core in any application including but not limited to Industrial Automation or Medical Monitoring. In addition, we plan to integrate the Digital Event Monitor with a Serial Peripheral Interface (SPI) port to dynamically configure the Digital Event Monitor and implement a Moving Average Filter to improve the performance of the Digital Event Monitor in environments where sensors produce noisy signals.

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