Computer Organization, Spring 2020

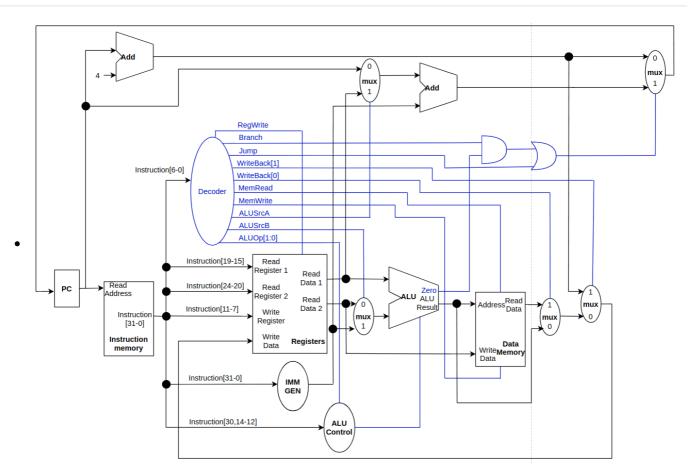
Lab 4: Single-Cycle CPU

Due: 2021/05/13

1. Goal

- To realize how to set the control signal in different instruction type.
 (Decoder & ALU Controller)
- To clarify how sign-extend work.
- · Connect all datapath to form a single cycle CPU

2. HW Requirement



- Finish the truth table for Decoder.(21%)
 - Every raw for 3 point. If a raw got any wrong answer, you will not get any point for that raw.

	Instr	RW	В	J	WB	MR	MW	Src	Op
0	R-type								
	addi								
	Load								
	Store								
	Branch								
	JAL								
	JALR								

- Implement bellow instruction for testing data.(60%)
 - add
 - o slt
 - o addi
 - o lw
 - SW
 - beq
 - jal
 - jalr
 - You would not get any score for this part if your program can't pass the test by script.
 - You should fill in name of your directory in all your {*.v} or you will not pass the script testing.

- Experiment (19 %)
 - What's the problem you encounter?(5%)
 - Your implement detail.(9%)
 - Anything you want to say.(5%)

3. Hand in

• Your hand in structure should like this.

- {\$(groupN)_\$(studentid1)_\$(studentid2)}.zip
 - \(\{\(\) \(\)
 - \$(studientid1)_report.pdf
 - \$(studientid2)_report.pdf
 - Makefile
 - Instruction.txt
 - {*.V}

```
group99_0811111_0811999/
 0811111_report.pdf
 0811999_report.pdf
 Adder.v
 ALU_Ctrl.v
 alu.v
 answer.txt
 Data_Memory.v
 Decoder.v
 demo.sh
 Imm_Gen.v
 Instr_Memory.v
 Instruction.txt
 Makefile
 MUX_2to1.v
 ProgramCounter.v
 Reg_File.v
 Simple_Single_CPU.v
 testbench.v
```

- Your report should be in PDF format.
- Report
 - o Truth table for decoder.
 - · Experiment.

4. Grade

- Pass the scritpt testing. 60%
- Truth table for decoder. 21%
- Experiment. 19%

5. Reference

- Slide (https://hackmd.io/@ameliawatson/ryBR8QZ8_#/)
- RISC V (https://riscv.org/technical/specifications/)