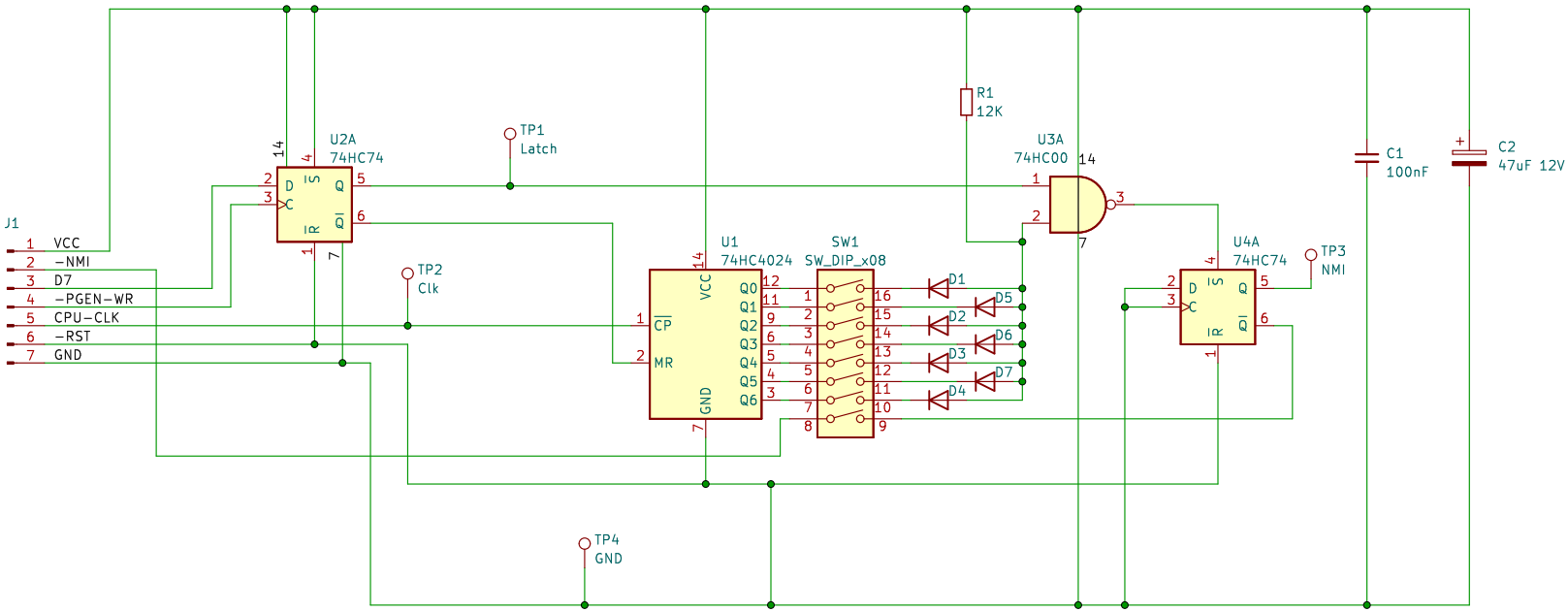

The Z80 samples the -NMI line on the rising edge of the last clock pulse of the previous instruction. So using the same clock the 4024 clocks on the 'negative transition' so we are not running into a race hazard.
The second latch will not set until all the selected bits are high so the switches read the number of T-states after the latch was set. As OUT (C),A; POP AF; RET is 32 T-states I anticipate needing a value about 30 depending where in the OUT the port actually sets. With 7 bits we can do 0-127.
Since a NOP is 4 T-states I would anticipate the best moment to hit it would be 2 T-states into the instruction we are single stepping.

NigSoft		
Sheet: File: Z80singlestep.kicad_sch		
Title: Z80 Single Step Adapter		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 7.0.1		Id: 1/1