Document Title

A7130 Data Sheet, 2.4GHz FSK/GFSK Transceiver with 3M / 4Mbps data rate

Revision History

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1. General Description

A7130 is a high performance and low cost 2.4GHz ISM band wireless transceiver. This device integrates both high sensitivity receiver (-88dBm @ 3Mbps, - 85dBm @4Mbps) and programmable high efficiency power amplifier (-20 ~ 5dBm). Based on Data Rate Register (0x0E), user can configure on-air data rates to either 3Mbps or 4Mbps.

A7130 supports fast settling time (100 us) for frequency hopping system. For packet handling, A7130 has built-in separated 64-bytes TX/RX FIFO (could be extended to 4K bytes) for data buffering and burst transmission, auto-ACK and auto-Resend, CRC for error detection and packet filtering, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, thermal sensor for monitoring relative temperature, WOR (Wake on RX) function to support periodically wake up from sleep mode to RX mode and listen for incoming packets without MCU interaction, data whitening for data encryption / decryption. In addition, A7130 has built-in AES128 co-processor (Advanced Encryption Standard) for advanced data encryption or decryption which consists of the transformation of a 128-bit block into an encrypted 128-bit block. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 20 pins package.

A7130's **control registers** and **Strobe commands** can be easily accessed via 3-wire or 4-wire SPI interface. Based on Strobe commands, MCU can control everything from power saving mode (deep sleep, sleep, idle, standby), TX delivery, RX receiving to **1-to-15 star networking management**. For easy to use, MCU can access control registers for channel monitoring, frequency hopping to auto calibrations. In addition, A7130 supports two general purpose I/O pins, GIO1 and GIO2, to inform MCU its status so that MCU could use either polling or interrupt scheme for radio control. Hence, it is very easy to monitor radio transmission between MCU and A7130 because of its digital interface.

2. Typical Applications

- 2.4GHz keyboard and mice
- 2.4GHz audio / video streaming
- HiFi quality wireless audio streaming
- 2400 ~ 2483.5 MHz ISM system
- Wireless metering and building automation
- Wireless toys and game controllers

3. Feature

- Small size (QFN4 X4, 20 pins).
- Frequency band: 2400 ~ 2483.5MHz.
- FSK or GFSK modulation
- Low current consumption: RX 24mA, TX 20mA (at 0dBm output power).
- Deep sleep current (0.1 uA).
- Sleep current (2.5 uA).
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Programmable data rate 3M or 4Mbps.
- Programmable TX power level from – 20 dBm to 5 dBm.
- Ultra High sensitivity:
  - -85dBm at 4Mbps on-air data rate.
  - -88dBm at 3Mbps on-air data rate.
- Fast settling time (100 us) synthesizer for frequency hopping system.
- On chip low power RC oscillator for WOR (Wake on RX) function.
- Built-in AES128 co-processor
- AGC (Auto Gain Control) for wide RSSI dynamic range.
- AFC (Auto Frequency Compensation) for frequency drift due to temperature.
- Support low cost crystal (12/ 16 / 18 / 24 / 26MHz).
- Support crystal sharing, (1 / 2 / 4 / 8MHz) to MCU.
- Low Battery Detector output indication.
- Easy to use.
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - ONE register setting for new channel frequency.
  - CRC Packet Filtering.
  - Auto Acknowledgement and Auto Resend.
  - PipeID to support 1-to-15 star networking.

- Dynamic FIFO length.
- 8-bits RSSI measurement for clear channel indication.
- Auto Calibrations.
- Auto IF function.
- Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
- Separated 64 bytes RX and TX FIFO.
- Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
- Support direct mode with recovery clock output to MCU.
- Support FIFO mode frame sync to MCU.

4. Pin Configurations

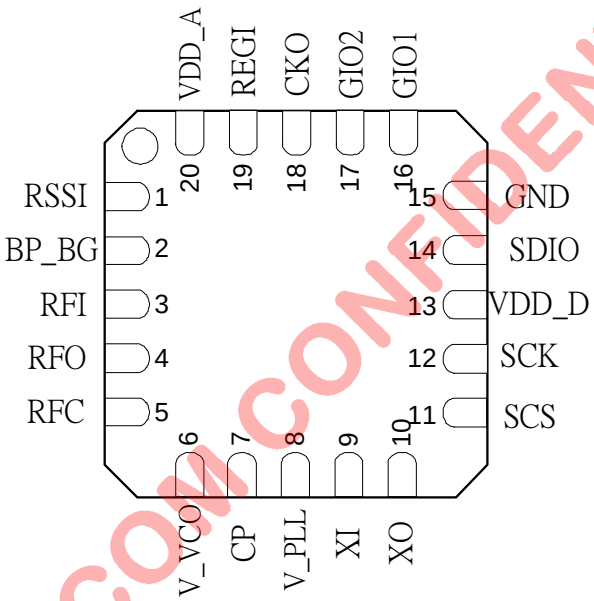


Fig 4-1. A7130 QFN 4x4 Package Top View

5. Pin Description (I: input; O: output, I/O: input or output)

Pin No.	Symbol	I/O	Function Description
1	RSSI	O	Connected to a bypass capacitor for RSSI.
2	BP_BG	O	Connected to a bypass capacitor for internal Regulator bias point.
3	RFI	I	LNA input. Connected to matching circuit.
4	RFO	O	PA input. Connected to matching circuit.
5	RFC	I	RF Choke input. Connected to matching circuit.
6	V_VCO	I	VCO supply voltage input.
7	CP	O	Charge-pump. Connected to loop filter.
8	V_PLL	I	PLL supply voltage input.
9	XI	I	Crystal oscillator input.
10	XO	O	Crystal oscillator output.
11	SCS	I	SPI chip select.
12	SCK	I	SPI clock input pin.
13	VDD_D	I	Connected to a bypass capacitor to supply voltage for digital part.
14	SDIO	I/O	SPI read/write data.
15	GND	G	Ground
16	GIO1	I/O	Multi-function GIO1 / 4-wire SPI data output.
17	GIO2	I/O	Multi-function GIO2 / 4-wire SPI data output.
18	CKO	O	Multi-function clock output.
19	REGI	I	Regulator input **(External Power Input)**
20	VDD_A	O	Internal Regulator output to supply **V_VCO (pin 6), V_PLL (pin 8) and RFC (pin 5).**
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

6. Chip Block Diagram

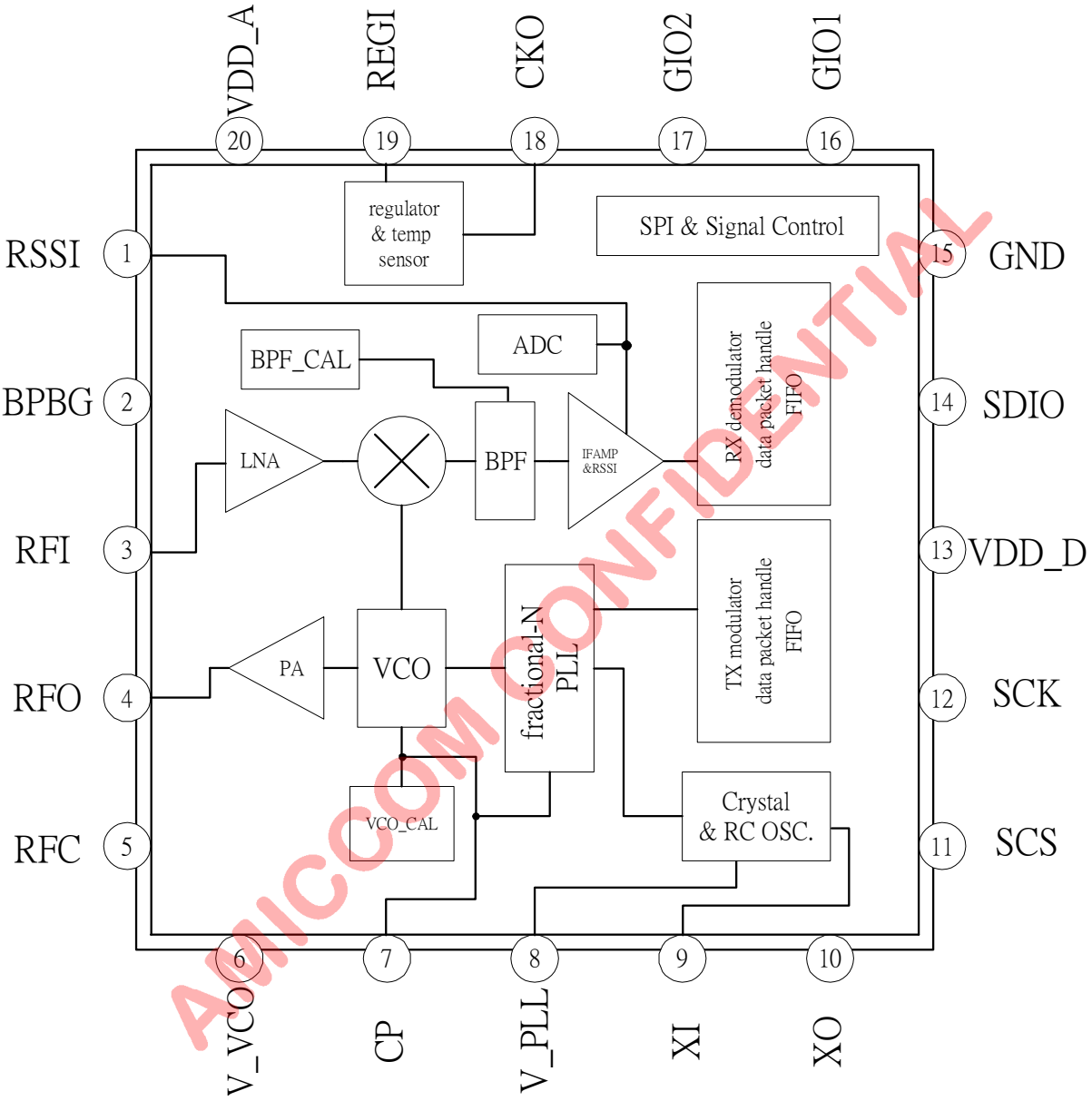


Fig 6-1. A7130 Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

8. Electrical Specification

(Ta=25℃, **VDD=3.0V**, F_{XTAL} =16MHz, with Match circuit and low pass filter, On Chip Regulator = **1.8V**, unless otherwise noted.)

Parameter	Description	Min.	Type	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD)	with internal regulator	2.0		3.6	V
Current Consumption	Deep Sleep mode*1 (No registers retention)		0.1		μA
	Sleep mode (RC OSC off) *1		2.5		μA
	Sleep mode (RC OSC on) *1		4		μA
	Idle Mode (Regulator on) *1		0.3		mA
	Standby Mode (XOSC on, CLK Gen. on)		2.5		mA
	PLL mode		10		mA
	RX Mode (4Mbps)		24		mA
	RX Mode (3Mbps)		21		mA
	TX Mode (@5dBm output)		TBD		mA
	TX Mode (@0dBm output)		18.5		mA
	TX Mode (@-3dBm output)		16.5		mA
	TX Mode (@-5dBm output)		15.5		mA
	TX Mode (@-10dBm output)		14		mA
	TX Mode (@-20dBm output)		13.5		mA
PLL block					
Crystal start up time*2			0.8		ms
Crystal frequency	Cload = 18 pF		16		MHz
Crystal tolerance	AFC disable		±30		ppm
	AFC enable		±50		ppm
Crystal ESR				80	ohm
VCO Operation Frequency		2400		2483.5	MHz
PLL phase noise	Offset 10k Offset 500K Offset 1M		75 85 95		dBc
PLL settling time*3 (Standby to PLL)	@Loop BW = TBD		50		μS
Transmitter					
Output power range		-20	0	5	dBm
Out Band Spurious Emission *4	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	dBm
	1.8GHz~ 1.9GHz			-47	dBm
	5.15GHz~ 5.3GHz			-47	dBm
Frequency deviation*5	Data rate 4Mbps		1M		Hz
	Data rate 3Mbps		735K		Hz
Data rate		3M		4M	bps
TX ready time*6 (PLL to WPLL + WPLL to TX)	@Loop BW = TBD LO changed		100		μS
Receiver					
Receiver sensitivity	Data rate 4M (FSK)		-85		dBm

@ BER = 0.1%	Data rate 4M (GFSK)		-82		
	Data rate 3M (FSK)		-88		
IF Filter bandwidth	Data rate 4M		4.8M		Hz
	Data rate 3M		3.6M		
IF center frequency	Data rate 4M		4M		Hz
	Data rate 3M		3M		Hz
Interference *7 (4Mbps , IF = 4MHz)	Co-Channel (C/I_0)		11		dB
	±4MHz Adjacent Channel		0		dB
	±8MHz Adjacent Channel		- 10		dB
	±12MHz Adjacent Channel		- 20		dB
	±16MHz Adjacent Channel		- 30		dB
	Image (C/I_{IM})		10		dB
Maximum Operating Input Power	@RF input (BER=0.1%)			5	dBm
RX Spurious Emission *4	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	AGC = 0	-95		-50	dBm
	AGC = 1	-95		-30	dBm
RX Ready Time*8 (PLL to WPLL + WPLL to RX)	@Loop BW = TBD LO changed		100		µs
Regulator					
Regulator settling time	Pin 2 connected to 1nF		300		µs
Band-gap reference voltage			1.23		V
Regulator output voltage		1.8	1.8	2.3	V
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, leakage current will be induced.
Note 2: Refer to Delay Register II (17h) to set up crystal settling delay.
Note 3: Refer to Delay Register I (17h) to set up PDL (PLL settling delay).
Note 4: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.
Note 5: Refer to TX Register II (15h) to set up FD [4:0].
Note 6: Refer to Delay Register I (17h) to set up PDL and TDL delay.
Note 7: The power level of wanted signal is set at sensitivity level +3dB. The modulation data for wanted signal and interferer are PN9 and PN15, respectively. Channel spacing is 500KHz.

9. Control Register

A7130 contains 51 x 8-bit control registers. MCU can access those control registers via 3-wire (SCS, SCK, SDIO) or 4-wire (SCS, SCK, SDIO, GIO1/GIO2) SPI interface (support max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details of SPI timing. A7130 is simply controlled by registers and outputs its status to MCU by GIO1 and GIO2 pins.

9.1 Control register table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Mode	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
	R	HECF	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
01h Mode control	W	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
	R	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
02h Calc	R/W	--	--	--	VCC	VBC	VDC	FBC	RSSC
03h FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
	R	LENF7	LENF6	LENF5	LENF4	LENF3	LENF2	LENF1	LENF0
04h FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
05h FIFO Data	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h ID Data	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
07h RC OSC I	W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
	R	RCOC7	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
08h RC OSC II	W	WOR_SL9	WOR_SL8	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0
09h RC OSC III	W	RTCS	RCOT2	RCOT1/ RTCC1	RCOT0/ RTCC0	CALWC	RCOSC_E	TSEL	TWOR_E
	R	--	--	--	--	CALWR	--	--	--
0Ah CKO Pin	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GPIO1 Pin I	W	VKM	VPM	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch GPIO2 Pin II	W	BBCKS1	BBCKS0	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
0Dh Clock	W	CGC1	CGC0	GRC3	GRC2	GRC1	GRC0	CGS	XS
	R	IFS1	IFS0	GRC3	GRC2	GRC1	GRC0	--	--
0Eh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
0Fh PLL II	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
10h PLL III	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
11h PLL IV	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	FSYN-FP15	AC14-FP14	AC13-FP13	AC12-FP12	AC11-FP11	AC10-FP10	AC9-FP9	AC8-FP8
12h PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	AC7-FP7	AC6-FP6	AC5-FP5	AC4-FP4	AC3-FP3	AC2-FP2	AC1-FP1	AC0-FP0
13h Channel Group I	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
14h Channel Group II	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
15h TX I	W	GDR	GF	TMDE	TXDI	TME	FDP2	FDP1	FDP0
16h TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

17h Delay I	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
18h Delay II	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
19h RX	W	LNAGE	AGCE	RXSM1	RXSM0	AFC	RXDI	DMG	ULS
1Ah RX Gain I	W	PRS	MIC	IGC1	IGC0	MGC1	MGC0	LGC1	LGC0
	R	--	MICR	IGCR1	IGCR0	MGCR1	MGCR0	LGCR1	LGCR0
1Bh RX Gain II	W	RSAGC1	RSAGC0	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0
	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
1Ch RX Gain III	W	--	RDU	IFS1	IFS0	RSM1	RSM0	ERSSM	RSS
	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
1Dh RX Gain IV	W	LIMC	IFBC1	IFBC0	IFAS	MHC1	MHC0	LHC1	LHC0
1Eh RSSI Threshold	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
1Fh ADC Control	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	RADC	FSARS	XADS	CDM
20h Code I	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
21h Code II	W	MSCRC	EDRL	HECS	ETH2	ETH1	ETH0	PMD1	PMD0
22h Code III	W	CRCINV	WS6	WS5	WS4	WS3	WS2	WS1	WS0
23h IF Calibration I	W	HFR	CKGS1	CKGS0	MFBS	MFB3	MFB2	MFB1	MFB0
	R	--	--	--	FBCF	FB3	FB2	FB1	FB0
24h IF Calibration II	W	PWORS	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	--	--	--	FCD4	FCD3	FCD2	FCD1	FCD0
25h VCO current Calibration	W	ROSCS	RSIS	VCRLS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
26h VCO band Calibration I	W	DCD1	DCD0	DAGS	CWS	MVBS	MVB2	MVB1	MVB0
	R	-	-	-	-	VBCF	VB2	VB1	VB0
27h VCO band Calibration II	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
28h VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
29h VCO deviation Calibration II	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
2Ah DASP0	W	QLIM	RFSP	INTRC (CSXTL5)	CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0
DASP1	W	STS	CELS	RGS	RGC1	RGC0	VRPL1	VRPL0	INTPRC
DASP2	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
DASP3	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
DASP4	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
	R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
DASP5	W	--	--	PKT1	PKT0	PKS	PKIS1	PKIS0	IFPK
DASP6	W	--	HPLS	HRS	PACTL	IWS	CNT	MXD	LXD

2Bh VCO modulation Delay	W	DMV1	DMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
2Ch Battery detect	W	LVR	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
	R	--	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
2Dh TX test	W	RMP1	RMP0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
2Eh Rx DEM test I	W	DMT	DCM1	DCM0	MLP1	MLP0	SLF2	SLF1	SLF0
2Fh Rx DEM test II	W	DCH1	DCH0	DCL2	DCL1	DCL0	RAW	CDTM1	CDTM0
30h Charge Pump Current I	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
31h Charge Pump Current II	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
32h Crystal test	W	CDPM	CPS	CPH	CPCS	DBD	XCC	XCP1	XCP0
33h PLL test	W	MDEN	OLM	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
34h VCO test	W	DEVGD2	DEVGD1	DEVGD0	TLB1	TLB0	RLB1	RLB0	VBS
35h RF Analog test	W	AGT3	AGT2	AGT1	AGT0	RFT3	RFT2	RFT1	RFT0
36h Key Data	W/R	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
37h Channel Select	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
38h ROM_P0	W	MPOR	EPRG	MIGS	MRGS	MRSS	MTMS	MADS	MBGS
ROMP1	W	APG	MPA1	MPA0	FBG4	FBG3	FBG2	FBG1	FBG0
ROMP2	W	PTM1	PTM0	CTR5	CTR4	CTR3	CTR2	CTR1	CTR0
ROMP3	W	FGC1	FGC0	SRS2	SRS1	SRS0	CRS2	CRS1	CRS0
ROMP4	W	--	STMP	STM5	STM4	STM3	STM2	STM1	STM0
39h Data Rate CLK	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
3Ah FCR	W	FCL1	FCL0	ARC3	ARC2	ARC1	ARC0	EACKS	EARTS
	R	ARTEF	VPOAK	RCR3	RCR2	RCR1	RCR0	EACKS	EARTS
3Bh ARD	W	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
3Ch AFEP	W	EACKF	SPSS	ACKFEP5	ACKFEP4	ACKFEP3	ACKFEP2	ACKFEP1	ACKFEP0
	R	--	--	EARTS	EARTS	EARTS	TXSID2	TXSID1	TXSID0
3Dh FCB	W/R	FCB7	FCB6	FCB5	FCB4	FCB3	FCB2	FCB1	FCB0
3Eh KEYC	W	KEYOS	AFIDS	ARTMS	MIDS	AESS	--	AKFS	EDCRS
3Fh USID	W	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0
	R	ICD7	ICD6	ICD5	ICD4	ICD3	ICD2	ICD1	ICD0

Legend: -- = unimplemented

9.2 Control register description

9.2.1 Mode Register (Address: 00h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode	R	--	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
Reset		--	--	--	--	--	--	--	--

RESETN: Write to this register by 0x00 to issue reset command, then it is auto clear

HECF: Head Control Flag. (Clear by any Strobe command.)
HEC is CRC-8 result for Packet Header (FCB and DFL, refer to chaper 16 for details)
[0]: HEC pass. **[1]:** HEC error.

FECF: FEC flag.
[0]: FEC pass. **[1]:** FEC error. (FECF is read clear.)

CRCF: CRC flag.
[0]: CRC pass. **[1]:** CRC error. (CRCF is read clear.)

CER: RF chip enable status.
[0]: RF chip is disabled. **[1]:** RF chip is enabled.

XER: Internal crystal oscillator enabled status.
[0]: Crystal oscillator is disabled. **[1]:** Crystal oscillator is enabled.

PLLE: PLL enabled status.
[0]: PLL is disabled. **[1]:** PLL is enabled.

TRER: TRX state enabled status.
[0]: TRX is disabled. **[1]:** TRX is enabled.

TRSR: TRX Status Register.
[0]: RX state. **[1]:** TX state.
Serviceable if TRER=1 (TRX is enable).

9.2.2 Mode Control Register (Address: 01h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control I	R	DDPC	ARSSI	AIF	DFCD	WORE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	CD	WORE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin.
[0]: Disable. **[1]:** Enable.

ARSSI: Auto RSSI measurement while entering RX mode.
[0]: Disable. **[1]:** Enable.

AIF (Auto IF Offset): RF LO frequency will auto offset one IF frequency while entering RX mode.
[0]: Disable. **[1]:** Enable.

CD: Carrier detector (Read only).
[0]: Input power below threshold. **[1]:** Input power above threshold.

DFCD: Data Filter by CD : The received packet would be filtered if the input power level is below RTH (1Eh).
[0]: Disable. **[1]:** Enable.

WORE: WOR (Wake On RX) Function Enable.
[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

ADCM: ADC measurement enable (Auto clear when done).
[0]: Disable measurement or measurement finished. **[1]:** Enable measurement.

ADCM	A7130 @ Standby mode	A7130 @ RX mode
[0]	Disable ADC	Disable ADC
[1]	No function	Measure RSSI, carrier detect

Refer to chapter 17 for details.

9.2.3 Calibration Control Register (Address: 02h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control II	R/W	--	--	--	VCC	VBC	VDC	FBC	RSSC
Reset		--	--	--	--	--	0	0	0

VCC: VCO Current calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VBC: VCO Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VDC: VCO Deviation calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

RSSC: RSSI calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.4 FIFO Register I (Address: 03h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO I	W	--	--	--	--	FEP11	FEP10	FEP9	FEP8
	R	--	--	--	--	LENF11	LENF10	LENF9	LENF8
	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
	R	LENF7	LENF6	LENF5	LENF4	LENF3	LENF2	LENF1	LENF0
Reset		0	0	1	1	1	1	1	1

FEP [11:0]: FIFO End Pointer for TX FIFO and Rx FIFO.
Refer to chapter 16 for details.

LENF [11:0]: Received FIFO Length for dynamic FIFO function. (Ready Only)
Used in dynamic length mode. (EDRL = 1).
Refer to chapter 16 for details.

9.2.5 FIFO Register II (Address: 04h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FPM [1:0]: FIFO Pointer Margin

PSA [5:0]: Used for Segment FIFO.
Refer to chapter 16 for details.

9.2.6 FIFO DATA Register (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	TX-FIFO[7:0]							
	R/W	RX-FIFO[7:0]							
Reset		0	0	0	0	0	0	0	0

FIFO [7:0]: TX FIFO / RX FIFO
TX FIFO and RX FIFO share the same address (05h).
TX FIFO and RX FIFO have independent physical 64 Bytes.
Refer to chapter 16 for details.

9.2.7 ID DATA Register (Address: 06h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ID DATA	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0

ID [7:0]: ID data.
When this address is accessed, ID Data is input or output sequential (ID Byte 0,1, 2 and 3) corresponding to Write or Read.
Recommend to set ID Byte 0 = 5xh or Axh.
Refer to section 10.6 for details.

9.2.8 RC OSC Register I (Address: 07h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RC OSC I	R	RCOC7	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
	W	WOR_SL7	WOR_SL6	WOR_SL5	WOR_SL4	WOR_SL3	WOR_SL2	WOR_SL1	WOR_SL0
Reset		0	0	0	0	0	0	0	0

RCOC [7:0]: Reserved for internal usage only.

9.2.9 RC OSC Register II (Address: 08h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RC OSC II	W	WOR_SL9	WOR_SL8	WOR_AC5	WOR_AC4	WOR_AC3	WOR_AC2	WOR_AC1	WOR_AC0
Reset		0	0	0	0	0	0	0	0

WOR_AC [5:0]: 6-bits WOR Active Timer for TWOR Function

WOR_SL [9:0]: 10-bits WOR Sleep Timer for TWOR Function.
WOR_SL [9:0] are from address (07h) and (08h),

Device Active = (WOR_AC+1) x (1/4092), (244us ~ 15.6ms).
Device Sleep = (WOR_SL+1) x (1/4092), (7.8ms ~ 7.99s).

9.2.10 RC OSC Register III (Address: 09h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RC OSC III	W	RTCS	RCOT2	RCOT1/ RTCC1	RCOT0/ RTCC0	CALWC	RCOSC_E	TSEL	TWOR_E
	R	--	--	--	--	CALWR	--	--	--
Reset		1	0	0	1	0	0	0	1

RTCS: internal Oscillator selection in sleep mode.
[0]: RC oscillator. **[1]:** RTC oscillator.

RCOT[1:0]: RCOSC current select for RC oscillator calibration.
(ROSCS,RSIS Recommand [0])
[00]: 240nA
[01]: 280nA
[10]: 320nA
[11]: 360nA

RCOT[2]: Reserved for internal used. Recommend [0]

TSEL: Timer select for TWOR function.

[0]: Use WOR_AC. **[1]:** Use WOR_SL.

CALWC: RC Oscillator Calibration Enable.
[0]: Disable. **[1]:** Enable.

CALWR: RC Oscillator Calibration ending indication.
[0]: ending. **[1]:** Not ending.

RCOSC_E: RC-oscillator enable. Reserved for internal usage only.
[0]: Disable. **[1]:** Enable.

TSEL: Timer select for TWOR function. Reserved for internal usage only.
[0]: Use WOR_AC. **[1]:** Use WOR_SL.

TWOR_E: Enable TWOR function. Reserved for internal usage only.
[0]: Disable. **[1]:** Enable.

9.2.11 CKO Pin Control Register (Address: 0Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKO Pin Control	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
Reset		1	0	1	1	1	0	1	0

ECKOE: External Clock Output Enable for CKOS [3:0]= [0100] ~ [0111].
[0]: Disable. **[1]:** Enable.

CKOS [3:0]: CKO pin output select.
[0000]: DCK (TX data clock) in TX mode, RCK (RX recovery clock) in RX mode.
[0001]: DCK (TX data clock) in TX mode, RCK (RX recovery clock) in RX mode.
[0010]: FPF (FIFO pointer flag).
[0011]: EOP, EOVBC, EOFBC, EOVCC, EOVDC, RSSC_OK. (Internal usage only).
[0100]: External clock output= F_{SYCK} / 2.
[0101]: External clock output / 2= F_{SYCK} / 4.
[0110]: RXD
[0111]: FSYNC.
[1000]: WCK.
[1001]: PF8M.(8Mhz)
[1010]: ROSC.
[1011]: MXDEC(SLF[0]=1:~OKADCN, SLF[1]=0: DEC)
[1100]: BDF.(Battery Detect flag).
[1101]: F_{SYCK} ..
[1110]: VPOAK
[1111]: WRTC. (RTC clock come from RTC oscillator.)

CKOI: CKO pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCKI: SPI clock input invert.
[0]: Non-inverted input. **[1]:** Inverted input.

9.2.12 GIO1 Pin Control Register I (Address: 0Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIO1 Pin Control I	W	VKM	VPM	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
Reset		0	0	0	0	0	0	0	1

VKM: Valid packet mode select.
[0]: by event. [1]: by pulse.

VPM: Valid Pulse width select.
[0]: 20u. [1]: 40u.

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	ARCWTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC (frame sync)
[0010]	TMEO or TMDEO(TX modulation enable)	CD (carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	TMRE or RTCS=1:MCU wakeup signal (TWOR) TMRE and RTCS=0:WTR (Wait until TX or RX finished)	
[0101]	In phase demodulator input(DMII)orVT[0]	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_RX	
[1011]	External FSYNC input in RX direct mode	
[1100]	MXINC(SLF[0]=1:EOADC.SLF[1]=0:INC.)	
[1101]	FPF	
[1110]	VPOAK (Auto Resend OK Ouput)	
[1111]	FMTDO	

If GIO1S=[1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, it is recommended that user asserts frame sync signal to this input to get better DC estimation of demodulation.

GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO1OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.13 GIO2 Pin Control Register II (Address: 0Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GIO2 Pin Control II	W	BBCKS1	BBCKS0	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
Reset		0	1	0	1	0	0	0	1

BBCKS [1:0]: Clock select for digital block. Recommend BBCKS = [00].
[00]: F_{SYCK}. **[01]:** F_{SYCK} / 2. **[10]:** F_{SYCK} / 4. **[11]:** F_{SYCK} / 8.
F_{SYCK} is A7130's System clock = 16MHz.

GIO2S [3:0]: GIO2 pin function select.

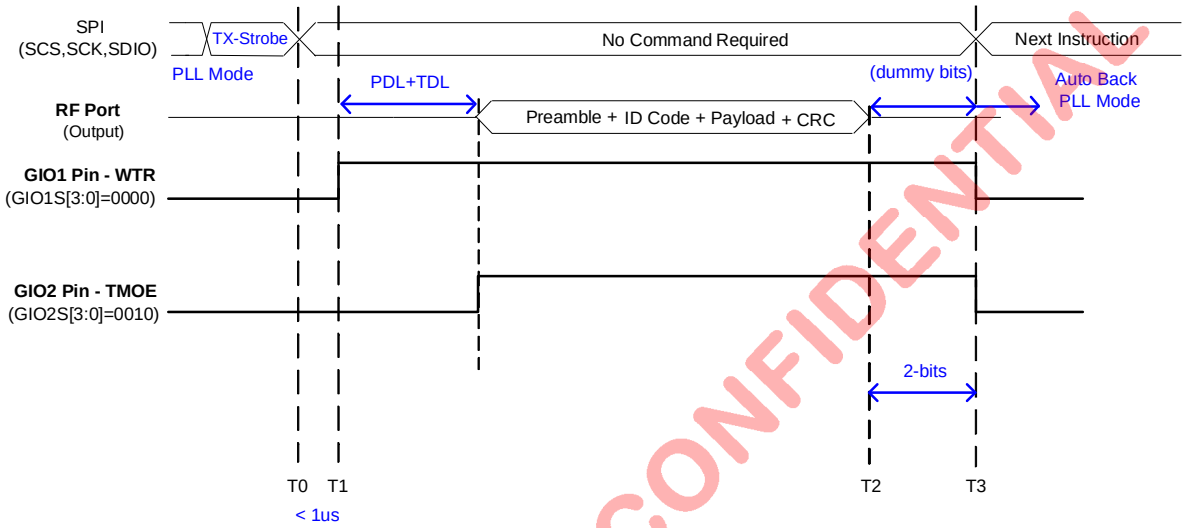
GIO2S	TX state	RX state
[0000]	ARCWTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC (frame sync)
[0010]	TMEO (TX modulation enable)	CD (carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	TMRE or RTCS=1:MCU wakeup signal (TWOR) TMRE and RTCS=0:WTR (Wait until TX or RX finished)	
[0101]	Quadrature phase demodulator input (DMIQ)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_TX	
[1011]	ROMOK(ROM Program OK)	
[1100]	BDF	
[1101]	FPF	
[1110]	VPOAK	

[1111]	~DCK

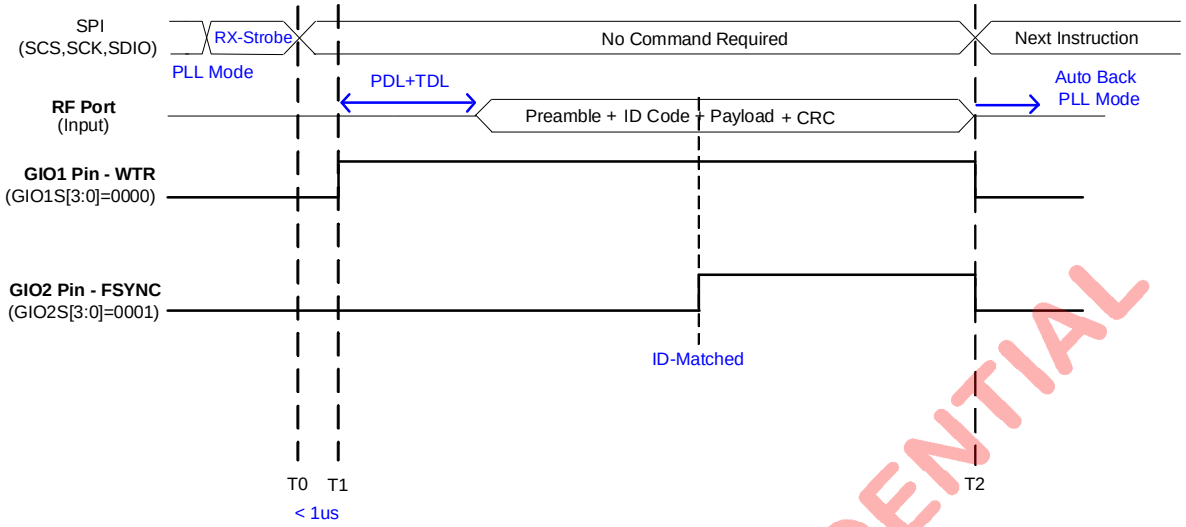
GIO2I: GIO2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO2OE: GIO2 pin Output Enable.
[0]: High Z. **[1]:** Enable.

In TX mode



In RX mode



9.2.14 Clock Register (Address: 0Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clock	W	CGC1	CGC0	GRC3	GRC2	GRC1	GRC0	CGS	XS
	R	IFS1	IFS0	GRC3	GRC2	GRC1	GRC0	--	--
Reset		1	0	0	1	1	1	0	1

Refer to chapter 13 for details.

IFS [1:0]: IF band selection reading

CGC [1:0]: for 96Mhz or 128Mhz clock generation current. Shall be set to [10].

CGS: Clock generator enable. Recommend CGS = [0]
[0]: Disable. **[1]:** Enable.

CGS = 0 (recommend)	CGS = 1
Disable internal 32MHz PLL clock	F_{MCLK} = 32 MHz

XS: Crystal oscillator select. Recommend XS = [1]
[0]: External clock. **[1]:** Crystal.

GRC [3:0]: Clock generation reference counter.

GRC[3:0]	Note
Don't care	**Recommend when CGS = 0**
F_{XTAL} x (DBL+1) / (GRC+1) = 2M	When CGS = 1

9.2.15 PLL Register I (Address: 0Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

CHN [7:0]: LO channel number select.
Refer to chapter 14 for details.

9.2.16 PLL Register II (Address: 0Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL II	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8

	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		1	0	0	1	1	1	1	0

DBL: Crystal frequency doubler selection. Recommend DBL = [1]
[0]: Disable. $F_{XREF} = F_{XTAL}$. **[1]:** Enable. $F_{XREF} = 2 * F_{XTAL}$.

RRC [1:0]: RF PLL reference counter setting.
The PLL comparison frequency, $F_{PFD} = F_{CRYSTAL} *(DBL+1) / (RRC+1)$.

CHR [3:0]: PLL channel step setting.

Refer to chapter 14 for details.

9.2.17 PLL Register III (Address: 10h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL III	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		0	1	0	0	1	0	1	1

BIP [8:0]: LO base frequency integer part setting. Recommend BIP[8:0] = [0x04B]
BIP [8:0] are from address (0Fh) and (10h),

IP [8:0]: LO frequency integer part value.
IP [8:0] are from address (0Fh) and (10h),

Refer to chapter 14 for details.

9.2.18 PLL Register IV (Address: 11h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL IV	R	RAC15	RAC14	RAC13	RAC12	RAC11	RAC10	RAC9	RAC8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		1	0	0	0	0	0	0	0

9.2.19 PLL Register V (Address: 12h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL V	R	RAC7	RAC6	RAC5	RAC4	RAC3	RAC2	RAC1	RAC0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	0	1	1

BFP [15:0]: LO base frequency fractional part setting. (BFP = [0000] is forbidden.)
BFP [15:0] are from address (11h) and (12h),

AC [14:0] : LO frequency fractional part

RAC [15:0] (Read): Auto Frequency compensation value if AFC (19h) =1.
Refer to chapter 14 for details.
PLLFF **[15:0]**: the fractional part in PLL,
the RAC value show in the following table.

AFC(19h)	RAC **[15:0]**
1	PLLFF **[15:0]**
0	{SYNCF, AC **[14:0]**}

Refer to chapter 14 for details.

9.2.20 Channel Group Register I (Address: 13h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHGI	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	0	1	0	0	0

CHGL [7:0]: PLL channel group low boundary setting.
Refer to chapter 15 for details.

9.2.21 Channel Group Register II (Address: 14h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHGII	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	0	1	0	0	0	0

CHGH [7:0]: PLL channel group high boundary setting.
Refer to chapter 15 for details.

PLL frequency is divided into 3 groups:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

Note: Each group needs its own VCO current, bank and deviation calibration. Use the same calibration value for the frequency in the same group.

9.2.22 TX Register I (Address: 15h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX I	W	GDR	GF	TMDE	TXDI	TME	FDP2	FDP1	FDP0
Reset		0	0	1	0	1	1	1	0

GDR: Gaussian Filter Over Sampling Rate Select.
[0]: BT= 1 **[1]:** BT= 0.5

GF: Gaussian Filter Select.
[0]: Disable. **[1]:** Enable.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert. **[1]:** Invert.

TME: TX modulation enable.
[0]: Disable. **[1]:** Enable.

FDP [2:0]: Frequency deviation power setting. Refer to control register (15h). Recommend FDP = [110].

9.2.23 TX Register II (Address: 16h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXI	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		0	0	1	0	1	1	1	1

FD [7:0]: Frequency deviation setting.
$F_{DEV} = F_{PFD} /2**16*FD* 2**(FDP-1)$.
Where $F_{PFD}= F_{XTAL} * (DBL+1) / (RRC [1:0]+1)$, PLL comparison frequency.

Data Rate	FD[7:0]	Fdev (KHz)
4Mbps	TBD	TBD
3Mbps	TBD	TBD

9.2.24 Delay Register I (Address: 17h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delay	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
Reset		0	0	0	1	0	0	1	0

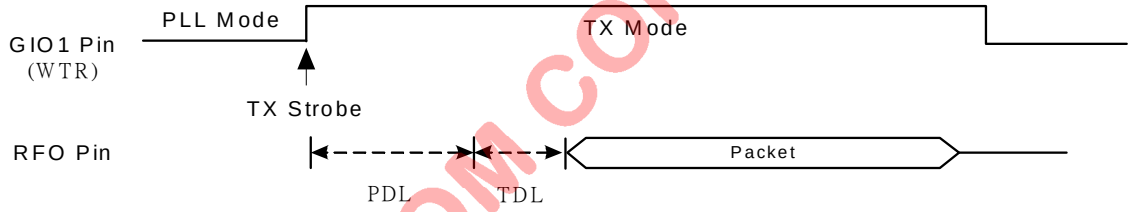
DPR [2:0]: Delay scale. Recommend DPR = [000].

TDL [1:0]: Delay for TX settling from WPLL to TX.
Delay= 20 * (TDL [1:0]+1)*(DPR [2:0]+1) us.

DPR [2:0]	TDL [1:0]	WPLL to TX	Note
000	00	20 us	
000	01	40 us	
000	10	60 us	**Recommend**
000	11	80 us	

PDL [2:0]: Delay for TX settling from PLL to WPLL.
Delay= 10+20 * (PDL [2:0]+1)*(DPR [2:0]+1) us.

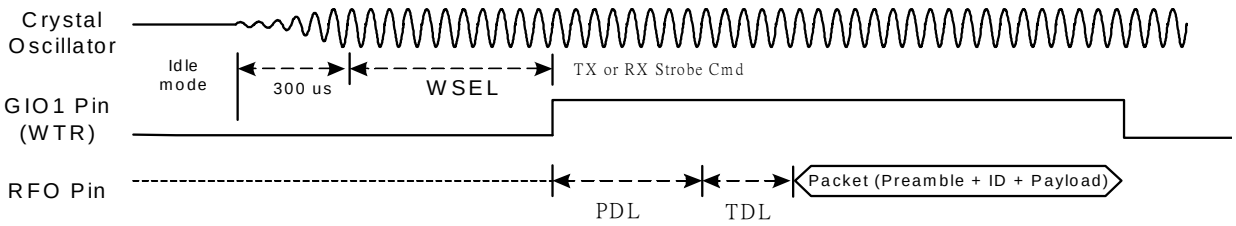
DPR [2:0]	PDL [2:0]	PLL to WPLL (LO freq. fixed)	PLL to WPLL (LO freq changed)	Note
000	001	10 us	50 us	
000	010	10 us	70 us	**Recommend**
000	011	10 us	90 us	
000	100	10 us	110 us	



9.2.25 Delay Register II (Address: 18h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delay	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
Reset		0	1	0	0	0	0	0	1

WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [010].
[000]: 200us. **[001]:** 400us. **[010]:** 600us. **[011]:** 800us.
[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.



RSSC_D [1:0]: RSSI calibration switching time (10us ~ 40us). Recommend RSSC_D = [00].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

RS_DLY [2:0]: RSSI measurement delay (10us ~ 80us). Recommend RS_DLY = [000].

[000]: 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us.
[100]: 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

9.2.26 RX Register (Address: 19h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX	W	LNAGE	AGCE	RXSM1	RXSM0	AFC	RXDI	DMG	ULS
Reset		0	0	1	0	0	0	0	0

LNAGE: Auto LNA Gain Control Select.
[0]: Disable. **[1]:** Enable.

AGCE: Auto Front end Gain Control Select.
[0]: Disable. **[1]:** Enable.

RXSM1: RX clock recovery circuit moving average filter length. Recommend RXSM1 = [1].
[0]: 4 bits. **[1]:** 8 bits.

RXSM0: Demodulator LPF Bandwidth Select. Recommend RXSM0 = [1].
[0]: 2*IF. **[1]:** 1*IF.

AFC: Frequency compensation select.
[0]: Disalbe . **[1]:** Enable.
Refer to section 14.4 for details.

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output. **[1]:** Inverted output.

DMG: Demodulator Gain Select. Recommend DMG = [0].
[0]: x 1. **[1]:** x 3.

ULS: RX Up/Low side band select.
[0]: Up side band, **[1]:** Low side band.
Refer to section 14.2 for details.

9.2.27 RX Gain Register I (Address: 1Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain I	W	PRS	MIC	IGC1	IGC0	MGC1	MGC0	LGC1	LGC0
	R	--	MICR	IGCR1	IGCR0	MGCR1	MGCR0	LGCR1	LGCR0
Reset		0	1	1	1	1	1	1	1

PRS: Limiter amplifier discharge manual select. Recommend PRS =[0].
MIC: Mixer buffer gain setting [0]: 0dB**[1]:** 6dB

IGC [1:0]: IFA Attenuation Select.
[00]: 0dB. **[01]:** 6dB. **[10]:** 12dB. **[11]:** 18dB.

MGC [1:0]: Mixer Gain Attenuation select.
[00]: 0dB. **[01]:** 6dB. **[10]:** 12dB. **[11]:** 18dB.

LGC [1:0]: LNA Gain Attenuation select.
[00]: 6dB. **[01]:** 12dB. **[10]:** 18dB. **[11]:** 24dB.

9.2.28 RX Gain Register II (Address: 1Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain II	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
	W	RSAGC1	RSAGC0	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0
Reset		0	0	1	0	0	1	0	0

RSAGC [1:0]: AGC clock select.
[00]: IF / 8. **[01]:** IF / 4. **[10]:** IF / 2. **[11]:** IF.

VTH [2:0] (write): auto gain control high voltage threshold select

VTL [2:0] (write): auto gain control low voltage threshold select.

VTH [2:0]: VCO tuning voltage upper threshold level setting. Recommend VTH = [111].
[000]: VDD_A – 0.6V. **[001]:** VDD_A – 0.7V. **[010]:** VDD_A – 0.8V. **[011]:** VDD_A – 0.9V
[100]: VDD_A – 1.0V. **[101]:** VDD_A – 1.1V. **[110]:** VDD_A – 1.2V. **[111]:** VDD_A – 1.3V

VDD_A is on chip analog regulator output voltage

VTL [2:0]: VCO tuning voltage lower threshold level setting. Recommend VTL = [011].
[000]: 0.1V. **[001]:** 0.2V. **[010]:** 0.3V. **[011]:** 0.4V.
[100]: 0.5V. **[101]:** 0.6V. **[110]:** 0.7V. **[111]:** 0.8V

RH [7:0]: RSSI Calibration High Threshold.

9.2.29 RX Gain Register III (Address: 1Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain III	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
	W	DCH	RDU	IFS1	IFS0	RSM1	RSM0	ERSSM	RSS
Reset		0	0	1	0	0	1	0	1

RL [7:0]: RSSI Calibration Low Threshold.

DCH: DC Estimation Waiting Time for DC Estimation Hold before ID Detected.
[0]: 4bit data after preamble is OK. **[1]:** 8bit data after preamble is OK.

RDU: data rate select. (CGS=1), when IFS=11.
[0]: 4MHZ **[1]:** 3MHZ**.**

IFS [1:0]: IF Frequency Select.
[00]:1MHZ. **[01]:** 2MHz. **[10]:** 3MHZ. **[11]:** 4MHZ.

RSM [1:0]: RSSI Margin = RTH – RTL. Recommend RSM = [01].
[00]: 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.
Refer to chapter 17 for details.

ERSSM: Ending Mode Select in RSSI Measurement
[0]: RSSI ending by RX. **[1]:** RSSI ending by SYNC_Ok.

RSS: RSSI measurement select. (XADS=0, RSS=0, default mode is 溫度sensor)
[0]: Disable. **[1]:** Enable.

9.2.30 RX Gain Register IV (Address: 1Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX Gain III	W	LIMC	IFBC1	IFBC0	IFAS	MHC1	MHC0	LHC1	LHC0
Reset		1	1	0	0	0	1	0	1

LIMC: IF limiter current select.
[0]: 0.3mA. **[1]:** 0.6mA.

IFBC [1:0]: IF BPF current Select.
[00]: 0.75 mA.. **[01]:** 1.4mA. **[10]:** 2.1mA. **[11]:** 3.5mA.

MHC: Mixer Current Select.
[0]: 0.6mA. **[1]:** 1mA.

LHC[1:0]: LNA Current Select.
[00]: 0.5mA. **[01]:** 1mA. **[10]:** 1.5mA. **[11]:** 2mA.

9.2.31 RSSI Threshold Register (Address: 1Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSSI Threshold	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
Reset		0	0	0	0	0	0	0	0

RTH [7:0]: Carrier detect threshold.
Refer to Chapter 17 for details.
CD (Carrier Detect)=1 when RSSI ≧ RTH.
CD (Carrier Detect)=0 when RSSI < RTL.

ADC [7:0]: ADC output value for RSSI measurement.
ADC input voltage= 1.2 * ADC [7:0] / 256 V.
Refer to chapter 17 for details.

9.2.32 ADC Control Register (Address: 1Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC Control	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	RADC	FSARS	XADS	CDM
Reset		1	0	1	0	0	1	0	0

AVSEL [1:0]: ADC average times (for Carrier / temeperature sensor / external ADC). Recommend AVSEL = [10].
[00]: No average. **[01]:** Average 2 times. **[10]:** Average 4 times. **[11]:** Average 8 times.

MVSEL [1:0]: ADC average times (for VCO calibration and RSSI). Recommend MVSEL = [01].
[00]: Average 8 times. **[01]:** Average 16 times. **[10]:** Average 32 times. **[11]:** Average 64 times.

RADC: ADC Read Out Average Mode.
[0]: 1, 2, 4, 8 average mode. The average number is according to the setting of AVSEL in **RX Gain Register (IV)**.
[1]: 8, 16, 32, 64 average mode. The average number is according to the setting of MVSEL in **RX Gain Register (IV)**.

FSARS: ADC clock select. Recommend FSARS = [0].
[0]: 4MHz. **[1]:** 8MHz.

XADS: External ADC Input Signal Select.
[0]: Disable. **[1]:** Enable.

CDM: RSSI measurement mode.
[0]: Single mode. **[1]:** Continuous mode.

9.2.33 Code Register I (Address: 20h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Code I	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
Reset		0	0	0	0	0	1	1	1

MSC: Manchester Enable.
[0]: Disable. **[1]:** Enable.

WHTS: Data Whitening (Data Encryption) Select.
[0]: Disable. **[1]:** Enable (The data is whitening by multiplying PN7).

FECS: FEC Select.
[0]: Disable. **[1]:** Enable (The FEC is (7, 4) Hamming code).

CRCS: CRC Select.
[0]: Disable. **[1]:** Enable.

IDL [1:0]: ID Code Length Select. Recommend IDL= [01].
[00]: 2 bytes. **[01]:** 4 bytes. **[10]:** 6 bytes. **[11]:** 8 bytes.

PML [1:0]: Preamble Length Select. Recommend PML= [11].
[00]: 1 byte. **[01]:** 2 bytes. **[10]:** 3 bytes. **[11]:** 4 bytes.

9.2.34 Code Register II (Address: 21h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Code II	W	MSCRC	EDRL	HECS	ETH2	ETH1	ETH0	PMD1	PMD0
Reset		0	0	0	0	0	1	1	0

MSCRC: Mask CRC (CRC Data Filtering Enable).
[0]: Disable. **[1]:** Enable.

EDRL: Enable FIFO Dynamic Length
[0]: Disable. **[1]:** Enable.

ETH [2:0]: Received ID Code Error Tolerance. Recommend ETH = [001].
[000]: 0 bit, **[001]:** 1 bit. **[010]:** 2 bit. **[011]:** 3 bit. **[100]:** 4 bit, **[101]:** 5 bit. **[110]:** 6 bit. **[111]:** 7 bit.

PMD [1:0]: Preamble pattern detection length.
[00]: 0bit. **[01]:** 4bits. **[10]:** 8bits. **[11]:** 16bits.

Data Rate (Kbps)	PMD[1:0]	Note
2 ~ 125	11	Also refer to addr. 29h
250 / 500	10	

Refer to chapter 16 for details.

9.2.35 Code Register III (Address: 22h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Code III	W	CRCINV	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		0	0	1	0	1	0	1	0

CRCINV: CRC Inverted Select.
[0]: Non-inverted. **[1]:** inverted.

WS [6:0]: Data Whitening seed setting (data encryption key).
Refer to chapter 16 for details.

9.2.36 IF Calibration Register I (Address: 23h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF Calibration I	R	--	--	--	FBCF	FB3	FB2	FB1	FB0
	W	HFR	CKGS1	CKGS0	MFBS	MFB3	MFB2	MFB1	MFB0
Reset		0	1	0	0	0	1	1	0

HFR: Half Rate setting. Recommend HFR = [0].
Clock gen = **[0]:**32xData Rate. **[1]:**16xData Rate

CKGS[1:0]: Clock genrtation data rate manual setting.
When RDU=0, CKGS[1:0] = IFS[1:0]
When RDU=1, CKGS[1:0] = Manual setting.
[00]: 1Mhz. **[01]:** 2MHz. **[10]:** 3MHZ. **[11]:** 4MHZ.

MFBS: IF filter calibration value select. Recommend MFBS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MFB [3:0]: IF filter manual calibration value.

FBCF: IF filter auto calibration flag.
[0]: Pass. **[1]:** Fail.

FB [3:0]: IF filter calibration value.
MFBS= 0: Auto calibration value (AFB),
MFBS= 1: Manual calibration value (MFB).

Refer to chapter 15 for details.

9.2.37 IF Calibration Register II (Address: 24h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IF Calibration II	R	--	--		FCD4	FCD3	FCD2	FCD1	FCD0
	W	PWORS	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
Reset		0	0	1	1	0	1	1	1

PWORS: TX high power setting.
[0]: Disable. **[1]:** Enable.

TRT [2:0]: TX Ramp down discharge current select. Recommand value=[000]

AMSV [2:0]: TX Ramp up Timing Select.
[000]: 2us, **[001]:** 4us. **[010]:** 6us. **[011]:** 8us. **[100]:** 10us, **[101]:** 12us. **[110]:** 14us. **[111]:** 16us.
Real timing is multiplied by **2^(RMP[1:0])**

AMVS: TX Ramp Up Enable.
[0]: Disable. **[1]:** Enable.

FCD [4:0]: IF filter calibration deviation from goal (Read only).

9.2.38 VCO current Calibration Register (Address: 25h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO current Calibration	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	ROSCS	RSIS	VCRLS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		0	0	0	0	0	1	0	0

ROSCS: Reserved for internal used. Recommend [0]

RSIS: Reserved for internal used. Recommend [0]

VCRLS: VCO Current Resistor Select.
[0]: low current select. **[1]:** high current select.

MVCS: VCO current calibration value select. Recommend MVCS = [1].
[0]: Auto calibration value. **[1]:** Manual calibration value.

VCOC [3:0]: VCO current manual calibration value. Recommend VCOC = [011].

VCCF: VCO Current Auto Calibration Flag.
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO current calibration value.
MVCS= 0: Auto calibration value (VCB).
MVCS= 1: Manual calibration value (VCOC).

Refer to chapter 15 for details.

9.2.39 VCO band Calibration Register I (Address: 26h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Single band Calibration I	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	DCD1	DCD0	DAGS	CWS	MVBS	MVB2	MVB1	MVB0
Reset		1	1	0	1	0	1	0	0

DCD [1:0]: VCO Deviation Calibration Delay. Recommend DCD = [01].
Delay time = PDL (Delay Register I, 17h) × (DDC + 1).

DAGS: DAG Calibration Value Select. Recommend DAGS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

CWS: Clock Disable for VCO Modulation.
[0]: Enable. **[1]:** Disable.

MVBS: VCO bank calibration value select. Recommend MVBS = [0].

[0]: Auto calibration value. **[1]:** Manual calibration value.

MVB [2:0]: VCO band manual calibration value.

VBCF: VCO band auto calibration flag.
[0]: Pass. **[1]:** Fail.

VB [2:0]: VCO bank calibration value.
MVBS= 0: Auto calibration value (AVB).
MVBS= 1: Manual calibration value (MVB).

Refer to chapter 15 for details.

9.2.40 VCO band Calibration Register II (Address: 27h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Single band Calibration II	W	DAGM7	DAGM6	DAGM5	DAGM4	DAGM3	DAGM2	DAGM1	DAGM0
	R	DAGB7	DAGB6	DAGB5	DAGB4	DAGB3	DAGB2	DAGB1	DAGB0
Reset		1	0	0	0	0	0	0	0

DAGB [7:0]: Auto DAG Calibration Value.

DAGM [7:0]: DAG Manual Setting Value. Recommend DAGM = [0x80].

9.2.41 VCO Deviation Calibration Register I (Address: 28h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Deviation Calibration I	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
Reset		0	1	1	1	0	0	0	0

DEVA [7:0]: Deviation Output Value.
MVDS (29h)= 0: Auto calibration value ((DEVC / 8) × (DEVS + 1)),
MVDS (29h)= 1: Manual calibration value (DEVM [6:0]).

DEVS [3:0]: Deviation Output Scaling. Recommend DEVS = [0011].

DAMR_M: DAMR Manual Enable. Recommend DAMR_M = [0].
[0]: Disable. **[1]:** Enable.

VMTE_M: VMT Manual Enable. Recommend VMTE_M = [0].
[0]: Disable. **[1]:** Enable.

VMS_M: VM Manual Enable. Recommend VMS_M = [0].
[0]: Disable. **[1]:** Enable.

MSEL: VMS, VMTE and DAMR control select. Recommend MSEL = [0].
[0]: Auto control. **[1]:** Manual control.

9.2.42 VCO Deviation Calibration Register II (Address: 29h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO Deviation Calibration II	R	DEVC7	DEVC6	DEVC5	DEVC4	DEVC3	DEVC2	DEVC1	DEVC0
	W	MVDS	DEVM6	DEVM5	DEVM4	DEVM3	DEVM2	DEVM1	DEVM0
Reset		0	0	1	0	1	0	0	0

DEVC [7:0]: VCO Deviation Auto Calibration Value.

MVDS: VCO Deviation Calibration Select. Recommend MVDS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

DEVM [6:0]: VCO Deviation Manual Calibration Value.

Refer to chapter 15 for details.

9.2.43 DASP0 (Address: 2Ah)(AGT [3:0]=0)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP0	W	QLIM	RFSP	INTXC (CSXTL5)	CSXTL4	CSXTL3	CSXTL2	CSXTL1	CSXTL0
Reset		0	0	0	0	0	0	0	0

QLIM: quick charge select for IF limiter amp.

[0]: disable. **[1]:** enable (QLIM fall down delay 10us)

RFSP: RF single port Select.

[1]: dual ports. **[0]:** single port.

INTXC: internal crystal oscillator capacitor selection
[0]: disable. **[1]:** enable.

CSXTAL[4:0]: On-chip Crystal loading select

{INTXC,CSXTAL[4:0]}	C load (pF)
0XXXXX	0
100000	16
100001	17
100010	18
…	
111110	46
111111	47

9.2.43 DASP1 (Address: 2Ah) (AGT[3:0]=1)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP1	W	STS	CELS	RGS	RGC1	RGC0	VRPL1	VRPL0	INTPRC
Reset		0	0	0	0	1	0	0	0

STS: Reserved for internal usage only. Shall be set to [0].
CELS:

RGS: Low Power Regulator Voltage Select.

LVR	RGS	Low Power Regulator Voltage	Note
0	0	3/5 *REGI	
0	1	3/4 * REGI	
1	0	1.8 V	Recommended
1	1	1.6 V	

RGC [1:0]: Low power band-gap current select. Recommend RGC = [01]

VRPL [1:0]: internal PLL loop filter resistor value select.
[00]: 500 ohm. **[01]:** 666 ohm. **[10]:** 1 K ohm. **[11]:** 2K ohm.

INTPRC: Internal PLL loop filter resistor and capacitor select.
[0]: disable. **[1]:** enable

9.2.43 DASP2 (Address: 2Ah) (AGT[3:0]=2)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP2	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
Reset		0	0	0	0	0	0	0	0

VTRB [3:0]: Resistor Bank for VT RC Filtering. Shall be set to [0000].

VMRB [3:0]: Resistor Bank for VM RC Filtering. Shall be set to [0000].

9.2.43 DASP3 (Address: 2Ah) (AGT[3:0]=3)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP3	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
Reset		1	0	0	0	0	0	0	0

DCV [7:0]: Demodulator Fix mode DC value. Recommend DCV = [0x80].

9.2.43 DASP4 (Address: 2Ah) (AGT[3:0]=4)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP4	W/R	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Reset		1	0	0	0	0	0	0	0

VMG [7:0]: VM Center Value for Deviation Calibration. Recommend VMG [7:0] = [0x80].

9.2.43 DASP5 (Address: 2Ah) (AGT[3:0]=5)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP5	W	--	--	PKT1	PKT0	PKS	PKIS1	PKIS0	IFPK
Reset		--	--	0	1	0	0	0	0

PKT[1:0]: VCO Peak Detect Current Select. Recommend PKT [1:0] = [01].

PKS: VCO Current Calibration Mode Select. Recommend PKS =[0].

PKIS[1:0]: AGC Peak Detect Current Select. Recommend PKIS[1:0[= [00].

IFPK: AGC Amplifier Current Select. Recommend IFPK = [0].

9.2.43 DASP6 (Address: 2Ah) (AGT[3:0]=6)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DASP6	W	--	HPLS	HRS	PACTL	IWS	CNT	MXD	LXD
Reset		--	0	0	0	0	0	0	0

HPLS: High Power LNA Gain Select.
[0]: LGC set to 6dB when in TX Mode.
[1]: LGC set to 24dB when in TX Mode.

HRS: Reserved for internal usage only. Shall be set to [0].
PACTL: Reserved for internal usage only. Shall be set to [0].
IWS: Reserved for internal usage only. Shall be set to [0].
CNT: Reserved for internal usage only. Shall be set to [0].
MXD: Reserved for internal usage only. Shall be set to [0].
LXD: Reserved for internal usage only. Shall be set to [0].

9.2.44 VCO Modulation Delay Register (Address: 2Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DMV1	DMV0	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		1	0	1	0	1	0	0	0

DMV [1:0]: Demodulator D/A Voltage Range Select. Recommend DMV = [10].
[00]: 1/32*1.2. **[01]:** 1/16*1.2. **[10]:** 1/8*1.2. **[11]:** 1/4*1.2.

DEVFD [2:0]: VCO Modulation Data Delay by 8x over-sampling Clock. Recommend DEVFD = [101].

DEVD [2:0]: VCO Modulation Data Delay by XCPCK Clock. Recommend DEVD = [000].

9.2.45 Battery detect Register (Address: 2Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Battery detect	W	LVR	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
	R	--	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

LVR: Low Power Bandgap Select. Recommend LVR = 1.

[0]: Disable. [1]: Enable.

RGV [1:0]: VDD_D and VDD_A voltage setting in non-Sleep mode. Recommend RGV = [00].
[00]: 2.1V. **[01]:** 2.0V. **[10]:** 1.9V. **[11]:** 1.8V.

BVT [2:0]: Battery voltage detect threshold.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.
[100]: 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BD_E: Battery Detect Enable.
[0]: Disable. **[1]:** Enable. It will be clear after battery detection is triggered.

BDF: Battery detection flag.
[0]: Battery voltage less than threshold. **[1]:** Battery voltage greater than threshold.

QDS: VDD_A Quick Discharge Select.
[0]: Disable. **[1]:** Enable.

Refer to chapter 18 for details.

9.2.46 TX test Register (Address: 2Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX test	W	RMP1	RMP0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		0	0	0	1	0	1	1	1

RMP [1:0]: PA ramp up timing scale. Delay scales 2^(RMP [1:0])

TXCS: TX Current Setting. [0]
[0]: lowest current. **[1]:** highest current.

PAC [1:0]: PA Current Setting. [10]

TBG [2:0]: TX Buffer Setting. [111]

Typical	Recommend setting			Typical
Output Power (dBm)	TXCS	TBG	PAC	TX current (mA)
1	0	7	3	TBD
0	0	7	1	TBD
-10	0	3	1	TBD
-20	0	1	0	TBD

Refer to chapter 19 and A7130 App. Note for more settings.

9.2.47 Rx DEM test Register I (Address: 2Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rx DEM test I	W	DMT	DCM1	DCM0	MLP1	MLP0	SLF2	SLF1	SLF0
Reset		0	1	1	0	0	1	0	0

DMT: Reserved for internal usage only. Shall be set to [0].

DCM [1:0]: Demodulator DC estimation mode.
(The average length before hold is selected by DCL in RX DEM Test Register II.)

[00]: Fix mode (For testing only). DC level is set by DCV [7:0].
[01]: Preamble hold mode. DC level is preamble average value.
[10]: ID hold mode. DC level is the average value hold about 8 bit data rate later if preamble is detected.
[11]: Payload average mode (For internal usage). DC level is payload data average.

MLP1: Preamble Amplitude Threshold Select. Shall set MLP1 = [0].
[0]: low. **[1]:** high.

MLP0: Symbol Recovery Dead Lock Detection Setting. Shall set MLP0 = [0]. Reserved

SLF [2:0]: Symbol Recovery Loop Filter Setting. Shall be SLF[2:0] = [100]. Reserved

9.2.48 Rx DEM test Register II (Address: 2Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rx DEM test II	W	-	-	DCL2	DCL1	DCL0	RAW	CDTM1	CDTM0
Reset		-	-	1	0	0	0	0	0

DCL [2]: DC Estimation Average Length After ID Detected.
[0]: 128 bits. **[1]:** 256 bits.

DCL [1:0]: DC Estimation Average Length Before ID Detected.
[00]: 8 bits. **[01]:** 16 bits. **[10]:** 32 bits. **[11]:** 64 bits.

RAW: Raw Data Output Select. Recommend RAW = [1].
[0]: latch data output. **[1]:** RAW data output.

CDTM [1:0]: Preamble carrier detect setting.

[00]: 12. [01]: 24 [10]: 36 [11]: 64.

9.2.49 Charge Pump Current Register I (Address: 30h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPC I	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	1	1	1	1

CPM [3:0]: Charge Pump Current Setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge Pump Current Setting for VT loop. Recommend CPT = [1111].
Charge pump current = (CPT + 1) / 16 mA.

9.2.50 Charge Pump Current Register II (Address: 31h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPC II	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
Reset		0	0	1	0	0	0	1	0

CPTX [3:0]: Charge Pump Current Setting for TX mode. Recommend CPTX = [0010].
Charge pump current = (CPTX + 1) / 16 mA.

CPRX [3:0]: Charge Pump Current Setting for RX mode. Recommend CPRX = [0010].
Charge pump current = (CPRX + 1) / 16 mA.

9.2.51 Crystal test Register (Address: 32h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Crystal test	W	CDPM	CPS	CPH	CPCS	DBD	XCC	XCP1	XCP0
Reset		1	1	1	1	0	1	0	1

CDPM:First Time Preamble Detect mode select. Recommend CDPM = [1]

CPS: PLL charge pump enable [1].
[0]: Enable. **[1]:** Disable.

CPH: Charge Pump High Current. Shall be set to [0].
[0]: Normal. **[1]:** High.

CPCS: Charge Pump Current Select. Shall be set to [0].
[0]: Use CPM for TX, CPT for RX.
[1]: Use CPTX for TX, CPRX for RX.

DBD: Crystal Frequency Doubler High Level Pulse Width Select. Recommend DBD = [0].
[0]: about 8 ns. **[1]:** about 16 ns.

XCC: Crystal Startup Current Selection. Recommend XCC = [1].
[0]: about 0.7 mA. **[1]:** about 1.5 mA.

XCP [1:0]: Crystal Oscillator Regulated Couple Setting. Recommend XCP = [01].
[00]: 1.5mA. **[01]:** 0.5mA. **[10]:** 0.35mA. **[11]:** 0.3mA.

9.2.52 PLL test Register (Address:33h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL test	W	MDEN	OLM	PRIC1	PRIC0	PRRC1	PRRC0	SDPW	NSDO
Reset		0	0	0	1	0	0	0	0

MDEN : Use for Manual VCO Calibration. Shall be set to [0].

OLM: Open Loop Modulation Enable. Shall be set to [0].
[0]: Disable. **[1]:** Enable.

PRRC [1:0]: Prescaler RF Part Current Setting. Shall be set to [00].
[00]: 1.0mA. **[01]:** 1.2mA. **[10]:** 1.4mA. **[11]:** 1.6mA.

PRIC [1:0]: Prescaler IF Part Current Setting. Shall be set to [01].
[00]: 0.95mA. **[01]:** 1.05mA. **[10]:** 1.15mA. **[11]:** 1.25mA.

SDPW: Clock Delay For Sigma Delta Modulator. Shall be set to [0].
[0]: 13 ns. **[1]:** 26 ns.

NSDO: Sigma Delta Order Setting. Shall be set to [1].
[0]: order 2. **[1]:** order 3.

9.2.53 VCO test Register I (Address:34h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCO test I	W	DEVGD2	DEVGD1	DEVGD0	TLB1	TLB0	RLB1	RLB0	VBS
Reset		0	0	0	0	0	0	0	0

DEVGD [2:0]: Sigma Delta Modulator Data Delay Setting. Recommend DEVGD = [000].

TLB [1:0]: LO Buffer Current Select. Shall be set to [00].
[00]: 0.6mA. **[01]:** 0.75mA. **[10]:** 0.9mA. **[11]:** 1.05mA.

RLB [1:0]: RF divider Current Select. Shall be set to [00].
[00]: 1.2mA. **[01]:** 1.5mA. **[10]:** 1.8mA. **[11]:** 2.1mA.

VBCS : VCO Buffer Current Setting. Shall be set to [0].
[0]: 1mA. **[1]:** 1.5mA.

9.2.54 RF Analog Test Register (Address: 35h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFT	W	AGT3	AGT2	AGT1	AGT0	RFT3	RFT2	RFT1	RFT0
Reset		0	0	0	0	0	0	0	0

AGT[3:0]:Page select.

AGT[3:0]	Address:2Ah	Address:38h
0	DASP0	ROMP0

1	DASP1	ROMP1
2	DADP2	ROMP2
3	DASP3	ROMP3
4	DASP4	ROMP4
5	DASP5	
6	DASP6	

RFT [3:0]: RF analog pin configuration for testing. Recommend RFT= [0000].

9.2.55 Key data Register (Address: 36h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Key Data	R	KEYO7	KEYO6	KEYO5	KEYO4	KEYO3	KEYO2	KEYO1	KEYO0
	W	KEYI7	KEYI6	KEYI5	KEYI4	KEYI3	KEYI2	KEYI1	KEYI0
Reset		0	0	0	0	0	0	0	0

KEYI [7:0]: Encryption key data. (Write only).

KEYO [7:0]: Encryption or decryption key data. (Read only). Select by KEYOS (bit3, address 3E)
Total 16 bytes length.

9.2.56 Channel Selct Register (Address: 37h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Channel Selct	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
Reset		0	0	0	1	0	1	0	1

CHI [3:0]: Auto IF Offset Channel Number Setting.
$F_{CHSP} \times (CHI + 1) = F_{IF}$
Refer to chapter 14 for F_{CHSP} setting.

CHD [3:0]: Channel Frequency Offset for Deviation Calibration.
Offset channel number = +/- (CHD + 1).

9.2.57 ROMP0 (Address: 38h)(AGT[3:0]=0)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ROMP0	W	MPOR	EPRG	MIGS	MRGS	MRSS	MTMS	MADS	MBGS
Reset		0	0	0	0	0	0	0	0

MPOR: manual SPI read in OTP program cycle.

EPRG: enable OTP program.
[0]: disable. **[1]:** enable.

MIGS: IF gain setting select.
[0]: SPI setting. **[1]:** OTP setting.

MRGS: LNA and mixer gain setting select.
[0]: SPI setting. **[1]:** OTP setting.

MRSS: RSSI voltage fine trim setting select.
[0]: SPI setting. **[1]:** OTP setting.

MTMS: Temp voltage fine trim setting select.
[0]: SPI setting. **[1]:** OTP setting.

MADS: ADC voltage fine trim setting select.
[0]: SPI setting. **[1]:** OTP setting.

MBGS: Bandgap voltage fine trim setting select.
[0]: SPI setting. **[1]:** OTP setting.

9.2.57 ROMP1 (Address: 38h)(AGT[3:0]=1)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	APG	MPA1	MPA0	FBG4	FBG3	FBG2	FBG1	FBG0
Reset		0	0	0	1	0	0	0	0

APG: OTP program select.
[1]: auto program. **[0]:** manual SPI setting.

MPA [1:0]: OPT address setting in manual SPI OTP program.

FBG [4:0]: Bandgap voltage SPI fine trim setting.

9.2.57 ROMP2 (Address: 38h)(AGT[3:0]=2)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	PTM1	PTM0	CTR4	CTR3	CTR2	CTR1	CTR0
Reset		0	0	0	1	0	0	0	0

PTM [1:0]: OTP program operation mode select. Recommend PTM = [00].

CTR [5:0]: ADC voltage SPI fine trim setting.

9.2.57 ROMP3 (Address: 38h)(AGT[3:0]=3)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	CRS2	CRS1	CRS0	SRS2	SRS1	SRS0
Reset		0	0	1	0	0	1	0	0

SRS [2:0]: RSSI voltage curve slope fine time setting.

CTS [2:0]: RSSI voltage offset fine trim setting.

9.2.57 ROMP4 (Address: 38h)(AGT[3:0]=4)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	STMP	STM5	STM4	STM3	STM2	STM1	STM0
Reset		0	0	1	0	0	0	0	0

STMP: Temp voltage ADC reading select.
[0]: 1 scale / degree C. **[1]:** 2 scale/degree C.

CTR [4:0]: ADC voltage fine trim setting.

9.2.58 Data Rate Clock Register (Address: 39h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Rate Clock	W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset		0	0	0	0	0	0	0	0

SDR [1:0]: Data Rate Setting.
Data rate = F_{IF} / (SDR+1).

Data Rate	F_{IF} (Hz)	SDR [7:0]
4M	4MHz	TBD
3M	3MHz	TBD

9.2.59 FCR Register (Address: 3Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FCR	R	ARTEF	VPOAK	RCR3	RCR2	RCR1	RCR0	EAK	EAR
	W	FCL1	FCL0	ARC3	ARC2	ARC1	ARC0	EAK	EAR
Reset		0	0	0	1	1	0	0	0

ARTEF : Auto re-transmission ending flag.
[0]: re-reansmission not end **[1]:** re-transmission end

VPOAK : Valid Packet or ACK OK Flag. (Strobe command reset)
[0]: Neither valid packet nor ACK OK. **[1]:** Valid packet or ACK OK.

RCR [3:0] : Decremental of ARC[3:0].

ARC [3:0] : Auto Resend Cycle Setting.
[0000]: no resend. **[0001]:** 1 **[0010]:** 2 **[0011]:** 3 **[0100]:** 4 **[0101]:** 5 **[0110]:** 6 **[0111]:** 7 **[1000]:** 8 **[1001]:** 9
[1010]: 10 **[1011]:** 11 **[1100]:** 12 **[1101]:** 13 **[1110]:** 14 **[1111]:** 15

FCL [1:0] : Frame Control Length.
[00]: No Frame Control
[01]: 1 byte Frame Control. (FCB0), refer to 3Dh.
[10]: 2 byte Frame control. (FCB0+FCB1), refer to 3Dh.
[11]: 4 byte Frame control. (FCB0+FCB1+FCB2+FCB3), refer to 3Dh.

EAK : Enable Auto ACK.
[0]: Disable. **[1]:** Enable.

EAR : Enable Auto Resend.
[0]: Disable. **[1]:** Enable.

9.2.60 ARD Register (Address: 3Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ARD	W	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
Reset		0	0	0	0	0	0	1	1

ARD[7:0] : Auto Resend Delay
ARD Delay = 200 us * (ARD+1) → (200us ~ 51.2 ms)

[0000-0000]: 200 us.
[0000-0001]: 400 us.
[0000-0010]: 600 us.
…
…
[1111-1111]: 51.2 ms.

9.2.61 AFEP Register (Address: 3Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AFEP	R	0	0	EARTS2	EARTS1	EARTS0	SID2	SID1	SID0
	W	EAF	SPSS	ACKFEP 5	ACKFEP 4	ACKFEP 3	ACKFEP 2	ACKFEP 1	ACKFEP 0
Reset		1	1	0	0	0	0	1	1

EAF: Enable ACK FIFO.
[0]: Disable. **[1]:** Enable.

SPSS : Mode Back Select for Auto ACK/Resend.
[0]: Standby mode. **[1]:** PLL mode.

ACKFEP [5:0]: FIFO End Point for Auto ACK.
ACK FIFO Length = (ACKFEP[5:0] + 1), max. 64 bytes.

EARTS [2:0]: Enable Auto Resend Read. Reserved.

9.2.62 FCB Register (Address: 3Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FCB	R/W	FCB7	FCB6	FCB5	FCB4	FCB3	FCB2	FCB1	FCB0
Reset		0	0	0	0	0	0	0	0

FCB [7:0]: Frame Control Buffer
Length of Frame Control Buffer is set by FCL (3Ah), max 4 bytes (FCB0 ~ FCB3)

Programmable FCB (Max 4 bytes)			
FCB0	FCB1	FCB2	FCB3
For Auto ACK/Resend	User definition (default value is 0x00)		

FCB0							
0	0	1	1	1	**SID2**	**SID1**	**SID0**

SID [2:0]: Serial Package ID.
The transmitter increments the SID field each time it generates a new packet and uses the same SID on packets that are retransmitted.

Be notice, to write FCB,
If FCL=[00], no frame control buffer. (auto resend/ACK are inactive.)
If FCL=[01], FCB= (FCB0), the device ignores input data.
If FCL=[10], FCB= (FCB0+FCB1), user can define 2 bytes data to FCB and the first byte is a dummy byte.
If FCL=[11], FCB= (FCB0+FCB1+FCB2+FCB3), user can define 4 bytes data to FCB and the first byte is a dummy byte.

Refer to chapter 20 for details.

9.2.62 KEYC Register (Address: 3Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KEYC	W	KEYOS	AFIDS	ARTMS	MIDS	AESS		AKFS	EDCRS
Reset		0	0	0	0	0	0	0	0

EDRCS: Data encrypt or decrypt selection.
[0]: Disable. **[1]:** Enable.

AKFS: Data packet with decrypted key appendixes selection.(NOTE):set EDRL=1 when FCL,AFIDS,EACKF=0.
[0]: Disable. **[1]:** Enable.

MEDCS: Manual encryption or decryption selection.
[0]: Disable. **[1]:** Enable.

AESS: encryption format selection.
[1]: Standard AES 128 bit. **[0]:** proprietary 32 bit.

MIDS: FIFO control byte address mapping for FIFO ID select..
[0]: Revieved device ID. **[1]:** internal FIFO control byte ID

ARTMS: auto retransmission interval mode select.
[0]: random interval. **[1]:** fixed interval.

AFIDS: FIFO ID appendixes selection.
[0]: Disable. **[1]:** Enable.

9.2.63 USID Register (Address: 3Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ICD7	ICD6	ICD5	ICD4	ICD3	ICD2	ICD1	ICD0
	W	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0

Reset		0	0	0	0	1	0	0	0

RND [7:0]: Random seed for auto retransmission interval.

USID [7:0]: Unique Security ID. Total 4 bytes.

10. SPI

A7130 only supports one SPI interface with maximum data rate up to 10Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A7130. Via SPI interface, user can access **control registers** and issue **Strobe command**. Figure 10.1 gives an overview of SPI access manners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1/GIO2) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 (or GIO2) pin is data output. In such case, GIO1S (0bh) or GIO2S (0ch) should be set to [0110].

For SPI write operation, SDIO pin is latched into A7130 at the rising edge of SCK. For SPI read operation, if input address is latched by A7130, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A7130's internal state machine, it is very easy to send Strobe command via SPI interface. The Strobe command is a unique command set with total 8 commands. See section 10.3, 10.4 and 10.5 for details.

	SPI chip select	Data In	Data Out
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110)

Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A7130 the following instruction is "Strobe command" or "control register". See Table 10.1 for SPI format. Based on Table 10.1, To access control registers, just set A7=0, then A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 (3-wire SPI) and Figure 10.3 (4-wire SPI) for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

Bit 7: Command bit
[0]: Control registers.
[1]: Strobe command.

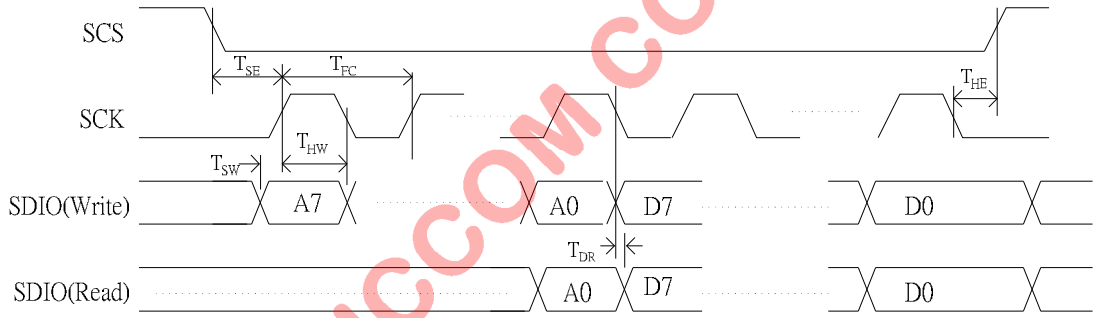
Bit 6: R/W bit
[0]: Write data to control register.
[1]: Read data from control register.

Bit [5:0]: Address of control register

Data Byte:
Bit [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI interface is configured, the maximum SPI data rate is 10 Mbps. To active SPI interface, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for SPI timing characteristic.



Parameter	Description	Min.	Max.	Unit
F_C	FIFO clock frequency.		10	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI interface read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

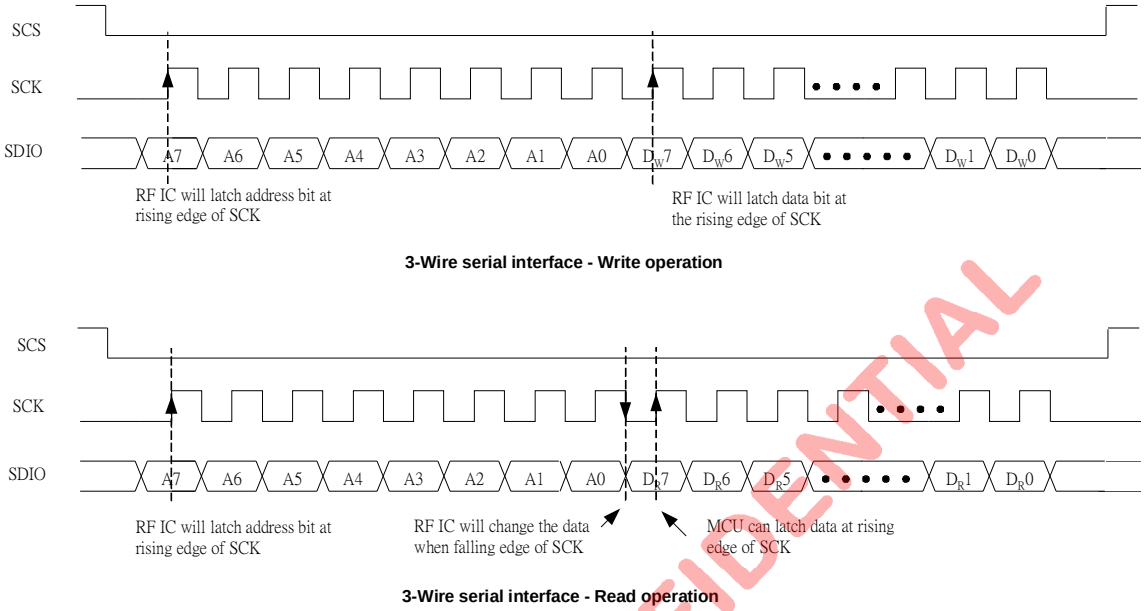


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI

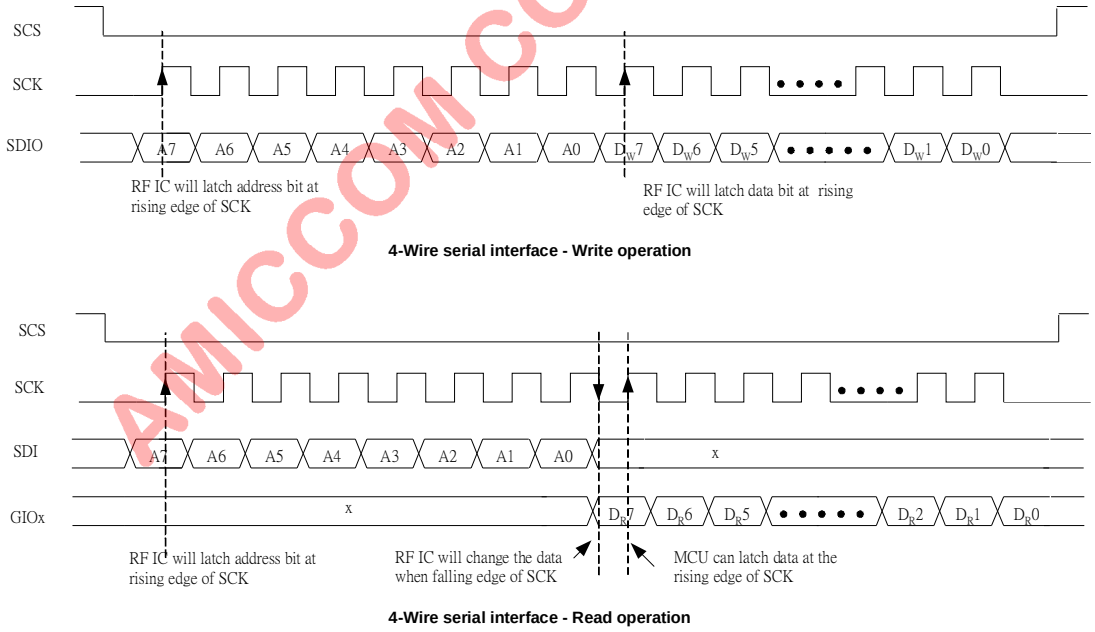


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A7130 supports 8 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	X	x	x	Sleep mode
1	0	0	1	x	X	x	x	Idle mode
1	0	1	0	x	X	x	x	Standby mode
1	0	1	1	x	X	x	x	PLL mode
1	1	0	0	x	X	x	x	RX mode
1	1	0	1	x	X	x	x	TX mode
1	1	1	0	x	X	x	x	FIFO write pointer reset
1	1	1	1	x	X	x	x	FIFO read pointer reset

Table 10.3 Strobe Commands by SPI interface

10.4.1 Strobe Command - Sleep Mode

Refer to Table 10.3 user can issue 4 bits (1000) Strobe command directly to set A7130 into Sleep mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	X	x	x	Sleep mode

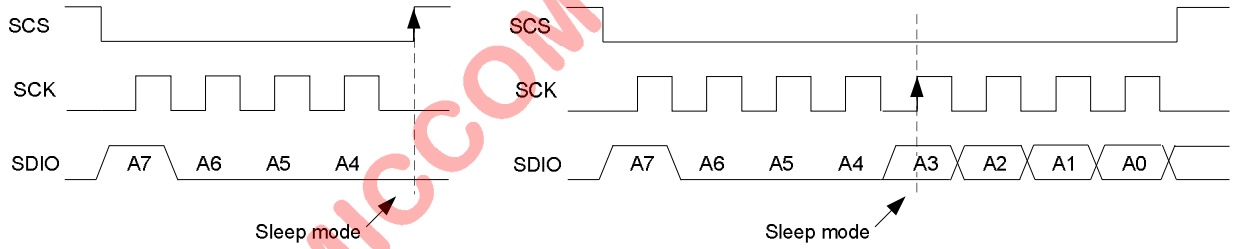


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe command directly to set A7130 into Idle mode. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	X	x	x	Idle mode

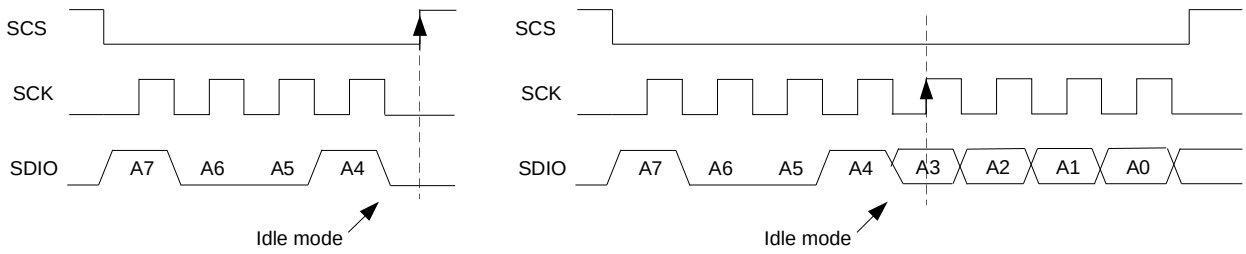


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe command directly to set A7130 into Standby mode. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	X	x	x	Standby mode

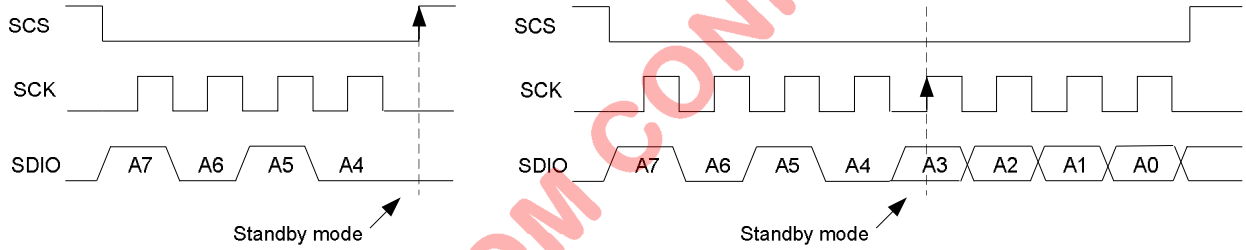


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe command directly to set A7130 into PLL mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	X	x	x	PLL mode

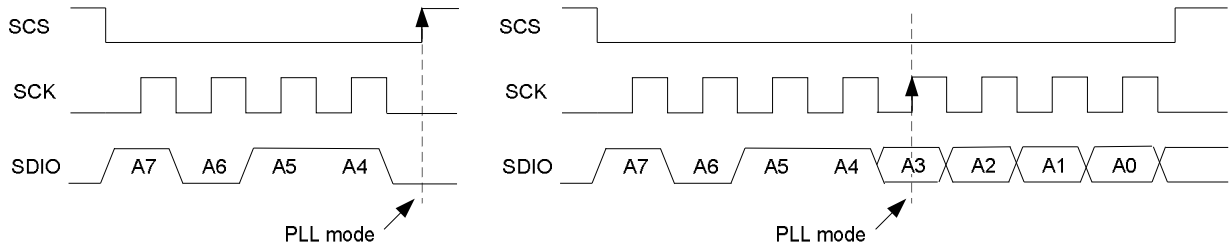


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - RX Mode

Refer to Table 10.3, user can issue 4 bits (1100) Strobe command directly to set A7130 into RX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	x	X	x	x	RX mode

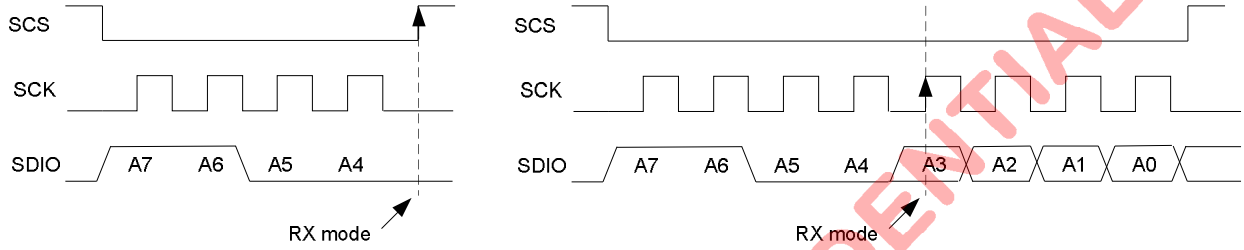


Figure 10.8 RX mode Command Timing Chart

10.4.6 Strobe Command - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe command directly to set A7130 into TX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

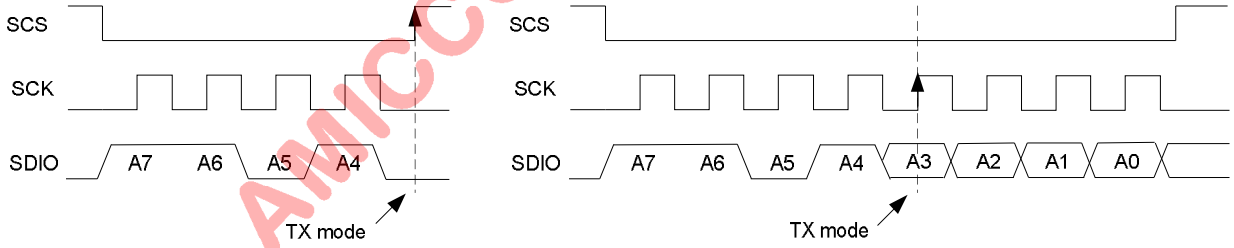


Figure 10.9 TX mode Command Timing Chart

10.4.7 Strobe Command – FIFO Write Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1110) Strobe command directly to reset A7130 FIFO write pointer. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	FIFO write pointer reset

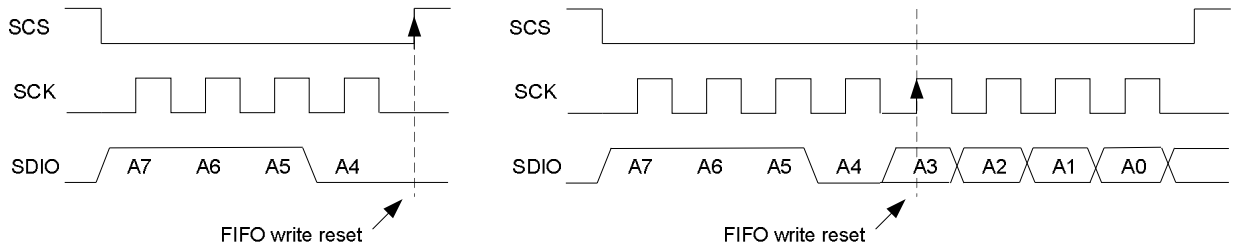


Figure 10.10 FIFO write pointer reset Command Timing Chart

10.4.8 Strobe Command – FIFO Read Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1111) Strobe command directly to reset A7130 FIFO read pointer. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	1	x	x	x	x	FIFO read pointer reset

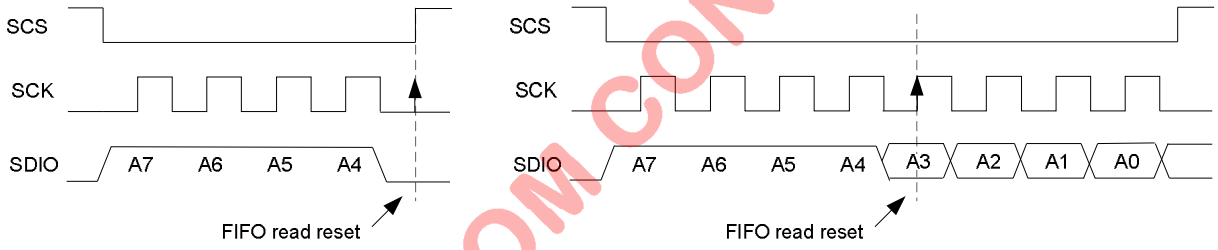


Figure 10.11 FIFO read pointer reset Command Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A7130 by setting Mode Register (00h) through SPI interface as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A7130 is informed to generate internal signal “RESETN” to initial itself. After reset command, A7130 is in standby mode and calibration procedure shall be issued again.

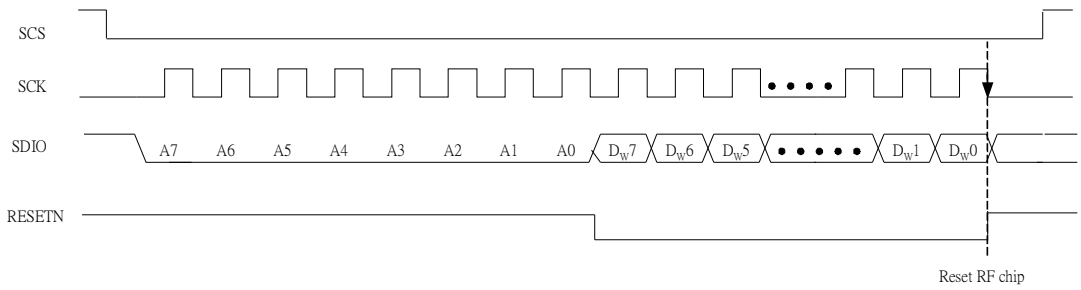


Figure 10.12 Reset Command Timing Chart

10.6 ID Accessing Command

A7130 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI interface. ID length is recommended to be 32 bits by setting IDL (1Fh). Therefore, user can toggle SCS pin to high to terminate ID accessing command when ID data is output completely.

Figure 10.13 and 10.14 are timing charts of 32-bits ID accessing via 3-wire SPI.

10.6.1 ID Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of ID write command.

Step1: Deliver A7~A0 = 00000110 (A6=0 for write, A5~A0 = 000110 for ID addr, 06h).
Step2: By SDIO pin, deliver 32-bits ID into A7130 in sequence by Data Byte 0 **(recommend 5xh or Axh)**, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

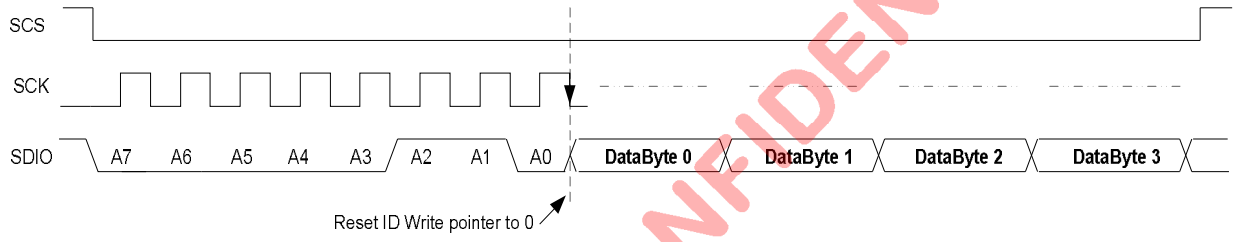


Figure 10.13 ID Write Command Timing Chart

10.6.2 ID Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of ID read command.

Step1: Deliver A7~A0 = 01000110 (A6=1 for read, A5~A0 = 000110 for ID addr, 06h).
Step2: SDIO pin outputs 32-bits ID in sequence by Data Byte 0, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

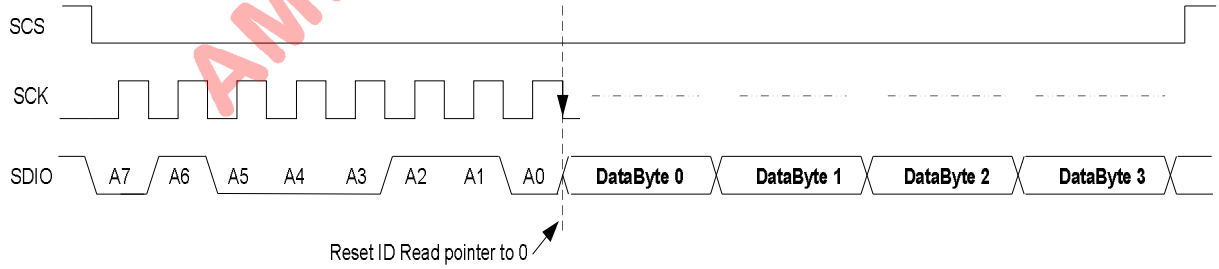


Figure 10.14 ID Read Command Timing Chart

10.7 FIFO Accessing Command

To use A7130's FIFO mode, enable FMS (01h) =1 via SPI interface. Before TX delivery, just write wanted data into TX FIFO (05h) then issue TX Strobe command. Similarly, user can read RX FIFO (05h) once payload data is received.

MCU can use polling or interrupt scheme to do FIFO accessing. FIFO status can output to GIO1 (or GIO2) pin by setting GIO1S (0Bh) or GIO2S (0Ch).

Figure 10.15 and 10.16 are timing charts of FIFO accessing via 3-wire SPI.

10.7.1 TX FIFO Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of TX FIFO write command.

Step1: Deliver A7~A0 = 00000101 (A6=0 for write control register and issue FIFO A [5:0] = 05h).
Step2: By SDIO pin, deliver (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send Strobe command of TX mode (Figure 10.9) to do TX delivery.

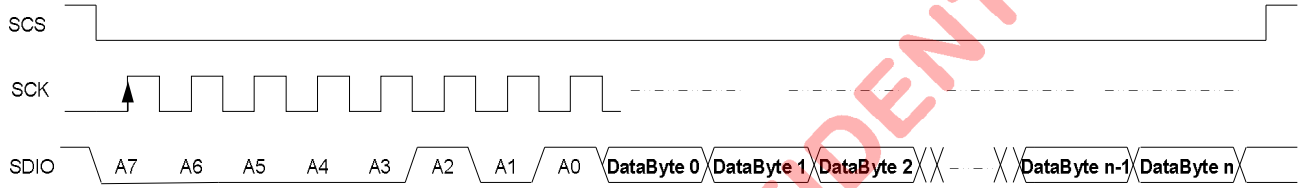


Figure 10.15 TX FIFO Write Command Timing Chart

10.7.2 Rx FIFO Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of RX FIFO read command.

Step1: Deliver A7~A0 = 01000101 (A6=1 for read control register and issue FIFO at address 05h).
Step2: SDIO pin outputs RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when RX FIFO is read completely.

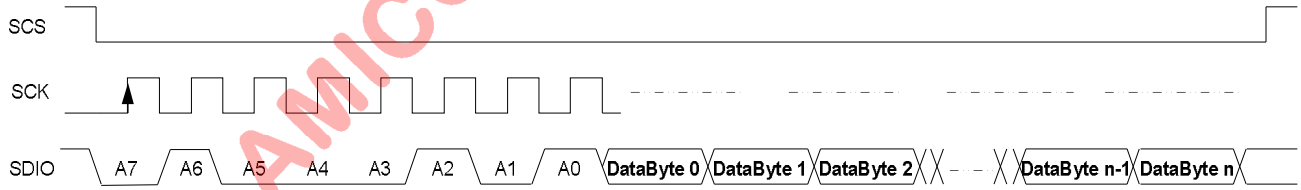


Figure 10.16 RX FIFO Read Command Timing Chart

11. State machine

In chapter 9 and chapter 10, user can not only learn A7130's control registers but also know how to issue Strobe command. From section 10.2 ~ 10.6, it is clear to know configurations of 3-wire SPI and 4-wire SPI, Strobe command, software reset, and how to access ID Registers as well as TX/RX FIFO.

Section 11.1 introduces 7 states of built-in state machine. Combined with Strobe command and accessing control registers, section 11.2, 11.3 and 11.4 demonstrate 3 state diagrams to explain how transitions of A7130's operation.

From accessing data point of view, if FMS=1 (01h), FIFO mode is enabled, otherwise, A7130 is in direct mode. If FMS=1 and FIFO Read/Write in Standby mode, we call it Normal FIFO mode. Otherwise, If FMS=1 and FIFO Read/Write in PLL mode,

we called it Quick FIFO mode due to the time reduction of PLL settling. If FMS=1 and FIFO Read/Write in IDLE mode, we called it Power Saving FIFO mode due to the reduction of average current.

	SPI chip select	Data In	Data Out	Operation Mode	Clock Recovery for Direct Mode
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin	FIFO (FMS=1) Direct (FMS=0)	CKO pin (CKOS = 0001)
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110)	FIFO (FMS=1) Direct (FMS=0)	CKO pin (CKOS = 0001)

(1) Normal FIFO Mode (FMS=1 and FIFO R/W @ Standby mode)
(2) Quick FIFO Mode (FMS=1 and FIFO R/W @ PLL mode)
(3) Power Saving FIFO Mode (FMS=1 and FIFO R/W @ IDLE mode)
(4) Quick Direct Mode (FMS=0 and FIFO ignored, write packet @ TX mode, read packet @ RX mode)

11.1 Key states

A7130 supports 7 key operation states. Those are,
(1) Standby mode
(2) Sleep mode
(3) Idle mode
(4) PLL mode
(5) TX mode
(6) RX mode
(7) CAL mode

After power on reset or software reset, A7130 is in standby mode. User has to do calibration process because all control registers are in initial values. The calibration process is very easy, user only needs to issue Strobe commands and enable calibration registers. Then, check the calibration flag because it is done automatic by internal state machine. Refer to 11.2, 11.3, 11.4 and chapter 15 for details. After calibration, A7130 is ready to do TX and RX operation.

11.1.1 Standby mode

If Standby Strobe command is issued, A7130 enters standby mode automatically. Internal power management is listed below. Be notice, A7130 is in standby mode once power on reset or software reset occurs.

Standby mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	OFF	OFF	OFF	OFF	1010xxxxb See Figure 10.6

11.1.2 Sleep mode

If Sleep Strobe command is issued, A7130 enters sleep mode automatically. In sleep mode, A7130 still can accept MCU's commands via SPI interface. But, NOT support to Read/Write FIFO. Internal power management is listed below.

Sleep mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
OFF	OFF	OFF	OFF	OFF	OFF	1000xxxxb See Figure 10.4

11.1.3 Idle mode

If Idle Strobe command is issued, A7130 enters idle mode automatically. In idle mode, A7130 can accept MCU's commands via SPI interface as well as supporting Read/Write FIFO. Internal power management is listed below.

Idle mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	OFF	OFF	OFF	OFF	OFF	1001xxxxb See Figure 10.5

11.1.4 PLL mode

If PLL Strobe command is issued, A7130 enters PLL mode automatically. In PLL mode, internal PLL and VCO are both turned on to generate LO (local oscillator) frequency before TX and RX operation. Internal power management is listed below. According to PLL Register I, II, III, IV and V, PLL circuitry is easy to be controlled by user's definition.

PLL mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	OFF	1011xxxxb See Figure 10.7

11.1.5 TX mode

If TX Strobe command is issued, A7130 enters TX mode automatically for data delivery. Internal power management is listed below.
(1) In FIFO mode, once TX data packet (Preamble + ID + Payload) is delivered, A7130 supports auto-back function to previous state for next delivered packet.

(2) In Direct mode, once TX data packet is delivered, A7130 stays in TX mode. User has to issue Strobe command to back to previous state.

TX mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	ON	(1101xxxx)b See Figure 10.9

11.1.6 RX mode

If RX Strobe command is issued, A7130 enters RX mode automatically for data receiving. Internal power management is listed below.
(1) In FIFO mode, once RX data packet (Preamble + ID + Payload) is received completely, A7130 supports auto-back function to previous state for next receiving packet.

(2) In Direct mode, once RX data packet is received, A7130 stays in RX mode. User has to issue Strobe command to back to previous state.

RX mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	ON	OFF	(1101xxxx)b See Figure 10.9

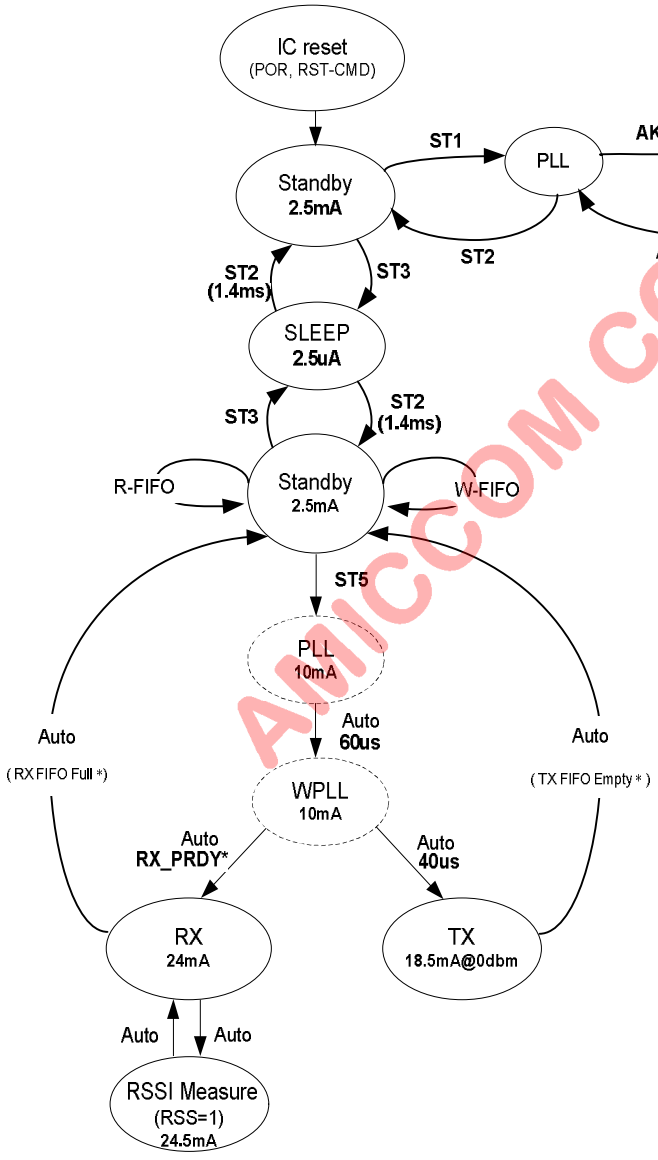
11.1.7 CAL mode

Calibration process shall be done after power on reset or software reset. Calibration items include VCO and IF Filter. It is easy to implement calibration process by Strobe command and enable CALC (02h) control register. See chapter 15 for details.

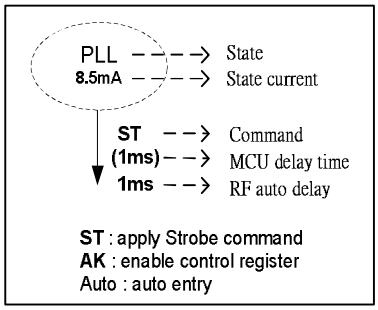
Be notice, VCO Calibration is only executable in PLL mode. However, IF Filter Calibration can be executed in Standby or PLL mode.

11.2 Normal FIFO Mode

This mode is suitable for requirement of general purpose applications. After calibration flow, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet transmission, only one Strobe command is needed. Once transmission is done, A7130 is auto back to standby mode. If all packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7130 staying in sleep mode. Figure 11.1 is the state diagram of Normal FIFO mode.



SYMBOL EXPLAIN



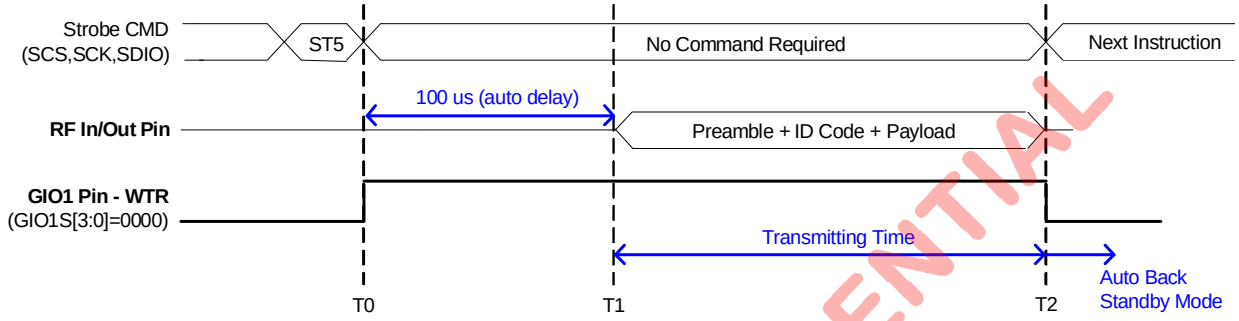
CAL CMD	CMD Value	Calibration	Section
AK	CALC.0=1.	IF Filter	15.2
	CALC.1=1.	VCO Band	15.3
	CALC.2=1.	VCO Current	15.4

Strobe	CMD Value	Note	Section
ST1	1011b	Enter to PLL	10.4.4
ST2	1010b	Enter to Standby	10.4.3
ST3	1000b	Enter to SLEEP	10.4.1
ST4	1001b	Enter to IDLE	10.4.2
ST5-TX	1101b	Enter to TX	10.4.6
ST5-RX	1100b	Enter to RX	10.4.5
RST-CMD	00000000b	Software Reset	10.5

- Refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.
- See Table 11.3 (next page) for RX-PRDY.

Figure 11.1 State diagram of Normal FIFO Mode

From Figure 11.1, when ST5 command is issued for TX operation, see Figure 11.2 for detailed timing. A7130 status can be represented to GIO1 or GIO2 pin to MCU for timing control.

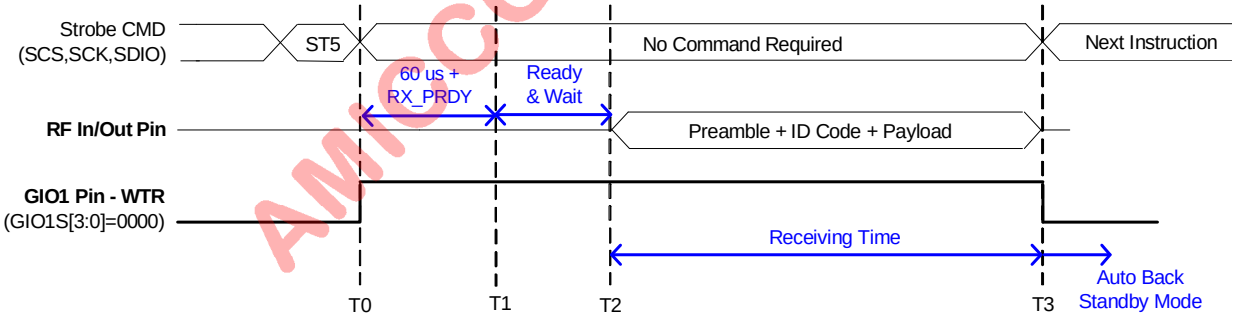


T0-T1: Auto Delay by Register setting

LO Freq.	Standby to WPLL	WPLL to TX	TX Ready Time
Changed	60 us	40 us	100 us
No Changed	60 us	40 us	100 us

Figure 11.2 Transmitting Timing Chart of Normal FIFO Mode

From Figure 11.1, when ST5 command is issued for RX operation, see Figure 11.3 for detailed timing. A7130 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



T0-T1: Delay by MCU
T1-T2: RX is ready, Wait for valid packet

Figure 11.3 Receiving Timing Chart of Normal FIFO Mode

12 Crystal Oscillator

A7130 needs external crystal or external clock that is either 6 or 8/12/16/20/24 MHz to generate internal wanted clock. Be noted if external clock is equal or lower than 8MHz, A7130 only supports data rate up to 250K.

Relative Control Register

Clock Register (Address: 0Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clock	R/W	GRC3	GRC2	GRC1	GRC0	CSC1	CSC0	CGS	XS
Reset		1	1	1	1	0	1	0	1

12.1 Use External Crystal

Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance are used to adjust different crystal loading. A7130 supports crystal accuracy within ±20 ppm under firmware frequency compensation. Be noted that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

A7130	Crystal Accuracy	Crystal ESR
Firmware FC = On	±20 ppm	≦80 ohm
Firmware FC = Off	±10 ppm	≦80 ohm

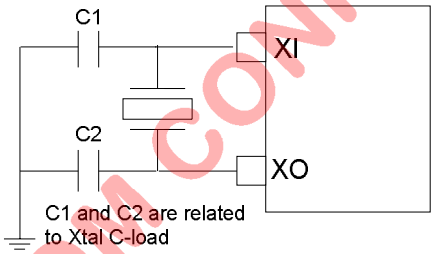


Fig12.1 Crystal oscillator circuit, refer to A7130 App. Note for C1 and C2.

12.2 Use external clock

A7130 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. In such case, XI pin is left opened. XS shall be low (0Dh) for selecting external clock. The frequency accuracy of external clock shall be controlled within ± 20 ppm, and the amplitude of external clock shall be within 1.2 ~ 1.8 V peak-to-peak.

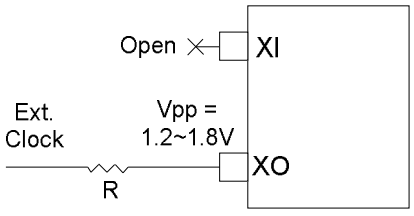


Fig12.2 External clock source. R is used to tune Vpp = 1.2~1.8V

13. System Clock

A7130 supports different crystal frequency by programmable "Clock Register". Based on this, three important internal clocks F_{CGR} , F_{DR} and F_{SYCK} are generated.

(1) F_{XTAL}: Crystal frequency.
(2) F_{XREF}: Crystal Ref. Clock = F_{XREF} * (DBL+1).
(3) F_{CGR}: Clock Generation Reference = 2MHz = F_{XREF} / (GRC+1), where F_{CGR} is used to generate 32M PLL.
(4) F_{MCLK}: Master Clock is either F_{XREF}: or 32M PLL, where F_{MCLK} is used to generate F_{SYCK}.
(5) F_{SYCK}: System Clock = 16MHz=F_{MCLK} / CSC= 32 * F_{IF}, where F_{IF} is recommended to set 500KHz.
(6) F_{DR}: Data Rate Clock = F_{IF} / (SDR+1).
(7) F_{FPD}: VCO Compared Clock = = F_{XREF} / (RRC+1).

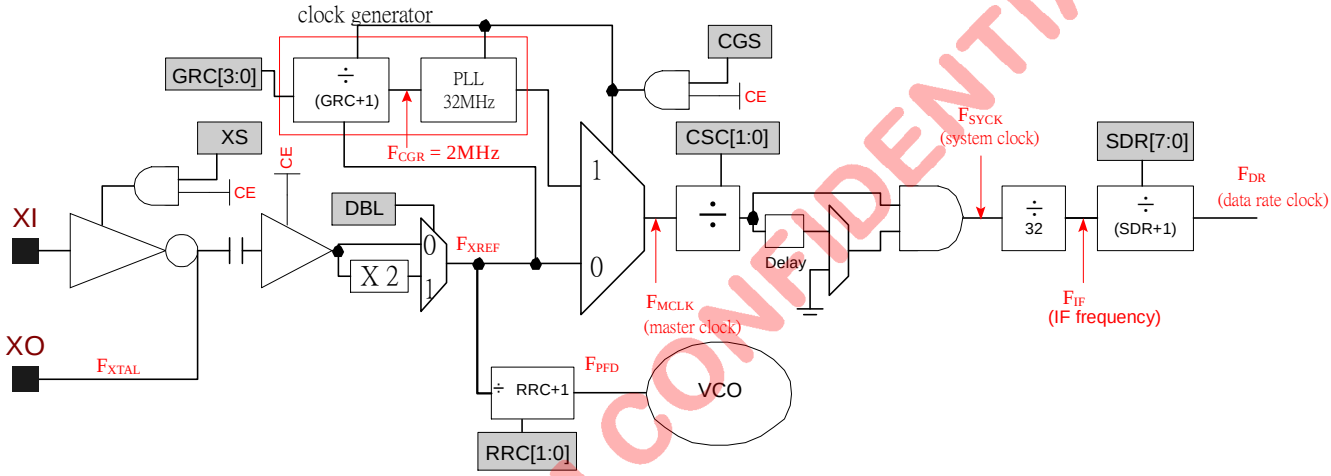


Fig13.1 System clock block diagram

As show in Fig 13.1, $F_{MCLK,}$ the master clock either come from F_{XREF} (CGS = 0) or PLL 32MHz (CGS = 1). The relation between F_{SYCK} (the system clock) and F_{MCLK} (master clock) show in table 13.1

F_{SYCK} (Master Clock)		
	CGS = 0	CGS = 1
DBL=0	F_{XTAL}	32 MHz
DBL=1	**2 * F_{XTAL} (Recommend)**	32 MHz

CSC [1:0]	**F_{SYCK} (system clock)**	**Note**
00	F_{MCLK}	F_{SYCK} is used to determine 1. Data rate clock 2. ADC clock 3. Internal digital clock 4. CKO pin
01	F_{MCLK} /2	
10	F_{MCLK} /2	
11	F_{MCLK} /4	

Table 13.1 System clock and master clock

13.1 Bypass clock generation

If crystal frequency is multiplier of 8MHz, the clock generator block can be turned off by setting CGS = 0.The relation between F_{XTAL} (crystal frequency) and data rate show below:

F_{XREF} = F_{XTAL} * (DBL+1)
F_{PFD} = F_{XREF} / (RRC [1:0]+1)
F_{DR} = F_{XREF} / (CSC [1:0]+1) / 32 / (SDR+1)

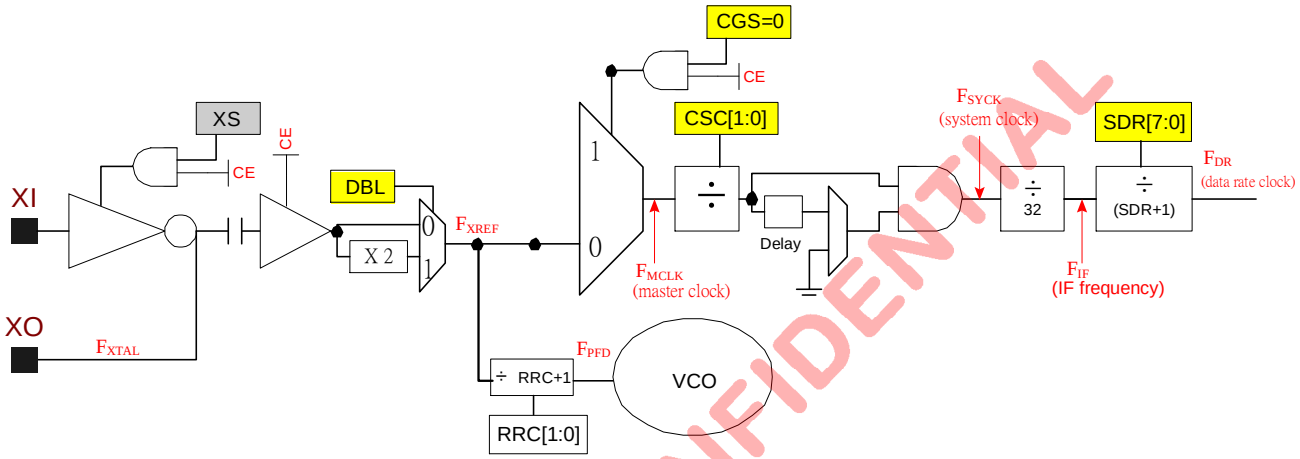


Fig13.2 By pass clock generator to get system clock

For various data rate application, list some examples below.
For more data rate options, please contact AMICCOM FAE team.

13.2 Enable clock generation

If crystal frequency is the multiplier of 2MHz and larger than 6MHz, set CGS = 1 to enable **F_{SYCK}**= 32MHz (internal 32MHz PLL). The comparison frequency of clock generator F_{CGR} shall be 2MHz by setting GRC[3:0] to meets the below equations.
F_{CRG} = F_{XTAL} * (1+DBL) / (GRC+1) = 2MHz.
F_{DR} = F_{SYCK} / 32 / (SDR+1).

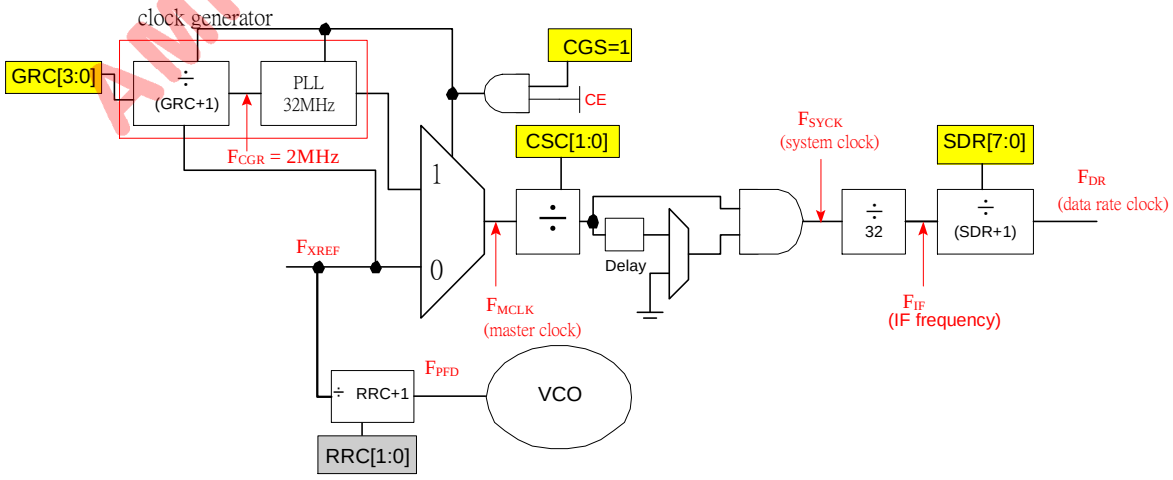


Fig13.3 Enable clock generator to get system clock

14. Transceiver LO Frequency

A7130 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO (Local Oscillator) frequency for two ways radio transmission.

To target full range of 2.4GHz ISM band (2400 MHz to 2483.5 MHz), A7130 applies offset concept by LO frequency **F_{LO} = F_{LO_BASE} + F_{OFFSET}**. Therefore, this device is easy to implement frequency hopping and multi-channels by just **ONE** register setting, **PLL Register I (CHN [7:0], 0Eh).**

Below is the LO frequency block diagram.

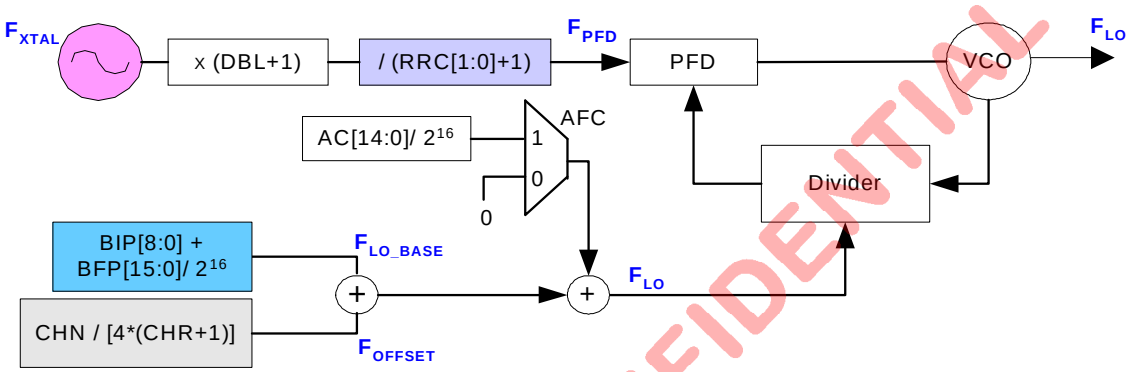


Fig14.1 Frequency synthesizer block diagram

14.1 LO Frequency Setting

From Figure 14.1, F_{LO} is not only for TX radio frequency but also to be RX LO frequency. To set up $F_{LO,}$ it is easy to implement by below 4 steps.

1. Set the base frequency (F_{LO_BASE}) by PLL Register II, III, IV and V.
   Recommend to set F_{LO_BASE} ~ 2400.001MHz.
2. Set the channel step (F_{CHSP}) by PLL Register II.
   F_{CHSP} = F_{XTAL} * (DBL+1) / 4 / (CHR+1), Recommend F_{CHSP} = 500 KHz.
3. Set CHN [7:0] to get offset frequency by PLL Register I.
   F_{OFFSET} = CHN [7:0] x F_{CHSP}
4. LO frequency is equal to base frequency plus offset frequency.
   F_{LO} = F_{LO_BASE} + F_{OFFSET}

F_{LO_BASE}

$$F_{LO\_BASE} = F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) = (DBL + 1) \cdot \frac{F_{XTAL}}{RRC[1:0] + 1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

Base on the above formula, for example, if F_{XTAL} = 16 MHz and set channel step F_{CHSP} = 500 KHz, to get **F_{LO_BASE} and F_{LO}**, see Table 14.1, 14.2, and Figure 14.2 for details.

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	DBL	1	Enable double function
3	RRC	0	If so, F_{PFD}= 32MHz
4	BIP	0x4B	To get F_{LO_BASE} =2400 MHz
5	BFP	0x0002	To get F_{LO_BASE} ~ 2400.001 MHz
6	**F_{LO_BASE}**	**~2400.001 MHz**	LO Base frequency

Table 14.1 How to set F_{LO_BASE}

How to set $F_{TXRF} = F_{LO} = F_{LO\_BASE} + F_{OFFSET}$ ~ 2405.001 MHz

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~2400.001 MHz	After set up BIP and BFP
2	CHR	0x0F	To get F_{CHSP}= 500 KHz
3	F_{CHSP}	500 KHz	Channel step = 500KHz
4	CHN	0x0A	Set channel number = 10
5	F_{OFFSET}	5 MHz	F_{OFFSET}= 500 KHz * (CHN) = 5MHz
6	F_{LO}	~2405.001 MHz	Get F_{LO}= F_{LO_BASE} + F_{OFFSET}
7	**F_{TXRF}**	**~2405.001 MHz**	F_{TXRF} = F_{LO}

Table 14.2 How to set F_{TXRF}

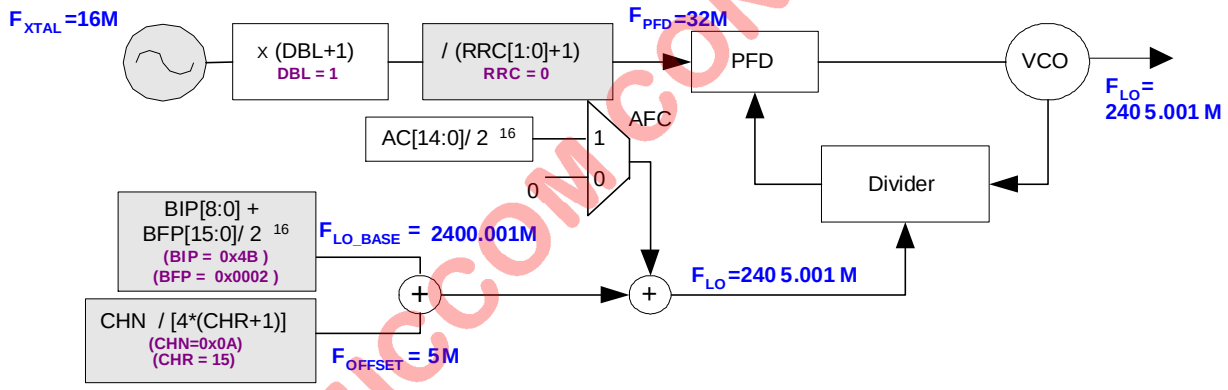


Figure 14.2 Block Diagram of set up F_{LO} ~ 2405.001 MHz

For different crystal frequency, 24MHz / 16MHz / 12 MHz, below are calculation details for F_{FPD} and F_{CHSP}

$$F_{\mathrm{PFD}} = \frac{(DBL+1)\cdot f_{XTAL}}{RRC[1:0]+1}$$

F_{XTAL} (MHz)	DBL	RRC	F_{PFD} (MHz)	Note
16	1	0	32	

$$F_{CHSP} = \frac{F_{PFD}}{4\cdot(CHR[3:0]+1)}$$

F_{XTAL} (MHz)	F_{PFD} (MHz)	CHR [3:0]	F_{CHSP} (KHz)	CHN [7:0]	F_{OFFSET} (MHz)	F_{LO} (MHz)
16	32	1111	500	0x00 ~ 0xA8	0 ~ 84	2400 ~ 2484

14.2 IF Side Band Select

In two ways radio, both master and slave have two roles, TX and RX. In general, slave usually has to reply an ACK-packet or status update. In such case, A7130 offers two methods to set up **F_{LO}** while TRX exchanging.

(1) Auto IF exchange
(2) Fast exchange

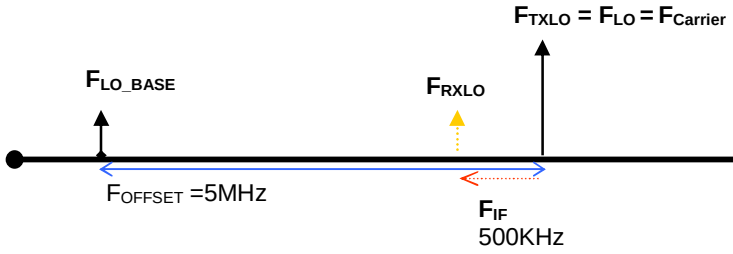
Register Setting	AIF Function	F_{RXLO} Formula
ULS=0	Disable (AIF=0)	$F_{RXLO} = F_{LO}$
ULS=1		$F_{RXLO} = F_{LO}$
ULS=0	Enable (AIF=1)	$F_{RXLO} = F_{LO} - 500KHz$
ULS=1		$F_{RXLO} = F_{LO} + 500Kz$

Table 14.3 F_{RXLO} Formula

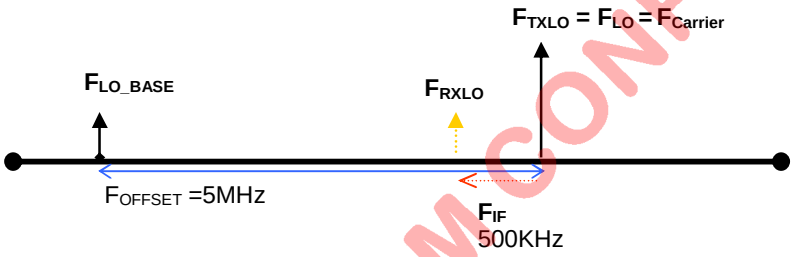
14.2.1 Auto IF Exchange

A7130 supports Auto IF offset function (AIF, 01h). If AIF is enabled, only one on-air occupied frequency (Fcarrier). In this case, user has no need to change F_{RXLO} while TRX exchanging because F_{RXLO} is auto shifted F_{IF}. See below Figures and Table 14.4 for details.

<Master>
AIF=1 and ULS=0, F_{RXLO} is auto shifted lower than F_{TXLO} for 500KHz (F_{IF}).



<Slave>
AIF=1 and ULS=0, F_{RXLO} is auto shifted lower than F_{TXLO} for 500KHz (F_{IF}).



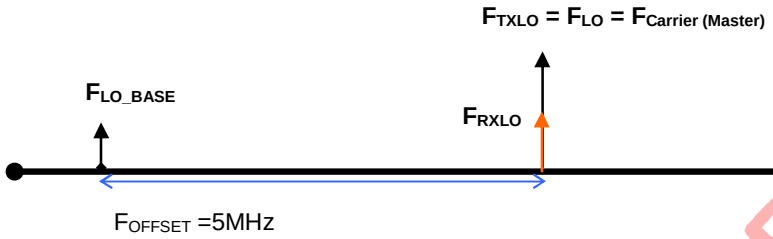
Item	Role	AIF	ULS	CHN[7:0]	F_{CHSP} (KHz)	F_{TXLO} (KHz)	F_{RXLO} (MHz)	NOTE
Master	TX	1	0	**10**	500	2405.001	-	
	RX	1	0	**10**	500	-	2404.501	Up side band F_{RXLO} is auto shifted
Slave	TX	1	0	**10**	500	2405.001	-	
	RX	1	0	**10**	500	-	2404.501	Up side band F_{RXLO} is auto shifted

Table 14.4 AIF function while TRX exchanging

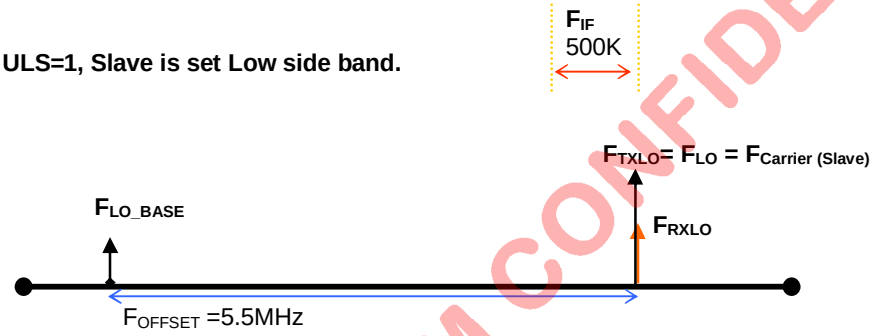
14.2.2 Fast Exchange

To reduce PLL settling time, user can disable AIF function. If AIF is disabled, two On-air frequency ($F_{Carrier\ (master)}$, $F_{Carrier\ (slave)}$) are occupied. In this case, user has to control ULS =0 (Master side) and ULS = 1 (Slave side) for fast exchange in two-way radio. See below Figures and Table 14.5 for details.

<Master>
AIF=0 and ULS=0, Master is set Up side band.



<Slave>
AIF=0 and ULS=1, Slave is set Low side band.



Item	Role	AIF	ULS	CHN[7:0]	F_{CHSP} (KHz)	F_{TXLO} (KHz)	F_{RXLO} (MHz)	NOTE
Master	TX	0	**0**	**10**	500	2405.001	-	
	RX	0	**0**	**10**	500	-	2405.001	Up side band
Slave	TX	0	**1**	**14**	500	2405.501	-	
	RX	0	**1**	**14**	500	-	2405.501	Low side band

Table 14.5 Fast exchange function while TRX exchanging

15. Calibration

A7130 needs calibration process after power on reset or software reset by 3 calibration items, they are, VCO Current, VCO Bank, and IF Filter Bank.

1. VCO Current Calibration (Standby or PLL mode) is used to find adequate VCO current.
2. VCO Bank Calibration (PLL mode) is used to select best VCO frequency bank for the calibrated frequency.
3. IF Filter Bank Calibration (Standby or PLL mode) is used to calibrate IF filter bandwidth and center frequency.

15.1 Calibration Procedure

1. Initialize all control registers (refer to A7130 reference code).
2. Select calibration mode (set MFBS=0, MVCS =1, MVBS = 0).
3. Set A7130 in PLL mode.
4. Enable IF Filter Bank (set FBC = 1),
   VCO Current (VCC = 1), and VCO Bank (VBC = 1).
5. After calibration done, FBC, VCC and VBC is auto clear.
6. Check pass or fail by reading calibration flag.
   (FBCF) and (VCCF, VBCF).

15.2 IF Filter Bank Calibration

1. Initialize all control registers (refer to A7130 reference code).
2. Set MFBS = 0 for auto calibration.
3. Set A7130 in PLL mode.
4. Set FBC= 1.
5. The maximum calibration time for this calibration is about 256us.
6. FBC is auto clear after calibration done.
7. User can read calibration flag (FBCF) to check pass or fail.
8. User can read FB [3:0] to get the auto calibration value.

15.3 VCO Current Calibration

1. Initialize all control registers (refer to A7130 reference code).
2. Set MVCS= 1 for manual calibration.
3. Set VCOC[3:0] = [0011].

15.4 VCO Bank Calibration

1. Initialize all control registers (refer to A7130 reference code).
2. Set MVBS= 0 for auto calibration.
3. Set A7130 in PLL mode.
4. Set VBC= 1. Set VCO tuning upper threshold voltage VH and lower threshold voltage VL. The recommended voltage is VTH [2:0] = [111], VTL[2:0] = [011].
5. The maximum calibration time for VCO Bank Calibration is about 240 us (4 * PLL settling time).
6. VBC is auto clear after calibration done.
7. User can read calibration flag (VBCF) to check pass or fail.
8. User can read VB [2:0] to get the auto calibration value.

16. FIFO (First In First Out)

A7130 supports separated 64-bytes TX and RX FIFO by enabling FMS =1. For FIFO accessing, TX FIFO (write-only) and RX FIFO (read-only) share the same register address 05h. TX FIFO represents transmitted payload. On the other hand, once RX circuitry synchronizes ID Code, received payload is stored into RX FIFO.

In chapter 10 and 11, user can also find listed FIFO information below.
(1) Figure 10.15 and 10.16 for FIFO accessing via 3-wire SPI.
(2) Section 10.4.7 and 10.4.8 for FIFO pointer reset command.
(3) Figure 11.2 and Figure 11.3 for Normal/Quick FIFO mode.

16.1 Packet Format

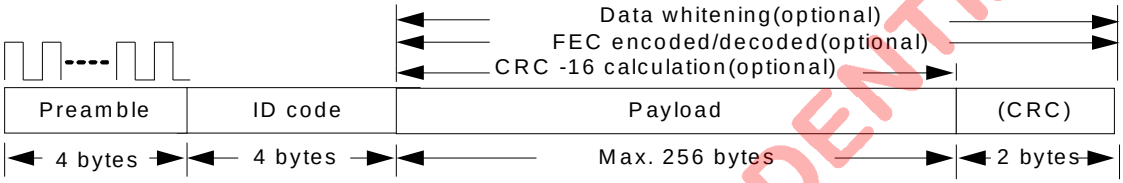


Figure 16.1 Packet Format of FIFO mode

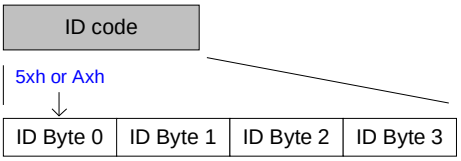


Figure 16.2 ID Code Format

Preamble:
The packet is led by preamble composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010…1010.
Preamble length is recommended to set 4 bytes by PML [1:0].

ID code:
ID code is recommended to set 4 bytes by IDL=1. ID Code is sequenced by Byte 0, 1, 2 and 3 (Recommend to set ID Byte 0 = 5xh or Axh). If RX circuitry checks the ID code correct, received payload will be stored into RX FIFO. In special case, ID code could be set error tolerance (0~ 3bit error) by ETH [1:0] for ID synchronization check.

Payload:
Payload length is programmable by FEP [7:0] from 1 byte to 64 bytes. The physical FIFO depth is 64 bytes. A7130 also supports logical FIFO extension up to 256 bytes. See section 16.4.3 for details.

CRC (option):
In FIFO mode, if CRC is enabled (CRCS=1), 2-bytes of CRC value is transmitted automatically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag.

16.2 Bit Stream Process

A7130 supports 3 optional bit stream process for payload, they are,
(1) CCITT-16 CRC ($x^{16} + x^{15} + x^2 + 1$)
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1. TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.
2. RX circuitry checks CRC value and shows the result to CRC Flag. If CRCF=0, received payload is correct, else error occurred. (CRCF is read only, it is revised internally while receiving every packet.)

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1. Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word as well as delivered out automatically. **(ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)**
3. RX circuitry decodes received code words automatically. FEC supports 1-bit error correction each code word. Once 1-bit error occurred, FEC flag=1. (FECF is read only, it is revised internally while receiving every packet.)

Data Whitening:

1. Data whitening is enabled by WHTS= 1. The initial seed of PN7 is WS [6:0]. Payload is always encrypted by bit XOR operation with PN7. CRC and/or FEC are also encrypted if CRCS=1 and/or if FECS=1.
2. RX circuitry decrypts received payload and 2-bytes CRC (if CRCS=1) automatically. Be notice, user shall set the same WS [6:0] to TX and RX.

16.3 Transmission Time

Based on CRC and FEC options, the transmission time are different. See table 16.1 for details.

Data Rate = 4Mbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 0.25 us = 144 us
32	32	512	16 bits	Disable	592 bit X 0.25 us = 148 us
32	32	512	Disable	512 x 7 / 4	960 bit X 0.25 us = 240 us
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 0.25 us = 247 us

Table 16.1 Transmission time

16.4 Usage of TX and RX FIFO

In application points of view, A7130 supports 3 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO
(3) FIFO Extension

For FIFO operation, A7130 supports Strobe command to reset TX and RX FIFO pointer as shown below. User can refer to section 10.5 for FIFO write pointer reset and FIFO read pointer reset.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	X	x	FIFO write pointer reset (for TX FIFO)
1	1	1	1	x	x	X	x	FIFO read pointer reset (for RX FIFO)

16.4.1 Easy FIFO

In Easy FIFO, max FIFO length is 64 bytes. FIFO length is equal to **(FEP [7:0] +1)**. User just needs to control FEP [7:0] and disable PSA and FPM as shown below.

Register setting

TX	RX	Control Registers		
FIFO Length (byte)	FIFO Length (byte)	FEP[7:0]	PSA [5:0]	FPM [1:0]
1	1	0x00	0	0
8	8	0x07	0	0
16	16	0x0F	0	0
32	32	0x1F	0	0
64	64	0x3F	0	0

Table 16.2 Control registers of Easy FIFO

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer to A7130 reference code).
2. Set FEP [7:0] = 0x3F for 64-bytes FIFO.
3. Refer to section 11.2 ~ 11.4.
4. Send Strobe command – TX FIFO write pointer reset.
5. MCU writes 64-bytes data to TX FIFO.
6. Send TX Strobe Command.
7. Done.

Procedures of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) can be used to trigger MCU for RX FIFO reading.
2. Send Strobe command – RX FIFO read pointer reset.
3. MCU read 64-bytes from RX FIFO.
4. Done

.

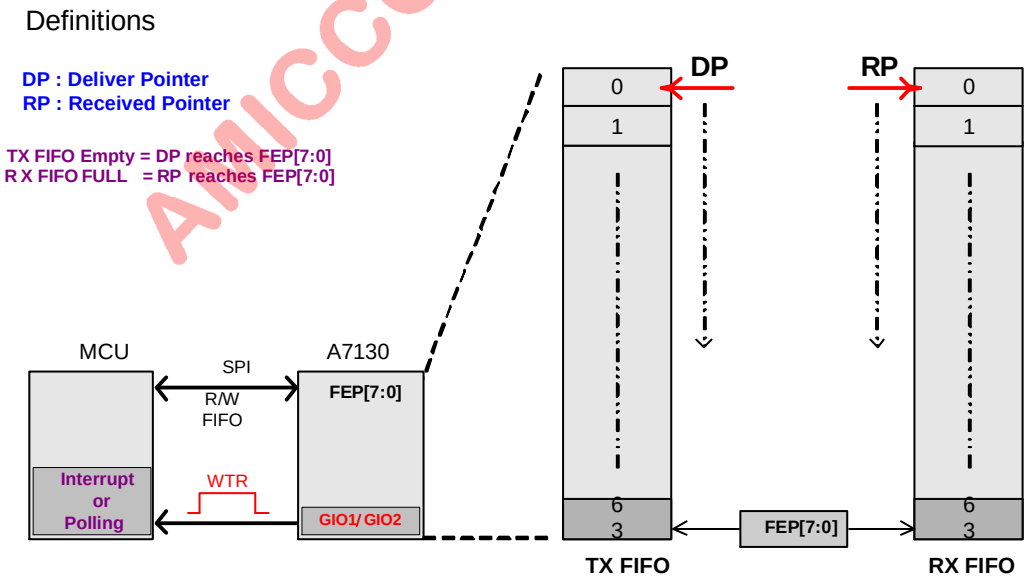


Figure 16.3 Easy FIFO

17. ADC (Analog to Digital Converter)

A7130 has built-in 8-bits ADC do RSSI measurement as well as carrier detection function. User can set FSARS to select 4MHz or 8MHz ADC clock (F_{ADC}). The ADC converting time is 20 x ADC clock periods.

Bit		Mode	
XADS	RSS	Standby	RX
0	1	None	RSSI / Carrier detect

Table 17.1 Setting of ADC function

17.1 RSSI Measurement

A7130 supports 8-bits digital RSSI to detect RF signal strength. RSSI value is stored in ADC [7:0]. Fig 17.1 shows a typical plot of RSSI reading as a function of input power. This curve is base on the current gain setting of A7130 reference code. A7130 automatically averages 8-times ADC conversion a RSSI measurement until A7130 exits RX mode. Therefore, each RSSI measuring time is (8 x 20 x F_{ADC}). For quick RSSI measurement, recommend to set FSARS = 1 (F_{ADC} =8MHz, 20 us measuring time). For power saving, recommend to set FSARS = 0 (F_{ADC} =4MHz, 40 us measuring time). Be aware RSSI accuracy is about ± 6dBm.

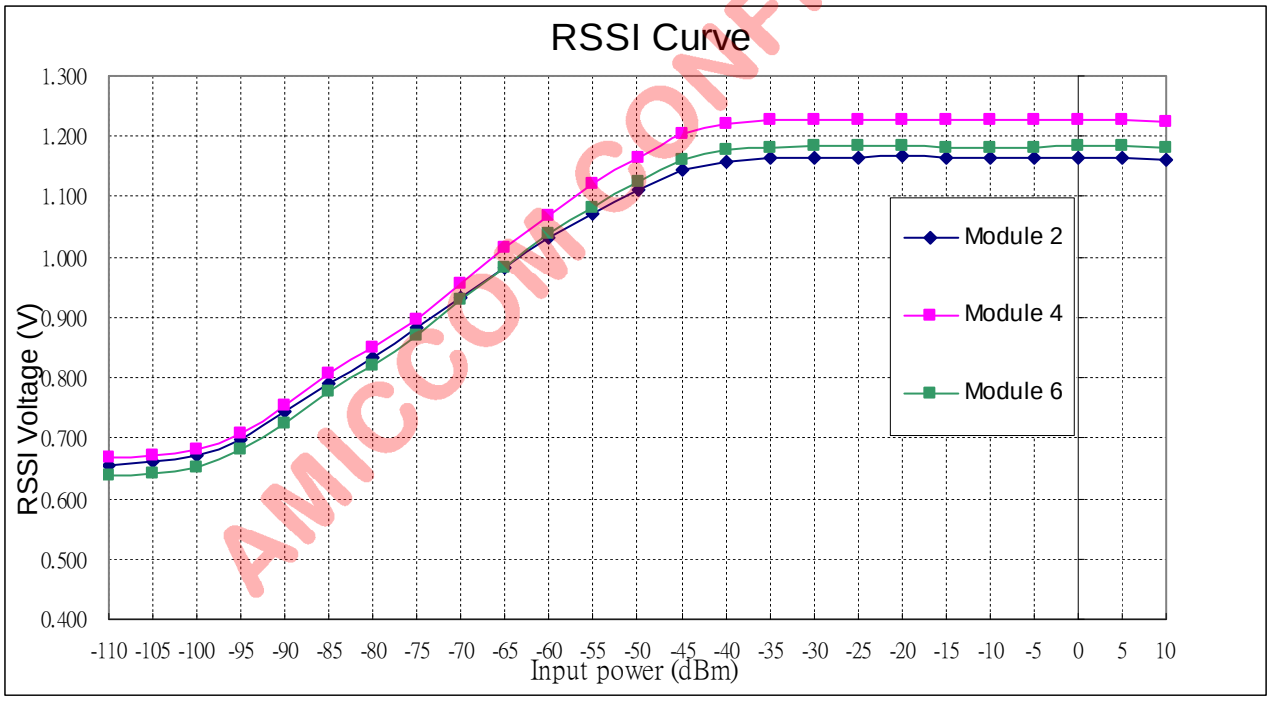
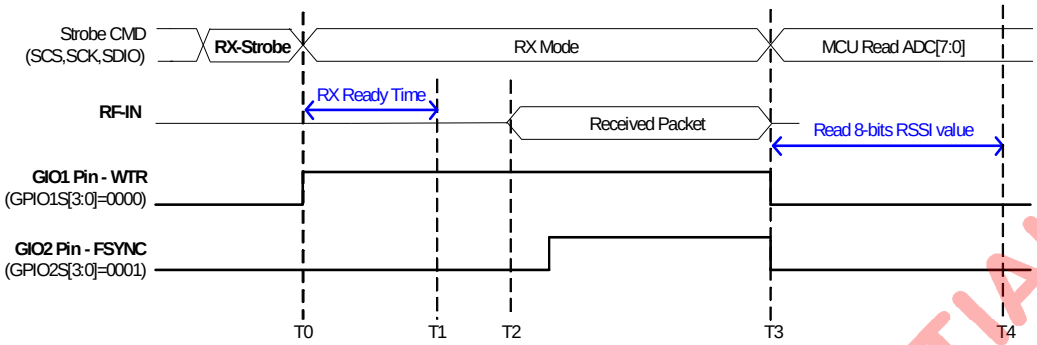


Figure 17.1 Typical RSSI characteristic.

Auto RSSI measurement for TX Power:

1. Set wanted F_{RXLO} (Refer to chapter 14).
2. Set RSS= 1, FSARS= 0 (4MHz ADC clock).
3. Enable ARSSI= 1.
4. Send RX Strobe command.
5. In RX mode, 8-times average a RSSI measurement periodically.
6. Exit RX mode, user can read digital RSSI value from ADC [7:0] for TX power.

In step 6, if A7130 is set in direct mode, MCU shall let A7130 exit RX mode within 40 us to prevent RSSI inaccuracy.

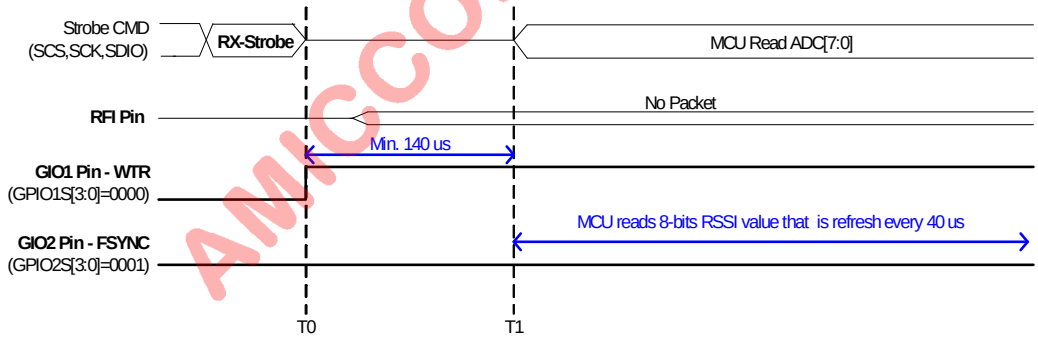


T0-T1: Settling Time
T2-T3: Receiving Packet
T3 : Exit RX mode automatically in FIFO mode
T3-T4: MCU read RSSI value @ ADC [7:0]

Figure 17.2 RSSI Measurement of TX Power.

Auto RSSI measurement for Background Power:

1. Set wanted F_{RXLO} (Refer to chapter 14).
2. Set RSS= 1, FSARS= 1 (4MHz ADC clock).
3. Enable ARSSI= 1.
4. Send RX Strobe command.
5. MCU delays min. 140us.
6. Read digital RSSI value from ADC [7:0] to get background power.
7. Send other Strobe command to let A7130 exit RX mode.

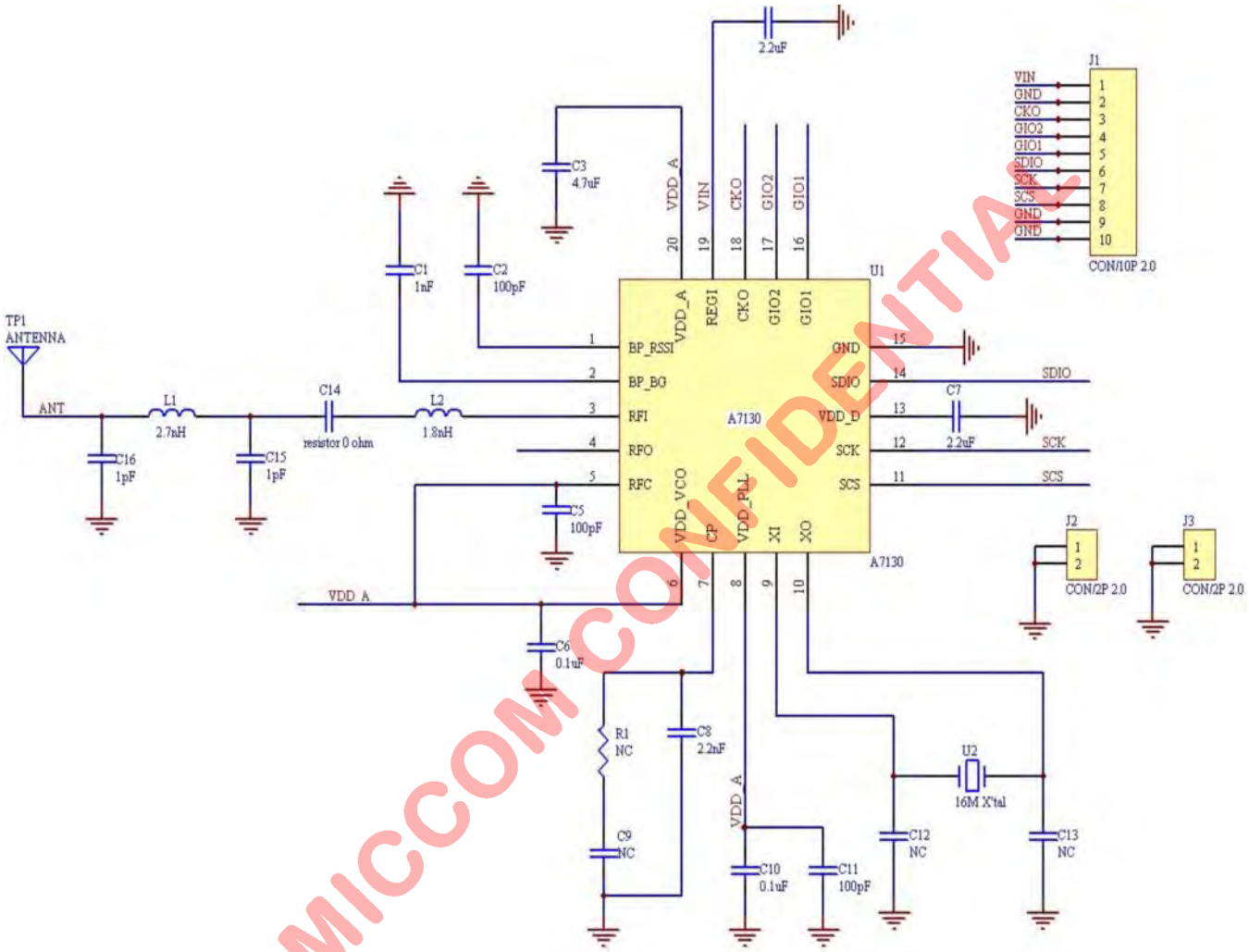


T0-T1: MCU Delay Loop from PLL to RX mode for RSSI measurment
T1 : Auto RSSI Measurment is done by 8-times average.
MCU can read RSSI value from ADC [7:0]

Figure 17.3 RSSI Measurement of Background Power.

20. Application circuit

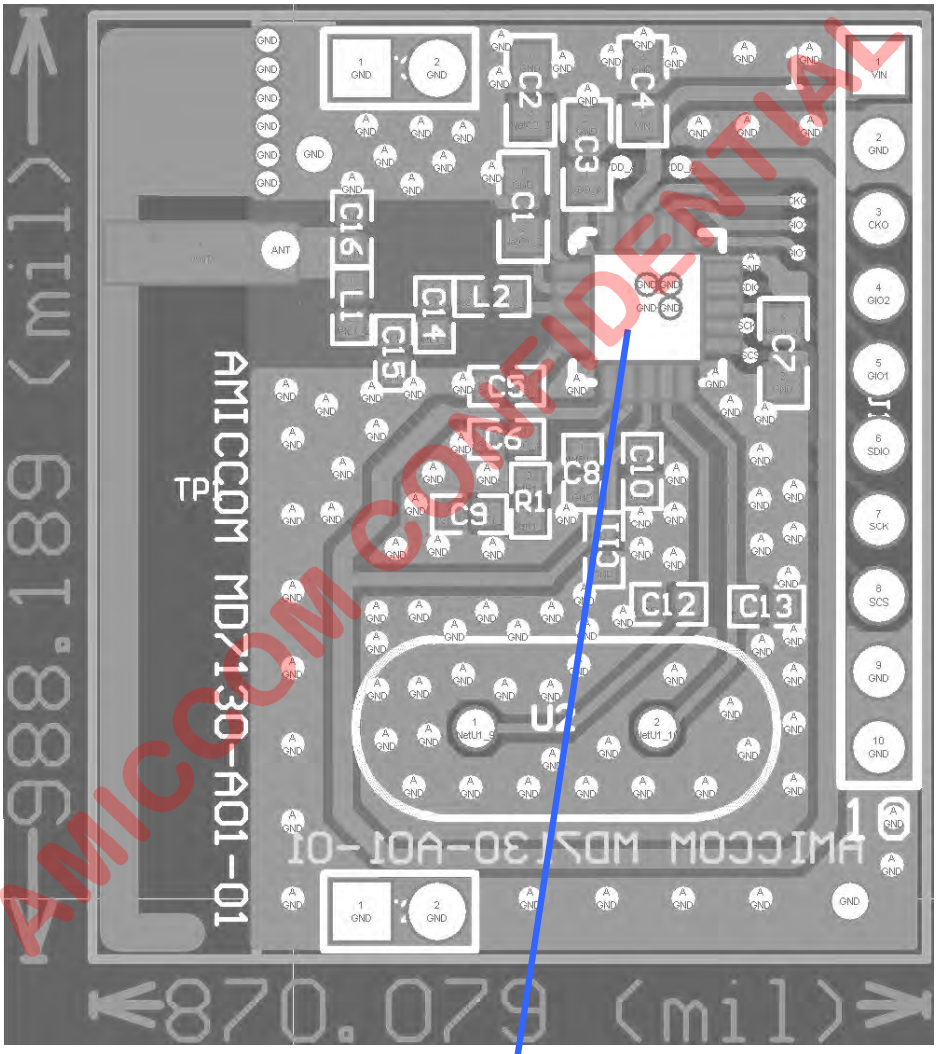
Below are AMICCOM's ref. design module, MD7130-A01, circuit example and its PCB layout.



1. A7130 schematic for RF layouts with single ended 50Ω RF output.
2. Y1 is a 16MHz crystal with 18 pF Cload, max 80ohm ESR and 30 ppm stability. Please see application note for detail.

MD7130-A01 which size is 988 mil x 870 mil with PCB antenna is suitable for small form factor application. MD7130-A01 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

To get a good RF performance, a well designed PCB is necessary. A poor layout can lead to loss of RF performance especially on matching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7130's **GND** pad and IC back side plate (**GND**).



Be Notice,
1. IC Back side plate shall be well-solder to ground (U1 area) for good RF performance.
2. Need at least 9 GND via holes at U1 area

21. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

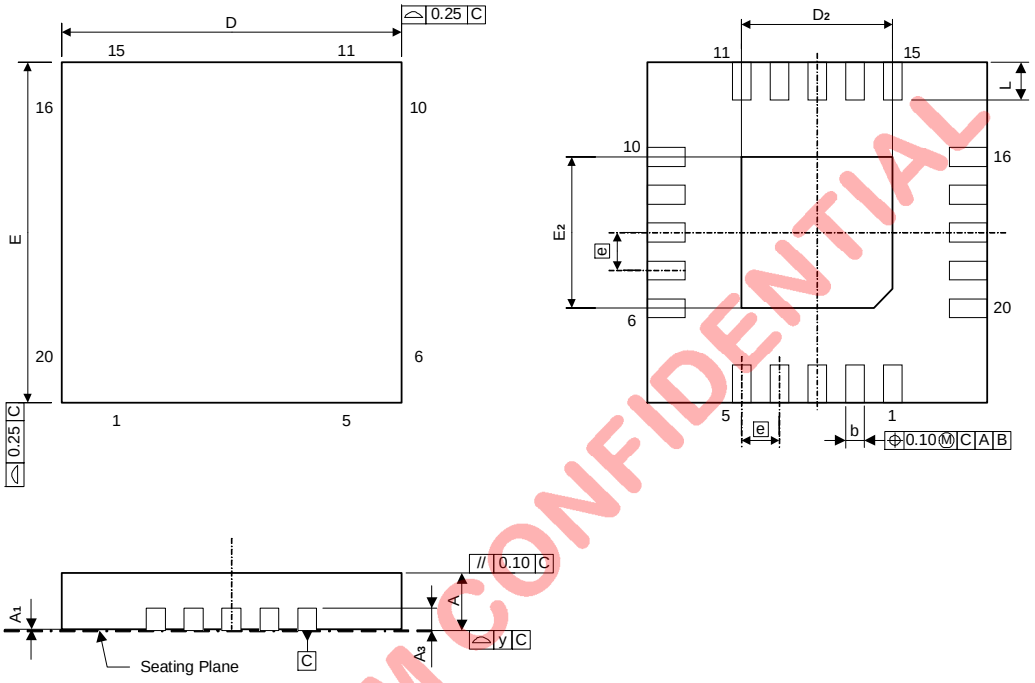
22. Ordering Information

Part No.	Package	Units Per Reel / Tray
A71C30AQFI/Q	QFN20L, Pb Free, Tape & Reel, -40℃～85℃	3K
A71C30AQFI	QFN20L, Pb Free, Tray, -40℃～85℃	490EA
A71C30BH	Die form, -40℃～85℃	100EA

23. Package Information

QFN 20L (4 X 4 X 0.8mm) Outline Dimensions unit: inches/mm

TOP VIEW **BOTTOM VIEW**

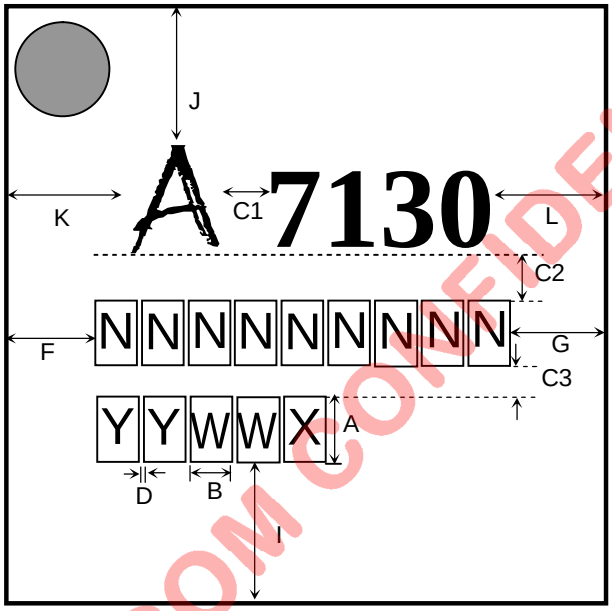


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3		0.008 REF			0.203 REF	
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.154	0.158	0.161	3.90	4.00	4.10
D_2	0.075	0.079	0.083	1.90	2.00	2.10
E	0.154	0.158	0.161	3.90	4.00	4.10
E_2	0.075	0.079	0.083	1.90	2.00	2.10
e		0.020 BSC			0.50 BSC	
L	0.012	0.016	0.020	0.30	0.40	0.50
y		0.003			0.08	

24. Top Marking Information

A71C30AQFI

- Part No. : **A71C30AQFI**
- Pin Count : **20**
- Package Type :**QFN**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type :**Arial**

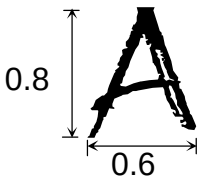


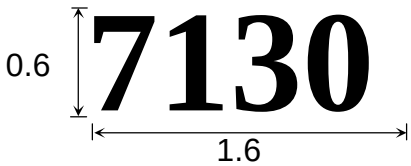
❖ **CHARACTER SIZE : (Unit in mm)**

A : 0.55
B : 0.36
C1 : 0.25 **C2 : 0.3**
C3 : 0.2
D : 0.03

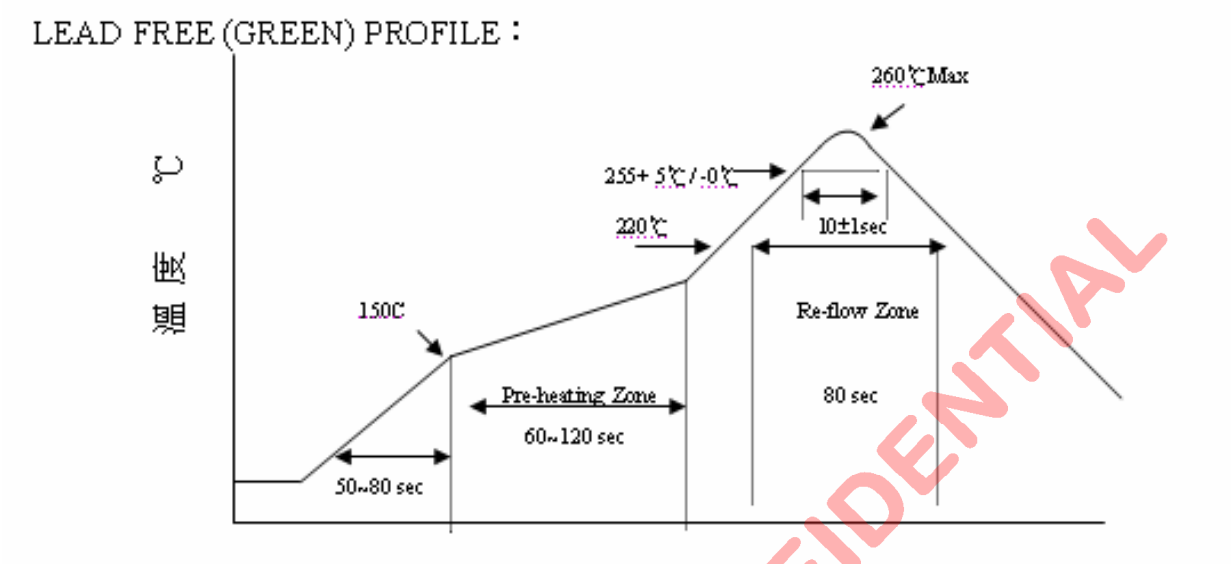
F=G
I=J

Y Y W W	:
X	: PKG HOUSE
N N N N N N N N N	: LOT NO. (max. 9 characters)





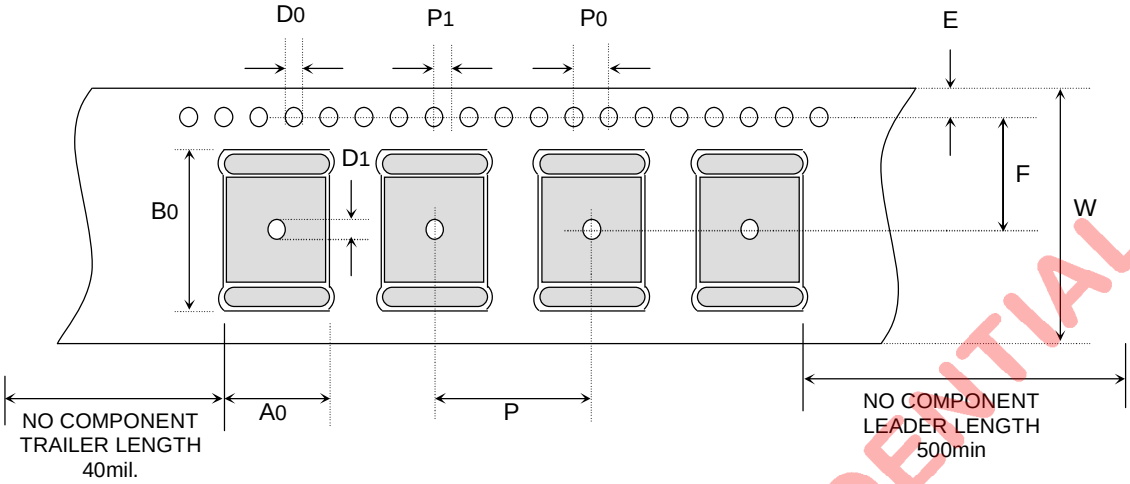
25. Reflow Profile



Actual Measurement Graph

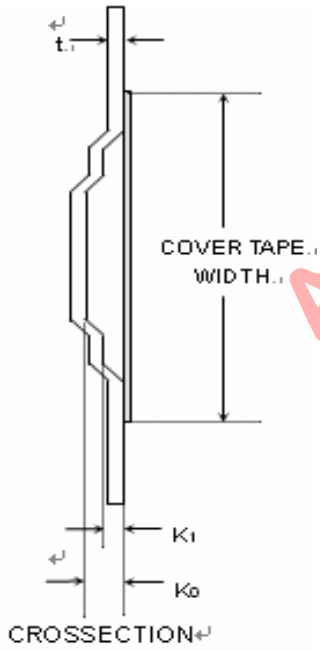
26. Type Reel Information

Cover / Carrier Tape Dimension



11 EA IC **60cm±4cm**

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
48 QFN 7*7	12	7.25	7.25	4.0	2.0	1.5	1.5	1.75	7.5	16
DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16
28 SSOP (150mil)	8	6	10	4.0	2.0	1.5	1.5	1.75	7.5	16



TYPE	K0	K1	t
20 QFN (4X4)	1.1	-	0.3
24 QFN (4X4)	1.4	-	0.3
32 QFN (5X5)	1.1	-	0.3
48 QFN (7X7)	1.1	-	0.3
DFN-10	0.75	-	0.25
20 SSOP	2.5	-	0.3
24 SSOP	2.1	-	0.3
28 SSOP (150mil)	2.5	-	0.3

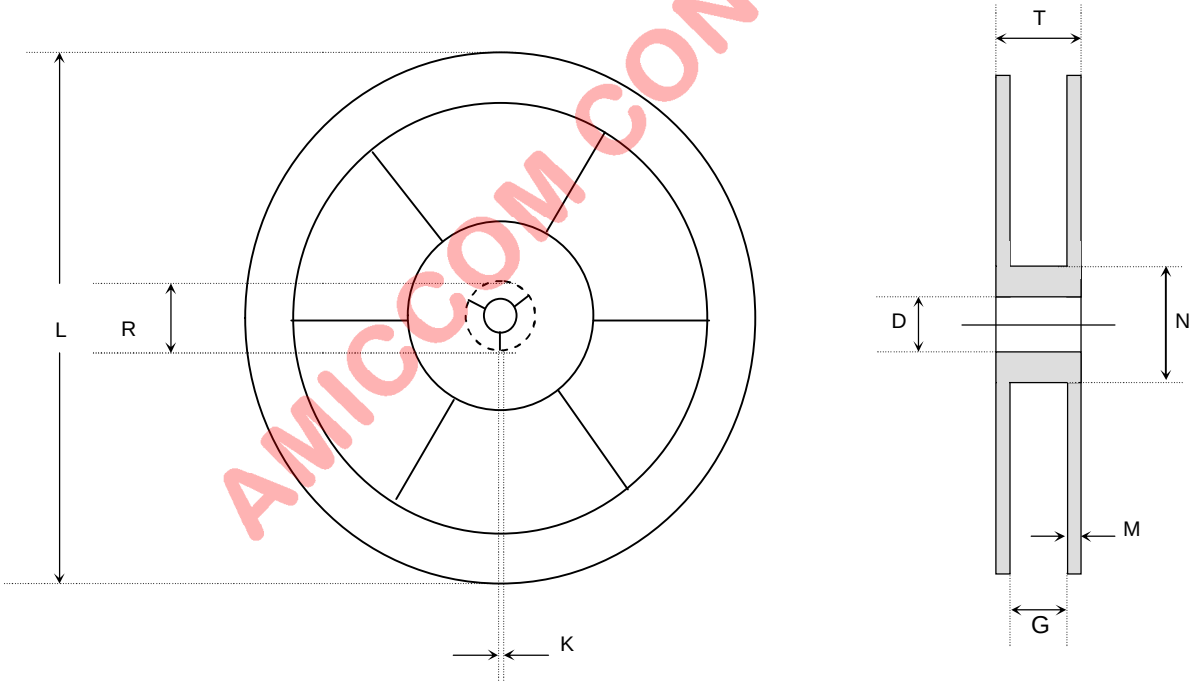
COVER TAPE WIDTH
9.2
9.2
9.2
13.3
8
13.3
13.3
12.5

Unit : mm

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330+ 0.00/-1.0	20.2



27. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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