Document Title

A7125 Data Sheet, 2.4GHz FSK Transceiver with 2M / 1Mbps data rate

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue.	Aug. 31, 2007	Preliminary
0.1	Logo change.	Oct. 18, 2007	Preliminary
0.2	Modify PIN Configuration and Description, Block Diagram, Electrical Specifications, Diagram of State Machine. Add Control Register and Function Description.	July 31, 2008	Preliminary
0.3	Add Power Saving FIFO Mode. Rename GPIO1 and GPIO2 into GIO1 and GIO2.	August 31, 2008	Preliminary
0.4	Modify register recommended value IGFI [2:0] = [000] Modify register recommended value IGFQ [2:0] = [000] Delete TWWS function	October 06, 2008	Preliminary
0.5	Modify register recommended value Delay Register I (17h): PDL= [000] Delay Register II (18h): WSEL= [011] Battery Detect Register (2Ch): QDS = [1] Crystal Test Register (32h): XCP= [00] IFAT Register (36h): IGFI [2:0] = [111], IGFQ [2:0] = [111] Modify PLL to WPLL settling time when PDL=[000] If LO is changed, from 20 us to 30 us If LO is fixed, from 20 us to 10 us Delete Ext Voltage Measurement function Add EOPD output to GIO2 Add PASW output to GIO2 Add EOPDS Register Add section 16.5	June 11, 2009	Preliminary
1.0	Modify register recommended value ADC Control (1Fh): CDM= [0] Modify recommended timing of PASW	Feb., 2010	Full Production
1.1	Add Note 8 (regulator settling time) in chapter 8.	Nov., 2010	Full Production
1.2	Change English Company Name	Nov. 30, 2010	

Table of Contents

1. Typical Application

- 2.4GHz ISM band Communication System
- 2.4GHz Remote Control
- Wireless Keyboard and Mouse
- Wireless Intelligent sports
- Wireless Toy and Gaming
- Wireless Audio/Video Streaming

2. General Description

A7125 is a high performance and low cost 2.4GHz ISM band wireless transceiver. It integrates high sensitivity receiver (-90dBm @2Mbps), high efficiency power amplifier (up to 3dBm), frequency synthesizer and base-band modem. In typical system, A7125 is used together with MCU (microcontroller) with very few external passive components. A7125 supports both FIFO mode and direct mode that contains clock recovery circuit CKO pin to MCU.

A7125 supports very fast settling time (90 us) for frequency hopping system. For packet handling, A7125 has built-in separated 64-bytes TX/RX FIFO (could be extended to 256 bytes) for data buffering and burst transmission, CRC for error detection, FEC for 1-bit data correction per code word, RSSI for clear channel assessment, data whitening for data encryption/decryption, thermal sensor for monitoring relative temperature. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 20 pins package.

A7125's data rate is up to 2Mbps and can be easily programmed to 1Mbps or 2 Mbps via 3-wire or 4-wire SPI bus. For power saving, A7125 supports sleep mode, idle mode, standby mode. For easy-to-use, A7125 has an unique SPI command set called **Strobe command** that are used to control A7125's state machine. Based on Strobe commands, from power saving, TX delivery, RX receiving, channel monitoring, frequency hopping to auto calibrations, MCU only needs to define A7125's control registers and send Strobe commands via SPI bus. In addition, A7125 supports two general purpose I/O pins, GIO1 and GIO2, to inform MCU its status so that MCU could use either polling or interrupt scheme to do radio control. Therefore, it is very easy to monitor transmission between MCU and A7125 because of its digital interface.

3. Feature

- Small size (QFN 4X4, 20 pins).
- Support 2400 ~ 2483.5 MHz ISM band.
- FSK modulation.
- Programmable data rate to 1Mbps or 2Mbps.
- Low current consumption: RX 17mA, TX 15.7mA (at 0dBm output power).
- Low sleep current (1.5uA).
- Programmable RF output power -20dBm ~ 3dBm.
- Very High sensitivity (-90dBm@2Mbps, -92dBm@1Mbps).
- On chip regulator, supports input voltage 2.0 ~ 3.6V.
- Easy to use
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - Change frequency channel by ONE register setting.
  - 8-bits Digital RSSI for clear channel indication.
  - Fast exchange mode during TRX role switching.
  - Auto RSSI measurement.
  - Auto Calibrations.
  - Auto IF function.
  - Auto CRC Check.
  - Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
  - Data Whitening for encryption and decryption.
  - Separated 64 bytes RX and TX FIFO.
  - Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
  - Support direct mode with recovery clock output to MCU.
  - Support direct mode with frame sync signal to MCU.
- Support low cost crystal (6 / 8 /12 / 16MHz).
- Support low accuracy crystal within ± 50ppm.
- Support Auto Frequency Compensation.
- Support crystal sharing, (1 / 2 / 4 / 8MHz) to MCU.
- Fast settling time synthesizer for frequency hopping system.
- Built-in thermal sensor for monitoring relative temperature.
- Built-in Battery Detector.

4. PIN Configuration

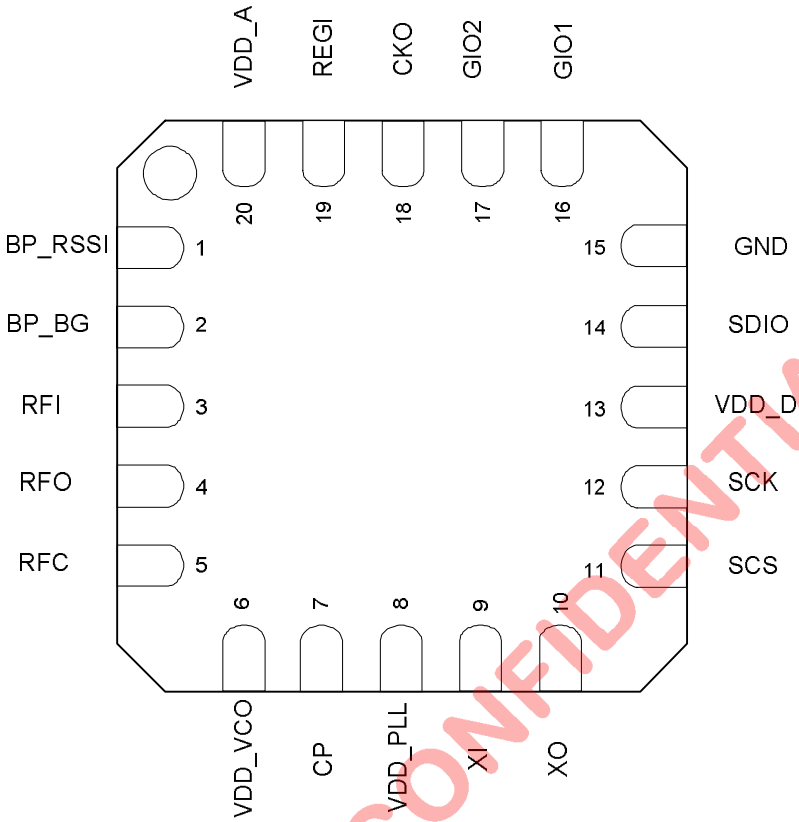


Figure 4.1 A7125 QFN 4x4 Package Top View

5. PIN Description (I: Input, O: Output, I/O: Input or Output, G: Ground, D: Digital)

Pin No.	Symbol	I/O	Function Description
1	BP_RSSI	O	O: RSSI bypass. Connect to bypass capacitor.
2	BP_BG	O	Band-gap bypass. Connect to bypass capacitor.
3	RFI	I	RF input. Connect to matching circuit.
4	RFO	O	RF output. Connect to matching circuit.
5	RFC	I	RF choke input. Connect to matching circuit.
6	VDD_VCO	I	VCO supply voltage input.
7	CP	O	Charge-pump output. Connect to loop filter.
8	VDD_PLL	O	PLL supply voltage input.
9	XI	I	Crystal oscillator input. Connect to tank capacitor.
10	XO	O	Crystal oscillator output. Connect to tank capacitor.
11	SCS	DI	SPI chip select input.
12	SCK	DI	SPI clock input.
13	VDD_D	O	Digital supply voltage output. Connect to bypass capacitor.
14	SDIO	DI/O	SPI data IO.
15	GND	G	Ground.
16	GIO1	DI/O	Multi-function IO 1 / SPI data output.
17	GIO2	DI/O	Multi-function IO 2 / SPI data output.
18	CKO	DO	Multi-function clock output.
19	REGI	I	Regulator input. Connect to VDD supply.
20	VDD_A	O	Analog supply voltage output. Connect to bypass capacitor.
	Back side plate	**G**	**Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

6. Block Diagram

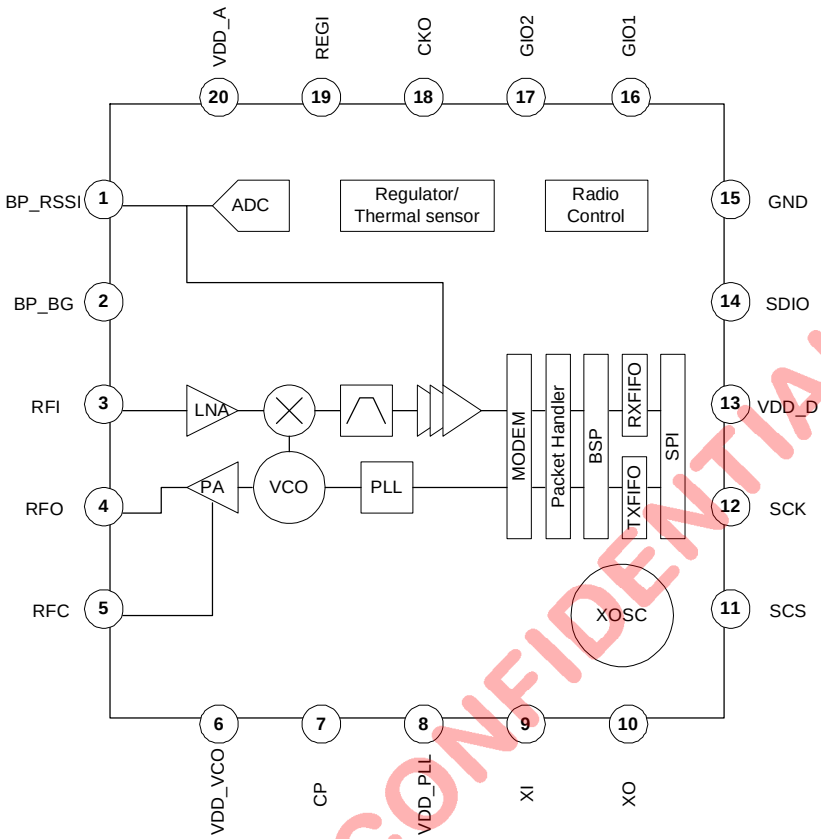


Figure 6.1 A7125 Block Diagram

7. Absolution Maximum Rating

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital I/O pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		14	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

8. Electrical Specifications

(Ta=25℃, VDD=3.3V, data rate= 2Mbps, F_{XTAL} =16MHz, with Matching Network and low pass filter, On Chip Regulator = 1.8V, unless otherwise noted.)

Parameter	Description	Minimum	Typical	Maximum	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD)	Regulator supply input	2.0	3.3	3.6	V
Current Consumption	Sleep Mode		1.5(1*)		uA
	Idle Mode (Regulator on)		300(1*)		uA
	Standby Mode (XOSC on, Clock generator on)		2.9		mA
	PLL Mode		9.8		mA
	RX Mode (2Mbps)		17.0		mA
	RX Mode (1 Mbps)		16.2		mA
	TX Mode (@3dBm output)		21		mA
	TX Mode (@0dBm output)		15.7		mA
	TX Mode (@-10dBm output)		13.7		mA
	TX Mode (@-20dBm output)		13.3		mA
Phase Locked Loop					
X'TAL Start-up Time (2*)			300		us
X'TAL Frequency (F_{XTAL})			6(3*), 8, 12, 16		MHz
VCO Operation Frequency		2400		2483.5	MHz
PLL Settling Time (4*)	@Loop BW = 200 KHz		30		μs
Transmitter					
TX Power Control Range			0		dBm
Out Band Spurious Emission (5*)	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	
	1.8GHz~ 1.9GHz			-47	
	5.15GHz~ 5.3GHz			-47	
Data rate		1	2	2	Mbps
Frequency Deviation			500		KHz
TX Settling Time (6*)	@Loop BW =200 KHz		40		μs
Receiver					
Sensitivity @BER=0.001	2Mbps		-90		dBm
Sensitivity @BER=0.001	1Mbps		-92		dBm
IF Frequency (F_{IF})			2		MHz
Interference (7*)	Co-Channel (C/I_0)		11		dB
	1st Adjacent Channel (C/I_1)		2		dB
	2nd Adjacent Channel (C/I_2)		-18		dB
	3rd Adjacent Channel (C/I_3)		-28		dB
	Image (C/I_{IM})		-12		dB
Maximum Operating Input Power	@RF input (BER=0.1%)			3	dBm
Spurious Emission (5*)	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	@RF input	-100		-50	dBm
RX Settling Time	@Loop BW = 200 KHz		40		μs
Regulator					
Regulator settling time (8*)			500		μs
Band-gap reference voltage			1.23		V
Regulator output voltage			1.8		V

Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, more leakage current will be induced in all operation modes.
Note 2: Refer to Delay Register II (18h) to set up crystal settling delay.
Note 3: If 6MHz external crystal is selected, A7125 only supports 1Mbps data rate.
Note 4: Refer to Delay Register I (17h) to set up PDL (PLL settling delay).
Note 5: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.
Note 6: Refer to Delay Register I (17h) to set up TDL delay.
Note 7: The power level of wanted signal is set at sensitivity +3dB. The modulation data for wanted signal and interferer are PN9 and PN15, respectively. Channel spacing is 2MHz.
Note 8: When VDD < 2.1V and temperature < -30 degree C, the regulator settling time will arise up to **20ms**.

9. Control Register

A7125 has totally built-in 57 control registers that cover all radio control. MCU can access those control registers via 3-wire or 4-wire SPI (Support max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details of SPI bus. A7125 is simply controlled by registers and outputs its status to MCU by GIO1 and GIO2 pins.

9.1 Control Register Table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Mode	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
	R	-	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
01h Mode control	W	DDPC	ARSSI	AIF	DFCD	WWSE	FMT	FMS	ADCM
	R	DDPC	ARSSI	AIF	CD	WWSE	FMT	FMS	ADCM
02h Calc	R/W	-	-	-	VCC	VBC	VDC	FBC	RSSC
03h FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
04h FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
05h FIFO Data	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h ID Data	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
07h RC OSC I	W	WWS_SL7	WWS_SL6	WWS_SL5	WWS_SL4	WWS_SL3	WWS_SL2	WWS_SL1	WWS_SL0
	R	-	-	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
08h RC OSC II	W	WWS_SL9	WWS_SL8	WWS_AC5	WWS_AC4	WWS_AC3	WWS_AC2	WWS_AC1	WWS_AC0
09h RC OSC III	W	BBCKS1	BBCKS0	-	-	-	RCOSC_E	TSEL	TWWS_E
0Ah CKO Pin	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GIO1 Pin I	W	-	-	GIO1S3	GIOS2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch GIO2 Pin II	W	-	-	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
0Dh Data Rate Clock	W	SDR1	SDR0	GRC3	GRC1	GRC1	GRC0	CGS	XS
	R	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	-	-
0Eh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
0Fh PLL II	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
10h PLL III	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
11h PLL IV	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	-FP15	AC14-FP14	AC13-FP13	AC12-FP12	AC11-FP11	AC10-FP10	AC9-FP9	AC8-FP8
12h PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	AC7-FP7	AC6-FP6	AC5-FP5	AC4-FP4	AC3-FP3	AC2-FP2	AC1-FP1	AC0-FP0
13h Channel Group I	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
14h Channel Group II	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
15h TX I	W	SDMS	TMDE	TXDI	TME	-	FDP2	FDP1	FDP0
16h TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
17h Delay I	W	EOPDS	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
18h Delay II	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
19h RX	W	-	RXSM1	RXSM0	FC	RXDI	DMG	RAW	ULS
1Ah RX Gain I	R/W	MVGS	MRHL	IGS	MGS1	MGS0	LGS2	LGS1	LGS0

1Bh RX Gain II	W	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
1Ch RX Gain III	W	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
1Dh RX Gain IV	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	MHC	LHC1	LHC0	AGCE
1Eh RSSI Threshold	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
1Fh ADC Control	W	RSM1	RSM0	RADC1	RADC0	FSARS	XADS	RSS	CDM
20h Code I	W	-	-	WHTS	FECS	CRCS	IDL	PML1	PML0
21h Code II	W	-	DCL2	DCL1	DCL0	ETH1	ETH0	PMD1	PMD0
22h Code III	W	-	WS6	WS5	WS4	WS3	WS2	WS1	WS0
23h IF Calibration I	W	-	-	-	MFBS	MFB3	MFB2	MFB1	MFB0
	R	-	-	-	FBCF	FB3	FB2	FB1	FB0
24h IF Calibration II	R	-	-	-	FCD4	FCD3	FCD2	FCD1	FCD0
25h VCO current Calibration	W	-	-	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	-	-	-	VCCF	VCB3	VCB2	VCB1	VCB0
26h VCO band Calibration I	W	DDC1	DDC0	MDAGS	-	MVBS	MVB2	MVB1	MVB0
	R	-	-	-	-	VBCF	VB2	VB1	VB0
27h VCO band Calibration II	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
28h VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
29h VCO deviation Calibration II	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
2Ah VCO deviation Calibration III	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
2Bh VCO modulation Delay	W	-	-	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
2Ch Battery detect	W	RGS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
	R	-	-	-	BDF	-	-	-	-
2Dh TX test	W	-	-	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
2Eh Rx DEM test I	W	DMT	DCM1	DCM0	MLP1	MLP0	SLF2	SLF1	SLF0
2Fh Rx DEM test II	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
30h Charge Pump Current I	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
31h Charge Pump Current II	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
32h Crystal test	W	-	-	-	-	DBD	XCC	XCP1	XCP0
33h PLL test	W	-	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
34h VCO test	W	-	-	-	TLB1	TLB0	RLB1	RLB0	VCBS
35h RF Analog test	W	OLM	VTBS	CPH	CPCS	-	RFT2	RFT1	RFT0

36h IFAT	W	IGFI2	IGFI1	IGFI0	IGFQ2	IGFQ1	IGFQ0	IFBC	LIMC
37h Channel Select	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
38h VRB	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0

Legend: - = unimplemented

9.2 Control Register Description

9.2.1 Mode Register (Address: 00h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
Reset		--	--	--	--	--	--	--	--

RESETN: Write to this register by 0x00 to issue reset command, then it is auto clear

FECF: FEC flag. (FECF is read only, it is updated for each valid packet.)
[0]: FEC pass. **[1]:** FEC error.

CRCF: CRC flag. (CRCF is read only, it is updated for each valid packet.)
[0]: CRC pass. **[1]:** CRC error.

CER: RF chip enable status.
[0]: RF chip is disabled. **[1]:** RF chip is enabled.

XER: Internal crystal oscillator enable status.
[0]: Crystal oscillator is disabled. **[1]:** Crystal oscillator is enabled.

PLLE: PLL enable status.
[0]: PLL is disabled. **[1]:** PLL is enabled.

TRER: TRX state enable status.
[0]: TRX is disabled. **[1]:** TRX is enabled.

TRSR: TRX Status Register.
[0]: RX state. **[1]:** TX state.
Serviceable if TRER=1 (TRX is enable).

9.2.2 Mode Control Register (Address: 01h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DDPC	ARSSI	AIF	CD	WWSE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	DFCD	WWSE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin when this register is enabled.
[0]: Disable. **[1]:** Enable.

ARSSI: Auto RSSI measurement while entering RX mode.
[0]: Disable. **[1]:** Enable.

AIF (Auto IF Offset): RF LO frequency will auto offset one IF frequency while entering RX mode.
[0]: Disable. **[1]:** Enable.

CD / DFCD:

DFCD (Data Filter by CD): The received packet will be filtered out if Carrier Detector signal is inactive.
[0]: Disable. **[1]:** Enable.

CD (Read): Carrier detector signal.
[0]: Input power below threshold. **[1]:** Input power above threshold.

WWSE: Reserved for internal usage only. Shall be set to [0].

FMT: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

ADCM: ADC measurement enable (Auto clear when done).
[0]: Disable measurement or measurement finished. **[1]:** Enable measurement.

ADCM	A7125 @ Standby mode	A7125 @ RX mode
[0]	Disable ADC	Disable ADC
[1]	Measure temperature	Measure RSSI, carrier detect

Refer to chapter 17 for details.

9.2.3 Calibration Control Register (Address: 02h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	--	--	--	VCC	VBC	VDC	FBC	RSSC
Reset		--	--	--	0	0	0	0	0

VCC: VCO Current calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VBC: VCO Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VDC: VCO Deviation calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

RSSC: RSSI calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.4 FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FEP [7:0]: FIFO End Pointer for TX FIFO and Rx FIFO.
Refer to chapter 16 for details.

9.2.5 FIFO Register II (Address: 04h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FPM [1:0]: FIFO Pointer Margin

PSA [5:0]: Used for Segment FIFO.
Refer to chapter 16 for details.

9.2.6 FIFO DATA Register (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

FIFO [7:0]: FIFO data. TX FIFO (Write only) and RX FIFO (Read only).
TX FIFO and RX FIFO share the same address (05h).
Refer to chapter 16 for details.

9.2.7 ID DATA Register (Address: 06h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0

ID [7:0]: ID data.

Once this address is accessed, ID Data is input/output in sequence corresponding to Write or Read.

Refer to section 10.6 for details.

9.2.8 RC OSC Register I (Address: 07h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R			RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
	W	WWS_SL7	WWS_SL6	WWS_SL5	WWS_SL4	WWS_SL3	WWS_SL2	WWS_SL1	WWS_SL0
Reset		0	0	0	0	0	0	0	0

RCOC [5:0]: Reserved for internal usage only.

9.2.9 RC OSC Register II (Address: 08h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	WWS_SL9	WWS_SL8	WWS_AC5	WWS_AC4	WWS_AC3	WWS_AC2	WWS_AC1	WWS_AC0
Reset		0	0	0	0	0	0	0	1

WWS_AC [5:0]: Reserved for internal usage only.

WWS_SL [9:0]: Reserved for internal usage only.

9.2.10 RC OSC Register III (Address: 09h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	BBCKS1	BBCKS0	--	--	--	RCOSC_E	TSEL	TWWS_E
Reset		0	0	--	--	--	1	0	1

BBCKS [1:0]: Clock select for digital block. Recommend BBCKS = [00].
[00]: F_{SYCK} / 8. **[01]:** F_{SYCK} / 16. **[10]:** F_{SYCK} / 32. **[11]:** F_{SYCK} / 64.
F_{SYCK} is A7125's System clock = 64MHz.

RCOSC_E: Reserved for internal usage only.

TSEL: Reserved for internal usage only.

TWWS_E: Reserved for internal usage only.

9.2.11 CKO Pin Control Register (Address: 0Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ECKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
Reset		1	0	1	1	1	0	1	0

ECKOE: External Clock Output Enable for CKOS [3:0]= [0100] ~ [0111].
[0]: Disable. **[1]:** Enable.

CKOS [3:0]: CKO pin output select.
[0000]: DCK (TX data clock) in TX mode, RCK (RX recovery clock) in RX mode.
[0001]: DCK (TX data clock) in TX mode, RCK (RX recovery clock) in RX mode.
[0010]: FPF (FIFO pointer flag).
[0011]: EOVBC, EOFBC, EOADC, EOVCC, OKADC (Internal usage only).
[0100]: External clock output= F_{SYCK} / 8.
[0101]: External clock output / 2= F_{SYCK} / 16.
[0110]: External clock output / 4= F_{SYCK} / 32.
[0111]: External clock output / 8= F_{SYCK} / 64.
[1xxx]: Reserved.

CKOI: CKO pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCKI: SPI clock input invert.
[0]: Non-inverted input. **[1]:** Inverted input.

9.2.12 GIO1 Pin Control Register (Address: 0Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Name	W	--	--	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
Reset		--	--	0	0	0	0	0	1

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	(Reserved.)	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	(Reserved.)	
[0101]	In phase demodulator input(DMII)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	In phase demodulator external input(EXDI0)	
[1011]	External FSYNC input in RX direct mode	
[1100]	**EOP** (End Of Packet)	
[1101]~[1111]	Inhibited	

GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO1OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.13 GIO2 Pin Control Register (Address: 0Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	GIO2S3	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
Reset		--	--	0	1	0	0	0	1

GIO2S [3:0]: GIO2 pin function select.

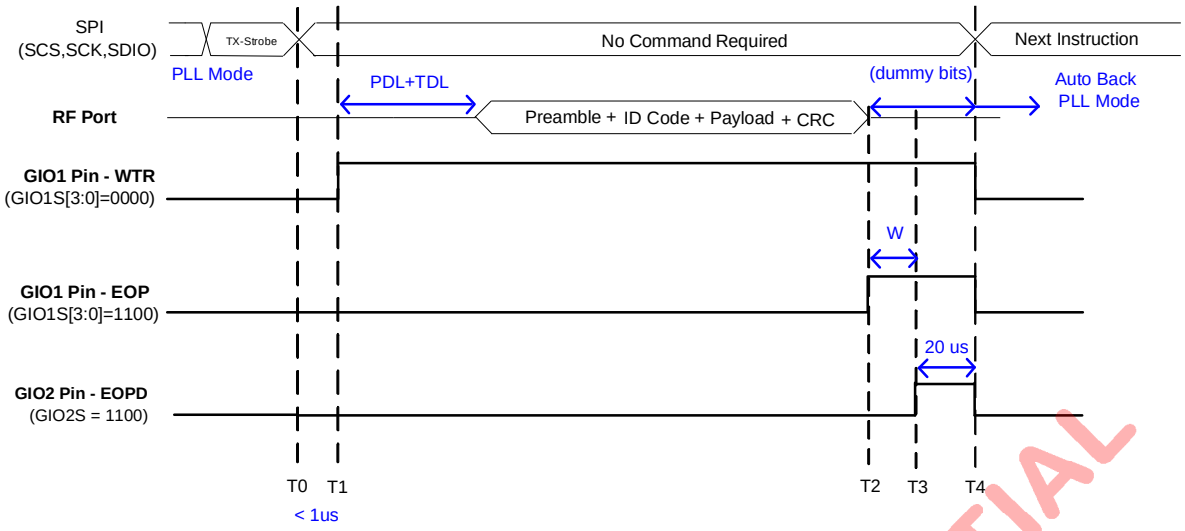
GIO2S	TX state	RX state
[0000]	WTR (Wait until TX or RX finished)	
[0001]	**PASW** (Output Signal to switch off external PA) *	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	Preamble Detect Output (PMDO)	
[0100]	(Reserved.)	
[0101]	Quadrature phase demodulator input(DMIQ)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	Quadrature phase demodulator external input(EXDI1)	
[1011]	External FSYNC input in RX direct mode	
[1100]	**EOPD** (End Of Packet Delay) *	
[1101]~[1111]	Inhibited	

* Refer to Section 14.3 for details.

GIO2I: GIO2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO2OE: GIO2 pin Output Enable.
[0]: High Z. **[1]:** Enable.

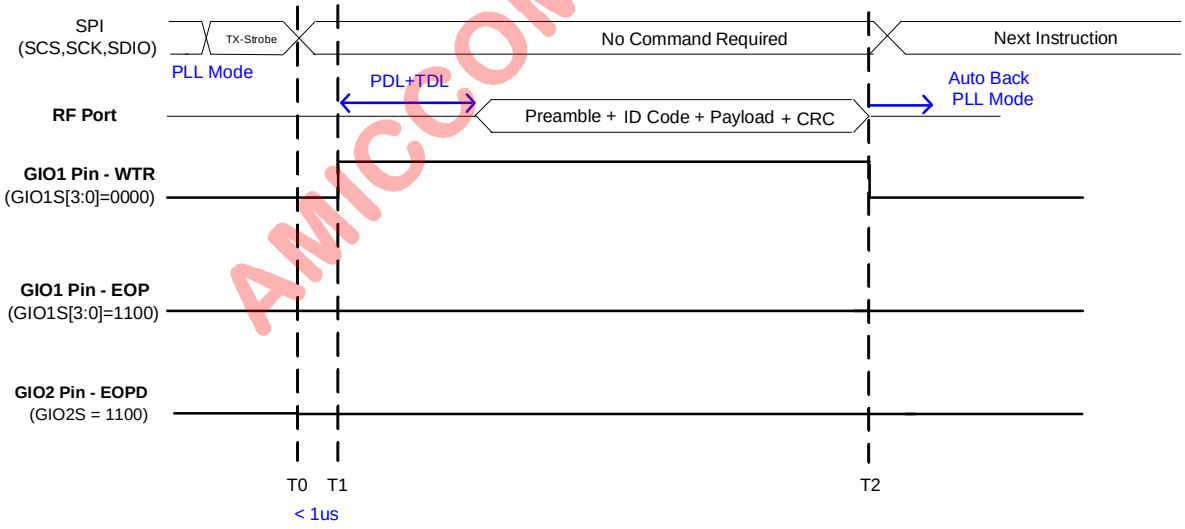
In TX Mode.
Timing diagram among WTR, EOP and EOPD are illustrated below when EOPDS = 1. However, if EOPDS = 0, T2~T4 is around 1 us only.



Preamble	ID	CRC	Payload (Byte)	W (us)
4 bytes (default)	4 bytes (recommend)	Enable	64	3.5
			32	11.5
			16	15.5
4 bytes (default)	4 bytes (recommend)	Disable	64	11.5
			32	19.5
			16	3.5

In RX Mode.

WTR goes low when last bit is recieved. Compared to TX mode, there are no dummy bits in RX mode. Hence, user can monitor the falling edge of WTR (if EOPDS=1) to turn on RX mode ahead of tunning on counterpart to TX mode for stable transmission timeslot.



9.2.14 Data Rate Clock Register (Address: 0Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	--	--
	W	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0	0	0	1	1	1	1	1

SDR [1:0]: Data rate setting.

SDR [1:0]	F_{SYCK} (Internal system clock)	Data Rate
[00]	64 MHz	2 Mbps
[01]	64 MHz	1 Mbps
[10]	64 MHz	Reserved
[11]	64 MHz	Reserved

Refer to chapter 13 for details.

GRC [3:0]: Generator Reference Counter
Due to A7125 supports different external crystals,
GRC is used to get 2 MHz Clock Generator Reference (F_{CGR}) for internal usage.
.

External Crystal (F_{XREF})	Clock Generation Reference (CGR)	GRC [3:0]
16 MHz	Must be 2 MHz	[0111]
12 MHz	Must be 2 MHz	[0101]
8 MHz	Must be 2 MHz	[0011]
6 MHz	Must be 2 MHz	[0010]

Refer to chapter 13 for details.

CGS: Clock generator enable. Shall be set to [1].
[0]: Disable. **[1]:** Enable.

XS: Crystal oscillator select. Recommend XS = [1]
[0]: Use external clock. **[1]:** Use external crystal.

9.2.15 PLL Register I (Address: 0Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

CHN [7:0]: RF LO channel number.
Change CHN to do frequency hopping. Refer to chapter 14 for details.

9.2.16 PLL Register II (Address: 0Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		0	0	1	0	1	1	1	0

DBL: Crystal frequency doubler enable.
[0]: Disable. $F_{XREF} = F_{XTAL}$. **[1]:** Enable. $F_{XREF} = 2 * F_{XTAL}$.

RRC [1:0]: RF PLL reference counter setting.

CHR [3:0]: PLL channel step setting.

Refer to chapter 14 for details.

9.2.17 PLL Register III (Address: 10h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		1	0	0	1	0	1	1	0

BIP [8:0]: LO base frequency integer part setting.
BIP [8:0] are from address (0Fh) and (10h),

IP [8:0]: LO frequency integer part value.
IP [8:0] are from address (0Fh) and (10h),

Refer to chapter 14 for details.

9.2.18 PLL Register IV (Address: 11h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--/FP15	AC14/FP14	AC13/FP13	AC12/P12	AC11/ FP11	AC10/FP10	AC9/FP9	AC8/FP8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0

9.2.19 PLL Register V (Address: 12h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	AC7/FP7	AC6/FP6	AC5/FP5	AC4/FP4	AC3/FP3	AC2/FP2	AC1/FP1	AC0/FP0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	1	0	0

BFP [15:0]: LO base frequency fractional part setting.
BFP [15:0] are from address (11h) and (12h),

AC [14:0] (Read): Frequency compensation value if AFC (19h) =1.

FP [15:0] (Read): LO frequency fractional part setting.
Refer to chapter 14 for details.

9.2.20 Channel Group Register I (Address: 13h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Name	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	1	1	1	0	0

CHGL [7:0]: PLL channel group low boundary setting.
Refer to chapter 15 for details.

9.2.21 Channel Group Register II (Address: 14h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	1	1	1	0	0	0

CHGH [7:0]: PLL channel group high boundary setting.
Refer to chapter 15 for details.

PLL frequency is divided into 3 groups:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

9.2.22 TX Register I (Address: 15h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SDMS	TMDE	TXDI	TME	--	FDP2	FDP1	FDP0
Reset		1	1	0	1	--	1	1	0

SDMS: Reserved for internal usage only. Shall be set to [1].

TMDE: TX data VCO modulation enable.
[0]: Disable. **[1]:** Enable.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert. **[1]:** Invert.

TME: TX modulation enable.
[0]: Disable. **[1]:** Enable.

FDP [2:0]: Frequency deviation power setting. Refer to control register (16h).

9.2.23 TX Register II (Address: 16h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		1	1	0	0	0	0	0	0

FD [7:0]: Frequency deviation setting.
Frequency deviation:

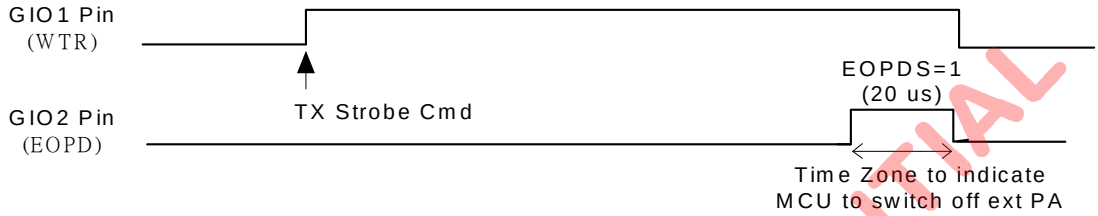
$F_{DEV} = F_{PFD} * 127 * (FD\ [7:0] + 1) * 2^{(FDP\ [2:0] + 1)} / 2^{26}$.

Recommend F_{DEV} = 500 KHz.

9.2.24 Delay Register I (Address: 17h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	EOPDS	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
Reset		0	0	0	1	0	0	1	0

EOPDS: End Of Packet Delay Select.
[0]: 1us. **[1]:** 20 us.
Recommend EOPDS = [0] in external PA free requirement.
Recommend EOPDS = [1] in external PA application. See below timing diagram.



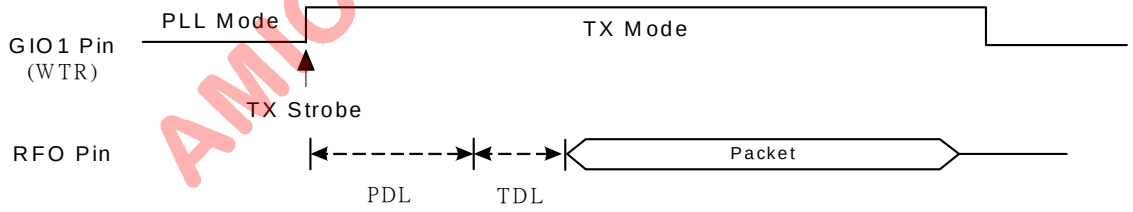
DPR [1:0]: Delay scale. Recommend DPR = [00].

TDL [1:0]: Delay for TRX settling from WPLL to TX/RX.
Delay= 20 * (TDL [1:0] + 1) * (DPR [1:0] + 1) us.

DPR [1:0]	TDL [1:0]	WPLL to TX	Note
00	00	20 us	
00	01	40 us	
00	**10**	**60 us**	**Recommend**
00	11	80 us	

PDL [2:0]: Delay for TX settling from PLL to WPLL.
Delay= 10+20 * (PDL [2:0] + 1) * (DPR [1:0] + 1) us.

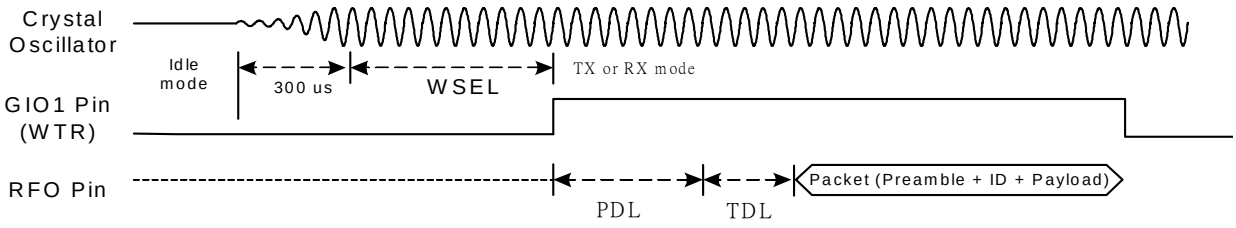
DPR [1:0]	PDL [2:0]	PLL to WPLL (LO freq. fixed)	PLL to WPLL (LO freq changed)	Note
00	**000**	**10 us**	**30 us**	**Recommend**
00	001	10 us	50 us	
00	010	10 us	70 us	
00	011	10 us	90 us	



9.2.25 Delay Register II (Address: 18h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	WSEL2	WSEL1	WSEL0	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0
Reset		0	1	0	0	0	0	0	1

WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [011].
[000]: 200us. **[001]:** 400us. **[010]:** 800us, **[011]:** 600us.
[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.



RSSC_D [1:0]: RSSI calibration switching time (10us ~ 40us). Recommend RSSC_D = [00].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

RS_DLY [2:0]: RSSI measurement delay (10us ~ 80us). Recommend RS_DLY = [001].
[000]: 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us.
[100]: 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

9.2.26 RX Register (Address: 19h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	RXSM1	RXSM0	FC	RXDI	DMG	RAW	ULS
Reset		--	1	0	0	0	0	1	0

RXSM0: Reserved for internal usage only. Shall be set to [1].

RXSM1: Reserved for internal usage only. Shall be set to [1].

AFC: Auto Frequency compensation.
[0]: Disable. **[1]:** Enable.
Refer to section 14.4 for details.

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output. **[1]:** Inverted output.

DMG: Reserved for internal usage only. Shall be set to [0].

RAW: Reserved for internal usage only. Shall be set to [1].

ULS: RX Up/Low side band select.
[0]: Up side band, **[1]:** Low side band.
Refer to section 14.2 for details.

9.2.27 RX Gain Register I (Address: 1Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	MVGS	MRHL	IGS	MGS1	MGS0	LGS2	LGS1	LGS0
Reset		0	0	0	0	0	0	0	0

MVGS: Manual VGA setting.
[0]: Auto. **[1]:** Manual.

MRHL: Manual RH, RL setting.
[0]: Auto. [1]: Manual.

IGS: Reserved for internal usage only. Shall be set to [1].

MGS [1:0]: Mixer gain attenuation select. Recommend MGS = [00].
[00]: 0dB. **[01]:** -6dB. **[10]:** -12dB. **[11]:** -18dB.

LGS [2:0]: LNA gain attenuation select. Recommend LGS = [000].
[000]: 0dB. **[001]:** -6dB. **[010]:** -12dB. **[011]:** -18dB. **[1XX]:** -24dB.

9.2.28 RX Gain Register II (Address: 1Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	RH7	RH 6	RH5	RH4	RH3	RH2	RH1	RH0
Reset		1	0	0	0	0	0	0	0

RH [7:0]: AGC calibration high threshold.

9.2.29 RX Gain Register III (Address: 1Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
Reset		1	0	0	0	0	0	0	0

RL [7:0]: AGC calibration low threshold.

9.2.30 RX Gain Register IV (Address: 1Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	MHC	LHC1	LHC0	AGCE
Reset		0	1	0	0	1	1	1	0

AVSEL [1:0]: ADC average times (AGC mode). Recommend AVSEL = [11].
[00]: No average. **[01]:** Average 2 times. **[10]:** Average 4 times. **[11]:** Average 8 times.

MVSEL [1:0]: ADC average times (VCO calibration and RSSI measurement mode). Recommend MVSEL = [01].
[00]: Average 8 times. **[01]:** Average 16 times. **[10]:** Average 32 times. **[11]:** Average 64 times.

MHC: Reserved for internal usage only. Shall be set to [0].

LHC: Reserved for internal usage only. Shall be set to [01].

AGCE: AGC active enable.
[0]: End AGC. **[1]:** AGC active.

9.2.31 RSSI Threshold Register (Address: 1Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
Reset		1	0	0	1	0	0	0	1

RTH [7:0]: Carrier detect threshold.
Refer to chapter 17 for details.

ADC [7:0]: ADC output value of temperature, RSSI .
ADC input voltage= 0.3 + 1.2 * ADC [7:0] / 256 V.
Refer to chapter 17 for details.

9.2.32 ADC Control Register (Address: 1Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RSM1	RSM0	RADC1	RADC0	FSARS	XADS	RSS	CDM
Reset		0	1	0	0	1	0	1	1

RSM [1:0]: RSSI margin = RTH – RTL. Recommend RSM = [11].
[00]: 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.
Refer to chapter 17 for details.

RADC: ADC read out average mode.
[00]: No average.
[01]: 1, 2, 4, 8 average mode. The average number is according to the setting of AVSEL (in RX Gain Register IV).
[10]: 8, 16, 32, 64 average mode. The average number is according to the setting of MVSEL (in RX Gain Register IV).
[11]: Reserved.

FSARS: ADC clock select.
[0]: 4MHz. **[1]:** 8MHz.

XADS: ADC input signal select.
[0]: Convert RSS signal. **[1]:** Reserved for internal usage.

RSS: Temperature / RSSI measurement select.
[0]: Temperature. **[1]:** RSSI or carrier-detect measurement.

CDM: RSSI measurement mode. Recommend CDM = [0].
[0]: Single mode. **[1]:** Continuous mode.

9.2.33 Code Register I (Address: 20h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	WHTS	FECS	CRCS	IDL	PML1	PML0
Reset		--	--	0	0	0	1	1	1

WHTS: Data whitening (Data Encryption) select.
[0]: Disable. **[1]:** Enable.

FECS: FEC select.
[0]: Disable. **[1]:** Enable.

CRCS: CRC select.
[0]: Disable. **[1]:** Enable.

IDL: ID code length select. Recommend IDL= [1].
[0]: 2 bytes. **[1]:** 4 bytes.

PML [1:0]: Preamble length select. Recommend PML= [11].
[00]: 1 byte. **[01]:** 2 bytes. **[10]:** 3 bytes. **[11]:** 4 bytes.

Refer to chapter 16 for details.

9.2.34 Code Register II (Address: 21h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	DCL2	DCL1	DCL0	ETH1	ETH0	PMD1	PMD0
Reset		--	1	1	1	0	1	1	1

DCL [2:0]: Demodulator DC estimation average mode. Refer to DCM (2Eh) for details.

DCL2: For payload average mode. Recommend DCL2 = [1].
[0]: 128 bits average. **[1]:** 256 bits average.

DCL1: For average and hold mode. Recommend DCL1 = [0].
[0]: 32 bits average. **[1]:** 64 bits average.

DCL0: Preamble detect delay. Count from preamble detected signal. Recommend DCL0 = [1].
[0]: 4 bits for DCL1=0, 8 bits for DCL1=1. **[1]:** 8 bits for DCL1=0, 16 bits for DCL1=1.

ETH [1:0]: ID code error tolerance. Recommend ETH = [01].
[00]: 0 bit, **[01]:** 1 bit. **[10]:** 2 bit. **[11]:** 3 bit.

PMD [1:0]: Preamble pattern detection length. Recommend PMD = [10].
[00]: 0bit. **[01]:** 4bits. **[10]:** 8bits. **[11]:** 16bits.

Refer to chapter 16 for details.

9.2.35 Code Register III (Address: 22h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		--	0	1	0	1	0	1	0

WS [6:0]: Data Whitening seed setting (data encryption key).
Refer to chapter 16 for details.

9.2.36 IF Calibration Register I (Address: 23h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	FBCF	FB3	FB2	FB1	FB0

	W	--	--	--	MFBS	MFB3	MFB2	MFB1	MFB0
Reset		--	--	--	0	0	1	1	0

MFBS: IF filter calibration value select. Recommend MFBS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MFB [3:0]: IF filter manual calibration value.

FBCF: IF filter auto calibration flag.
[0]: Pass. **[1]:** Fail.

FB [3:0]: IF filter calibration value.
MFBS= 0: Auto calibration value (AFB),
MFBS= 1: Manual calibration value (MFB).

Refer to chapter 15 for details.

9.2.37 IF Calibration Register II (Address: 24h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	FCD4	FCD3	FCD2	FCD1	FCD0
Reset		--	--	--	--	--	--	--	--

FCD [4:0]: IF filter auto calibration deviation.

9.2.38 VCO Current Calibration Register (Address: 25h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	--	--	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		--	--	1	0	1	1	0	0

VCCS: Reserved for internal usage only. Shall be set [0].

MVCS: VCO current calibration value select. Recommend MVCS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

VCOC [3:0]: VCO current manual calibration value.

FVCC: VCO current auto calibration flag.
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO current calibration value.
MVCS= 0: Auto calibration value (AVCB).
MVCS= 1: Manual calibration value (VCOC).

Refer to chapter 15 for details.

9.2.39 VCO Bank Calibration Register I (Address: 26h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	DDC1	DDC0	MDAGS	--	MVBS	MVB2	MVB1	MVB0
Reset		1	1	0	--	0	1	0	0

DDC [1:0]: VCO deviation calibration delay. Recommend DDC = [01].
Delay time = PLL delay time × (DDC + 1).

MDAGS: DAG calibration value select. Recommend MDAGS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MVBS: VCO bank calibration value select. Recommend MVBS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MVB [2:0]: VCO band manual calibration value.

VBCF: VCO band auto calibration flag.
[0]: Pass. **[1]:** Fail.

VB [2:0]: VCO bank calibration value.
MVBS= 0: Auto calibration value (AVB).
MVBS= 1: Manual calibration value (MVB).

Refer to chapter 15 for details.

9.2.40 VCO Bank Calibration Register II (Address: 27h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
Reset		1	0	0	0	0	0	0	0

MDAG [7:0]: DAG manual calibration value. Recommend MDAG = [0x80].

ADAG [7:0]: DAG auto calibration value.

9.2.41 VCO Deviation Calibration Register I (Address: 28h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
Reset		0	1	1	1	0	0	0	0

DEVS [3:0]: Deviation output scaling. Recommend DEVS = [0011].

DAMR_M: DAMR manual enable. Recommend DAMR_M = [0].
[0]: Disable. **[1]:** Enable.

VMTE_M: VMT manual enable. Recommend VMTE_M = [0].
[0]: Disable. **[1]:** Enable.

VMS_M: VM manual enable. Recommend VMS_M = [0].
[0]: Disable. **[1]:** Enable.

MSEL: VMS, VMTE and DAMR control select. Recommend MSEL = [0].
[0]: Auto control. **[1]:** Manual control.

DEVA [7:0]: Deviation output value.
MVDS= 0: Auto calibration value ((ADEV / 8) × (DEVS + 1)),
MVDS= 1: Manual calibration value (MDEV).

9.2.42 VCO Deviation Calibration Register II (Address: 29h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
Reset		0	0	1	0	1	0	0	0

MVDS: VCO deviation calibration value select. Recommend MVDS = [0].
[0]: Auto calibration value. **[1]:** Manual calibration value.

MDEV [6:0]: VCO deviation manual calibration value.

ADEV [7:0]: VCO deviation auto calibration value.

Refer to chapter 15 for details.

9.2.43 VCO Deviation Calibration Register III (Address: 2Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Reset		1	0	0	0	0	0	0	0

VMG [7:0]: Reserved for internal usage only. Shall be set to [0x80].

9.2.44 VCO Modulation Delay Register (Address: 2Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		--	--	0	0	0	0	0	0

DEVFD [2:0]: Reserved for internal usage only. Shall be set to [000].

DEVD [2:0]: Reserved for internal usage only. Shall be set to [000].

9.2.45 Battery Detect Register (Address: 2Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	BDF	--	--	--	--
	W	RGS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

RGS: VDD_D voltage setting in Sleep mode.
[0]: 3/5 * REGI. **[1]:** 3/4 * REGI.

RGV [1:0]: VDD_D and VDD_A voltage setting in non-Sleep mode. Recommend RGV = [11].
[00]: 2.1V. **[01]:** 2.0V. **[10]:** 1.9V. **[11]:** 1.8V.

QDS: Reserved for internal usage only. Shall be set [1].

BVT [2:0]: Battery voltage detect threshold.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.
[100]: 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BD_E: Battery detect enable.
[0]: Disable. **[1]:** Enable. It will be clear after battery detection done.

BDF: Battery detect flag.
[0]: Battery voltage less than threshold. **[1]:** Battery voltage greater than threshold.

Refer to chapter 19 for details.

9.2.46 TX test Register (Address: 2Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		--	--	0	1	0	1	1	1

TXCS: TX Current Setting.

PAC [1:0]: PA Current Setting.

TBG [2:0]: TX Buffer Setting.

Typical	Recommend setting			Typical
Output Power (dBm)	TXCS	TBG	PAC	TX current (mA)
3	1	7	2	21
0	1	7	0	15.7
-10	1	4	0	13.7
-20	1	0	0	13.3

Also, refer to App. Note for more setting of TX power level.

9.2.47 RX DEM test Register I (Address: 2Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DMT	DCM1	DCM0	MLP1	MLP0	SLF2	SLF1	SLF0
Reset		0	1	1	0	0	1	0	0

DMT: Reserved for internal usage only. Shall be set to [0].

DCM [1:0]: Demodulator DC estimation mode.
[00]: Fix mode (For ±10ppm crystal accuracy only). DC level is set by DCV [7:0].
[01]: Preamble hold mode. DC level is preamble average value at PMDO.
[10]: Average and hold mode. DC level is the average value at PMDO with DCL0 delay.
[11]: Payload average mode (For internal usage). DC level is payload data average.

MLP [1:0]: Reserved for internal usage only. Shall be set to [00].

SLF [2:0]: Reserved for internal usage only. Shall be set to [111].

9.2.48 RX DEM test Register II (Address: 2Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
Reset		0	1	0	0	0	0	0	0

DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].

9.2.49 Charge Pump Current Register I (Address: 30h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	1	1	1	1

CPM [3:0]: Charge pump current setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge pump current setting for VT loop. Recommend CPT = [0001].
Charge pump current = (CPT + 1) / 16 mA.

9.2.50 Charge Pump Current Register II (Address: 31h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CPTX3	CPTX2	CPTX1	CPTX0	CPRX3	CPRX2	CPRX1	CPRX0
Reset		1	1	1	1	0	0	1	1

CPTX [3:0]: Charge pump current setting for TX mode. Recommend CPTX = [0001].
Charge pump current = (CPTX + 1) / 16 mA.

CPRX [3:0]: Charge pump current setting for RX mode. Recommend CPRX = [0001].
Charge pump current = (CPRX + 1) / 16 mA.

9.2.51 Crystal test Register (Address: 32h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	--	--	DBD	XCC	XCP1	XCP0
Reset		--	--	--	--	0	1	0	0

DBD: Reserved for internal usage only. Shall be set to [0].

XCC: Reserved for internal usage only. Shall be set to [1].

XCP [1:0]: Reserved for internal usage only. Shall be set to [00].

9.2.52 PLL test Register (Address: 33h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
Reset		--	1	0	1	0	0	0	1

CPS: Reserved for internal usage only. Shall be set to [1].

PRRC [1:0]: Reserved for internal usage only. Shall be set to [00].

PRIC [1:0]: Reserved for internal usage only. Shall be set to [01].

SDPW: Reserved for internal usage only. Shall be set to [0].

NSDO: Reserved for internal usage only. Shall be set to [1].

9.2.53 VCO test Register (Address: 34h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	--	TLB1	TLB0	RLB1	RLB0	VCBS
Reset		--	--	--	1	1	0	0	0

TLB [1:0]: Reserved for internal usage only. Shall be set to [11].

RLB [1:0]: Reserved for internal usage only. Shall be set to [00].

VCBS: Reserved for internal usage only. Shall be set to [0].

9.2.54 RF Analog test Register (Address: 35h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	OLM	VTBS	CPH	CPCS	--	RFT2	RFT1	RFT0
Reset		0	0	0	0	--	0	0	0

OLM: Reserved for internal usage only. Shall be set to [0].

VTBS: Reserved for internal usage only. Shall be set to [0].

CPH: Reserved for internal usage only. Shall be set to [0].

CPCS: Reserved for internal usage only. Shall be set to [1].

RFT [2:0]: RF analog pin configuration. Recommend RFT= [000].

{XADS, RFT[2:0]}	BP_BG	BP_RSSI
[0000]	Band-gap voltage	RSSI voltage
[0001]	Analog temperature voltage	RSSI voltage
[0010]	Band-gap voltage	No connection
[0011]	Analog temperature voltage	No connection
[0100]	BPF positive in phase output	BPF negative in phase output
[0101]	BPF positive quadrature phase output	BPF negative quadrature phase output
[0110]	No connection	No connection
[0111]	No connection	No connection
[1000]	Band-gap voltage	External ADC input source
[1001]	Analog temperature voltage	External ADC input source
[1010]	Band-gap voltage	External ADC input source
[1011]	Analog temperature voltage	External ADC input source
[1100]	No connection	External ADC input source
[1101]	No connection	External ADC input source
[1110]	No connection	External ADC input source
[1111]	No connection	External ADC input source

9.2.55 IFAT Register (Address: 36h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	IGFI2	IGFI1	IGFI0	IGFQ2	IGFQ1	IGFQ0	IFBC	LIMC
Reset		1	0	0	1	0	0	1	1

IGFI [2:0]: Reserved for internal usage only. Shall be set to [111].

IGFQ [2:0]: Reserved for internal usage only. Shall be set to [111].

IFBC: Reserved for internal usage only. Shall be set to [1].

LIMC: Reserved for internal usage only. Shall be set to [1].

9.2.56 Channel Select Register (Address: 37h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
Reset		0	1	0	0	0	1	0	0

CHI [3:0]: Auto IF offset channel number setting.
F_{CHSP} * (CHI + 1) = 2MHz
Refer to chapter 14 for F_{CHSP} setting.

CHD [3:0]: The channel frequency offset for deviation calibration. If F_{CHSP} = 500KHz, recommend CHD = [0111].
Offset channel number = +/- (CHD + 1).

9.2.57 VRB Register (Address: 38h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
Reset		0	0	0	0	0	0	0	0

VTRB [3:0]: Reserved for internal usage only. Shall be set to [1111].
VMRB [3:0]: Reserved for internal usage only. Shall be set to [1111].

10. SPI

A7125 only supports one SPI bus with maximum data rate 10Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A7125. Via SPI bus, user can access **control registers** and issue **Strobe command**. Figure 10.1 gives an overview of SPI access manners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1/GIO2) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 (or GIO2) pin is data output. In such case, GIO1S (0bh) or GIO2S (0ch) should be set to [0110].

For SPI write operation, SDIO pin is latched into A7125 at the rising edge of SCK. For SPI read operation, if input address is latched by A7125, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A7125's internal state machine, it is very easy to send Strobe command via SPI bus. The Strobe command is a unique command set with total 8 commands. See section 10.3, 10.4 and 10.5 for details.

	SPI chip select	Data In	Data Out
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110)

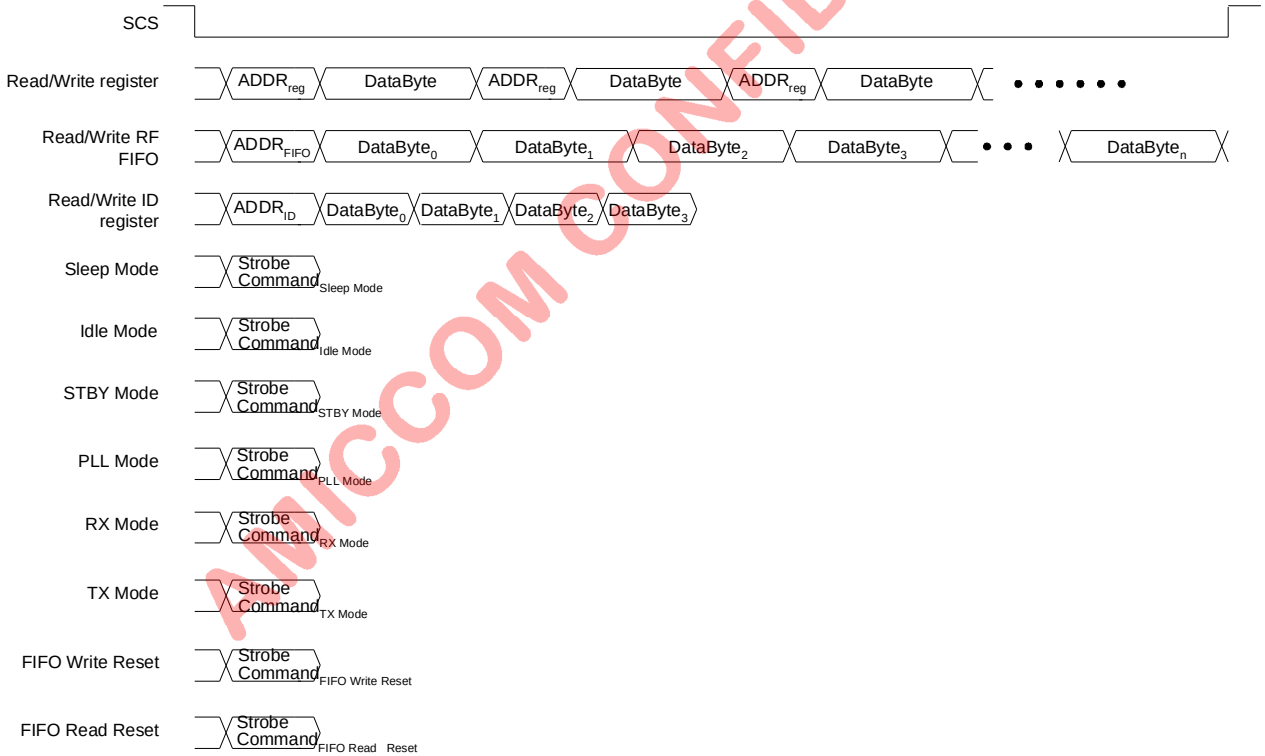


Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A7125 the following instruction is “Strobe command” or “control register”. See Table 10.1 for SPI format. Based on Table 10.1, if A7=0, A7125 is informed for control register accessing. So, A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 and Figure 10.3 for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

Bit 7: Command bit
[0]: Control register command.
[1]: Strobe command.

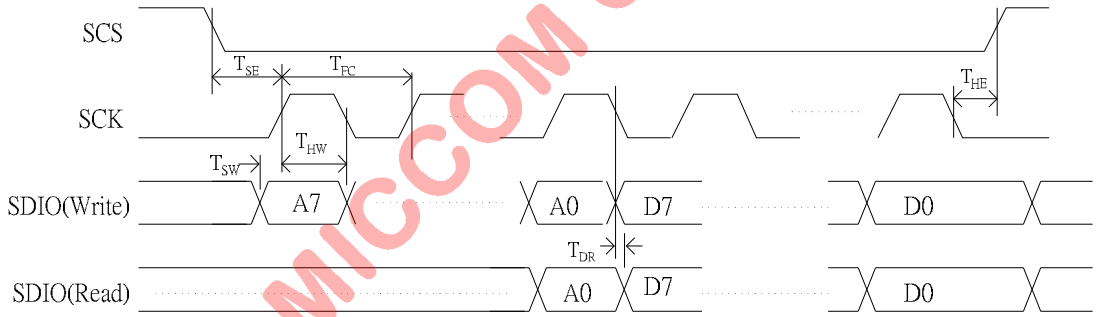
Bit 6: R/W bit
[0]: Write data to control register.
[1]: Read data from control register.

Bit [5:0]: Address of control register

Data Byte:
Bit [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI bus is configured, the maximum SPI data rate is 10 Mbps. To active SPI bus, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for details.



Parameter	Description	Min.	Max.	Unit
F_C	FIFO clock frequency.		10	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI bus read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

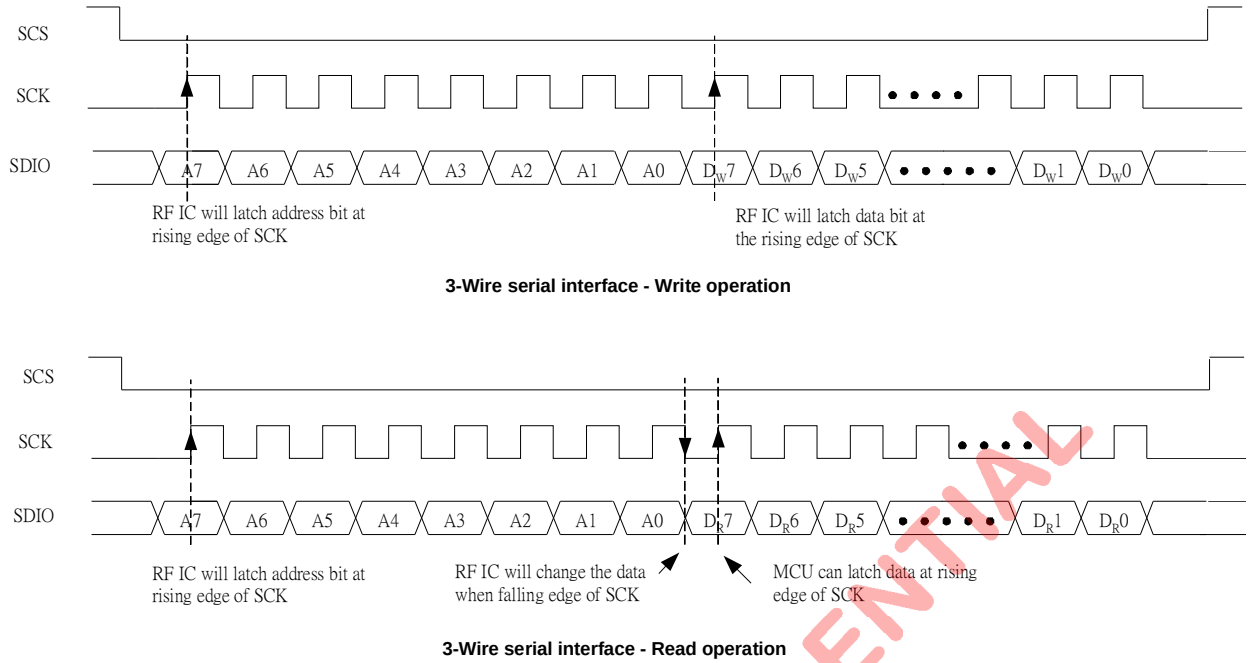


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI

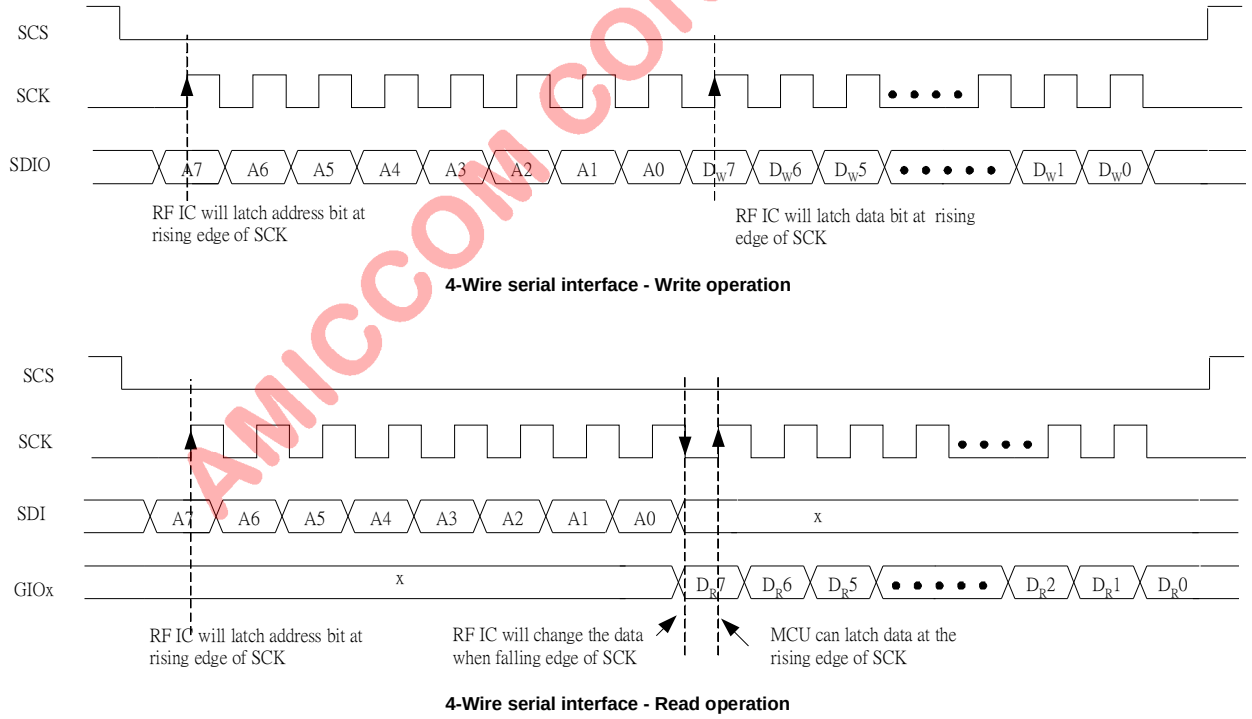


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A7125 supports 8 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode
1	1	1	0	x	x	x	x	FIFO write pointer reset
1	1	1	1	x	x	x	x	FIFO read pointer reset

Table 10.3 Strobe Commands by SPI bus

10.4.1 Strobe Command - Sleep Mode

Refer to Table 10.3, user can issue 4 bits (1000) Strobe command directly to set A7125 into Sleep mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	0	0	0	0	Sleep mode

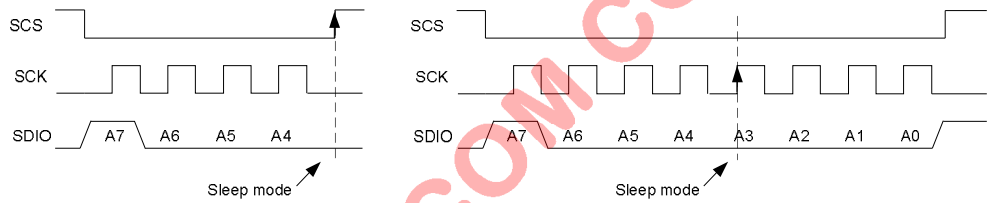


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe command directly to set A7125 into Idle mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	x	x	x	Idle mode

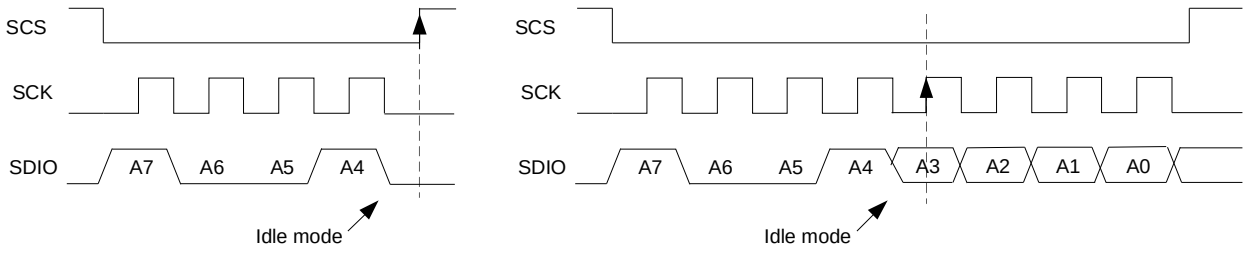


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe command directly to set A7125 into Standby mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	x	x	x	Standby mode

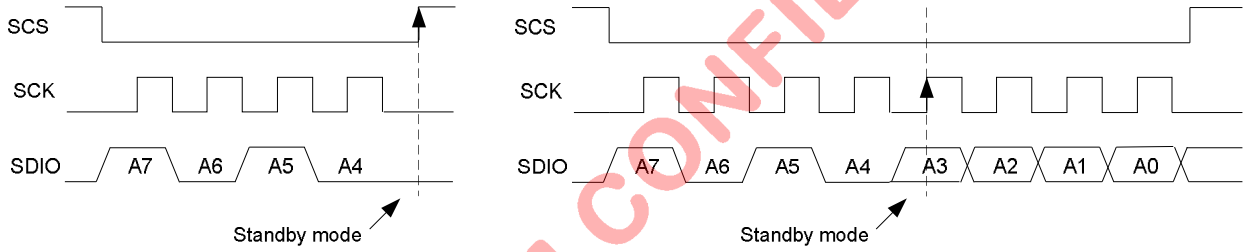


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe command directly to set A7125 into PLL mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	x	x	x	PLL mode

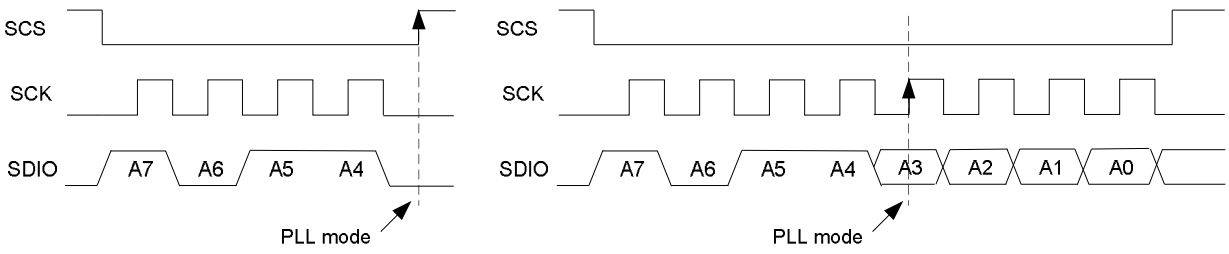


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - RX Mode

Refer to Table 10.3, user can issue 4 bits (1100) Strobe command directly to set A7125 into RX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	x	x	x	x	RX mode

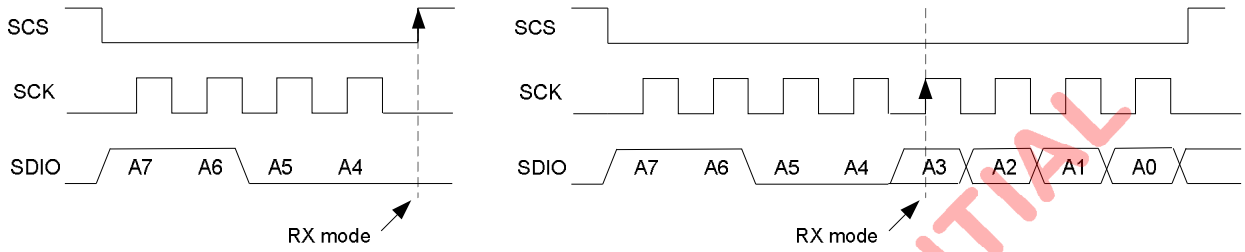


Figure 10.8 RX mode Command Timing Chart

10.4.6 Strobe Command - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe command directly to set A7125 into TX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

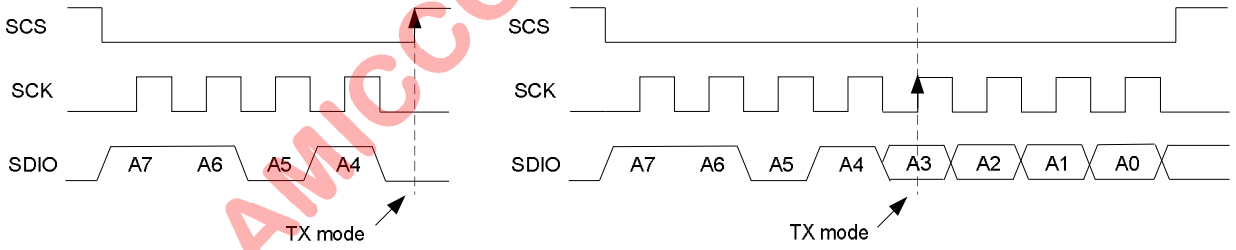


Figure 10.9 TX mode Command Timing Chart

10.4.7 Strobe Command – FIFO Write Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1110) Strobe command directly to reset A7125 FIFO write pointer. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	FIFO write pointer reset

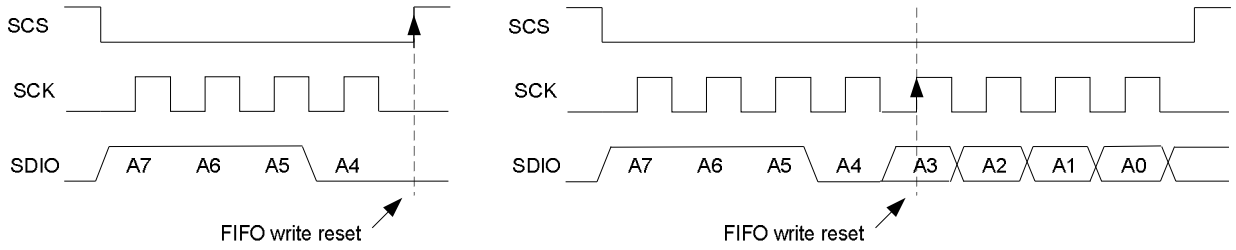


Figure 10.10 FIFO write pointer reset Command Timing Chart

10.4.8 Strobe Command – FIFO Read Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1111) Strobe command directly to reset A7125 FIFO read pointer. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	1	x	x	x	x	FIFO read pointer reset

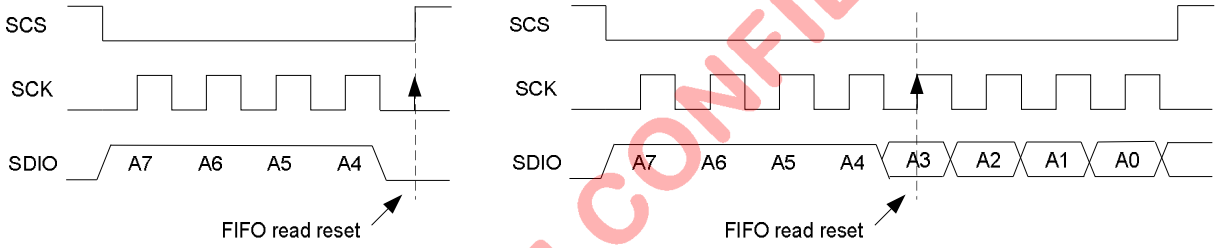


Figure 10.11 FIFO read pointer reset Command Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A7125 by setting Mode Register (00h) through SPI bus as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A7125 is informed to generate internal signal "RESETN" to initial itself. After reset command, A7125 is in standby mode.

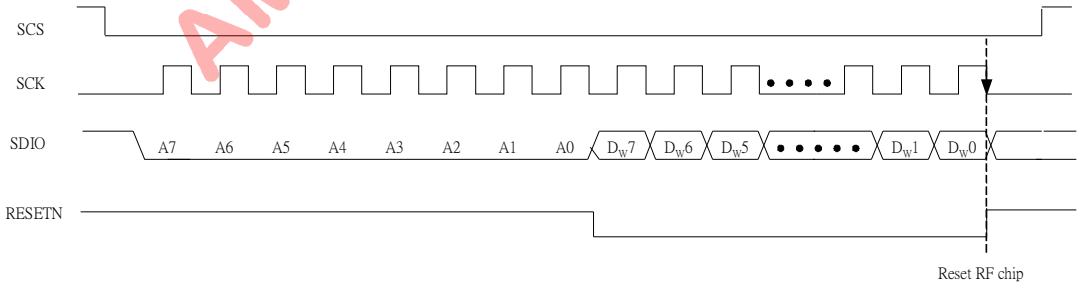


Figure 10.12 Reset Command Timing Chart

10.6 ID Accessing Command

A7125 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI bus. ID length is recommended to be 32 bits by setting IDL (20h).

Figure 10.13 and 10.14 are timing charts of 32-bits ID accessing via 3-wire SPI.

10.6.1 ID Write Command

User can refer to Figure 10.2 for SPI write timing chart. Below is the procedure of ID write command.

Step1: Deliver A7~A0 = 00000110 (A7=0 for control register, A6=0 for write operation, ID addr = 06h).
Step2: Via SDIO pin, 32-bits ID are written in sequence by Data Byte 0, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

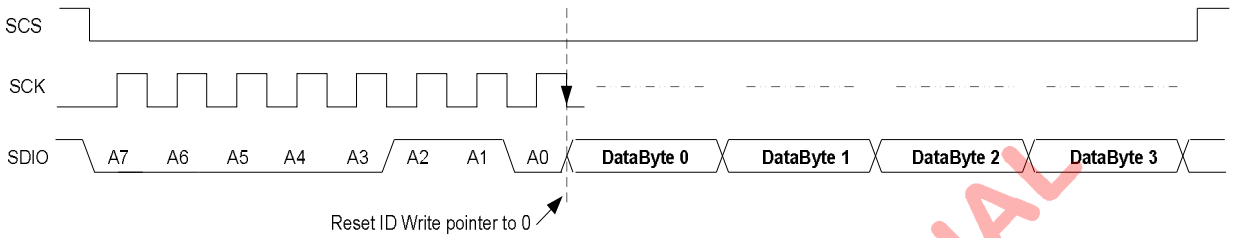


Figure 10.13 ID Write Command Timing Chart

10.6.2 ID Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of ID read command.

Step1: Deliver A7~A0 = 01000110 (A7=0 for control register, A6=1 for read operation, ID addr = 06h).
Step2: Via SDIO pin, 32-bits ID are read in sequence by Data Byte 0, 1, 2 and 3.
Step3: Toggle SCS pin to high when step2 is completed.

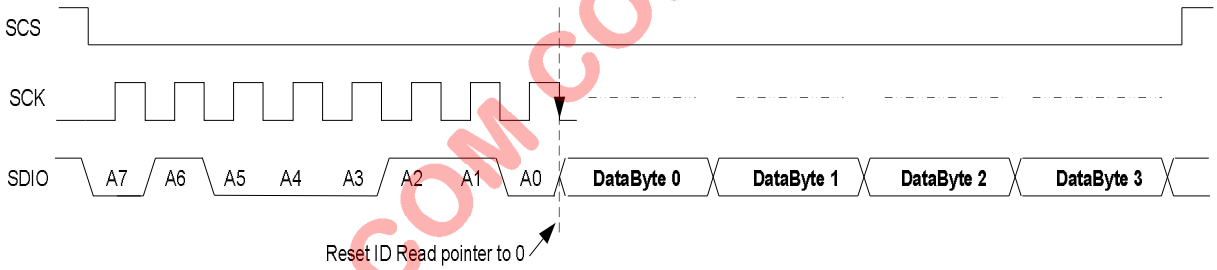


Figure 10.14 ID Read Command Timing Chart

10.7 FIFO Accessing Command

A7125 has separated TX / RX FIFO, user just needs to set FMS (01h) =1 to enable FIFO mode. In FIFO mode, before packet is delivered, write wanted data into TX FIFO and issue TX strobe command. Similarly, user can read RX FIFO once packet is received.

User can choose polling or interrupt scheme for FIFO accessing. FIFO status is output via GIO1 (or GIO2) pin by setting GIO1 (0Bh) or GIO2 (0Ch).

See Figure 10.15 and 10.16 for timing charts of FIFO accessing via 3-wire SPI.

10.7.1 TX FIFO Write Command

User can refer to Figure 10.2 for SPI write timing chart. Below is the procedure of TX FIFO write command.

Step1: Deliver A7~A0 = 00000101 (A7=0 for control register, A6=0 for write operation, FIFO addr = 05h).
Step2: Via SDIO pin, write (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send TX Strobe command for packet transmitting. Refer to Figure 10.9.

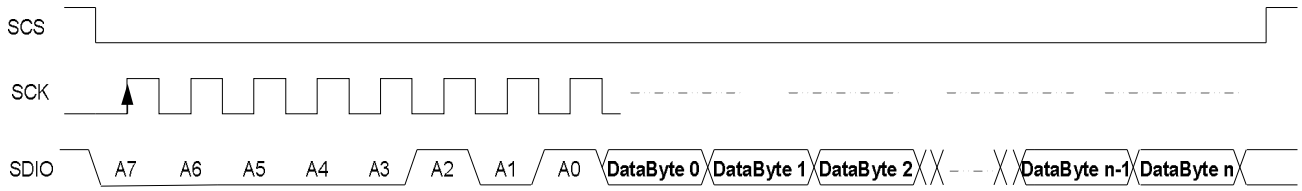


Figure 10.15 TX FIFO Write Command Timing Chart

10.7.2 Rx FIFO Read Command

User can refer to Figure 10.2 for SPI read timing chart. Below is the procedure of RX FIFO read command.

Step1: Deliver A7~A0 = 01000101 (A7=0 for control register, A6=1 for read operation, FIFO addr = 05h).
Step2: Via SDIO pin, RX FIFO is read in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when RX FIFO is read completely.

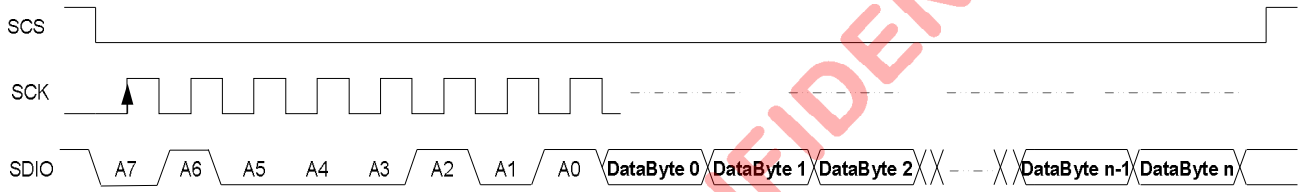


Figure 10.16 RX FIFO Read Command Timing Chart

11. State machine

In chapter 9 and chapter 10, user can learn both accessing A7125's control registers as well as issuing Strobe commands. From section 10.2 ~ 10.6, it is clear to know configurations of 3-wire SPI and 4-wire SPI, Strobe command, software reset, and how to access ID Registers and TX/RX FIFO.

In section 11.1, built-in state machine is introduced. Then, combined with Strobe command, software reset and A7125's control registers, section 11.2 , 11.3 and 11.4 demonstrate 3 state diagrams to explain how transitions of A7125's operation.

From accessing data point of view, if FMS=1 (01h), FIFO mode is enabled, otherwise, A7125 is in direct mode. If FMS=1 and FIFO Read/Write at standby mode, we call it is Normal FIFO mode. Otherwise, If FMS=1 and FIFO Read/Write at PLL mode, we called it is Quick FIFO mode due to the reduction of PLL settling time. If FMS=1 and FIFO Read/Write at IDLE mode, we called it is Power Saving FIFO mode due to the reduction of average current.

	SPI chip select	Data In	Data Out	Operation Mode	Clock Recovery for Direct Mode
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin	FIFO (FMS=1) Direct(FMS=0)	CKO pin (CKOS = 0001)
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110) / GIO2 (GIO2S=0110)	FIFO (FMS=1) Direct(FMS=0)	CKO pin (CKOS = 0001)

(1) Normal FIFO Mode (FMS=1 and FIFO R/W @ Standby mode)
(2) Quick FIFO Mode (FMS=1 and FIFO R/W @ PLL mode)
(3) Power Saving FIFO Mode (FMS=1 and FIFO R/W @ IDLE mode)
(4) Quick Direct Mode (FMS=0 and FIFO ignored, write packet @ TX mode, read packet @ RX mode)

11.1 Key states

A7125 supports 7 key operation states. Those are,
(1) Standby mode
(2) Sleep mode
(3) Idle mode
(4) PLL mode
(5) TX mode
(6) RX mode
(7) CAL mode

After power on reset or software reset, A7125 is automatically into standby mode. Then, user has to do calibration process because all control registers are in initial values. The calibration process of A7125 is very easy, user only needs to issue Strobe commands and enable calibration registers. If so, the calibrations are automatically completed by A7125's internal state machine. See 11.2, 11.3, 11.4 and chapter 15 for details. After calibration, A7125 is ready to do TX and RX operation. User can start wireless transmission.

11.1.1 Standby mode

When Standby Strobe is issued, A7125 enters standby mode automatically. Internal power management is listed below. Be noted that A7125 is in standby mode after power on reset or software reset.

Standby mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	OFF	OFF	OFF	OFF	(1010xxxx)b See Figure 10.6

11.1.2 Sleep mode

When Sleep Strobe is issued, A7125 enters sleep mode automatically. In sleep mode, A7125 still can accept other strobe commands via SPI bus. But, A7125 can not support Read/Write FIFO in sleep mode. Internal power management is listed below.

Sleep mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
OFF	OFF	OFF	OFF	OFF	OFF	(1000xxxx)b See Figure 10.4

11.1.3 Idle mode

When Idle Strobe is issued, A7125 enters idle mode automatically. In idle mode, A7125 can accept other strobe commands as well as supporting Read/Write FIFO. Internal power management is listed below.

Idle mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	OFF	OFF	OFF	OFF	OFF	(1001xxxx)b See Figure 10.5

11.1.4 PLL mode

When PLL Strobe is issued, A7125 enters PLL mode automatically. In PLL mode, internal PLL and VCO are both turned on to generate LO (local oscillator) frequency before TX and RX operation. Internal power management is listed below. According to PLL Register I, II, III, IV and V, PLL circuitry is easy to control by user's definition.

PLL mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	OFF	(1011xxxx)b See Figure 10.7

11.1.5 TX mode

When TX Strobe is issued, A7125 enters TX mode automatically for data delivery. Internal power management is listed below.

Be notice,

(1) If A7125 is in FIFO mode, TX data packet (Preamble + ID + Payload) is delivered through TX circuitry. Then, A7125 supports auto-back function to previous state for the next packet.

(2) If A7125 is in direct mode, TX data packet is also delivered through TX circuitry. Then, A7125 stays in TX mode. User has to issue Strobe command to back to previous state.

TX mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	ON	(1101xxxx)b See Figure 10.9

11.1.6 RX mode

When RX Strobe is issued, A7125 enters RX mode automatically for data receiving. Internal power management is listed below.

Be notice,

(1) If A7125 is in FIFO mode, RX data packet is caught through RX circuitry. Then, A7125 supports auto-back function to previous state for next receiving packet.

(2) If A7125 is in direct mode, RX data packet is also caught through RX circuitry. Then, A7125 stays in RX mode. User has to issue Strobe command to back to previous state.

RX mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	ON	OFF	(1101xxxx)b See Figure 10.9

11.1.7 CAL mode

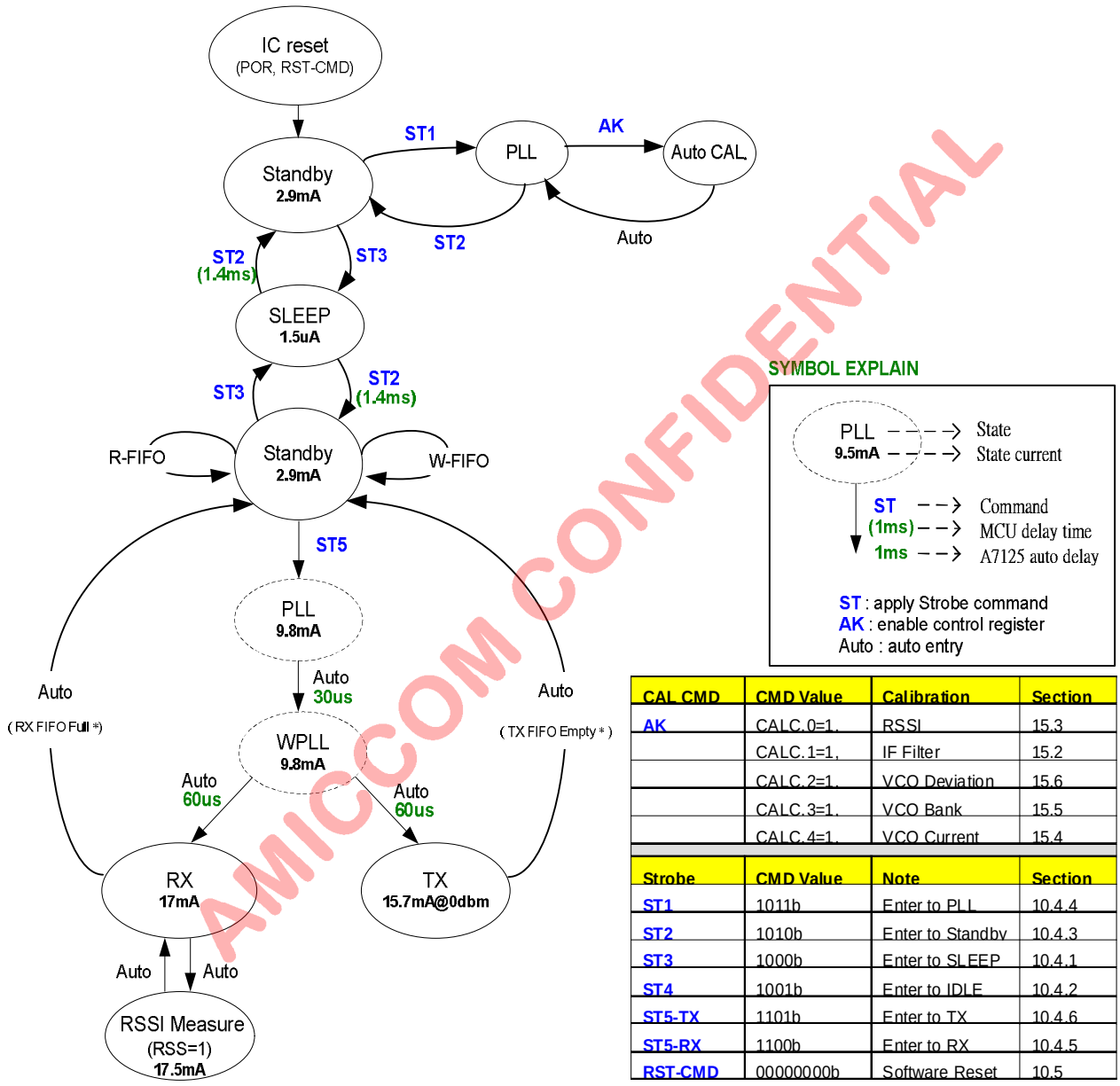
Calibration process shall be done after power on reset or software reset. Calibration items include VCO, IF Filter and RSSI. It is easy to implement calibration process by Strobe command and enable CALC (02h) control register. See chapter 15 for details.

Be noted that VCO Calibration is executed in PLL mode only. However, IF Filter and RSSI Calibration can be executed in Standby or PLL mode.

11.2 Normal FIFO Mode

This mode is suitable for requirement of general purpose applications. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet data transceiving, only one Strobe command is needed. Once transmission is done, A7125 is auto back to standby mode.

If all packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7125 staying in sleep mode. Figure 11.1 is the state diagram of Normal FIFO mode.



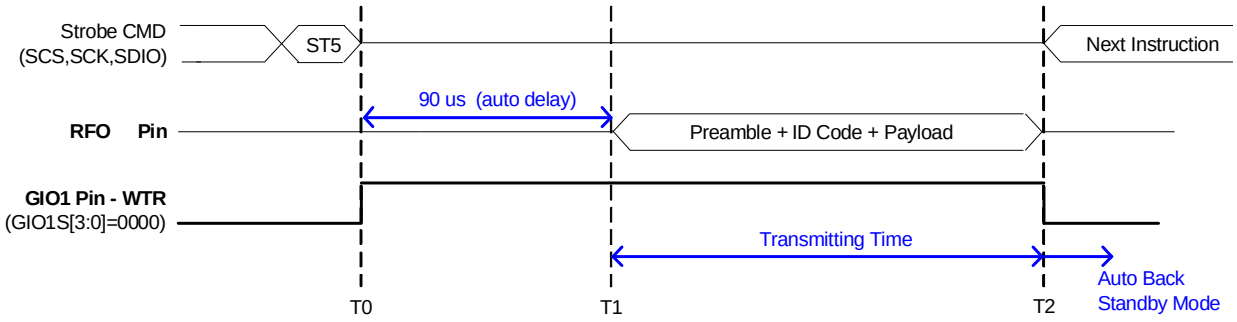
CAL CMD	CMD Value	Calibration	Section
AK	CALC.0=1,	RSSI	15.3
	CALC.1=1,	IF Filter	15.2
	CALC.2=1,	VCO Deviation	15.6
	CALC.3=1,	VCO Bank	15.5
	CALC.4=1,	VCO Current	15.4

Strobe	CMD Value	Note	Section
ST1	1011b	Enter to PLL	10.4.4
ST2	1010b	Enter to Standby	10.4.3
ST3	1000b	Enter to SLEEP	10.4.1
ST4	1001b	Enter to IDLE	10.4.2
ST5-TX	1101b	Enter to TX	10.4.6
ST5-RX	1100b	Enter to RX	10.4.5
RST-CMD	00000000b	Software Reset	10.5

- Be notice, refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.

Figure 11.1 State diagram of Normal FIFO Mode

From Figure 11.1, when ST5 command is issued for TX operation, see Figure 11.2 for detailed timing. A7125 status can be represented to GIO1 or GIO2 pin to MCU for timing control.

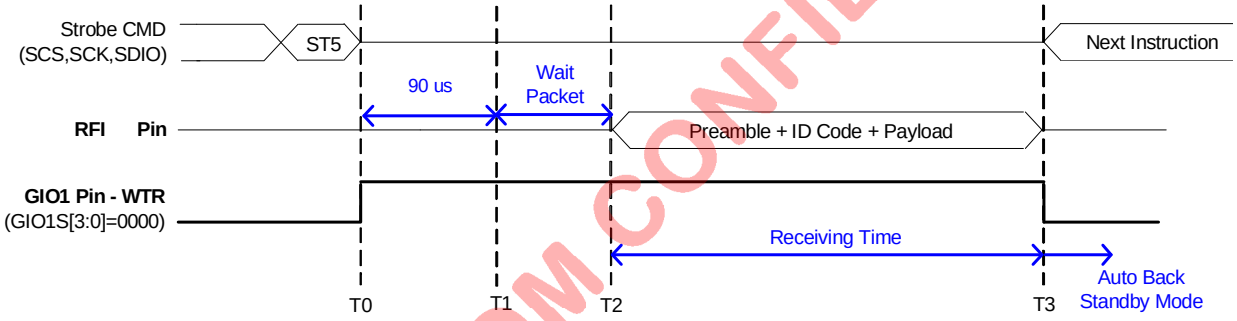


T0-T1: Auto Delay by Register setting (PDL + TDL)

LO Freq.	Standby to WPLL (PDL)	WPLL to TX (TDL)	TX Ready Time
Changed	30 us	60 us	90 us
No Changed	30 us	60 us	90 us

Figure 11.2 Transmitting Timing Chart of Normal FIFO Mode

From Figure 11.1, when ST5 command is issued for RX operation, see Figure 11.3 for detailed timing. A7125 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



T0-T1: RX Settling.
T1-T2: RX is ready, Wait for valid packet

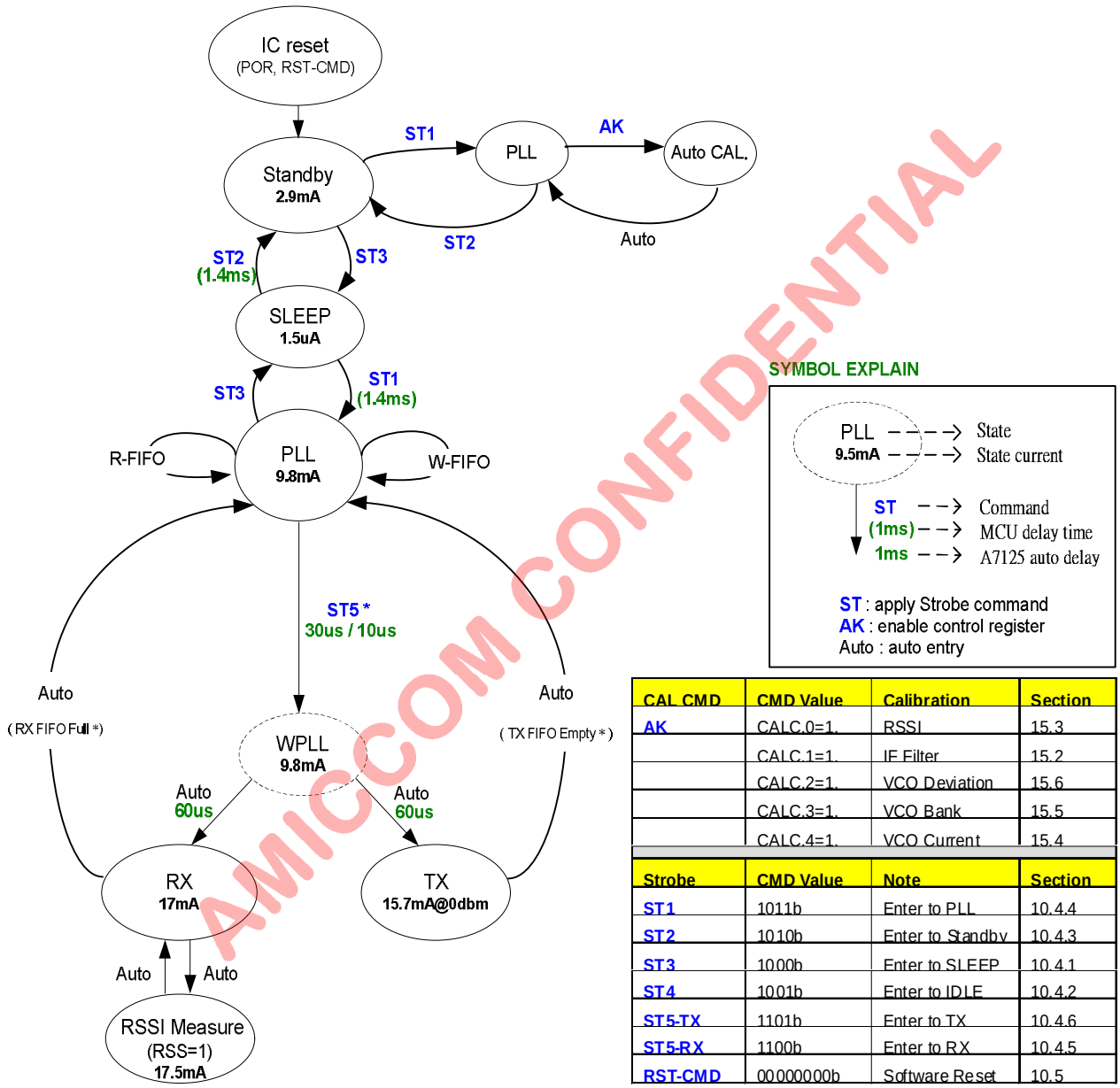
LO Freq.	Standby to WPLL	WPLL to RX	RX Ready Time
Changed	30 us	60 us	90 us
No Changed	30 us	60 us	90 us

Figure 11.3 Receiving Timing Chart of Normal FIFO Mode

11.3 Quick FIFO Mode

This mode is suitable for requirement of fast transceiving. After calibration flow, user can issue Strobe command to enter PLL mode where write TX FIFO or read RX FIFO. From PLL mode to packet data transceiving, only one Strobe command is needed. Once transmission is done, A7125 is auto back to PLL mode.

When packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7125 staying in sleep mode. Figure 11.4 is the state diagram of Quick FIFO mode.



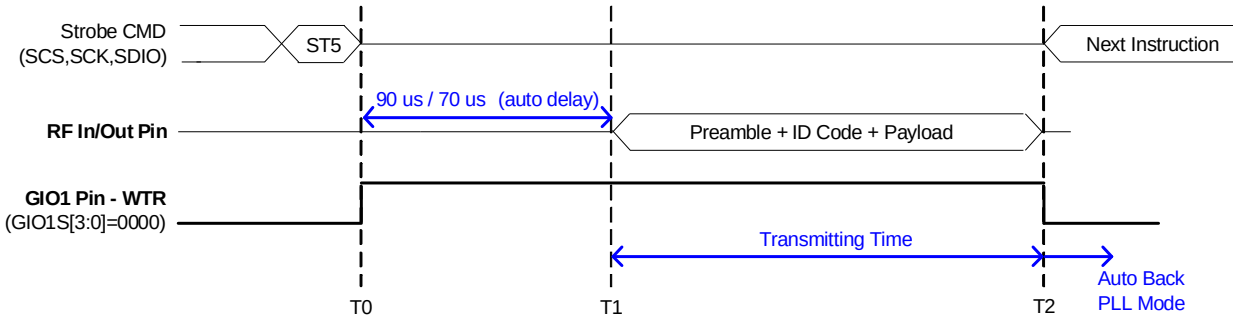
CAL CMD	CMD Value	Calibration	Section
AK	CALC.0=1.	RSSI	15.3
	CALC.1=1.	IF Filter	15.2
	CALC.2=1.	VCO Deviation	15.6
	CALC.3=1.	VCO Bank	15.5
	CALC.4=1.	VCO Current	15.4

Strobe	CMD Value	Note	Section
ST1	1011b	Enter to PLL	10.4.4
ST2	1010b	Enter to Standby	10.4.3
ST3	1000b	Enter to SLEEP	10.4.1
ST4	1001b	Enter to IDLE	10.4.2
ST5-TX	1101b	Enter to TX	10.4.6
ST5-RX	1100b	Enter to RX	10.4.5
RST-CMD	00000000b	Software Reset	10.5

- Be notice, refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.
- Be notice, ST5 delay time is either 70 us (LO frequency changed) or 10 us (LO frequency NOT changed)

Figure 11.4 State diagram of Quick FIFO Mode

From Figure 11.4, when ST5 command is issued for TX operation, see Figure 11.5 for detailed timing. A7125 status can be represented to GIO1 or GIO2 pin to MCU for timing control.

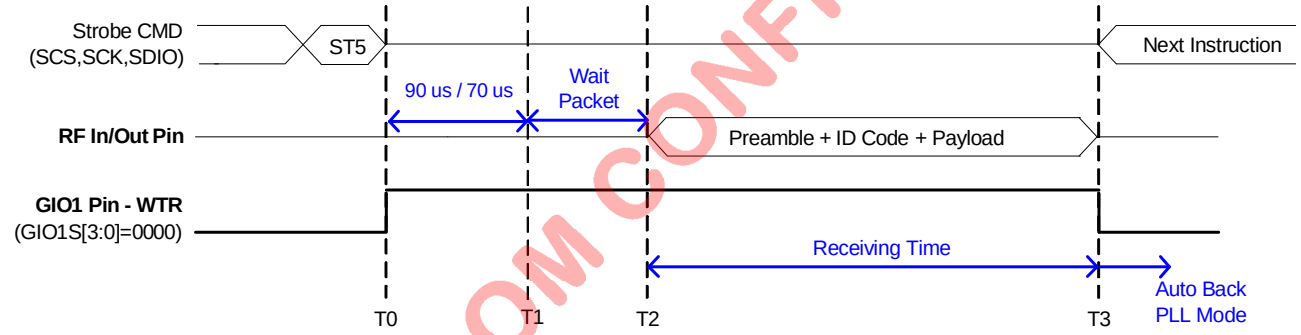


T0-T1: Auto Delay by Register setting(PDL+TDL)

LO Freq.	PLL to WPLL (PDL)	WPLL to TX (TDL)	TX Ready Time
Changed	30 us	60 us	90 us
No Changed	10 us	60 us	70 us

Figure 11.5 Transmitting Timing Chart of Quick FIFO Mode

From Figure 11.4, when ST5 command is issued for RX operation, see Figure 11.6 for detailed timing. A7125 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



T0-T1: RX Settling by register setting (PDL+TDL).
T1-T2: RX is ready, Wait for valid packet

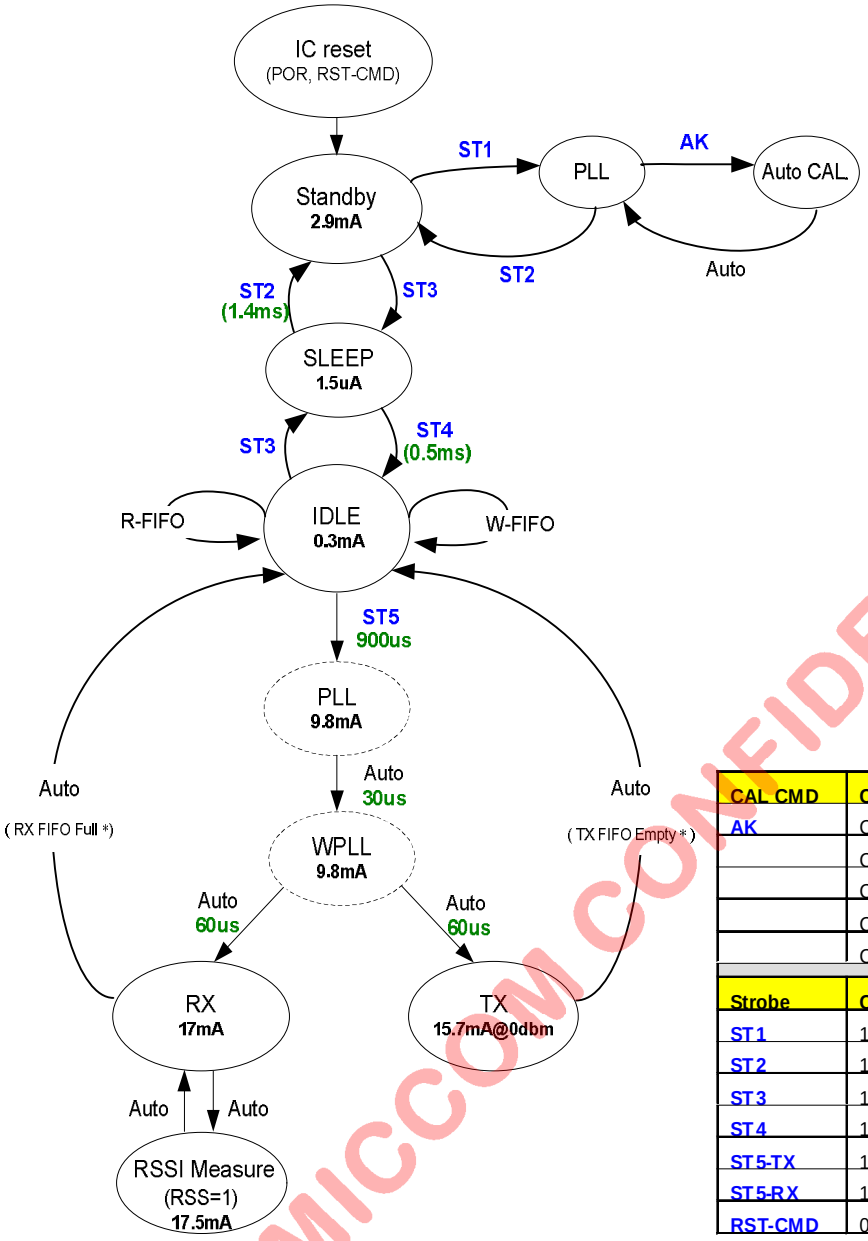
LO Freq.	Standby to WPLL (PDL)	WPLL to RX (TDL)	RX Ready Time
Changed	30 us	60 us	90 us
No Changed	10 us	60 us	70 us

Figure 11.6 Receiving Timing Chart of Quick FIFO Mode

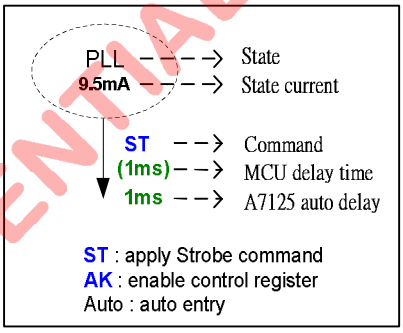
11.4 Power Saving FIFO Mode

This mode is suitable for requirement of low power consumption. After calibration flow, user can issue Strobe command to enter idle mode where write TX FIFO or read RX FIFO. From idle mode to packet data transceiving, only one Strobe command is needed. Once transmission is done, A7125 is auto back to idle mode.

When packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7125 staying in sleep mode. Figure 11.7 is the state diagram of Power Saving FIFO mode.



SYMBOL EXPLAIN



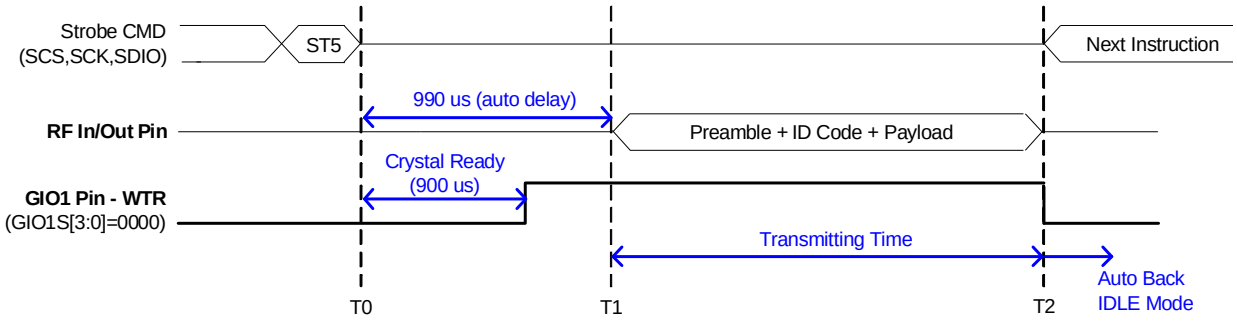
CAL CMD	CMD Value	Calibration	Section
AK	CALC.0=1.	RSSI	15.3
	CALC.1=1.	IF Filter	15.2
	CALC.2=1.	VCO Deviation	15.6
	CALC.3=1.	VCO Bank	15.5
	CALC.4=1.	VCO Current	15.4

Strobe	CMD Value	Note	Section
ST1	1011b	Enter to PLL	10.4.4
ST2	1010b	Enter to Standby	10.4.3
ST3	1000b	Enter to SLEEP	10.4.1
ST4	1001b	Enter to IDLE	10.4.2
ST5-TX	1101b	Enter to TX	10.4.6
ST5-RX	1100b	Enter to RX	10.4.5
RST-CMD	00000000b	Software Reset	10.5

- Be notice, refer to chapter 16 for definition of RX FIFO Full and TX FIFO Empty.

Figure 11.7 State diagram of Power Saving FIFO Mode

From Figure 11.7, when ST5 command is issued for TX operation, see Figure 11.8 for detailed timing. A7125 status can be represented to GIO1 or GIO2 pin to MCU for timing control.

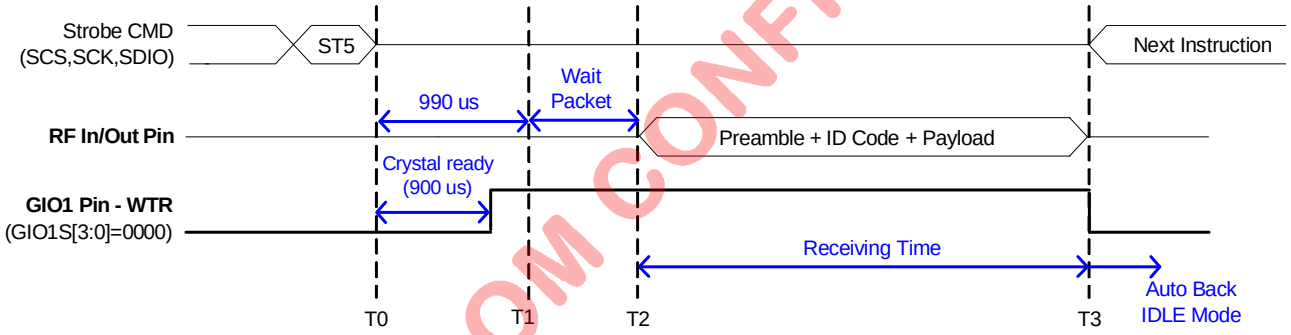


T0-T1: Auto Delay by Register setting (WSEL+PDL+TDL)

LO Freq.	IDLE to PLL (WSEL, Crystal Ready)	PLL to WPLL (PDL)	WPLL to TX (TDL)	TX Ready Time
Changed	300+600 us	30 us	60 us	990 us
No Changed	300+600 us	30 us	60 us	990 us

Figure 11.8 Transmitting Timing Chart of Power Saving FIFO Mode

From Figure 11.7, when ST5 command is issued for RX operation, see Figure 11.9 for detailed timing. A7125 status can be represented to GIO1 or GIO2 pin to MCU for timing control.



T0-T1: Crystal Ready + RX settling by register setting (WSEL+PDL+TDL)
T1-T2: RX is ready, Wait for valid packet

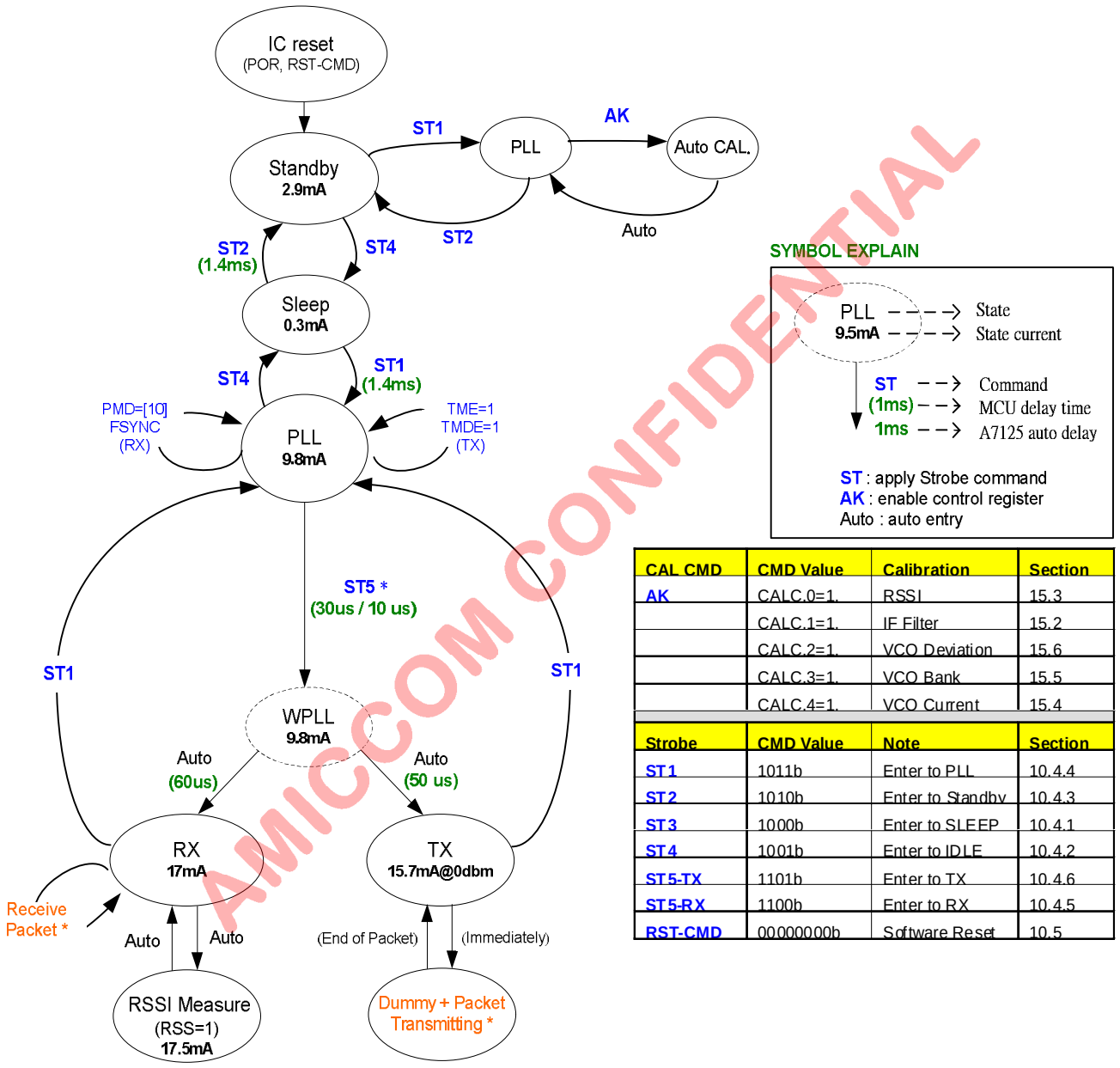
LO Freq.	IDLE to PLL (WSEL)	WPLL to RX (TDL)	WPLL to RX (TDL)	RX Ready Time
Changed	300+600 us	30 us	60 us	990 us
No Changed	300+600 us	30 us	60 us	990 us

Figure 11.9 Receiving Timing Chart of Power Saving FIFO Mode

11.5 Quick Direct Mode

This mode is suitable for fast transceiving. After calibration flow, for every state transition, user has to issue Strobe command to A7125.This mode is also suitable for the requirement of versatile packet format. Noted that user needs to take care the transition time by MCU's timer.

When packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7125 staying in idle mode (or sleep mode). Figure 11.3 is the state diagram of Quick Direct mode.



CAL CMD	CMD Value	Calibration	Section
AK	CALC.0=1.	RSSI	15.3
	CALC.1=1.	IF Filter	15.2
	CALC.2=1.	VCO Deviation	15.6
	CALC.3=1.	VCO Bank	15.5
	CALC.4=1.	VCO Current	15.4

Strobe	CMD Value	Note	Section
ST1	1011b	Enter to PLL	10.4.4
ST2	1010b	Enter to Standby	10.4.3
ST3	1000b	Enter to SLEEP	10.4.1
ST4	1001b	Enter to IDLE	10.4.2
ST5-TX	1101b	Enter to TX	10.4.6
ST5-RX	1100b	Enter to RX	10.4.5
RST-CMD	00000000b	Software Reset	10.5

- Be notice, Dummy stands for dummy preamble.
- Be notice, ST5 delay time is either 70 us (LO frequency changed) or 10 us (LO frequency NOT changed)

Figure 11.10 State diagram of Quick Direct Mode

From Figure 11.10, when PLL mode transits to WPLL mode, LO (local oscillator) frequency changed or not will induce different PLL setting time by either 70us or 10 us. Therefore, MCU total delay time is different. See Table 11.1 for details.

LO Freq.	PLL to WPLL	WPLL to TX	TX Ready Time
Changed	30 us	50 us	80 us
No Changed	10 us	50 us	60 us

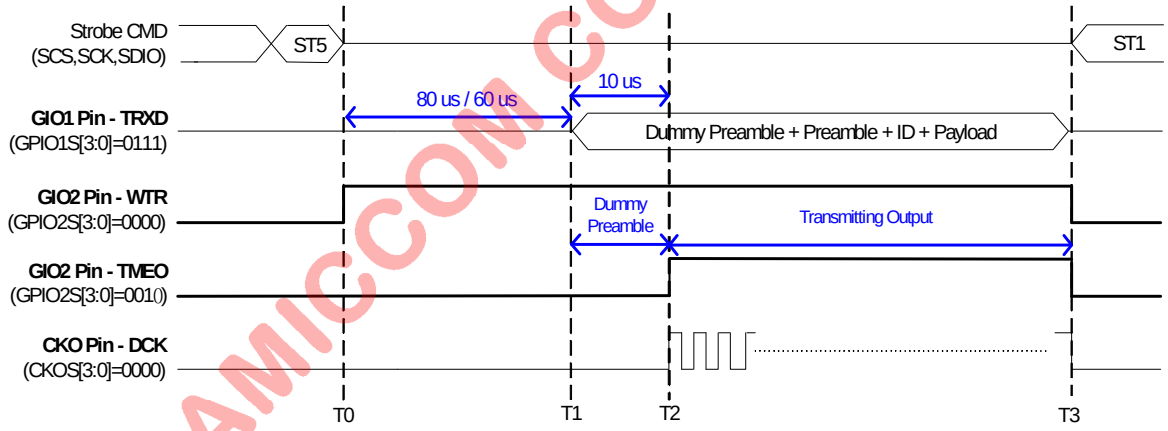
Table 11.1 MCU total delay time from PLL to TX mode.

From Figure 11.10, when A7125 enters TX mode, MCU should immediately deliver dummy preamble and defined packet to A7125's GIO1 or GIO2 pin. Dummy preamble is used to stabilize TX circuitry. See Table 11.2 for details.

A7125 Data Rate	Dummy Preamble	Packet			Note
		Preamble	ID	Max Payload	
1 Mbps	10 bits	32 bits	32 bits	512 bytes	Total Preamble = 42 bits
2 Mbps	20 bits	32 bits	32 bits	512 bytes	Total Preamble = 52 bits

Table 11.2 Format of dummy preamble and packet.

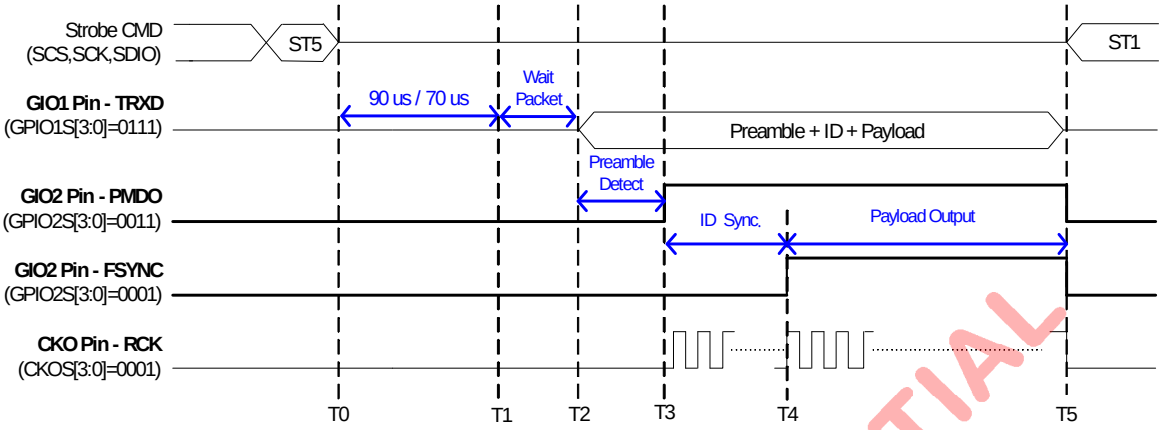
From Figure 11.10, Table 11.1 and 11.2, MCU total delay time and dummy preamble are important for quick direct mode. When ST5 command is issued for TX operation, see Figure 11.4 for detailed timing. A7125 status can be represented to GIO1 and GIO2 pin to MCU for timing control.



T0-T1: MCU Total Delay Time, Refer to Table 11.1
T1-T2: Dummy Preamble, Refer to Table 11.2
T2: TMEO (TX Modulation Enable) is auto triggered
T2-T3: Transmitting Time

Figure 11.11 Transmitting Timing Chart of Quick Direct Mode

From Figure 11.3, Table 11.1 and 11.2, RX settling time is important for quick direct mode. When ST5 command is issued for RX operation, after RX settling and preamble detect, A7125 offers ID sync function (if 32 bits ID is stored in ID Register) to generate FSYNC signal to inform MCU. Figure 11.5 is the detailed timing. A7125 status can be represented to GIO1 and GIO2 pin to MCU for timing control.



T0-T1: RX Ready Time
T1-T2: RX is ready, wait for valid packet
T2-T3: Preamble Detect
T3-T4: ID Sync
T4-T5: Payload Output

LO Freq.	PLL to WPLL	WPLL to RX	RX Ready Time
Changed	30 us	60 us	90 us
No Changed	10 us	60 us	70 us

Figure 11.12 Receiving Timing Chart of Quick Direct Mode

12 Crystal Oscillator Circuit

A7125 needs external crystal or external clock that is either 6 or 8/12/16 MHz, to generate internal wanted clock.
Be notice if 6MHz external crystal (clock) is selected, A7125 only supports 1Mbps data rate.

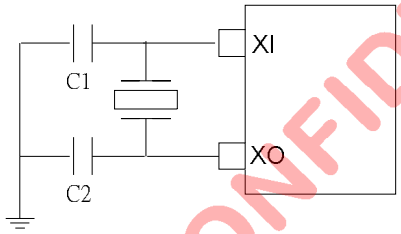
Relative Control Register

Data Rate Clock Register (Address: 0Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	--	--
	W	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0	0	0	1	1	1	1	1

12.1 Use External Crystal

To use external crystal, user just sets XS= 1 (0Dh) to enable crystal oscillator. Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance are used to adjust different crystal loading. A7125 support low cost crystal within ± 50ppmaccuracy. Be noted that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.



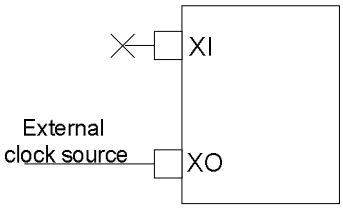
i.e., Crystal = 16MHz (Cload =20pF), C1=C2=33pF.

Figure12.1 Crystal network connection for using external crystal

12.2 Use External Clock

A7125 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. In such case, XI pin is left opened.

To use external clock from MCU instead of external crystal, user just sets XS= 0 (0Dh) to active AC couple capacitor. Be notice, the frequency accuracy of external clock shall be controlled within ± 50ppm and the clock swing (peak-to-peak) shall be larger than 1.5V.



(External clock is controlled within ± 50ppm and > 1.5Vpp.)

Figure 12.2 Connect to external clock source

13. System Clock

System clock (64MHz) is generated from crystal oscillator for internal digital circuitry. User can set "Data Rate Clock Register" (0Dh) to adapt different wanted crystal frequency (6/8/12/16MHz). Based on this, two important internal clocks F_{CGR} and F_{SYCK} are generated.

(1) F_{CGR}: Clock Generation Reference = 2MHz (Ref. clock of internal 64MHz PLL)
(2) F_{SYCK}: System Clock = 64 MHz (Main clock for internal digital circuit)

Relative Control Register

Data Rate Clock Register (Address: 0Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	--	--
	W	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0	0	0	1	1	1	1	1

PLL Register II (Address: 0Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		0	0	1	0	1	1	1	0

13.1 Derive System Clock

Because A7125 supports different external crystals, GRC [3:0] (0Dh) are used to get 2 MHz Clock Generation Reference (F_{CGR}) for internal usage.

$$F_{CGR} = \frac{F_{XREF}}{(GRC[3:0]+1)}.$$

Below is block diagram of system clock. F_{XTAL} is the crystal frequency. User can set registers to get F_{SYCK} = 64MHz. F_{XREF} is the reference clock of Clock Generator to generate F_{CGR} = 2MHz and F_{SPLL} = 64MHz. After delay circuitry, System clock is derived, F_{SYCK} = 64MHz. ADC clock (F_{ADC} = 4MHz or 8MHz) is from F_{SYCK} = 64MHz after frequency divider.

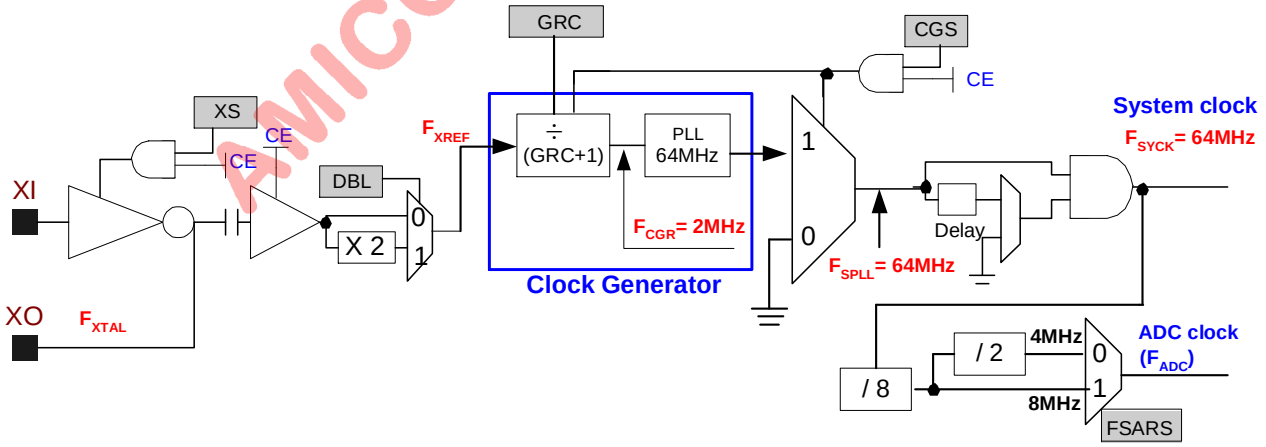


Figure 13.1 System Clock Block Diagram

Recommend to set DBL (0Fh) = [0], then, $F_{XREF} = F_{XTAL}$

Crystal Frequency (F_{XTAL})	Internal Crystal Reference (F_{XREF})	Clock Generation Reference (F_{CGR})	GRC [3:0]	CGS
16 MHz	16 MHz	Must be 2 MHz	[0111]	1

12 MHz	12 MHz	Must be 2 MHz	[0101]	1
8 MHz	8 MHz	Must be 2 MHz	[0011]	1
6 MHz	6 MHz	Must be 2 MHz	[0010]	1

Be notice if 6MHz external crystal (clock) is selected, A7125 only supports 1Mbps data rate.

13.2 Data Rate

A7125 supports programmable data rate by setting SDR [1:0] (0Dh). Data rate = (F_{IFCK} / (SDR [1:0] +1)). The data rate clock is from IF clock (F_{IFCK}) and F_{IFCK} = F_{SYCK} / 32 = 2 MHz

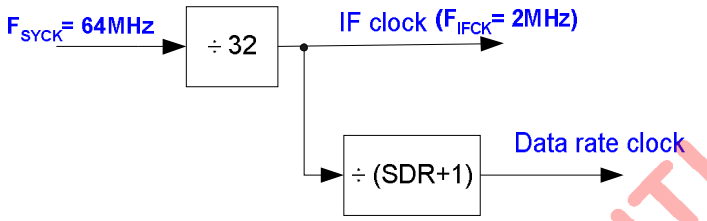


Figure 13.2 Data Rate Block Diagram

$$\text{A7125 Data Rate} = \frac{1}{32} \cdot \frac{F_{SYCK}}{SDR[1:0]+1}$$

F_{SYCK} (system clock)	F_{IFCK} (IF clock)	SDR [1:0] (0Dh)	Data Rate
64 MHz	2 MHz	[00]	2 Mbps
64 MHz	2 MHz	[01]	1 Mbps
64 MHz	2 MHz	[10]	Reserved
64 MHz	2 MHz	[11]	Reserved

14. Transceiver Frequency

A7125 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO (Local Oscillator) frequency for two-way radio transmission.

To target full range of 2.4GHz ISM band (2400 MHz to 2483.5 MHz), A7125 applies offset concept by LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, A7125 is easy to implement frequency hopping and multi-channels by **ONE** register setting, **PLL Register I (CHN [7:0], 0Eh).** In general, user can plan the wanted channels by a CHN Look-Up-Table to implement hopping table for two-way radio between master and slave.

Below is the LO frequency block diagram.

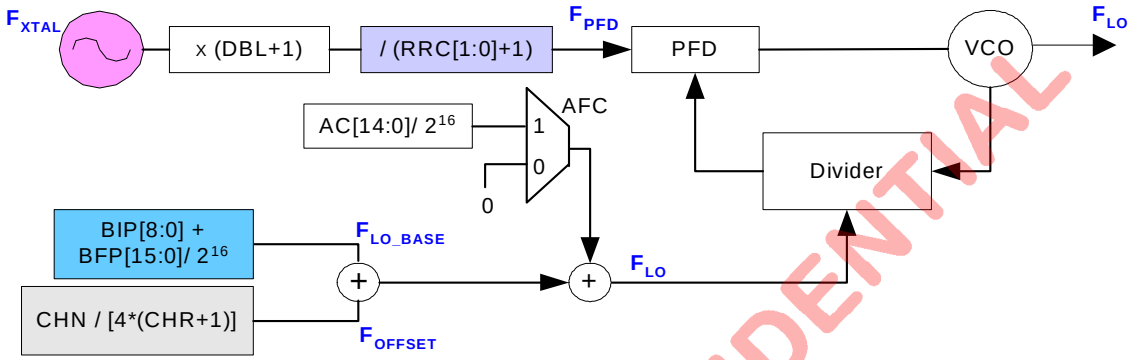


Figure 14.1 Block Diagram of Local Oscillator

Relative Control Register

PLL Register I (Address: 0Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

PLL Register II (Address: 0Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
Reset		0	0	1	0	1	1	1	0

PLL Register III (Address: 10h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		1	0	0	1	0	1	1	0

PLL Register IV (Address: 11h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--/FP15	AC14/FP14	AC13/FP13	AC12/P12	AC11/ FP11	AC10/FP10	AC9/FP9	AC8/FP8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0

PLL Register V (Address: 12h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	AC7/FP7	AC6/FP6	AC5/FP5	AC4/FP4	AC3/FP3	AC2/FP2	AC1/FP1	AC0/FP0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	1	0	0

RX Register (Address: 19h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	RXSM1	RXSM0	FC	RXDI	DMG	RAW	ULS
Reset		--	1	0	0	0	0	1	0

14.1 LO Frequency Setting

From Figure 14.1, F_{LO} is not only for TX radio frequency but also to be RX LO frequency. To set up $F_{LO,}$ it is easy to implement by below 8 steps.

1. Set the base frequency (**F_{LO_BASE}**) by PLL Register II, III, IV and V (0Fh, 10h, 11h and 12h).
   Recommend to set **F_{LO_BASE} ~ 2400.001MHz**.

2. Set the channel step (F_{CHSP}) by PLL Register II (0Fh).
   A7125 supports different channel steps by **2M / 1M / 500K / 250K. (500K is recommended.)**

3. Set CHN [7:0] to get offset frequency by PLL Register I (0Eh).
   F_{OFFSET} = CHN [7:0] * F_{CHSP}

4. LO frequency is equal to base frequency plus offset frequency.
   F_{LO} = F_{LO_BASE} + F_{OFFSET}

$$F_{LO\_BASE} = F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) = (DBL + 1) \cdot \frac{F_{XTAL}}{RRC[1:0] + 1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

Base on the above formula, for example, if F_{XTAL} = 16 MHz and step F_{CHSP} = 500 KHz, To get **F_{LO_BASE} and F_{LO}** ,see Table 14.1, 14.2, 14.3 and Figure 14.2 for details.

How to set F_{LO_BASE} ~ 2400.001 MHz

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	DBL	0	Disable double function
3	RRC	0	If so, F_{PFD}= 16MHz
4	BIP	0x96	To get F_{LO_BASE} =2400 MHz
5	BFP	0x0004	To get F_{LO_BASE} ~ 2400.001 MHz
6	**F_{LO_BASE}**	**~2400.001 MHz**	**LO Base frequency**

Table 14.1 How to set F_{LO_BASE}

How to set F_{LO} = F_{LO_BASE} + F_{OFFSET} ~ 2405.001 MHz

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~2400.001 MHz	After set up BIP and BFP
2	CHR	7	To get F_{CHSP}= 500 KHz
3	F_{CHSP}	500 KHz	Channel step = 500KHz
4	CHN	0x0A	Set channel number = 10
5	F_{OFFSET}	5 MHz	F_{OFFSET}= 500 KHz * (CHN) = 5MHz
6	**F_{LO}**	**~2405.001 MHz**	**Get F_{LO}= F_{LO_BASE} + F_{OFFSET}**

Table 14.2 How to set F_{LO}

Figure 14.2 show F_{LO} ~ 2405.001 MHz and its registers setting.

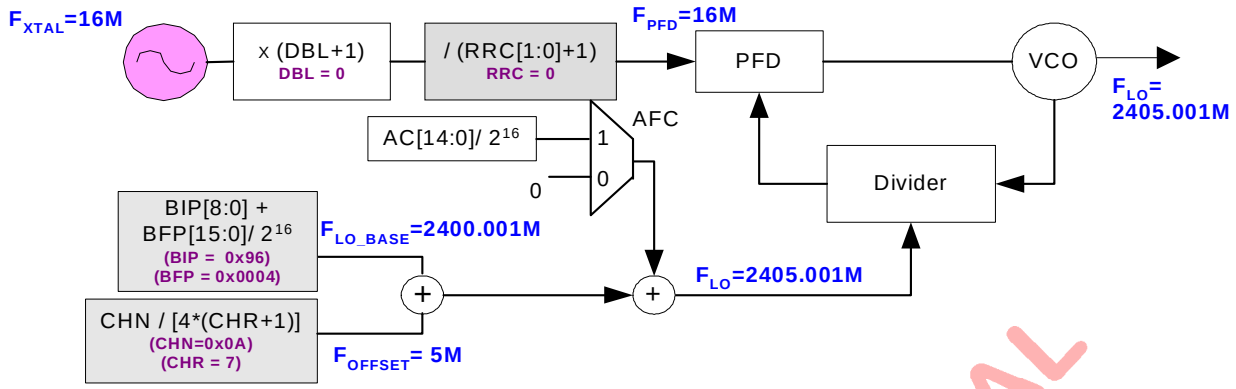


Figure 14.2 Block Diagram of F_{LO} ~ 2405.001 MHz

For different crystal frequency, 16MHz / 12MHz / 8 MHz / 6MHz, below are calculation details for
(1) How to set F_{LO_BASE} ~ 2400.001 MHz
(2) How to set F_{LO} ~ 2405.005 MHz

$$F_{PFD} = \frac{(DBL+1)\cdot f_{XTAL}}{RRC[1:0]+1}$$

Recommend DBL = 0

F_{XTAL} (MHz)	DBL	PRC	F_{PFD} (MHz)
16	0	0	16
12	0	0	12
8	0	0	8
6	0	0	6

Be notice if 6MHz external crystal (clock) is selected, A7125 only supports 1Mbps data rate.

$$F_{LO\_BASE} = F_{PFD}\cdot(BIP[8:0]+\frac{BFP[15:0]}{2^{16}})$$

F_{PFD} (MHz)	BIP (integer part)	BFP (floating part)	F_{LO_BASE} (MHz)
16	0x096	0x0004	~2400.001
12	0x0C8	0x0005	~2400.001
8	0x12C	0x0008	~2400.001
6	0x190	0x000A	~2400.001

$$F_{CHSP} = \frac{F_{PFD}}{4\cdot(CHR[3:0]+1)}$$

$$F_{LO} = F_{LO\_BASE} + (CHN[7:0]\cdot F_{CHSP})$$

F_{XTAL} = 16 MHz, How to set F_{CHSP}

F_{PFD} (MHz)	CHR [3:0]	F_{CHSP} (KHz)	CHN [7:0]	F_{OFFSET} (MHz)	F_{LO} (MHz)
16	1	2000	0x00 ~ 0x2A	0 ~ 84	2400 ~ 2484
16	3	1000	0x00 ~ 0x54	0 ~ 84	2400 ~ 2484
16	**7**	**500**	**0x00 ~ 0xA8**	**0 ~ 84**	**2400 ~ 2484**
16	15	250	0x00 ~ 0xFF	0 ~ 63.75	Depends on **F_{LO_BASE}**

F_{XTAL} = 12 MHz, How to set F_{CHSP}

F_{PFD} (MHz)	CHR [3:0]	F_{CHSP} (KHz)	CHN [7:0]	F_{OFFSET} (MHz)	F_{LO} (MHz)
12	2	1000	0x00 ~ 0x54	0 ~ 84	2400 ~ 2484
12	**5**	**500**	**0x00 ~ 0xA8**	**0 ~ 84**	**2400 ~ 2484**
12	11	250	0x00 ~ 0xFF	0 ~ 63.75	Depends on **F_{LO_BASE}**

F_{XTAL} = 8 MHz, How to set F_{CHSP}

F_{PFD} (MHz)	CHR [3:0]	F_{CHSP} (KHz)	CHN [7:0]	F_{OFFSET} (MHz)	F_{LO} (MHz)
8	0	2000	0x00 ~ 0x2A	0 ~ 84	2400 ~ 2484
8	1	1000	0x00 ~ 0x54	0 ~ 84	2400 ~ 2484
8	**3**	**500**	**0x00 ~ 0xA8**	**0 ~ 84**	**2400 ~ 2484**
8	7	250	0x00 ~ 0xFF	0 ~ 63.75	Depends on **F_{LO_BASE}**

F_{XTAL} = 6 MHz, How to set F_{CHSP}

F_{PFD} (MHz)	CHR [3:0]	F_{CHSP} (KHz)	CHN [7:0]	F_{OFFSET} (MHz)	F_{LO} (MHz)
6	**2**	**500**	**0x00 ~ 0xA8**	**0 ~ 84**	**2400 ~ 2484**
6	5	250	0x00 ~ 0xFF	0 ~ 63.75	Depends on **F_{LO_BASE}**

Be notice if 6MHz external crystal (clock) is selected and DBL=0, A7125 only supports 1Mbps data rate.

14.2 IF Side Band Select

In two ways radio, both master and slave have two roles, TX and RX. In general, slave usually has to reply an ACK-packet or status update. In such case, A7125 offers two methods to set up F_{LO} while TRX exchanging.

(1) Auto IF exchange
(2) Fast exchange

Relative Control Register

Mode Control Register (Address: 01h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DDPC	ARSSI	AIF	CD	WWSE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	DFCD	WWSE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

RX Register (Address: 19h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	RXSM1	RXSM0	FC	RXDI	DMG	RAW	ULS
Reset		--	1	0	0	0	0	1	0

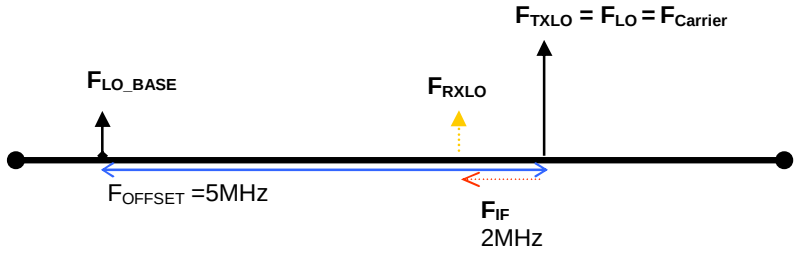
Register Setting	AIF Function	F_{RXLO} Formula
ULS=0	Disable (AIF=0)	$F_{RXLO} = F_{LO}$
ULS=1		$F_{RXLO} = F_{LO}$
ULS=0	Enable (AIF=1)	$F_{RXLO} = F_{LO} - 2MHz$
ULS=1		$F_{RXLO} = F_{LO} + 2MHz$

Table 14.3 F_{RXLO} Formula

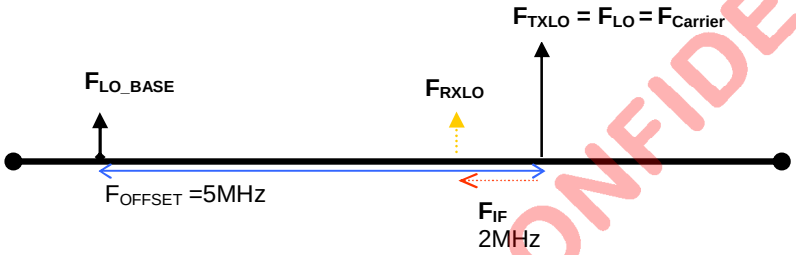
14.2.1 Auto IF Exchange

A7125 supports Auto IF offset function (AIF, 01h). If AIF is enabled, only one On-air frequency (Fcarrier) is occupied. In this case, user has no need to change F_{RXLO} while TRX exchanging because F_{RXLO} is auto shifted F_{IF}. See below Figures and Table 14.4 for details.

<Master>
AIF=1 and ULS=0, F_{RXLO} is auto shifted lower than F_{TXLO} for 2MHz (F_{IF}).



<Slave>
AIF=1 and ULS=0, F_{RXLO} is auto shifted lower than F_{TXLO} for 2MHz (F_{IF}).



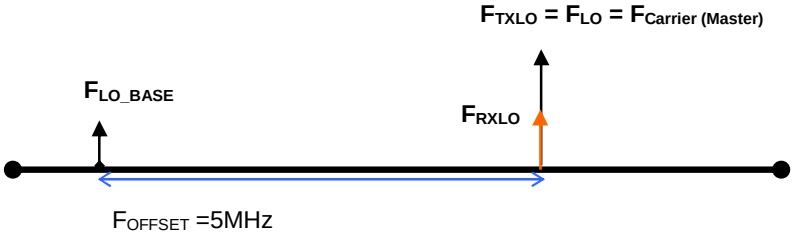
Item	Role	AIF	ULS	CHN[7:0]	F_{CHSP} (KHz)	F_{TXLO} (KHz)	F_{RXLO} (MHz)	NOTE
Master	TX	1	0	**10**	500	2405.001	-	
	RX	1	0	**10**	500	-	2403.001	Up side band F_{RXLO} is auto shifted
Slave	TX	1	0	**10**	500	2405.001	-	
	RX	1	0	**10**	500	-	2403.001	Up side band F_{RXLO} is auto shifted
Role Exchanging		Above setting is the same to Master and Slave.						
Switching Time		Refer to Figure 11.4, If A7125 delivers one packet and receives one packet, F_{LO} is changed from 2405.001 to 2403.001, longer switching time. Total Switching time = TX ready time + RX ready time =(30 us + 60 us) + (30 us + 60 us) = **180 us**						
On air frequency		Master **F_{TXLO}** = 2405.001 MHz Slave **F_{TXLO}** = 2405.001 MHz (ONE occupied frequency only.)						

Table 14.4 AIF function while TRX exchanging

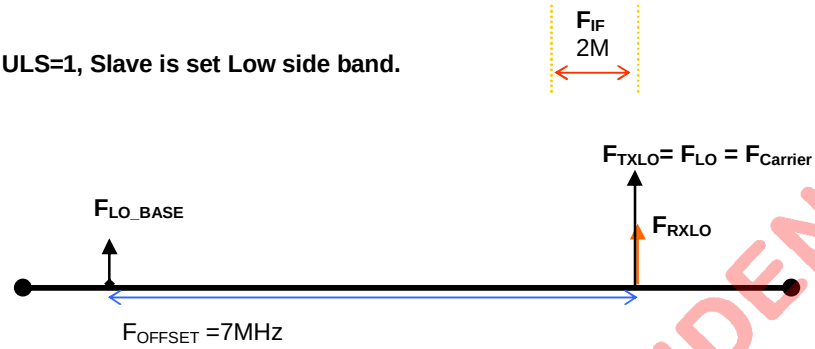
14.2.2 Fast Exchange

To reduce PLL settling time, user can disable AIF function. If AIF is disabled, two On-air frequency (**$F_{Carrier\ (master)}$**, **$F_{Carrier\ (slave)}$**) are occupied. In this case, user has to control ULS =0 (Master side) and ULS = 1 (Slave side) for fast exchange in two-way radio. See below Figures and Table 14.5 for details.

<Master>
AIF=0 and ULS=0, Master is set Up side band.



<Slave>
AIF=0 and ULS=1, Slave is set Low side band.



Item	Role	AIF	ULS	CHN[7:0]	F_{CHSP} (KHz)	F_{TXLO} (KHz)	F_{RXLO} (MHz)	NOTE
Master	TX	0	**0**	**10**	500	2405.001	-	
	RX	0	**0**	**10**	500	-	2405.001	Up side band
Slave	TX	0	**1**	**14**	500	2407.001	-	
	RX	0	**1**	**14**	500	-	2407.001	Low side band
Role Exchanging		ULS and CHN setting are different in Master and Slave site.						
Switching Time		Refer to Figure 11.4, If A7125 delivers one packet and receives one packet, Master's F_{LO} is fixed at 2405.001MHz, shorter settling time. Total Settling time = TX ready time + RX ready time = (10 us + 60 us) + (10 us + 60 us) = **140 us**						
On air frequency		Master **F_{TXLO}** = 2405.001 MHz Slave **F_{TXLO}** = 2407.001 MHz (TWO occupied on-air frequency.)						

Table 14.5 Fast exchange function while TRX exchanging

14.3 Band Edge Frequency Setting

For 2.4GHz ISM band, it is free licensed from 2400 MHz to 2483.5 MHz. Due to regulation criteria, in general, most of applications are avoided to use band edge of 2400MHz and 2483.5MHz. Therefore, in such cases, user can define specific band edges and set different **F_{LO_BASE}**. Combined with different channel step **F_{CHSP}**, user can gain different on air channel numbers. See table 14.1 for reference.

User Defined (Low Band Edge)	User Defined (High Band Edge)	Cover Range (MHz)	$F_{LO\ BASE}$ (MHz) (recommended)	F_{CHSP} (KHz)	On air Channel	NOTE

					Numbers	
2400 MHz	2483.5 MHz	83.5 MHz	~2400.001	2000	**42**	2.0 MHz / on air channel step
				1000		
				500		
2405 MHz	2477.0 MHz	72.0 MHz	~2405.001	2000	**37**	2.0 MHz / on air channel step
				1000		
				500		
2405 MHz	2467.0 MHz	62.0 MHz	~2405.001	2000	**32**	2.0 MHz / on air channel step
				1000		
				500		
2410 MHz	2463.0 MHz	52.0 MHz	~2410.001	2000	**27**	2.0 MHz / on air channel step
				1000		
				500		

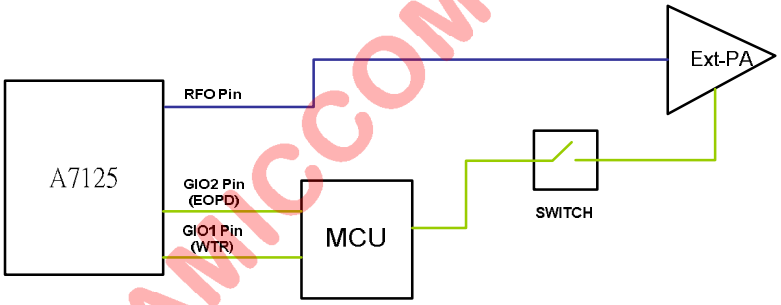
User Defined (Low Band Edge)	User Defined (High Band Edge)	Cover Range (MHz)	F_{LO_BASE} (MHz)	F_{CHSP} (KHz)	On air Channel Numbers	NOTE
2405 MHz	2468.0 MHz	63.0 MHz	~2405.001	250	**37**	1.75 MHz / on air channel step
2410 MHz	2462.5 MHz	52.5 MHz	~2405.001	250	**31**	1.75 MHz / on air channel step

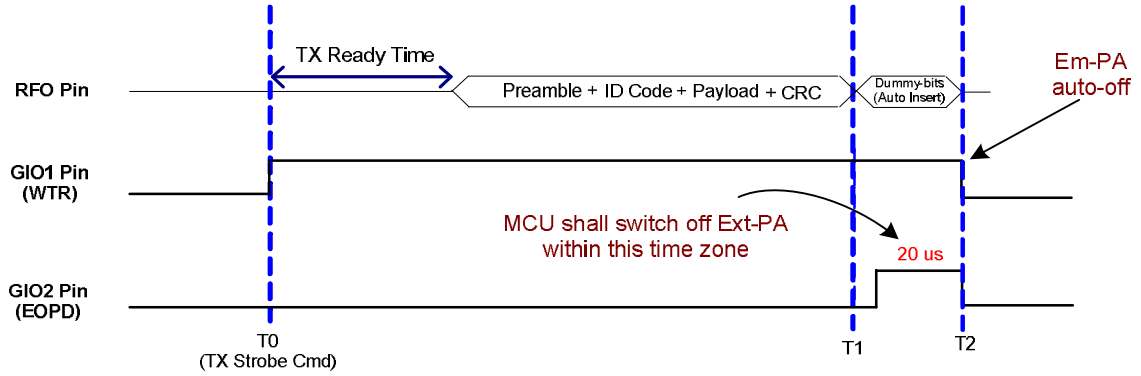
Be notice, if F_{CHSP} = 250 KHz, due to limitation of CHN [7:0], max cover range of F_{LO} is 63.75MHz.

Table 14.6 Band edge frequency setting vs. on air channel number

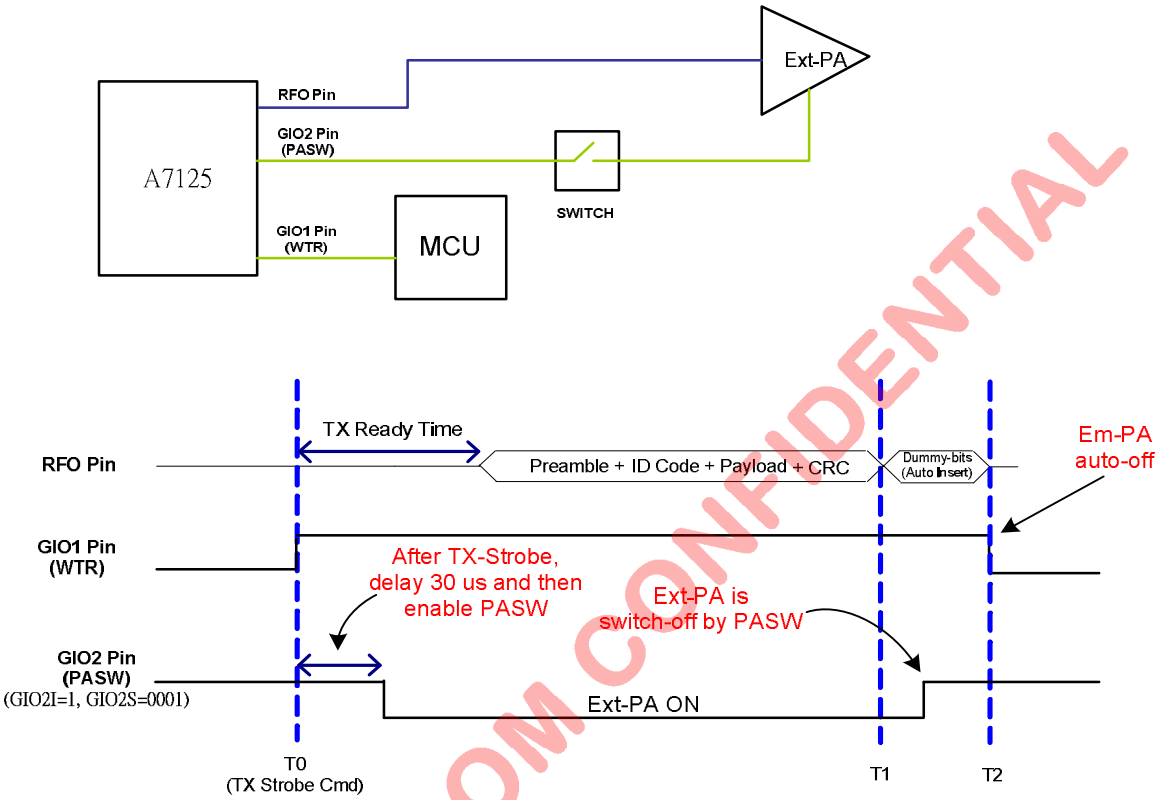
In long distance applications, user usually adds external PA (Ext-PA) to extend TX power level up 10dBm ~ 20 dBm. To gain the most available hopping channels under FCC / ETSI regulations, **user has to switch off Ext-PA before A7125's PA (Em-PA) to minimize spurious emission**. In the other words, band edge becomes critical so that A7125 supports two methods (EOPD and PASW) to let user switch Ext-PA easily.

(1) EOPD (End Of Packet Delay)
Set GIO2S = [1100] and EOPDS=1, then EOPD outputs 20 us pulse to GIO2 pin.





(2) PASW (Ext-PA Switch)
Set GIO2S = [0001] and EOPDS=1, then PASW outputs to GIO2 pin. However, GIO2S[3:0] shall be set different in TX mode [0001] and RX mode [0100] to avoid FSYNC conflict in RX mode. Therefore, before issue TX Strobe command, write GIO2S = [0001]. Before issue RX Strobe command, write GIO2S = [0100]. Then, PASW is only active in TX mode. In such case, user just needs to connect GIO2 pin to control external PA as shown below. Generally, this procedure could support sufficient band edge control. In more rigorous condition, it is recommended to switch GIO2S from [0100] to [0001] after delaying 30us counting from TX strobe command.



14.4 Frequency Compensation

AFC (Auto Frequency Compensation) function supports low accuracy crystal without sensitivity degradation. If AFC=1 (19h), bit error rate is optimized because AFC circuitry adjusts RX LO frequency (F_{RXLO}) to compensate crystal drift automatically.

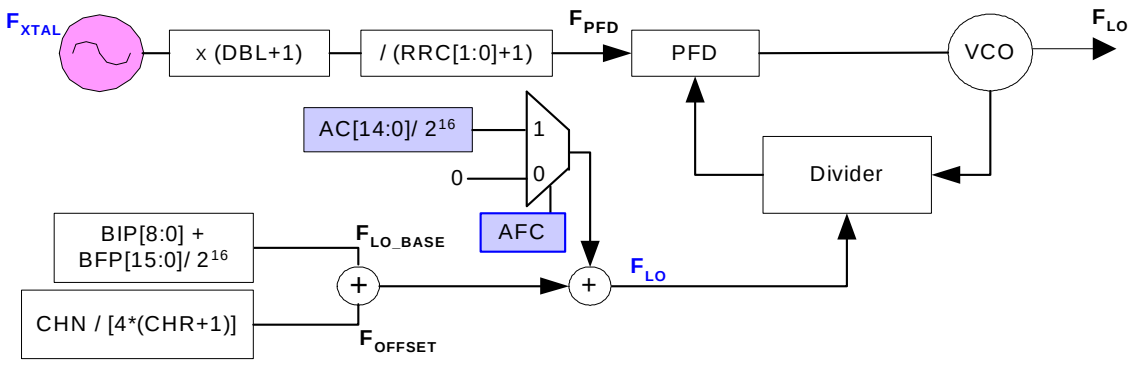


Figure 14.3 Block Diagram of enabling FC function

Relative Control Register

RX Register (Address: 19h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	RXSM1	RXSM0	AFC	RXDI	DMG	RAW	ULS
Reset		--	1	0	0	0	0	1	0

PLL Register IV (Address: 11h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--/FP15	AC14/FP14	AC13/FP13	AC12/P12	AC11/ FP11	AC10/FP10	AC9/FP9	AC8/FP8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0

PLL Register V (Address: 12h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	AC7/FP7	AC6/FP6	AC5/FP5	AC4/FP4	AC3/FP3	AC2/FP2	AC1/FP1	AC0/FP0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	1	0	0

15. Calibration

A7125 needs calibration process during initialization by below 5 items, they are, VCO Current, VCO Bank, VCO Deviation, IF Filter Bank and RSSI Calibration.

1. VCO Current Calibration is to find adequate VCO current.
2. VCO Bank Calibration is to select best VCO frequency bank for the calibrated frequency.
3. VCO Deviation Calibration is to calibrate 500 KHz deviation of VCO.
4. IF Filter Bank Calibration is to calibrate IF filter bandwidth and center frequency.
5. RSSI Calibration is to find the RSSI value corresponding to -70dBm RF input and RSSI curve.

Be notice that VCO Current, Bank and Deviation is calibrated in PLL mode by sequence. IF Filter Bank and RSSI can be calibrated either in standby or PLL mode. User can set A7125 in PLL mode and enable 5 control registers together, then, all calibration procedures are automatically executed and its results are stored in calibration flags.

Relative Control Register

Calibration Control Register (Address: 02h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	--	--	--	VCC	VBC	VDC	FBC	RSSC
Reset		--	--	--	0	0	0	0	0

15.1 Calibration Procedure

1. Initialize all control registers (refer to A7125 reference code).
2. Select auto value mode (set MFBS, MVCS, MVBS, MVDS= 0).
3. Set A7125 in PLL mode.
4. Enable IF Filter Bank and RSSI Calibration (set FBC, RSSC= 1) and
   Enable VCO Current, Bank and Deviation Calibration (VCC, VBC, VDC= 1).
5. After calibration done, FBC, RSSC, VCC, VBC and VDC are auto clear.
6. Check pass or fail by calibration flag
   (FBCF) and (VCCF, VBCF).

15.2 IF Filter Bank Calibration

IF Calibration Register I (Address: 23h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	FBCF	FB3	FB2	FB1	FB0
	W	--	--	--	MFBS	MFB3	MFB2	MFB1	MFB0
Reset		--	--	--	0	0	1	1	0

1. Initialize all control registers (refer A7125 reference code).
2. Set MFBS= 0 for auto calibration.
3. Set A7125 in PLL mode.
4. Set FBC= 1 (02h).
5. The maximum calibration time for this calibration is about 64us.
6. FBC is auto clear after calibration done.
7. User can read calibration flay (FBCF, 23h) to check pass or fail.
8. User also can read FB [3:0] (23h) to get the auto calibration value.

15.3 RSSI Calibration

1. Initialize all control registers (refer A7125 reference code).
   Set A7125 in PLL mode.
2. Set RSSC= 1 (02h).
3. RSSC is auto clear after calibration done.

4. No need to check calibration flag.

15.4 VCO Current Calibration

VCO Current Calibration Register (Address: 25h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	--	--	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		--	--	1	0	1	1	0	0

1. Initialize all control registers (refer A7125 reference code).
2. Set MVCS= 0 for auto calibration.
3. Set A7125 in PLL mode.
4. Set VCC= 1 (02h).
5. VCC is auto clear after calibration done.
6. User can read calibration flag (VCCF, 25h) to check pass or fail.
7. User can read VCB [3:0] (25h) to get the auto calibration value.

15.5 VCO Bank Calibration

VCO Bank Calibration Register I (Address: 26h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	DDC1	DDC0	DAGS	--	MVBS	MVB2	MVB1	MVB0
Reset		1	1	0	--	0	1	0	0

1. Initialize all control registers (refer A7125 reference code).
2. Set MVBS= 0 for auto calibration.
3. Set A7125 in PLL mode.
4. Set VBC= 1 (02h).
5. The maximum calibration time for VCO Bank Calibration is about 240 us (4 * PLL settling time).
6. VBC is auto clear after calibration done.
7. User can read calibration flag (VBCF, 26h) to check pass or fail.
8. User can read VB [2:0] (26h) to get the auto calibration value.

15.6 VCO Deviation Calibration

VCO Deviation Calibration Register II (Address: 29h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
Reset		0	0	1	0	1	0	0	0

1. Initialize all control registers (refer A7125 reference code).
2. Set MVDS= 0 for auto calibration.
3. Set A7125 in PLL mode.
4. Set VDC= 1 (02h).
5. VDC is auto clear after calibration done.
6. User can read ADEV [7:0] (29h) to get the auto calibration value.
7. No need to check calibration flag.

15.7 Channel Group Function

Channel group function is used for VCO calibration that supports to increase the accuracy of VCO Current, Bank and Deviation. By this function, user can easily set Channel Group Register I and II (13h, 14h) to get 2.4G ISM band into 3 groups as shown below. Then, choose middle frequency (2415MHz / 2445MHz / 2475MHz) of 3 groups to do the VCO

Current, Bank and Deviation Calibration.

Below is an example of channel group distribution.

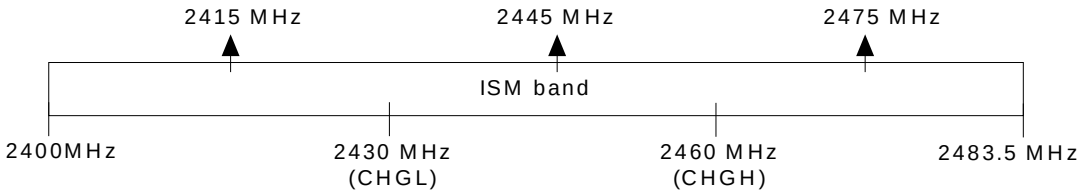


Figure 15.1 Channel Group setting of VCO calibration

Channel Group Register I (Address: 13h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	1	1	1	0	0

Channel Group Register II (Address: 14h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	1	1	1	0	0	0

See below table for setting CHGL and CHGH to get 2430MHz and 2460MHz respectively.

F_{PFD} (MHz)	BIP (integer part)	BFP (floating part)	F_{LO_BASE} (MHz)	F_{CHSP} (KHz)	CHGL[7:0]	CHGH[7:0]
16	0x096	0x0004	~2400.001	500	**0x3C**	**0x78**
12	0x0C8	0x0005	~2400.001	500	**0x3C**	**0x78**
8	0x12C	0x0008	~2400.001	500	**0x3C**	**0x78**
6	0x190	0x000A	~2400.001	500	**0x3C**	**0x78**

16. FIFO (First In First Out)

A7125 supports separated 64-bytes TX and RX FIFO by enabling FMS =1 (01h). For FIFO accessing, TX FIFO (write-only) and RX FIFO (read-only) share the same register address 05h. TX FIFO represents transmitted payload. On the other hand, once RX circuitry synchronizes ID Code, received payload is stored into RX FIFO.

In chapter 10 and 11, user can also find below FIFO information.
(1) Figure 10.15 and 10.16 for FIFO accessing via 3-wire SPI.
(2) Section 10.4.7 and 10.4.8 for FIFO pointer reset command.
(3) Figure 11.2 and Figure 11.3 for Normal/Quick FIFO mode.

16.1 Packet Format of FIFO mode

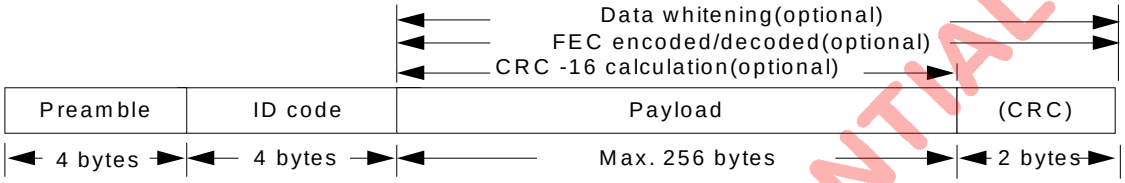


Figure 16.1 Packet Format of FIFO mode

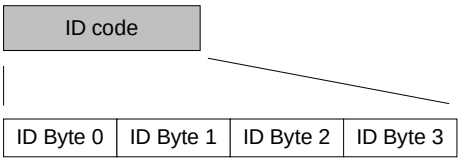


Figure 16.2 ID Code Format

Preamble:
The packet is led by preamble which is composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010…1010.
Preamble length is recommended to set 4 bytes by PML [1:0] (20h).

ID code:
ID code is recommended to set 4 bytes by IDL=1 (20h) and ID Code is sequenced by ID Byte 0, 1, 2 and 3. If RX circuitry check ID code is correct, payload will be written into RX FIFO. In special case, ID code could be set error tolerance (0~ 3bit error) by ETH [1:0] (21h) for ID synchronization check.

Payload:
Payload length is programmable by FEP [7:0] (03h). The physical FIFO depth is 64 bytes. A7125 also supports logical FIFO extension up to 256 bytes. See section 16.5 for details.

CRC (option):
In FIFO mode, if CRC is enabled (CRCS=1, 20h), 2-bytes of CRC value is transmitted automatically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag (00h).CRC Flag is updated by each received packet.

Relative Control Register

Mode Register (Address: 00h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	FECF	CRCF	CER	XER	PLLER	TRSR	TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
Reset		--	--	--	--	--	--	--	--

FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

Code Register I (Address: 20h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	WHTS	FECS	CRCS	IDL	PML1	PML0
Reset		--	--	0	0	0	1	1	1

Code Register II (Address: 21h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	DCL2	DCL1	DCL0	ETH1	ETH0	PMD1	PMD0
Reset		--	1	1	1	0	1	1	1

Code Register III (Address: 22h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		--	0	1	0	1	0	1	0

16.2 Bit Stream Process

A7125 supports 3 optional bit stream process for payload, they are,
(1) CCITT-16 CRC
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1 (20h). TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.
2. RX circuitry checks CRC value and shows the result to CRC Flag (00h). If CRCF=0, received payload is correct, else error occurred. (CRCF is read only, it is updated by each valid packet.)

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1 (20h). Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word and delivered out automatically.
   (ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)
3. RX circuitry decodes received code words automatically. FEC supports 1-bit error correction each code word. Once 1-bit error occurred, FEC flag=1 (00h). (FECF is read only, it is updated by each valid packet.)

Data Whitening:

1. Data whitening is enabled by WHTS= 1 (20h). Payload and CRC value (if CRCS=1) or their encoded code words (if FECS=1) are encrypted by bit XOR operation with PN7. The initial seed of PN7 is set by WS [6:0] (22h).
2. RX circuitry decrypts received payload and 2-bytes CRC (if CRCS=1) automatically. Be notice, user shall set the same WS [6:0] (22h) to TX and RX.

16.3 Transmission Time

Based on CRC and FEC options, the transmission time are different. See table 16.1 for details.

Data Rate = 2 Mbps

Data Rate (Mbps)	Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
2	32	32	512	Disable	Disable	576 bit * 0.5 us = 288 us
2	32	32	512	16 bits	Disable	592 bit * 0.5 us = 296 us
2	32	32	512	Disable	512 * 7 / 4	960 bit * 0.5 us = 480 us
2	32	32	512	16 * 7 / 4	512 * 7 / 4	988 bit * 0.5 us = 494 us

Table 16.1 Transmission time of 2 Mbps data rate

Data Rate = 1 Mbps

Data Rate (Mbps)	Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
1	32	32	512	Disable	Disable	576 bit * 1.0 us = 576 us
1	32	32	512	16 bits	Disable	592 bit * 1.0 us = 592 us
1	32	32	512	Disable	512 * 7 / 4	960 bit * 1.0 us = 960 us
1	32	32	512	16 * 7 / 4	512 * 7 / 4	988 bit * 1.0 us = 988 us

Table 16.2 Transmission time of 1 Mbps data rate

16.4 Usage of TX and RX FIFO

In application points of view, A7125 supports 3 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO
(3) FIFO Extension

For FIFO operation, A7125 supports Strobe command to reset TX and RX FIFO pointer as shown below. User can refer to section 10.5 for FIFO write pointer reset and FIFO read pointer reset.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	X	x	FIFO write pointer reset (for TX FIFO)
1	1	1	1	x	x	X	x	FIFO read pointer reset (for RX FIFO)

FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FIFO Register II (Address: 04h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FIFO DATA Register (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

16.4.1 Easy FIFO

In Easy FIFO, max FIFO length is 64 bytes. FIFO length is equal to **(FEP [7:0] +1)**. User just needs to control FEP [7:0] (03h) and disable PSA and FPM as shown below.

Register setting

TX	RX	Control Registers		
FIFO Length (byte)	**FIFO Length (byte)**	**FEP[7:0] (03h)**	**PSA[5:0] (04h)**	**FPM[1:0] (04h)**
1	1	0x00	0	0

8	8	0x07	0	0
16	16	0x0F	0	0
32	32	0x1F	0	0
64	64	0x3F	0	0

Table 16.3 Control registers of Easy FIFO

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A7125 reference code).
2. Set FEP [7:0] = 0x3F for 64-bytes FIFO.
3. Refer to Figure 11.2 and Figure 11.3
4. Send Strobe command – TX FIFO write pointer reset.
5. MCU writes 64-bytes data to TX FIFO.
6. Send TX Strobe Command.
7. Done.

Procedures of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) can be used to trigger MCU for RX FIFO reading.
2. Send Strobe command – RX FIFO read pointer reset.
3. MCU read 64-bytes from RX FIFO.
4. Done.

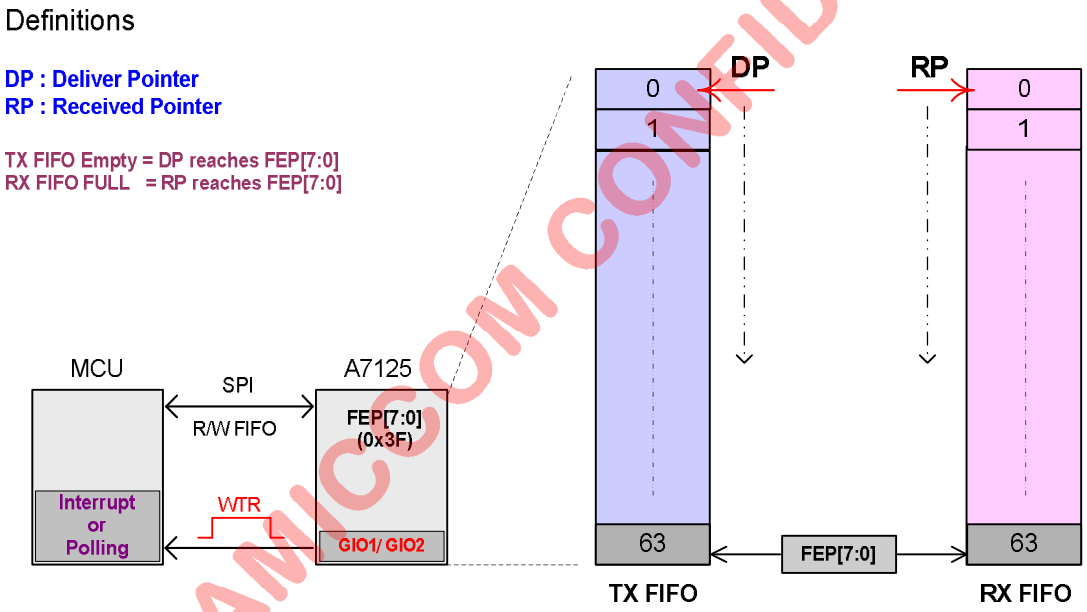


Figure 16.3 Easy FIFO

16.4.2 Segment FIFO

In Segment FIFO, TX FIFO length is equal to (FEP [7:0] – PSA [5:0]+1). FPM [1:0] should be zero. This function is very useful for button applications. In such case, each button is used to transmit fixed code (data) every time. During initialization, each fixed code is written into corresponding segment FIFO once and for all. Then, if button is triggered, MCU just assigns corresponding segment FIFO (PSA [5:0] and FEP [7:0]) and issues TX strobe command.

If TX FIFO is arranged into 8 segments, each TX segment and RX FIFO length are 8 bytes

TX				Control Registers		
Segment	**PSA**	**FEP**	**FIFO Length**	**PSA[5:0] (04h)**	**FEP[7:0] (03h)**	**FPM[1:0] (04h)**

			(byte)			
1	PSA1	FEP1	8	0x00	0x07	0
2	PSA2	FEP2	8	0x08	0x0F	0
3	PSA3	FEP3	8	0x10	0x17	0
4	PSA4	FEP4	8	0x18	0x1F	0
5	PSA5	FEP5	8	0x20	0x27	0
6	PSA6	FEP6	8	0x28	0x2F	0
7	PSA7	FEP7	8	0x30	0x37	0
8	PSA8	FEP8	8	0x38	0x3F	0

RX	Control Registers		
FIFO Length (byte)	PSA[5:0] (04h)	FEP[7:0] (03h)	FPM[1:0] (04h)
8	0	0x07	0

Table 16.4 Segment FIFO is arranged into 8 segments

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A7125 reference code).
2. Refer to Figure 11.2 and Figure 11.3 (in chapter 11).
3. Send Strobe command – TX FIFO write pointer reset.
4. MCU writes fixed code into corresponding segment FIFO once and for all.
5. To consign Segment 1, set PSA = 0x00 and FEP= 0x07
   To consign Segment 2, set PSA = 0x08 and FEP= 0x0F
   To consign Segment 3, set PSA = 0x10 and FEP= 0x17
   To consign Segment 4, set PSA = 0x18 and FEP= 0x1F
   To consign Segment 5, set PSA = 0x20 and FEP= 0x27
   To consign Segment 6, set PSA = 0x28 and FEP= 0x2F
   To consign Segment 7, set PSA = 0x30 and FEP= 0x37
   To consign Segment 8, set PSA = 0x38 and FEP= 0x3F
6. Send TX Strobe Command.
7. Done.

Procedures of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) is used to trigger MCU for RX FIFO reading.
2. Send Strobe command – RX FIFO read pointer reset.
3. MCU read 8-bytes from RX FIFO.
4. Done.

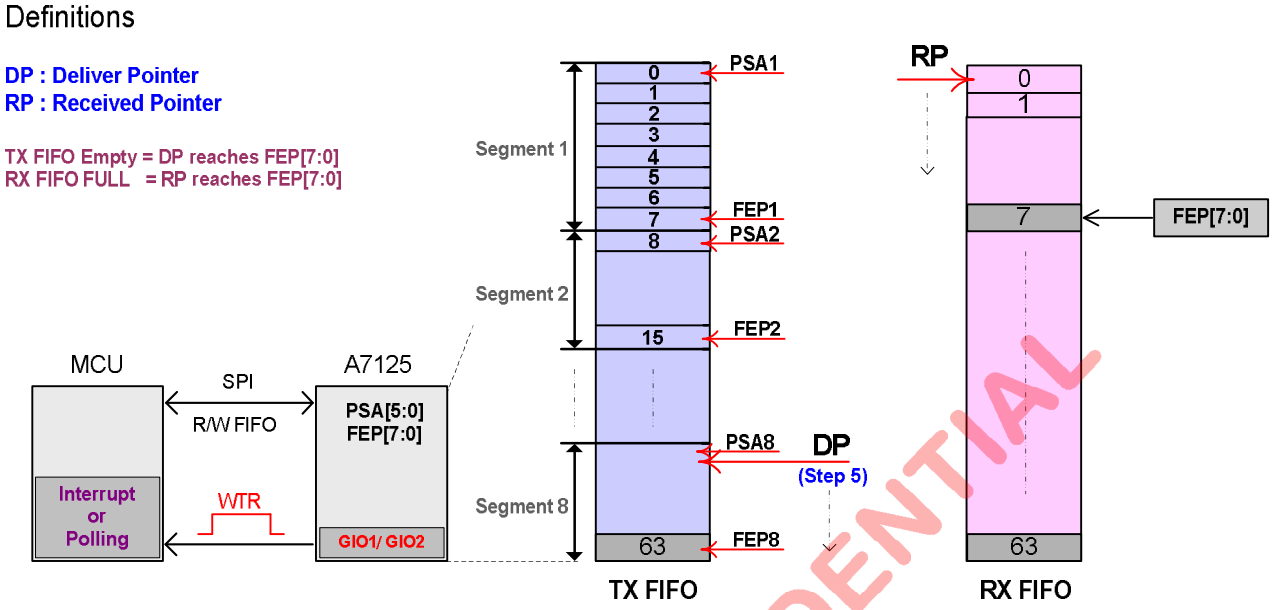


Figure 16.4 Segment FIFO Mode

16.4.3 FIFO Extension

In FIFO Extension, FIFO length is equal to **(FEP [7:0] +1)**. PSA [5:0] shall be zero, and FPM [1:0] is used to set FIFO Pointer Flag (FPF) to MCU. FIFO extension could be set up to 256 bytes by FEP [7:0] with different FPF trigger conditions.

Be notice, setting of SPI data rate is important to prevent error operation of FIFO extension. The min. SPI data rate shall be equal or greater than **(A125 data rate + 500Kbps)** and refer Table 16.4 and 16.5 for max. SPI Data Rate.

If A7125 data rate = 2Mbps and FIFO extension = 256 bytes.

TX			RX			Control Registers		
FIFO Length (byte)	**FPF Trigger Condition**	**Max. SPI Data Rate**	**FIFO Length (byte)**	**FPF Trigger Condition**	**Max. SPI Data Rate**	**FEP[7:0]**	**FPM[1:0]**	**PSA[5:0]**
256	Delta = 04	10 Mbps	256	Delta = 60	10 Mbps	0xFF	00	0
	Delta = 08	10 Mbps		Delta = 56	10 Mbps		01	0
	Delta = 12	10 Mbps		Delta = 52	10 Mbps		10	0
	Delta = 16	**8 Mbps**		**Delta = 48**	**8 Mbps**		**11**	0

Table 16.5 How to set FIFO extension when A7125 is at 2Mbps data rate

If A7125 data rate = 1Mbps and FIFO extension = 256 bytes.

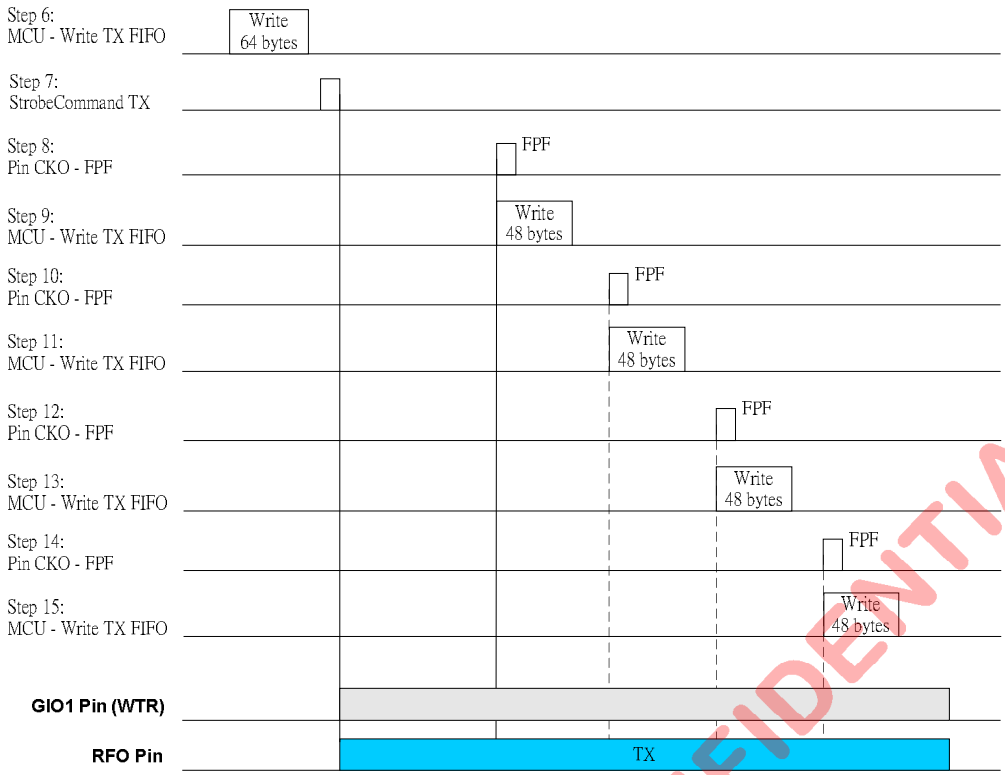
TX			RX			Control Registers		
FIFO Length (byte)	**FPF Trigger Condition**	**Max SPI Data Rate**	**FIFO Length (byte)**	**FPF Trigger Condition**	**Max SPI Data Rate**	**FEP[7:0]**	**FPM[1:0]**	**PSA[5:0]**
256	Delta = 04	10 Mbps	256	Delta = 60	10 Mbps	0xFF	00	0
	Delta = 08	**8 Mbps**		**Delta = 56**	**8 Mbps**		**01**	0
	Delta = 12	5 Mbps		Delta = 52	5 Mbps		10	0
	Delta = 16	4 Mbps		Delta = 48	4 Mbps		11	0

Table 16.6 How to set FIFO extension when A7125 is at 1Mbps data rate

Please refer to AMICCOM's reference code (FIFO extension) for details.

Procedures of TX FIFO Extension

1. Initialize all control registers (refer A7125 reference code).
2. Set FEP [7:0] = 0xFF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11 for FPF trigger condition.
4. Set CKO Register = 0x12
5. Send Strobe command – TX FIFO write pointer reset.
6. MCU writes 1st 64-bytes TX FIFO.
7. Send TX Strobe command.
8. MCU monitors FPF from A7125's CKO pin.
9. FPF triggers MCU to write 2nd 48-bytes TX FIFO.
10. Monitor FPF.
11. FPF triggers MCU to write 3rd 48-bytes TX FIFO.
12. Monitor FPF.
13. FPF triggers MCU to write 4th 48-bytes TX FIFO.
14. Monitor FPF.
15. FPF triggers MCU to write 5th 48-bytes TX FIFO.
16. Done.



Definitions

DP : Deliver Pointer
RP : Received Pointer
WTX : Write TX FIFO Pointer
Delta : WTX-DP+1 = 16 if FPM=11

TX FIFO Empty = DP reaches FEP[7:0]
RX FIFO FULL = RP reaches FEP[7:0]

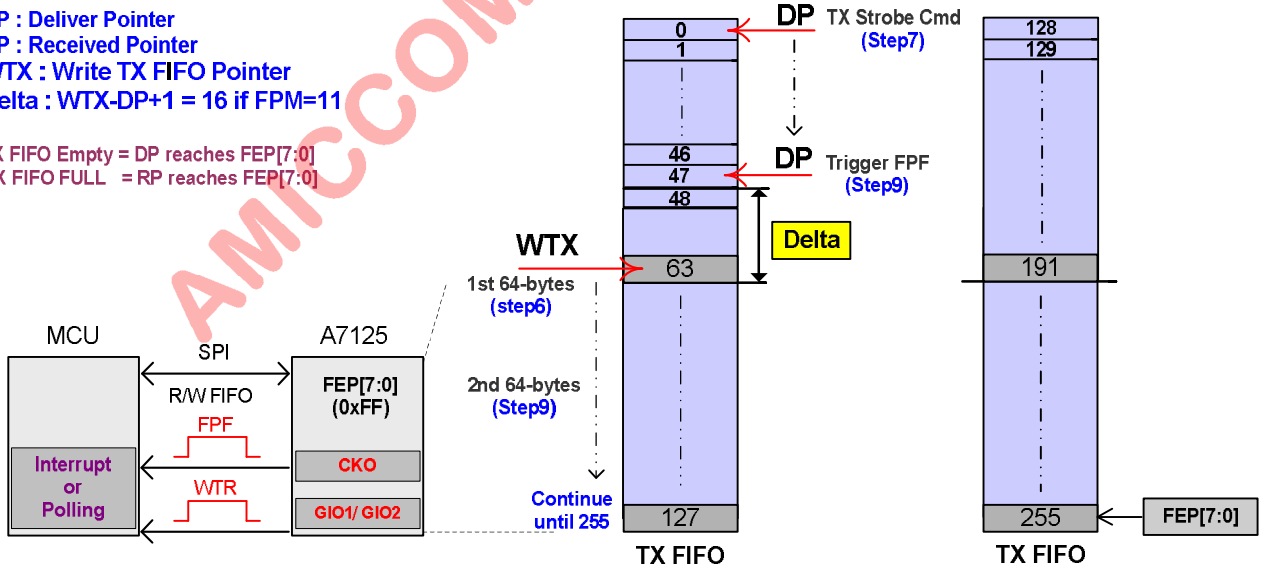
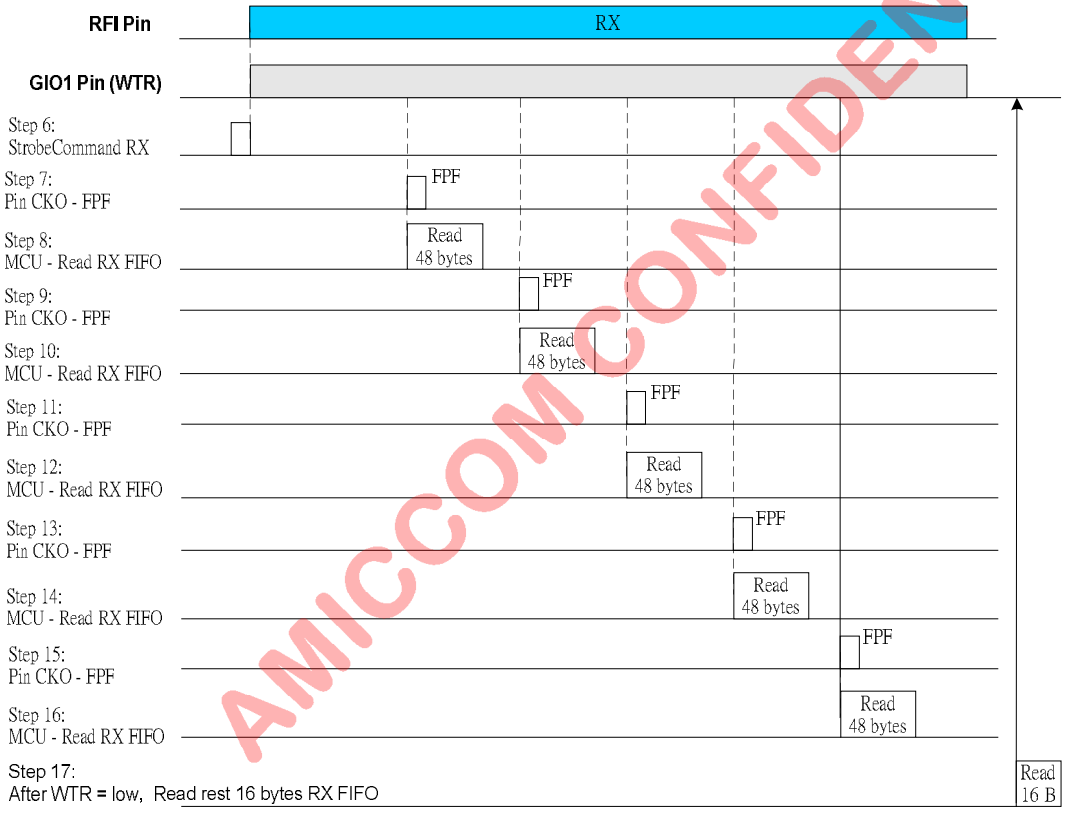


Figure 16.5 TX FIFO Extension

Procedures of RX FIFO Reading

1. Initialize all control registers (refer A7125 reference code).
2. Set FEP [7:0] = 0xFF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11b for FPF trigger condition.
4. Set CKO Register = 0x12
5. Send Strobe command – RX FIFO read pointer reset.
6. Send RX Strobe command.
7. MCU monitors FPF from A7125's CKO pin.
8. FPF triggers MCU to read 1st 48-bytes RX FIFO.
9. Monitor FPF.
10. FPF triggers MCU to read 2nd 48-bytes RX FIFO.
11. Monitor FPF.
12. FPF triggers MCU to read 3rd 48-bytes RX FIFO.
13. Monitor FPF.
14. FPF triggers MCU to read 4th 48-bytes RX FIFO.
15. Monitor FPF.
16. FPF triggers MCU to read 5th 48-bytes RX FIFO.
17. Monitor WTR falling edge or WTR = low, read the rest 16-bytes RX FIFO
18. Done.



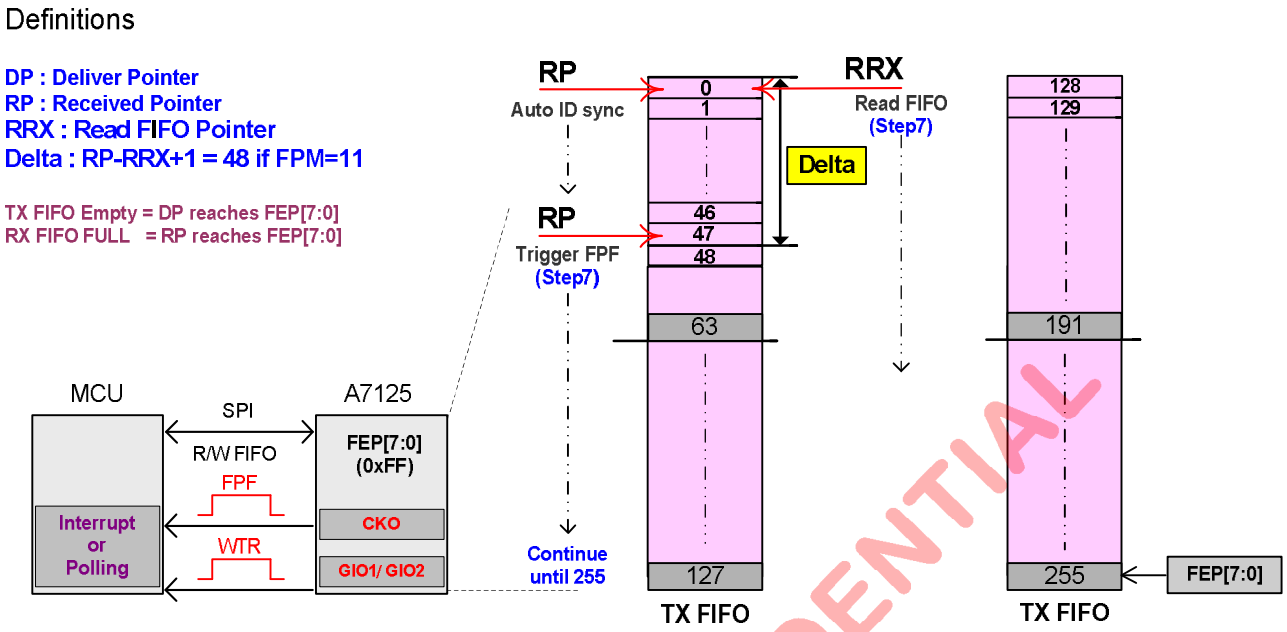


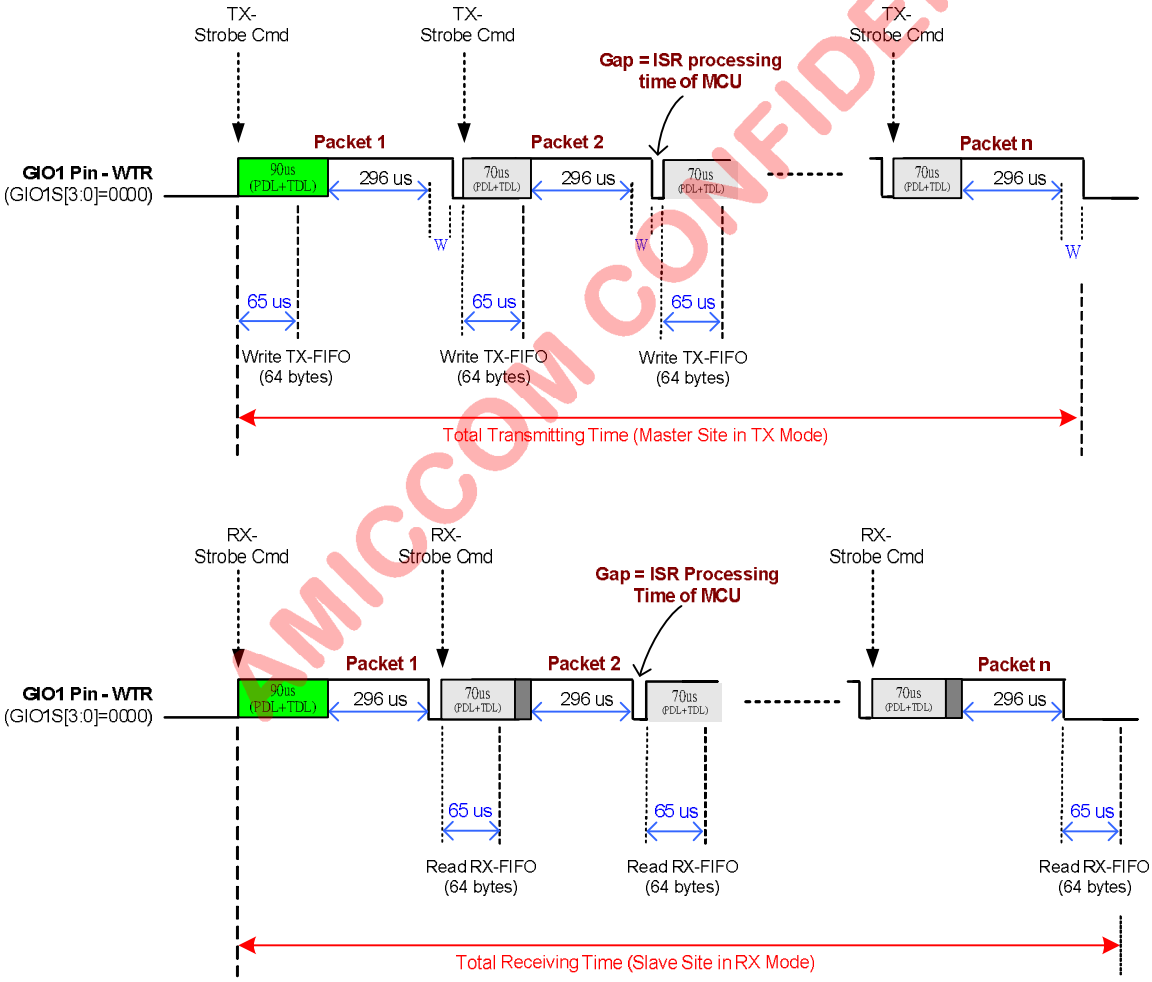
Figure 16.6 RX FIFO Extension Mode

16.5 Optimize Throughput

To get the best throughput during two-way radio transmission, user can use FIFO Extension mode, section 16.4.3, to reduce overhead of preamble, ID, settling time delay of PDL and TDL. The disadvantage of FIFO Extension is more MCU loading and overhead of retransmission time if packet lost. In another way, by Easy FIFO mode, If MCU's SPI bus ≧ 2.5Mbps, user can use WTR signal to Read / Write FIFO during PDL+TDL settling time to gain more throughput. See below illustrations with pre-conditions.

Pre-Conditions:

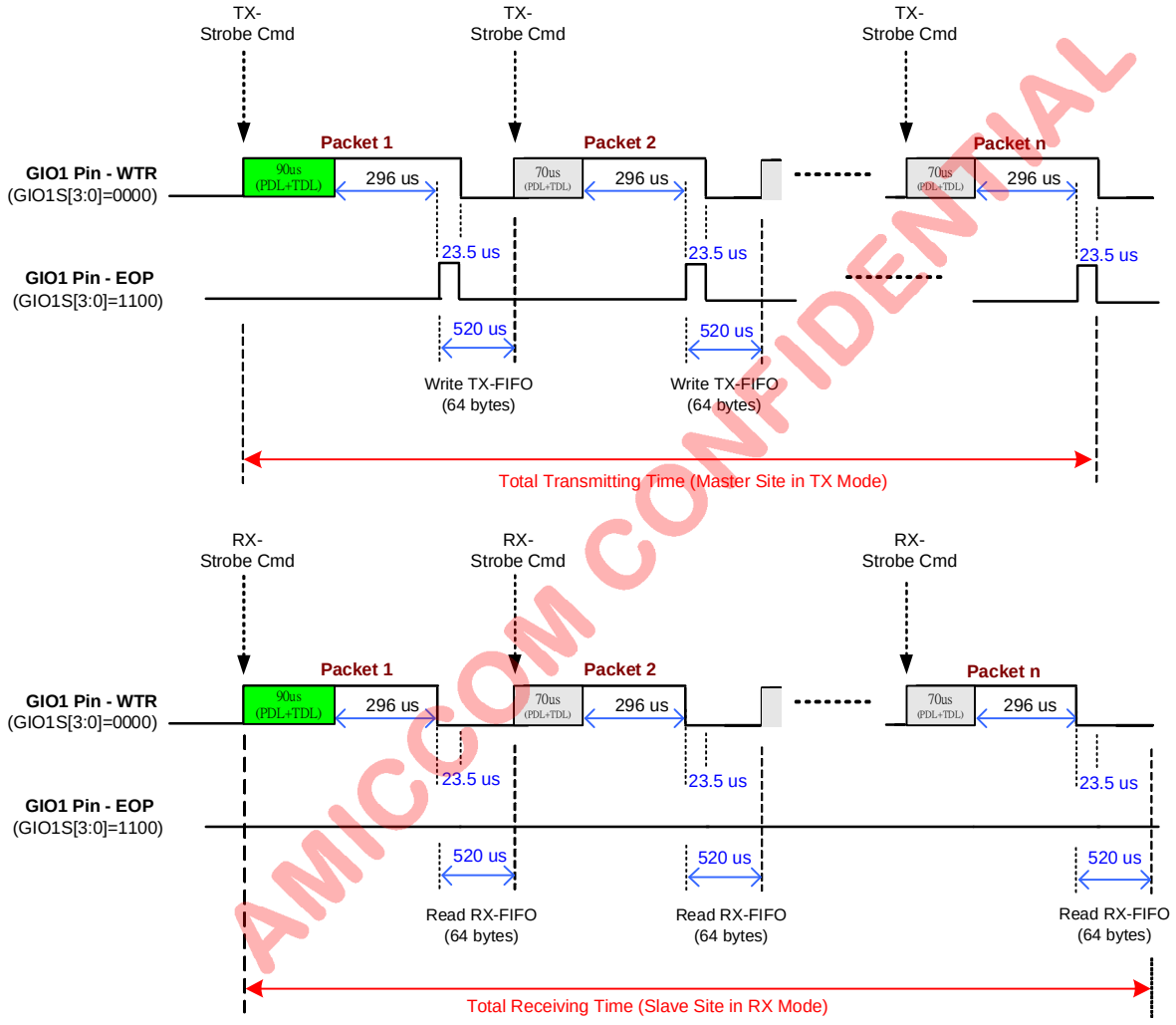
1. A7125's data rate = 2Mbps.
2. Min. requirement of CPU SPI bus = 2.5 Mbps > A7125's data rate.
3. If MCU SPI bus = 8Mbps and ignore guard time of SPI.
   i. Write TX-FIFO = (addr+data) * 0.125 us = (1+64) * 8 * 0.125 = 65 us.
   ii. Read RX-FIFO = (addr+data) * 0.125 us = (1+64) * 8 * 0.125 = 65 us.
4. CRC is enabled.
5. Use Easy FIFO mode (64 bytes).
6. One packet = Preamble + ID + Payload + CRC = (4+4+64+2) * 8 = 592 bit.
7. One packet transmission time = 592 bits * 0.5 = 296 us.
8. W=1 us if EOPDS = 0; W=23.5 us if EOPDS = 1
9. One frequency channel for n-packets.
10. MCU monitors WTR.



However, If MCU's SPI bus < 2.5Mbps and EOPD =1 for band edge optimization in adding Ext-PA application, user can use EOP signal to Write FIFO to gain a few throughput. See below illustrations with pre-conditions.

Pre-Conditions:

1. A7125's data rate = 2Mbps.
2. If MPU SPI bus = 1Mbps and ignore guard time of SPI, CRCF Check and MCU's ISR.
   i. Write TX-FIFO = (addr+data) * 1 us = (1+64) * 8 * 1 = 520 us.
   ii. Read RX-FIFO = (addr+data) * 1 us = (1+64) * 8 * 1 = 520 us.
3. CRC is enabled.
4. Use Easy FIFO mode (64 bytes).
5. One packet = Preamble + ID + Payload + CRC = (4+4+64+2) * 8 = 592 bit.
6. One packet transmission time = 592 bits * 0.5 = 296 us.
7. EOPDS = 1.
8. One frequency channel for n-packets.
9. MCU monitors EOP.



17. ADC (Analog to Digital Converter)

A7125 has built-in 8-bits ADC that supports multi-functions to do temperature measurement, RSSI, carrier detection. User can set FSARS (1Fh) to select 4MHz or 8MHz ADC clock (F_{ADC}). The converting time is 20 times of ADC clock periods.

Bit		Description	
XADS	RSS	Standby mode	RX mode
0	0	Temperature	None
0	1	None	RSSI / Carrier detect
1	X	Reserved	None

Table 17.1 ADC Function List.

Relative Control Register

Mode Control Register (Address: 01h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DDPC	ARSSI	AIF	CD	WWSE	FMT	FMS	ADCM
	W	DDPC	ARSSI	AIF	DFCD	WWSE	FMT	FMS	ADCM
Reset		0	0	0	0	0	0	0	0

RX Gain Register IV (Address: 1Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	AVSEL1	AVSEL0	MVSEL1	MVSEL0	MHC	LHC1	LHC0	AGCE
Reset		0	1	0	0	1	1	1	0

RSSI Threshold Register (Address: 1Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	W	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
Reset		1	0	0	1	0	0	0	1

ADC Control Register (Address: 1Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RSM1	RSM0	RADC1	RADC0	FSARS	XADS	RSS	CDM
Reset		0	1	0	0	1	0	1	1

17.1 Temperature Measurement

A7125 has built-in thermal sensor. Combined with 8-bits ADC, it can be used to monitor the relative environment temperature. Below is the measurement procedure:

1. Set RSS= 0 (1Fh), FSARS= 0 (1Fh).
2. Enter Standby mode.
3. Set ADCM= 1 (01h). A7125 will enable relative temperature measurement automatically.
4. After measurement done, ADCM is auto clear.
5. User can read digital temperature value from ADC [7:0] (1Eh).

17.2 RSSI Measurement

A7125 has built-in 8-bits digital RSSI to detect RF signal strength. After measurement done, RSSI is stored in ADC [7:0] (1Eh). The more signal power, the larger RSSI value.
Below is the measurement procedure:

Auto RSSI measurement for TX Power:

1. Set wanted F_{RXLO} (Refer to chapter 14).
2. Set ADCM=1 (01h), RSS= 1 (1Fh), FSARS= 1 (1Fh, 8MHz ADC clock).
3. Enable MVSEL = [00] (1Dh) and RADC = [10] (1Fh) to do 8-times average RSSI measurement.
4. Set ARSSI= 1 (01h).
5. Send RX Strobe command.
6. Once entering into RX mode, A7125 executes 8-times average measurement repeatedly.
7. Once A7125 leaves RX mode, user can read digital RSSI value from ADC [7:0] (1Eh) for TX power.

Be notice, in step 7, if A7125 is set in direct mode, once the received packet is completed, MCU shall ask A7125 to leave RX mode within 40 us to prevent RSSI inaccuracy.

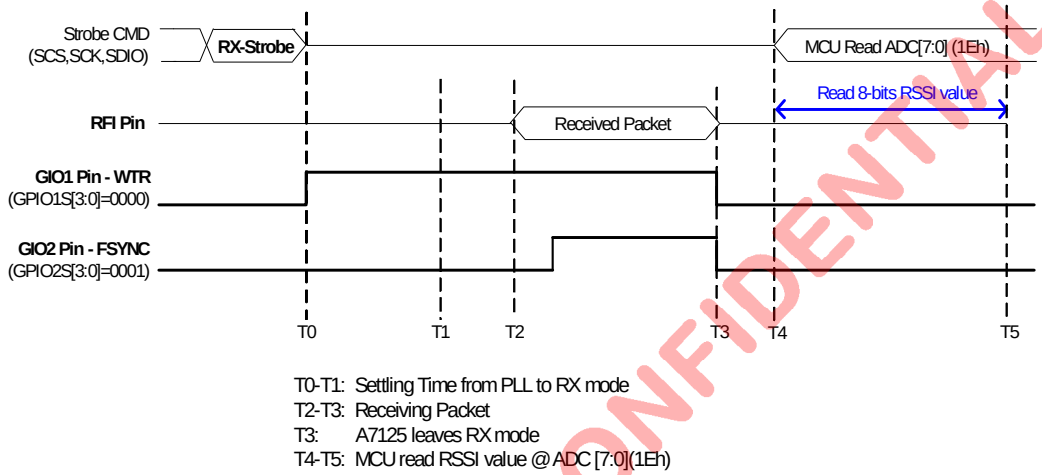


Figure 17.1 Timing chart of Auto RSSI measurement for TX Power:

Auto RSSI measurement for Background Power:

1. Set wanted F_{RXLO} (Refer to chapter 14).
2. Set ADCM=1 (01h), RSS= 1 (1Fh), FSARS= 1 (1Fh, 8MHz ADC clock).
3. Enable MVSEL = [00] (1Dh) and RADC = [10] (1Fh) to do 8-times average RSSI measurement.
4. Set ARSSI= 1 (01h).
5. Send RX Strobe command.
6. MCU delays min. 140us.
7. Read digital RSSI value from ADC [7:0] (1Eh) to get background power.
8. Send Strobe command to ask A7125 to leave RX mode.

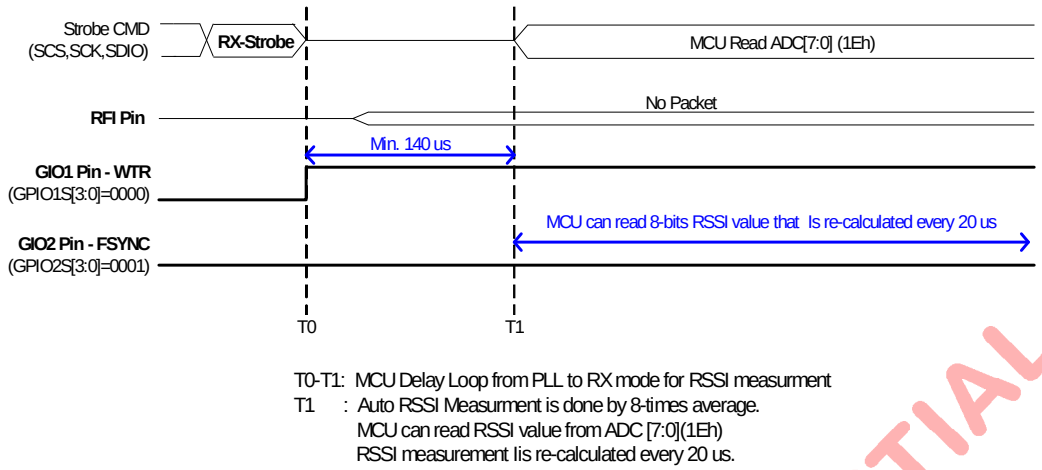


Figure 17.2 Timing chart of Auto RSSI measurement for Background Power:

17.3 Carrier Detect

Base on RSSI measurement, user can extend its application to do carrier detect (CD). If CD is triggered, its output can be set to GIO1 or GIO2 pin to inform MCU the occupied channel.
Below is the detection procedure:

1. Set RTH (1Eh) for RSSI higher threshold by user's definition (see below Table 17.2).
2. Set RTL (RTL = RTH – RSM) by RSM = [11] (1Fh) (recommended).
3. Set GIO1S = [0010] (0Bh) for GIO1 pin to output CD signal.
4. Follow procedure of auto RSSI measurement.
5. MCU checks GIO1 pin for carrier detect (CD) signal.

In step 1, MCU can read RH and RL to calculate and store the RTH value corresponding to desired CD trigger level below.

RSSI Range	RH [7:0]	RL [7:0]	CD Trigger Level (dBm)	RTH (Recommended)	Note
Max (-50 dBm) Min (-100 dBm)	Address 1Bh	Address 1Ch	-58	(3RH - RL) / 2	Formula of digital RSSI values is just approximate for reference.
			-64	RH	
			-70	(RH + RL) / 2	
			-76	RL	
			-82	(3RL - RH) / 2	

Table 17.2 RTH Recommended Setting

In step 5, CD=1 if measured RSSI ≧ RTH. That means this channel is occupied.
CD=0 if measured RSSI ≦ RTL. That means this channel is clear.

18. Battery Detect

A7125 has built-in battery detector to check supply voltage (REGI pin). The detect range is 2.0V ~ 2.7V in 8 levels.

Relative Control Register

Battery Detect Register (Address: 2Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	BDF	--	--	--	--
	W	RGS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

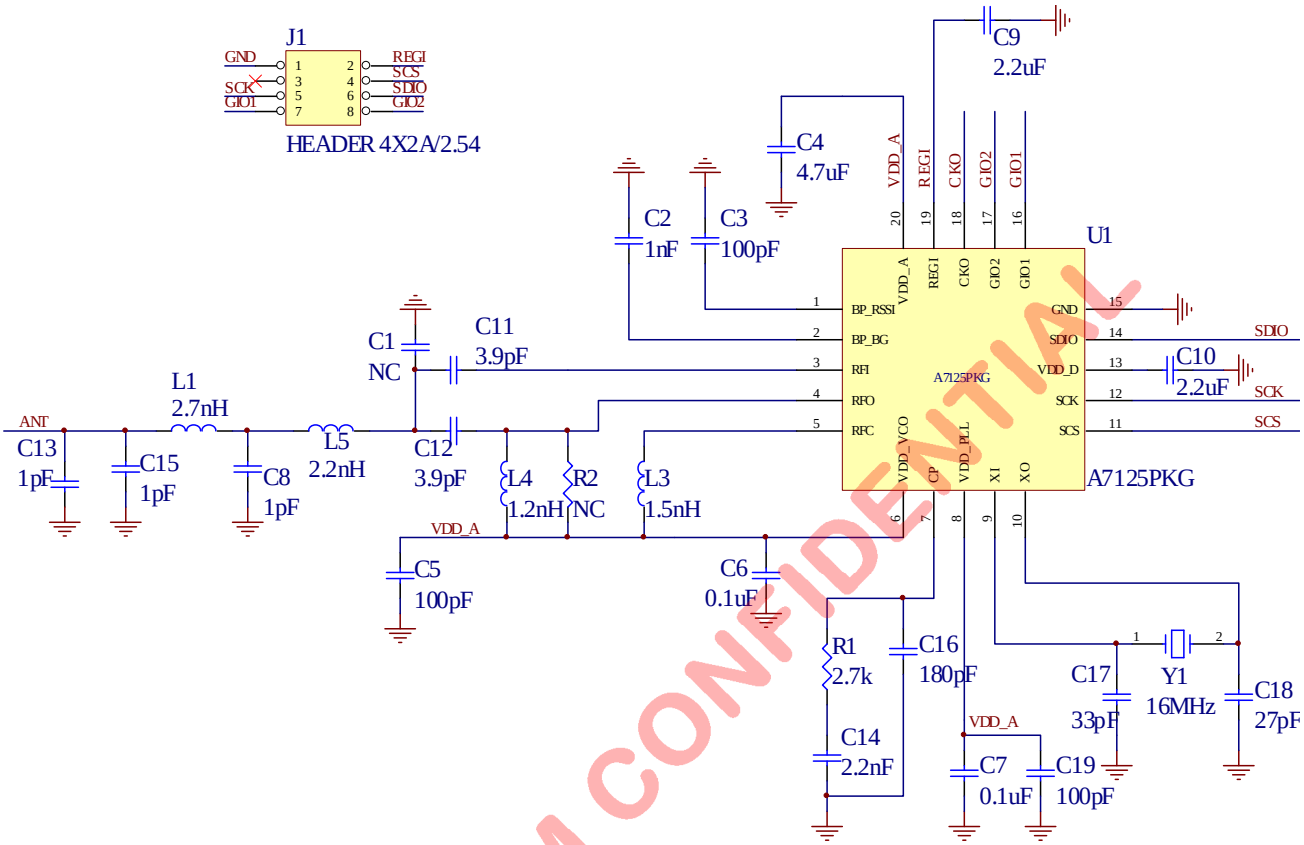
BVT [2:0]: Battery voltage detect threshold.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.
[100]: 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

Below is the procedure of battery detect for low voltage detection (ex., below 2.1V):

1. Set A7125 in standby or PLL mode.
2. Set BVT (2Ch) = [001] and enable BD_E (2Ch) = 1.
3. After 5 us, BD_E is auto clear.
4. MCU check BDF (2Ch).
   If REGI pin > 2.1V,
   BDF = 1. Else, BDF = 0.

19. Application Circuit Example

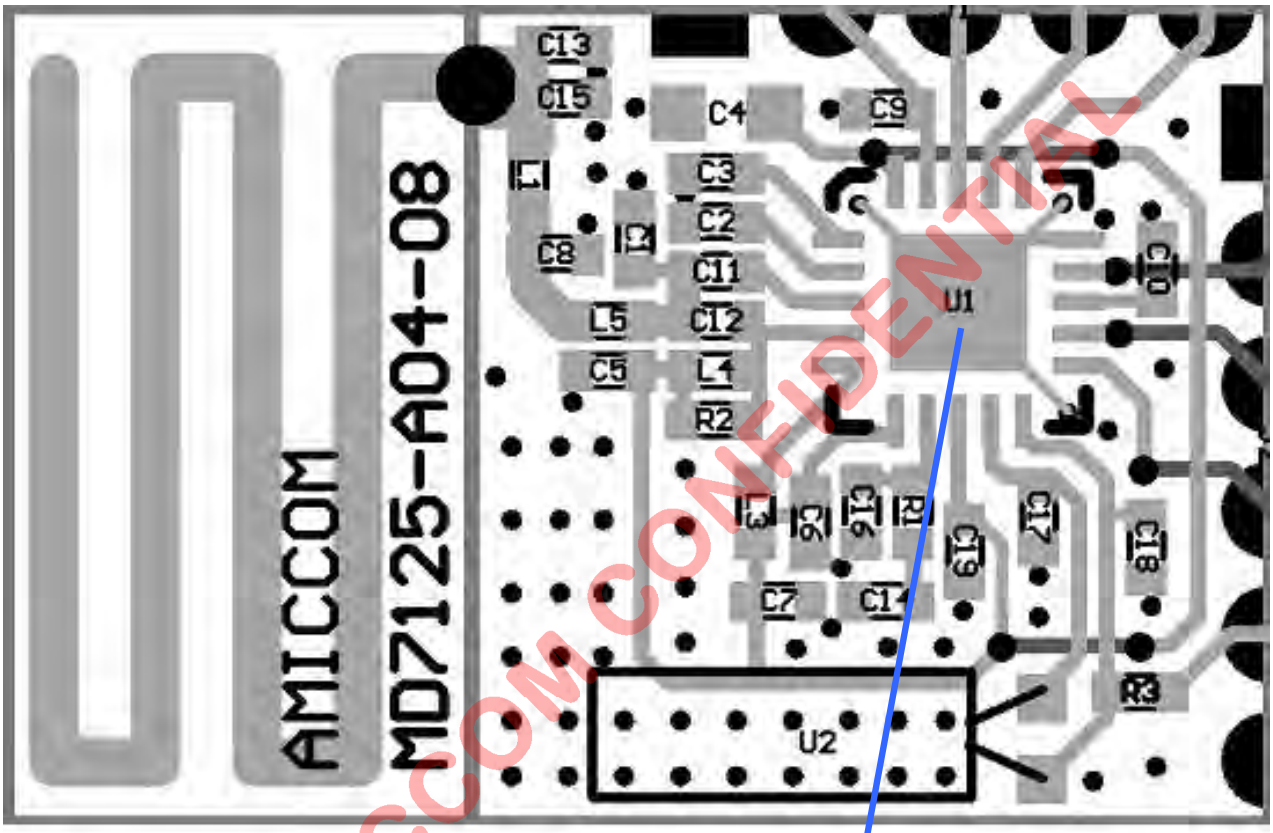
Below are AMICCOM's ref. design module, MD7125-A04, circuit example and its PCB layout.



1. A7125 schematic for RF layouts with single ended 50Ω RF output.
2. C17 and C18 must be matched to the crystal's load capacitance, Cload. Please see application note for detail.

MD7125-A04 which size is 13mm x 20mm with PCB antenna is suitable for small form factor application. MD7125-A04 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

To get a good RF performance, the well designed PCB is necessary. A poor layout can lead to loss of RF performance especially on matching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7125's **GND** pad and IC back side plate (**GND**).



Be Notice,
1. IC Back side plate shall be well-solder to ground (U1 area) for good RF performance.
2. Need at least 9 GND via holes at U1 area

20. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
FC	Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXLO	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

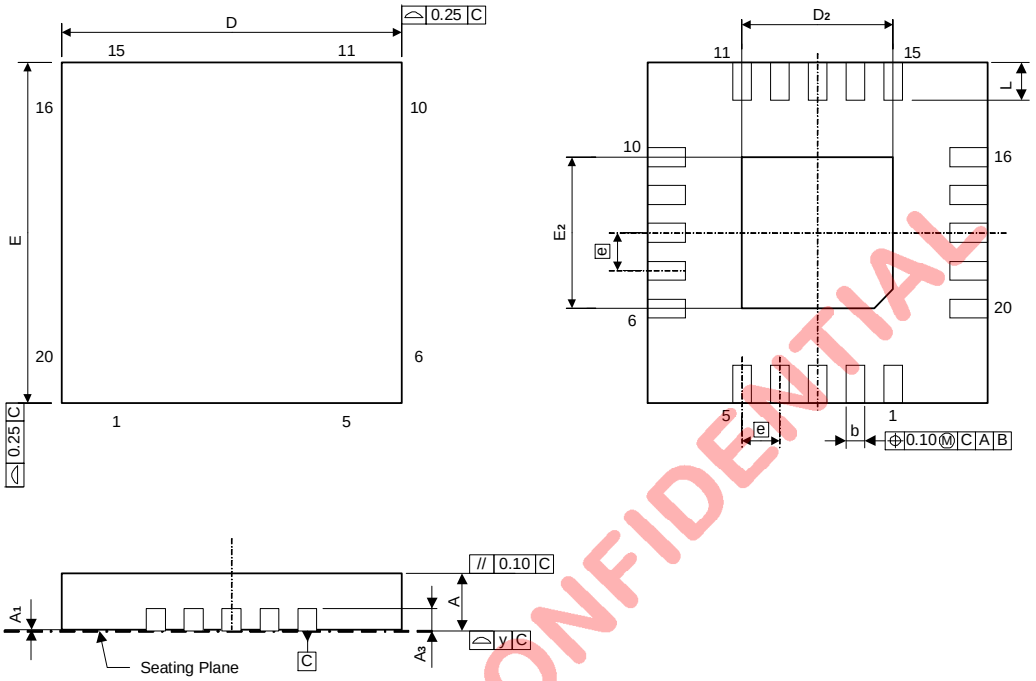
21. Ordering Information

Part No.	Package	Units Per Reel / Tray
A71X25AQFI/Q	QFN20L, Pb Free, Tape & Reel, -40℃～85℃	3K
A71X25AQFI	QFN20L, Pb Free, Tray, -40℃～85℃	490EA
A71X25AH	Die form, -40℃～85℃	250EA

22. Package Information

QFN 20L (4 X 4 X 0.8mm) Outline Dimensions unit: inches/mm

TOP VIEW **BOTTOM VIEW**

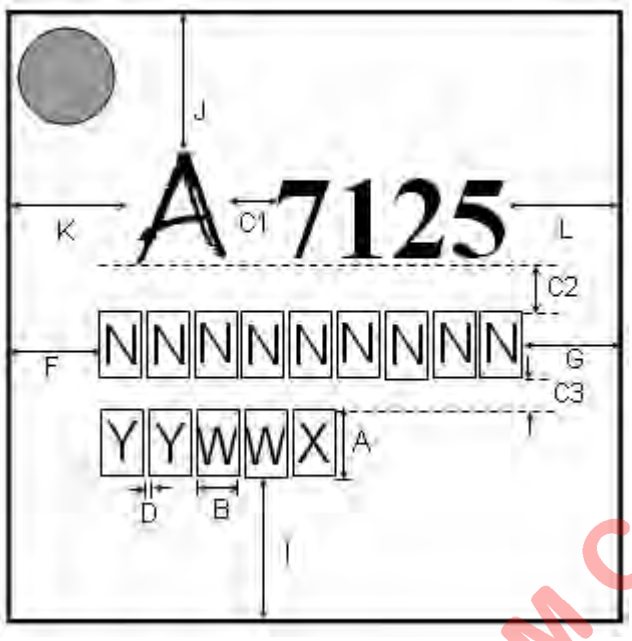


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3	0.008 REF			0.203 REF		
B	0.007	0.010	0.012	0.18	0.25	0.30
D	0.154	0.158	0.161	3.90	4.00	4.10
D_2	0.075	0.079	0.083	1.90	2.00	2.10
E	0.154	0.158	0.161	3.90	4.00	4.10
E_2	0.075	0.079	0.083	1.90	2.00	2.10
e	0.020 BSC			0.50 BSC		
L	0.012	0.016	0.020	0.30	0.40	0.50
Y	0.003			0.08		

23. Top Marking Information

A71X25AQFI

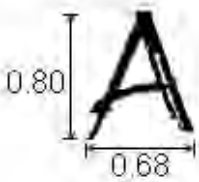
- Part No. : **A71X25AQFI**
- Pin Count : **20**
- Package Type : **QFN**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



❖ CHARACTER SIZE : (Unit in mm)

A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03
A1 : 0.75
B2 : 0.7

F=G
I=J
K=L

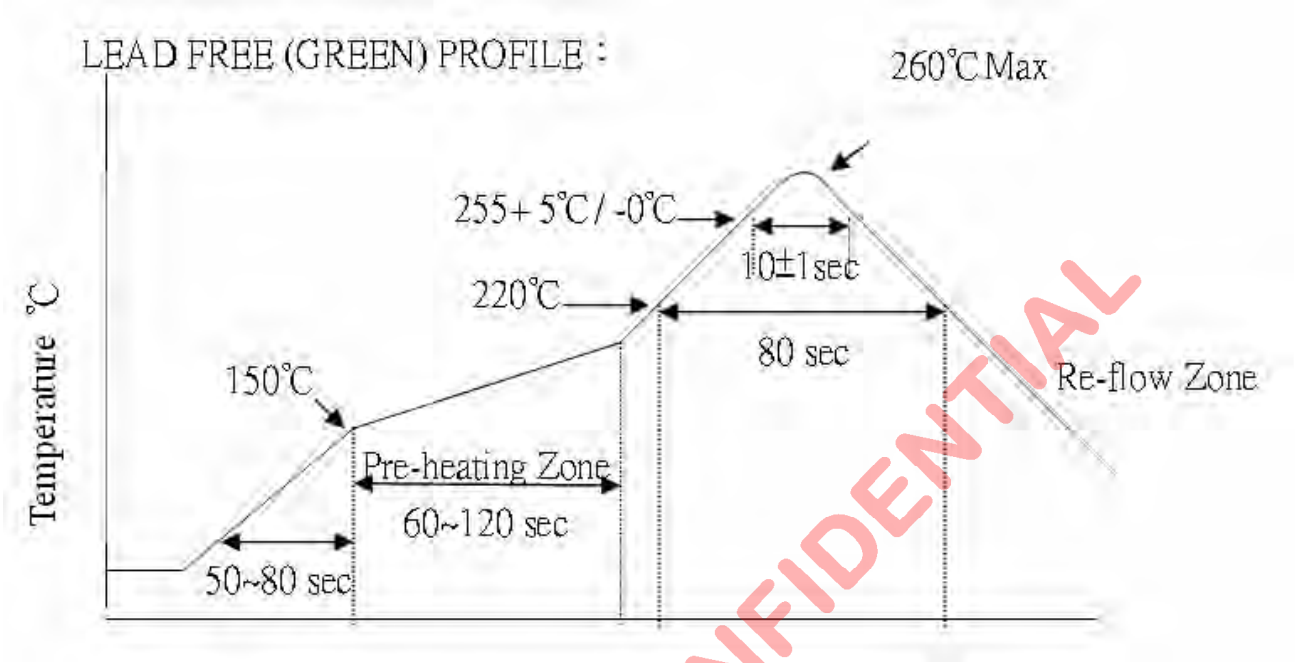


YYWW : DATECODE

X : PKG HOUSE ID

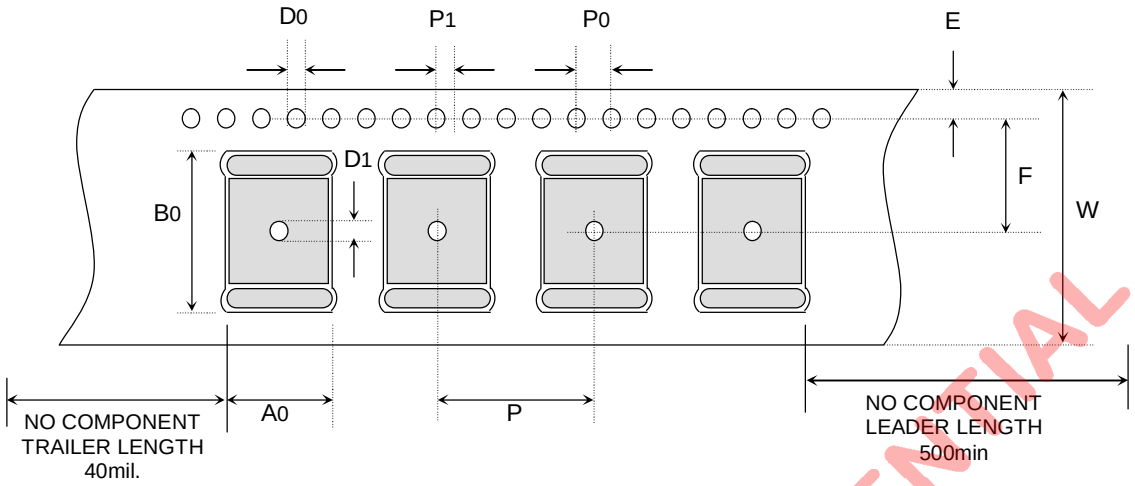
NNNNNNNNN : LOT NO.
(max. 9 characters)

24. Reflow Profile



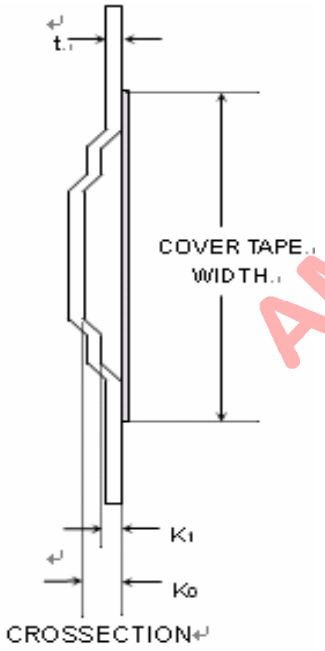
25. Tape Reel Information

Cover / Carrier Tape Dimension



11 EA IC **60cm±4cm**

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4X4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4X4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5X5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
48 QFN 7X7	12	7.25	7.25	4.0	2.0	1.5	1.5	1.75	7.5	16
DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16
28 SSOP (150mil)	8	6	10	4.0	2.0	1.5	1.5	1.75	7.5	16



TYPE	K0	K1	t
20 QFN (4X4)	1.1	-	0.3
24 QFN (4X4)	1.4	-	0.3
32 QFN (5X5)	1.1	-	0.3
48 QFN (7X7)	1.1	-	0.3
DFN-10	0.75	-	0.25
20 SSOP	2.5	-	0.3
24 SSOP	2.1	-	0.3
28 SSOP (150mil)	2.5	-	0.3

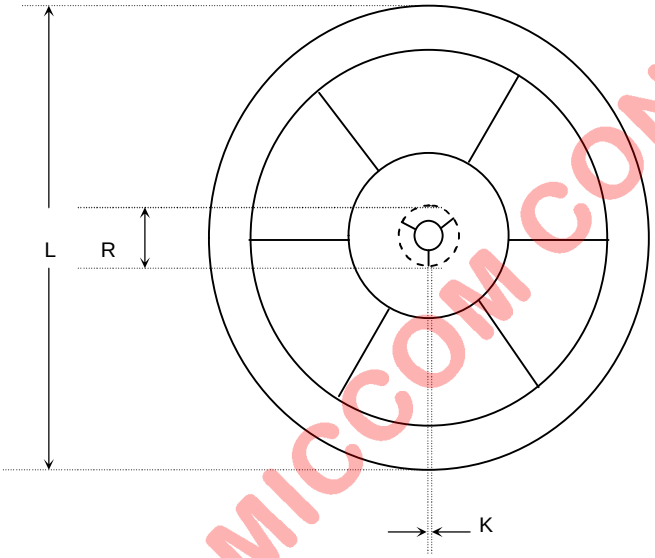
COVER TAPE WIDTH
9.2
9.2
9.2
13.3
8
13.3
13.3
12.5

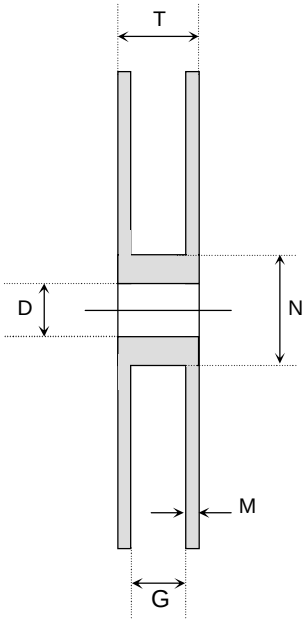
Unit : mm

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330+ 0.00/-1.0	20.2





26. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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