

**Document Title**

Low power 2.4GHz RF Transmitter with 2K ~ 2Mbps data rate.

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Issue Date</u>	<u>Remark</u>
0.0	Initial issue.	March, 2008	
0.1	Add state machine and reference layout	Feb , 2010	
0.2	Add deep sleep mode, revise sleep mode current	June, 2010	
0.3	Add TX current vs TX power	Nov., 2010	
0.4	Change English Company Name	Nov. 30, 2010	

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1. General Description

A7325 is a high performance and low cost 2.4GHz ISM band wireless transmitter. This device integrates high efficiency power amplifier (up to 5dBm). According to Data Rate Register, on-air data rates could be configured from 2Kbps to 2Mbps. In RX site, user can choose either A7105 (2K ~ 500Kbps TRX) or A7125 (1Mbps / 2Mbps TRX) to complete a one-way wireless system.

A7325 supports fast settling time (130 us) for frequency hopping system. For packet handling, A7325 has built-in 64-bytes TX FIFO (could be extended to 256 bytes) for data buffering and burst transmission, CRC for error detection, FEC for 1-bit data correction per code word, data whitening for data encryption / decryption. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 16 pins package.

A7325's control registers can be easily accessed via 3-wire or 4-wire SPI bus. For power saving, A7325 supports sleep mode, idle mode, standby mode. For easy-to-use, A7325 has a unique SPI command set called **Strobe command** that are used to control internal state machine. Based on Strobe commands via SPI bus, MCU can control everything from power saving, TX delivery, frequency hopping to auto calibrations. In addition, A7325 supports one general purpose I/O pin, GIO1, to inform MCU its status so that MCU could use either polling or interrupt scheme to do radio control. Hence, it is very easy to monitor radio transmission between MCU and A7325 because of its digital interface.

2. Typical Applications

- Wireless toys and game controllers
- Remote control
- Helicopter and airplane radio controller
- 2400 ~ 2483.5 MHz ISM system
- Wireless audio streaming
- Wireless video streaming

3. Feature

- Small size (QFN4 X4, 16 pins).
- Frequency band: 2400 ~ 2483.5MHz.
- FSK or GFSK modulation
- Deep sleep current (0.1 uA).
- Sleep mode current (2 uA).
- Low current consumption: TX 14.5mA (at 0dBm output power).
- Low current consumption: TX 16.5mA (at 5dBm output power).
- On chip regulator, support input voltage 2.0 ~ 3.6 V.
- Programmable data rate from 2Kbps to 2Mbps.
- Programmable TX power level from -17 dBm to 5 dBm.
- Fast settling time (130 us) synthesizer for frequency hopping system.
- Built-in Battery Detector.
- Support low cost crystal (8 / 12 / 16 / 24MHz).
- Support crystal sharing, (1 / 2 / 4 / 8MHz) to MCU.
- Customized USID (Unique Security ID) to avoid purposed system clone for copyright protection.
- Easy to use.
 - ◆ Support 3-wire or 4-wire SPI.
 - ◆ Unique Strobe command via SPI.
 - ◆ ONE register setting for new channel frequency.
 - ◆ Auto Calibrations.
 - ◆ Auto CRC.
 - ◆ Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
 - ◆ Data Whitening for encryption and decryption.
 - ◆ 64 bytes TX FIFO.
 - ◆ Easy FIFO / Segment FIFO / FIFO Extension (up to 256 bytes).
 - ◆ Support direct mode data input to GIO1 pin.

4. Pin Configurations

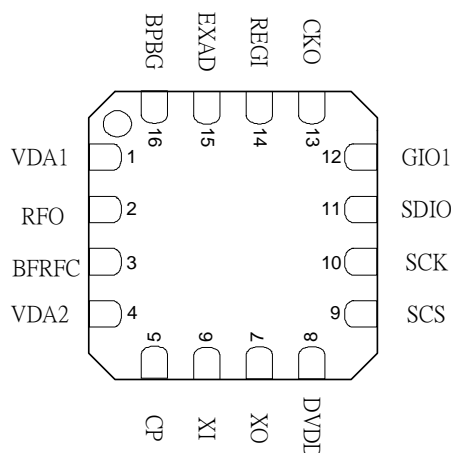


Fig4.1. A7325 QFN Package Top View

5. Pin Descriptions

Note: I: input; O: output, I/O: input or output

Pin No.	Symbol	I/O	Function Description
1	VDA1	O	Voltage supply TX analog part
2	RFO	O	Power amplifier output.
3	BFRFC	O	TX buffer output pin, connected to external bypass capacitor.
4	VDA2	I	Voltage supply for VCO analog part
5	CP	I	VCO frequency control input, internal connected to PLL charge pump.
6	XI	I	Crystal oscillator input node
7	XO	O	Crystal oscillator output node
8	DVDD	I	Voltage supply for PLL part and digital part
9	SCS	I	3 wire SPI chip select.
10	SCK	I	3 wire SPI clock input pin.
11	SDIO	I/O	3 wire SPI read/write data pin.
12	GIO1	I/O	General purpose I/O pin
13	CKO	O	Clock output pin
14	REGI	I	Regulator input
15	EXAD	I	External input for A/D conversion
16	BPBG	I	Regulator bias point
	Back side plate	G	Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.

6. Chip Block Diagram

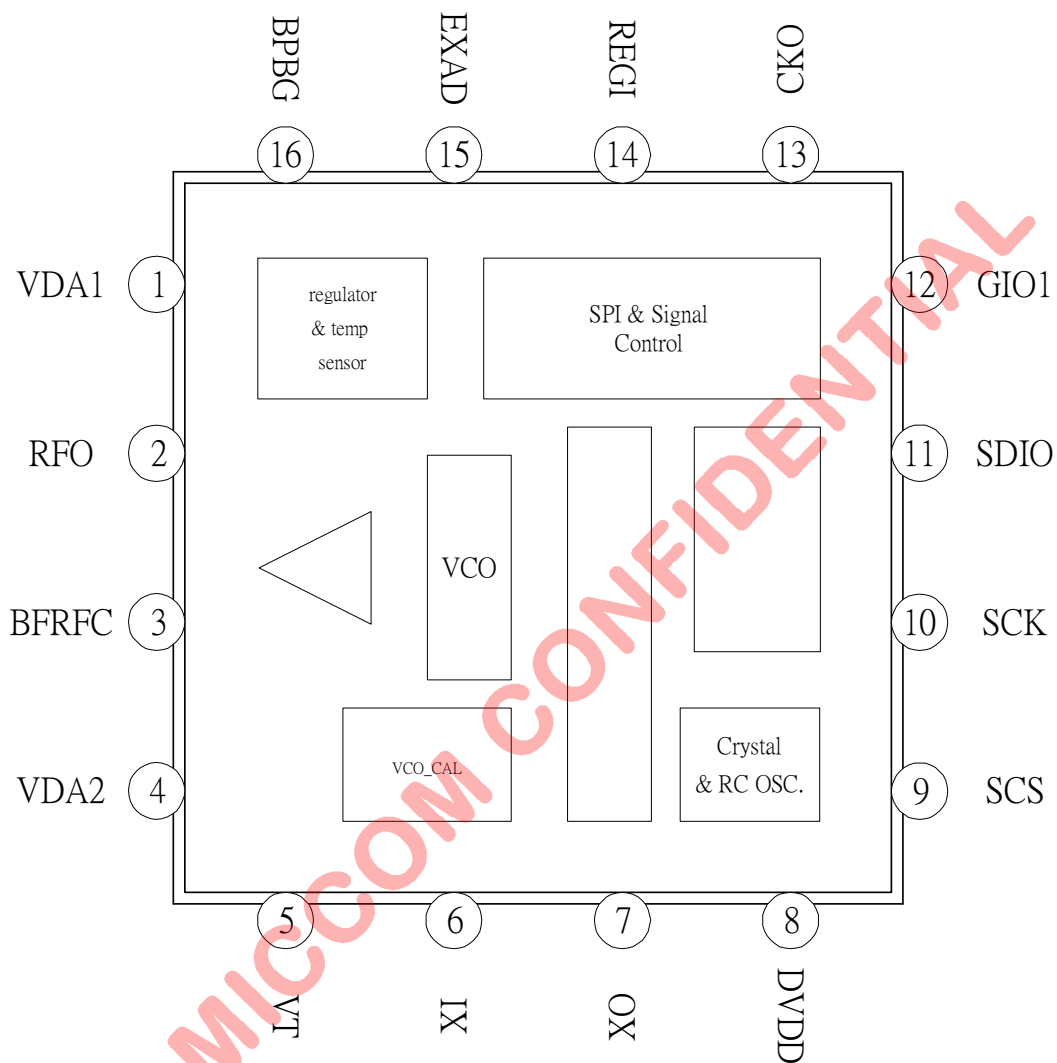


Fig6.1. Chip Block Diagram

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		5	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM	± 100	V

*Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.

*Device is Moisture Sensitivity Level III (MSL 3).



8. Specification

(Ta=25°C, VDD=3.0V, data rate= 500Kbps, IF bandwidth = 500KHz, F_{XTAL} =16MHz, with Match Networking and low pass filter, On Chip Regulator = 2.1V, unless otherwise noted.)

Parameter	Description	Min.	Type	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (with internal regulator)		2.0		3.6	V
Current Consumption ⁽¹⁾	Deep sleep mode (no data retention)		0.1		μA
	Sleep mode		2		μA
	Idle mode (regulator on)		0.3		mA
	Standby mode (Crystal OSC, regulator on)		1.8		mA
	PLL mode (Crystal OSC, regulator, PLL on)		9		mA
	TX mode (output power -17dBm)		10.7		mA
	TX mode (output power -5dBm)		11.5		mA
	TX mode (output power 0dBm)		14.5		mA
	TX mode (output power 5dBm)		16.5		mA
Synthesizer block (includes crystal oscillator, PLL and VCO.)					
Xtal start up time ^{*2}			1		mS
Xtal frequency			8 / 12 / 16 / 24		MHz
Xtal tolerance			±20	±50	ppm
Xtal ESR	C-load = 18 pF			60	ohm
VCO Operation Frequency		2400		2483.5	MHz
PLL phase noise	Offset 10 KHz		70		dBc
	Offset 100 KHz		75		
	Offset 500 KHz		100		
	Offset 2 MHz		110		
PLL settling time ^{*3}	Loop bandwidth 500K		70		μs
Transmitter					
Output power		-17	0	5	dBm
Data rate		2K		2M	Bps
Out Band Spurious Emission ^{*4}	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	dBm
	1.8GHz~ 1.9GHz			-47	dBm
	5.15GHz~ 5.3GHz			-47	dBm
Frequency deviation ^{*5}	Data rate > 50Kbps		186K		Hz
	Date rate <=50Kbps		124K		Hz
		25K		2M	Hz
TX settling time	Loop bandwidth 500K		60		μS
TX ready time ^{*6} (PLL to WPLL + WPLL to TX)	@Loop BW = 500 KHz, LO fixed		10+60		μS
	@Loop BW = 500 KHz, Hopping		70+60		μS
Regulator					

Regulator settling time	Pin 2 connected to 1.5 nF		500		μs
Band-gap reference voltage			1.23		V
Regulator output voltage		1.8	2.1	2.3	V
Line regulation	Load current 30mA	35	40		dBc
Digital IO DC characteristics					
High Level Input Voltage (V _{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V _{IL})		0		0.2*VDD	V
High Level Output Voltage (V _{OH})	@I _{OH} = -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V _{OL})	@I _{OL} = 0.5mA	0		0.4	V

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, leakage current will be induced.

Note 2: Refer to Delay Register II (17h) to set up crystal settling delay.

Note 3: Refer to Delay Register I (17h) to set up PDL (PLL settling delay).

Note 4: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.

Note 5: Refer to TX Register II (16h) to set up FD [7:0].

Note 6: Refer to Delay Register I (17h) to set up PDL and TDL delay.

9. Control Register

A7325 contains 45 x 8-bit control registers. MCU can access those control registers via 3-wire (SCS, SCK, SDIO) or 4-wire (SCS, SCK, SDIO, GIO1) SPI interface (support max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details of SPI timing. A7325 is simply controlled by registers and outputs its status to MCU by GIO1 pins.

Note: In sleep mode the read function from SPI registers is not allowed.

9.1 Control register table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h MODE	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
	R	--	--	--	CER	XER	PLLER	TRSR	TRER
01h MODEC	R/W	DDPC	--	--	SPSS	WOTE	--	FMS	ADCM
02h CALC	R/W	--	--	--	VCC	VBC	VDC	--	--
03h FIFO1	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
04h FIFO2	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
05h FIFOD	W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h IDD	W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
07h RCOSC1	W	WOTDLY7	WOTDLY6	WOTDLY5	WOTDLY4	WOTDLY3	WOTDLY2	WOTDLY1	WOTDLY0
	R	--	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
08h RCOSC2	W	WOTDLY9	WOTDLY8	WRDLY5	WRDLY4	WRDLY3	WRDLY2	WRDLY1	WRDLY0
09h RCOSC3	W	BBCKS1	BBCKS0	RCOT1	RCOT0	CALW	RCOSC_E	TSEL	TWOT_E
0Ah CKO	W	DDCKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GIO1	W	--	--	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch Clock	R/W	IFS	CSC	GRC3	GRC2	GRC1	GRC0	CGS	XS
0Dh Data rate	R/W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
0Eh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
0Fh PLL II	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IPO8
10h PLL III	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
	R	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
11h PLL IV	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
12h PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
13h CHG1	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
14h CHG2	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0

15h TX1	W	--	TMDE	TXDI	TME	FS	FDP2	FDP1	FDP0
16h TX2	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
17h DELAY1	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
18h DELAY2	W	WSEL2	WSEL1	WSEL0	RGC1	RGC0	--	WOTS1	WOTS0
19h ADC	W	AVSEL1	AVSEL0	RADC	FSARS	MVSEL1	MVSEL0	XADS	CDM
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
1Ah CODE1	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
1Bh CODE2	W	HWCKS	WS6	WS5	WS4	WS3	WS2	WS1	WS0
1Ch VCOC	W	--	--	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
1Dh VCOCB1	W	DCD1	DCD0	MDAGS	DMGS	MVBS	MVB2	MVB1	MVB0
	R	--	--	--	--	VBCF	VB2	VB1	VB0
1Eh VCOCB2	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
1Fh VCODC1	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
20h VCODC2	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
21h VCODC3	R/W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
22h VCOMD	W	MDEN	CMV	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
23h BD	W	RGS	RGV1	RGV0	LVR	BVT2	BVT1	BVT0	BD_E
	R	RGS	RGV1	RGV0	BDF	BVT2	BVT1	BV0	BD_E
24h TXT	W	TXSM1	TXSM0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
25h CPC	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
26h XTLT	W	VRPL1	VRPL0	INTXC	INTPRC	DBD	XCC	XCP1	XCP0
27h PLLT	W	CPH	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
28h VCOT	W	OLM	SDMS	VTBS	TLB1	TLB0	RSIS	ROSCS	VBHC
29h CHS	W	XADPS	RFT2	RFT1	RFT0	CHD3	CHD2	CHD1	CHD0
2Ah VRB	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
2Bh RTX	W	QDS	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
2Ch INTS	W	CELS	PWORS	STS	IXTLS4	IXTLS3	IXTLS2	IXTLS1	IXTLS0

Legend: - = unimplemented

9.2 Control register description

9.2.1 Mode Register (MODE at address: 00h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode	R		--	--	CER	XER	PLLER	TRSR	TRER
	W	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN	RESETN
Reset		--	--	--	--	--	--	--	--

RESETN: Write to this register by 0x00 to issue reset command, then it is auto clear

CER: RF chip enable status.

[0]: RF chip is disabled. [1]: RF chip is enabled.

XER: Internal crystal oscillator enable status.

[0]: Crystal oscillator is disabled. [1]: Crystal oscillator is enabled.

PLLE: PLL enable status.

[0]: PLL is disabled. [1]: PLL is enabled.

TRER: TRX state enable status.

[0]: TRX is disabled. [1]: TRX is enabled.

TRSR: TRX Status Register.

[0]: Not TX state. [1]: TX state.

9.2.2 Mode Control Register (MODEC at address 01h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control I	W	DDPC	--	--	SPSS	WOTE	--	FMS	ADCM
	R	DDPC	--	--	SPSS	WOTE	--	FMS	ADCM
Reset		0	--	--	--	0	--	0	0

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin when this register is enabled.

[0]: Disable. [1]: Enable.

SPSS: Reserved for internal usage only. Shall be set to [0].

WOTE: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.

[0]: Direct mode. [1]: FIFO mode.

ADCM: ADC measurement enable (Auto clear when done).

[0]: Disable measurement or measurement finished. [1]: Enable measurement.

9.2.3 Calibration Control Register (CALC at address 02h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control II	W/R	--	--	--	VCC	VBC	VDC	--	--
Reset		--	--	--	0	0	0	--	--

VCC: VCO Current calibration enable (Auto clear when done).

[0]: Disable. [1]: Enable .

VBC: VCO Bank calibration enable (Auto clear when done).

[0]: Disable. [1]: Enable.

VDC: VCO Deviation calibration enable (Auto clear when done).

[0]: Disable. [1]: Enable.

9.2.4 FIFO Register I (FIFO1 at address 03h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
------	-----	-------	-------	-------	-------	-------	-------	-------	-------

FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FEP [7:0]: FIFO End Pointer for TX FIFO.

Refer to chapter 16 for details.

9.2.5 FIFO Register II (FIFO2 at address 04h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FPM [1:0]: FIFO Pointer Margin

PSA [5:0]: Used for Segment FIFO.

Refer to chapter 16 for details.

9.2.6 FIFO DATA Register (FIFOD at address 05h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFOD	W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

FIFO [7:0]: FIFO data. (Write only).

TX FIFO and RX FIFO share the same address (05h).

Refer to chapter 16 for details.

9.2.7 ID DATA Register (IDD at address 06h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDD	W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0

ID [7:0]: ID data.

Once this address is accessed, ID Data is input/output in sequence corresponding to Write or Read.

Refer to chapter 16 for details.

9.2.8 RC OSC Register I (RCOSC1 at address 07h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC1	W	WOT_SL7	WOT_SL6	WOT_SL5	WOT_SL4	WOT_SL3	WOT_SL2	WOT_SL1	WOT_SL0
	R	--	RCOC6	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
Reset		0	0	0	0	0	0	0	0

RCOC [6:0]: RC Oscillator Output Calibration.

Refer to chapter 20 for details.

9.2.9 RC OSC Register II (RCOSC2 at address: 08h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCOSC2	W	WOT_SL9	WOT_SL8	WOT_AC5	WOT_AC4	WOT_AC3	WOT_AC2	WOT_AC1	WOT_AC0
Reset		0	0	0	0	0	0	0	1

WOT_AC [5:0]: 6-bits WOT_AC Timer for TWOT Function (244us ~ 15.6ms).

WOT_SL [9:0]: 10-bits WOT_SL Timer for TWOT Function (7.8ms ~ 7.99s).

WOT_SL [9:0] are from address (07h) and (08h).

9.2.10 RC OSC Register III (RCOSC3 at address: 09h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
------	-----	-------	-------	-------	-------	-------	-------	-------	-------

RCOSC3I	W	BBCKS1	BBCKS0	RCOT1	RCOT0	CALW	RCOSC_E	TSEL	TWOT_E
Reset		0	0	0	1	1	1	0	1

BBCKS [1:0]: Clock select for digital block. Recommend BBCKS = [00]

[00]: $F_{SYCK} / 1$. [01]: $F_{SYCK} / 2$. [10]: $F_{SYCK} / 4$. [11]: $F_{SYCK} / 8$.

F_{SYCK} is A7325's System clock = 16MHz.

RCOT [1:0] : RC oscillator current selection. Recommend RCOT = [00]

CALW: RC oscillator calibration active.

[0]: Disable. [1]: Enable.

RCOSC_E: RC oscillator enable.

[0]: Disable. [1]: Enable.

TSEL: Timer select for TWOT function.

[0]: Use WOT_AC. [1]: Use WOT_SL.

TWOT_E: Enable TWOT function.

[0]: Disable. [1]: Enable.

9.2.11 CKO Pin Control Register (CKO at address 0Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CKO Pin Control	W	DDCKOE	CKOS3	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
Reset		1	0	1	1	0	0	1	0

DDCKOE: External Clock Output Enable for CKOS [3:0]= [0100] ~ [0111].

[0]: Disable. [1]: Enable.

CKOS [3:0]: CKO pin output select.

[0000]: BCK (TX bit clock).

[0001]: MRCK (modulation rate).

[0010]: FPF (FIFO pointer flag).

[0011]: EOP, EOVCB, EOADC, EOVCB, OKADC (Internal usage only).

[0100]: External clock output= $F_{SYCK} / 2$.

[0101]: External clock output / 2= $F_{SYCK} / 4$.

[0110]: External clock output / 4= $F_{SYCK} / 8$.

[0111]: External clock output / 8= $F_{SYCK} / 16$.

[1000]: Wake up radio clock.

[1001]: 8 Mhz clock.

[1010]: internal ring OSC..

CKOI: CKO pin output signal invert.

[0]: Non-inverted output. [1]: Inverted output.

CKOE: CKO pin Output Enable.

[0]: High Z. [1]: Enable.

SCKI: SPI clock input invert.

[0]: Non-inverted input. [1]: Inverted input.

9.2.12 GIO1 Pin Control Register I (GPIO1 at address: 0Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GPIO1	W	--	--	GIO1S3	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
Reset		--	--	0	0	0	0	0	1

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state
[0000]	WTR (Wait until TX)

[0001]	EOAC(end of access code)
[0010]	TMEO(TX modulation enable)
[0011]	TMEOD (delta sigma TX modulation enable) output.
[0100]	WAK (For TWOT only)
[0101]	Direct mode data input.
[0110]	SDO (4 wires SPI data out)
[0111]	Direct mode data input.
[1000]	Internal FPF output
[1001]	Internal PDN_TX
[1010]	Data rate output
[1011]	Reserve, for FIFO mode data output
[11xx]	Reserved

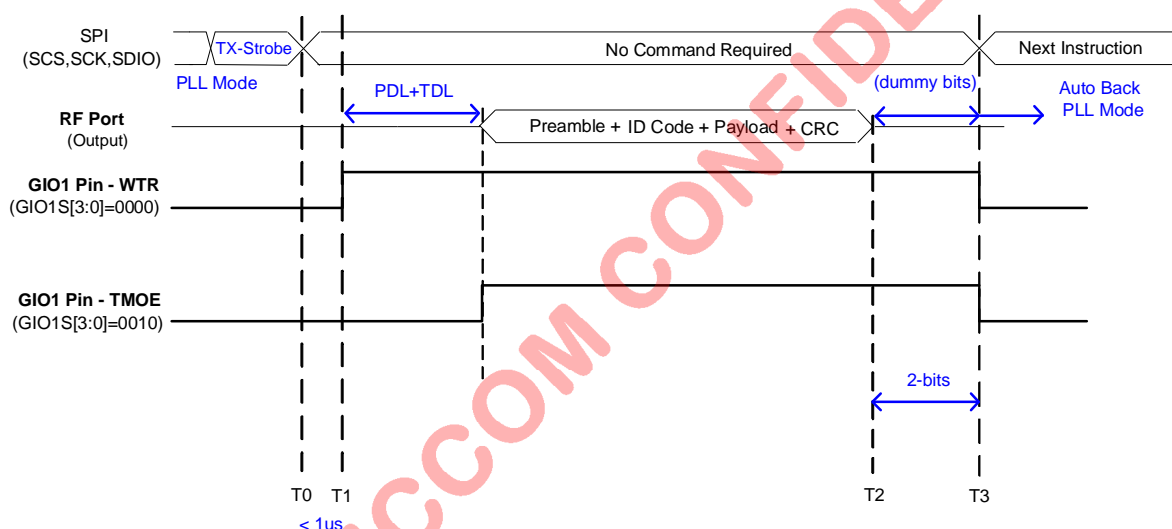
GIO1I: GIO1 pin output signal invert.

[0]: Non-inverted output. [1]: Inverted output.

GIO1OE: GIO1 pin output enable.

[0]: High Z. [1]: Enable.

In TX mode



9.2.13 Clock Register (Address: 0Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clock	RW	IFS	CSC	GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0	1	0	1	1	1	1	1

IFS: Maximum data rate setting

[0]: 500K bps. [1]: 2M bps.

CSC: system clock FSYCK divider select. Recommend CSC = [0]

[0]: $F_{CSCK} / 1$. [1]: $F_{CSCK} / 2$.

GRC [3:0]: Clock generation reference counter. Recommend GRC = [0111]

GRC is used to get 2 MHz Clock Generator Reference (F_{CGR}) for internal usage.

Clock generation reference = $F_{CSCK} / (GRC+1)$. Maximum divide ratio is 16.

F_{CSCK} is A7325's master clock. Refer to chapter 13 and 14 for details

CGS: Clock generator enable. Recommend CGS = [0]

[0]: Disable. [1]: Enable.

XS: Crystal oscillator select. Recommend XS = [1]

[0]: Use external clock. [1]: Use external crystal.

Master clock frequency	CGS = 0	CGS = 1
DBL = 0	Crystal frequency	32 MHz
DBL = 1	2*crystal frequency	32 MHz

Refer to chapter 13 and 14 for details

9.2.14 Data Rate Register (DR at address: 0Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DR	R/W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
Reset		0	0	0	0	0	0	0	0

SDR [7:0]: Data rate division selection.

Data rate = system clock / (8*(4-3*IFS)*(SDR [7:0]+1))

Refer to chapter 13 for details

9.2.15 PLL Register I (PLL1 at address 0Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL1I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

CHN [7:0]: LO channel number select.

Refer to chapter 14 for details.

9.2.16 PLL Register II (PLL2 at address 0Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL2I	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
Reset		0	0	1	0	1	1	1	0

DBL: Crystal frequency doubler selection. Recommend DBL = [0]

[0]: Disable. $F_{XREF} = F_{XTAL}$. [1]: Enable. $F_{XREF} = 2 * F_{XTAL}$.

RRC [1:0]: RF PLL reference counter setting. Recommend RRC = [00]

CHR [3:0]: PLL channel step setting. Recommend BBCKS = [0111]

Refer to chapter 14 for details.

9.2.17 PLL Register III (PLL3 at address: 10h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL III	W	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	R	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		1	0	0	1	0	1	0	0

BIP [8:0]: LO base frequency integer part setting.

BIP [8:0] are from address (0Fh) and (10h),

IP [8:0]: LO frequency integer part value.

IP [8:0] are from address (0Fh) and (10h),

Refer to chapter 14 for details.

9.2.18 PLL Register IV (PLL4 at address 11h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL4	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
Reset		0	0	0	0	0	0	0	0

9.2.19 PLL Register V (PLL5 at address 12h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset		0	0	0	0	0	1	0	0

BFP [15:0]: LO base frequency fractional part setting.

BFP [15:0] are from address (11h) and (12h),

FP [15:0] (Read): LO frequency fractional part setting.

Refer to chapter 14 for details.

9.2.20 Channel group Register I (CHG1 at address 13h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHG1	R/W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	1	1	1	0	0

CHGL [7:0]: PLL channel group low boundary setting.

Refer to chapter 15 for details.

9.2.21 Channel group Register II (CHG2 at address 14h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHG2	R/W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	1	1	1	0	0	0

CHGH [7:0]: PLL channel group high boundary setting.

Refer to chapter 15 for details.

PLL frequency is divided into 3 groups:

	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

9.2.22 TX Register I (TX1 at address 15h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX1	W		TMDE	TXDI	TME	FS	FDP2	FDP1	FDP0
Reset			1	0	1	0	1	1	0

TMDE: VCO modulation enable. Recommend TMDE = [1]

[0]: Disable. [1]: Enable.

TXDI: TX data invert. Recommend TXDI = [0].

[0]: Non-invert. [1]: Invert.

TME: TX modulation enable. Recommend TME = [1]

[0]: Disable. [1]: Enable.

FS: Filter select. The filter shape is gaussian filter (BT=0.7).

[0]: disable. [1]: enable.

FDP [2:0]: Frequency deviation power setting. Recommend FDP = [110]

Refer to TX Register II (16h)

9.2.23 TX Register II (TX2 at address 16h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX2	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		1	1	0	0	0	0	0	0

FD [7:0]: Frequency deviation setting.

TX modulation frequency deviation = $F_{PFD} * 127 * 2^{FDP[2:0]} * (FD[4:0] + 1) / 2^{24}$

Where F_{PFD} , the PLL comparison frequency, is equal to crystal frequency * (DBL+1) / ((RRC [1:0]+1).

Data Rate (Kbps)	F_{PFD}	FDP [2:0]	FD[7:0]	Fdev (KHz)
<= 50Kbps	16MHz	110	0x1F	124
Data Rate (Kbps)	F_{PFD}	FDP [2:0]	FD[7:0]	Fdev (KHz)
500K ~ 50Kbps	16MHz	110	0x2F	186
Data Rate (Kbps)	F_{PFD}	FDP [2:0]	FD[7:0]	Fdev (KHz)
2M / 1Mbps	16MHz	110	0x80	500

9.2.24 Delay Register I (DELAY1 at address 17h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delay	W	DPR2	DPR1	DPR0	TDL1	TDL0	PDL2	PDL1	PDL0
Reset		0	0	0	1	0	0	1	0

DPR [2:0]: Delay scale. Recommend DPR = [000].

TDL [1:0]: Delay for TX settling from WPLL to TX.

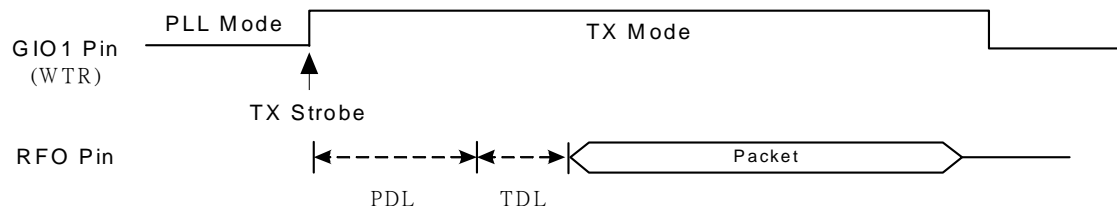
Delay = $20 * (TDL[1:0] + 1) * (DPR[2:0] + 1)$ us.

DPR [2:0]	TDL [1:0]	WPLL to TX	Note
000	00	20 us	
000	01	40 us	
000	10	60 us	Recommend
000	11	80 us	

PDL [2:0]: Delay for TX settling from PLL to WPLL.

Delay = $10 + 20 * (PDL[2:0] + 1) * (DPR[2:0] + 1)$ us.

DPR [2:0]	PDL [2:0]	PLL to WPLL (LO freq. fixed)	PLL to WPLL (LO freq changed)	Note
000	001	10 us	50 us	
000	010	10 us	70 us	Recommend
000	011	10 us	90 us	
000	100	10 us	110 us	



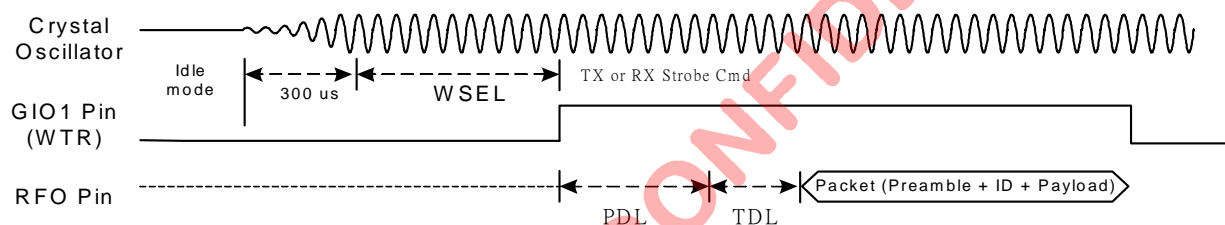
9.2.25 Delay Register II (DELAY2 at address: 18h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Delay	W	WSEL2	WSEL1	WSEL0	RGC1	RGC0		WOTS1	WOTS0
Reset		0	1	0	0	0	--	0	0

WSEL [2:0]: XTAL settling delay setting (200us ~ 2.5ms). Recommend WSEL = [010].

[000]: 200us. [001]: 400us. [010]: 600us. [011]: 800us.

[100]: 1ms. [101]: 1.5ms. [110]: 2ms. [111]: 2.5ms.



RGC [1:0]: Reserved for internal usage only. Shall be set to [01].

WOTS [1:0]: the repetition times of wake on transmission.

[00]: 1. [01]: 2. [10]: 3. [11]: 4.

9.2.26 ADC Control Register (ADC at address 19h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC	W	AVSEL1	AVSEL0	RADC	FSARS	MVSEL1	MVSEL0	XADS	CDM
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset		1	0	0	0	1	1	0	0

AVSEL [1:0]: ADC average times (VCO calibration). Recommend AVSEL = [11].

[00]: Average 8 times. [01]: Average 16 times. [10]: Average 32 times. [11]: Average 64 times.

RADC: ADC reading select. Recommend RADC = [0].

[0]: reading of ADC average for MVSEL mode.

[1]: reading of ADC average for AVSEL mode.

MVSEL [1:0]: ADC average times. Recommend MVSEL = [11].

[00]: No average. [01]: Average 2 times. [10]: Average 4 times. [11]: Average 8 times.

FSARS: ADC clock select. Recommend FSARS = [0].

[0]: 4MHz. [1]: 8MHz.

XADS: ADC input signal select.

[0]: Convert internal temperature. [1]: Convert external voltage,

CDM: continuous measurement mode. Recommend CDM = [0].

[0]: Single mode. [1]: Continuous mode.

ADC [7:0]: ADC output value of temperature or external voltage measurement.

ADC input voltage= 0.3 + 1.2 * ADC [7:0] / 256 V.

Refer to chapter 17 for details.

9.2.27 Code Register I (CODE1 at address 1Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CODE1I	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
Reset		0	0	0	0	0	1	1	1

MCS: Maches Code Select

[0]: Disable. [1]: Enable.

WHTS: Data whitening (Data Encryption) select.

[0]: Disable. [1]: Enable.

FECS: FEC select.

[0]: Disable. [1]: Enable.

CRCS: CRC select.

[0]: Disable. [1]: Enable.

IDL: ID code length select. Recommend IDL= [01].

[00]: 2 bytes. [01]: 4 bytes. [10]: 6 bytes. [11]: 8 bytes.

PML [1:0]: Preamble length select. Recommend PML= [11].

[00]: 1 byte. [01]: 2 bytes. [10]: 3 bytes. [11]: 4 bytes.

Refer to chapter 16 for details.

9.2.28 Code Register II (CODE2 at address: 1Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CODE2	W	HWCKS	WS6	WS5	WS4	WS3	WS2	WS1	WS0
Reset		--	0	1	0	1	0	1	0

HWCKS: WOT calibration reference clock selection. Recommend HWCKS = [0].

[0]: 4KHz. [1]: 2KHz.

WS [6:0]: Data Whitening seed setting (data encryption key).

Refer to chapter 16 for details.

9.2.29 VCO current Calibration Register (VOCC at address 1Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOC	W	--	--	VCCS	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
Reset		--	--	1	0	1	1	0	0

VCCS: Reserved for internal usage only. Shall be set [1].

MVCS: VCO current calibration value select. Recommend MVCS = [0].

[0]: Auto calibration value. [1]: Manual calibration value.

VCOC [3:0]: VCO current manual calibration value. Recommend VCOC = [1100].

VCCF: VCO current auto calibration flag.

[0]: Pass. [1]: Fail.

VCB [3:0]: VCO current calibration value.

MVCS= 0: Auto calibration value (VCB).

MVCS= 1: Manual calibration value (VCOC).

Refer to chapter 15 for details.

9.2.30 VCO band Calibration Register I (VCOBC1 at address 1Dh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOBC1	W	DCD1	DCD0	DAGS	DMGS	MVBS	MVB2	MVB1	MVB0
	R	--	--	--	--	VBCF	VB2	VB1	VB0
Reset		1	1	0	--	0	1	0	0

DCD [1:0]: VCO deviation calibration delay. Recommend DCD = [11].

Delay time = PLL delay time \times (DCD + 1).

MDAGS: DAG calibration value select. Recommend MDAGS = [0].

[0]: Auto calibration value. [1]: Manual calibration value.

DAGS: reserved. For internal testing. Shall be set to [0].

DMGS: reserved. For internal testing. Shall be set to [0].

MVBS: VCO bank calibration value select. Recommend MVBS = [0].

[0]: Auto calibration value. [1]: Manual calibration value.

MVB [2:0]: VCO band manual calibration value. Recommend MVB = [100].

VBCF: VCO band auto calibration flag.

[0]: Pass. [1]: Fail.

VB [2:0]: VCO bank calibration value.

MVBS= 0: Auto calibration value (AVB).

MVBS= 1: Manual calibration value (MVB).

Refer to chapter 15 for details.

9.2.31 VCO band Calibration Register II (VCOBC2 at address 1Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOBC2	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
Reset		1	0	0	0	0	0	0	0

MDAG [7:0]: DAG manual calibration value. Recommend MDAG = [0x80].

ADAG [7:0]: DAG auto calibration value.

9.2.32 VCO Deviation Calibration Register I (VCODC1 at address 1Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCODC1	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
Reset		0	1	1	1	0	0	0	0

DEVS [3:0]: Deviation output scaling. Recommend DEVS = [0011].

DAMR_M: DAMR manual enable. Recommend DAMR_M = [0].

[0]: Disable. [1]: Enable.

VMTE_M: VMT manual enable. Recommend VMTE_M = [0].

[0]: Disable. [1]: Enable.

VMS_M: VM manual enable. Recommend VMS_M = [0].

[0]: Disable. [1]: Enable.

MSEL: VMS, VMTE and DAMR control select. Recommend MSEL = [0].

[0]: Auto control. [1]: Manual control.

DEVA [7:0]: Deviation output value.

MVDS= 0: Auto calibration value ((ADEV / 8) × (DEVS + 1)),

MVDS= 1: Manual calibration value (MDEV).

9.2.33 VCO Deviation Calibration Register II (VCODC2 at address 20h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCODC2	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
Reset		0	0	1	0	1	0	0	0

MVDS: VCO deviation calibration value select. Recommend MVDS = [0].

[0]: Auto calibration value. [1]: Manual calibration value.

MDEV [6:0]: VCO deviation manual calibration value. Recommend MDEV = [0110101].

ADEV [7:0]: VCO deviation auto calibration value.

Refer to chapter 15 for details.

9.2.34 VCO Deviation Calibration Register III (VCODC3 at address 21h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCODC3	R/W	VMG7	VMG6	VMG5	VMG4	VMG3	VMG2	VMG1	VMG0
Reset		1	0	0	0	0	0	0	0

VMG [7:0]: Reserved for internal usage only. Shall be set to [0x80].

9.2.35 VCO Modulation Delay Register (VCOMD at address 22h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOMD	W	MDEN	CMV	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		0	0	0	0	0	0	0	0

MDEN: Reserved for internal usage only. Shall be set to [0].

CMV: modulation D/A scale select.

[0]: 1/4 * 1.2V. [1]: 1/8 * 1.2V

DEVFD [2:0]: Reserved for internal usage only. Shall be set to [000].

DEVD [2:0]: Reserved for internal usage only. Shall be set to [010].

9.2.36 Battery detect Register (BD at address: 23h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BD	W	RGS	RGV1	RGV0	LVR	BVT2	BVT1	BVT0	BD_E
	R	RGS	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

RGS: VDD_D voltage setting in Sleep mode. Recommend RGS = 0.

RGV [1:0]: VDD_D and VDD_A voltage setting in non-Sleep mode. Recommend RGV = [11].

[00]: 2.1V. [01]: 2.0V. [10]: 1.9V. [11]: 1.8V.

LVR: Reserved for internal usage only. Shall be set [1].

BVT [2:0]: Battery voltage detect threshold.

[000]: 2.0V. [001]: 2.1V. [010]: 2.2V. [011]: 2.3V.

[100]: 2.4V. [101]: 2.5V. [110]: 2.6V. [111]: 2.7V.

BD_E: Battery detect enable.

[0]: Disable. [1]: Enable. It will be clear after battery detection done.

BDF: Battery detect flag.

[0]: Battery voltage less than threshold. [1]: Battery voltage greater than threshold.

Refer to chapter 18 for details.

9.2.37 TX test Register (TXT at address 24h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXT	W	TXSM1	TXSM0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		0	0	0	1	0	1	1	1

TXSM [1:0]: Moving average for non-filter select. Recommend TXSM = [00].

[00]: not moving average. [01]: 2 moving average. [10]: 4 moving average. [11]: 8 moving average.

TXCS: TX Current Setting. Recommend TXCS = [0].

PAC [1:0]: PA Current Setting. Recommend PAC = [10].

TBG [2:0]: TX Buffer Setting. Recommend TBG = [111].

Refer to chapter 19 for details.

9.2.38 Charge Pump Current Register (CPC at address 25h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CPC	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	1	1	1	1

CPM [3:0]: Charge pump current setting for VM loop. Recommend CPM = [1111].

Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge pump current setting for VT loop. Recommend CPT = [0001].

Charge pump current = (CPT + 1) / 16 mA.

9.2.39 Crystal test Register (XTLT at address 26h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Crystal test	W	VRPL1	VRPL0	INTXC	INTPRC	DBD	XCC	XCP1	XCP0
Reset		0	0	0	0	0	1	0	1

VRPL [1:0]: Internal PLL register select

[00]: 500 ohm. [01]: 666 ohm. [10]: 1K ohm. [11]: 2K ohm.

INTXC: Internal crystal capacitor enable. Recommend INTXC = [1]

[0]: Disable. [1]: Enable.

INTPRC: Internal PLL capacitor and resistor enable. Recommend INTPRC = [1]

[0]: Disable. [1]: Enable.

DBD: Reserved for internal usage only. Shall be set to [0].

XCC: Reserved for internal usage only. Shall be set to [1].

XCP [1:0]: Reserved for internal usage only. Shall be set to [01].

9.2.40 PLL Test Register (PLLT at address: 27h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL test	W	CPH	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
Reset		1	1	0	0	0	1	0	1

CPH: high current mode enable of Charge pump. Recommend CPH = [1].

CPS: Reserved for internal usage only. Shall be set to [1].

PRRC [1:0]: Reserved for internal usage only. Shall be set to [01].

PRIC [1:0]: Reserved for internal usage only. Shall be set to [01].

SDPW: Reserved for internal usage only. Shall be set to [0].

NSDO: Reserved for internal usage only. Shall be set to [1].

9.2.41 VCO Test Register (VCOT at address: 28h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VCOT	W	OLM	SDMS	VTBS	TLB1	TLB0	RSIS	ROSCS	VBHC
Reset		0	1	0	1	1	0	0	0

OLM: Reserved for internal usage only. Shall be set to [0].

SDMS: Reserved for internal usage only. Shall be set to [1].

VTBS: Reserved for internal usage only. Shall be set to [0].

TLB [1:0]: Reserved for internal usage only. Shall be set to [01].

RSIS: current bias selection for differential mode ring OSC. Shall be set to [0].

ROSCS: ring Oscillation selection. Shall be set to [0].

[0]: single mode. [1]: differential mode.

VBHC: Reserved for internal usage only. Shall be set to [0].

9.2.42 Channel Select Register (CHS at address 29h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHS	W	XADPS	RFT2	RFT1	RFT0	CHD3	CHD2	CHD1	CHD0
Reset		--	--	--	--	0	1	0	0

XADPS: External ADC pin selection. Recommend XADPS = [0].

RFT [2:0]: RF analog pin configuration for testing. Below is the connection table for pin EXAD.

{XADPS, RFT[2:0]}	XADI	BPBG
[0000]	For external AD input.	Band-gap voltage
[0001]	Analog temperature voltage	Band-gap voltage
[0010]	Internal DA output	Band-gap voltage
[0011]	Low power current source	Band-gap voltage
[10XX]	For external AD input.	Band-gap voltage

CHD [3:0]: The channel frequency offset setting for deviation calibration. Recommend CHD = [1000].

Offset channel number = +/- (CHD+1).

9.2.43 VRB Register (VRB at address: 2Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VRB	W	VTRB3	VTRB2	VTRB1	VTRB0	VMRB3	VMRB2	VMRB1	VMRB0
Reset		0	0	0	0	0	0	0	0

VTRB [3:0]: Resistor bank for VT RC filtering. Recommend VTRB = [0000].

VMRB [3:0]: Resistor bank for VM RC filtering. Recommend VMRB = [0000].

9.2.44 RTX Register (RTX at address: 2Bh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTX	W	QDS	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS

Reset		0	0	0	0	0	0	0	0
-------	--	---	---	---	---	---	---	---	---

QDS: regulator quick charge select. Shall be set to [1].

TRT [2:0]: TX ramping time select. Recommend TRT = [111].

Ramping down time = $2 \times \text{TRT}$ us

[000]: 2us. [001]: 4us. [010]: 6us. [011]: 8us.

[100]: 10us. [101]: 12us. [110]: 14us. [111]: 16us.

ASMV [2:0]: TX ramp up timing select. Recommend ASMV = [111].

Ramping up time = $2 \times \text{ASMV}$ us

[000]: 2us. [001]: 4us. [010]: 6us. [011]: 8us.

[100]: 10us. [101]: 12us. [110]: 14us. [111]: 16us.

AMVS: TX ramping up and down select. Recommend AMVS = [1].

[0]: disable, [1]: enable.

9.2.44 INTS Register (INTS at address: 2Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RTX	W	CELS	PWORS	STS	IXTLS4	IXTLS3	IXTLS2	IXTLS1	IXTLS0
Reset		0	0	0	1	0	0	0	0

CELS: reserved for internal used. Shall be set to [1].

PWORS: reserved for internal used. Shall be set to [0].

STS: reserved for internal used. Shall be set to [0].

IXTALS [4:0]: Internal crystal capacitor value selection. Recommend IXTALS = [10100].

10. SPI

A7325 only supports one SPI interface with maximum data rate up to 10Mbps. MCU should assert SCS pin low (SPI chip select) to active accessing of A7325. Via SPI interface, user can access **control registers** and issue **Strobe command**. Figure 10.1 gives an overview of SPI access manners.

3-wire SPI (SCS, SCK and SDIO) or 4-wire SPI (SCS, SCK, SDIO and GIO1) configuration is provided. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 pin is data output. In such case, GIO1S should be set to [0110].

For SPI write operation, SDIO pin is latched into A7325 at the rising edge of SCK. For SPI read operation, if input address is latched by A7325, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

To control A7325's internal state machine, it is very easy to send Strobe command via SPI interface. The Strobe command is a unique command set with total 8 commands. See section 10.3, 10.4 and 10.5 for details.

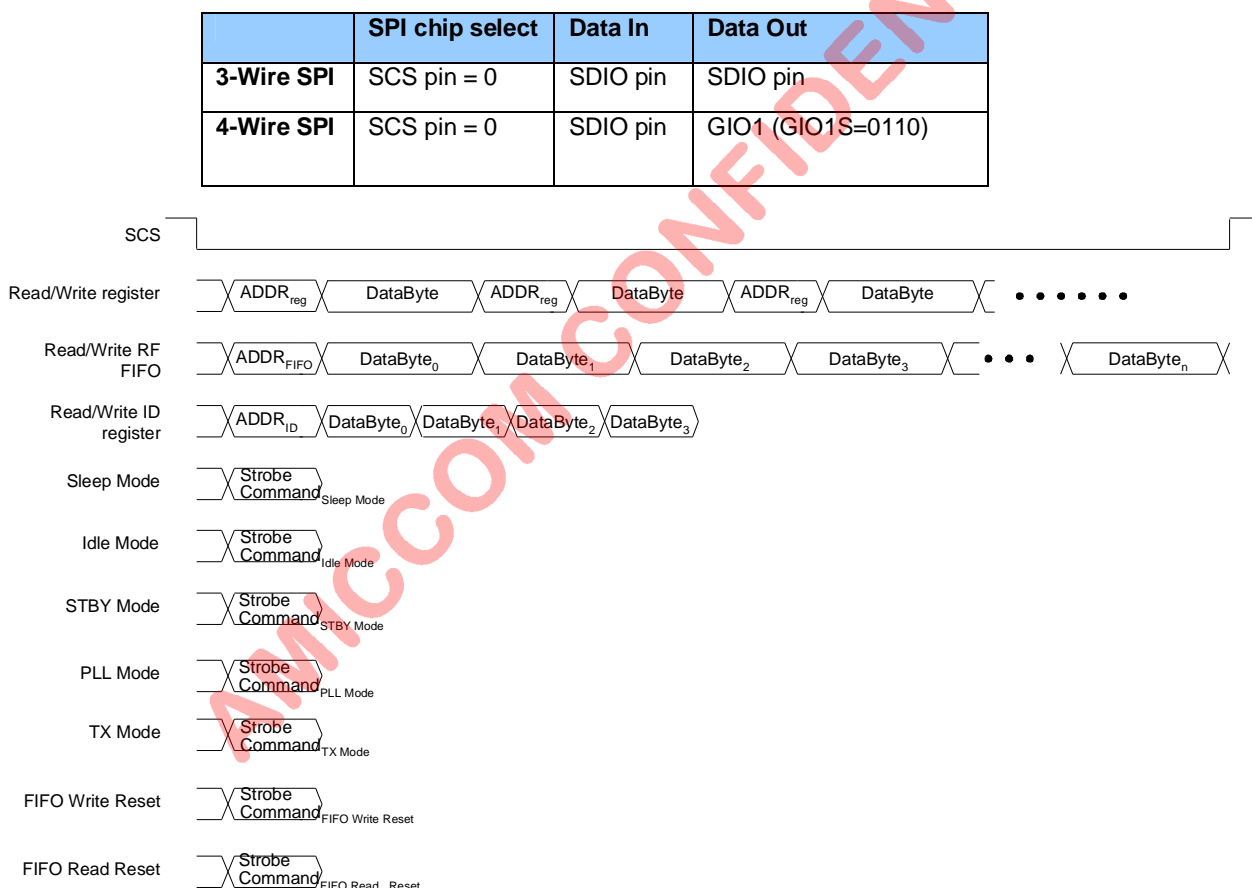


Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A7325 the following instruction is “Strobe command” or “control register”. See Table 10.1 for SPI format. Based on Table 10.1, To access control registers, just set A7=0, then A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 (3-wire SPI) and Figure 10.3 (4-wire SPI) for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

A7: Command bit

[0]: Control registers.

[1]: Strobe command.

A6: R/W bit

[0]: Write data to control register.

[1]: Read data from control register.

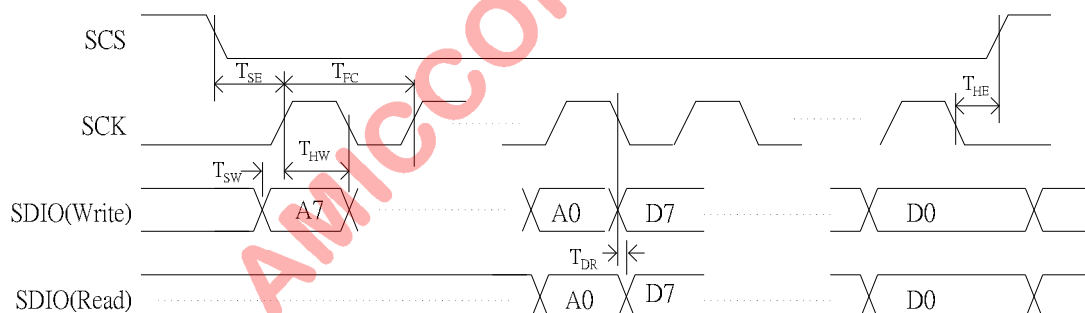
Bit [5:0]: Address of control register

Data Byte:

Bit [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI interface is configured, the maximum SPI data rate is 10 Mbps. To active SPI interface, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for SPI timing characteristic.



Parameter	Description	Min.	Max.	Unit
F _C	FIFO clock frequency.		10	MHz
T _{SE}	Enable setup time.	50		ns
T _{HE}	Enable hold time.	50		ns
T _{SW}	TX Data setup time.	50		ns
T _{HW}	TX Data hold time.	50		ns
T _{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI interface read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

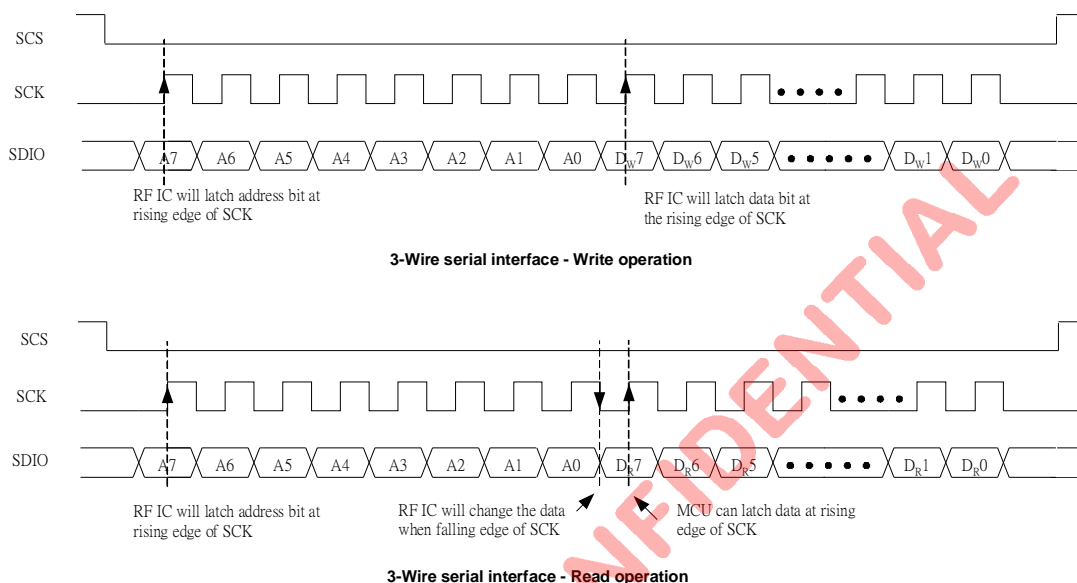


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI

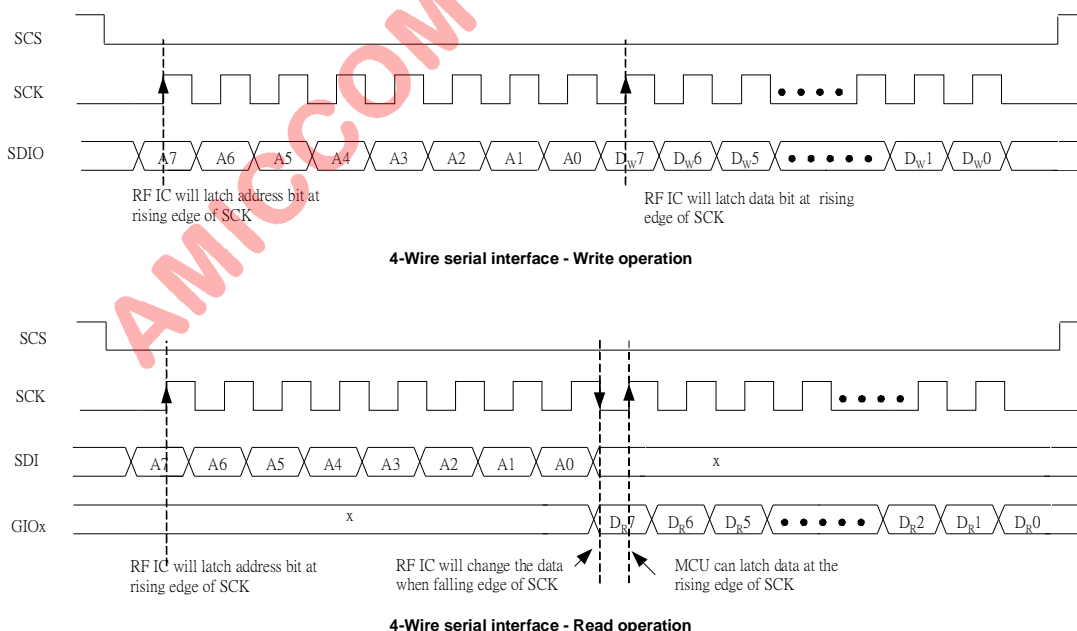


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A7325 supports 8 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	X	x	x	Sleep mode
1	0	0	1	x	X	x	x	Idle mode
1	0	1	0	x	X	x	x	Standby mode
1	0	1	1	x	X	x	x	PLL mode
1	1	0	1	x	X	x	x	TX mode
1	1	1	0	x	X	x	x	FIFO write pointer reset
1	1	1	1	x	X	x	x	FIFO read pointer reset

Table 10.3 Strobe Commands by SPI interface

10.4.1 Strobe Command - Sleep Mode

Refer to Table 10.3 user can issue 4 bits (1000) Strobe command directly to set A7325 into Sleep mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode

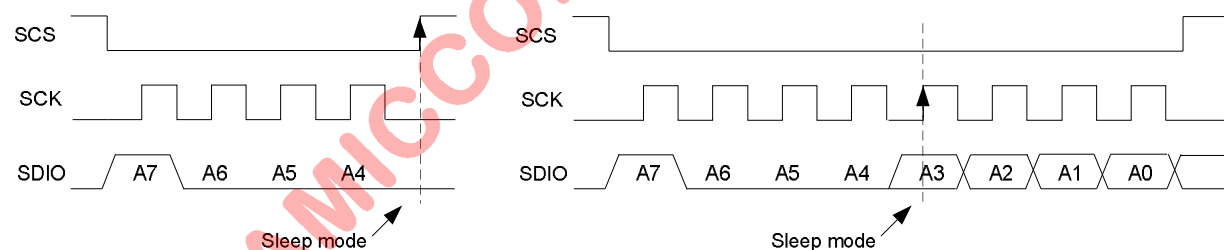


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe command directly to set A7325 into Idle mode. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	X	x	x	Idle mode

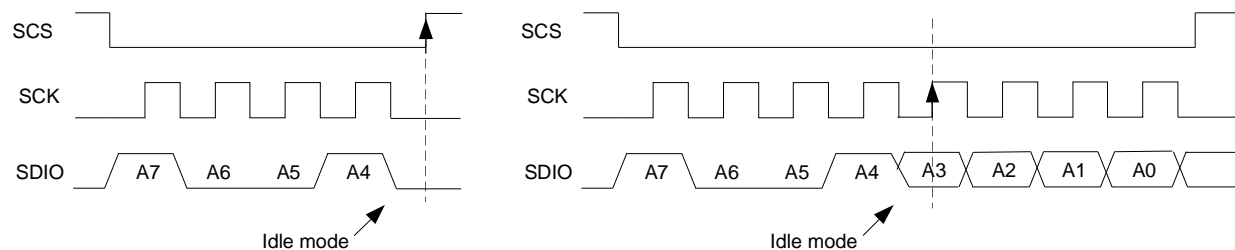


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe command directly to set A7325 into Standby mode. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	X	x	x	Standby mode

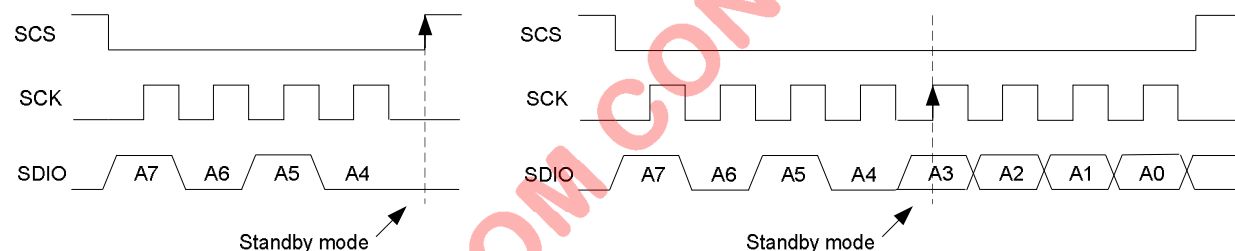


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe command directly to set A7325 into PLL mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	X	x	x	PLL mode

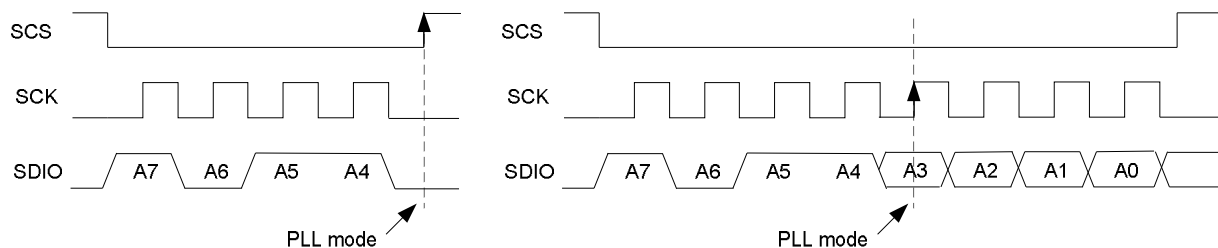


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe command directly to set A7325 into TX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

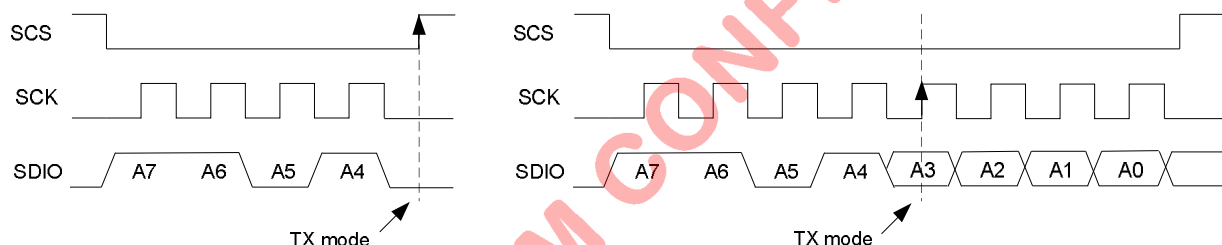


Figure 10.8 TX mode Command Timing Chart

10.4.6 Strobe Command – FIFO Write Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1110) Strobe command directly to reset A7325 FIFO write pointer. Below is the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	FIFO write pointer reset

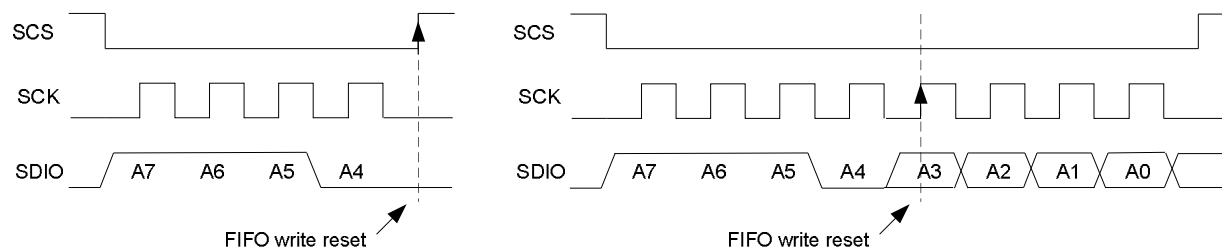


Figure 10.9 FIFO write pointer reset Command Timing Chart

10.4.7 Strobe Command – FIFO Read Pointer Reset

Refer to Table 10.3, user can issue 4 bits (1111) Strobe command directly to reset A7325 FIFO read pointer. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	1	x	x	x	x	FIFO read pointer reset

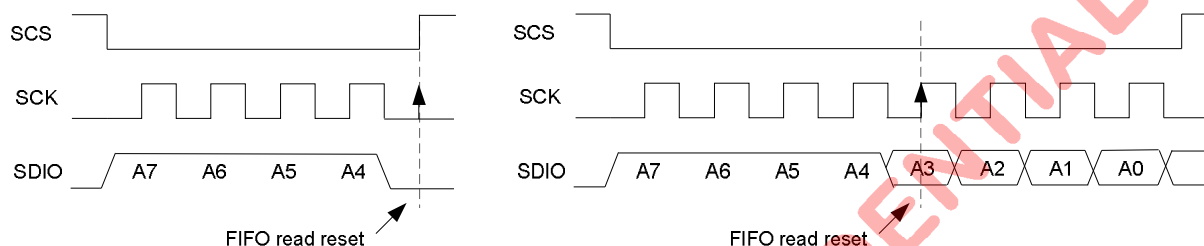


Figure 10.10 FIFO read pointer reset Command Timing Chart

10.4.8 Strobe Command – Deep Sleep Mode

Refer to Table 10.3, user can issue 8 bits (1000-0000) Strobe command directly to switch off power supply to A7128. In this mode, A7128 is staying minimum current consumption and all registers are no data retention. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	0	0	Tri-state of GIO1 (no data retention)
1	0	0	0	1	0	1	1	Internal Pull-High of GIO1 (no data retention)

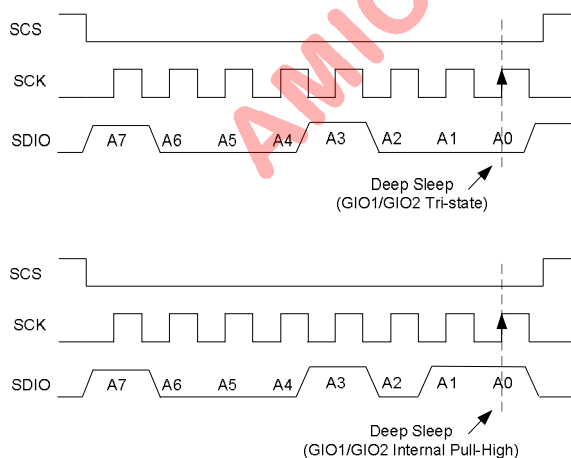


Figure 10.11 Deep Sleep Mode Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A7325 by setting Mode Register (00h) through SPI interface as shown below. As long as 8-bits address (A7~A0) are delivered zero and data (D7~D0) are delivered zero, A7325 is informed to generate internal signal "RESETN" to initial itself. After reset command, A7325 is in standby mode and calibration procedure shall be issued again.

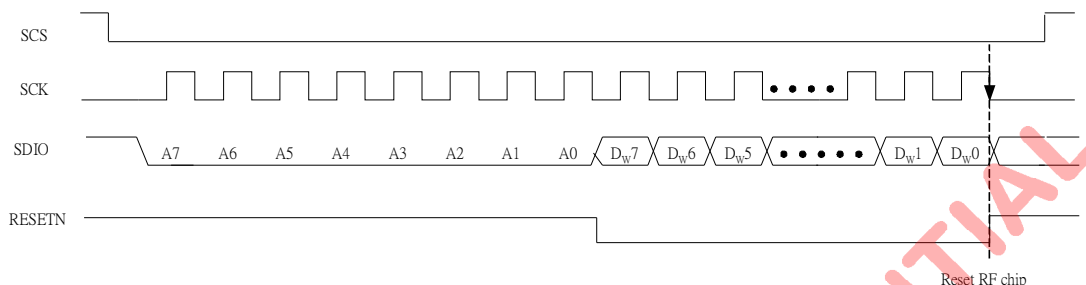


Figure 10.11 Reset Command Timing Chart

10.6 ID Accessing Command

A7325 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI interface. ID length is recommended to be 32 bits by setting IDL (1Ah). Therefore, user can toggle SCS pin to high to terminate ID accessing command when ID data is output completely.

Figure 10.13 and 10.14 are timing charts of 32-bits ID accessing via 3-wire SPI.

10.6.1 ID Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of ID write command.

- Step1: Deliver A7~A0 = 00000110 (A6=0 for write, A5~A0 = 000110 for ID addr, 06h).
- Step2: By SDIO pin, deliver 32-bits ID into A7325 in sequence by Data Byte 0 (**recommend 5xh or Axh**), 1, 2 and 3.
- Step3: Toggle SCS pin to high when step2 is completed.

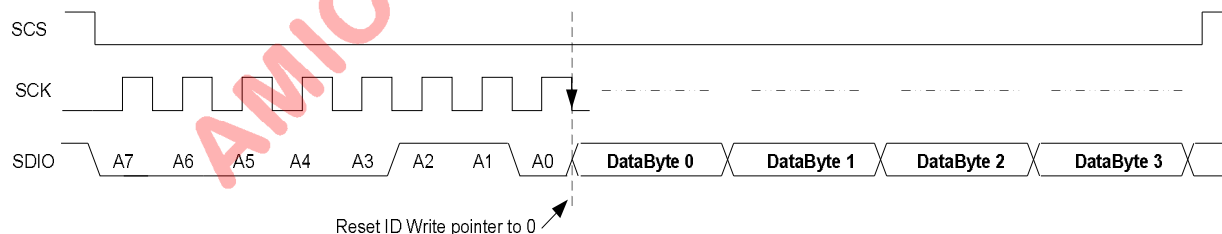


Figure 10.12 ID Write Command Timing Chart

10.6.2 ID Read Command

User can refer to Figure 10.2 for SPI read timing chart in details. Below is the procedure of ID read command.

- Step1: Deliver A7~A0 = 01000110 (A6=1 for read, A5~A0 = 000110 for ID addr, 06h).
- Step2: SDIO pin outputs 32-bits ID in sequence by Data Byte 0, 1, 2 and 3.
- Step3: Toggle SCS pin to high when step2 is completed.

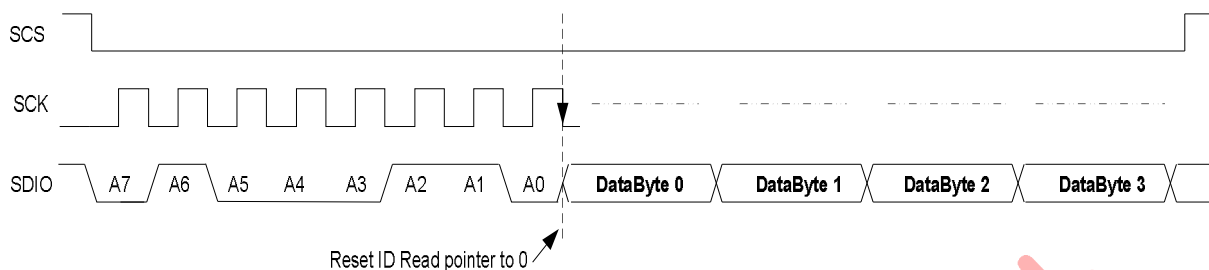


Figure 10.13 ID Read Command Timing Chart

10.7 FIFO Accessing Command

To use A7325's FIFO mode, enable FMS (01h) = 1 via SPI interface. Before TX delivery, just write wanted data into TX FIFO (05h) then issue TX Strobe command.

MCU can use polling or interrupt scheme to do FIFO accessing. FIFO status can output to GIO1 pin by setting GIO1S.

Figure 10.15 and 10.16 are timing charts of FIFO accessing via 3-wire SPI.

10.7.1 TX FIFO Write Command

User can refer to Figure 10.2 for SPI write timing chart in details. Below is the procedure of TX FIFO write command.

- Step1: Deliver A7~A0 = 00000101 (A6=0 for write control register and issue FIFO A [5:0] = 05h).
- Step2: By SDIO pin, deliver (n+1) bytes TX data into TX FIFO in sequence by Data Byte 0, 1, 2 to n.
- Step3: Toggle SCS pin to high when step2 is completed.
- Step4: Send Strobe command of TX mode (Figure 10.9) to do TX delivery.

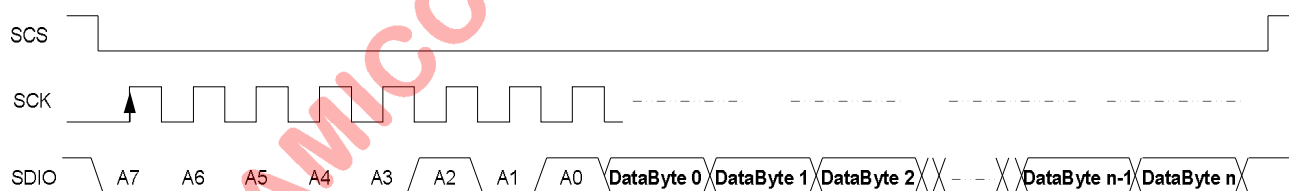


Figure 10.14 TX FIFO Write Command Timing Chart

11. State machine

In chapter 9 and chapter 10, user can not only learn A7325's control registers but also know how to issue Strobe command. From section 10.2 ~ 10.6, it is clear to know configurations of 3-wire SPI and 4-wire SPI, Strobe command, software reset, and how to access ID Registers as well as TX FIFO.

Section 11.1 introduces 6 states of built-in state machine. Combined with Strobe command and accessing control registers, section 11.2, 11.3 and 11.4 demonstrate 3 state diagrams to explain how transitions of A7325's operation.

From accessing data point of view, if FMS=1 (01h), FIFO mode is enabled, otherwise, A7325 is in direct mode. If FMS=1 and FIFO Read/Write in Standby mode, we call it Normal FIFO mode. Otherwise, If FMS=1 and FIFO Read/Write in PLL mode, we called it Quick FIFO mode due to the time reduction of PLL settling. If FMS=1 and FIFO Read/Write in IDLE mode, we called it Power Saving FIFO mode due to the reduction of average current.

	SPI chip select	Data In	Data Out	Operation Mode	Clock Recovery for Direct Mode
3-Wire SPI	SCS pin = 0	SDIO pin	SDIO pin	FIFO (FMS=1) Direct (FMS=0)	CKO pin (CKOS = 0001)
4-Wire SPI	SCS pin = 0	SDIO pin	GIO1 (GIO1S=0110)	FIFO (FMS=1) Direct (FMS=0)	CKO pin (CKOS = 0001)

- (1) Normal FIFO Mode (FMS=1 and FIFO R/W @ Standby mode)
- (2) Quick FIFO Mode (FMS=1 and FIFO R/W @ PLL mode)
- (3) Power Saving FIFO Mode (FMS=1 and FIFO R/W @ IDLE mode)
- (4) Quick Direct Mode (FMS=0 and FIFO ignored, write packet @ TX mode)

11.1 Key states

A7325 supports 6 key operation states. Those are,

- (1) Standby mode
- (2) Sleep mode
- (3) Idle mode
- (4) PLL mode
- (5) TX mode
- (6) CAL mode

After power on reset or software reset, A7325 is in standby mode. User has to do calibration process because all control registers are in initial values. The calibration process is very easy, user only needs to issue Strobe commands and enable calibration registers. Then, check the calibration flag because it is done automatic by internal state machine. Refer to 11.2, 11.3, 11.4 and chapter 15 for details. After calibration, A7325 is ready to do TX and RX operation.

11.1.1 Standby mode

If Standby Strobe command is issued, A7325 enters standby mode automatically. Internal power management is listed below. Be notice, A7325 is in standby mode once power on reset or software reset occurs.

Standby mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	OFF	OFF	OFF	OFF	1010xxxxb See Figure 10.6

11.1.2 Sleep mode

If Sleep Strobe command is issued, A7325 enters sleep mode automatically. In sleep mode, A7325 still can accept MCU's commands via SPI interface. But, NOT support to Read/Write FIFO. Internal power management is listed below.

Sleep mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
OFF	OFF	OFF	OFF	OFF	OFF	1000xxxxb See Figure 10.4

11.1.3 Idle mode

If Idle Strobe command is issued, A7325 enters idle mode automatically. In idle mode, A7325 can accept MCU's commands via SPI interface as well as supporting Read/Write FIFO. Internal power management is listed below.

Idle mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	OFF	OFF	OFF	OFF	OFF	1001xxxxb See Figure 10.5

11.1.4 PLL mode

If PLL Strobe command is issued, A7325 enters PLL mode automatically. In PLL mode, internal PLL and VCO are both turned on to generate LO (local oscillator) frequency before TX and RX operation. Internal power management is listed below. According to PLL Register I, II, III, IV and V, PLL circuitry is easy to be controlled by user's definition.

PLL mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	OFF	1011xxxxb See Figure 10.7

11.1.5 TX mode

If TX Strobe command is issued, A7325 enters TX mode automatically for data delivery. Internal power management is listed below.

- (1) In FIFO mode, once TX data packet (Preamble + ID + Payload) is delivered, A7325 supports auto-back function to previous state for next delivered packet.
- (2) In Direct mode, once TX data packet is delivered, A7325 stays in TX mode. User has to issue Strobe command to back to previous state.

TX mode						Strobe Command
On Chip Regulator	Crystal Oscillator	VCO	PLL	RX Circuitry	TX Circuitry	
ON	ON	ON	ON	OFF	ON	(1101xxxx)b See Figure 10.9

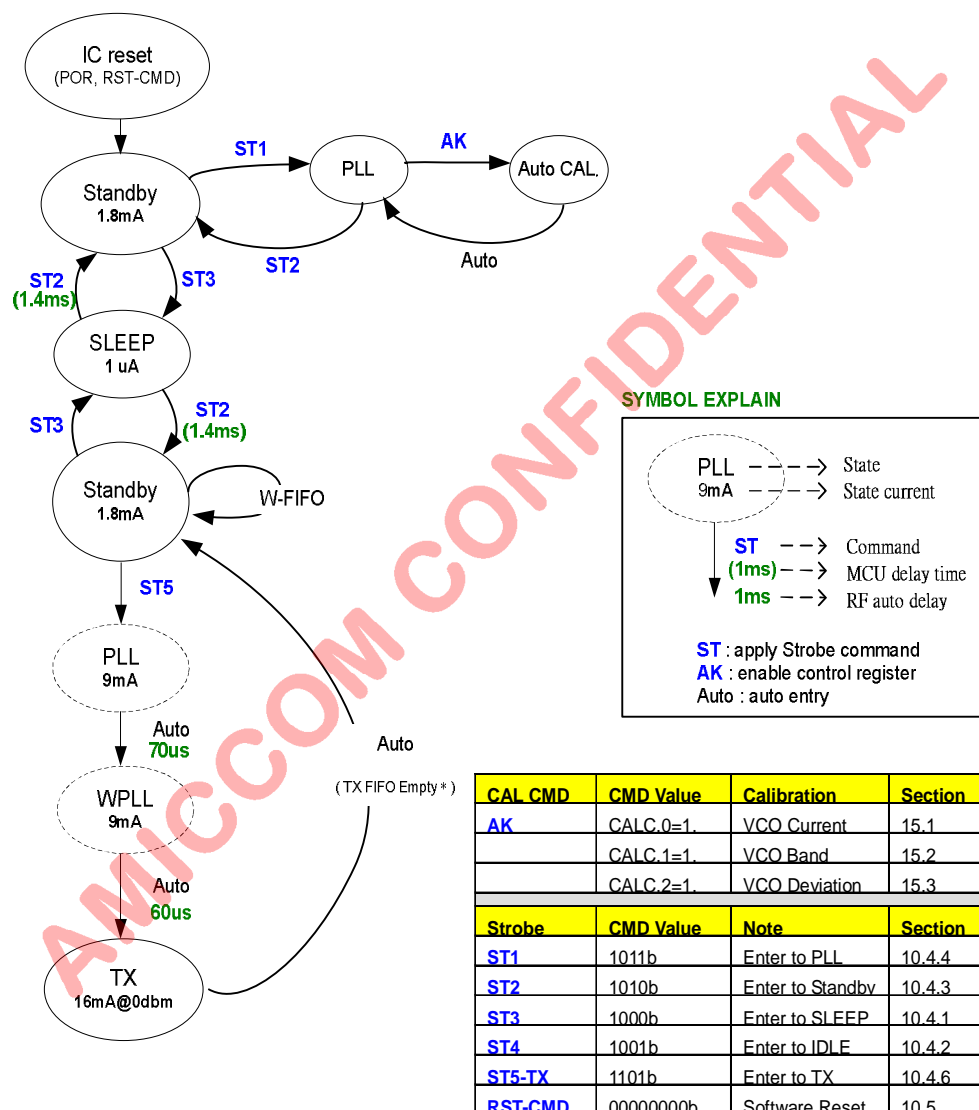
11.1.6 CAL mode

Calibration process shall be done after power on reset or software reset. Calibration items include VCO and IF Filter. It is easy to implement calibration process by Strobe command and enable CALC (02h) control register. See chapter 15 for details.

Be notice, VCO Calibration is only executable in PLL mode. However, IF Filter Calibration can be executed in Standby or PLL mode.

11.2 Normal FIFO Mode

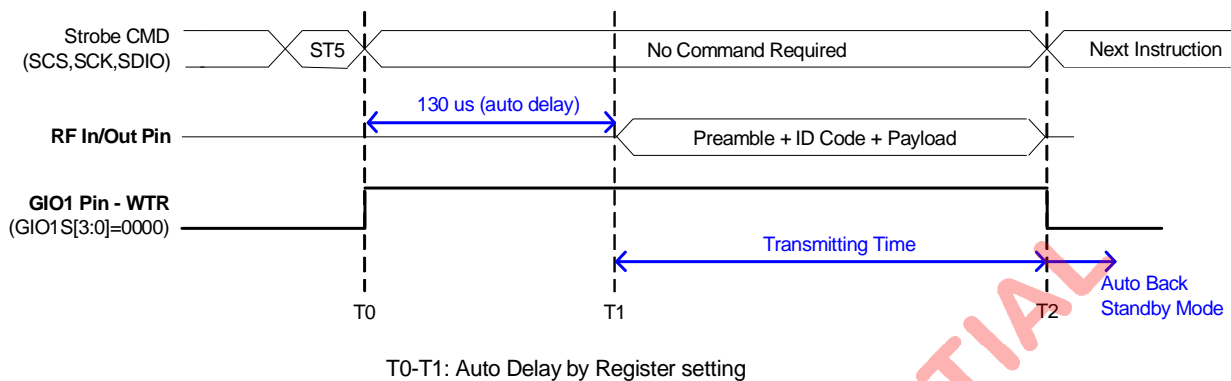
This mode is suitable for requirement of general purpose applications. After calibration flow, user can issue Strobe command to enter standby mode where write TX FIFO. From standby mode to packet transmission, only one Strobe command is needed. Once transmitting is done, A7325 is auto back to standby mode. If all packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7325 staying in sleep mode (all registers are data retention, but, A7325 does NOT support read functionality in sleep mode.). Figure 11.1 is the state diagram of Normal FIFO mode.



- Refer to chapter 16 for definition of TX FIFO Empty.

Figure 11.1 State diagram of Normal FIFO Mode

From Figure 11.1, when ST5 command is issued for TX operation, see Figure 11.2 for detailed timing. A7325 status can be represented to GIO1 pin to MCU for timing control.



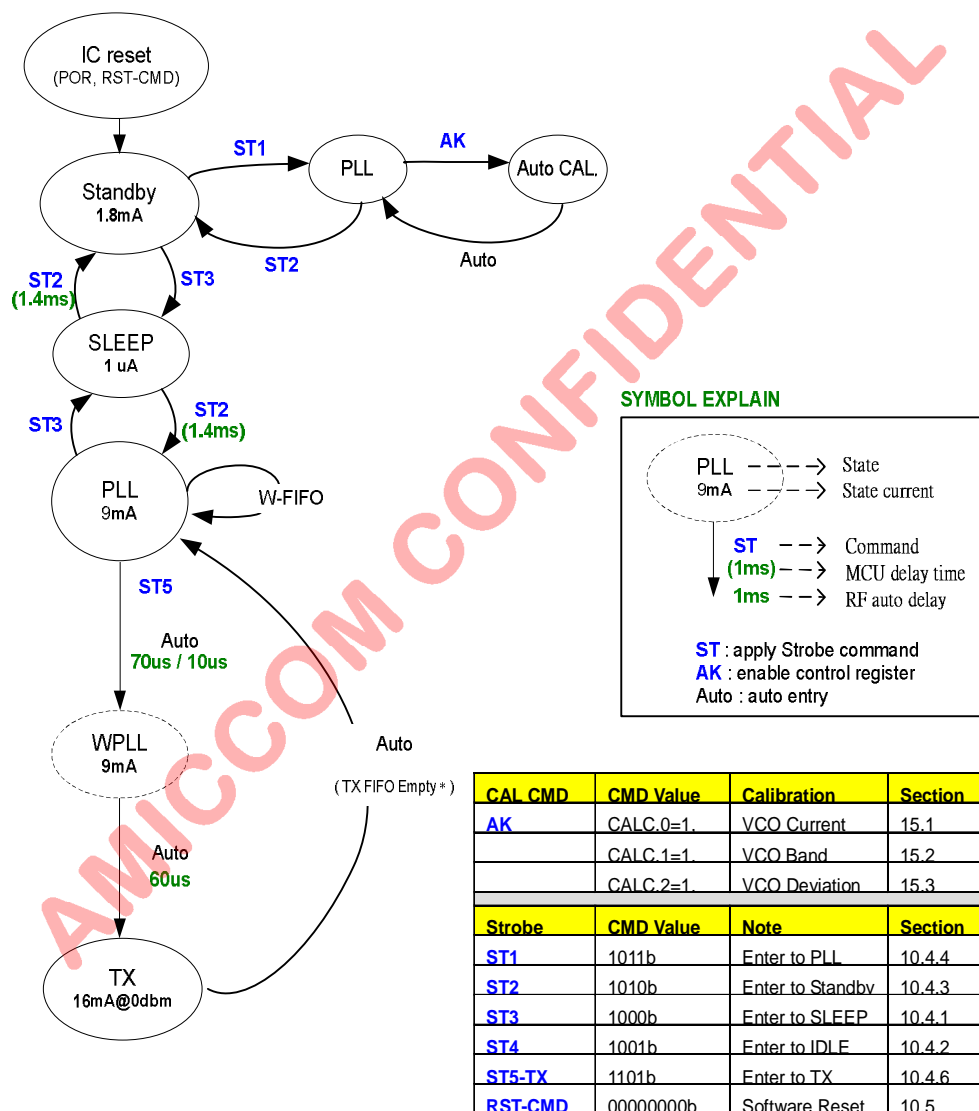
LO Freq.	Standby to WPLL	WPLL to TX	TX Ready Time
Changed	70 us	60 us	130 us
No Changed	70 us	60 us	130 us

Figure 11.2 Transmitting Timing Chart of Normal FIFO Mode

11.3 Quick FIFO Mode

This mode is suitable for requirement of fast transmitting. After calibration flow, user can issue Strobe command to enter PLL mode where write TX FIFO. From PLL mode to packet data transmitting, only one Strobe command is needed. Once transmitting is finished, A7325 is auto back to PLL mode.

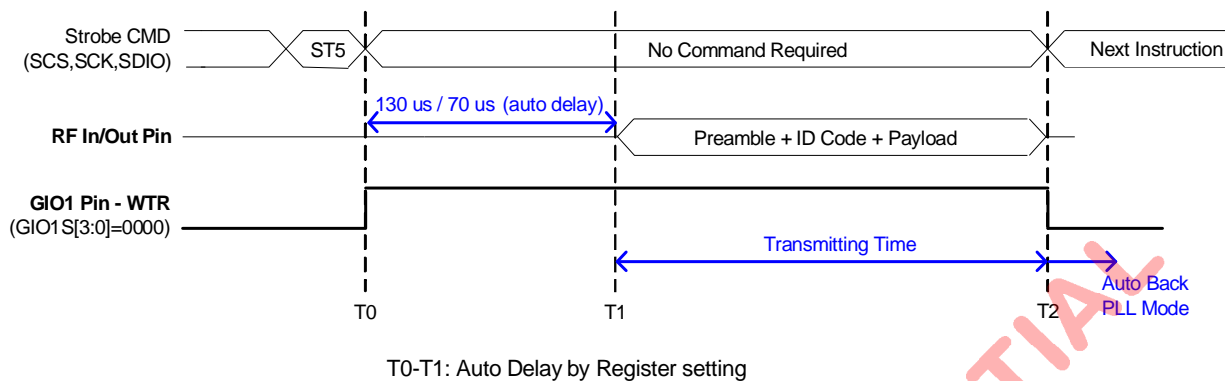
When packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7325 staying in sleep mode (all registers are data retention, but, A7325 does NOT support read functionality in sleep mode.). Figure 11.4 is the state diagram of Quick FIFO mode.



- Refer to chapter 16 for definition of TX FIFO Empty.
- From PLL to WPLL, it is either 70 us (LO frequency changed) or 10 us (LO frequency NOT changed)

Figure 11.4 State diagram of Quick FIFO Mode

From Figure 11.4, when ST5 command is issued for TX operation, see Figure 11.5 for detailed timing. A7325 status can be represented to GIO1 pin to MCU for timing control.



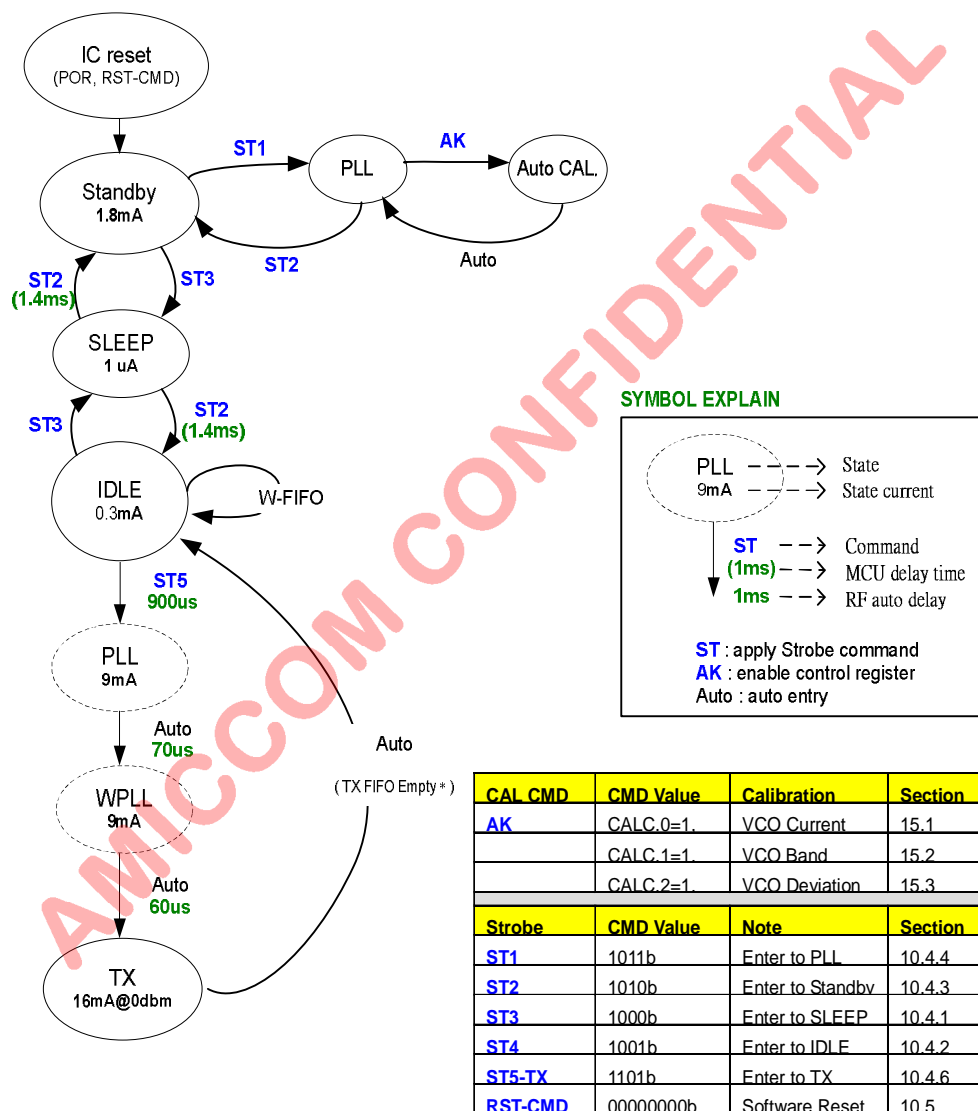
LO Freq.	PLL to WPLL	WPLL to TX	TX Ready Time
Changed	70 us	60 us	130 us
No Changed	10 us	60 us	70 us

Figure 11.5 Transmitting Timing Chart of Quick FIFO Mode

11.4 Power Saving FIFO Mode

This mode is suitable for requirement of low power consumption. After calibration flow, user can issue Strobe command to enter idle mode where write TX FIFO. From idle mode to packet data transmitting, only one Strobe command is needed. Once transmitting is done, A7325 is auto back to idle mode.

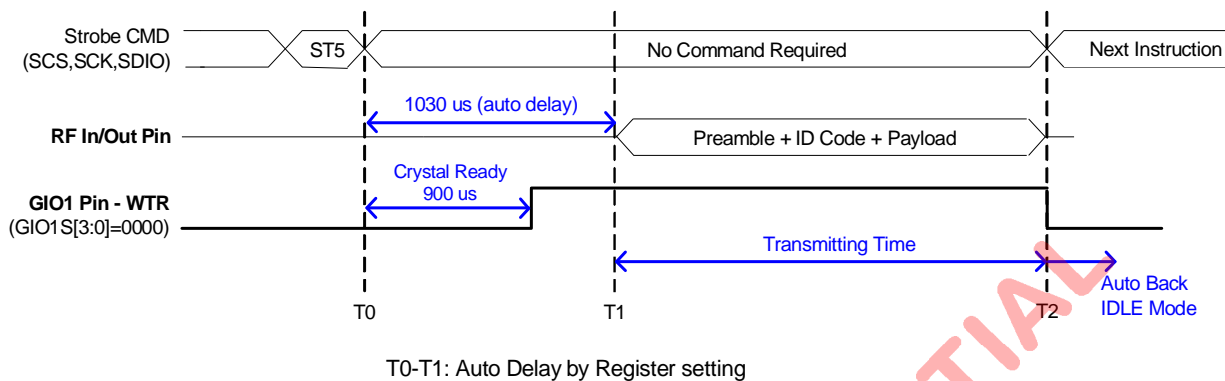
When packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7325 staying in sleep mode (all registers are data retention, but, A7325 does NOT support read functionality in sleep mode.). Figure 11.7 is the state diagram of Power Saving FIFO mode.



- Refer to chapter 16 for definition of TX FIFO Empty.

Figure 11.7 State diagram of Power Saving FIFO Mode

From Figure 11.7, when ST5 command is issued for TX operation, see Figure 11.8 for detailed timing. A7325 status can be represented to GIO1 pin to MCU for timing control.



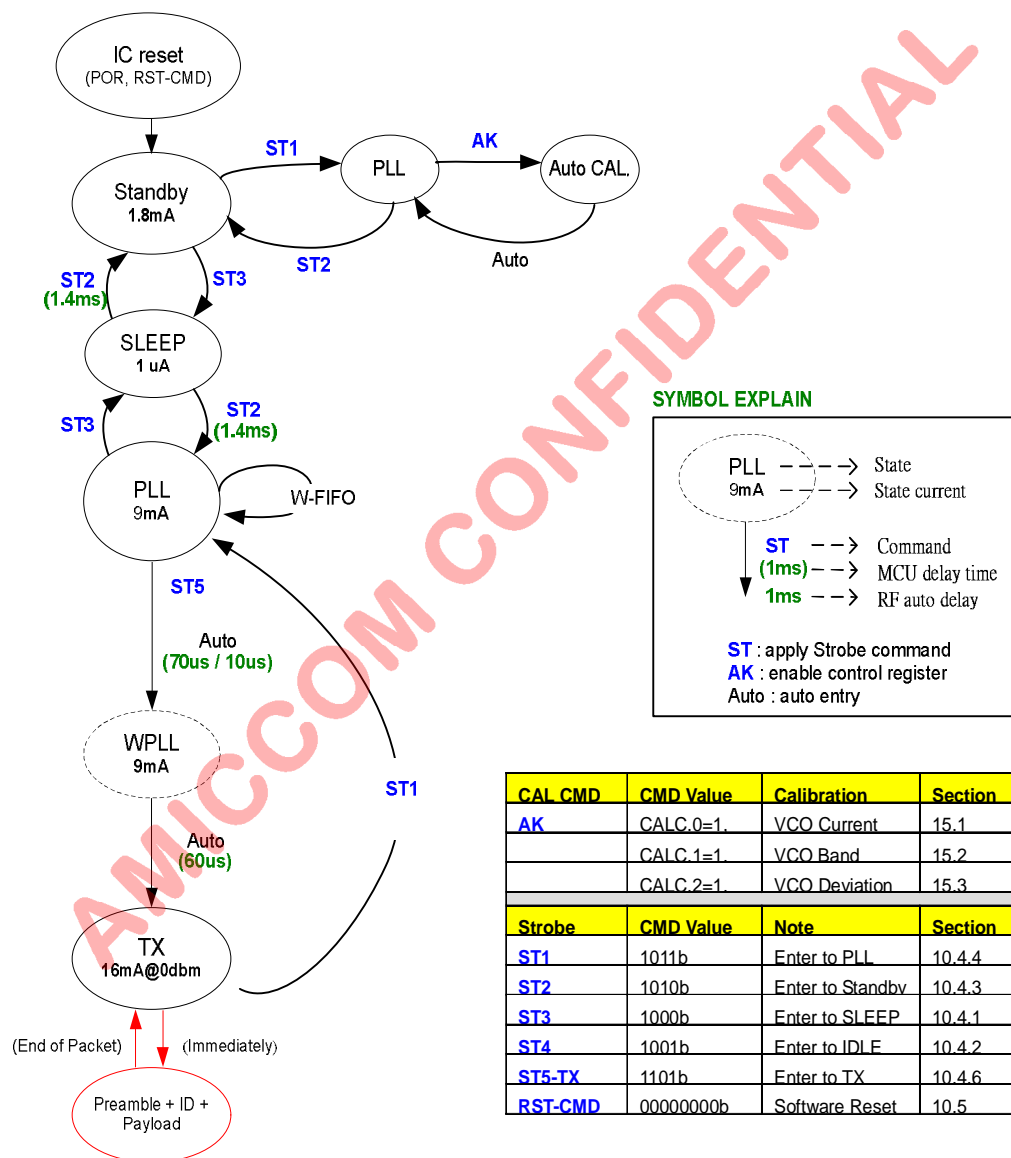
LO Freq.	IDLE to WPLL	WPLL to TX	TX Ready Time
Changed	970 us	60 us	1030 us
No Changed	970 us	60 us	1030 us

Figure 11.8 Transmitting Timing Chart of Power Saving FIFO Mode

11.5 Quick Direct Mode

This mode is suitable for fast transmitting. After calibration flow, for every state transition, user has to issue Strobe command to A7325. This mode is also suitable for the requirement of versatile packet format. Noted that user needs to take care the transition time by MCU's timer.

When packets are finished and deeper power saving is necessary, user can issue Strobe command to ask A7325 staying in idle mode (or sleep mode, all registers are data retention, but, A7325 does NOT support read functionality.). Figure 11.3 is the state diagram of Quick Direct mode.



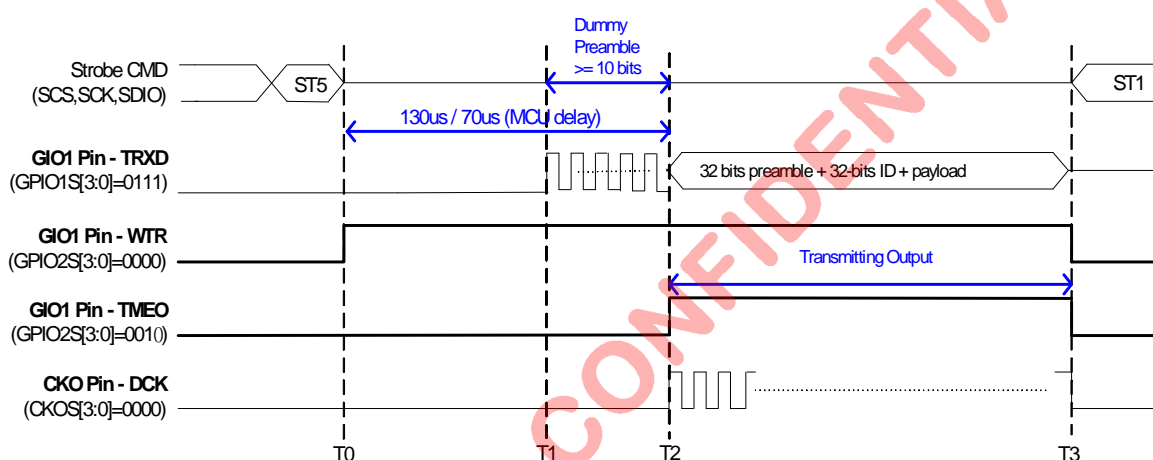
- From PLL to WPLL, it is either 70 us (LO frequency changed) or 10 us (LO frequency NOT changed)

Figure 11.10 State diagram of Quick Direct Mode

From Figure 11.10, After A7325 enters TX mode, MCU should immediately deliver preamble. Therefore, user can send dummy preamble since WTR goes high or plus a delay loop to make sure dummy preamble is 10 bits at least before DCK is active. See below figure for detail timing.

A7325 Data Rate	Dummy Preamble	Packet			Note
		Preamble	ID (06h)	Max Payload	
2K~2Mbps	≥ 10 bits	32 bits	32 bits	512 bytes	Total Preamble = 42 bits

Table 11.2 Format of dummy preamble and packet.



T0-T1: MCU delay loop
T1-T2: Dummy Preamble.
T2: TMEO (TX Modulation Enable) is auto triggered
T2-T3: Transmitting Time

LO Freq.	PLL to WPLL	WPLL to TX	TX Ready Time
Changed	70 us	60 us	130 us
No Changed	10 us	60 us	70 us

Figure 11.11 Transmitting Timing Chart of Quick Direct Mode

12 Crystal Oscillator

A7325 needs external crystal or external clock that is either 8 or 12/16/20/24 MHz to generate internal wanted clock.

Relative Control Register

Clock Register (Address: 0Ch)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Clock	RW	IFS	CSC	GRC3	GRC2	GRC1	GRC0	CGS	XS
Reset		0	1	0	1	1	1	1	1

12.1 Use External Crystal

Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 are built inside A7325. Also, C1 and uC2 are programmable to support different crystal loading. It is ok to use crystal accuracy within ± 50 ppm. Be noted that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

A7325	Crystal Accuracy	Crystal ESR
	± 50 ppm	≤ 80 ohm

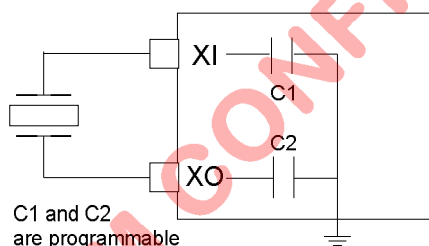


Fig12.1 Crystal oscillator circuit.

12.2 Use external clock

A7325 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. In such case, XI pin is left opened. XS shall be low (0Dh) for selecting external clock. The frequency accuracy of external clock shall be controlled within ± 20 ppm, and the amplitude of external clock shall be within 1.2 ~ 1.8 V peak-to-peak.

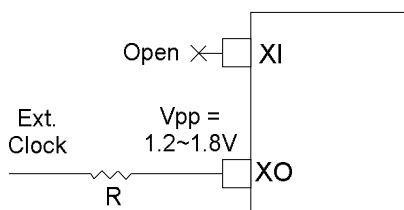


Fig12.2 External clock source. R is used to tune $V_{pp} = 1.2 \sim 1.8V$

13. System Clock

A7325 supports different crystal frequency by programmable "Clock Register" (0Ch). Based on this, three important internal clocks F_{CGR} , F_{DR} and F_{SYCK} are generated.

- (1) F_{XTAL} : Crystal frequency.
- (2) F_{XREF} : Crystal Ref. Clock = $F_{XREF} * (DBL+1)$.
- (3) F_{CGR} : Clock Generation Reference = 2MHz = $F_{XREF} / (GRC+1)$, where F_{CGR} is used to generate 32M PLL.
- (4) F_{MCLK} : Master Clock is either F_{XREF} or 32M PLL, where F_{MCLK} is used to generate F_{SYCK} .
- (5) F_{SYCK} : System Clock = $F_{MCLK} / CSC = 32 * F_{IF}$, where F_{IF} is IF frequency.
- (6) F_{DR} : Data Rate Clock = $F_{IF} / (SDR+1)$.
- (7) F_{PPD} : VCO Compared Clock = $F_{XREF} / (RRC+1)$.

For application using A7325, user should keep in mind that the IF center frequency must be larger than data rate used and the system clock is 32 times of IF center frequency. The relationship of crystal frequency, system clock and data rate is shown below.

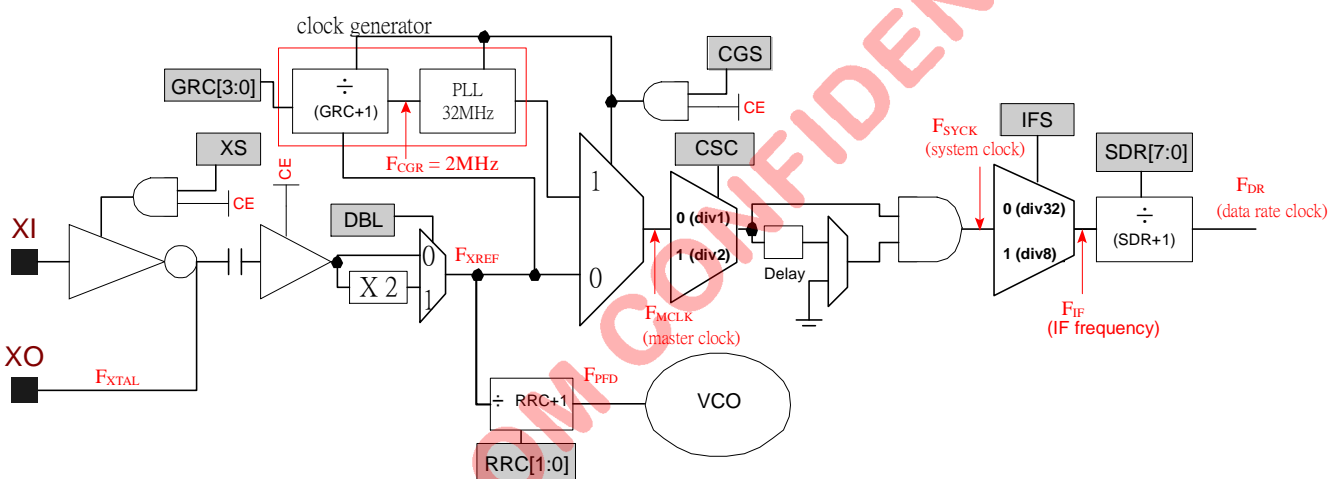


Fig13.1 System clock block diagram

As show in Fig 13.1, F_{MCLK} , the master clock either come from F_{XREF} ($CGR = 0$) or PLL 32MHz ($CGR = 1$). The relation between F_{SYCK} (the system clock) and F_{MCLK} (master clock) show in table 13.1

F_{SYCK} (Master Clock)		
DBL	$CGR=0$	$CGR=1$
0	F_{XTAL}	32MHz
1	$2 * F_{XTAL2}$ (recommend)	32MHz

CSC	F_{SYCK} (system clock)	Note
0	F_{MCLK}	F_{SYCK} is used to determine 1. Data rate register (0Dh) 2. ADC clock (19h) 3. Internal digital clock (09h) 4. CKO pin (0Ah)
1	$F_{MCLK} / 2$	

Table 13.1 System clock and master clock

13.1 Bypass clock generation

If crystal frequency is 16MHz, the clock generator block can be turned off by setting CGS = 0. The relation between F_{XTAL} (crystal frequency) and data rate show below:

$$F_{XREF} = F_{XTAL} * (DBL+1)$$

$$F_{PFD} = F_{XREF} / (RRC[1:0]+1)$$

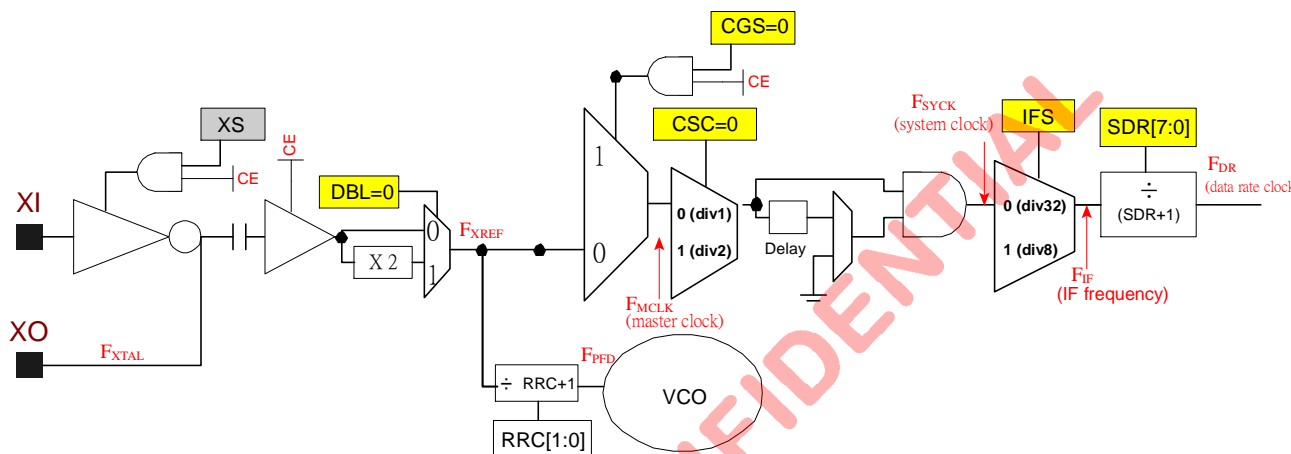


Fig13.2 By pass clock generator to get system clock for 16MHz Xtal.

For various data rate application, list some examples below.
For more data rate options, please contact AMICCOM FAE team.

Data rate 2Mbps

Crystal source	CGS (0Ch)	DBL (0Fh)	CSC[1:0] (0Ch)	IFS (0Ch)	GRC [3:0] (0Ch)	RRC [1:0] (0Fh)	F _{PFD} (MHz)	CHR [3:0] (0Fh)	F _{CHSP} (MHz)	SDR [7:0] (0Dh)
16MHz	0	0	0	1	Don't care	00	16	0111	0.5	0x00

Data rate 1Mbps

Crystal source	CGS (0Ch)	DBL (0Fh)	CSC[1:0] (0Ch)	IFS (0Ch)	GRC [3:0] (0Ch)	RRC [1:0] (0Fh)	F _{PFD} (MHz)	CHR [3:0] (0Fh)	F _{CHSP} (MHz)	SDR [7:0] (0Dh)
16MHz	0	0	0	1	Don't care	00	16	0111	0.5	0x01

Data rate = 500Kbps / 250K / 125K / 100K / 50K / 25K / 10K / 2Kbps

Crystal source	CGS (0Ch)	DBL (0Fh)	CSC[1:0] (0Ch)	IFS (0Ch)	GRC [3:0] (0Ch)	RRC [1:0] (0Fh)	F _{PFD} (MHz)	CHR [3:0] (0Fh)	F _{CHSP} (MHz)	SDR [7:0] (0Dh)
16MHz	0	0	0	1	Don't care	00	16	0111	0.5	See SDR table

SDR Table

	500Kbps	250Kbps	125Kbps	100Kbps	50Kbps	25Kbps	10Kbps	2Kbps
SDR [7:0]	0x00	0x01	0x03	0x04	0x09	0x13	0x31	0xF9

13.2 Enable clock generation

If crystal frequency is the multiplier of 2MHz and larger than 6MHz, set CGS = 1 to enable $F_{SYCK} = 32\text{MHz}$ (internal 32MHz PLL). The comparison frequency of clock generator F_{CGR} shall be 2MHz by setting GRC[3:0] to meets the below equations.

$$F_{CRG} = F_{XTAL} * (1 + DBL) / (GRC + 1) = 2\text{MHz.}$$

$$F_{DR} = F_{SYCK} / 32 / (SDR + 1).$$

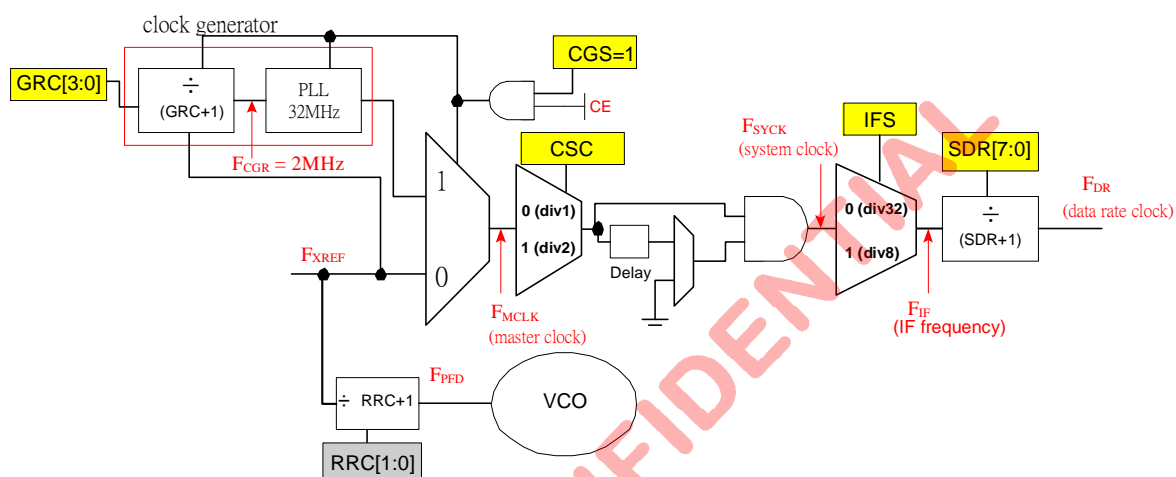


Fig13.3 Enable clock generator to get system clock

For various data rate application, list some examples below. For more options, please contact AMICCOM FAE team.

Data rate 2Mbps

Crystal source	CGS (0Ch)	DBL (0Fh)	CSC (0Ch)	GRC [3:0] (0Ch)	F _{IF} (MHz)	IFS (0Ch)	RRC [1:0] (0Fh)	F _{PFD} (MHz)	CHR [3:0] (0Fh)	F _{CHSP} (MHz)	SDR [7:0]
12MHz	1	0	1	0101	2	1	00	12	0101	0.5	0x00
16MHz		0	0	0111				16	0111		
24MHz		0	1	1011				24	1011		

Data rate 1Mbps

Crystal source	CGS (0Ch)	DBL (0Fh)	CSC (0Ch)	GRC [3:0] (0Ch)	F _{IF} (MHz)	IFS (0Ch)	RRC [1:0] (0Fh)	F _{PFD} (MHz)	CHR [3:0] (0Fh)	F _{CHSP} (MHz)	SDR [7:0]
12MHz	1	0	1	0101	2	1	00	12	0101	0.5	0x01
16MHz		0	0	0111				16	0111		
24MHz		0	1	1011				24	1011		

Data rate = 500K / 250K / 125K / 100K / 50K / 25K / 10K / 2Kbps

Crystal source	CGS (0Ch)	DBL (0Fh)	CSC (0Ch)	GRC [3:0] (0Ch)	F _{IF} (KHz)	IFS (0Ch)	RRC [1:0] (0Fh)	F _{PFD} (MHz)	CHR [3:0] (0Fh)	F _{CHSP} (MHz)	SDR [7:0]
12MHz	1	0	1	0101	500	0	00	12	0101	0.5	See SDR table
16MHz		0	0	0111				16	0111		
24MHz		0	1	1011				24	1011		

SDR Table

	500Kbps	250Kbps	125Kbps	100Kbps	50Kbps	25Kbps	10Kbps	2Kbps
SDR [7:0]	0x00	0x01	0x03	0x04	0x09	0x13	0x31	0xF9

14. Transceiver LO Frequency

For A7325 TX RF frequency setting, user just needs to set up LO (Local Oscillator) frequency for one ways radio transmission.

To target full range of 2.4GHz ISM band (2400 MHz to 2483.5 MHz), A7325 applies offset concept by LO frequency $F_{LO} = F_{LO_BASE} + F_{OFFSET}$. Therefore, this device is easy to implement frequency hopping and multi-channels by just **ONE** register setting, **PLL Register I (CHN [7:0], 0Eh)**.

Below is the LO frequency block diagram.

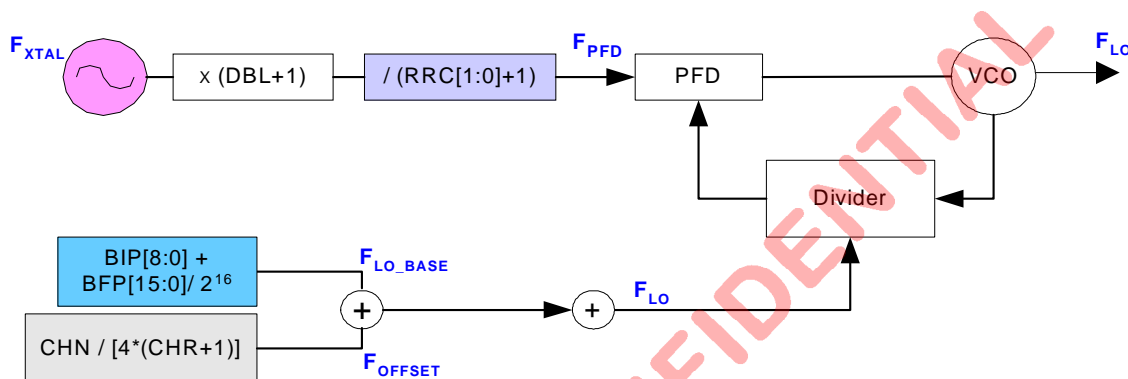


Fig14.1 Frequency synthesizer block diagram

Relative Control Register

PLL Register I (PLL1 at address 0Eh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL1I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	0	0	0	0	0	0	0

PLL Register II (PLL2 at address 0Fh)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL2I	W	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	BIP8
	R	DBL	RRC1	RRC0	CHR3	CHR2	CHR1	CHR0	IP8
Reset		0	0	1	0	1	1	1	0

PLL Register III (PLL3 at address: 10h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL III	W	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
	R	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		1	0	0	1	0	1	0	0

PLL Register IV (PLL4 at address 11h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL4	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	R	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
Reset		0	0	0	0	0	0	0	0

PLL Register V (PLL5 at address 12h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL V	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
	R	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset		0	0	0	0	0	1	0	0

14.1 LO Frequency Setting

From Figure 14.1, to set up F_{LO} , it is easy to implement by below 4 steps.

- Set the base frequency (F_{LO_BASE}) by PLL Register II, III, IV and V (0Fh, 11h, 11h and 12h).
Recommend to set $F_{LO_BASE} \sim 2400.001\text{MHz}$.
- Set the channel step (F_{CHSP}) by PLL Register II (0Fh).
 $F_{CHSP} = F_{XTAL} * (DBL+1) / 4 / (CHR+1)$, Recommend $F_{CHSP} = 500\text{ KHz}$.
- Set CHN [7:0] to get offset frequency by PLL Register I (0Fh).
 $F_{OFFSET} = CHN [7:0] * F_{CHSP}$
- LO frequency is equal to base frequency plus offset frequency.
 $F_{LO} = F_{LO_BASE} + F_{OFFSET}$



$$F_{LO_BASE} = F_{PFD} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}}) = (DBL+1) \cdot \frac{F_{XTAL}}{RRC[1:0]+1} \cdot (BIP[8:0] + \frac{BFP[15:0]}{2^{16}})$$

Base on the above formula, for example, if $F_{XTAL} = 16\text{ MHz}$ and set channel step $F_{CHSP} = 500\text{ KHz}$, to get F_{LO_BASE} and F_{LO} , see Table 14.1, 14.2, and Figure 14.2 for details.

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	DBL	0	Disable double function
3	RRC	0	If so, $F_{PFD} = 16\text{MHz}$
4	BIP	0x4B	To get $F_{LO_BASE} = 2400\text{ MHz}$
5	BFP	0x0002	To get $F_{LO_BASE} \sim 2400.001\text{ MHz}$
6	F_{LO_BASE}	$\sim 2400.001\text{ MHz}$	LO Base frequency

Table 14.1 How to set F_{LO_BASE}

How to set $F_{TXRF} = F_{LO} = F_{LO_BASE} + F_{OFFSET} \sim 2405.001\text{ MHz}$

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	$\sim 2400.001\text{ MHz}$	After set up BIP and BFP
2	CHR	0x07	To get $F_{CHSP} = 500\text{ KHz}$
3	F_{CHSP}	500 KHz	Channel step = 500KHz
4	CHN	0x0A	Set channel number = 10
5	F_{OFFSET}	5 MHz	$F_{OFFSET} = 500\text{ KHz} * (CHN) = 5\text{MHz}$
6	F_{LO}	$\sim 2405.001\text{ MHz}$	Get $F_{LO} = F_{LO_BASE} + F_{OFFSET}$
7	F_{TXRF}	$\sim 2405.001\text{ MHz}$	$F_{TXRF} = F_{LO}$

Table 14.2 How to set F_{TXRF}



2.4GHz FSK/GFSK RF Transmitter

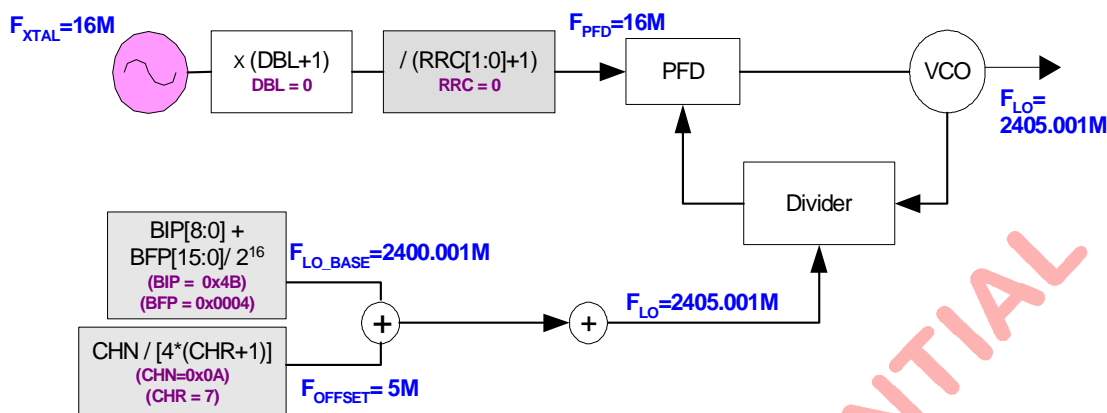


Figure 14.2 Block Diagram of set up $F_{LO} \sim 2405.001$ MHz

For different crystal frequency, 24MHz / 16MHz / 12 MHz / 8MHz, below are calculation details for F_{FPD} and F_{CHSP}

$$F_{\text{PFD}} = \frac{(DBL+1) \cdot f_{XTAL}}{RRC[1:0] + 1}$$

F _{XTAL} (MHz)	DBL	RRC	F _{PPD} (MHz)	Note
24	0	0	24	
16	0	0	16	(reference design)
12	0	0	12	

$$F_{CHSP} = \frac{F_{PFD}}{4 \cdot (CHR[3:0] + 1)}$$

F _{XTAL} (MHz)	F _{PFD} (MHz)	CHR [3:0]	F _{CHSP} (KHz)	CHN [7:0]	F _{OFFSET} (MHz)	F _{LO} (MHz)
24	24	1011	500	0x00 ~ 0xA8	0 ~ 84	2400 ~ 2484
16	16	0111	500	0x00 ~ 0xA8	0 ~ 84	2400 ~ 2484
12	12	0101	500	0x00 ~ 0xA8	0 ~ 84	2400 ~ 2484

15. Calibration

A7325 needs calibration process during initialization by below 3 items, they are, VCO Current, VCO Bank, and VCO Deviation Calibration.

1. VCO Current Calibration is to find adequate VCO current.
2. VCO Bank Calibration is to select best VCO frequency bank for the calibrated frequency.
3. VCO Deviation Calibration is to calibrate 500 KHz deviation of VCO.

Be notice that VCO Current, Bank and Deviation shall be calibrated in PLL mode. After calibration, its results are stored in calibration flags.

15.1 Calibration Procedure

1. Initialize all control registers (refer to A7325 reference code).
2. Set A7325 in PLL mode.
3. Set VCC=1, VBC =1, VDC = 1.
4. After calibration done, VCC, VBC and VDC are auto clear.
5. Check pass or fail by reading calibration flag. (VCCF and VBCF).

Relative Control Register

Calibration Control Register (CALC at address 02h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control II	W/R	--	--	--	VCC	VBC	VDC	--	--
Reset		--	--	--	0	0	0	--	--

15.2 VCO current Calibration Process

Set MVCS=0(auto calibration) and VCC=1, A7325 will enter CAL state. Once the calibration is completed, VCC will be auto clear. The max calibration time is about 80 * (1 / system clock).

15.3 VCO band Calibration Process

Set MVBS=0(auto calibration) and VBC=1, A7325 will enter CAL state. Once the calibration is completed, VBC will be auto clear. The max calibration time is about 4 * PLL settling time.

15.4 VCO deviation Calibration Process

Set MVDS=0(auto calibration) and VDC=1, A7325 will enter CAL state. Once the calibration is completed, VDC will be auto clear.

16. FIFO (First In First Out)

A7325 supports separated 64-bytes TX FIFO by enabling FMS =1 (01h). For FIFO accessing, TX FIFO represents transmitted payload.

In chapter 10 and 11, user can also find below FIFO information.

- (1) Figure 10.15 and 10.16 for FIFO accessing via 3-wire SPI.
- (2) Section 10.4.7 and 10.4.8 for FIFO pointer reset command.
- (3) Figure 11.2 and Figure 11.3 for Normal/Quick FIFO mode.

16.1 Packet Format

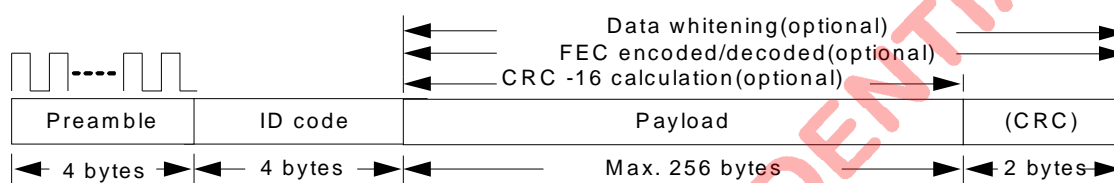


Figure 16.1 Packet Format of FIFO mode

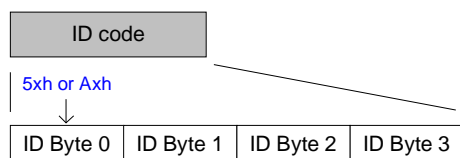


Figure 16.2 ID Code Format

Preamble:

The packet is led by preamble which is composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101...0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010...1010. Preamble length is recommended to set 4 bytes by PML [1:0] (1Ah).

ID code:

ID code is recommended to set 4 bytes by IDL=1 (1Ah) and ID Code is sequenced by ID Byte 0, 1, 2 and 3.

Payload:

Payload length is programmable by FEP [7:0] (03h). The physical FIFO depth is 64 bytes. A7325 also supports logical FIFO extension up to 256 bytes. See section 16.5 for details.

CRC (option):

In FIFO mode, if CRC is enabled (CRCS=1, 1Ah), 2-bytes of CRC value is transmitted automatically after payload.

Relative Control Register

Mode Control Register (MODEC at address 01h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Control I	W	DDPC	--	--	SPSS	WOTE	--	FMS	ADCM
	R	DDPC	--	--	SPSS	WOTE	--	FMS	ADCM
Reset		0	--	--	--	0	--	0	0

FIFO Register I (FIFO1 at address 03h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO I	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FIFO Register II (FIFO2 at address 04h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFO II	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FIFO DATA Register (FIFOD at address 05h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFOD	W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

ID DATA Register (IDD at address 06h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IDD	W	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Reset		0	0	0	0	0	0	0	0

Code Register I (CODE1 at address 1Ah)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CODE1I	W	MCS	WHTS	FECS	CRCS	IDL1	IDL0	PML1	PML0
Reset		0	0	0	0	0	1	1	1

16.2 Bit Stream Process

A7325 supports 3 optional bit stream process for payload, they are,

- (1) CCITT-16 CRC
- (2) (7, 4) Hamming FEC
- (3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1 (1Ah). TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1 (1Ah). Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word and delivered out automatically.
(ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)

Data Whitening:

1. Data whitening is enabled by WHTS= 1 (1Ah). Payload and CRC value (if CRCS=1) or their encoded code words (if FECS=1) are encrypted by bit XOR operation with PN7. The initial seed of PN7 is set by WS [6:0] (1Bh).

16.3 Transmitting Time

Based on CRC and FEC options, the transmission time are different. See table 16.1 for details.

Data Rate = 2 Mbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit * 0.5 us = 288 us
32	32	512	16 bits	Disable	592 bit * 0.5 us = 296 us
32	32	512	Disable	512 * 7 / 4	960 bit * 0.5 us = 480 us
32	32	512	16 * 7 / 4	512 * 7 / 4	988 bit * 0.5 us = 494 us

Data Rate = 1 Mbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit * 1.0 us = 576 us
32	32	512	16 bits	Disable	592 bit * 1.0 us = 592 us
32	32	512	Disable	512 * 7 / 4	960 bit * 1.0 us = 960 us
32	32	512	16 * 7 / 4	512 * 7 / 4	988 bit * 1.0 us = 988 us

Data Rate = 500 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 2 us = 1.152 ms
32	32	512	16 bits	Disable	592 bit X 2 us = 1.184 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 2 us = 1.920 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 2 us = 1.976 ms

Data Rate = 250 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 4 us = 2.304 ms
32	32	512	16 bits	Disable	592 bit X 4 us = 2.368 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 4 us = 3.840 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 4 us = 3.952 ms

Data Rate = 125 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 8 us = 4.608 ms
32	32	512	16 bits	Disable	592 bit X 8 us = 4.736 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 8 us = 7.580 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 8 us = 7.904 ms

Data Rate = 50 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 20 us = 11.52 ms
32	32	512	16 bits	Disable	592 bit X 20 us = 11.84 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 20 us = 19.20 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 20 us = 19.76 ms

Data Rate = 2 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
-----------------	----------------	----------------	------------	-----	----------------------------

32	32	512	Disable	Disable	576 bit X 0.5 ms = 0.288 s
32	32	512	16 bits	Disable	592 bit X 0.5 ms = 0.296 s
32	32	512	Disable	512 x 7 / 4	960 bit X 0.5 ms = 0.480 s
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 0.5 ms = 0.494 s

Table 16.1 Transmission time

16.4 Usage of TX FIFO

In application points of view, A7325 supports 3 options of FIFO arrangement.

- (1) Easy FIFO
- (2) Segment FIFO
- (3) FIFO Extension

For FIFO operation, A7325 supports Strobe command to reset TX FIFO pointer as shown below. User can refer to section 10.5 for FIFO write pointer reset and FIFO read pointer reset.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	X	x	FIFO write pointer reset (for TX FIFO)

FIFO Register I (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	0	1	1	1	1	1	1

FIFO Register II (Address: 04h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0
Reset		0	1	0	0	0	0	0	0

FIFO DATA Register (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
Reset		0	0	0	0	0	0	0	0

16.4.1 Easy FIFO

In Easy FIFO, max FIFO length is 64 bytes. FIFO length is equal to (FEP [7:0] + 1). User just needs to control FEP [7:0] (03h) and disable PSA and FPM as shown below.

Register setting

TX	Control Registers		
FIFO Length (byte)	FEP[7:0] (03h)	PSA[5:0] (04h)	FPM[1:0] (04h)
1	0x00	0	0
8	0x07	0	0
16	0x0F	0	0

32	0x1F	0	0
64	0x3F	0	0

Table 16.3 Control registers of Easy FIFO

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A7325 reference code).
2. Set FEP [7:0] = 0x3F for 64-bytes FIFO.
3. Refer to Figure 11.2 and Figure 11.3
4. Send Strobe command – TX FIFO write pointer reset.
5. MCU writes 64-bytes data to TX FIFO.
6. Send TX Strobe Command.
7. Done.

Definitions

DP : Deliver Pointer

TX FIFO Empty = DP reaches FEP[7:0]

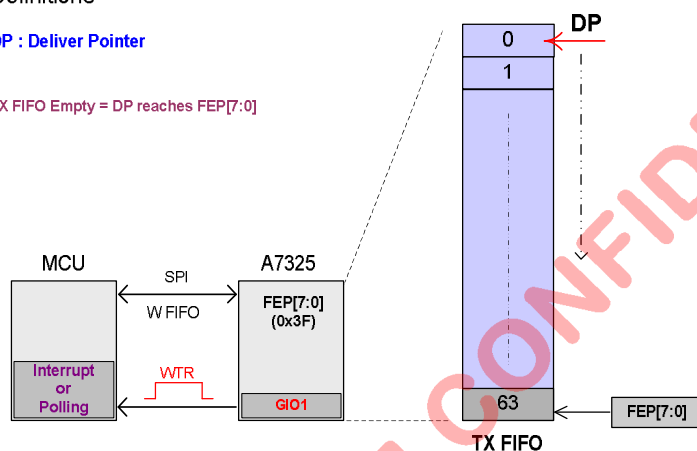


Figure 16.3 Easy FIFO

16.4.2 Segment FIFO

In Segment FIFO, TX FIFO length is equal to $(FEP [7:0] - PSA [5:0] + 1)$. FPM [1:0] should be zero. This function is very useful for button applications. In such case, each button is used to transmit fixed code (data) every time. During initialization, each fixed code is written into corresponding segment FIFO once and for all. Then, if button is triggered, MCU just assigns corresponding segment FIFO (PSA [5:0] and FEP [7:0]) and issues TX strobe command.

If TX FIFO is arranged into 8 segments, each TX segment is 8 bytes

TX				Control Registers		
Segment	PSA	FEP	FIFO Length (byte)	PSA[5:0] (04h)	FEP[7:0] (03h)	FPM[1:0] (04h)
1	PSA1	FEP1	8	0x00	0x07	0
2	PSA2	FEP2	8	0x08	0x0F	0
3	PSA3	FEP3	8	0x10	0x17	0
4	PSA4	FEP4	8	0x18	0x1F	0
5	PSA5	FEP5	8	0x20	0x27	0
6	PSA6	FEP6	8	0x28	0x2F	0
7	PSA7	FEP7	8	0x30	0x37	0
8	PSA8	FEP8	8	0x38	0x3F	0

Table 16.4 Segment FIFO is arranged into 8 segments

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer A7325 reference code).
2. Refer to Figure 11.2 and Figure 11.3 (in chapter 11).
3. Send Strobe command – TX FIFO write pointer reset.
4. MCU writes fixed code into corresponding segment FIFO once and for all.
5. To consign Segment 1, set PSA = 0x00 and FEP= 0x07
To consign Segment 2, set PSA = 0x08 and FEP= 0x0F
To consign Segment 3, set PSA = 0x10 and FEP= 0x17
To consign Segment 4, set PSA = 0x18 and FEP= 0x1F
To consign Segment 5, set PSA = 0x20 and FEP= 0x27
To consign Segment 6, set PSA = 0x28 and FEP= 0x2F
To consign Segment 7, set PSA = 0x30 and FEP= 0x37
To consign Segment 8, set PSA = 0x38 and FEP= 0x3F
6. Send TX Strobe Command.
7. Done.

Definitions

DP : Deliver Pointer

TX FIFO Empty = DP reaches FEP[7:0]

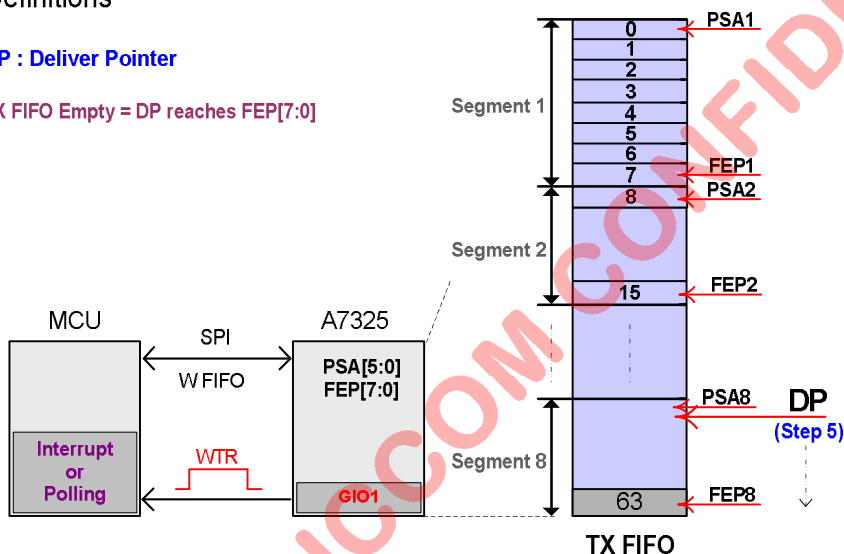


Figure 16.4 Segment FIFO Mode

16.4.3 FIFO Extension

In FIFO Extension, FIFO length is equal to **(FEP [7:0] +1)**. PSA [5:0] shall be zero, and FPM [1:0] is used to set FIFO Pointer Flag (FPF) to MCU. FIFO extension could be set up to 256 bytes by FEP [7:0] with different FPF trigger conditions.

Be notice, setting of SPI data rate is important to prevent error operation of FIFO extension. The min. SPI data rate shall be equal or greater than **(A7325 data rate + 500Kbps)** and refer Table 16.4 and 16.5 for max. SPI Data Rate.

If A7325 data rate = 2Mbps and FIFO extension = 256 bytes.

TX			Control Registers		
FIFO Length (byte)	FPF Trigger Condition	Max. SPI Data Rate	FEP[7:0]	FPM[1:0]	PSA[5:0]
256	Delta = 04	10 Mbps	0xFF	00	0
	Delta = 08	10 Mbps		01	0
	Delta = 12	10 Mbps		10	0
	Delta = 16	8 Mbps		11	0

Table 16.5 How to set FIFO extension when A7325 is at 2Mbps data rate

If A7325 data rate = 1Mbps and FIFO extension = 256 bytes.

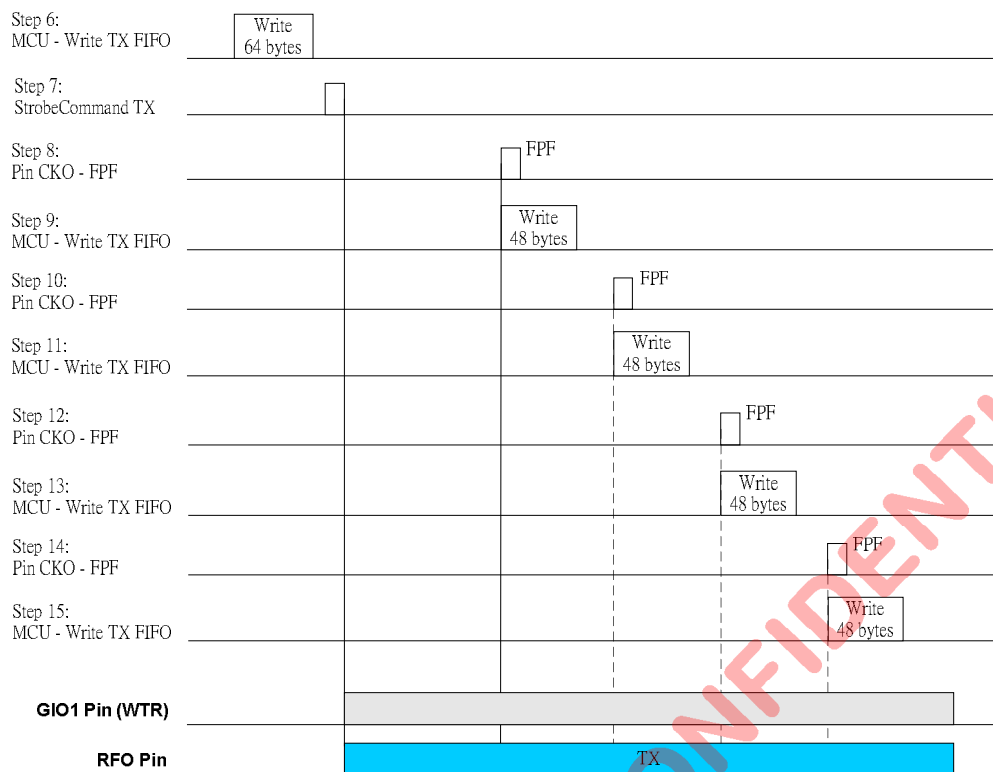
TX			Control Registers		
FIFO Length (byte)	FPF Trigger Condition	Max SPI Data Rate	FEP[7:0]	FPM[1:0]	PSA[5:0]
256	Delta = 04	10 Mbps	0xFF	00	0
	Delta = 08	8 Mbps		01	0
	Delta = 12	5 Mbps		10	0
	Delta = 16	4 Mbps		11	0

Table 16.6 How to set FIFO extension when A7325 is at 1Mbps data rate

Please refer to AMICCOM's reference code (FIFO extension) for details.

Procedures of TX FIFO Extension

1. Initialize all control registers (refer A7325 reference code).
2. Set FEP [7:0] = 0xFF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11 for FPF trigger condition.
4. Set CKO Register = 0x12
5. Send Strobe command – TX FIFO write pointer reset.
6. MCU writes 1st 64-bytes TX FIFO.
7. Send TX Strobe command.
8. MCU monitors FPF from A7325's CKO pin.
9. FPF triggers MCU to write 2nd 48-bytes TX FIFO.
10. Monitor FPF.
11. FPF triggers MCU to write 3rd 48-bytes TX FIFO.
12. Monitor FPF.
13. FPF triggers MCU to write 4th 48-bytes TX FIFO.
14. Monitor FPF.
15. FPF triggers MCU to write 5th 48-bytes TX FIFO.
16. Done.



Definitions

DP : Deliver Pointer
 RP : Received Pointer
 WTX : Write TX FIFO Pointer
 Delta : $WTX - DP + 1 = 16$ if FPM=11

TX FIFO Empty = DP reaches FEP[7:0]

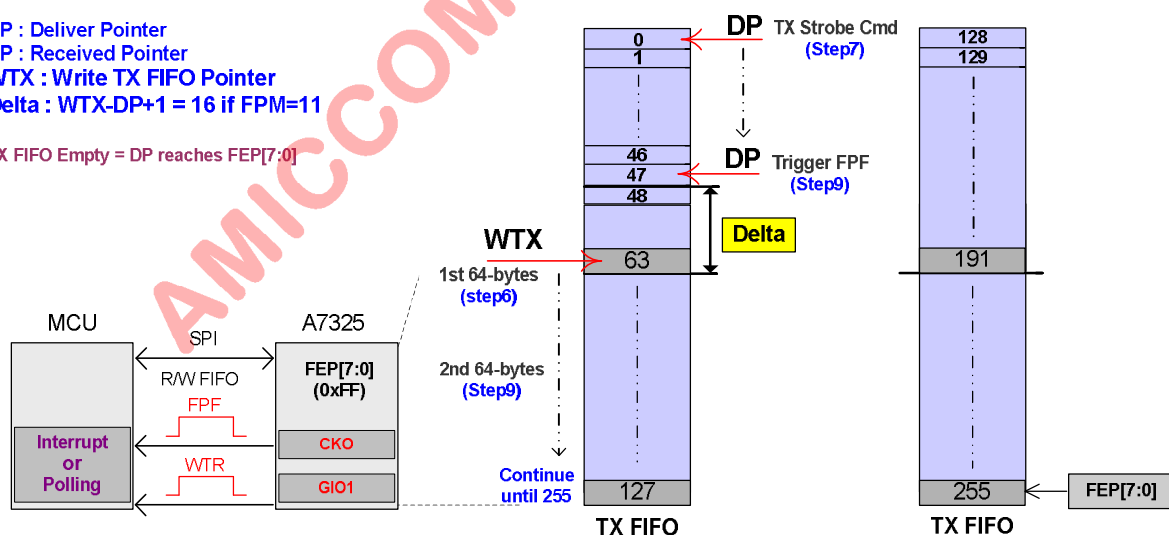


Figure 16.5 TX FIFO Extension

17. Analog Digital Converter

A7325 builds in 8-bit ADC for internal temperature measurement as well as perform external signal measurement through EXAD pin by set bit XADS = 1 in ADC control register (address 19h).

The conversion time of 8-bit ADC is depends on FSARS (19h) which is ADC clock select. Recommend 8 times average of ADC operation (MVSEL = [11]) to insure the accurate ADC result. Therefore, it total takes 160 ADC clock cycles (if FSARS = 0, one cycle is 0.25us. If FSARS = 1, one cycle is 0.125us.) for one ADC conversion.

17.1 temperature measurement

A7325 has built-in thermal sensor. Combined with 8-bits ADC, it can be used to monitor the relative environment temperature. Below is the measurement procedure:

1. Set XADS = 0 (19h), FSARS= 0 (19h).
2. Enter Standby mode.
3. Set ADCM= 1 (01h). A7325 will enable relative temperature measurement automatically.
4. After measurement done, ADCM is auto clear.
5. User can read digital temperature value from ADC [7:0] (19h).

17.2 External voltage measurement

A7325 provides an input pin EXAD for measurement of external signal. The measurable range is 0.3 ~ 1.5 Volt. Connect the signal to EXAD pin and set ADC register bit XADS=1 in standby mode.

1. Set XADS = 1 (19h), FSARS= 0 (19h).
2. Enter Standby mode.
3. Set ADCM= 1 (01h). A7325 will enable ADC conversion from EXAD pin automatically.
4. After measurement done, ADCM is auto clear.
5. User can read digital temperature value from ADC [7:0] (19h).

18. Battery Detect

A7325 has a built-in battery detector to check supply voltage (REGI pin). The detecting range is 2.0V ~ 2.7V in 8 levels.

Battery detect Register (BD at address: 23h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BD	W	RGS	RGV1	RGV0	LVR	BVT2	BVT1	BVT0	BD_E
	R	RGS	RGV1	RGV0	BDF	BVT2	BVT1	BVT0	BD_E
Reset		0	1	0	0	0	1	1	0

BVT [2:0]: Battery voltage detect threshold.

[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V.

[100]: 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

Below is the procedure to detect low voltage input (ex. below 2.1V):

1. Set A7325 in standby or PLL mode.
2. Set BVT (23h) = [001] and enable BD_E (23h) = 1.
3. After 5 us, BD_E is auto clear.
4. MCU reads BDF (23h).
If REGI pin > 2.1V,
BDF = 1 (battery high). Else, BDF = 0 (battery low).

19 TX power setting

A7325 supports programmable TX power from – 20dBm ~ 5 dBm by TX test register. User can configures PAC[1:0] and TBG[2:0] for different TX power level. The following tables show the typical TX power vs. current in different settings.

TX test Register (TXT at address 24h)

Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXT	W	TXSM1	TXSM0	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		0	0	0	1	0	1	1	1

TX Output Power and Current		PAC							
		0		1		2		3	
		power (dBm)	current (mA)	power (dBm)	current (mA)	power (dBm)	current (mA)	power (dBm)	current (mA)
TBG	0	-17.05	10.67	-16.05	11.70	-15.35	13.52	-15.09	16.06
	1	-14.31	10.74	-13.22	11.74	-12.60	13.55	-12.33	16.09
	2	-11.54	10.84	-10.45	11.82	-9.82	13.61	-9.55	16.13
	3	-8.29	11.05	-7.23	11.98	-6.58	13.72	-6.29	16.21
	4	-4.99	11.44	-4.02	12.28	-3.35	13.92	-3.04	16.34
	5	-1.48	12.17	-0.66	12.89	0.00	14.33	0.36	16.59
	6	1.87	13.31	2.53	13.96	3.15	15.15	3.55	17.16
	7	4.63	14.70	5.20	15.45	5.76	16.49	6.19	18.10

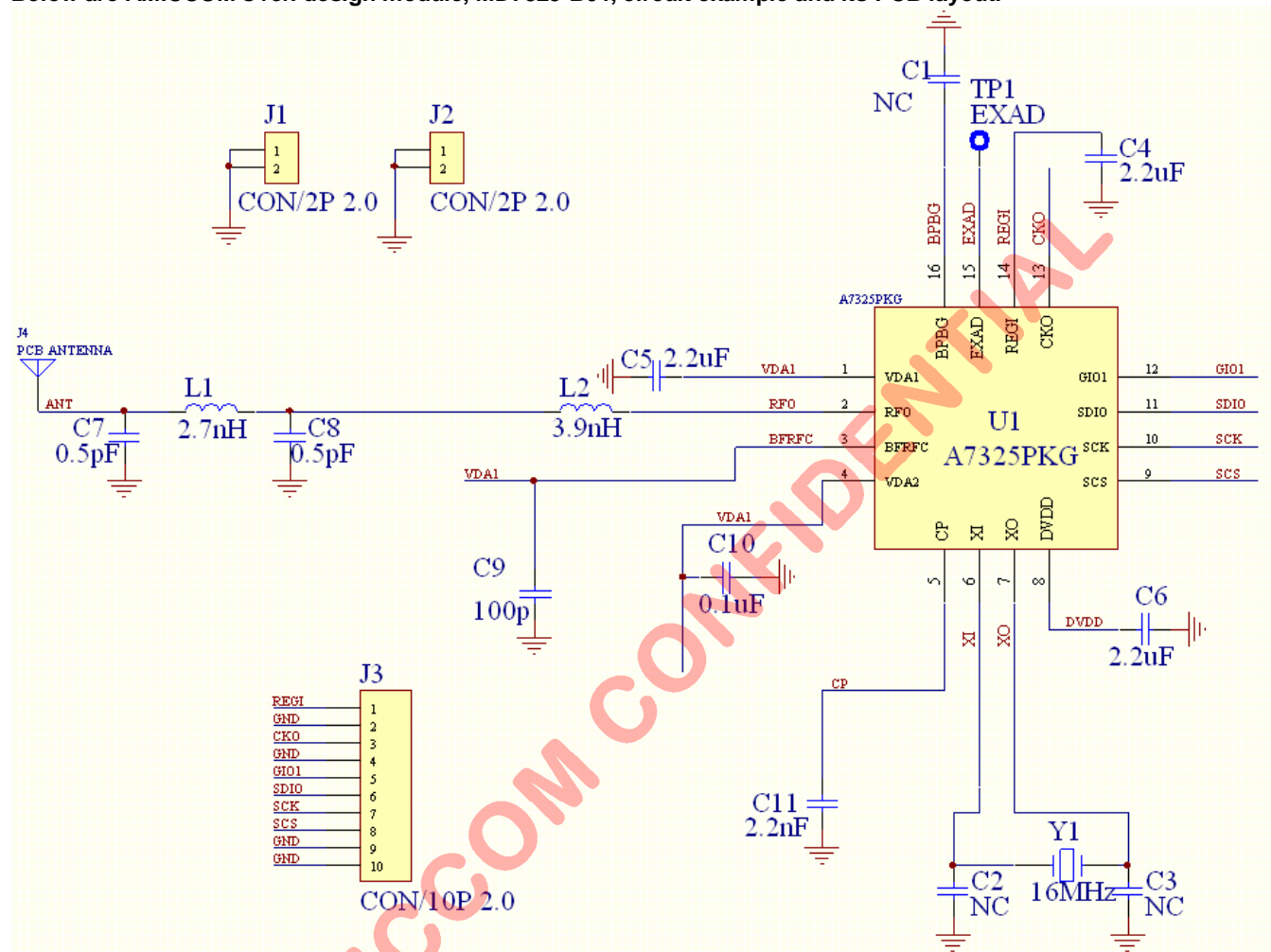
For 5 dBm TX output power, the register setting: PAC = 2 and TBG = 7 are recommended.

For 0 dBm TX output power, the register setting: PAC = 2 and TBG = 5 are recommended.

For -5 dBm TX output power, the register setting: PAC = 0 and TBG = 4 are recommended.

20. Application circuit

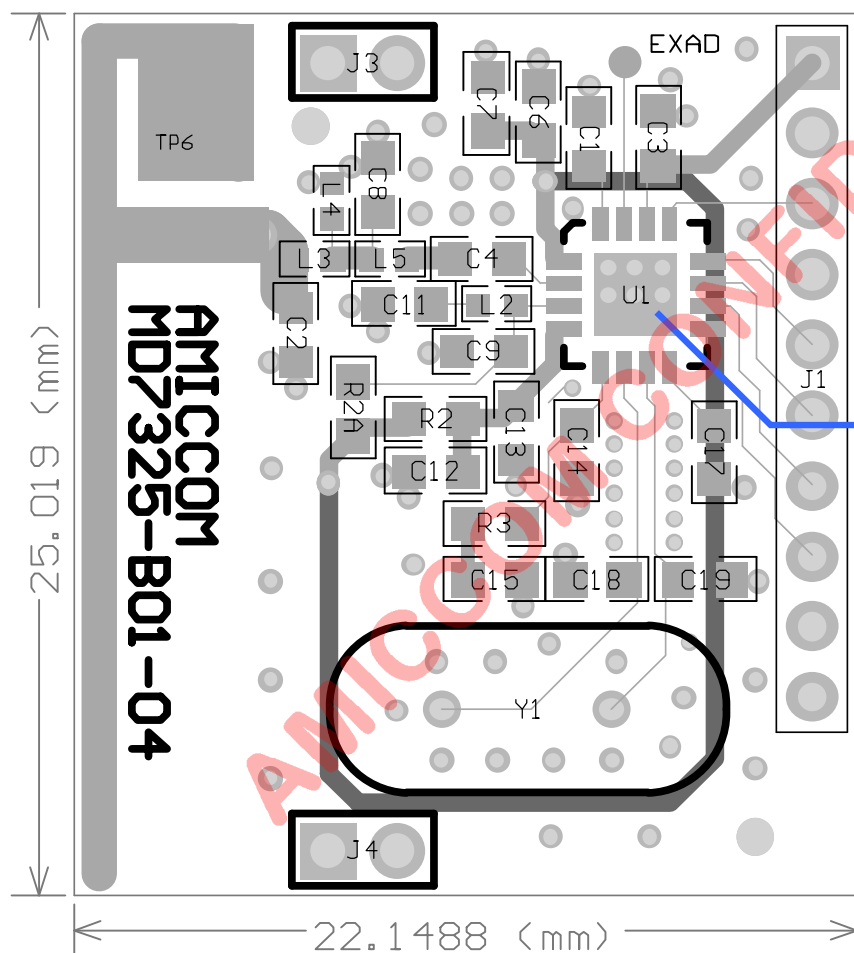
Below are AMICCOM's ref. design module, MD7325-B01, circuit example and its PCB layout.



1. A7325 schematic for RF layouts with single ended 50Ω RF output.
2. C18 and C19 could be leaf out, but use internal programmable Xtal capacitors to match different Xtal's load capacitance (C-load). The recommended crystal C-load is 18 pF.

MD7325-B01 which size is 25mm x 22mm with PCB antenna is suitable for small form factor application. MD7325-B01 is based on a design by a double-sided **FR-4** board of **0.8mm** thickness. All passive components are 0402 / 0603 size. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. Keep sufficient via holes to connect the top layer ground areas to the bottom layer ground plane. **Be notice, IC back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

To get a good RF performance, the well designed PCB is necessary. A poor layout can lead to loss of RF performance especially on matching networks as well as VDD bypass capacitors. PCB layout of critical traces shall follow AMICCOM's recommended values and layout placement. Long power supply lines on the PCB should be avoided. Keep GND via holes as close as possible to A7325's **GND** pad and IC back side plate (**GND**).



- Be Notice,
1. IC Back side plate shall be well-solder to ground (U1 area) for good RF performance.
 2. Need at least 6 GND via holes at U1 area

21. Abbreviations

ADC	Analog to Digital Converter
BW	Bandwidth
CHSP	Channel Step
CRC	Cyclic Redundancy Check
DC	Direct Current
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

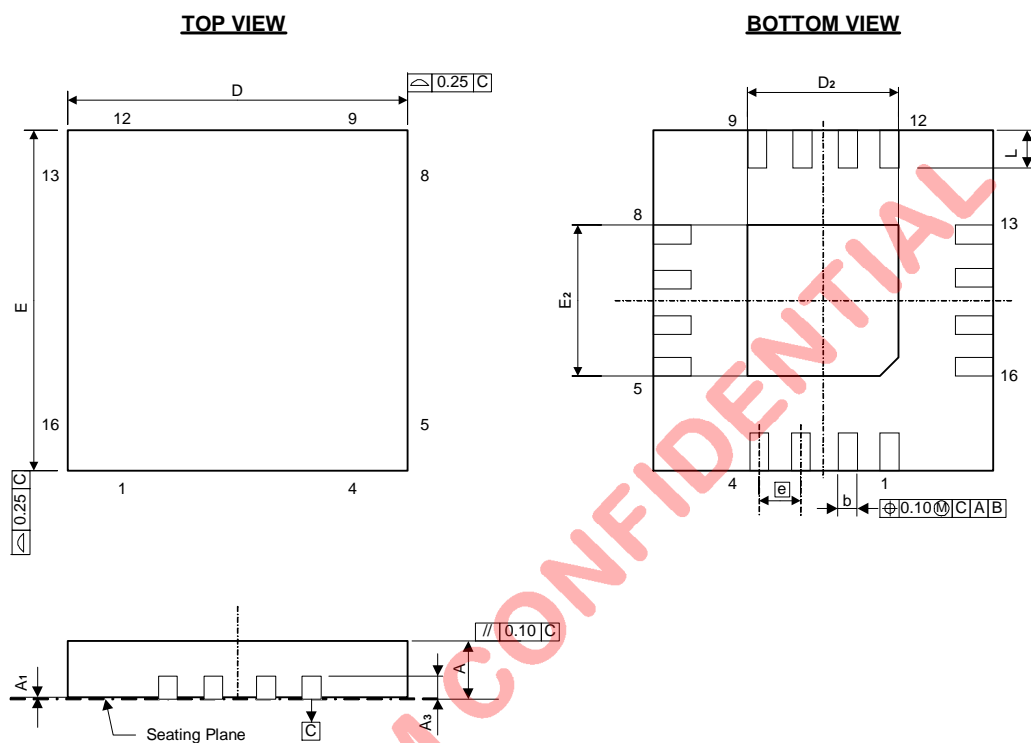
22. Ordering Information

Part No.	Package	Units Per Reel / Tray
A73X25AQFI/Q	QFN16L, Pb Free, Tape & Reel, -40°C ~ 85°C	3K
A73X25AQFI	QFN16L, Pb Free, Tray, -40°C ~ 85°C	490EA
A73X25AH	Die form, Tray, -40°C ~ 85°C	250EA

23 Package Information

QFN16L (4 X 4 X 0.8mm) Outline Dimensions

unit: inches/mm

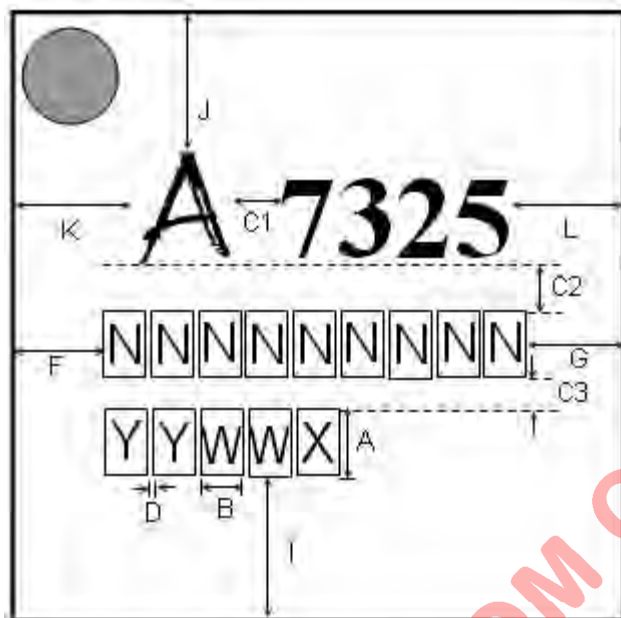


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.7	0.75	0.8	27.56	29.53	31.5
A1	0	0.02	0.05	0	0.79	1.97
A3	8.00 REF			0.203 REF		
b	9.84	11.81	14.96	0.25	0.3	0.38
D	151.57	157.48	163.39	3.85	4.00	4.15
D2	78.72	90.54	102.36	2.00	2.30	2.60
E	151.57	157.48	163.39	3.85	4.00	4.15
E2	78.72	90.54	102.36	2.00	2.30	2.60
e	25.59 BSC			0.65 BSC		
L	15.74	20.86	25.58	0.40	0.53	0.65

24. Top Marking Information

A73X25AQFI

- Part No. : A73X25AQFI
- Pin Count : 16
- Package Type : QFN
- Dimension : 4*4 mm
- Mark Method : Laser Mark
- Character Type : Arial



✧ CHARACTER SIZE : (Unit in mm)

A : 0.55
 B : 0.36
 C1 : 0.25 C2 : 0.3 C3 : 0.2
 D : 0.03
 A1 : 0.75
 B2 : 0.7

F=G
 I=J
 K=L

YYWW

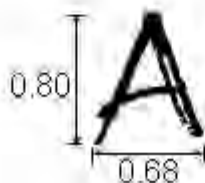
: DATECODE

X

: PKG HOUSE ID

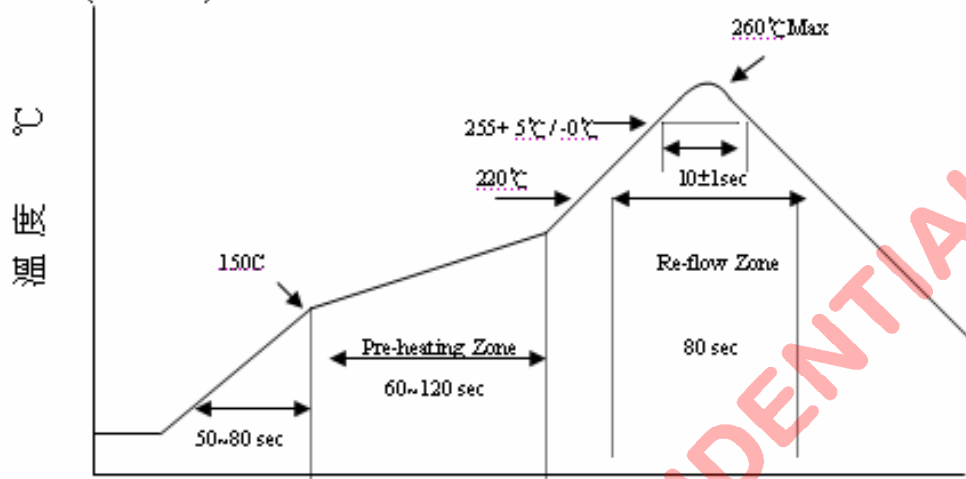
NNNNNNNNNN

: LOT NO.
(max. 9 characters)

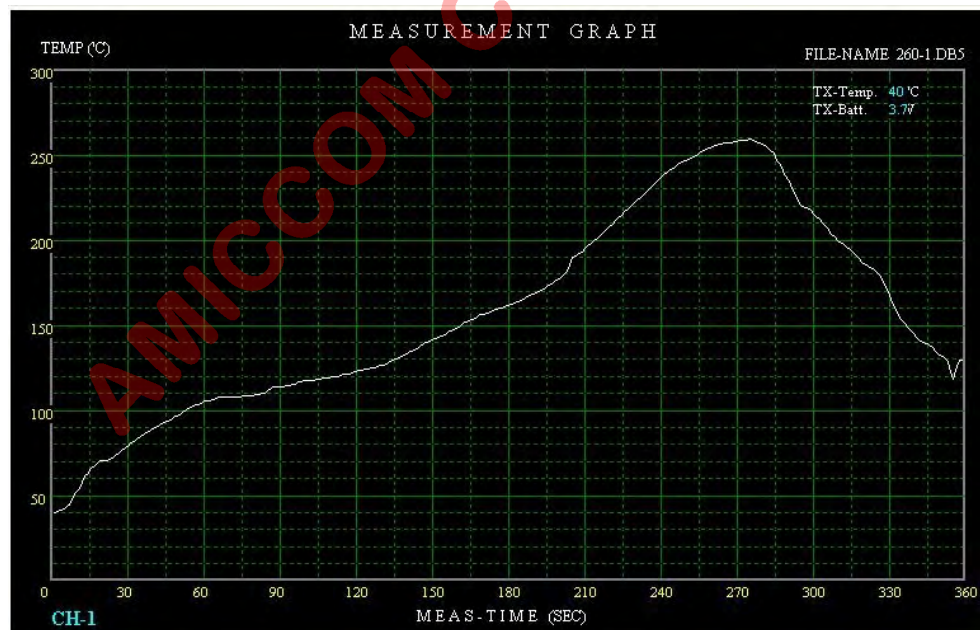


25. Reflow Profile

LEAD FREE (GREEN) PROFILE :

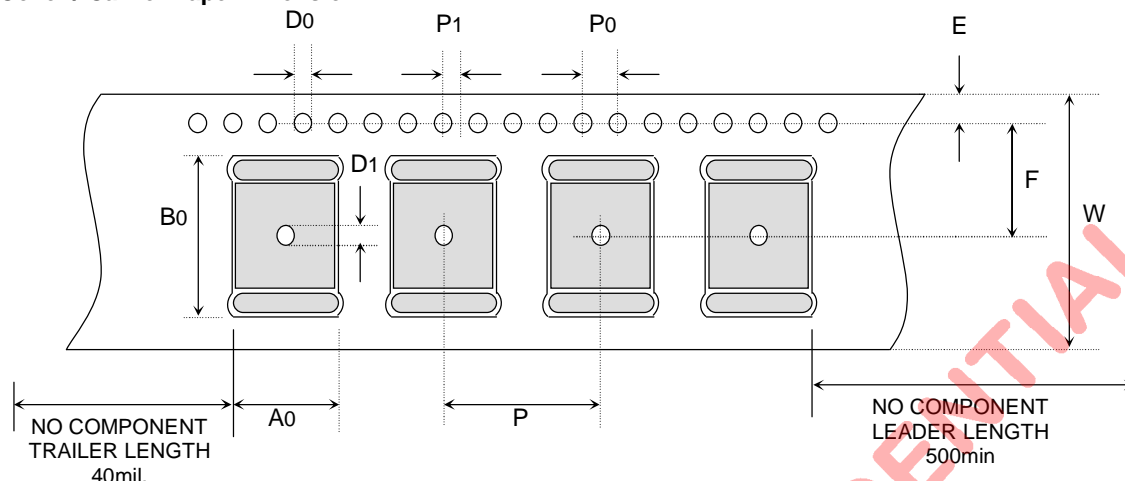


Actual Measurement Graph



26. Type Reel Information

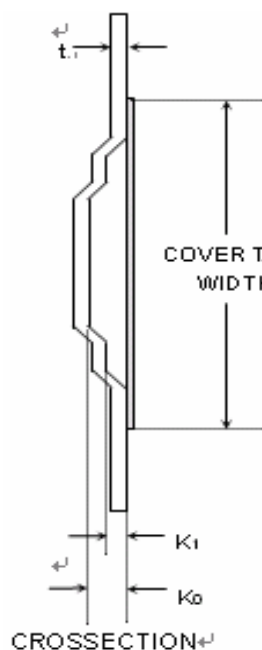
Cover / Carrier Tape Dimension



11 EA IC

60cm±4cm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
48 QFN 7*7	12	7.25	7.25	4.0	2.0	1.5	1.5	1.75	7.5	16
DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16
28 SSOP (150mil)	8	6	10	4.0	2.0	1.5	1.5	1.75	7.5	16



TYPE	K0	K1	t
20 QFN (4X4)	1.1	-	0.3
24 QFN (4X4)	1.4	-	0.3
32 QFN (5X5)	1.1	-	0.3
48 QFN (7X7)	1.1	-	0.3
DFN-10	0.75	-	0.25
20 SSOP	2.5	-	0.3
24 SSOP	2.1	-	0.3
28 SSOP (150mil)	2.5	-	0.3

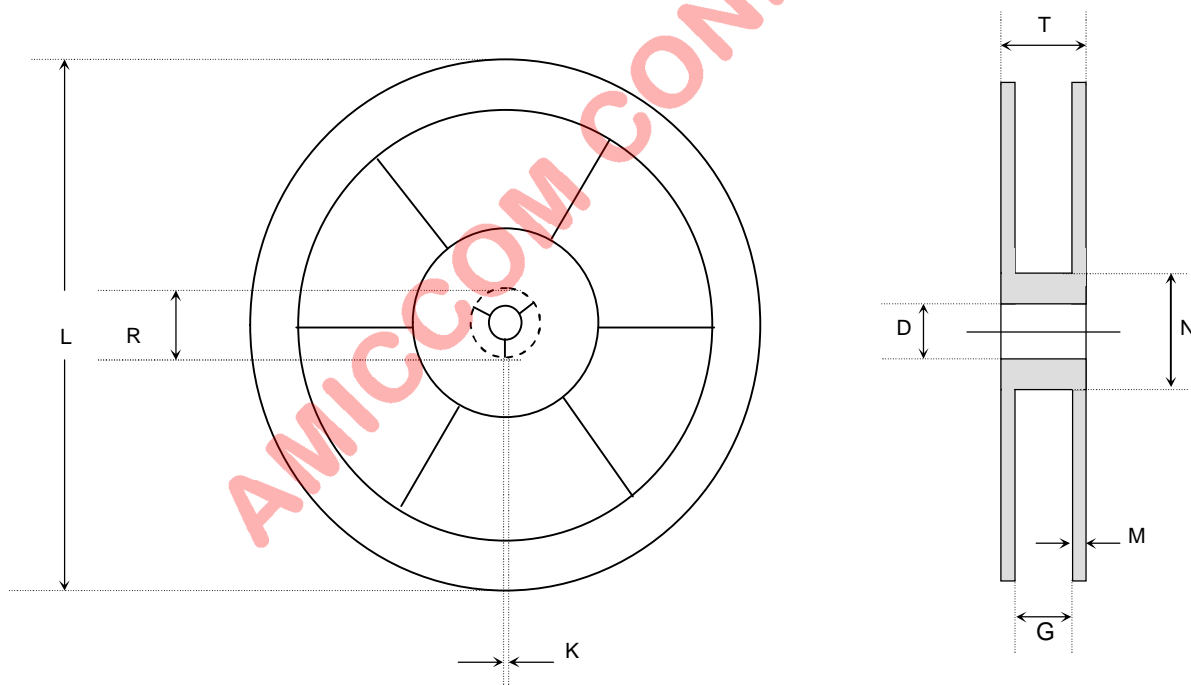
COVER TAPE WIDTH
9.2
9.2
9.2
13.3
8
13.3
13.3
12.5

Unit : mm

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+ 0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330+ 0.00/-1.0	20.2



27. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

RF ICs AMICCOM



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