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FW introduction -- A7103 series



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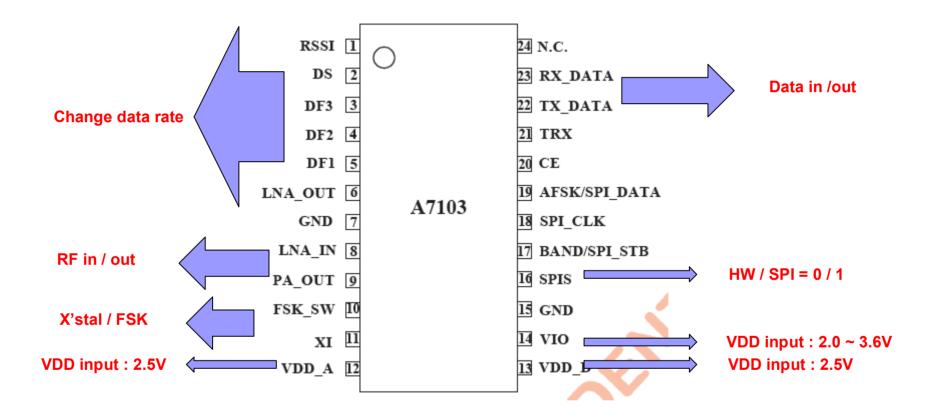
- A7103
- A7201
- A7202
- A7302

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- > RF Frequency:
 - >315/433MHz(A7103A)
 - >868/915MHz(A7103B)
- RF modulation : ASK / FSK
- Data rate: 1-10Kbps(ASK) / 1-20Kbps(FSK)
- > Operating voltage : 2.2V-3.0V(EXT. 2.5V LDO)
- TX/RX current : 18mA[FSK]/10mA[ASK](@10dBm), 9mA
- RX sensitivity : -106 ~ -110dBm(2.4Kbps)
- Build in Analog RSSI
- ► I/O voltage : 2.0 ~ 3.6V(VIO)
- Support SPI & HW modes

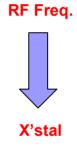


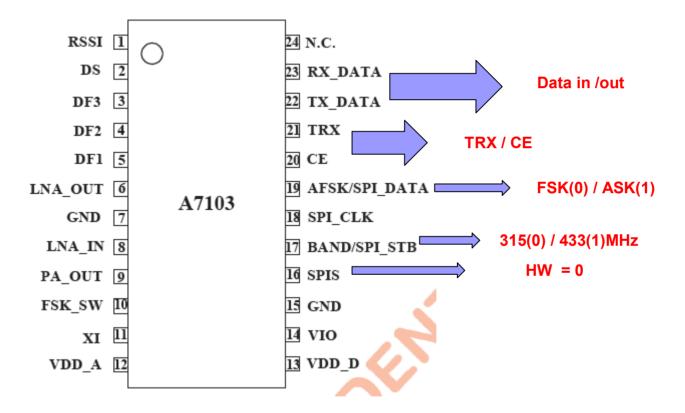


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A7103





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A7103

	Band 315N	1Hz		Band 434MF	łz
Xtal (MHz)	Pin 17	F _{RF} (MHz)	Xtal (MHz)	Pin 17	F _{RF} (MHz)
13.0498	0	303	13.2785	1	424.5
13.064	0	303.33	13.3337	1	426.2625
13.0853	0	303.825	13.3407	1	426.4875
13.0875	0	303.875	13.3517	1	426.8375
13.1036	0	304.25	13.4663	1	430.5
13.1144	0	304.5	13.5445	1	433
13.2866	0	308.5	13.5288	1	432.5
13.3513	0	310	13.542	1	432.92
13.3943	0	311	13.546	1	433.05
13.397	0	311.062	13.5576	1	433.42
13.502	0	313.5	13.56	1	433.496
13.5235	0	314	13.5717	1	433.87
13.545	0	314.5	13.5732	1	433.92
13.56	0	314.846	13.5804	1	434.15
13.5666	0	315	13.5889	1	434.42
13.5732	0	315.1527	13.8181	1	441.75
13.5752	0	315.2			
13.5881	0	315.5			
13.6097	0	316			
13.6442	0	316.8			
13.6958	0	318			
	F _{RF} = F _{XTAL} x 743 / 32			$F_{RF} = F_{XTAL} \times 102$	3 / 32

Table 9.3.2 Xtal selection guide in HW control mode

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A7103

Default setting in HW Mode					
TX Power	Max (typical 10 dBm)				
IFB [1:0]	[10] (mid)				
AGC	Enable				

Table 9.3.3 Default settings in HW control mode.

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A7103

Settling time

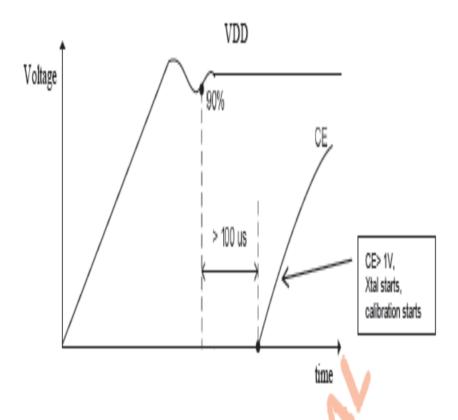


Fig 9.5.2. CE pin is controlled by MCU for a correct start up sequence.

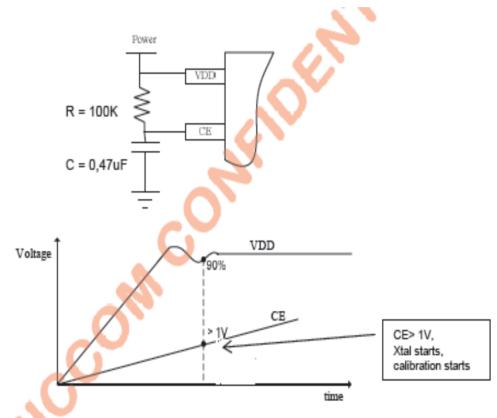


Fig 9.5.1. An extra RC delay on CE pin for correct start up sequence.

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A7103

868/915MHz

	Settling Time (Typical)	
Xtal settling	Without Ccomp	1.2 ms
	With Ccomp	6 ms
TX settling time		0.3 ms
RX settling time		3 ms

Settling time - 15/433MHz

Table 9.5.1 Typical settling time

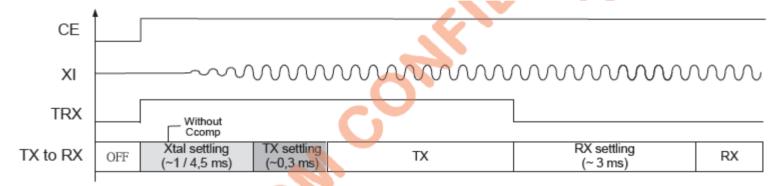


Fig 9.5.3 Settling time from shut down mode to TX mode.

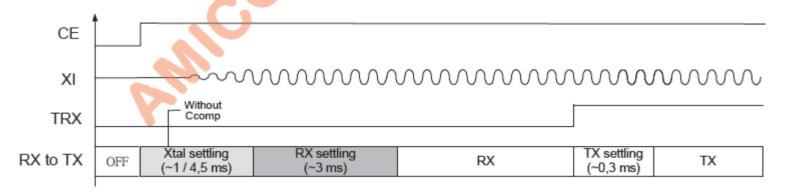


Fig 9.5.4 Settling time from shut down mode to RX mode.

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A7103

Preamble

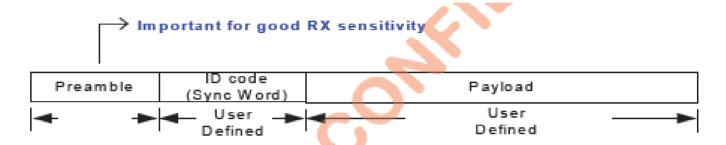


Figure 9.6.1 Packet Format

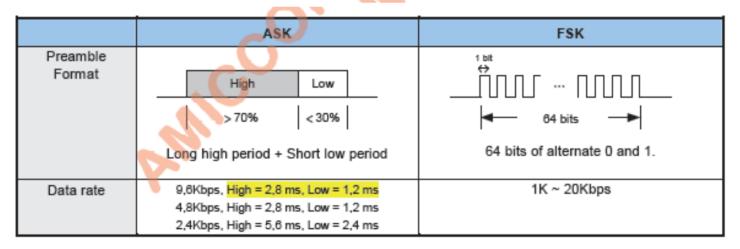


Table 9.6.1 Preamble Format

Payload:

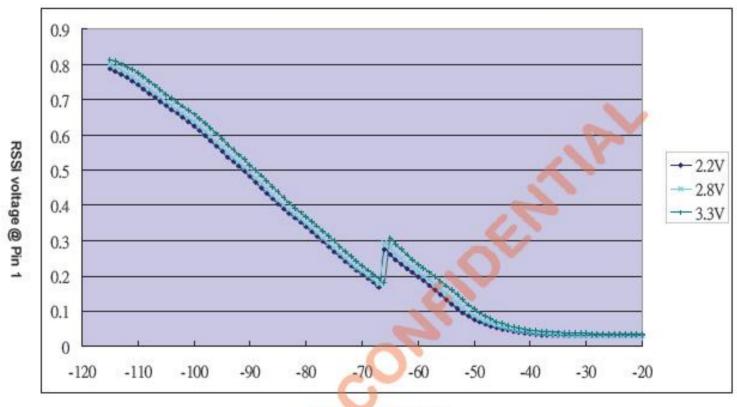
Payload is a carrier-information by user definition. Please noted, in ASK modulation, Do NOT apply data pattern in continuous low for over 40 ms. Otherwise, AGC circuit will operate abnormal.

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A7103

RSSI - SPI(en/disable)



Input RF Power (dBm)

Figure 9.7.1 Typical RSSI curve at 434MHz

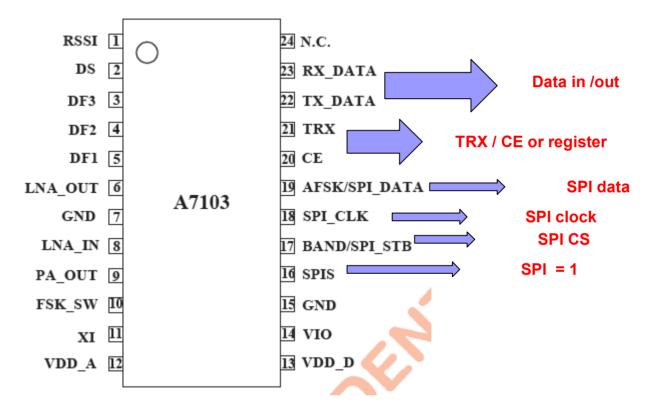
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A7103

SPI mode





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SPI mode

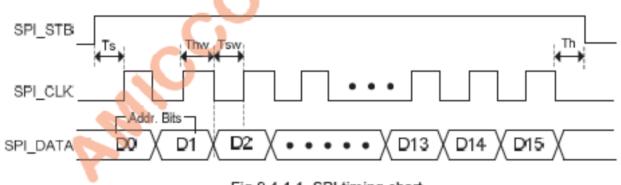


Fig 9.4.1.1 SPI timing chart

Parameter	Description	Min	Max	Unit
Fc	SPI Clock Frequency		4	MHz
Ts	SPI_STB Setup Time	50		ns
Thw	SPI_DATA Hold Time	50		ns
Tsw	SPI_DATA Setup Time	50		ns
Th	SPI_STB Hold Time	50		ns

Table 9.4.1.1 SPI timing characteristic

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A7103

SPI mode

R[1:0]: Xtal reference frequency.

R [1:0]	Xtal (MHz)	R counter	Note
11 /	Reserved	Reserved	
10	12	15	PLL ref. freq = 800KHz, PLL step = RF step = 800KHz
01	13.5732 /13.56	16	PLL ref. freq = 848KHz, PLL step = RF step = 848KHz
00	16	20	PLL ref. freq = 800KHz, PLL step = RF step = 800KHz

NB, NA: Used to define wanted FRF of PLL (see below table).

NA[3:0]: NA is odd (1 / 3 / 5 / 7) and complement.

NB[7:0]: NB is (5 ~ 40) and complement.

Formula Ex		Example of 4	Example of 433.92 MHz				
		NA = 15 = [111	NA = 15 = [1111b] NA 1's complement = [0000b]				
FRF = FXTAL X N / 2	2R		NB = 63 = [001]	1-1111b]	NB 1's complement = [1100-0000b]		
			$N = 16 \times 63 + 6$	15 = 1023			
			R = 16 (FXTAL =	13.5732MHz)			
			F _{RF} = 13.5732	(1023 / 2 / 16	F _{RF} = 433.92	MHz	
	Band 315MHz			Band 434MHz			
NA	NB	E	xample	NA	NB	Example	
1	43	FRF	9	1	62	FRE	
3	44		(743) / 2 / 16	3	63	= 13.5732 x (1023) / 2 /	
5	45	= 314.84 [VIHz 5	5	64	16	
7	46	0.0		7	65	= 433.92 MHz	
9	47 🌑	30		9	66		
11				11			
13			112	13			
15				15			



A7103 RF Module







A7103 EK kit



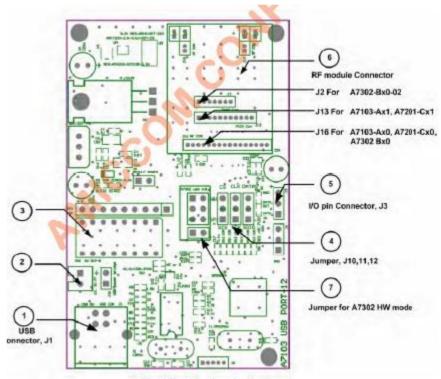


Fig. 1 Topside of evaluation board



A7103 DK kit





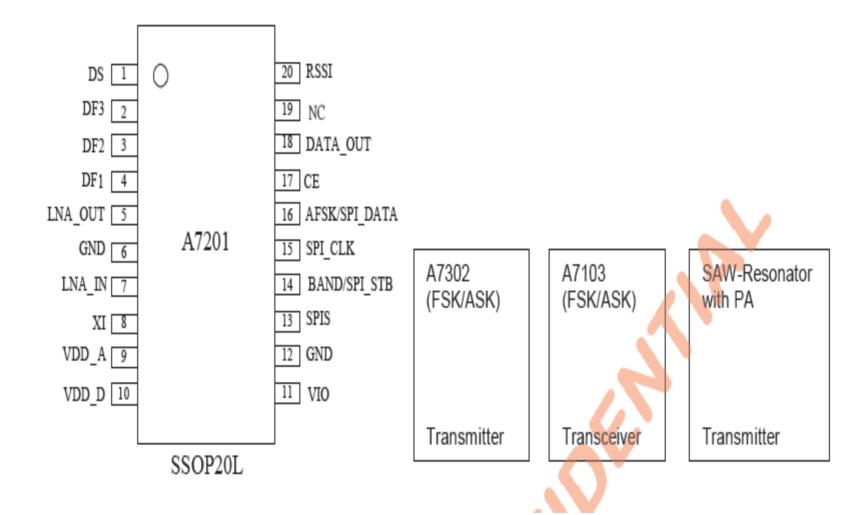
A7103 TF kit



- > RF Frequency:
 - >315/433MHz(A7201A)
 - >868/915MHz(A7201B)
- RF modulation : ASK / FSK
- Data rate: 1-10Kbps(ASK) / 1-20Kbps(FSK)
- Operating voltage : 2.2V-3.0V(EXT. 2.5V LDO)
- RX current : 9mA
- RX sensitivity : -106 ~ -110dBm(2.4Kbps)
- Build in Analog RSSI
- ► I/O voltage : 2.0 ~ 3.6V(VIO)
- Support SPI & HW modes

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A7201

Development tools

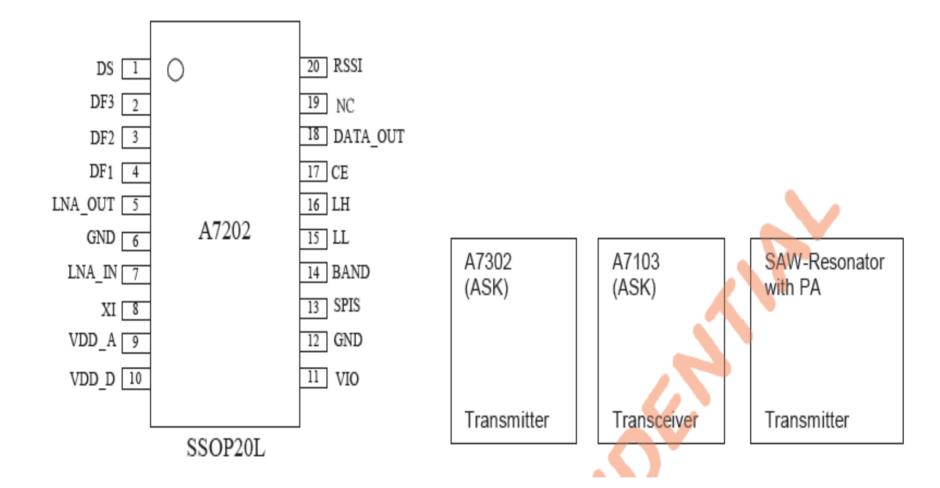
Module / reference code / EK / DK / TF



- > RF Frequency:
 - >315/433MHz(A7202A)
 - >868/915MHz(A7202B)
- > RF modulation : ASK
- Data rate : 1-10Kbps(ASK)
- Operating voltage : 2.2V-3.0V(EXT. 2.5V LDO)
- RX current : 9mA
- RX sensitivity: -106 ~ -110dBm(2.4Kbps)
- Build in Analog RSSI
- I/O voltage : 2.0 ~ 3.6V(VIO)
- Support HW modes

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A7202

Development tools

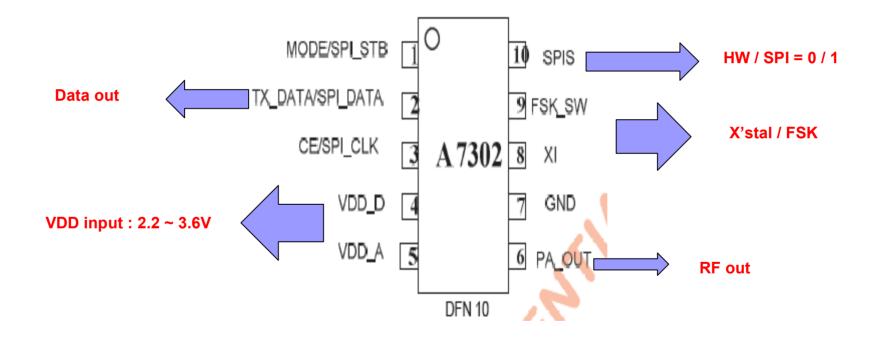
Module / reference code / EK / DK / TF

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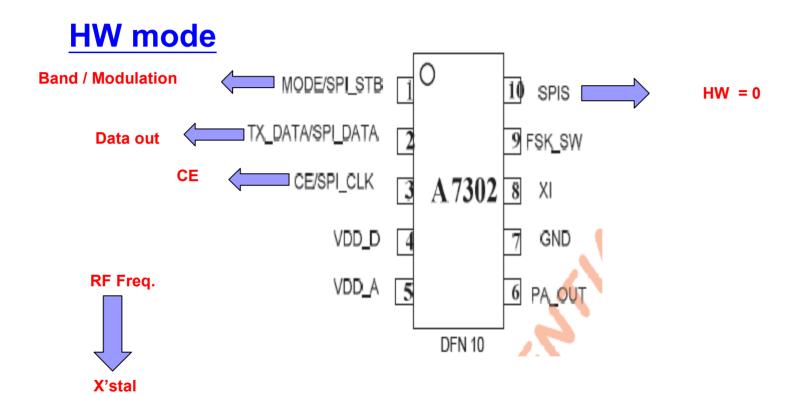
- > RF Frequency:
 - >315/433MHz(A7302C)
 - >868/915MHz(A7302D)
- RF modulation : ASK / FSK
- Data rate: 1-10Kbps(ASK) / 1-20Kbps(FSK)
- Operating voltage : 2.2V-3.0V(EXT. 2.5V LDO)
- TX current : 14mA[FSK]/8.8mA[ASK](@10dBm)
- ➢ I/O voltage : 2.0 ~ 3.6V(VIO)
- Support SPI & HW modes







A7302



FSK(0) / ASK(1)

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A7302

	310MHz ~ 330MHz			425MHz ~ 445	MHz
Crystal (MHz)	SPIS	FRF (MHz)	Crystal (MHz)	SPIS	F _{RF} (MHz)
9.6875	0	310	13.4531	0	430.5
9.7187	0	311	13.5	0	432
9.7206	0	311.062	13.5156	0	432.5
9.7968	0	313.5	13.5287	0	432.92
9.8125	0	314	13.5328	0	433.05
9.8281	0	314.5	13.5443	0	433.42
9.8389	0	314.846	13.5467	0	433.496
9.8437	0	315	13.5584	0	433.87
9.8485	0	315.1527	13.56	0	433.92
9.85	0	315.2	13.5671	0	434.15
9.8593	0	315.5	13.5756	0	434.42
9.875	0	316			
9.9	0	316.8			
9.9375	0	318			
F _{RF} =	F _{RF} = F _{XTAL} x 32			FXTAL X 32	

Table 9.2.3 Crystal selection guide in HW control mode



A7302

Default setting in HW Mode						
TX Power	typical 10 dBm					
R [1:0]	R = 2					
N	N=128					
PLL Comparison freq.	6.78MHz					

Table 9.2.1 Default settings in HW control mode.

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A7302

Settling time

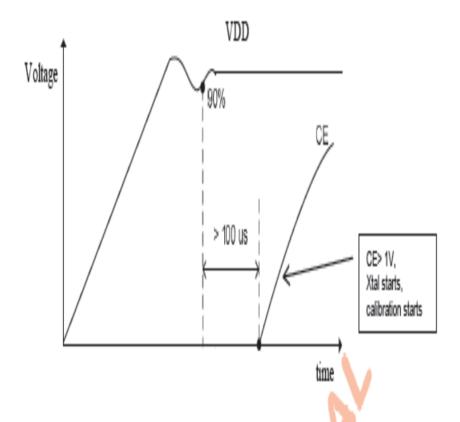


Fig 9.5.2. CE pin is controlled by MCU for a correct start up sequence.

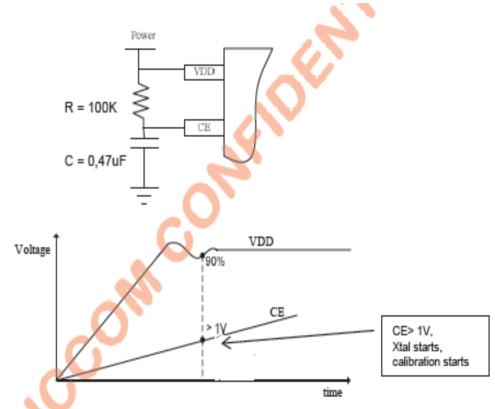


Fig 9.5.1. An extra RC delay on CE pin for correct start up sequence.

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A7302

Settling time

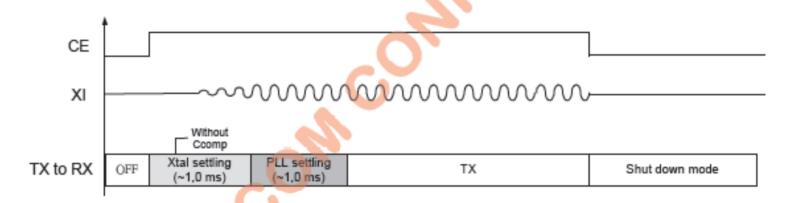


Fig 9.4.3 Settling time from shut down mode to TX mode.

Settling Time (Typical)							
Xtal settling	Without Ccomp	1 ms					
	With Ccomp	5 ms					
PLL settling time		1 ms					

Table 9.4.1 Typical settling time



A7302

Preamble

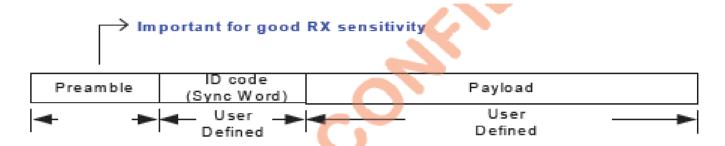


Figure 9.6.1 Packet Format

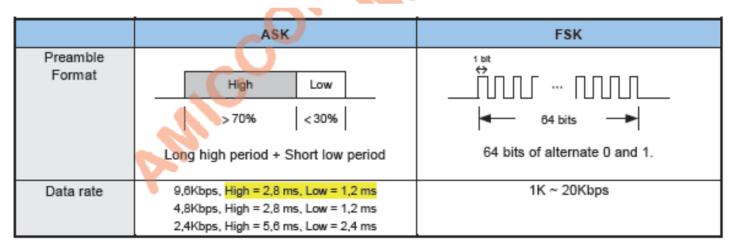


Table 9.6.1 Preamble Format

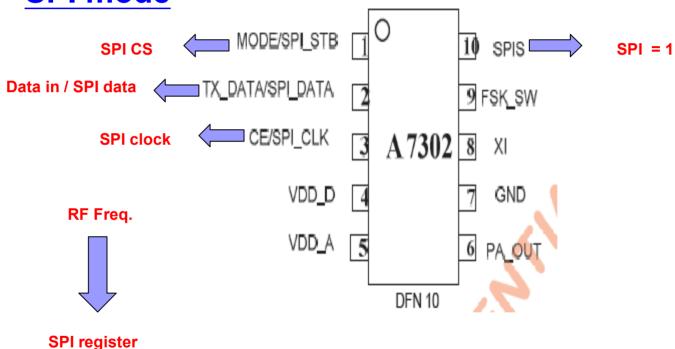
Payload:

Payload is a carrier-information by user definition. Please noted, in ASK modulation, Do NOT apply data pattern in continuous low for over 40 ms. Otherwise, AGC circuit will operate abnormal.



A7302

SPI mode



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A7302

SPI mode - timing

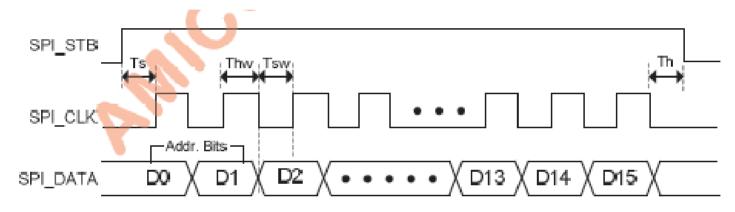


Fig 9.3.1.1 SPI timing chart

Parameter	Description	Min	Max	Unit
Fc	SPI Clock Frequency		4	MHz
Ts	SPI_STB Setup Time	50		Ns
Thw	SPI_DATA Hold Time	50		Ns
Tsw	SPI_DATA Setup Time	50		Ns
Th	SPI_STB Hold Time	50		Ns

Table 9.3.1.1 SPI timing characteristic



A7302

SPI mode – SPI data / TX data

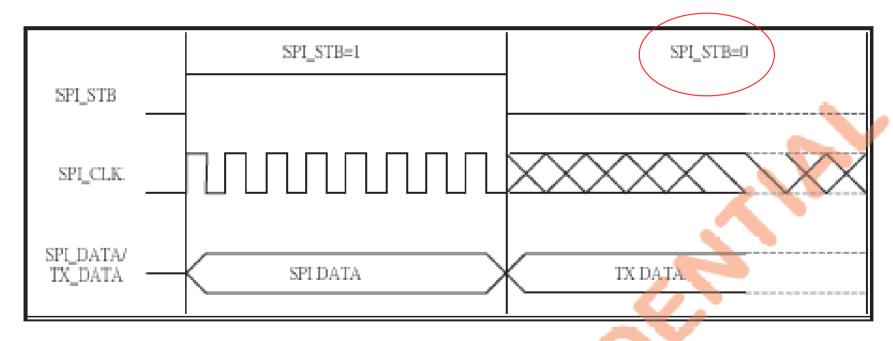


Figure 9.3.1.2 Timing chart of SPI_STB

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A7302

SPI mode - Freq.

R[1:0]: Crystal reference frequency.

R [1:0]	Crystal (MHz)	R counter	Note
00	Reserved	Reserved	
01	12	15	PLL step = 800KHz, RF step = 400 KHz
10	13.56	16	PLL step = 847.5KHz, RF step = 423.75 KHz
11	16	20	PLL step = 800KHz, RF step = 400 KHz

N= (16XNB) +NA. NB=46~144, NA=0~15

NB, NA: Used to define wanted FRF of PLL (see below table).

NA[3:0]: NA is 0 ~ 15. NB[7:0]: NB is 40~65.

Formula

N = 16 x NB + NA F _{RF} = F _{XTAL} x N / 2 / R		NA = 0 = [0000] NB = 64 = [0100] N = 16 x 64 + 0 R = 16 (FXTAL =	0-0000] = 1024 13,56MHz)		
		F _{RF} = 13,56 x 10	24 / 2 / 16	F _{RF} = 433,92 l	
	310MHz ~ 3	330MHz	Ť	425MHz ~	445MHz
NA	NB	Example	NA	NB	Example
0	40	FRE	0	60	FRE
1	41	= 13,56 x(16x46+7) /2 /16	1	61	= 13,56 x(16x64+0) /2/16
3	42	= 314,846 MHz	3	62	= 433,92 MHz
4	43		4	63	
5	44	7.	5	64	
6	45		6	65	
7	46	7	7		
8	47	7	8		
9	48	7.	9		
10	49		10		
11		T'	11		
12			12		
13			13		
14			14		
15			15		

Example

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Development tools

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