Document Title

A7153 Data Sheet, 2.4GHz IEEE 802.15.4 Transceiver

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue.	March 31, 2009	Objective
0.1	Add Register table and update technical info.	Jan, 2010	Objective
0.2	Modify PIN ADCI, VDD_A and BP_BG order	July, 2010	Preliminary
0.3	Modify Chapter 9, register map.	Nov., 2010	Preliminary

Table of Contents

1. Typical Application

- 2.4GHz IEEE 802.15.4 System
- 2.4GHz ZigBee Application
- 2.4GHz RF4CE Remote Control
- Wireless Sensor Network
- Home Automation
- Industrial Control

2. General Description

A7153 is a high performance and low power 2.4GHz IEEE 802.15.4 DSSS transceiver (direct sequence spread spectrum defined in IEEE 802.15.4). It integrates the PHY and MAC functionality in a single chip solution. Regarding to IEEE 802.15.4, the transmit modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping. A7153 integrates LNA, mixer, on-chip filter, power amplifier (up to 3.5dBm), frequency synthesizer and baseband modem. In typical system, A7153 is used together with MCU (microcontroller) with only 13 external passive components including Xtal.

A7153 has built-in separated 128-bytes TX/RX FIFO for data buffering and burst transmission, auto FCS(CRC) filtering, ED for clear channel assessment, AES128 CCM* mode for security packet as well as CSMA-CA to avoid communication collision, thermal sensor for measuring related temperature, CCA to assent clear channel indication. In addition, in two way communication, A7153 supports auto ACK, auto Resend mechanism, Zigbee/RF4CE Frame Filtering and wake-up-radio to simplify system development and cost. Those functions are very easy to use while developing a wireless system. All features are integrated in a small QFN 4X4 24 pins package.

For power saving, A7153 supports deep sleep, sleep mode, idle mode, and standby mode. For easy-to-use, A7153 has a unique SPI command set called **Strobe command** that are used to control A7153's state machine. Based on Strobe commands, from power saving, TX delivery, to RX receiving, MCU only needs to define A7153's control registers and send Strobe commands via SPI interface. In addition, A7153 supports GIO1and GIO2 pins to inform MCU its status so that MCU could use either polling or interrupt scheme to do radio control. Therefore, it is very easy to monitor transmission between MCU and A7153 because of its digital interface.

For range extension, A7153 is very easy to control A7700 (AMICCOM's 2.4GHz RF front-end) by pin22 (XTR1) and pin 23 (XTR2) without the interaction of MCU. A7700 is a range extender for 2.4 GHz RF transceivers products from AMICCOM. A7700 increases the link budget by providing a Power Amplifier (PA), Low Noise Amplifier (LNA) and RF switch. For complete reference design, please refer to MD7153-F07 module spec.

3. Feature

- Small size (QFN 4X4, 24 pins).
- Support 2.4GHz IEEE 802.15.4 DSSS RF Modulation format.
- Low RX current consumption (18mA).
- Low TX current consumption (15mA @ 0dBm, 21mA @ 3.5 dBm output power).
- Deep sleep current (0.02 uA)
- Low sleep current (2.5 uA).
- Programmable RF output power -10dBm ~ 3.5dBm.
- On chip regulator, supports input voltage 2.0 ~ 3.6V.
- Easy to use
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - Change frequency channel by ONE register setting.
  - Clear channel assessment (CCA).
  - Auto-ack and Auto-resend scheme.
  - Auto RSSI measurement.
  - Auto CSMA-CA.
  - Auto Calibrations.
  - Auto IF function.
  - Auto FCS (CRC) Filtering.
  - Zigbee / RF4CE Frame Filtering.
  - Separated 128 bytes RX and TX FIFO.
  - XTR1-XTR2 external RF front-end control.
- Fast settling time synthesizer for transceiver turn around.
- HW AES128 to support CCM* security.
- Support ED (Energy Detect) for CCA.
- Integrated Ring Oscillator for WOR function.
- Built-in Battery Detect, Thermal Sensor and Crystal load capacitors.
- Support low cost crystal (16MHz).
- Support crystal sharing, (4 / 8MHz) to MCU.
- Only 13 external components including Xtal. No balun or crystal load capacitors needed.

4. PIN Configuration

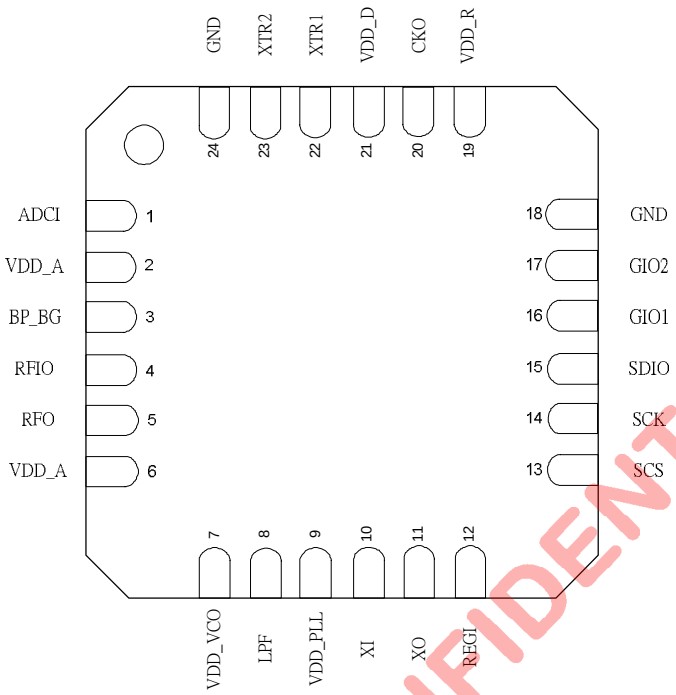


Figure 4.1 A7153 QFN 4X4 Package Top View

5. PIN Description (I: Input, O: Output, I/O: Input or Output, G: Ground, D: Digital)

Pin No.	Symbol	I/O	Function Description
1	ADCI	I	ADC input.
2	VDD_A	O	Analog supply voltage output. Connect to bypass capacitor.
3	BP_BG	O	Band-gap bypass. Connect to bypass capacitor.
4	RFIO	I/O	RF input/output.
5	RFO	O	RF output.
6	VDD_A	O	Analog supply voltage output. Connect to bypass capacitor.
7	VDD_VCO	I	VCO supply voltage input.
8	LPF	O	PLL Loop filter output. Connect to loop filter.
9	VDD_PLL	I	PLL supply voltage input.
10	XI	I	Crystal oscillator input.
11	XO	O	Crystal oscillator output.
12	REGI	I	Regulator input. Connect to VDD supply.
13	SCS	DI	SPI chip select input.
14	SCK	DI	SPI clock input.
15	SDIO	DI/O	SPI data IO.
16	GIO1	DI/O	Multi-function IO 1.
17	GIO2	DI/O	Multi-function IO 2.
18	GND	G	Ground.
19	VDD_R	O	Wakeup timer supply voltage output. Connect to bypass capacitor.
20	CKO	DO	Multi-function clock output.
21	VDD_D	O	Digital supply voltage output. Connect to bypass capacitor.
22	XTR1	DO	External TR switch control output 1.
23	XTR2	DO	External TR switch control output 2.
24	GND	G	Ground.
	Back side plate	G	Ground. **Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

6. Block Diagram

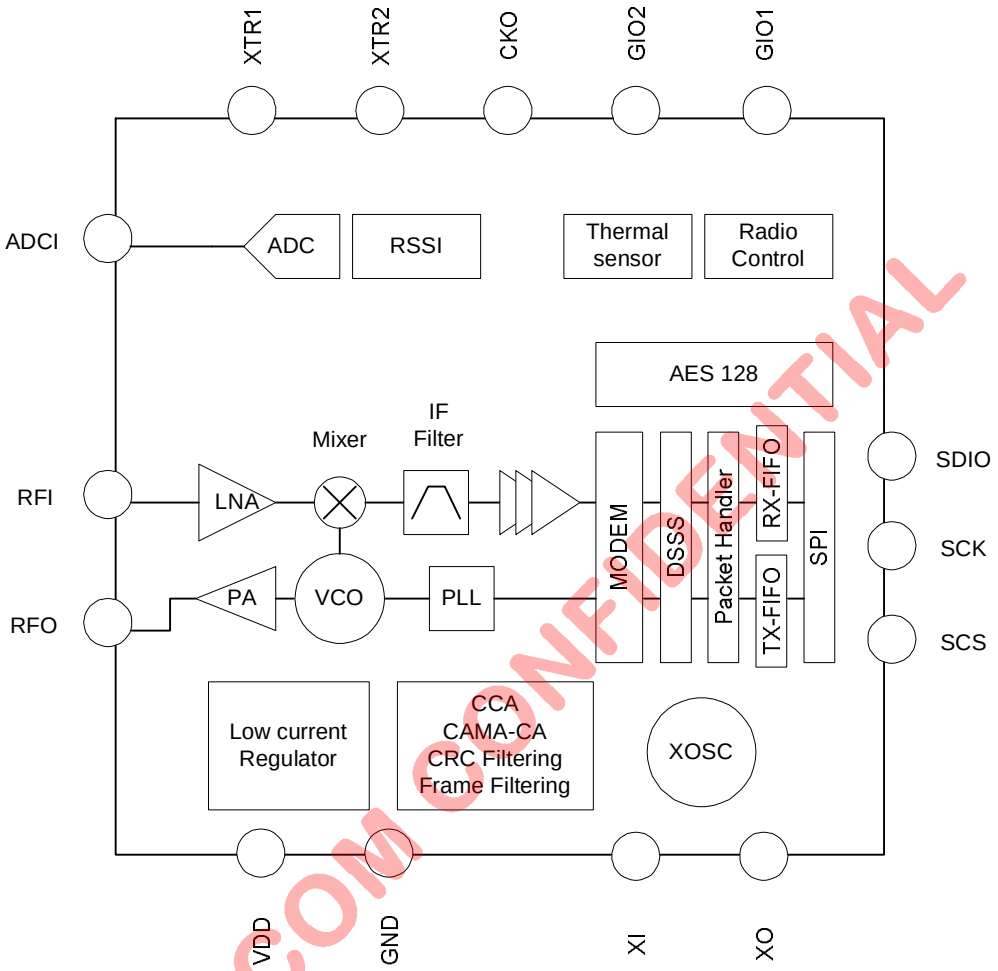


Figure 6.1 A7153 Block Diagram

7. Absolution Maximum Rating

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital I/O pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Input RF level		14	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

8. Electrical Specifications

(Ta=25℃, VDD=3.3V, data rate= 250Kbps, F_{XTAL} =16MHz, On Chip Regulator = 1.8V, PN9 pattern, with matching network and low pass filter, unless otherwise noted.)

Parameter	Description	Minimum	Typical	Maximum	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage (VDD)	Regulator supply input	2.0	3.3	3.6	V
Current Consumption	Deep Sleep Mode		20		nA
	Low Voltage Sleep Mode		1.5		uA
	Sleep Mode		2.5		uA
	Idle Mode (Regulator on)		0.25		mA
	Standby Mode		3		mA
	PLL Mode		9.5		mA
	RX Mode (AGC Off)		18		mA
	RX Mode (AGC On)		20		mA
	TX Mode (@0dBm output)		15		mA
	TX Mode (@3.5dBm output)		21		mA
Phase Locked Loop					
X'TAL Settling Time			500		µs
X'TAL Frequency (F_{XTAL})			**16**		MHz
X'TAL Frequency Accuracy Requirement	Include Tolerance, Over Temperature Stability, Aging	-40		40	ppm
X'TAL Load Capatitance			18		pF
X'TAL ESR				TBD	ohm
PLL Settling Time	@Loop BW = 200 KHz		30		µs
Transmitter					
Carrier Frequency		2405		2480	MHz
Data rate	DSSS mode	125	250	375	Kbps
Chip rate		1	2	3	Mcps
TX Power Control Range	With external LPF	-10	0	3.5	dBm
PSD (Power Spectral Density) Mask	|F-Fc| > 3.5MHz (2Mbps chip rate)		-45		dBm
EVM (Error Vector Magnitude)	Measured for 1000 chips		15		%
Out Band Spurious Emission [1]	30MHz~1GHz			-36	dBm
	1GHz~12.75GHz			-30	
	1.8GHz~ 1.9GHz			-47	
	5.15GHz~ 5.3GHz			-47	
TX Settling Time	@ Loop BW = TBD		30		µs
Receiver					
Sensitivity	PER=1% @PSDU=20 octets		-96		dBm
IF Frequency (F_{IF})			2		MHz
Channel rejection	Adjacent (+/-5MHz)		30		dB
	Alternate (+/-10MHz)		40		dB
Maximum Operating Input Power	@RF input (PER = 1%)			7	dBm
Spurious Emission [1]	30MHz~1GHz			-57	dBm
	1GHz~12.75GHz			-47	
RSSI Range	@RF input	-110		-50	dBm
RX Settling Time	@ Loop BW =200 KHz		30		µs
Regulator					
Regulator settling time			100		µs
Band-gap reference voltage			1.25		V

Regulator output voltage			1.8		V
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: With external RF filter that provides minimum 17dB of attenuation in the band: 30MHz ~ 2GHz and 3GHz ~12.75GHz.

9. Control Register

A7153 has totally built-in 60 control registers that cover all radio control. MCU can access those control registers via 3-wire or 4-wire SPI (Support max. SPI data rate up to 10 Mbps). User can refer to chapter 10 for details of SPI bus. A7153 is simply controlled by registers and outputs its status to MCU by GIO1 and GIO2 pins.

9.1 Control Register Table

Address / Name	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Addr 00h~30h	Short Registers (8 bits)								
00h Mode	W	RESETN	FWPRN	FRPRN	CCMRN	FIFORN	BFCRN	--	--
	R	CSMAF	CCAF	CRCF	CER	XER	PLLER	TRER	TRSR
01h Mode control	W	DFCRC	ENC	CCMS	DFCD	WORE	FMT	FMS	ADCM
	R	--	MICF	CCMS	CD	WORE	FMT	FMS	ADCM
02h Mode select	W	MDS	DMS	PNS	PNIVS	ACKS	ARTS	CSMAS	SLOT
03h Calc	R/W	--	ADCC	RCC	VCC	VBC	VDC	FBC	RSSC
04h PHR	R/W	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
05h FIFO Data	R/W	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
06h SFD	R/W	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0
07h RC OSC I	W	MRONS	INCM	ROS	WUS1	WUS0	ROCE	ROE	TWWS
08h RC OSC II	W	RCDL2	RCDL1	RCDL0	MROBS	MROB3	MROB2	MROB1	MROB0
	R	--	--	--	--	ROB3	ROB2	ROB1	ROB0
09h RC OSC III	W	MRON7	MRON6	MRON5	MRON4	MRON3	MRON2	MRON1	MRON0
	R	RON7	RON6	RON5	RON4	RON3	RON2	RON1	RON0
0Ah CKO Pin	W	FIFOSS	TRDC	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
0Bh GIO1 Pin I	W	XTR1I	XTR1OE	--	GIOS2	GIO1S1	GIO1S0	GIO1I	GIO1OE
0Ch GIO2 Pin II	W	XTR2I	XTR2OE	--	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
0Dh XTR Pin	W	XTR2S3	XTR2S2	XTR2S1	XTR2S0	XTR1S3	XTR1S2	XTR1S1	XTR1S0
0Eh Data Rate Clock	W	SDR1	SDR0	GRC3	GRC1	GRC1	GRC0	CNTR1	CNTR0
0Fh PLL I	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
10h TX I	W	--	PADL	TXDI	TME	TRAMP	FDP2	FDP1	FDP0
11h TX II	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
12h RX	W	IGCR	MGCR	RCP2	RCP1	RCP0	DMG	RXDI	ULS
13h RX Gain I	R/W	IGS1	IGS0	LGS2	LGS1	LGS0	MGS2	MGS1	MGS0
14h RX Gain II	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
15h RX Gain III	W	RSSL7	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
16h RX Gain IV	W	AGS1	AGS0	--	VRSEL	MHC	LHC1	LHC0	AGCE
	R	RU7	RU6	RU5	RU4	RU3	RU2	RU1	RU0
17h ADC	W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0

18h ADC Control	W	--	CDM	RADC1	RADC0	MRHL	XADS	AVGS1	AVGS0
19h IF Calibration I	W	IFHCM	IFTS	--	MFBS	MFB3	MFB2	MFB1	MFB0
	R	VTB1	VTB0	--	FBCF	FB3	FB2	FB1	FB0
1Ah VCO current Calibration	W	--	VCCS1	VCCS0	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
1Bh VCO band Calibration I	W	LPFT1	LPFT0	LPFS	MDAGS	MVBS	MVB2	MVB1	MVB0
	R	--	--	--	--	VBCF	VB2	VB1	VB0
1Ch VCO band Calibration II	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
1Dh VCO deviation Calibration I	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
1Eh VCO deviation Calibration II	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
1Fh VCO modulation Delay	W	--	--	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
20h Channel Offset	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
21h Battery detect	W	ATP2	ATP1	ATP0	ECE	BLE	BDS1	BDS0	BDE
	R	--	--	--	--	BDF	--	--	--
22h TX test	W	--	--	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
23h Rx DEM test I	W	--	--	DCM1	DCM0	LQICE	ARSSI	AIF	LQIS
	R	LQIV7	LQIV6	LQIV5	LQIV4	LQIV3	LQIV2	LQIV1	LQIV0
24h Rx DEM test II	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
	R	DCO7	DCO6	DCO5	DCO4	DCO3	DCO2	DCO1	DCO0
25h Charge Pump Current	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
26h Crystal test	W	CGS	XS	XCL3	XCL2	XCL1	XCL0	XCC	XCP
27h PLL test	W	--	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
28h VCO test	W	--	--	CPCH1	CPCH0	RLB1	RLB0	VCBS1	VCBS0
29h Delay I	W	WD	WSEL1	WSEL0	PDL1	PDL0	TDL2	TDL1	TDL0
2Ah ACK DLY	W	AGC_DLY1	AGC_DLY0	RS_DLY1	RS_DLY0	ACKD3	ACKD2	ACKD1	ACKD0
2Bh ART DLY1	W	RTRTD3	RTRTD2	RTRTD1	RTRTD0	RTTRD3	RTTRD2	RTTRD1	RTTRD0
2Ch ART DLY2	W	RTRAT7	RTRAT6	RTRAT5	RTRAT4	RTRAT3	RTRAT2	RTRAT1	RTRAT0
2Dh CSMA DLY	W	ATLP2	ATLP1	ATLP0	CST1	CST0	MaxNB2	MaxNB1	MaxNB0
2Eh BE	W	MaxBE3	MaxBE2	MaxBE1	MaxBE0	MinBE3	MinBE2	MinBE1	MinBE0
2Fh PTRS	W	--	--	--	--	PTRS3	PTRS2	PTRS1	PTRS0
30h INTST	W	ISTRN	--	CCAM1	CCAM0	EDS	CCAS	ERX	--
	R	INT	IST2	IST1	IST0	EDS	CCAS	ERX	FLAG
Addr 31h~3Eh	Long Registers (>16 bits) High byte and MSB first								
31h ADFC	W	FADDE	ACBEN	ACDAT	ACACK	ACCMD	ACRES	PCORR	MAXVER1
	W	MAXVER0	RESMUX2	RESMUX1	RESMUX0	--	--	--	--
32h ADFF	W	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
	W	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0

	W	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8
	W	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
	W	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56
	W	LADD55	LADD54	LADD53	LADD52	LADD51	LADD50	LADD49	LADD48
	W	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40
	W	LADD39	LADD38	LADD37	LADD36	LADD35	LADD34	LADD33	LADD32
	W	LADD31	LADD30	LADD29	LADD28	LADD27	LADD26	LADD25	LADD24
	W	LADD23	LADD22	LADD21	LADD20	LADD19	LADD18	LADD17	LADD16
	W	LADD15	LADD14	LADD13	LADD12	LADD11	LADD10	LADD9	LADD8
	W	LADD7	LADD6	LADD5	LADD4	LADD3	LADD2	LADD1	LADD0
33h AD CAL	R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0
	R	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
34h ACK FIFO	W	AFCF7	AFCF6	AFCF5	AFCF4	AFCF3	AFCF2	AFCF1	AFCF0
	W	AFCF15	AFCF14	AFCF13	AFCF12	AFCF11	AFCF10	AFCF9	AFCF8
35h PN	W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8
	R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8
	W	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
	R	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
36h PLLII	W	--	--	--	--	--	--	--	BIP8
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
37h PLL III	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
38h PLL IV	W	-	CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8
	W	CHR7	CHR6	CHR5	CHR4	CHR3	CHR2	CHR1	CHR0
39h Channel Group	W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
	W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
3Ah RBTO	W	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
	R	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
	W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8
	R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8
3Bh RBT	W	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
	R	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
	W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8
	R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8
	W	RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
	R	BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
3Ch LAMH	W	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0
	W	LM7	LM6	LM5	LM4	LM3	LM2	LM1	LM0
	W	LH7	LH6	LH5	LH4	LH3	LH2	LH1	LH0
3Dh KEY	W	KEY	KEY	KEY	KEY	KEY	KEY	KEY	KEY
3Eh NONCE	W	NONCE	NONCE	NONCE	NONCE	NONCE	NONCE	NONCE	NONCE

Legend: - = unimplemented

9.2 Control Register Description

SHORT REGISTERS

Addr 00h~30h	Short Registers (8 bits)

9.2.1 Mode Register (Address: 00h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	CSMAF	CCAF	CRCF	CER	XER	PLLER	TRER	TRSR
	W	RESETN	FWPRN	FRPRN	CCMRN	FIFORN	BFCRN	--	--
Write Reset Value		0	0	0	0	0	0	0	0

RESETN: Soft reset. (Write only)
[1]: Soft reset this device. Auto clear when done.

FWPRN: FIFO write point reset. (Write only)
[1]: reset FIFO write pointer. Auto clear when done.

FRPRN: FIFO read point reset. (Write only)
[1]: reset FIFO read pointer. Auto clear when done.

CCMRN: CCM reset. (Write only)
[1]: CCM reset command. Auto clear when done.

FIFORN: FIFO data reset. (Write only)
[1]: Reset FIFO Data to all zero. Auto clear when done.

BFCRN: Back-off counter reset. (Write this register to 1 to issue reset command, then it is auto clear.)
[1]: Reset Back-off counter to zero. Auto clear when done.

CSMAF: CSMA function flag.
[0]: CSMA pass. [1]: CSMA Fail.

CCAF: CCA flag.
[0]: CCA pass. [1]: CCA fail.

CRCF: CRC flag. (Read only and updated for each valid packet.)
[0]: CRC pass. [1]: CRC error.

CER: Chip Status. (Read only)
[0]: Chip is disabled. [1]: Chip is enabled.

XER: Xtal Status. (Read only)
[0]: Crystal oscillator is disabled. [1]: Crystal oscillator is enabled.

PLLE: PLL Status. (Read only)
[0]: PLL is disabled. [1]: PLL is enabled after PLL strobe command.

TRER: TRX Status I. (Read only)
[0]: TRX is disabled. [1]: TRX is enabled.

TRSR: TRX Status II. (Read only)
[0]: RX mode. [1]: TX mode.
Serviceable when TRER=1 (TRX is enable).

9.2.2 Mode Control Register (Address: 01h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	MICF	CCMS	CD	WORE	FMT	FMS	ADCM
	W	DFCRC	ENC	CCMS	DFCD	WORE	FMT	FMS	ADCM
Reset		1	1	0	0	0	0	1	0

DFCRC: Filter RX packet with CRC check.
[0]: Disable. **[1]:** Enable.

ENC: Encryption mode select.
[0]: Dencryption. **[1]:** Encryption.

MICF: MIC flag. (MICF is read only and updated for each valid packet.)
[0]: MIC pass. **[1]:** MIC error.

CCMS: CCM function select. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

DFCD (Data Filter by CD): The received packet will be filtered out.
[0]: Disable. **[1]:** Enable.

CD: Carrier detector (Read only).
[0]: Input power below threshold. **[1]:** Input power above threshold.

WORE: Wake On RX enable.
[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only. It should be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ADCM	Standby mode	RX mode
[0]	Disable ADC	Disable ADC
[1]	Measure temperature or external voltage	Measure RSSI, carrier detect

XADC: Refer to ADC control register (18h).

9.2.3 Mode Select Register (Address: 02h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MDS	MS	PNS	PNIVS	ACKS	ARTS	CSMAS	SLOT
Reset		0	0	0	0	1	0	1	0

MDS: Reserved for internal usage only. It should be set to [0].

MS: Modulation select.
[0]: DSSS. **[1]:** MSK (Turbo mode).

PNS: Reserved. Shall be set to [0].

PNIVS: PN initial seed select. Recommend PNIVS = [0].
[0]: Use RF calibration value. **[1]:** Manual settting by PNIV (35h).

ACKS: Auto ACK enable.
[0]: Disable. **[1]:** Enable.

ARTS: Auto Resend enable.
[0]: Disable. **[1]:** Enable.

CSMAS: CSMA-CA enable.
[0]: Disable. **[1]:** Enable.

SLOT: CSMA_CA algorithm type.
[0]: Unslotted. **[1]:** Slotted.

9.2.4 Calibration Control Register (Address: 03h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	--	ADCC	ROBC	VCC	VBC	VDC	FBC	RSSC
Reset		--	0	0	0	0	0	0	0

ADCC: ADC calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ROBC: RO bank calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VCC: VCO current calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VBC: VCO bank calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

VDC: VCO deviation calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF filter bank Calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

RSSC: RSSI calibration (Auto clear when done).
[0]: Disable. **[1]:** Enable.

9.2.5 PHR Register (Address: 04h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	PHR7	PHR6	PHR5	PHR4	PHR3	PHR2	PHR1	PHR0
Reset		0	0	0	0	0	0	0	0

PHR [7:0] : Physical Header of IEEE 802.15.4.

PHR7: PHR7 is a reserved bit in IEEE802.15.4. In this device, PHR7 is used as FIFO write select.
[0]: Write to TX FIFO.
[**1]:** Write to RX FIFO for CCM operation.
During on-air tramitting, PHR7 is always sent by zero.

PHR [6:0]: Frame Length in IEEE 802.15.4.
Write : TX FIFO Length.
Read : RX FIFO received length.

9.2.6 FIFO DATA Register (Address: 05h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	TX-FIFO[7:0]							
	R/W	RX-FIFO[7:0]							
Reset		0	0	0	0	0	0	0	0

FIFO [7:0]: TX FIFO / RX FIFO
TX FIFO and RX FIFO share the same address (05h).
TX FIFO and RX FIFO have independent physical 128 Bytes.

Noted that RX FIFO is writble for CCM operation when FIFOWS = 1 (04h).

9.2.7 SFD Register (Address: 06h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SFD7	SFD6	SFD5	SFD4	SFD3	SFD2	SFD1	SFD0
Reset		1	0	1	0	0	1	1	1

SFD [7:0]: Start Frame Delimiter (write only).
SFD [7:0] is default 0xA7 based on IEEE 802.15.4.

9.2.8 RO Register I (Address: 07h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MRONS	INCM	ROS	WUS1	WUS0	RONC	ROE	WORE
Reset		0	0	0	1	1	0	1	0

MRONS: Manual RON value setting.
[0]: Auto. **[1]:** Manual.

INCM: Reserved for internal usage only. It should be set to [0].

ROS: Internal ring oscillator select. It should be set to [1].

WUS [1:0]: Wake up select when WOR is enbled.
[00]: Carrier detect.
[01]: IEEE 802.15.4 Sync word detect.

[10]: IEEE 802.14.4 Beacon detect.
[11]: CRC pass.

RONC: RON calibration.
[0]: Disable. **[1]:** Enable.

ROE: Internal ring oscillator enable.
[0]: Disable. **[1]:** Enable.

WORE: Wake On RX enable.
[0]: Disable. **[1]:** Enable.

9.2.9 RO Register II (Address: 08h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	ROB3	ROB2	ROB1	ROB0
	W	ROBCD2	ROBCD1	ROBCD0	MROBS	MROB3	MROB2	MROB1	MROB0
Reset		1	0	1	0	1	0	0	0

ROBCD [2:0]: Reserved for internal usage only. It should be set to [010].

MROBS: Manual ROB setting.
[0]: Auto settting. **[1]:** Manual setting.

MROB [3:0]: RO Bank manual calibration value (write only).
Manual setting when MROBS =1.

ROB [3:0]: RO Bank auto calibration value (read only).

9.2.10 RO Register III (Address: 09h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RON7	RON6	RON5	RON4	RON3	RON2	RON1	RON0
	W	RONCG7	RONCG6	RONCG5	RONCG4	RONCG3	RONCG2	RONCG1	RONCG0
Reset		0	1	0	1	0	0	0	0

RON[7:0]: RO N Counter calibration result (read only).

RONCG[7:0]: RO N Counter Generator (write only).
RO N Counter calibration goal or manual setting.

9.2.11 CKO Pin Control Register (Address: 0Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FIFOSS	TRDC	CKOS2	CKOS1	CKOS0	CKOI	CKOE	SCKI
Reset		0	0	0	0	0	0	1	0

FIFOSS: FIFO sequence order select.
[0]: LSB first. **[1]:** MSB first.

TRDC: RFIO pin and RFO pin control.
[0]: Internal Combined.
RFIO pin is Input/Output (bi-directional for PA output and LNA input).
RFO pin is NC.

[1]: External Cominbed.
RFIO pin is Input (single-directional for LNA input).
RFO pin is Output (single-directional for PA output).

CKOS [2:0]: CKO pin output select.
[000]: INTF (refer to 30h).
[**001]:** BDF (Low battery detection output).
[010]: XRDY.
[011]: SDO (4 wires SPI data output).
[100]: BBCK (4XDR).
[101]: RO 320us. (20 symbols).
[110]: RO frequency.

[111]: Data clock (2M or 250K).

CKOI: CKO pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCKI: SPI clock input invert.
[0]: Non-inverted input. **[1]:** Inverted input.

9.2.12 GIO1 Pin Control Register (Address: 0Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	XTR1I	XTR1OE	--	GIO1S2	GIO1S1	GIO1S0	GIO1I	GIO1OE
Reset		1	1		0	1	1	0	1

XTR1I: XTR1 pin output invert.
[0]: Non-inverted output. **[1]:** Inverted output.

XTR1OE: XTR1 pin Output Enable.
[0]: High Z. **[1]:** Enable.

GIO1S [2:0]: GIO1 pin function select.

GIO1S	TX state	RX state
[000]	INT (Interrupt)	
[001]	WTR (Wait until TX or RX finished)	
[010]	WOR	
[011]	SDO (4 wires SPI data out)	
[100]	EOAC (end of access code)	FSYNC (frame sync)
[101]	TMEO (TX modulation enable)	CD (carrier detect)
[110]	Preamble Detect Output (PMDO)	
[111]	TRXD (Direct mode)	

INT: Interrupt sources (refer to 30h).

GIO1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO1OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.13 GIO2 Pin Control Register (Address: 0Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	XTR2I	XTR2OE	--	GIO2S2	GIO2S1	GIO2S0	GIO2I	GIO2OE
Reset		1	1		0	0	1	0	1

XTR2I: XTR2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

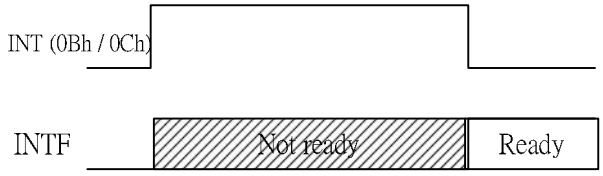
XTR2OE: XTR2 pin Output Enable.
[0]: High Z. **[1]:** Enable.

GIO2S [2:0]: GIO2 pin function select.

GIO2S	TX state	RX state
[000]	INT	
[001]	WTR (Wait until TX or RX finished)	
[010]	Wake up signal	
[011]	SDO (4 wires SPI data out)	
[100]	EOAC (end of access code)	FSYNC (frame sync)
[101]	TMEO (TX modulation enable)	CD (carrier detect)
[110]	Preamble Detect Output (PMDO)	
[111]	TRXD	

INT: Interrupt Soucrs (refer to 30h).

IST (30h)	INT	INTF (30h)	Note
IST[2:0]=0	none	none	
IST[2:0]=1	**WTR**	**CRCF**	
IST[2:0]=2	CSMA_CA	CSMAF	
IST[2:0]=3	CCA	CCAF	
IST[2:0]=4	ART	Reserved	
IST[2:0]=5	**ED**	none	
IST[2:0]=6	CCM	MICF	
IST[2:0]=7	Reserved	Reserved	



GIO2I: GIO2 pin output invert.
[0]: Non-inverted output. **[1]:** Inverted output.

GIO2OE: GIO2 pin output Enable.
[0]: High Z. **[1]:** Enable.

9.2.14 XTR Pin Control Register (Address: 0Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	**XTR2S3**	**XTR2S2**	**XTR2S1**	**XTR2S0**	**XTR1S3**	**XTR1S2**	**XTR1S1**	**XTR1S0**
Reset		0	0	0	1	0	0	0	0

XTR2S [2:0]: XTR2 pin function select.

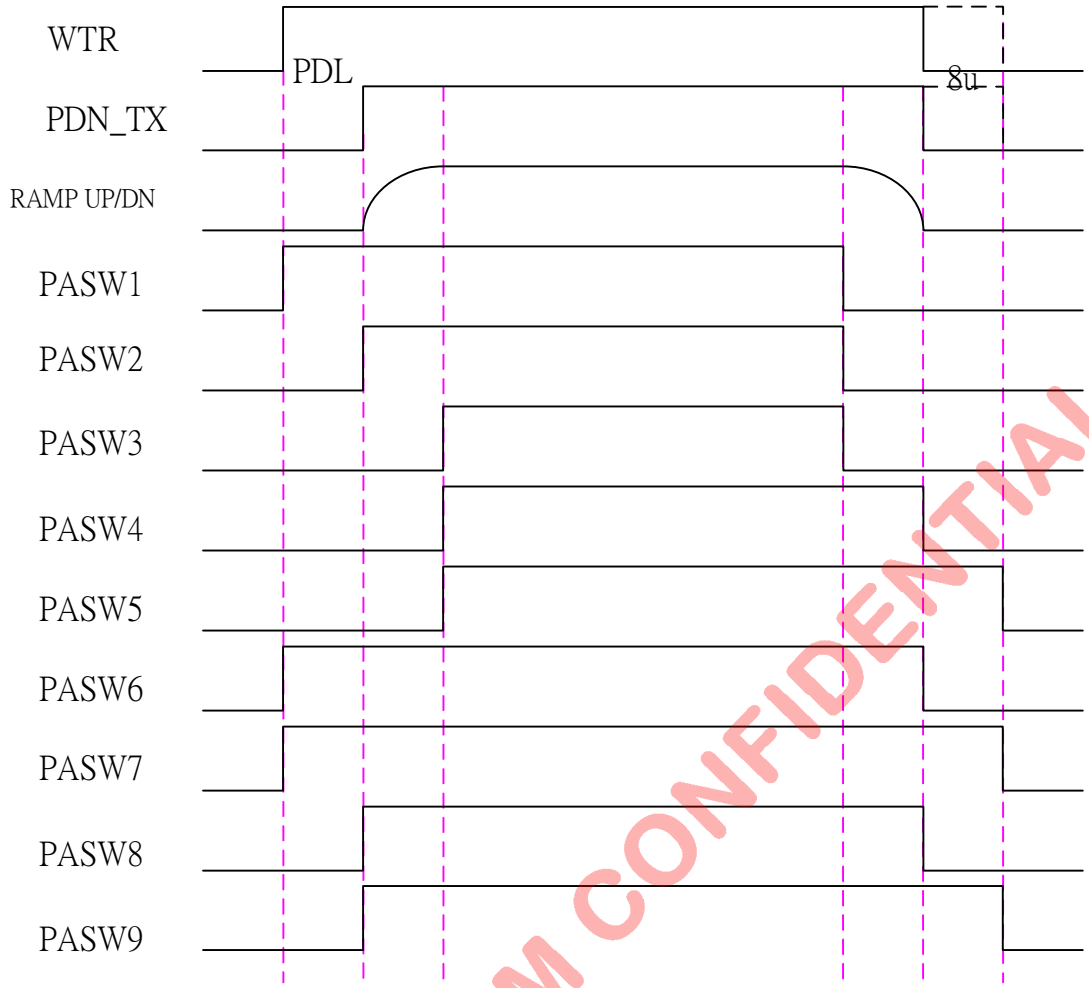
XTR2S	Function
[0000]	PDN_RX
[0001]	PDN_TX
[0010] ~ [1010]	PASW1 ~ PASW9
[1011]	VTB[0]
[1100]	In phase demodulator input (DMII)
[1101]	Internal usage

XTR1S [2:0]: XTR1 pin function select.

XTR1S	Function
[0000]	PDN_RX
[0001]	PDN_TX
[0010] ~ [1010]	PASW9 ~ PASW1
[1011]	VTB[1]
[1100]	Quadrature phase demodulator input (DMQI)
[1101]	Internal usage

EOFF: EOP, EOVBC, EOFBC, EOADC, EOVCC, EOVDC, EORSSC, OKADC, EOAGC (Internal usage only).

Recommend XTR1S = [0000] for PDN_RX.
Recommend XTR2S = [1001] for PSAW8.



9.2.15 Data Rate Clock Register (Address: 0Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	SDR1	SDR0	GRC3	GRC2	GRC1	GRC0	CGFS1	CGFS0
Reset		1	0	0	1	1	1	0	1

SDR [1:0]: Data rate setting.

SDR [1:0]	Data Rate	Chip Rate (DSSS)
[00]	Reserved	Reserved
[01]	1 Mbps	125 Kcps
[10]	2 Mbps	250 Kcps
[11]	3 Mbps	375 Kps

GRC [3:0]: Generator Reference Counter
GRC is used to get internal 2 MHz Clock Generator Reference (F_{CGR}) for different Xtal frequency.

External Crystal (F_{XREF})	Clock Generation Reference (CGR)	GRC [3:0]
16 MHz	Must be 2 MHz	[0111]
12 MHz	Must be 2 MHz	[0101]
8 MHz	Must be 2 MHz	[0011]

CGFS [1:0]: Clock generator frequency select. Recommed CGFS = [01].
[00]: Reserved. **[01]:** 32MHz. **[10]:** 48MHz. **[11]:** 64MHz.

9.2.16 PLL Register I (Address: 0Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	CHN7	CHN6	CHN5	CHN4	CHN3	CHN2	CHN1	CHN0
Reset		0	1	1	0	0	1	0	0

CHN [7:0]: RF Channel Number.

9.2.17 TX Register I (Address: 10h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	PADL	TXDI	TME	TRAMP	FDP2	FDP1	FDP0
Reset			0	0	1	0	1	1	1

PADL: Embedded PA off delay.
[0]: 8us. **[1]:** 0us.

TXDI: TX data invert. Recommend TXDI = [0].
[0]: Non-invert. **[1]:** Invert.

TME: TX modulation enable.
[0]: Disable. **[1]:** Enable.

TRAMP: Embedded PA rampup time.
[0]: 8us. **[1]:** 16us.

FDP [2:0]: Frequency deviation power setting. Recommend FDP = [111].

9.2.18 TX Register II (Address: 11h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		0	1	0	0	0	0	0	0

FD [7:0]: Frequency deviation setting. Recommend FD = [0x40]
Frequency deviation:
$F_{DEV} = F_{PFD} \times 127 \times (FD\ [7:0] + 1) \times 2^{(FDP\ [2:0] + 1)} / 2^{26}$.

Recommend F_{DEV} = 500 KHz.

9.2.19 RX Register (Address: 12h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	IGCR	MGCR	RCP2	RCP1	RCP0	DMG	RXDI	ULS
Reset		1	1	0	1	0	0	0	0

IGCR: IF gain control range. Recommend IGCR = [0].
[0]: 0dB to -12dB. **[1]:** -6dB to -12dB.

MGCR: Mixer gain control range. Recommend MGCR = [1].
[0]: 0dB to -24dB. **[1]:** 0dB to -18dB.

RCP [2:0]: Turbo mode recovery clock position. Recommend RCP = [010].

DMG: Reserved for internal usage only. It should be set to [0].

RXDI: RX data output invert. Recommend RXDI = [0].
[0]: Non-inverted output. **[1]:** Inverted output.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band. **[1]:** Low side band.

9.2.20 RX Gain Register I (Address: 13h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R/W	IGS1	IGS0	LGS2	LGS1	LGS0	MGS2	MGS1	MGS0
Reset		0	0	0	0	0	0	0	0

IGS [1:0]: IF gain select.
[00]: 0dB. **[01]:** -6dB. **[1X]:** -12dB.

MGS [2:0]: Mixer gain attenuation select. Recommend MGS = [000].
[000]: 0dB. **[001]:** -6dB. **[010]:** -12dB. **[011]:** -18dB. **[1XX]:** -24dB.

LGS [2:0]: LNA gain attenuation select. Recommend LGS = [000].
[000]: 0dB. **[001]:** -6dB. [**010]:** -12dB. **[011]:** -18dB. **[100]:** -24dB. **[101]** ~ **[111]:** -30dB.

9.2.21 RX Gain Register II (Address: 14h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0
Reset		0	0	0	0	0	0	0	0

RH [7:0]: RSSI high level calibration value.

9.2.22 RX Gain Register III (Address: 15h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
	W	RSSL7	RSSL6	RSSL5	RSSL4	RSSL3	RSSL2	RSSL1	RSSL0
Reset		0	0	0	1	1	0	0	1

RL [7:0]: RSSI low level calibration value (read only).

RSSL [7:0]: RSSI slope (write only).

9.2.23 RX Gain Register IV (Address: 16h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	RU7	RU6	RU5	RU4	RU3	RU2	RU1	RU0
	W	AGCS1	AGCS0	--	VRSEL	MHC	LHC1	LHC0	AGCE
Reset		1	0	--	0	1	0	1	1

RU [7:0]: RSSI upper level calibration value.

AGCS [1:0]: AGC stop mode. Recommend AGCS = [10].
[00]: Non-stop. **[01]:** Stop by PRAOK. **[10]:** Stop by FSYNC. **[11]:** AGC test mode.

VRSEL: AGC reference voltage select. Recommend VRSEL = [0].
[0]: Low voltage. **[1]:** High voltage.

MHC: Mixer Current Control. It should be set to [1].

LHC[1:0]: LNA Current Control. It should be set to [01].

AGCE: AGC enable. Recommend AGCE = [1].
[0]: Disable. **[1]:** Enable.

9.2.24 ADC Register (Address: 17h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
	W	CDTH7	CDTH6	CDTH5	CDTH4	CDTH3	CDTH2	CDTH1	CDTH0
Reset		0	0	0	0	0	0	0	0

CDTH [7:0]: Carrier detect threshold (write only).

ADC [7:0]: ADC digital output value (read only).

ADC input voltage= 0.3 + 1.2 * ADC [7:0] / 256 V.

9.2.25 ADC Control Register (Address: 18h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	CDM	ADCOM1	ADCOM0	MRSSL	XADS	AVGS1	AVGS0

Reset			1	1	1	0	0	1	1

CDM: CD margin = CDTH – CDTL. Recommend CDM = [1].
[0]: 6 LSB. **[1]:** 12 LSB.

ADCOM: ADC output mode. Recommend ADCOM = [10].
[00]: Single mode.
[01]: Average mode (2, 4, 8, 16 average is according to AVGS [1:0] (18h).
[10]: ED. No hold.
[11]: ED. Hold after sync 128us.

MRSSL: Reserved for internal usage only. It should be set to [0].

XADS: ADC Source Input.
[0]: RSSI. **[1]:** External voltage.

AVGS [1:0]: ADC average mode. Recommend AVGS = [11].
[00]: 2. **[01]:** 4. **[10]:** 8. **[11]:** 16.

Please note that AVGS = [11] during VBC, VDC and RSSI calibration.

9.2.26 IF Calibration Register I (Address: 19h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	FBCF	FB3	FB2	FB1	FB0
	W	IFHCM	IFTS	--	MFBS	MFB3	MFB2	MFB1	MFB0
Reset		0	0	--	0	0	1	1	1

IFHCM: Reserved for internal usage only. It should be set to [0].

IFTS: Reserved for internal usage only. It should be set to [0].

MFBS: IF filter calibration select. Recommend MFBS = [0].
[0]: Auto. **[1]:** Manual.

MFB [3:0]: IF filter manual calibration value.

FBCF: IF filter calibration flag.
[0]: Pass. **[1]:** Fail.

FB [3:0]: IF filter calibration result (read only).
Auto calibration result when MFBS = 0.
Manual calibration result when MFBS = 1.

9.2.27 VCO Current Calibration Register (Address: 1Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
	W	--	VCCS1	VCCS0	MVCS	VCOC3	VCOC2	VCOC1	VCOC0
Reset		--	1	0	0	0	1	0	0

VCCS [1:0]: VCO current calibration value select. It should be set to [10].
[00]: 0.6mA. **[01]:** 0.8mA. **[10]:** 1.0mA. [**11]:** 1.2mA.

MVCS: VCO current calibration select. Recommend MVCS = [0].
[0]: Auto. **[1]:** Manual.

VCOC [3:0]: VCO current manual calibration value.
VCO current manual setting when MVCS = 1.

VCCF: VCO current calibration flag.
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO current calibration value (read only).
Auto calibration result when MVCS = 0.
Manual calibration result when MVCS = 1.

9.2.28 VCO Bank Calibration Register I (Address: 1Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Name	R	--	--	--	--	VBCF	VB2	VB1	VB0
	W	LPFT1	LPFT0	LPFS	MDAGS	MVBS	MVB2	MVB1	MVB0
Reset		0	1	0	0	0	1	0	0

LPFT [1:0]: Loop Filter. It should be set to [01].
[00]: R1=22.0K, C1=21.5pF.
[01]: R1=11.0K, C1=43.0pF.
[10]: R1= 7.3K, C1=64.5pF.
[11]: R1= 5.5K, C1=86.0pF.

LPFS: Loop Filter Select. It should be set to [0].
[0]: Internal. **[1]:** External.

MDAGS: DAG calibration select. Recommend MDAGS = [0].
[0]: Auto. **[1]:** Manual.

MVBS: VCO bank calibration select. Recommend MVBS = [0].
[0]: Auto. **[1]:** Manual.

MVB [2:0]: VCO band manual calibration value.
VCO band manual setting when MVBS = 1.

VBCF: VCO band calibration flag.
[0]: Pass. **[1]:** Fail.

VB [2:0]: VCO bank calibration value (read only).
Auto calibration result when MVBS = 0.
Manual calibration result when MVBS = 1.

9.2.29 VCO Bank Calibration Register II (Address: 1Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADAG7	ADAG6	ADAG5	ADAG4	ADAG3	ADAG2	ADAG1	ADAG0
	W	MDAG7	MDAG6	MDAG5	MDAG4	MDAG3	MDAG2	MDAG1	MDAG0
Reset		1	0	0	0	0	0	0	0

MDAG [7:0]: DAG manual calibration value. Recommend MDAG = [0x80].

ADAG [7:0]: DAG auto calibration result (read only).

9.2.30 VCO Deviation Calibration Register I (Address: 1Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	DEVA7	DEVA6	DEVA5	DEVA4	DEVA3	DEVA2	DEVA1	DEVA0
	W	DEVS3	DEVS2	DEVS1	DEVS0	DAMR_M	VMTE_M	VMS_M	MSEL
Reset		0	0	1	1	0	0	0	0

DEVS [3:0]: Deviation output scaling. Recommend DEVS = [0011].

DAMR_M: DAMR manual enable. Recommend DAMR_M = [0].
[0]: Disable. **[1]:** Enable.

VMTE_M: VMT manual enable. Recommend VMTE_M = [0].
[0]: Disable. **[1]:** Enable.

VMS_M: VM manual enable. Recommend VMS_M = [0].
[0]: Disable. **[1]:** Enable.

MSEL: VCO control select. Recommend MSEL = [0].
[0]: Auto control for VMS /VMTE / DAMR. **[1]:** Manual control for VMS /VMTE / DAMR.

DEVA [7:0]: VCO Deviation result.
Auto calibration result when MVDS = 0. (1Fh)
Manual calibration result when MVDS = 1. (1Fh)
Where auto calibration result is ((ADEV / 8) × (DEVS + 1)).

9.2.31 VCO Deviation Calibration Register II (Address: 1Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Name	R	ADEV7	ADEV6	ADEV5	ADEV4	ADEV3	ADEV2	ADEV1	ADEV0
	W	MVDS	MDEV6	MDEV5	MDEV4	MDEV3	MDEV2	MDEV1	MDEV0
Reset		0	0	0	1	1	0	1	1

MVDS: VCO deviation calibration select. Recommend MVDS = [0].
[0]: Auto. **[1]:** Manual.

MDEV [6:0]: VCO deviation manual calibration value.

ADEV [7:0]: VCO deviation auto calibration value.

9.2.32 VCO Modulation Delay Register (Address: 1Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	DEVFD2	DEVFD1	DEVFD0	DEVD2	DEVD1	DEVD0
Reset		--	--	0	0	0	0	1	1

DEVFD [2:0]: Reserved for internal usage only. It should be set to [000].
8XDR (8X2=16M).

DEVD [2:0]: Reserved for internal usage only. It should be set to [011].
XCPCK(16M).

9.2.33 Channel Select Register (Address: 20h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CHI3	CHI2	CHI1	CHI0	CHD3	CHD2	CHD1	CHD0
Reset		0	0	1	1	0	1	1	1

CHI [3:0]: Auto IF offset channel number setting.
If F_{CHSP} = 500 KHz, recommend **CHI = [0011]**.
F_{CHSP} × (CHI + 1) = 2MHz.

CHD [3:0]: Channel frequency offset for deviation calibration.
If F_{CHSP} = 500 KHz, recommend **CHD = [0111]**.
Where Offset channel number = +/- (CHD + 1).

9.2.34 Battery Detect Register (Address: 21h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	--	--	--	--	BDF		--	--
	W	ATP2	ATP1	ATP0	ECE	BLE	BDS1	BDS0	BDE
Reset		0	1	0	0	0	1	0	0

ATP [2:0]: Analog Test Pin. Recommend ATP= [000].

ATP [2:0]	BP_BG	BP_RSSI
[000]	Band-gap voltage	RSSI voltage
[001]	Analog temperature voltage	RSSI voltage
[010]	Band-gap voltage	External ADC input source
[011]	Analog temperature voltage	External ADC input source
[100]	BPF positive in phase output	BPF negative in phase output
[101]	BPF positive quadrature phase output	BPF negative in phase output
[110]	BPF positive in phase output	BPF negative quadrature phase output
[111]	BPF positive quadrature phase output	BPF negative quadrature phase output

ECE: External Regulator enable. Recommend ECE = [0].
[0]: Disable. **[1]:** Enable.

BLE: Battary life extension. Reserved for internal usage.

BDF: Battery detection flag.
[0]: Low Battery. **[1]:** High Battery.

BDS[1:0]: Battery detection threshold.
[00]: 2.0V. **[01]:** 2.2V. [**10]:** 2.4V. **[11]:** 2.6V.

When REGI < Threshold, BDF= low.
When REGI > Threshold, BDF= high.

BDE: Battery detection enable.
[0]: Disable. **[1]:** Enable.

9.2.35 TX test Register (Address: 22h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	TXCS	PAC1	PAC0	TBG2	TBG1	TBG0
Reset		--	--	0	0	0	1	1	0

TXCS: TX Current Setting.

PAC [1:0]: PA Current Setting.

TBG [2:0]: TX Buffer Setting.

Outputpower (dBm)	Recommend setting			Typical TX current (mA)
	TXCS	TBG	PAC	
3.5	1	7	3	21
0	0	6	0	15

9.2.36 RX LQI Register I (Address: 23h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	LQI7	LQI6	LQI5	LQI4	LQI3	LQI2	LQI1	LQI0
	W	--	--	DCM1	DCM0	LQICE	ARSSI	AIF	LQIE
Reset		--	--	0	1	0	1	1	0

DCM[1:0] : Demodulator DC estimation mode. Recommend DCM = [01].
[00]: Fix mode (For ±10 ppm crytal accuracy only). DC level is set by DCV [7:0].
[01]: 32 bits average before frame sync, hold after frame sync.
[1X]: 32 bits average before frame sync and then become 128 bits average after frame sync.

LQICE: LQI Counter enable for WOR, ATRE, RX timeout.
[0]: Disable. **[1]:** Enable.

ARSSI: Auto RSSI measurement whenever in RX mode. Recommend ARSSI = [1].
[0]: Disable. **[1]:** Enable.

AIF: Auto IF. Recommend AIF = [1].
[0]: Disable. [1]: Enable.

RF LO frequency will auto offset one IF frequency whenever entering to RX mode.

LQIE: LQI enable. Recommend LQIE = [1].
[0]: Disable. **[1]:** Enable.

LQI [7:0]: Link quality indication (read only).
LQI=0x00, low link quality.
LQI=0xFF, high link quality.

A7153's LQI calucatiton is implemented by 32-Packets Moving Average.
LQI = (1 – PER) x 256, where LQI initial value is 0xFF and PER stands for Packet Errorr Rate.

9.2.37 RX DEM DC Register II (Address: 24h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0
	R	DCO7	DCO6	DCO5	DCO4	DCO3	DCO2	DCO1	DCO0
Reset		1	0	0	0	0	0	0	0

DCV [7:0]: Demodulator fix mode DC value. Recommend DCV = [0x80].

DCO[7:0]: DC average output (read only).

9.2.38 Charge Pump Current Register (Address: 25h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CPM3	CPM2	CPM1	CPM0	CPT3	CPT2	CPT1	CPT0
Reset		1	1	1	1	0	0	1	1

CPM [3:0]: Charge pump current setting for VM loop. Recommend CPM = [1111].
Charge pump current = (CPM + 1) / 16 mA.

CPT [3:0]: Charge pump current setting for VT loop. Recommend CPT = [0011].
Charge pump current = (CPT + 1) / 16 mA.

9.2.39 Crystal test Register (Address: 26h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	CGS	XS	XCL3	XCL2	XCL1	XCL0	XCC	XCP
Reset		1	1	1	0	1	0	1	1

CGS: Clock generator select. Recommend CGS = [1].
[0]: By pass clock generator. **[1]:** Use clock generator.

XS: Crystal oscillator select. Recommend XS = [1].
[0]: Use external clock. **[1]:** Use external crystal.

XCL [3:0]: Reserved for internal usage only. It should be set to [1010].

XCC: Reserved for internal usage only. It should be set to [1].

XCP : Reserved for internal usage only. It should be set to [1].

9.2.40 PLL test Register (Address: 27h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	CPS	PRRC1	PRRC0	PRIC1	PRIC0	SDPW	NSDO
Reset		--	1	0	1	0	0	0	1

CPS: Reserved for internal usage only. It should be set to [1].

PRRC [1:0]: Reserved for internal usage only. It should be set to [01].

PRIC [1:0]: Reserved for internal usage only. It should be set to [00].

SDPW: Reserved for internal usage only. It should be set to [0].

NSDO: Reserved for internal usage only. It should be set to [1].

9.2.41 VCO test Register (Address: 28h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	CPCH1	CPCH0	RLB1	RLB0	VCBS1	VCBS0
Reset		--	--	0	0	0	0	1	0

CPCH [1:0]: Charge pump high current. It should be set to [00].

RLB [1:0]: LO RX Buffer current. It should be set to [00].
[00]:1.2mA. **[01]:**1.5mA. **[10]:** 1.8mA. **[11]:** 2.1mA.

VCBS [1:0]: VCO Buffer current Select. Recommend VCBS = [10].
[00]: 0.6mA. **[01]:** 0.8mA. **[10]:** 1.0mA. **[11]:** 1.2mA.

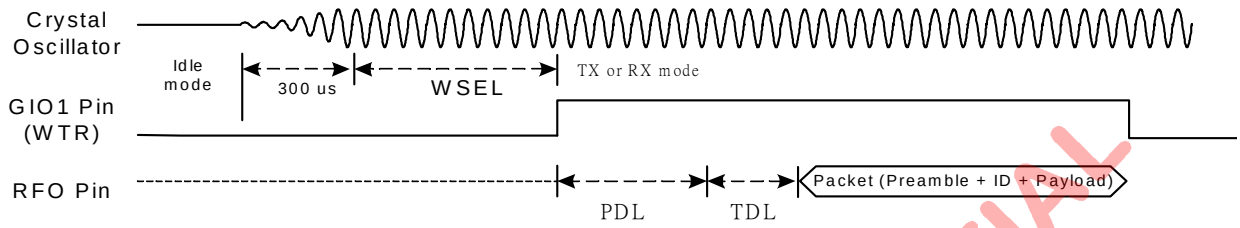
9.2.42 Delay Register (Address: 29h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	WD	WSEL1	WSEL0	PDL1	PDL0	TDL2	TDL1	TDL0

Reset		0	1	0	1	0	1	0	0

WD: Wait delay for SLOT mode. Recommend WD = [0].
[0]: 5-BOTS. **[1]:** 6-BOTS.
Where BOTS is Back-off timer.

WSEL [1:0]: XTAL settling delay (0us ~ 600us). Recommend WSEL = [11].
[00]: 0us. **[01]:** 200us. **[10]:** 400us. **[11]:** 600us.



PDL [1:0]: PLL Settling Delay. Recommend PDL = [10].
[00]: 0us. **[01]:** 16us. **[10]:** 32us. **[11]:** 48us.

TDL [2:0]: TRX Settling Delay. Recommend TDL = [100].
[000]: 0us. **[001]:** 16us. **[010]:** 32us. **[011]:** 48us. **[100]:** 64us. **[101]:** 80us. **[110]:** 96us. **[111]:** 112us.

9.2.43 ACK Delay Register (Address: 2Ah)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	AGC_DLY 1	AGC_DLY 0	RS_DLY1	RS_DLY0	ACKD3	ACKD2	ACKD1	ACKD0
Reset		0	0	0	1	1	0	0	0

AGC_DLY [1:0]: AGC Settling Delay (4us ~ 16us). Recommend AGC_DLY = [00].
[00]: 4us. **[01]:** 8us. **[10]:** 12us. **[11]:** 16us.

RS_DLY [1:0]: RSSI Measurement Delay (10us ~ 40us). Recommend RS_DLY = [01].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

ACKD [3:0]: Auto-ACK Delay. Recommend ACKD = [1000] for 128 us.
Delay= 16 * (ACKD [3:0]) us.

Based on IEEE802.15.4, ACK Packet shall be replied within **192 us** after receiving the ACK request package.

9.2.44 ART Delay Register I (Address: 2Bh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RTD 3	RTD 2	RTD 1	RTD 0	TRD 3	TRD 2	TRD 1	TRD 0
Reset		0	0	0	0	1	0	0	0

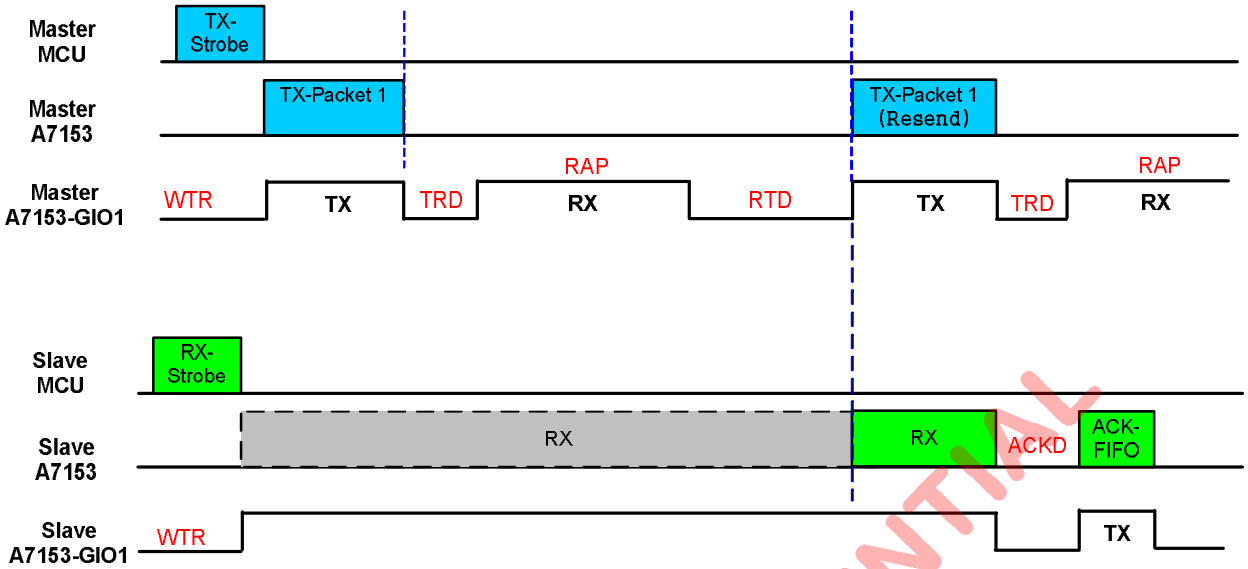
RTD [3:0]: Delay from TX to RX of Auto-resend function.
Delay= 16 * (RTD [3:0]) us.

TRD [3:0]: Delay from RX to TX of Auto-resend function.
Delay= 16 * (TRD [3:0]) us.

9.2.45 ART Delay Register II (Address: 2Ch)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	RAP 7	RAP 6	RAP 5	RAP 4	RAP 3	RAP 2	RAP 1	RAP 0
Reset		0	0	0	1	1	1	0	1

RAP [7:0]: RX Acitve Period of Auto-resend function.
Delay= 16 * (**RAP** [7:0]) us.



9.2.46 CSMA Register I (Address: 2Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ATLP2	ATLP1	ATLP0	CST1	CST0	MaxNB2	MaxNB1	MaxNB0
Reset		0	1	1	0	0	1	0	0

ATLP [2:0]: Loop times for auto resend algorithm.

CST[1:0]: Carrier sense time. Recommend CST = [00].
[00]:128us. **[01]:**160us. **[10]:** 192us. **[11]:**224us.

MaxNB [2:0]: Loop times for CSMA-CA algorithm.

9.2.47 CSMA Register II (Address: 2Eh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	MaxBE3	MaxBE2	MaxBE1	MaxBE0	MinBE3	MinBE2	MinBE1	MinBE0
Reset		0	1	0	1	0	0	1	1

MaxBE [3:0]: Maxmum back-off exponent in CSMA-CA algorithm.

MinBE [3:0]: Minimum back-off exponent in CSMA-CA algorithm.

9.2.48 Pre_TRX setting Register (Address: 2Fh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	--	--	--	--	PTRS3	PTRS2	PTRS1	PTRS0
Reset		--	--	--	--	0	0	0	0

PTRS [3:0]: Pre_TRX setting. Recommend PTRS = [0000].

9.2.49 Interrupt State Register (Address: 30h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	ISTRN	--	CCAM1	CCAM0	EDS	CCAS	ERX	--
	R	INT	ST2	ST1	ST0	EDS	CCAS	ERX	INTF
Reset		0	--	0	1	0	0	0	--

ISTRN: Interrupt state reset. (write only). Recommend ISTRN = [0].
[1]: Reset interrupts sources. Auto clear when done.

CCAM[1:0]: CCA mode. Recommend CCAM = [00].
[00]: CCAF=1, when RSSI > RTH, and detect pramble frame.

[01]: CCAF=1, when RSSI > RTH.
[10]: CCAF=1, when detect pramble frame.
[11]: CCAF=1, when RSSI > RTH or detect pramble frame.

EDS: Energe detect. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

CCAS: CCA function. (Auto clear when done).
[0]: Disable. **[1]:** Enable.

ERX: RX Behaviour.
[0]: Normal RX.
[1]: For CCA and ED. When CCA or ED is done, auto back to previouse state (i.e. Standby or PLL mode).

INT: Interrupt source state.
[0]: None. **[1]:** Busy.

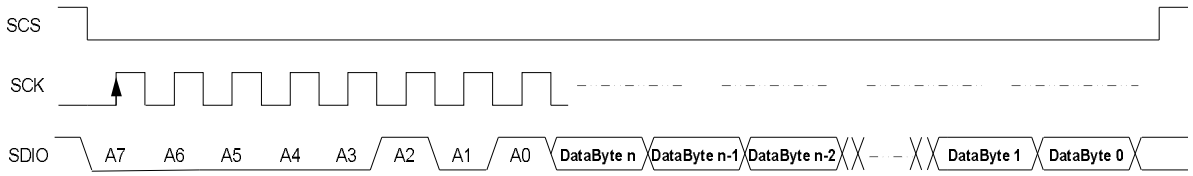
IST[2:0]: Interrupt source select.

IST[2:0]	Interrupt source	INTF (Bit 0)	Note
000	none	none	
001	WTR	CRCF	
010	CSMA_CA	CSMAF	
011	CCA	CCAF	
100	ART	Reserved	
101	EDM	None	
110	CCM	MICF	
111	Reserved	Reserved	

LONG REGISTERS

Addr 31h~3Eh	Long Registers (> 16 bits) High Byte and MSB First

In Long registers, all bytes via SPI R/W are High Byte and MSB first as shown below.



9.2.50 ADF control Register (Address: 31h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	**FADDE**	**ACBEN**	**ACDAT**	**ACACK**	**ACCMD**	**ACRES**	**PCORR**	**MAXVER1**
Reset		1	1	1	1	1	1	0	0
Name	W	**MAXVER0**	**RESMUX2**	**RESMUX1**	**RESMUX0**	**--**	**--**	**--**	**--**
Reset		1	0	0	0	--	--	--	--

FADDE: MAC Address Filtering.
[0]: Disable. **[1]:** Enable.

ACBEN: Accept Beacon frame type (0)
[0]: Reject. **[1]:** Accept.

ACDAT: Accept Data frame type (1)
[0]: Reject. **[1]:** Accept.

ACACK: Accept Ack frame type (2)
[0]: Reject. **[1]:** Accept.

ACCMD: Accept MAC command frame type (3)
[0]: Reject. **[1]:** Accept.

ACRES: Accept Reserved frame type (4,5,6,7)
[0]: Reject. **[1]:** Accept.

PCORR: PAN Corrdinator.
[0]: End device. **[1]:** Corrdinator.

MAXVER: Max frame version. Recommend MAXVER = [01].

RESMUX: FCF reserved bit mask. Recommend RESMUX = [000].

9.2.51 ADF Frame Register (Address: 32h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
	W	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
	W	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8
	W	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
	W	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56
	W	LADD55	LADD54	LADD53	LADD52	LADD51	LADD50	LADD49	LADD48
	W	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40
	W	**LADD39**	**LADD38**	**LADD37**	**LADD36**	**LADD35**	**LADD34**	**LADD33**	**LADD32**
	W	**LADD31**	**LADD30**	**LADD29**	**LADD28**	**LADD27**	**LADD26**	**LADD25**	**LADD24**
	W	**LADD23**	**LADD22**	**LADD21**	**LADD20**	**LADD19**	**LADD18**	**LADD17**	**LADD16**
	W	**LADD15**	**LADD14**	**LADD13**	**LADD12**	**LADD11**	**LADD10**	**LADD8**	**LADD8**
	W	**LADD7**	**LADD6**	**LADD5**	**LADD4**	**LADD3**	**LADD2**	**LADD1**	**LADD0**
Reset		1	1	1	1	1	1	1	1

PID[15:0]: PAN ID Storage.
PID [15:0]: Store PAN_ID for frame filtering.
Default : 0xFFFF.

SADD[15:0]: Short Adderss Storage.
SADD [15:0]: Store Short address for frame filtering.
Default : 0xFFFF.

LADD[63:0]: Long Address Storage.
LADD [63:0]: Store Long address for frame filtering.
Default : 0xFFFF-FFFF-FFFF-FFFF.

Refer to Chapter 13 for frame filtering.

9.2.52 ADHL Register (Address: 33h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	R	ADH7	ADH6	ADH5	ADH4	ADH3	ADH2	ADH1	ADH0
Reset		0	0	0	0	0	0	0	0
Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	ADL7	ADL6	ADL5	ADL4	ADL3	ADL2	ADL1	ADL0
Reset		0	0	0	0	0	0	0	0

ADH[7:0]: AD high level calibration result.

ADL[7:0]: AD low level calibration result.

9.2.53 ACK Frame Control Register (Address: 34h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	W	AFCF7	AFCF6	AFCF5	AFCF4	AFCF3	AFCF2	AFCF1	AFCF0
Reset		0	0	0	0	0	0	1	0
Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	AFCF15	AFCF14	AFCF13	AFCF12	AFCF11	AFCF10	AFCF9	AFCF8
Reset		0	0	0	0	0	0	0	0

AFCF[15:0]: ACK Frame Control Field.
AFCF [15:0] shall be filled in advance based on IEEE 802.15.4 Frame Control Field when ACKS =1 (02h).

9.2.54 PNG Register (Address: 35h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	R	PNO15	PNO14	PNO13	PNO12	PNO11	PNO10	PNO9	PNO8
	W	PNIV15	PNIV14	PNIV13	PNIV12	PNIV11	PNIV10	PNIV9	PNIV8
Reset		0	1	1	1	0	0	0	1
Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	R	PNO7	PNO6	PNO5	PNO4	PNO3	PNO2	PNO1	PNO0
	W	PNIV7	PNIV6	PNIV5	PNIV4	PNIV3	PNIV2	PNIV1	PNIV0
Reset		0	1	0	1	0	0	1	1

PNO [15:0]: 16-bits Random number generator output.

PNIV [15:0]: Intial value of 16-bits Random number generator.

9.2.55 PLL Register II (Address: 36h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W	--	--	--	--	--	--	--	BIP8
Reset		--	--	--	--	--	--	--	0
Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W	BIP7	BIP6	BIP5	BIP4	BIP3	BIP2	BIP1	BIP0
Reset		1	0	0	1	0	1	1	0

BIP [8:0]: LO frequency integer part setting. Recommend BIP = [0x0096].

9.2.56 PLL Register III (Address: 37h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W	BFP15	BFP14	BFP13	BFP12	BFP11	BFP10	BFP9	BFP8
Reset		0	0	0	0	0	0	0	0

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W	BFP7	BFP6	BFP5	BFP4	BFP3	BFP2	BFP1	BFP0
Reset		0	0	0	0	0	1	0	0

BFP [15:0]: LO frequency floating part setting. Recommend BFP = [0x0004].

9.2.57 PLL Register IV (Address: 38h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	W	--	CHR14	CHR13	CHR12	CHR11	CHR10	CHR9	CHR8
Reset		--	0	0	0	1	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	W	CHR7	CHR6	CRH5	CHR4	CHR3	CHR2	CHR1	CHR0
Reset		0	0	0	0	0	0	0	0

CHR [14:0]: Channel resolution setting. Recommend CHR = [0x0800] for 16MHz Xtal.
Defualt value of CHR [14:0] is 0.5MHz step under 16MHz Xtal.

9.2.58 Channel Group Register (Address: 39h)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	W	CHGL7	CHGL6	CHGL5	CHGL4	CHGL3	CHGL2	CHGL1	CHGL0
Reset		0	0	1	1	1	1	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	W	CHGH7	CHGH6	CHGH5	CHGH4	CHGH3	CHGH2	CHGH1	CHGH0
Reset		0	1	1	1	1	0	0	0

CHGL [7:0]: PLL channel group low boundary setting. Recommend CHGL = [0x3C].

CHGH [7:0]: PLL channel group high boundary setting. Recommend CHGH = [0x78].

PLL frequency is divided into 3 groups:

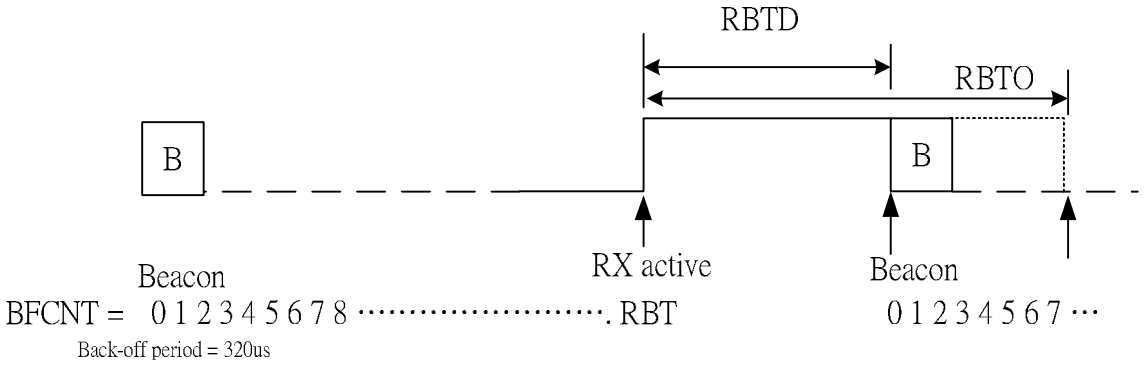
	Channel
Group1	0 ~ CHGL-1
Group2	CHGL ~ CHGH-1
Group3	CHGH ~ 255

9.2.59 Random Back Off Time-Out Register (Address: 3Ah)

Bit	R/W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Name	R	RBTD7	RBTD6	RBTD5	RBTD4	RBTD3	RBTD2	RBTD1	RBTD0
	W	RBTO7	RBTO6	RBTO5	RBTO4	RBTO3	RBTO2	RBTO1	RBTO0
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	R	RBTD15	RBTD14	RBTD13	RBTD12	RBTD11	RBTD10	RBTD9	RBTD8
	W	RBTO15	RBTO14	RBTO13	RBTO12	RBTO11	RBTO10	RBTO9	RBTO8
Reset		0	0	0	0	0	0	0	0

RBTO [15:0]: Random back off time-out in RX.
Time-out = (RBTO+1) X 320 us.

RBTD [15:0]: Random back off difference.
The difference is the value between the active position and the beacon position.



9.2.60 Random Back Off Register (Address: 3Bh)

Bit	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Name	R	BFCNT7	BFCNT6	BFCNT5	BFCNT4	BFCNT3	BFCNT2	BFCNT1	BFCNT0
	W	RBT7	RBT6	RBT5	RBT4	RBT3	RBT2	RBT1	RBT0
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Name	R	BFCNT15	BFCNT14	BFCNT13	BFCNT12	BFCNT11	BFCNT10	BFCNT9	BFCNT8
	W	RBT15	RBT14	RBT13	RBT12	RBT11	RBT10	RBT9	RBT8
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Name	R	BFCNT23	BFCNT22	BFCNT21	BFCNT20	BFCNT19	BFCNT18	BFCNT17	BFCNT16
	W	RBT23	RBT22	RBT21	RBT20	RBT19	RBT18	RBT17	RBT16
Reset		0	0	0	0	0	0	0	0

RBT [23:0]: Random back off active position. (write only)
Active time = (**RBT**+1) X 320us.

BFCNT [23:0]: Random back off counter. (read only)
It could show the position after enable back-off counter or received the beacon frame.
Each back off period is **320us**.
Use the **BFCNT** to calculate the active position (**RBT**).

9.2.61 LAMH Register (Address: 3Ch)

Bit	R/W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Name	W	Reserved	LA6	LA5	LA4	LA3	LA2	LA1	LA0
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 15**	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
	W	Reserved	LM6	LM5	LM4	LM3	LM2	LM1	LM0
Reset		0	0	0	0	0	0	0	0
Bit	**R/W**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	W	Reserved	LH6	LH5	LH4	LH3	LH2	LH1	LH0
Reset		0	0	0	0	0	0	0	0

CCM Mode needed information.

LA [6:0] : LA Length information for CCM. Bit 23 shall be written by [0].

LM [6:0] : LM Length information for CCM. Bit 15 shall be written by [0].

LH [6:0] : LH Length information for CCM. Bit 7 shall be written by [0].

9.2.62 Key Register (Address: 3Dh)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	KEY127	KEY126	KEY125	KEY124	KEY123	KEY122	KEY121	KEY120
	W	KEY119	KEY118	KEY117	KEY116	KEY115	KEY114	KEY113	KEY112
	W	KEY111	KEY110	KEY109	KEY108	KEY107	KEY106	KEY105	KEY104
	W	KEY103	KEY102	KEY101	KEY100	KEY99	KEY98	KEY97	KEY96

	W	KEY95	KEY94	KEY93	KEY92	KEY91	KEY90	KEY89	KEY88
	W	KEY87	KEY86	KEY85	KEY84	KEY83	KEY82	KEY81	KEY80
	W	KEY79	KEY78	KEY77	KEY76	KEY75	KEY74	KEY73	KEY72
	W	KEY71	KEY70	KEY69	KEY68	KEY67	KEY66	KEY65	KEY64
	W	KEY63	KEY62	KEY61	KEY60	KEY59	KEY58	KEY57	KEY56
	W	KEY55	KEY54	KEY53	KEY52	KEY51	KEY50	KEY49	KEY48
	W	KEY47	KEY46	KEY45	KEY44	KEY43	KEY42	KEY41	KEY40
	W	KEY39	KEY38	KEY37	KEY36	KEY35	KEY34	KEY33	KEY32
	W	KEY31	KEY30	KEY29	KEY28	KEY27	KEY26	KEY25	KEY24
	W	KEY23	KEY22	KEY21	KEY20	KEY19	KEY18	KEY17	KEY16
	w	KEY15	KEY14	KEY13	KEY12	KEY11	KEY10	KEY9	KEY8
	W	KEY7	KEY6	KEY5	KEY4	KEY3	KEY2	KEY1	KEY0
Reset		0	0	0	0	0	0	0	0

KEY [127:0]: KEY information for CCM.

9.2.63 NONCE Register (Address: 3Eh)

Bit		R/W	Bit 103	Bit 102	Bit 101	Bit 100	Bit 99	Bit 98	Bit 97	Bit 96
Name	Byte12	W	SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0
	Byte11	W	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
	Byte10	W	FC15	FC14	FC13	FC12	FC11	FC10	FC8	FC8
	Byte9	W	FC23	FC22	FC21	FC20	FC19	FC18	FC17	FC16
	Byte8	W	FC31	FC30	FC29	FC28	FC27	FC26	FC25	FC24
	Byte7	W	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
	Byte6	W	SA15	SA14	SA13	SA12	SA11	SA10	SA8	SA8
	Byte5	W	SA23	SA22	SA21	SA20	SA19	SA18	SA17	SA16
	Byte4	W	SA31	SA30	SA29	SA28	SA27	SA26	SA25	SA24
	Byte3	W	SA39	SA38	SA37	SA36	SA35	SA34	SA33	SA32
	Byte2	W	SA47	SA46	SA45	SA44	SA43	SA42	SA41	SA40
	Byte1	W	SA55	SA54	SA53	SA52	SA51	SA50	SA49	SA48
	Byte0	W	SA63	SA62	SA61	SA60	SA59	SA58	SA57	SA56
Reset			0	0	0	0	0	0	0	0

NONCE is 13 bytes ([103:0]) which is composed by SL[7:0], FC [31:0] and SA[63:0].

NONCE information is used for CCM* operation.

SL [7:0]: Security Level.

FC [31:0]: Frame Counter.

SA [63:0]: Source Address.

10. SPI

A7153 supports max 10Mbps SPI interface. Via SPI, user can access **Control Registers** and issue **Strobe Command**. Figure 10.1 gives an overview of SPI access manners.

A7153 can be communicated with a host microcontroller via a 3-wire or 4-wire SPI port as a slave device. For 3-wire SPI, SDIO pin is configured as bi-direction to be data input and output. For 4-wire SPI, SDIO pin is data input and GIO1 (or GIO2) pin acts as SDO.

SCS pin must be held low to enable A7153 SPI communication. For SPI write operation, SDIO pin is latched into A7153 at the rising edge of SCK. For SPI read operation, if input address is latched by A7153, data output is aligned at falling edge of SCK. Therefore, MCU can latch data output at the rising edge of SCK.

	SPI chip select	Data In	Data Out
3-Wire SPI	SCS pin = 0 (active low)	SDIO pin	SDIO pin
4-Wire SPI	SCS pin = 0 (active low)	SDIO pin	GIO1 (GIO1S=0110) GIO2 (GIO2S=0110)

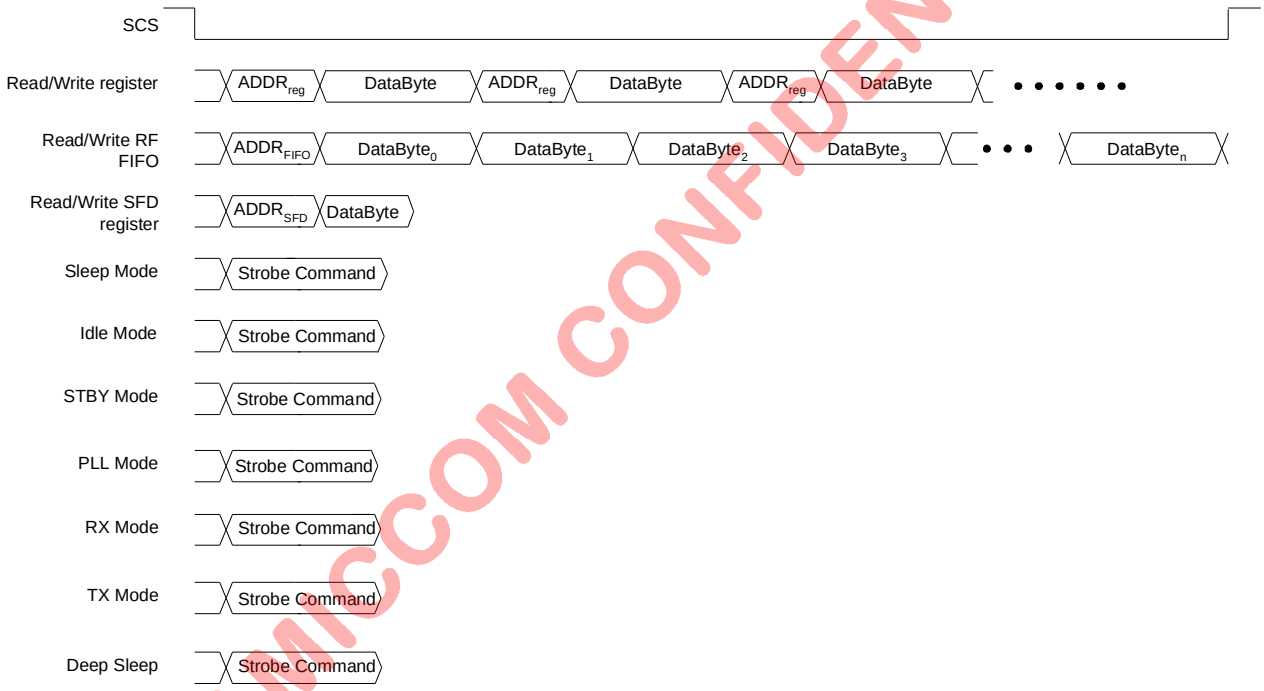


Figure 10.1 SPI Access Manners

10.1 SPI Format

The first bit (A7) is critical to indicate A7153 the following instruction wheather “Strobe command” or “control register”. See Table 10.1 for SPI format. Based on Table 10.1, if A7=0, A7153 is informed for control register accessing. So, A6 bit is used to indicate read (A6=1) or write operation (A6=0). See Figure 10.2 and Figure 10.3 for details.

Address Byte (8 bits)								Data Byte (8 bits)							
CMD	R/W	Address						Data							
A7	A6	A5	A4	A3	A2	A1	A0	7	6	5	4	3	2	1	0

Table 10.1 SPI Format

Address byte:

Bit 7: Command bit
[0]: Control register.
[1]: Strobe command.

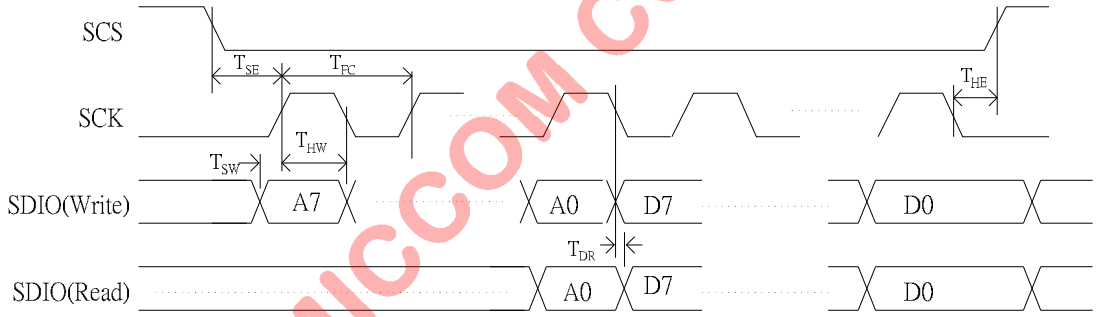
Bit 6: R/W bit
[0]: Write data to control register.
[1]: Read data from control register.

Bit [5:0]: Address of control register

Data Byte [7:0]: SPI input or output data, see Figure 10.2 and Figure 10.3 for details.

10.2 SPI Timing Characteristic

No matter 3-wire or 4-wire SPI interface, the maximum SPI data rate is 10 Mbps. To active SPI interface, SCS pin must be set to low. For correct data latching, user has to take care hold time and setup time between SCK and SDIO. See Table 10.2 for details.



Parameter	Description	Min.	Max.	Unit
F_C	FIFO clock frequency.		10	MHz
T_{SE}	Enable setup time.	50		ns
T_{HE}	Enable hold time.	50		ns
T_{SW}	TX Data setup time.	50		ns
T_{HW}	TX Data hold time.	50		ns
T_{DR}	RX Data delay time.	0	50	ns

Table 10.2 SPI Timing Characteristic

10.3 SPI Timing Chart

In this section, 3-wire and 4-wire SPI interface read / write timing are described.

10.3.1 Timing Chart of 3-wire SPI

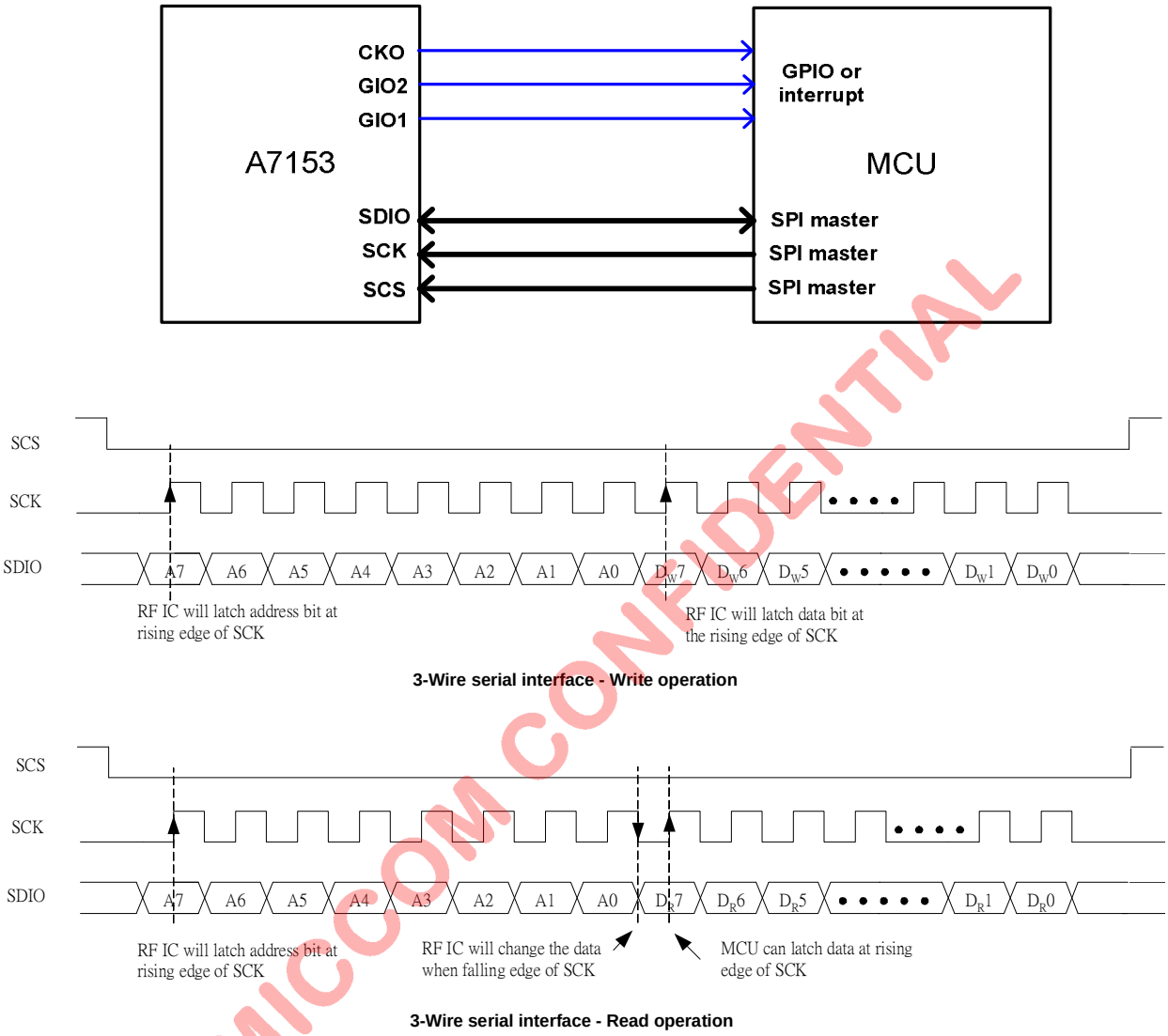
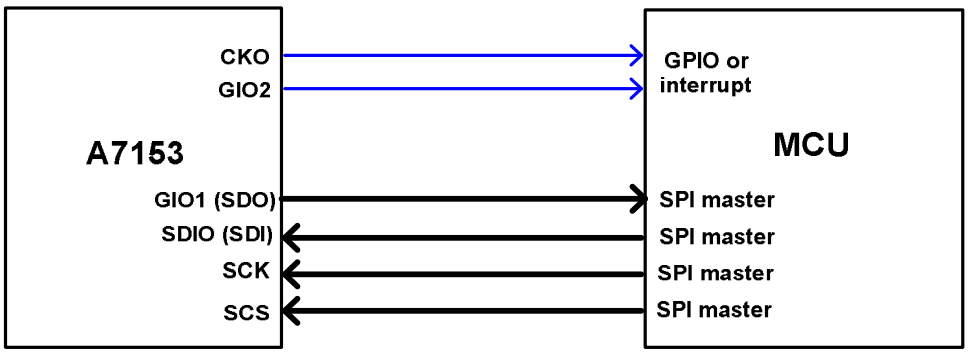


Figure 10.2 Read/Write Timing Chart of 3-Wire SPI

10.3.2 Timing Chart of 4-wire SPI



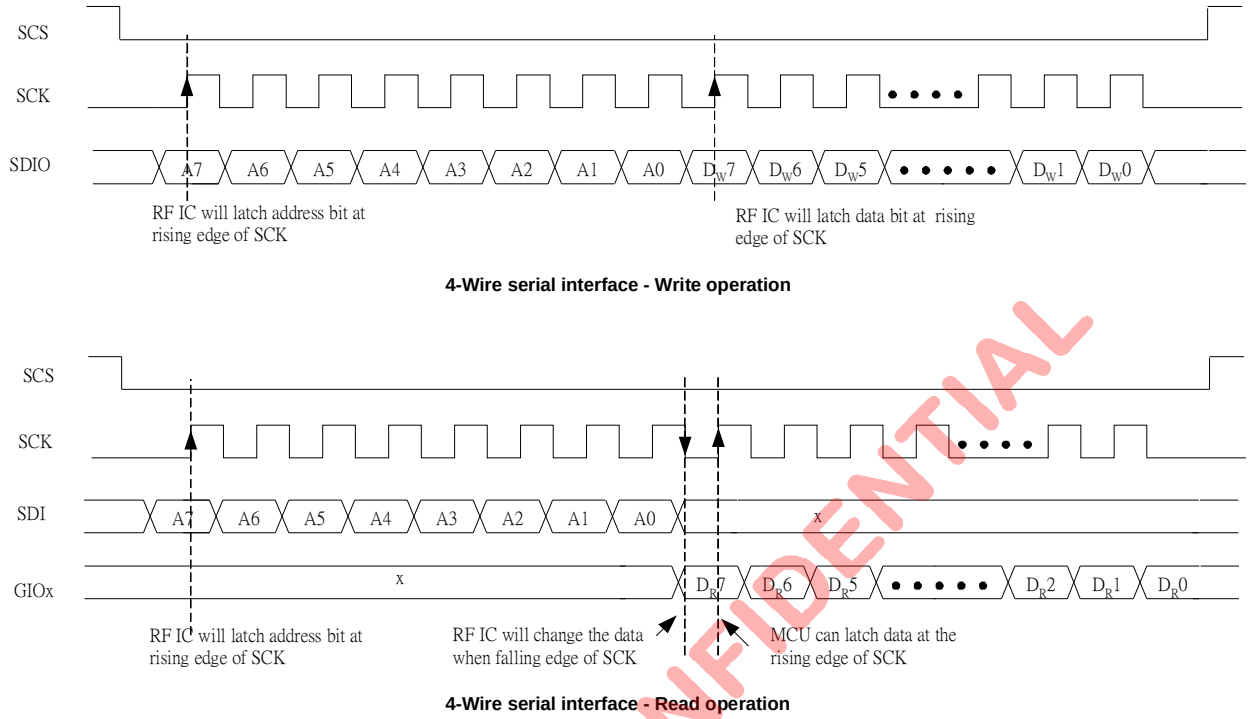


Figure 10.3 Read/Write Timing Chart of 4-Wire SPI

10.4 Strobe Commands

A7153 supports 7 Strobe commands to control internal state machine for chip's operations. Table 10.3 is the summary of Strobe commands.

Be notice, Strobe command could be defined by 4-bits (A7~A4) or 8-bits (A7~A0). If 8-bits Strobe command is selected, A3 ~ A0 are don't care conditions. In such case, SCS pin can be remaining low for asserting next commands.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode
1	0	0	1	x	x	x	x	Idle mode
1	0	1	0	x	x	x	x	Standby mode
1	0	1	1	x	x	x	x	PLL mode
1	1	0	0	x	x	x	x	RX mode
1	1	0	1	x	x	x	x	TX mode
1	0	0	0	1	0	x	x	Deep sleep mode, need re-calibration. (no data retension, GIO1, GIO2 internal pull high)
1	1	1	0	x	x	x	x	Low voltage sleep mode, no need re-calibration. (with data retension)

Table 10.3 Strobe Commands by SPI interface

10.4.1 Strobe Command - Sleep Mode

Refer to Table 10.3, user can issue 4 bits (1000) Strobe command directly to set A7153 into Sleep mode. Below are the

Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	x	x	x	x	Sleep mode

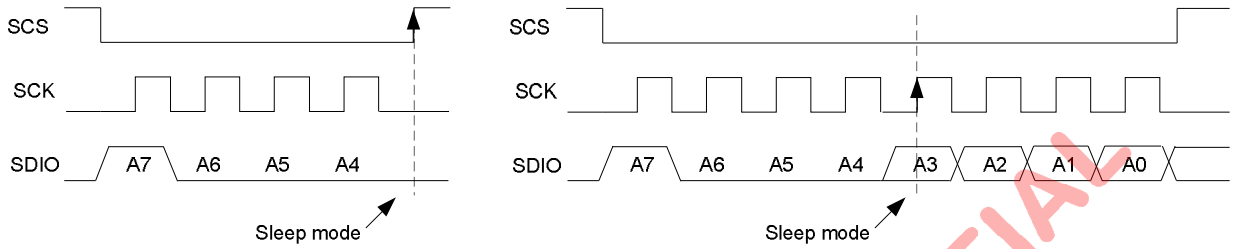


Figure 10.4 Sleep mode Command Timing Chart

10.4.2 Strobe Command - Idle Mode

Refer to Table 10.3, user can issue 4 bits (1001) Strobe command directly to set A7153 into Idle mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	1	x	x	x	x	Idle mode

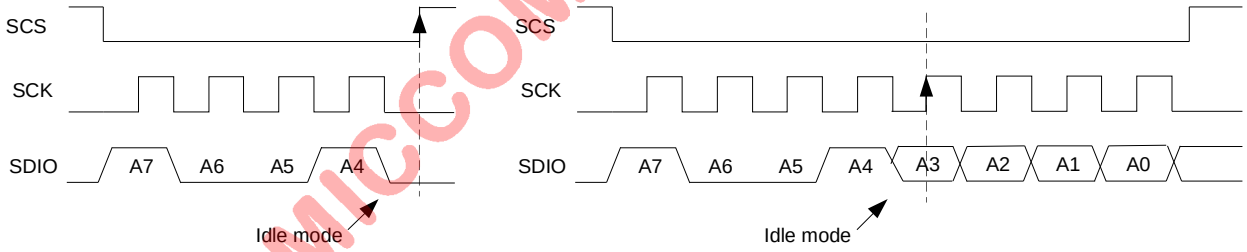


Figure 10.5 Idle mode Command Timing Chart

10.4.3 Strobe Command - Standby Mode

Refer to Table 10.3, user can issue 4 bits (1010) Strobe command directly to set A7153 into Standby mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	0	x	x	x	x	Standby mode

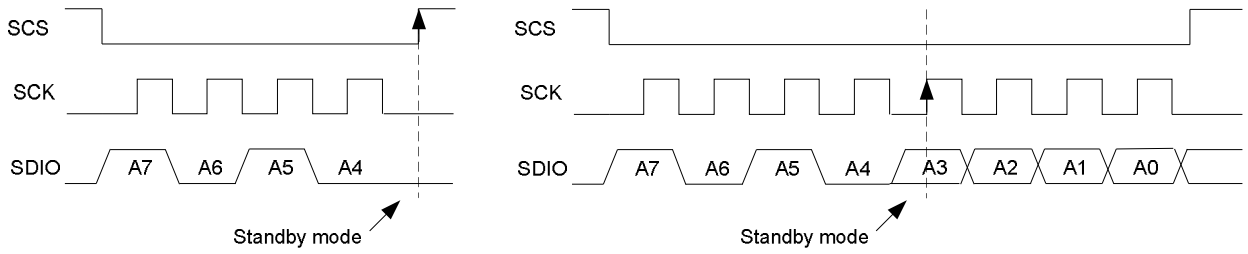


Figure 10.6 Standby mode Command Timing Chart

10.4.4 Strobe Command - PLL Mode

Refer to Table 10.3, user can issue 4 bits (1011) Strobe command directly to set A7153 into PLL mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	1	1	x	x	x	x	PLL mode

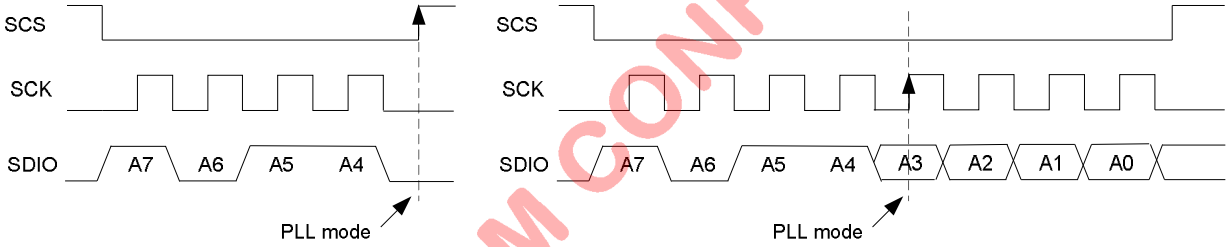


Figure 10.7 PLL mode Command Timing Chart

10.4.5 Strobe Command - RX Mode

Refer to Table 10.3, user can issue 4 bits (1100) Strobe command directly to set A7153 into RX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								**Description**
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	x	x	x	x	RX mode

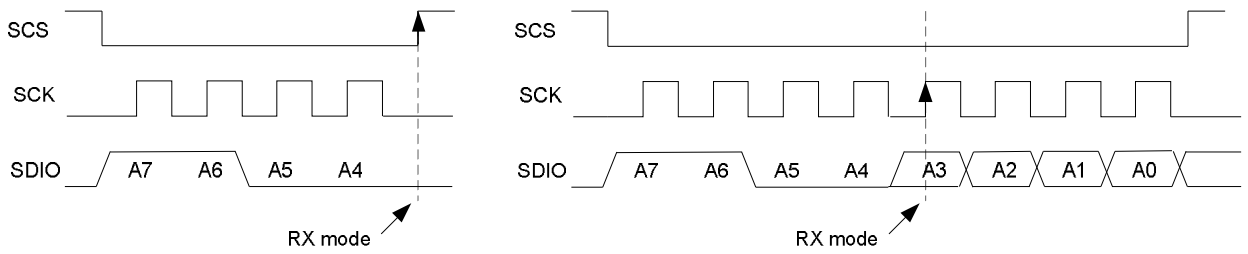


Figure 10.8 RX mode Command Timing Chart

10.4.6 Strobe Command - TX Mode

Refer to Table 10.3, user can issue 4 bits (1101) Strobe command directly to set A7153 into TX mode. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	1	x	x	x	x	TX mode

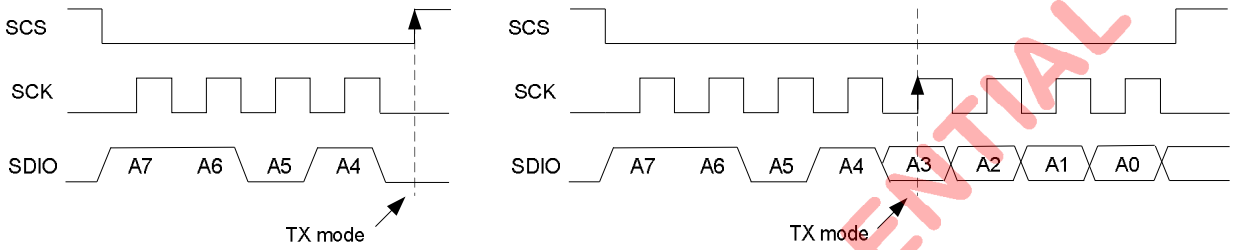


Figure 10.9 TX mode Command Timing Chart

10.4.7 Strobe Command – Deep Sleep Mode

Refer to Table 10.3, user can issue 8 bits (1000-10xx) Strobe command directly to switch off power supply to A7153. In this mode, A7153 is staying minimum current comsuption and all registers are no data retention. After deep sleep mode, A7153 shall be re-calibration. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	1	0	x	x	No registers retention, need re-calibration. GIO1 and GIO2 are internal pull high.

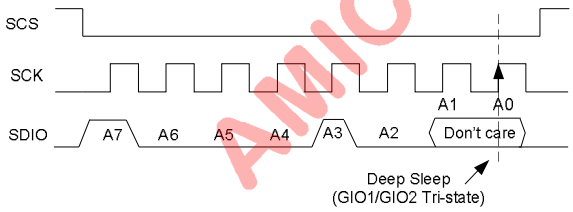


Figure 10.10 Deep Sleep Mode Timing Chart

10.4.8 Strobe Command – Low voltage Sleep Mode

Refer to Table 10.3, user can issue 8 bits (1000-10xx) Strobe command directly to switch off power supply to A7153. In this mode, A7153 is staying minimum current comsuption and all registers are no data retention. After deep sleep mode, A7153 shall be re-calibration. Below are the Strobe command table and timing chart.

Strobe Command

Strobe Command								Description
A7	A6	A5	A4	A3	A2	A1	A0	
1	1	1	0	x	x	x	x	With registers retention, no need re-calibration.

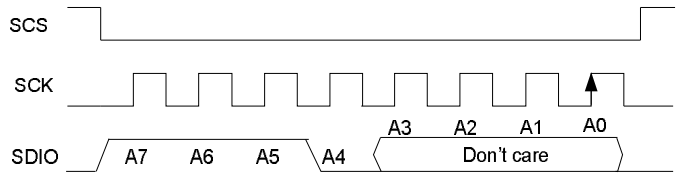


Figure 10.11 Low voltage Sleep Mode Timing Chart

10.5 Reset Command

In addition to power on reset (POR), MCU could issue software reset to A7153 by setting Mode Register (00h) through SPI interface as shown below. If address (A7~A0) are all zero and data is 0x80, A7153 generates an internal signal "RESETN" to initial itself. After reset command, A7153 is in standby mode and re-calibration is necessary.

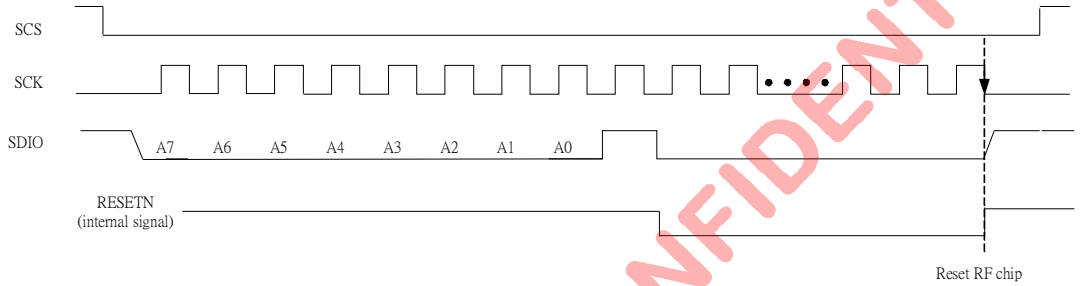


Figure 10.12 Reset Command Timing Chart

10.7 FIFO Accessing Command

To enable FIFO mode, MCU just needs to set FMS (01h) =1 via SPI interface. In FIFO mode, before TX delivery, user only needs to write wanted data into TX FIFO in advance. Similarly, user can read RX FIFO once payload data is received.

10.7.1 TX FIFO Write Command

Below is the procedure of writing TX FIFO.

Step1: Set A7~A0 = 00000101 (A6=0 for write control register and FIFO address is 05h).
Step2: Via SDIO and SCK pin, send (n+1) bytes TX data in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when step2 is completed.
Step4: Send TX Strobe command for transmitting. Refer to Figure 10.9.

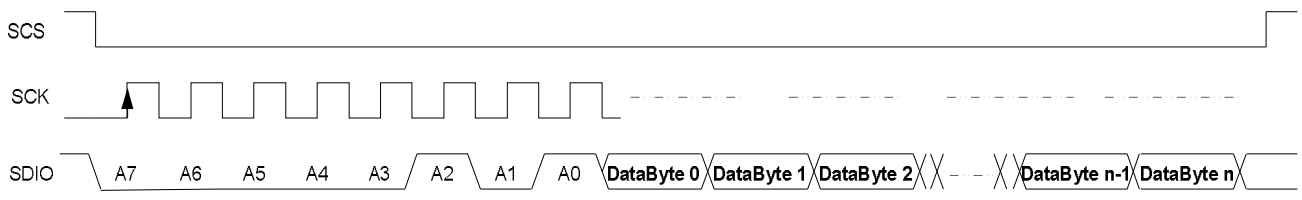


Figure 10.13 TX FIFO Write Command Timing Chart

10.7.2 Rx FIFO Read Command

Below is the procedure of reading RX FIFO.

Step1: Set A7~A0 = 01000101 (A6=1 for read control register and FIFO address is 05h).

Step2: SDIO pin outputs RX data from RX FIFO in sequence by Data Byte 0, 1, 2 to n.
Step3: Toggle SCS pin to high when RX FIFO is read completely.

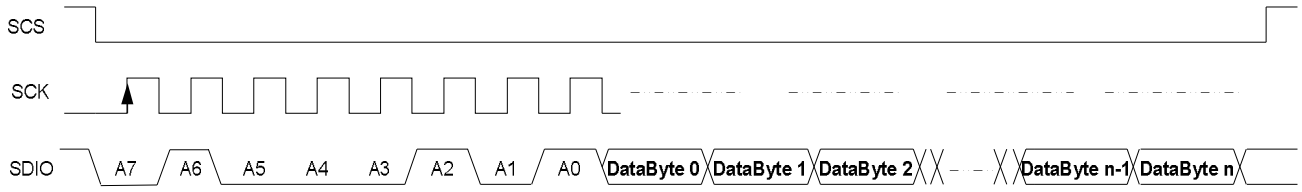


Figure 10.14 RX FIFO Read Command Timing Chart

11. Introduction of IEEE 802.15.4 - 2006

11.1 IEEE 802.15.4 PHY Frame Structure

From IEEE 802.15.4 definition, the physical layer (PHY) frame structure is shown in Figure 11.1.

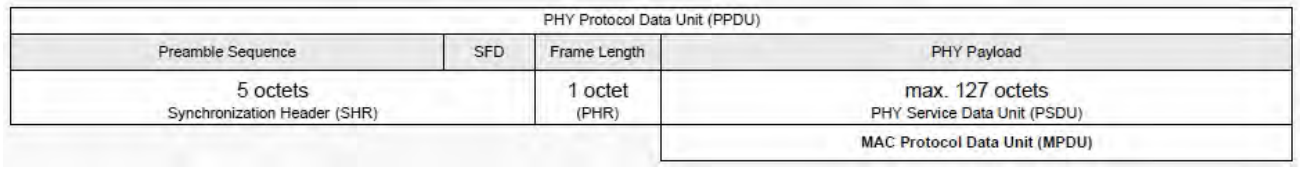


Figure 11.1 IEEE 802.15.4 Frame Format - PHY-Layer Frame Structure (PPDU)

11.1.1 Synchronization Header (SHR)

The SHR consists of a four-octet preamble field (all zero), followed by a single byte start-of-frame delimiter (SFD) which has the predefined value 0xA7 (A7153 register address 06h, default 0xA7). During transmit, the SHR is automatically generated by A7153, thus the Frame Buffer shall contain PHR and PSDU only.

The transmission of the SHR requires 160 µs (10 symbols). As the SPI data rate is normally higher than 2Mbps (over-air data rate), this allows MCU to initiate a transmission without having transferred the full frame data already. Instead it is possible to subsequently write the frame content.

During frame reception of A7153, the SHR is used for synchronization purposes. The matching SFD determines the beginning of the PHR and the following PSDU payload data.

11.1.2 PHY Header (PHR)

The PHY header is a single octet following the SHR. The least significant 7 bits denote the frame length of the following PSDU, while the most significant bit of that octet is reserved, and shall be set to zero for IEEE 802.15.4 compliant frames which defines frame lengths ≤127 bytes.

11.1.3 PHY Payload (PHY Service Data Unit, PSDU)

The PSDU has a variable length between 0 and MaxPHYPacketSize (127, maximum PSDU size in octets) whereas the last two octets are used for the Frame Check Sequence (FCS). The length of the PSDU is signaled by the frame length field (PHR). The PSDU contains the MAC Protocol Layer Data Unit (MPDU).

11.2 IEEE 802.15.4 MAC Frame Structure

From IEEE 802.15.4 definition, medium access control (MAC) layer frame structure is shown below, Figure 11.2.

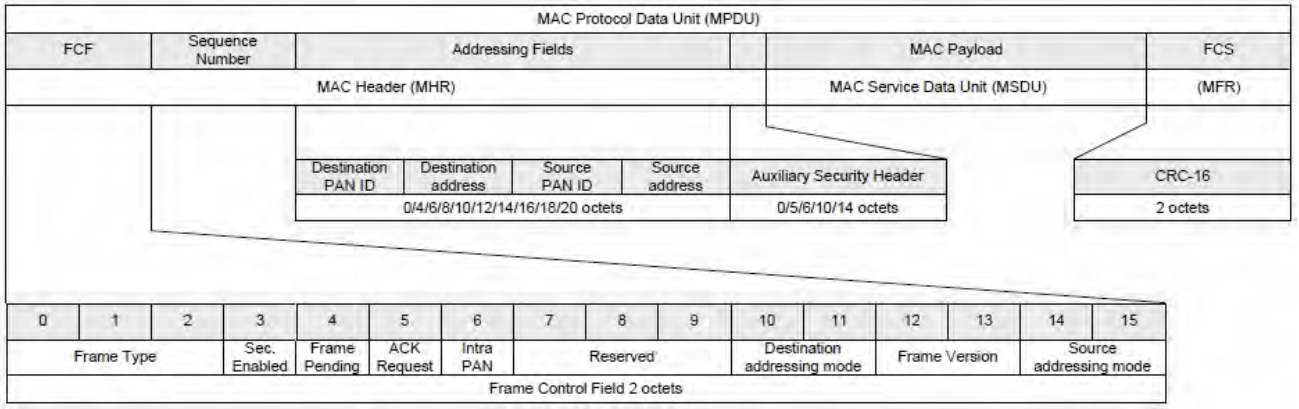


Figure 11.2 IEEE 802.15.4 Frame Format - MAC-Protocol Data Unit (MPDU)

11.2.1 MAC Header (MHR)

The MAC header consists of the Frame Control Field (FCF), a sequence number, and the addressing fields (which are of variable length, and can even be empty in certain situations).

11.2.2 Frame Control Field (FCF)

The FCF consists of 16 bits, and occupies the first two octets of the MPDU or PSDU, respectively.

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Frame Type			Sec. Enabled	Frame Pending	ACK Request	Intra PAN	Reserved			Destination addressing mode		Frame Version		Source addressing mode	
Frame Control Field 2 octets															

Bit [0:2]: Frame Type.
[000]: Beacon.
[001]: Data.
[010]: ACK (acknoledgement).
[011]: MAC command.
[Other]: Reserved.

Bit [3]: Security Enable.
[0]: Disable.
[1]: Enable.

Bit [4]: Frame Pending.
[0]: Disable.
[1]: To set in an acknowledgment frame (ACK) in response to a data request MAC command frame.

This bit can be set in an acknowledgment frame (ACK) in response to a data request MAC command frame. This bit indicates that the node, which transmitted the ACK, has more data to send to the node receiving the ACK.

Bit [5]: ACK Request.
[0]: No need ACK.
[1]: To set within a data or MAC command frame that is not broadcast, the recipient shall acknowledge the reception of the frame within the time specified by IEEE 802.15.4 (i.e. within 192 μs for non beacon-enabled networks).

For acknowledgment frames (5 bytes) automatically generated by A7153, user just needs to enable ACKS (02h) and configure ACK frame control field in advance by AFCF (34h).

Bit [6]: Intra PAN.
[0]: Disable.
[1]: To set Intra-PAN to indicates that in a frame, where both, the destination and source addresses are present, the PAN-ID of the source address field is omitted.

Bit [7:9]: Reserved.

Bit [10:11]: Destination Address Mode.
[00]: PAN identifier and address fields are not present.
[01]: Reserved.
[10]: Address field contains a 16-bit short address.
[11]: Address field contains a 64-bit extended address.

Bit [12:13]: Frame Version.
[00]: Frames are compatible with IEEE 802.15.4 2003.
[01]: Frames are compatible with IEEE 802.15.4-2006.
[10]: Reserved.
[11]: Reserved.

Bit [14:15]: Source Address Mode.

[00]: PAN identifier and address fields are not present.
[01]: Reserved.
[10]: Address field contains a 16-bit short address.
[11]: Address field contains a 64-bit extended address.

11.2.3 Sequence Number (SN)

SN (Sequence Number) following the FCF identifies a particular frame, so that duplicated frame transmissions can be detected. The next packet shall be larger than then current packet.

Be aware that the content of SN is copied from the frame to be acknowledged into the acknowledgment frame which behaviour is automatically done by A7153 if ACKS =1 (auto ACK is enabled).

11.2.4 Address Field

The addressing fields of the MAC Header (MPDU) are used for address matching indication. The destination address (if present) is always first, followed by the source address (if present). Each address field consists of the Intra PAN ID and a device address.

If both addresses are present, and the "Intra PAN-ID compression" subfield in the FCF is set to one, the source Intra PAN ID is omitted.

Note that in addition to these general rules, IEEE 802.15.4 further restricts the valid address combinations for the individual possible MAC frame types. For example, the situation where both addresses are omitted (source addressing mode = 0 and destination addressing mode = 0) is only allowed for acknowledgment frames.

11.2.5 Auxiliary Security Header Field

The Auxiliary Security Header specifies information required for security processing and has a variable length. This field determines how the frame is actually protected (security level) and which keying material from the MAC security PIB is used (see IEEE 802.15.4-2006, section 7.6.1). This field shall be present only if the Security Enabled subfield b3 is set to one. For details of its structure, see IEEE 802.15.4-2006, section 7.6.2. Auxiliary security header.

11.2.6 MAC Service Data Unit (MSDU)

This is the actual MAC payload. It is usually structured according to the individual frame type. A description can be found in IEEE 802.15.4-2006, section 5.5.3.2.

11.2.7 MAC Footer (MFR) Fields

The MAC footer consists of a two-octet Frame Checksum (FCS). The Frame Check Sequence (FCS) is characterized by:

1. Indicate bit errors, based on a cyclic redundancy check (CRC) of length 16 bit
2. Uses International Telecommunication Union (ITU) CRC polynomial ($x^{16} + x^{12} + x^5 + 1$)
3. Applying an ITU CRC polynomial to all transferred bytes following the length field (MHR and MSDU fields).
4. Automatically FCS check on each received frame. A CRCF (00h) is set if the FCS of a received frame is valid.
5. A7153 can be automatically generated during transmission

11.3 IEEE 802.15.4 Frame Type

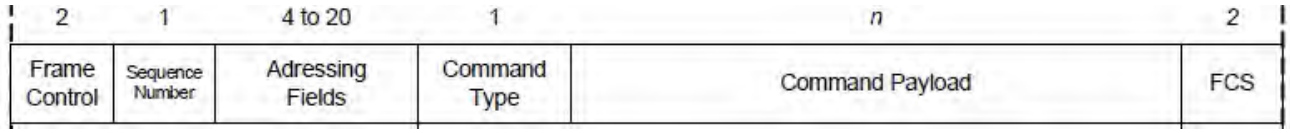
11.3.1 Beacon Frame

If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match MAC PAN-ID unless MAC PAN-ID is equal to 0xFFF.

2	1	4 or 10	2	*k*	*m*	*n*	2
Frame Control	Sequence Number	Adressing Fields	Superframe Specification	GTS Fields	Pending Address Fields	Beacon Payload	FCS

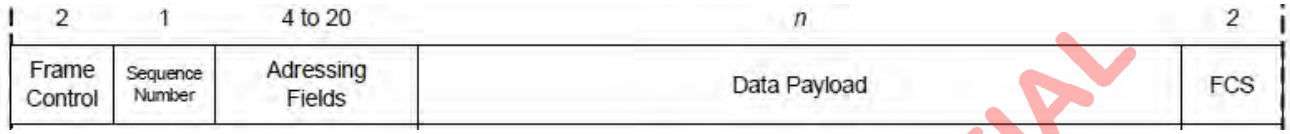
11.3.2 MAC Command Frame

If the frame type indicates that the frame is a MAC Command frame, the MAC payload stores command information.



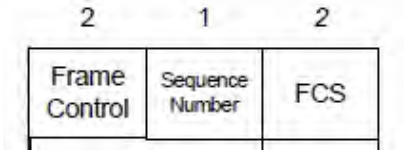
11.3.3 MAC Data Frame

If the frame type indicates that the frame is a MAC Command frame, the MAC payload stores command information.



11.3.4 ACK Frame

If the frame type indicates that the frame is an ACK frame, see below standard format (5 bytes) regarding to ZigBee or RF4CE. A7153 supports auto ACK. User just needs to enable ACKS (02h) and configure ACK frame control field in advance by AFCF (34h). In addition, SN and FCS are also auto attached if ACKS = 1.



11.4 IEEE 802.15.4 CCA (Clear Channel Assessment)

The main features of the Clear Channel Assessment (CCA) module are:
• All 4 modes are available as defined by IEEE 802.15.4-2006 in section 6.9.9
• Adjustable threshold for energy detection algorithm

A CCA measurement is used to detect a clear channel. Three modes are specified by IEEE 802.15.4 - 2006:

CCA Mode 1: Energy above threshold. (A7153's MAC HW supports this mode only.)
CCA shall report a busy medium upon detecting any energy above the ED threshold.

CCA Mode 2: Carrier sense only.
CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of an IEEE 802.15.4 compliant signal. The signal strength may be above or below the ED threshold.

CCA Mode 3: Carrier sense with engery above threshold.
CCA shall report a busy medium using logic combination logic by
-- Detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4
-- Energy above the ED threshold.
Where the logical operator may be configured as either OR or AND.

11.5 IEEE 802.15.4 LQI (Link Quality Indication)

According to IEEE 802.15.4, the LQI measurement is a characterization of the strength and/or quality of a received packet. The measurement may be implemented using receiver ED, a signal-to-noise ratio estimation, or a combination of these methods. The use of the LQI result by the network or application layers is not specified in this standard. LQI values shall be an integer ranging from 0x00 to 0xFF. The minimum and maximum LQI values (0x00 and 0xFF) should be associated with

the lowest and highest quality compliant signals, respectively, and LQI values in between should be uniformly distributed between these two limits.

The LQI measurement of A7153 is implemented as a measure of the link quality which can be described by

- ED value for this link (ADCOM=11, read from ADC, 17h, in RSSI mode).
- LQIV values for 32 frame moving average (a kind of packet error rate correlation).

This is done for each received frame in ranging from 0 to 255.

According to IEEE 802.15.4 a low LQI value is associated with low signal strength and/or high signal distortions. Signal distortions are mainly caused by interference signals and/or multipath propagation. High LQI values indicate a sufficient high signal power and low signal distortions.

Note, the received signal power as indicated by received signal strength indication (RSSI) value or energy detection (ED) value of A7153 do not characterize the signal quality and the ability to decode a signal.

ZigBee networks often require the identification of the "best" routing between two nodes. Both, the LQI and the RSSI/ED can be used for this, dependent on the optimization criteria.

If a low packet error rate (corresponding to high throughput) is the optimization criteria then the LQI value should be taken into consideration. If a low transmission power or the link margin is the optimization criteria then the RSSI/ED value is also helpful.

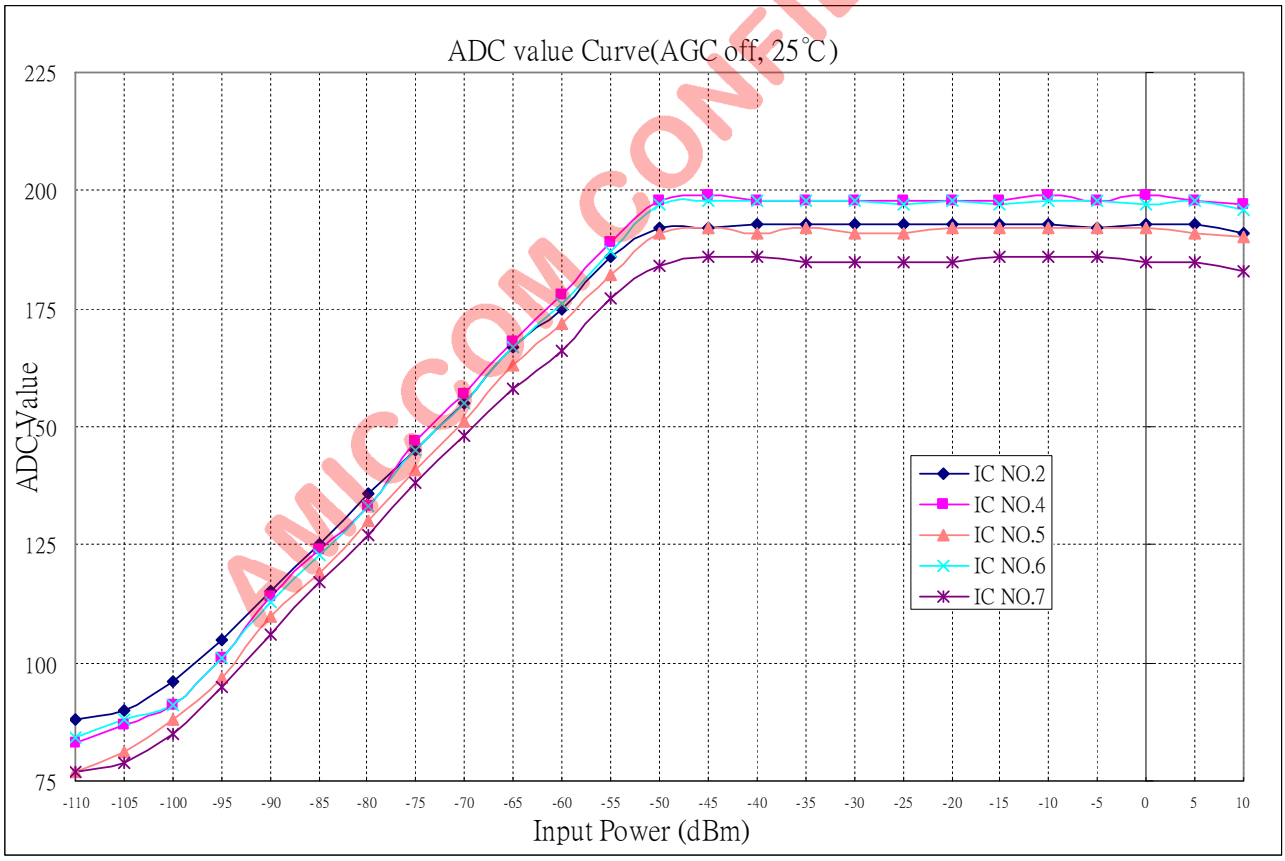


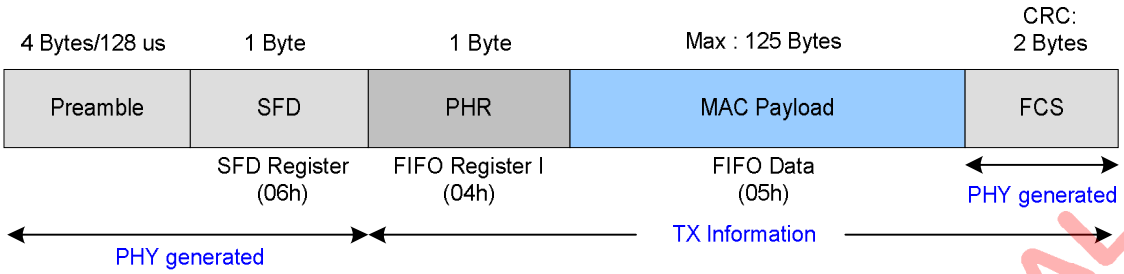
Figure 11.4.1 ED curve vs Input TX Power

Combinations of LQI, RSSI and ED are possible for routing decisions. As a rule of thumb RSSI and ED values are useful to differentiate between links with high LQI values. Transmission links with low LQI values should be discarded for routing decisions even if the RSSI/ED values are high. This is because RSSI/ED does not say anything about the possibility to decode a signal. It is only information about the received signal strength whereas the source can be an interferer.

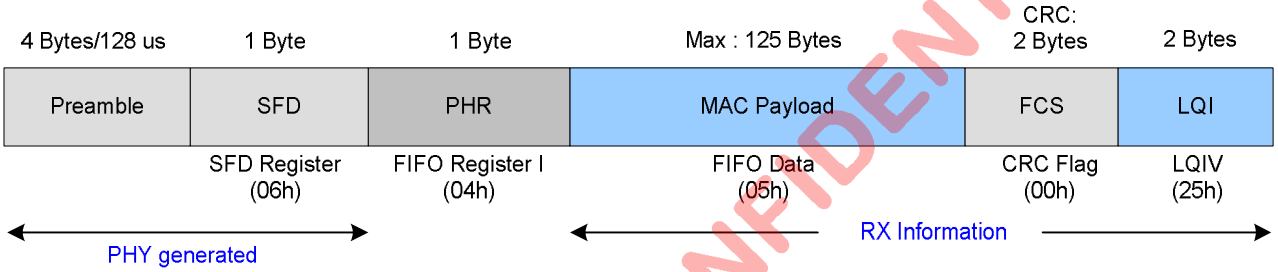
11.6 A7153 Frame Structure

A7153 contains a 128 byte TX FIFO and a 128 byte RX FIFO connected to the SPI interface. The TX FIFO and RX FIFO shares the same address space 05h.

TX Operation



RX Operation



12. Transceiver Frequency

A7153 is a half-duplex transceiver with embedded PA and LNA. The receiver is a low-IF architecture consisting of a LNA, down conversion mixers, polyphase channel filters and IF limiting amplifiers with RSSI. The transmitter is direct modulation architecture with 3.5 dBm maximum output power and 13 dB power control range. For TX or RX frequency setting, user just needs to set up one register, CHN (0Fh), for frequency agility.

A7153's main PLL features are:

- Frantional-N to generate RX/TX frequencies for all IEEE 802.15.4 - 2.4 GHz channels
- Autonomous calibration loops for stable operation within the operating range
- Fast PLL settling to support frequency hopping

During receive operation, the frequency synthesizer works as a local oscillator. During transmit operation, the voltage-controlled oscillator (VCO) is directly modulated to generate the RF transmit signal. The frequency synthesizer is implemented as a fractional-N PLL.

The PLL is designed to support 16 channels in the 2.4 GHz ISM band with channel spacing of 5 MHz according to IEEE 802.15.4. An offset scheme is implemented to get the center frequency of these channels as follows:

F_{LO} = 2400 + (CHN x 0.5) in [MHz], where CHN is the channel number, addr 0Fh.

A7153's LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, A7153 is very easy to implement frequency hopping by **ONE register setting, (CHN, 0Fh).** In general, user can plan the wanted channels by a CHN Look-Up-Table between master and slaves for two-way frequency hopping. Below is the LO frequency block diagram.

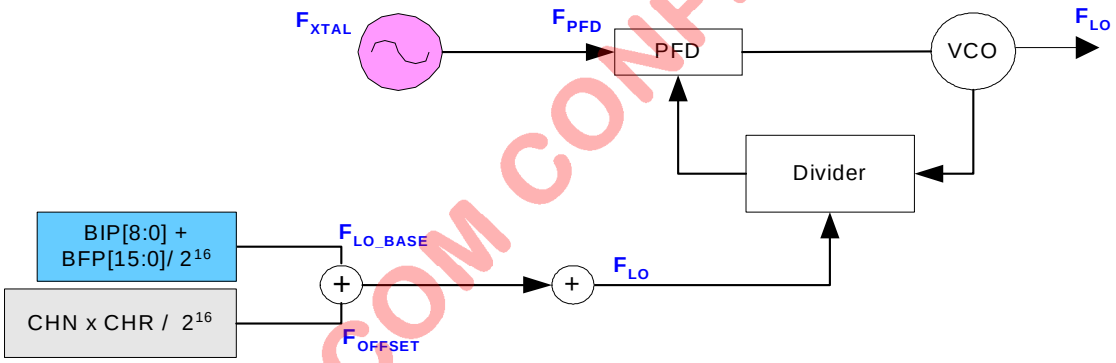


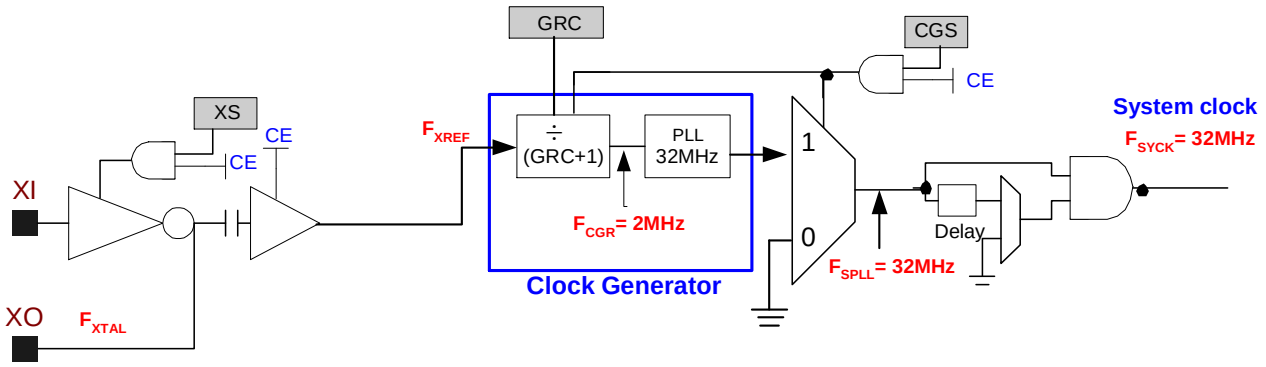
Figure 12.1 Block Diagram of Local Oscillator

12.1 System Clock

The system clock of A7153 (F_{SYCK}= 32 MHz) is generated by the PLL clock generator which reference frequency (F_{CGR}= 2MHz) is derived from frequency divider of crystal oscillator.

$F_{CGR} = \frac{F_{XREF}}{(GRC[3:0]+1)}$, where GRC [3:0] (0Eh) is the divide number to get F_{CGR} (2 MHz) from crystal oscillator.

Below is block diagram of system clock where F_{XTAL} is the crystal frequency. User can set XS, GRC, CGS to get F_{SYCK} = 32MHz. F_{XREF} is a reference clock to generate F_{CGR} = 2MHz and F_{SPLL} = 32MHz. After delay circuitry, F_{SYCK} (32MHz) is derived.



F_{XTAL}	F_{XREF}	F_{CGR}	GRC [3:0]	XS	CGS
16 MHz	16 MHz	Must be 2 MHz	[0111]	1	1

Figure 12.2 System Clock Block Diagram

A7153 supports programmable data rate by SDR [1:0] (0Eh). Additional feature such as turbo mode (2Mbps @ MSK modulation) is implemented in this device. See below table for details.

F_{SYCK} (system clock)	SDR [1:0] (0Eh)	CNTR[1:0] (27h)	Data Rate (DSSS)	Turbo Mode (MDS=1, 02h)
Reserved	[00]	[00]	Forbidden	Note supported
32 MHz	[01]	[01]	125Kbps	Note supported
32 MHz	[10]	[01]	250Kbps	2 Mbps
48 MHz	[11]	[10]	375Kbps	Note supported

Table 12.1 Data Rate Configuration

12.1 LO Frequency Setting

To set up 2.4GHz LO Frequency ($F_{LO,}$), user can refer to below 4 steps.

1. Set the base frequency (**F_{LO_BASE}**) by PLL Register II (36h) and III (37h).
   Recommend to set **F_{LO_BASE} ~ 2400.001MHz**.

2. Set channel step F_{CHSP} = 500KHz by PLL Register IV (38h).

3. Set CHN [7:0] to get offset frequency by PLL Register I (0Fh).
   F_{OFFSET} = CHN [7:0] * F_{CHSP}

4. LO frequency is equal to base frequency plus offset frequency.
   F_{LO} = F_{LO_BASE} + F_{OFFSET}

12.1.1 How to set F_{LO_BASE}

Regarding to LO frequency setting, Table 12.2 shows 2400.001 MHz base frequency by 16MHz Xtal.

STEP	ITEMS	VALUE	NOTE
1	F_{XTAL}	16 MHz	Crystal Frequency
2	BIP[7:0]	0x96	To get F_{LO_BASE} =2400 MHz
3	BFP[15:0]	0x0004	To get F_{LO_BASE} ~ 2400.001 MHz
4	F_{LO_BASE}	~2400.001 MHz	LO Base frequency

Table 12.2 How to configure F_{LO_BASE}

12.1.2 How to set $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$

Regarding to frequency offset scheme, Table 12.3 shows IEEE 802.15.4 Channel 11 (2405.001 MHz) by 16MHz Xtal.

STEP	ITEMS	VALUE	NOTE
1	F_{LO_BASE}	~2400.001 MHz	After cofigure BIP and BFP
2	CHR[14:0]	0x0800	To get F_{CHSP}= 500 KHz
3	CHN[7:0]	0x0A	To set channel number = 10
4	F_{OFFSET}	5 MHz	To get F_{OFFSET}= 500 KHz * (CHN) = 5MHz
5	F_{LO}	~2405.001 MHz	To get F_{LO}= F_{LO_BASE} + F_{OFFSET}

Table 12.3 How to configure F_{LO}

12.2 Frequency Agility

A7153 supports frequency agility with a channel spacing of 5 MHz according to IEEE 802.15.4 and RF4CE specification. The center frequency of these channels is defined as follows:

CHN [7:0] PLL I (0Fh)	Channel Number (IEEE 802.15.4)	Center Frequency (MHz)	Note
0x0A	11	2405	
0x14	12	2410	
0x1E	13	2415	
0x28	14	2420	
0x32	15	2425	RF4CE
0x3C	16	2430	
0x46	17	2435	
0x50	18	2440	
0x5A	19	2445	
0x64	20	2450	RF4CE
0x6E	21	2455	
0x78	22	2460	
0x82	23	2465	
0x8C	24	2470	
0x96	25	2475	RF4CE
0xA0	26	2480	

Table 12.4 Channel Assignment for IEEE 802.15.4 - 2.4 GHz Band

When the PLL is enabled during state transition from Standby to TX Ready, the settling time is typically 70 µs, including settling of PLL and Power Amplify. Switching from Standby to RX Ready is typically done 70 µs. This makes the radio transceiver highly suitable for frequency hopping applications.

IEEE 802.15.4 Operation Mode	PDL (2Ch)	TDL [2:0] (2Ch)	Note
Slot	PDL = [10], 32 us	TDL = [100], 64 us	
Unslot	PDL = [10], 32 us	TDL = [100], 64 us	

Table 12.5 Settling time configuraiton for IEEE 802.15.4 operation modes.

13. Frame Filtering

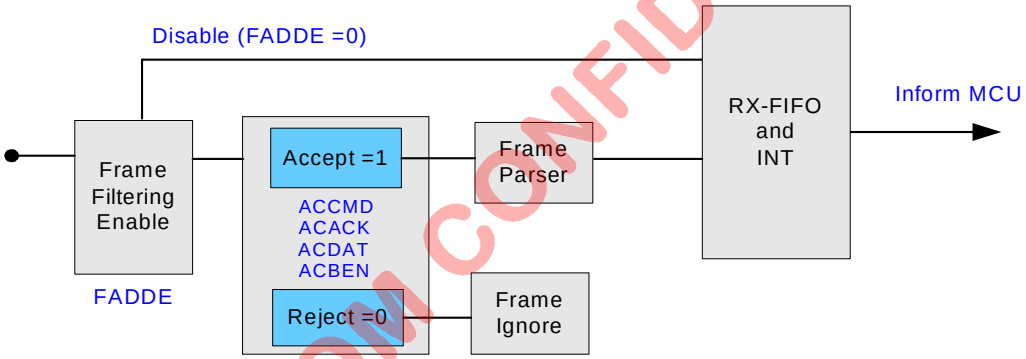
A7153 supports frame filtering to accept or to ignore coming packets regarding to frame type by setting (31h). User just needs to set PCORR (31h, 1 for coordinator and 0 for end device) and enable FADDE (31h). With different frame type filtering (Beacon or Command or Data or ACK) and consigned PAD_ID, Short Address and Long Address of specific Zigbee network into ADF Frame Registers (32h), The frame filtering function rejects non-intended frames, third filtering level, automatically identify valid packets to inform MCU to simplify Zigbee network complexity and MCU loading.

ADF control Register (Address: 31h)

Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	**FADDE**	**ACBEN**	**ACDAT**	**ACACK**	**ACCMD**	**ACRES**	**PCORR**	**MAXVER1**
Reset		1	1	1	1	1	1	0	0
Name	W	**MAXVER0**	**RESMUX2**	**RESMUX1**	**RESMUX0**	**--**	**--**	**--**	**--**
Reset		1	0	0	0	--	--	--	--

FADDE: MAC Address Filtering.
[0]: Disable. **[1]:** Enable.

PCORR: PAN Corrdinator.
[0]: End device. **[1]:** Corrdinator.



ADF Frame Register (Address: 32h)

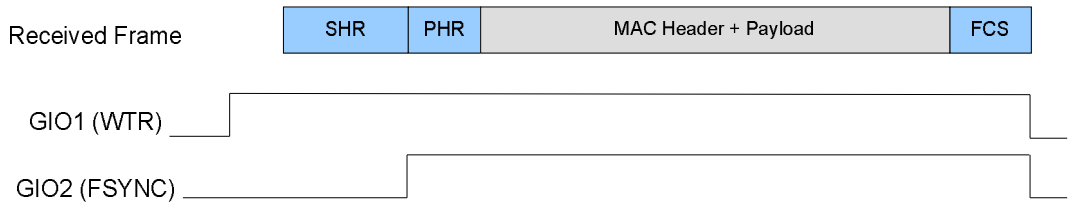
Bit	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	W	PID15	PID14	PID13	PID12	PID11	PID10	PID9	PID8
	W	PID7	PID6	PID5	PID4	PID3	PID2	PID1	PID0
	W	SADD15	SADD14	SADD13	SADD12	SADD11	SADD10	SADD9	SADD8
	W	SADD7	SADD6	SADD5	SADD4	SADD3	SADD2	SADD1	SADD0
	W	LADD63	LADD62	LADD61	LADD60	LADD59	LADD58	LADD57	LADD56
	W	LADD55	LADD54	LADD53	LADD52	LADD51	LADD50	LADD49	LADD48
	W	LADD47	LADD46	LADD45	LADD44	LADD43	LADD42	LADD41	LADD40
	W	**LADD39**	**LADD38**	**LADD37**	**LADD36**	**LADD35**	**LADD34**	**LADD33**	**LADD32**
	W	**LADD31**	**LADD30**	**LADD29**	**LADD28**	**LADD27**	**LADD26**	**LADD25**	**LADD24**
	W	**LADD23**	**LADD22**	**LADD21**	**LADD20**	**LADD19**	**LADD18**	**LADD17**	**LADD16**
	W	**LADD15**	**LADD14**	**LADD13**	**LADD12**	**LADD11**	**LADD10**	**LADD8**	**LADD8**
	W	**LADD7**	**LADD6**	**LADD5**	**LADD4**	**LADD3**	**LADD2**	**LADD1**	**LADD0**
Reset		1	1	1	1	1	1	1	1

PID[15:0]: PAN ID Storage.

SADD[15:0]: Short Adderss Storage.

LADD[63:0]: Long Address Storage.

Frame reception starts with detection of a start-of-frame delimiter (SFD), followed by the length byte. When the reception is completed, The FSYNC (Frame Sync, 0Bh or 0Ch), which can be output on GIO1 or GIO2, can be connected to a timer input on a MCU to capture the start of received frames.



Filtering Algorithm Map

Conditions								
FADDE = 1								
MAXVER [1:0]<= [01]								
RESMUX [9:7] = [000]								
Source and Destination address modes != [01]								
Beacon Frames Filtering	Data Frames Filtering			ACK Frames Filtering	MAC Command Frames Filtering			Reserved Frame Filtering
ACBEN = 1	ACDAT = 1			ACACK = 1	ACCMD = 1			ACRES = 1
Length byte >= 9	Length byte >= 9			Length byte = 5	Length byte >= 9			
Dest addr mode = 0	Dest addr mode = 0	Dest addr mode = 2	Dest addr mode = 3		Dest addr mode = 0	Dest addr mode = 2	Dest addr mode = 3	
source addr mode = 2 or 3	PAN COR = 1	Dest PAN ID = PID[15:0] or 0xFFFF	Dest PAN ID = PID[15:0] or 0xFFFF		PAN COR = 1	Dest PAN ID = PID[15:0 or 0xFFFF	Dest PAN ID = PID[15:0] or 0xFFFF	
source PAN ID = PID[15:0] or 0xFFFF	Source PAN ID = PID[15:0]	Dest addr = SADD[15:0] or 0xFFFF	Dest addr = LADD[63:0]		Source PAN ID = PID[15:0]	Dest addr = SADD[15:0] or 0xFFFF	Dest addr = LADD[63:0]	

FADDE (31h) bit controls whether frame filtering is applied or not. When disabled, A7153 will accept all received frames. When enabled (which is the default setting), A7153 will only accept frames that fulfill all of the following requirements:

-- The length byte must be equal to or higher than the “minimum frame length”, which is derived from the source and destination address mode and PAN ID compression subfields of the FCF.

-- The value of the frame version subfield of the FCF cannot be higher than MAXVER[1:0] (31h).

-- The source and destination address modes cannot be reserved values (1).

-- Destination address:
(1) If a destination PAN ID is included in the frame, it must match PANID[15:0] (32h) or must be the broadcast PAN identifier (0xFFFF).

(2) If a short destination address is included in the frame, it must match either SADD[15:0] (32h) or the broadcast address (0xFFFF).

(3) If an extended destination address is included in the frame, it must match LADD[63:0] (32h).

-- Frame type:
(1) Beacon frames (0) are only accepted when:
- ACBEN = 1 (31h)
- Length byte >= 9
- The destination address mode is 0 (no destination address)
- The source address mode is 2 or 3 (i.e. a source address is included)
- The source PAN ID matches PANID [15:0] (32h), or PANID equals 0xFFFF

(2) Data (1) frames are only accepted when:
- ACDAT = 1 (31h)
- Length byte >= 9
- A destination address and/or source address is included in the frame. If no destination address is included in the frame, the PCORR = 1(31h) and the source PAN ID must equal PANID [15:0] (32h).

-- Acknowledgment (2) frames are only accepted when:
- ACACK = 1 (31h)
- Length byte = 5

-- MAC command (3) frames are only accepted when:
- ACCMD = 1 (31h)
- Length byte >= 9
- A destination address and/or source address is included in the frame. If no destination address is included in the frame, PCORR = 1 (31h) and the source PAN ID must equal PANID [15:0] (31h) for the frame to be accepted.

-- Reserved frame types (4, 5, 6 and 7) are only accepted when:
- ACRES = 1 (default is 0)
- Length byte >= 9

If a frame is rejected, A7153 will start searching a new frame once current frame is rejected.

The FSYNC (0Bh or 0Ch) will go high when start of frame delimiter is completely received and remains high until either the last byte in MPDU is received or the received frame has failed to pass address recognition and been rejected.

FSYNC can preferably be connected to a timer capture pin on MCU to extract timing information of transmitted and received data frames.

Tips and Tricks

The following register settings must be configured correctly:

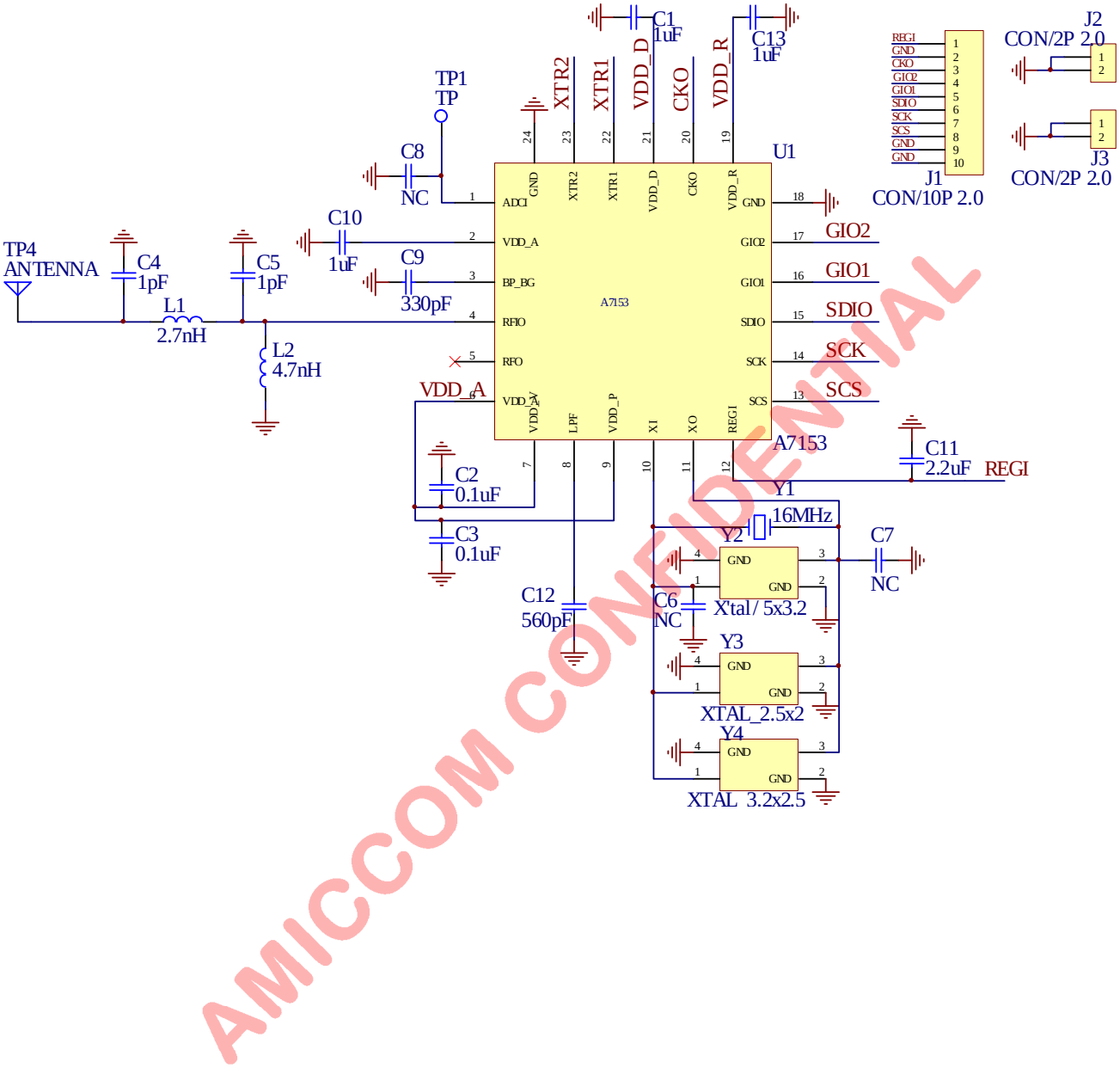
- PCORR (31h) must be set if the device is a PAN coordinator, and cleared if not.
- RESMUX [9:7] must be [000].
- MAXVER[1:0] (31h) must correspond to the supported version(s) of the IEEE 802.15.4 standard.
- The local address information (PANID [15:0], SADD [15:0, LADD [63:0]) must be loaded into ADF Frame Register (32h).

During operation in a busy IEEE 802.15.4 environment, A7153 will receive large numbers of non-intended ACK frame. To effectively block reception of these frames, use ACK Frame Filtering (ACACK=0 (31h)).

Set ACACK = 1 after successfully starting a transmission with acknowledgment request, and clear the bit again after the acknowledgment frame has been received, or the timeout has been reached.

It is not necessary to turn off the receiver while changing the values of (31h) registers and (32h) register. However, **if the changes take place between reception of the SFD byte and the source PAN ID, the modified values will impact Frame Parser to induce errors.**

14. Application Circuit Example



15. Abbreviations

ADC	Analog to Digital Converter
AIF	Auto IF
AGC	Automatic Gain Control
BW	Bandwidth
CBC-MAC	Cipher Block Chaining Message Authentication Code
CCA	Clear Channel Assessment
CCM	Counter with CBC-MAC
CCM*	Extension of CCM
CD	Carrier Detect
CHSP	Channel Step
CRC	Cyclic Redundancy Check
CSMA-CA	Carrier Sense Multiple Access with Collision Avoidance
DC	Direct Current
ED	Energy Detection
FIFO	First in First out
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
LQI	Link Quailty Indication
MCU	Micro Controller Unit
MPDU	MAC Protocol Data Unit
MPSU	MAC Protocol Service Unit
PER	Packet Error Rate
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
PSDU	PHY Service Data Unit
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SFD	Start of Frame Delimiter
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXLO	Transmitter Local Oscillator
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

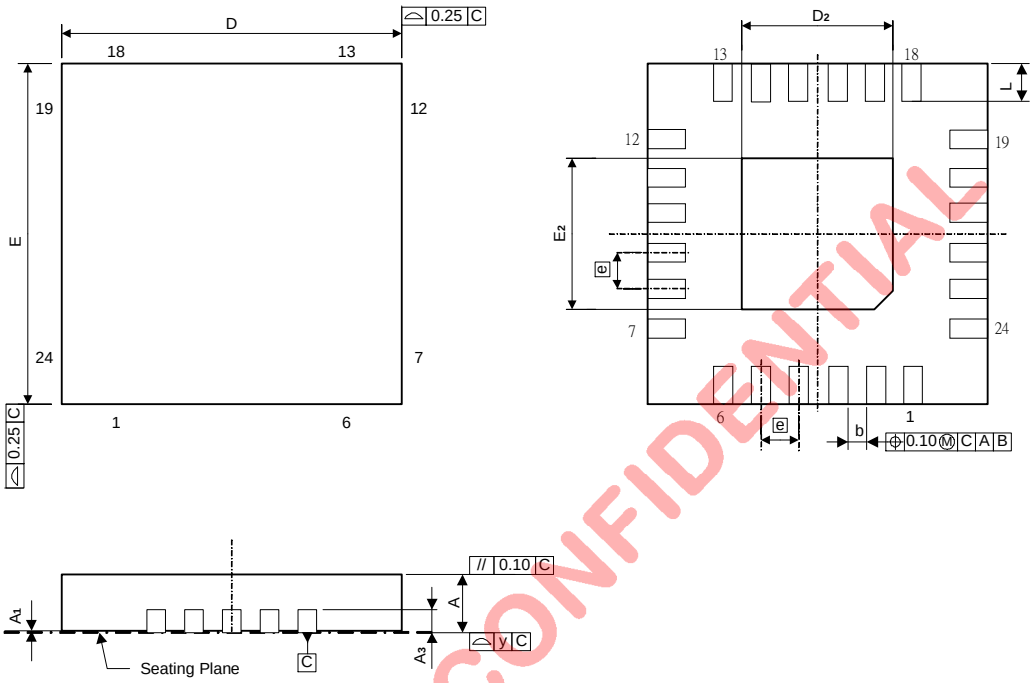
16. Ordering Information

Part No.	Package	Units Per Reel / Tray
A71X53AQFI/Q	QFN24L, Pb Free, Tape & Reel, -40℃～85℃	3K
A71X53AQFI	QFN24L, Pb Free, Tray, -40℃～85℃	490EA

17. Package Information

QFN 24L (4 X 4 X 0.8mm) Outline Dimensions unit: inches/mm

TOP VIEW **BOTTOM VIEW**

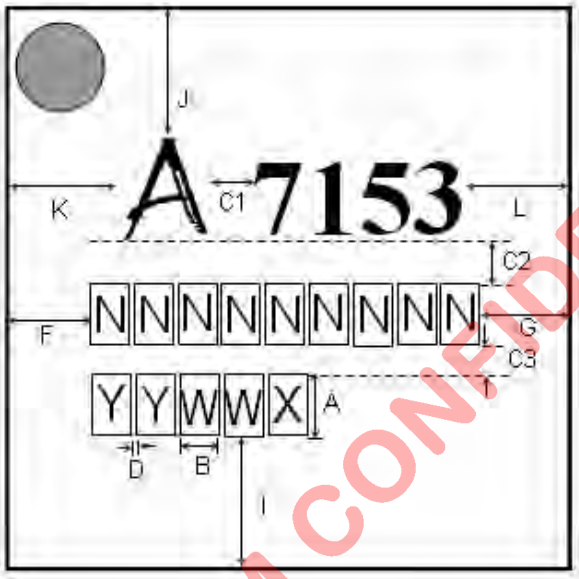


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3		0.008 REF			0.203 REF	
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.154	0.158	0.161	3.90	4.00	4.10
D_2	0.075	-.	0.114	1.90	-	2.90
E	0.154	0.158	0.161	3.90	4.00	4.10
E_2	0.075	-	0.114	1.90	-	2.90
e		0.020 BSC			0.50 BSC	
L	0.012	0.016	0.020	0.30	0.40	0.50
y		0.003			0.08	

18. Top Marking Information

- Part No. : **A71X53AQFI**
- Pin Count : **24**
- Package Type : **QFN**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**

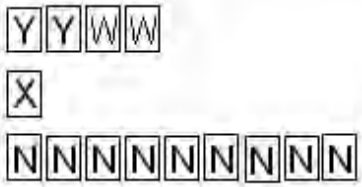
❖TOP MARKING LAYOUT:

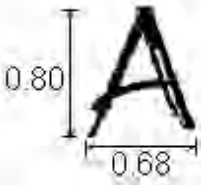


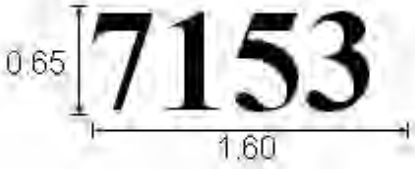
❖ CHARACTER SIZE : (Unit in mm)

A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03
A1 : 0.75
B2 : 0.7

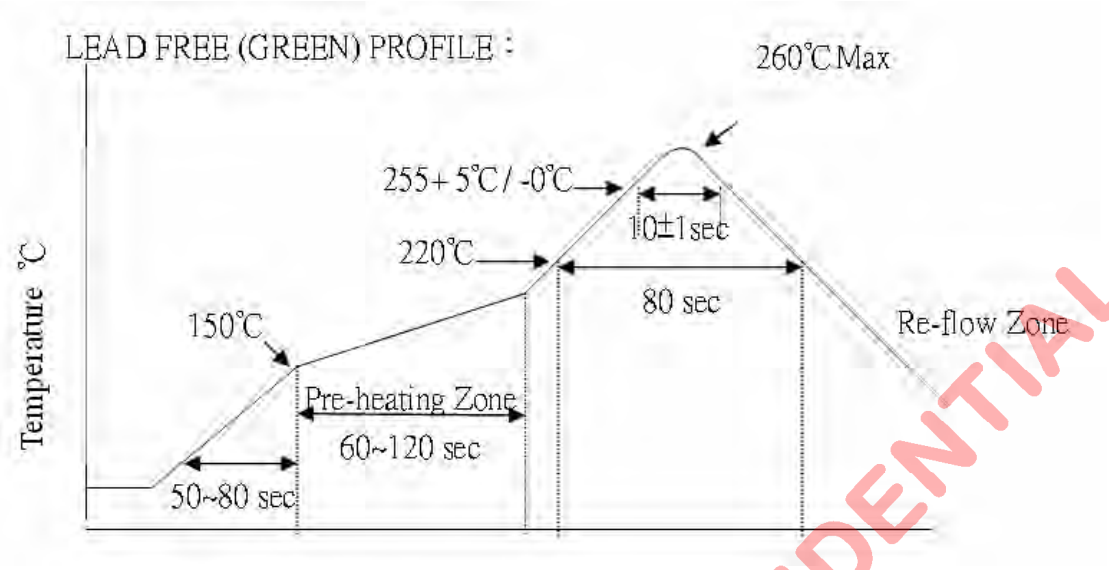
F=G
I=J
K=L





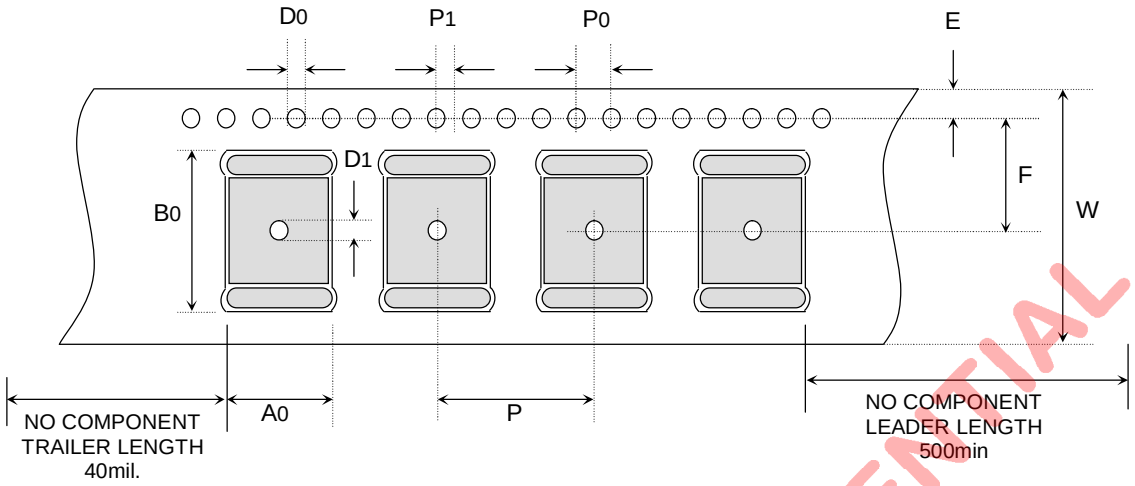


19. Reflow Profile



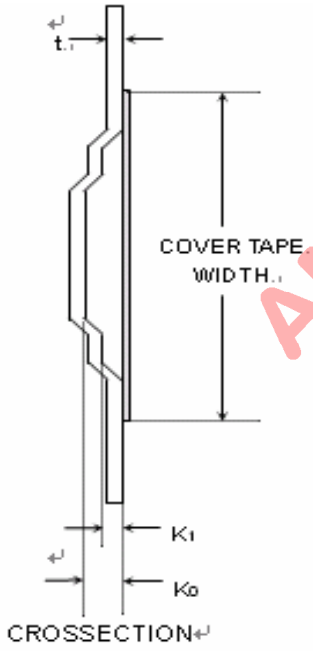
20. Tape Reel Information

Cover / Carrier Tape Dimension



11 EA IC **60cm±4cm**

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
48 QFN 7*7	12	7.25	7.25	4.0	2.0	1.5	1.5	1.75	7.5	16
DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16
28 SSOP (150mil)	8	6	10	4.0	2.0	1.5	1.5	1.75	7.5	16



TYPE	K0	K1	t
20 QFN (4X4)	1.1	-	0.3
24 QFN (4X4)	1.4	-	0.3
32 QFN (5X5)	1.1	-	0.3
48 QFN (7X7)	1.1	-	0.3
DFN-10	0.75	-	0.25
20 SSOP	2.5	-	0.3
24 SSOP	2.1	-	0.3
28 SSOP (150mil)	2.5	-	0.3

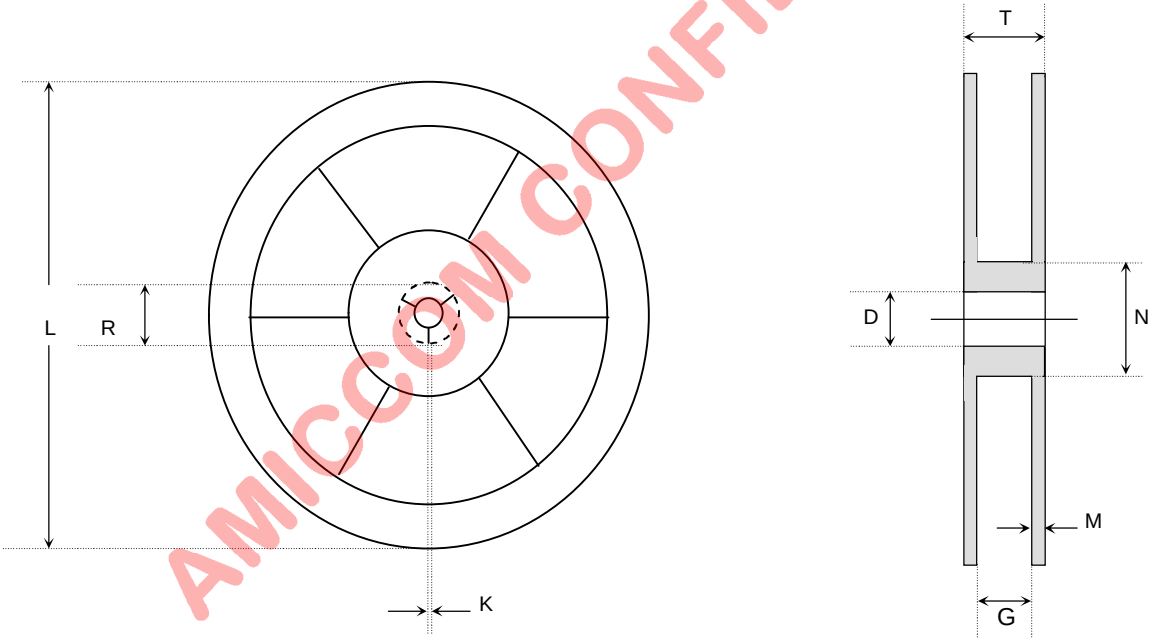
COVER TAPE WIDTH
9.2
9.2
9.2
13.3
8
13.3
13.3
12.5

Unit : mm

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋ 0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋ 0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330＋ 0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330＋ 0.00/-1.0	20.2



21. Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

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