FW introduction -- A7102

Table of Contents

RF feature

- Frequency bands: 315MHz/433MHz, 868MHz/915MHz @ FSK,GFSK
- Programmable RF TX output power: up to 15dBm@40mA
- Data rate up to 150Kpbs@sensitivity : -104dBm, RX :14mA
- Data rate up to 50Kpbs@sensitivity : -110dBm
- Build in RSSI, temperature sensor function
- Build in RTC, 1ch external ADC function
- Supply voltage 2.2 ~ 3.6V
- 64 bytes TX/RX FIFO buffer
- Build in FIFO extension function with up to 256 bytes FIFO No
- Optional Manchester Data / FEC / CRC / data whitening (encryption)
- It is applicable with long distance remote control(~700M).
- Oscillator clock out / External clock in

RF feature

如果你要讀接收数据的 RSSI :

1. 設 REG A: XADS = 0,CDM = 1.
2. 設 REG D: IRQ1,0 = 01(FSYNC)
3. 進入RX mode
4. 設 REG F: ADCM=1

==> 等待 TX packet.....

5. 如果有 packet 則, ID 對時 IRQ 會 go high.
6. 此時去 read REG A,取出ADC值.
7. delay 30us
8. go to 6.(做8次RSSI, 把結果平均)
9. 再設 REG D: IRQ1,0 = 00(WTR), 等待結束.

RSSI 公式 : Power = -56 – (5/16) * RSSI[7:0]

*** 相對 power, 非絕對 power**

如果你要讀溫度 :

1. 設 REG A: XADS = 0,CDM = 0.
2. 進入Standby mode
3. 設 REG F: ADCM=1
4. 當 REG F: ADCM=0 時, read REG A,取出ADC值.

溫度公式 : 數據差 1, 爲 2度.(相對溫度, 非絕對溫度)

如果你要讀外部 ADC :

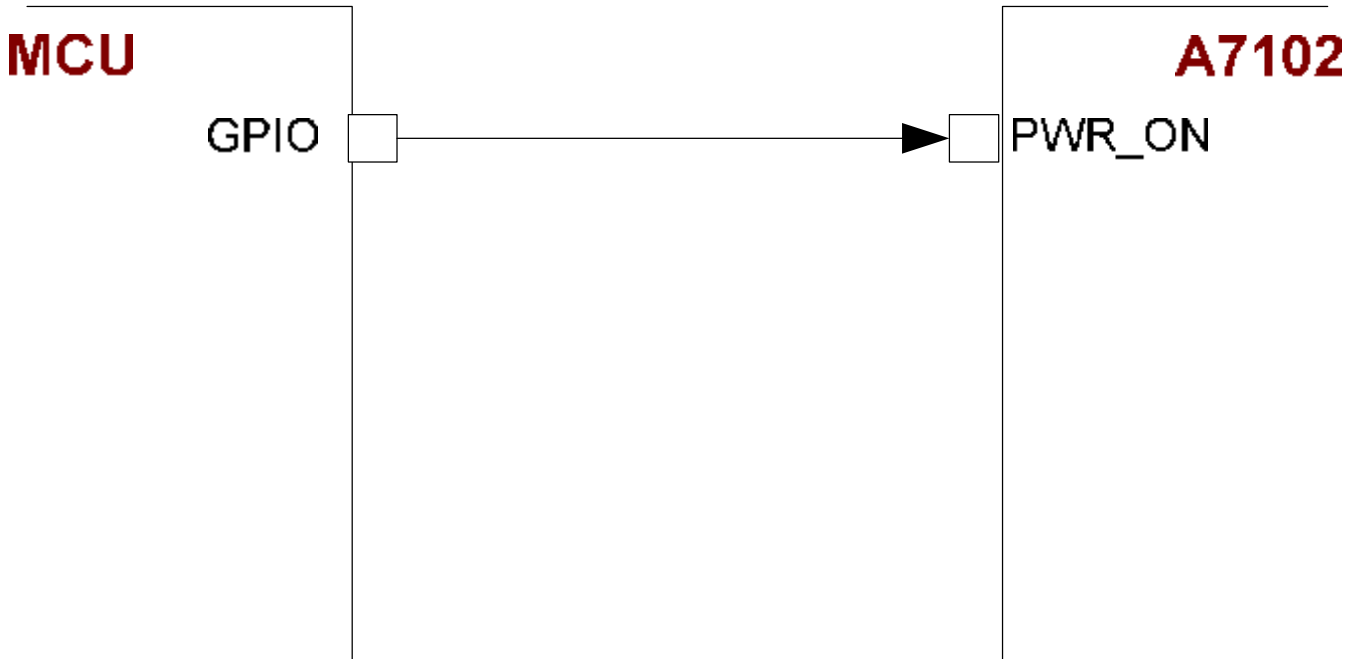
1. 設 REG A: XADS = 1,CDM = 0.
2. 進入RX mode**(settling time 要正確)**
3. 設 REG F: ADCM=1
4. 當 REG F: ADCM=0 時, read REG A,取出ADC值

EXT. ADC 公式 : 0-1.28V

*** 分壓電阻須小於 30K ohm / sleep mode 下, ADC_IN 要拉 low.**

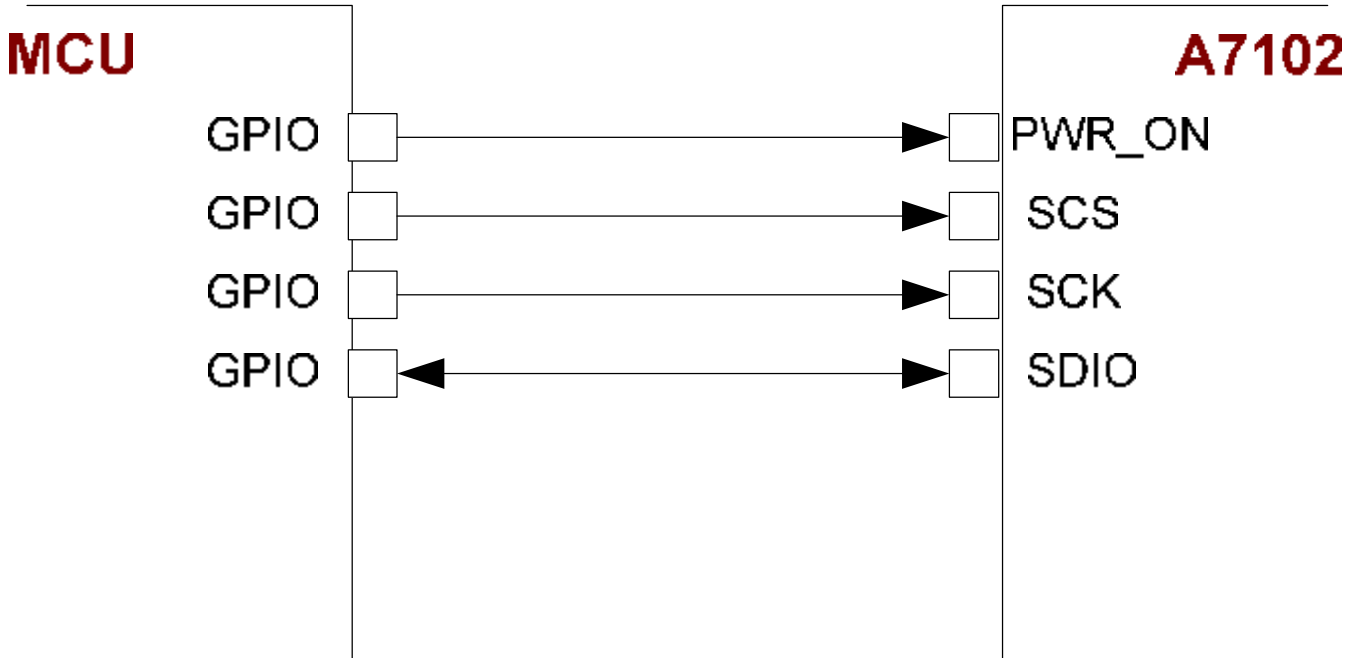
RF interface

- PWR_ON → enable internal regulator



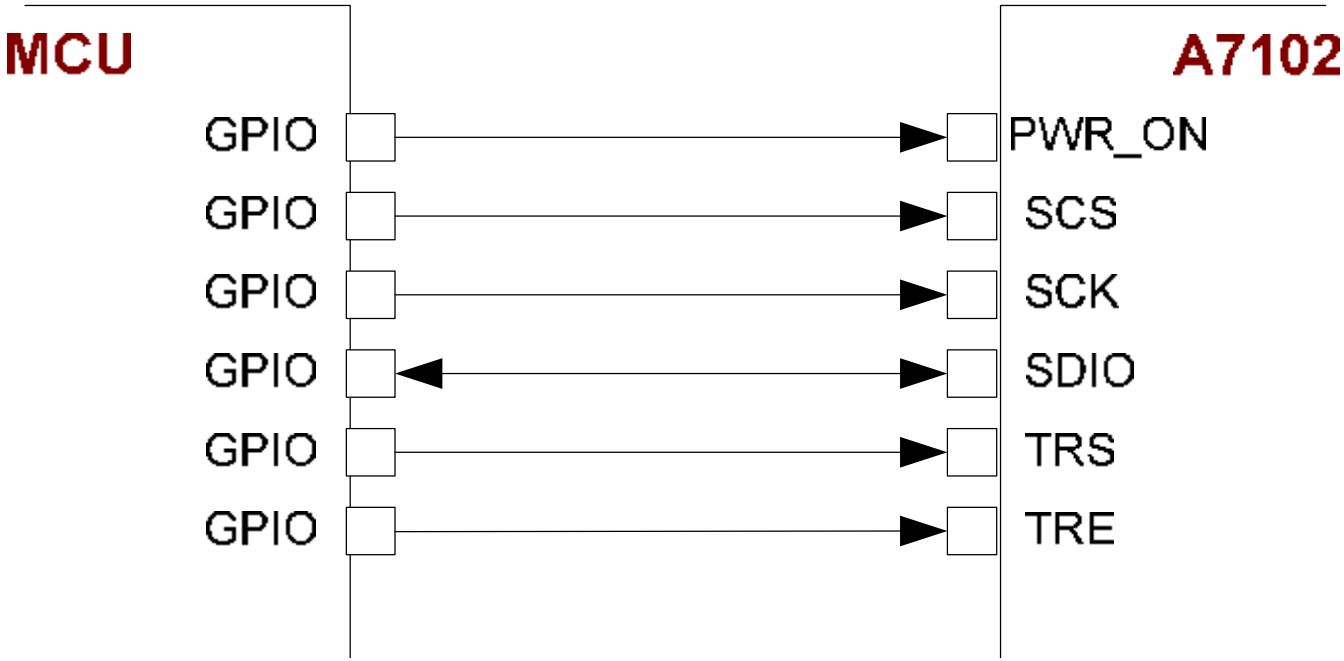
RF interface

- PWR_ON → enable internal regulator
- 3 wire serial bus → R/W RF control register



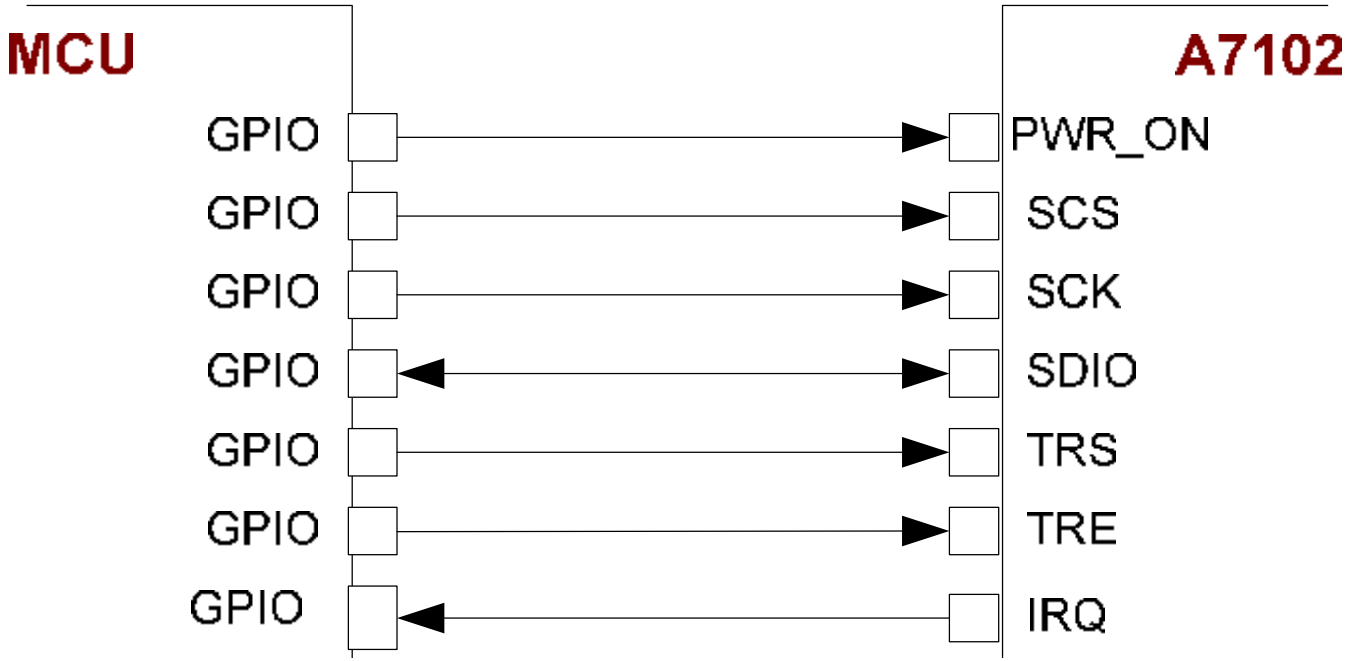
RF interface

- PWR_ON → enable internal regulator
- 3 wire serial bus → R/W RF control register
- TRS / TRE → TRX mode / TRX enable (control by register)



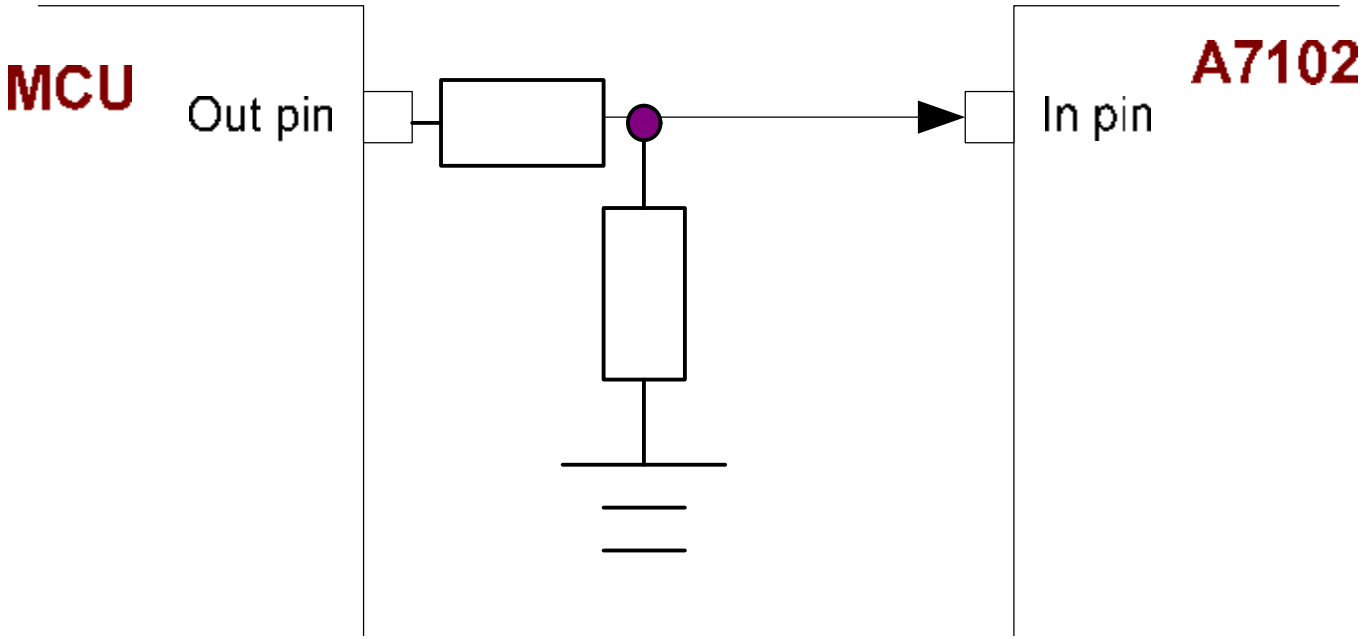
RF interface

- PWR_ON → enable internal regulator
- 3 wire serial bus → R/W RF control register
- TRS / TRE → TRX mode / TRX enable (control by register)
- IRQ → TRX indication signal



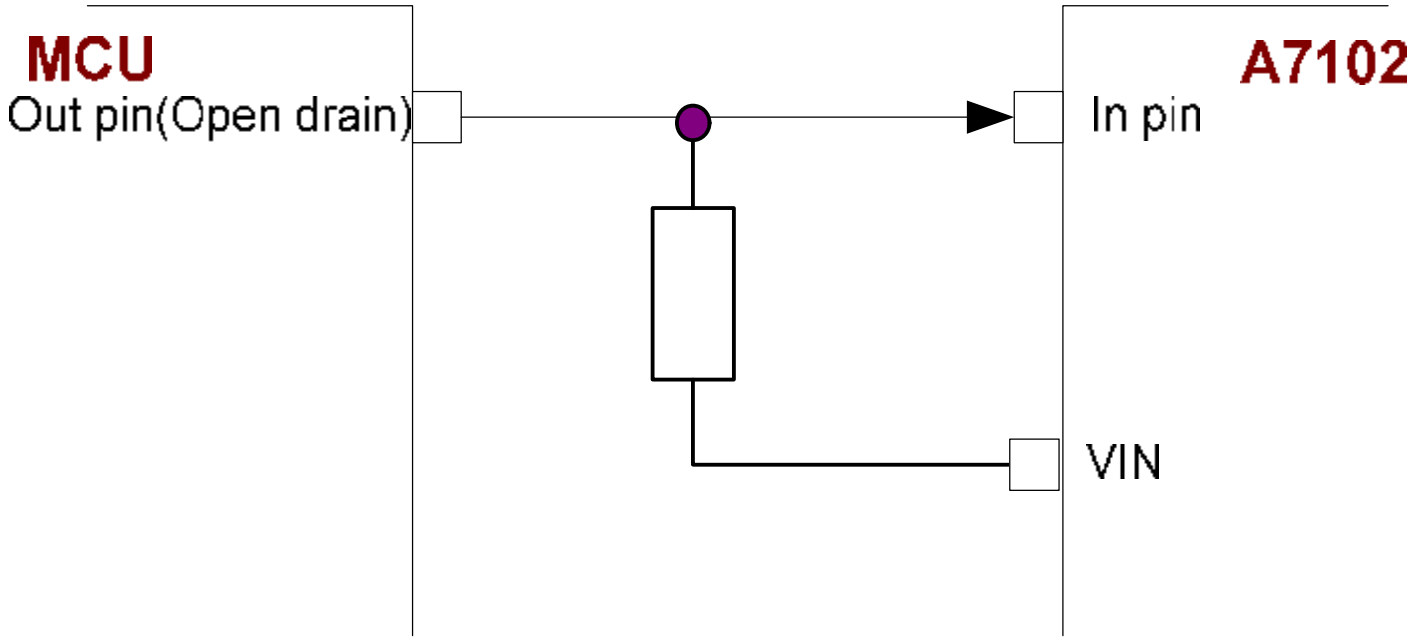
RF interface

- Input port VS MCU 5V I/O



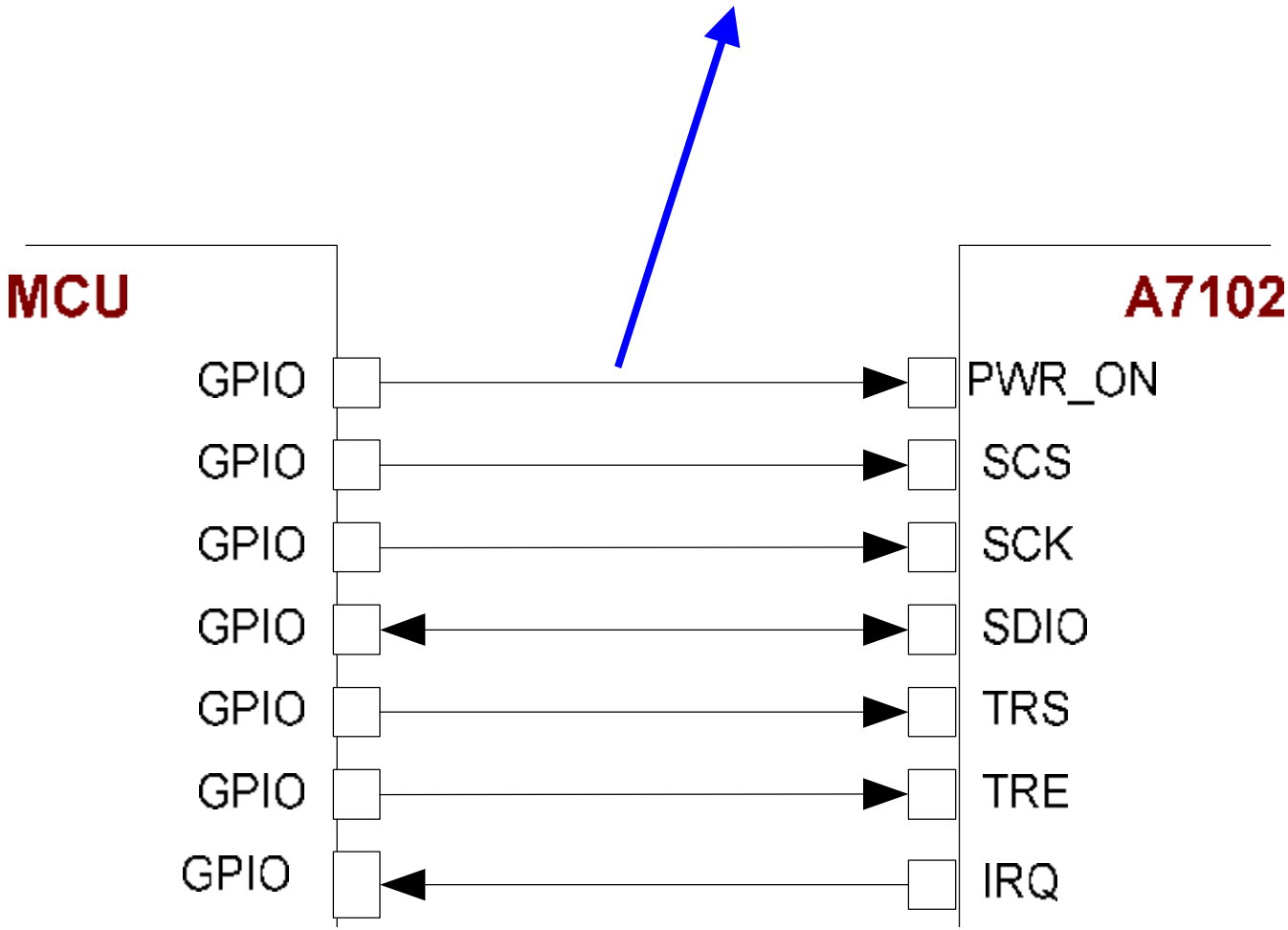
RF interface

- Input port VS MCU 5V I/O(open drain)



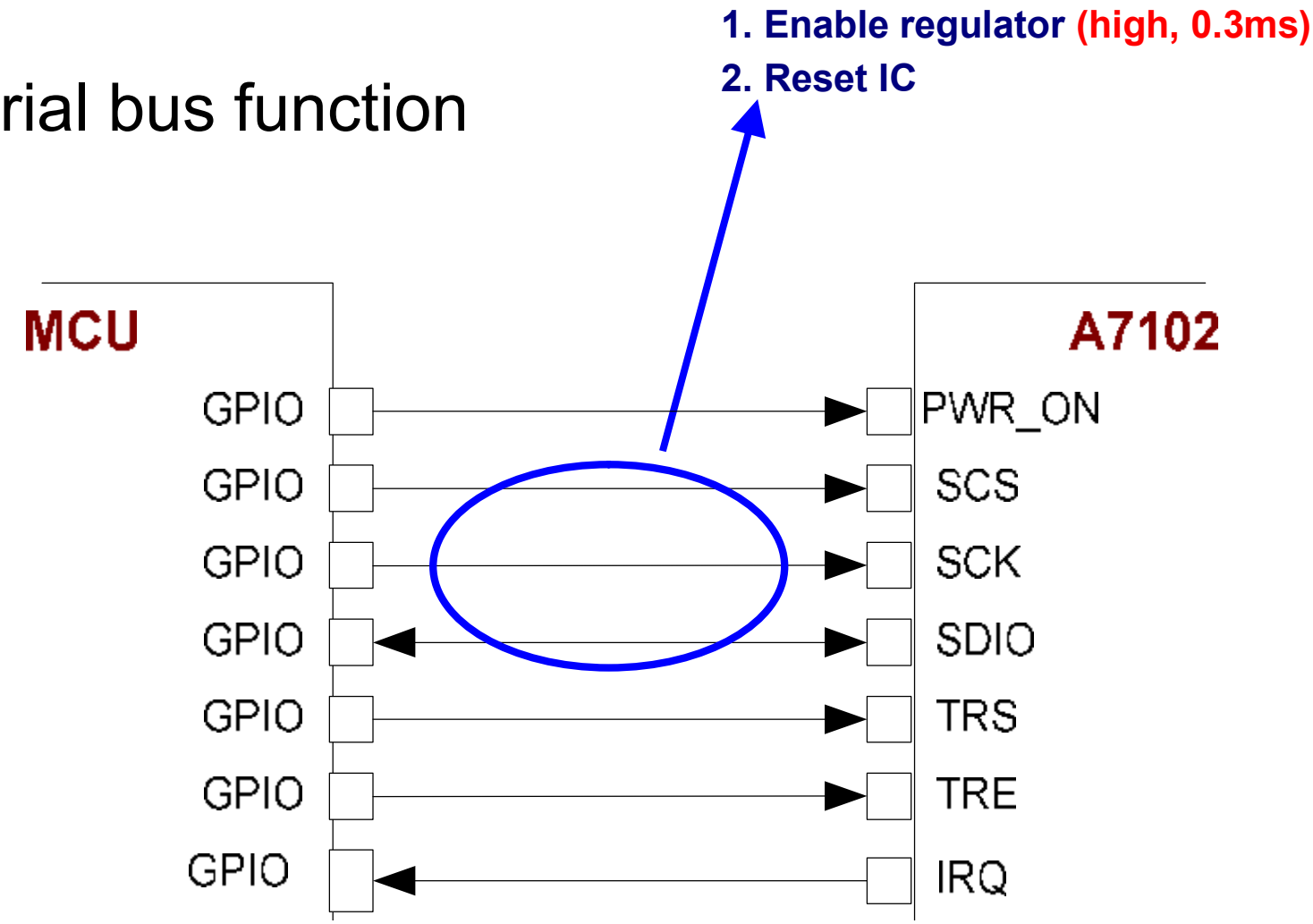
RF interface

1. **Enable regulator (high, 0.3ms)**



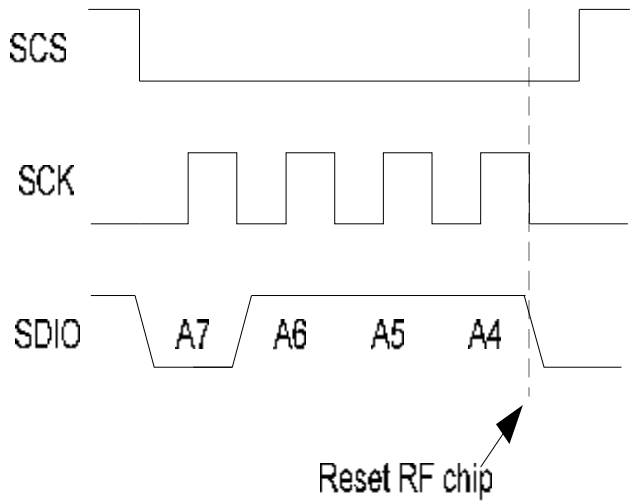
RF interface

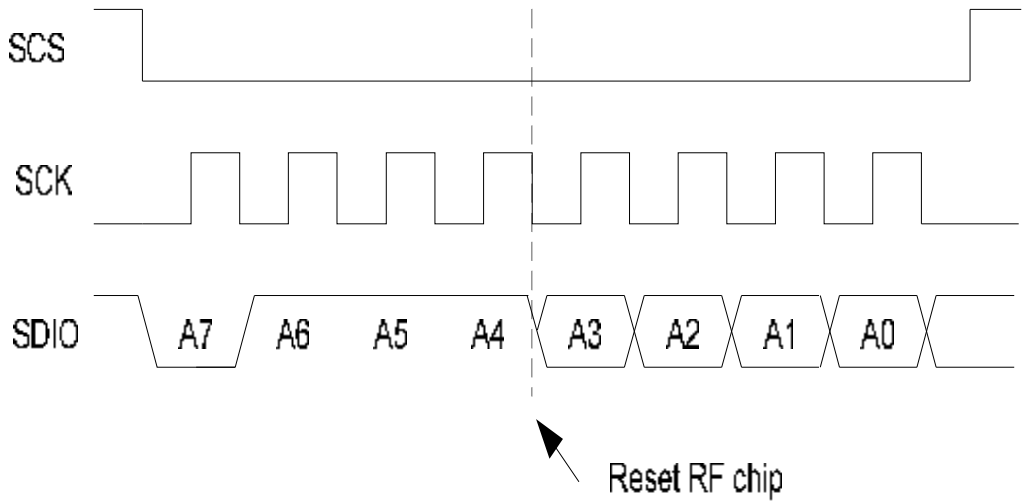
- Serial bus function



RF interface

- **Reset RF IC**

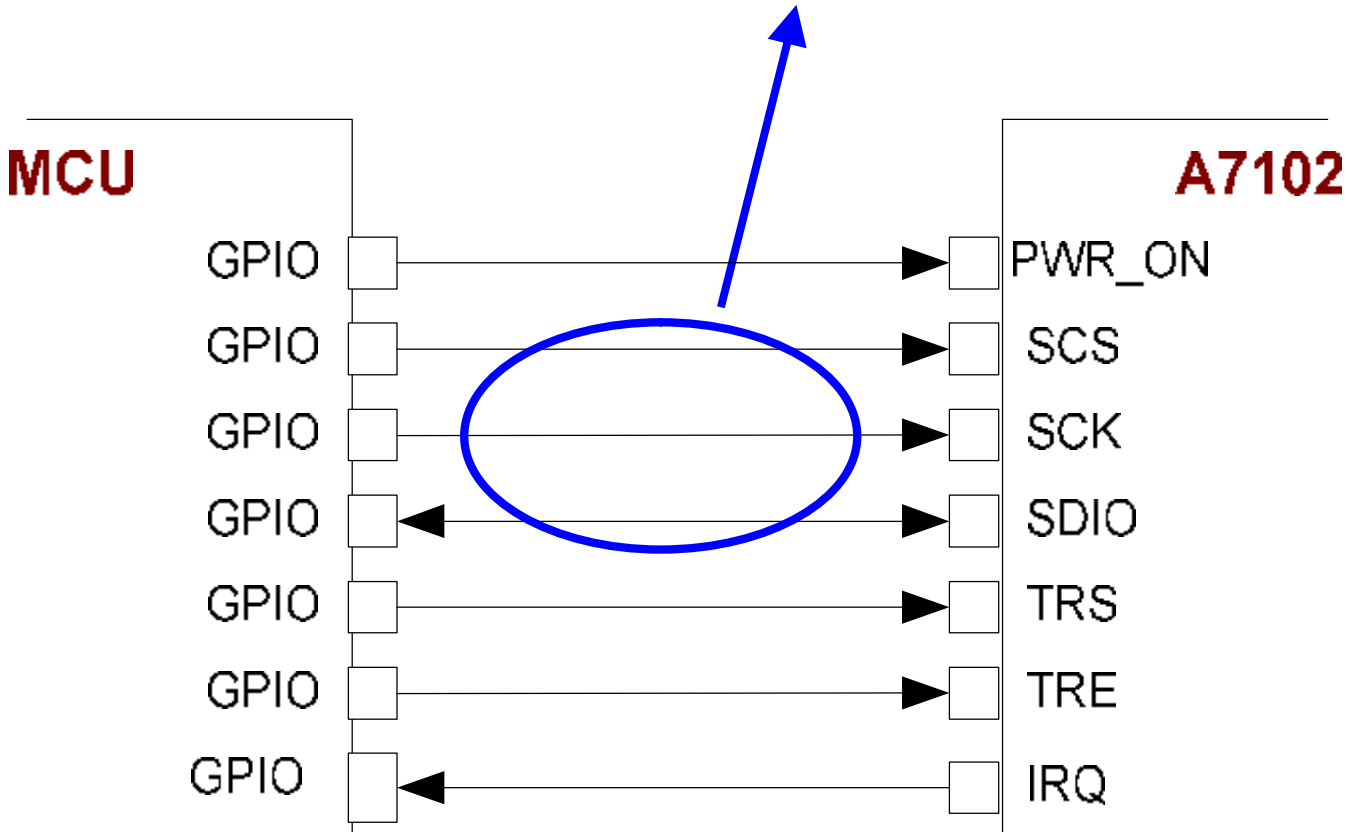




RF interface

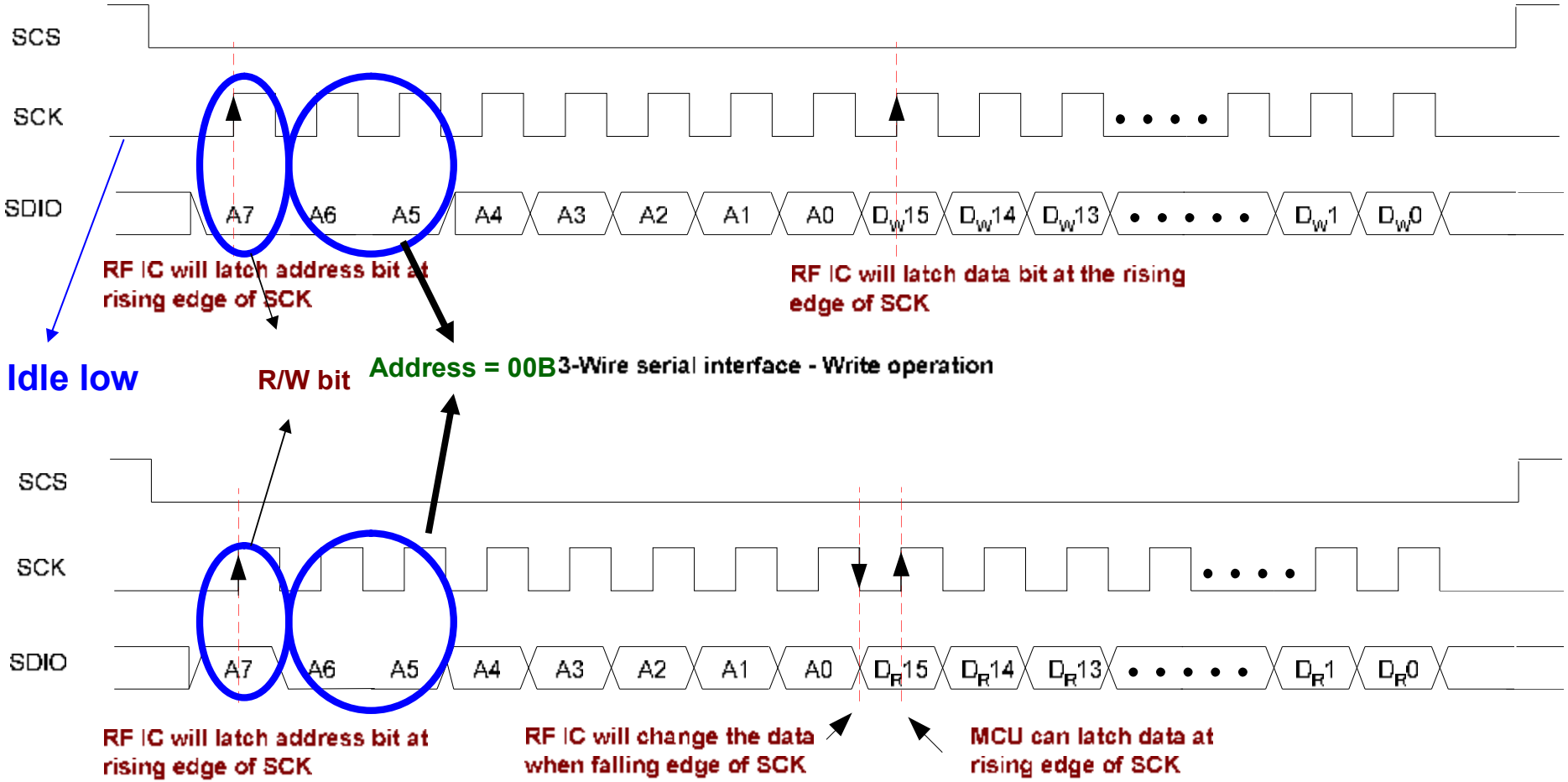
- Serial bus function

1. Enable regulator (high, 0.3ms)
2. Reset IC
3. R/W RF CTRL REG



RF interface

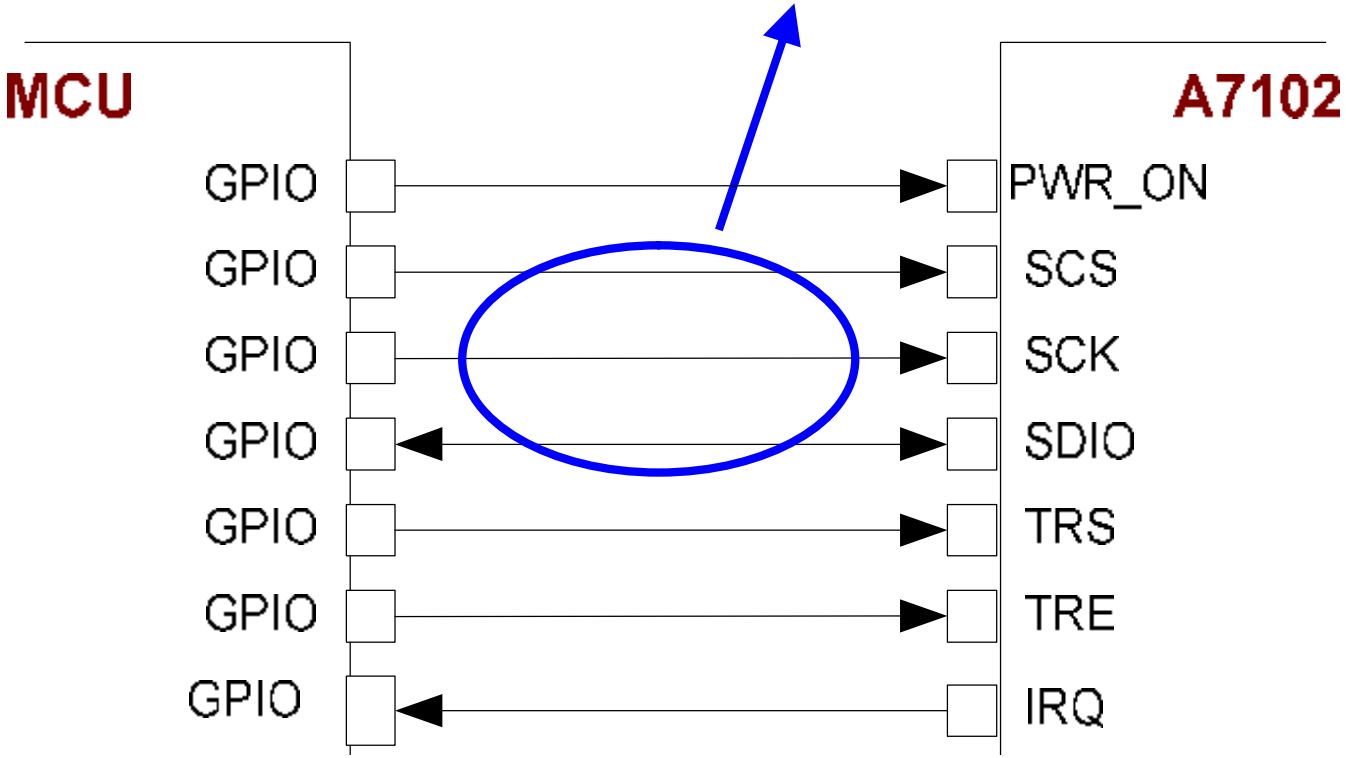
- **R/W RF CTRL REG**



RF interface

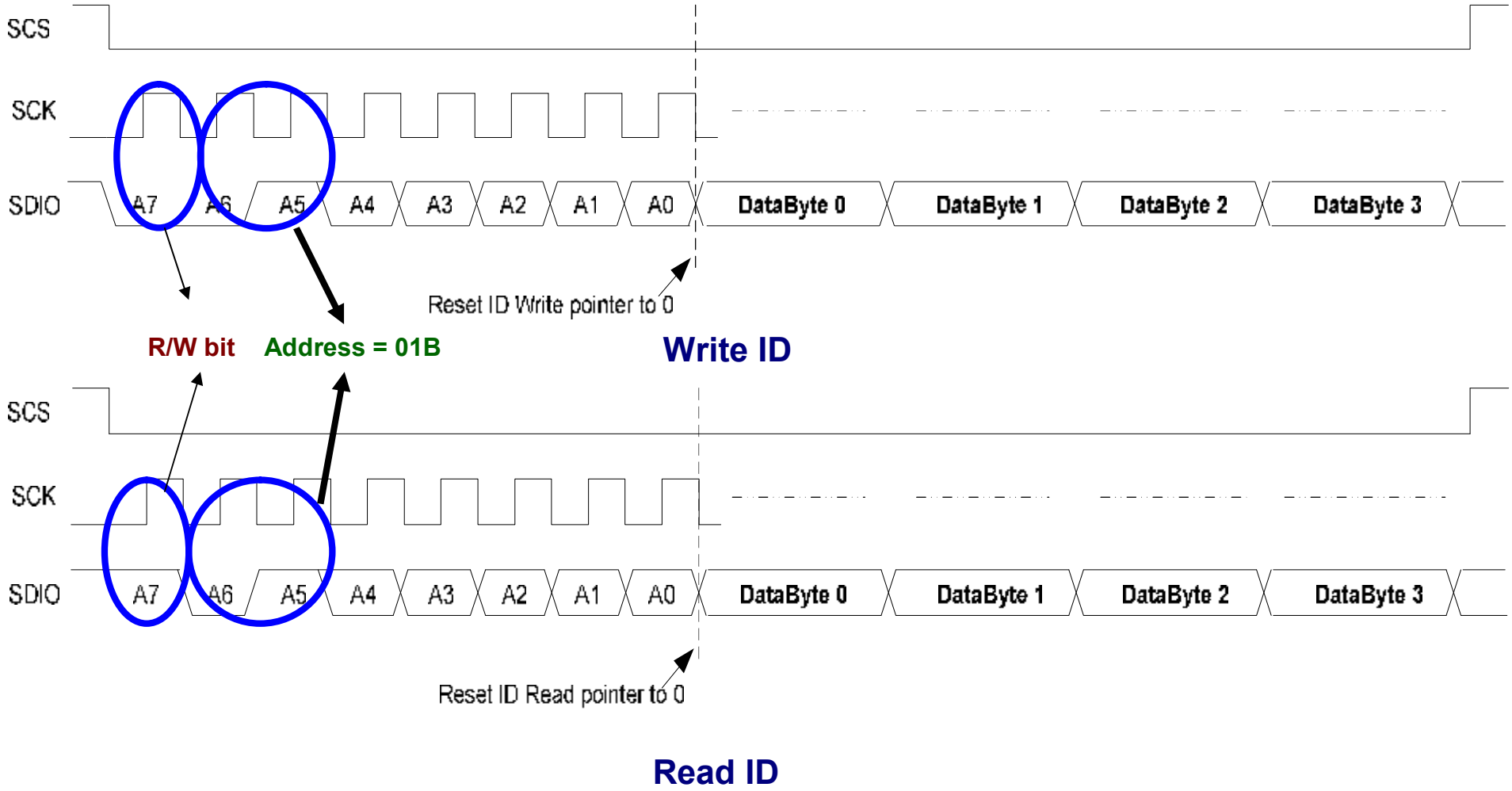
- Serial bus function

1. Enable regulator (high, 0.3ms)
2. Reset IC
3. R/W RF CTRL REG
4. R/W ID & FIFO



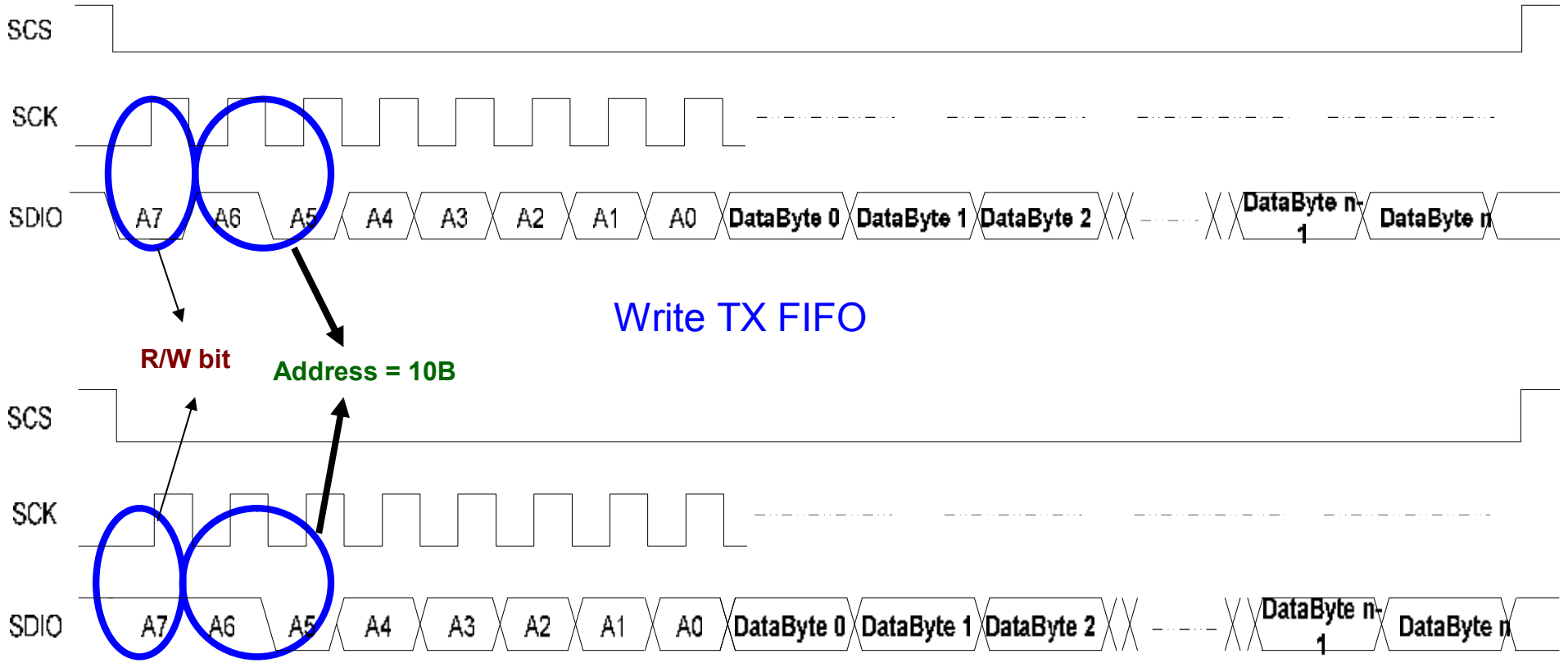
RF interface

- **R/W ID**



RF interface

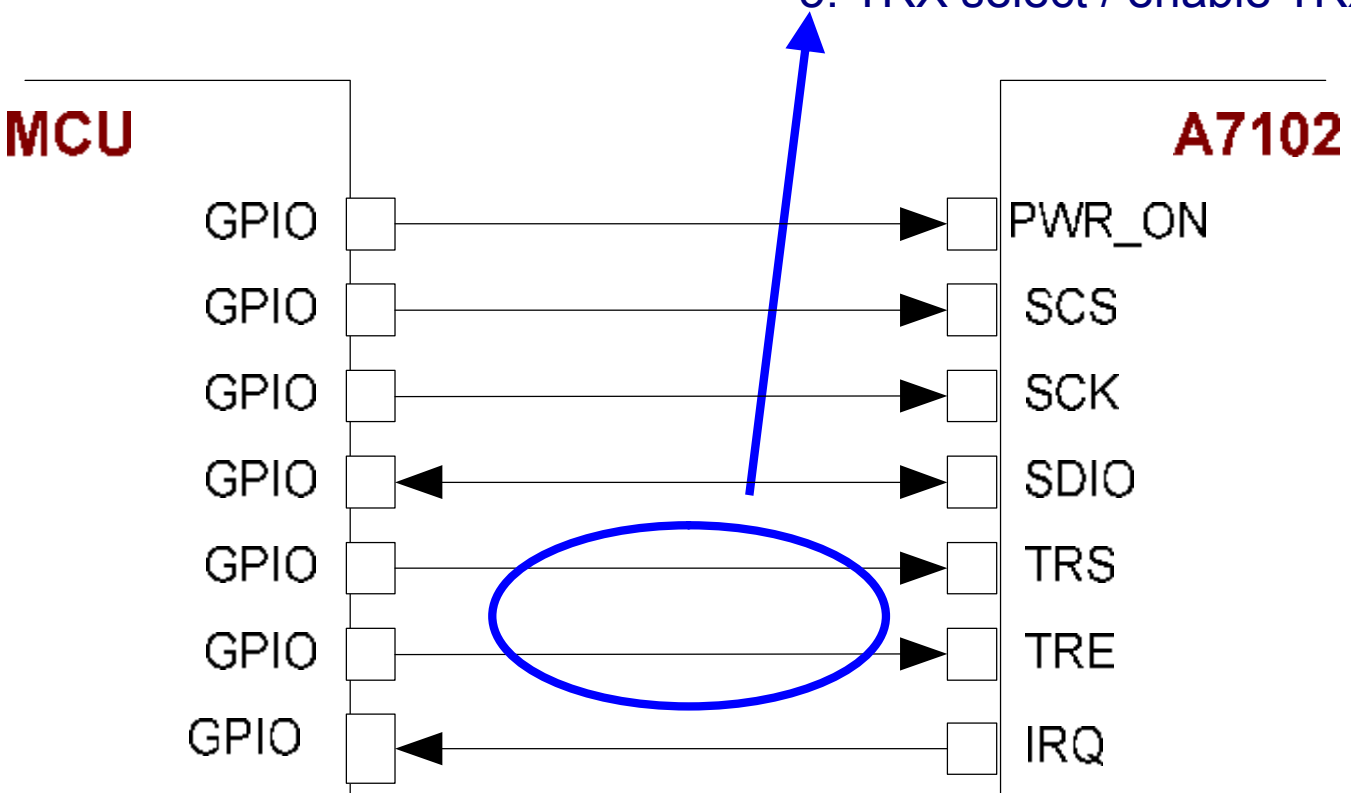
- **Read RXFIFO / Write TX FIFO**



RF interface

- Serial bus function

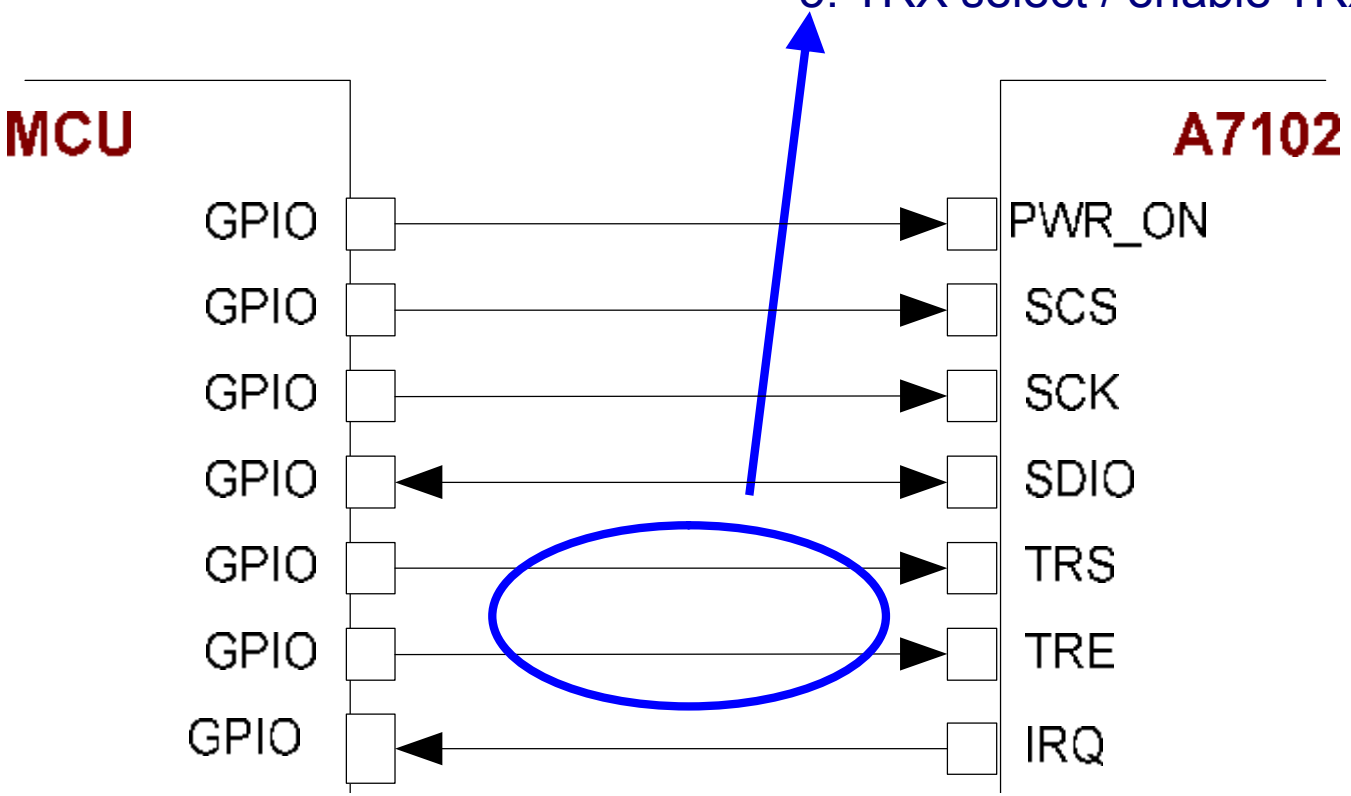
1. Enable regulator (high, 0.3ms)
2. Reset IC
3. R/W RF CTRL REG
4. R/W ID & FIFO
5. TRX select / enable TRX



RF interface

- Serial bus function

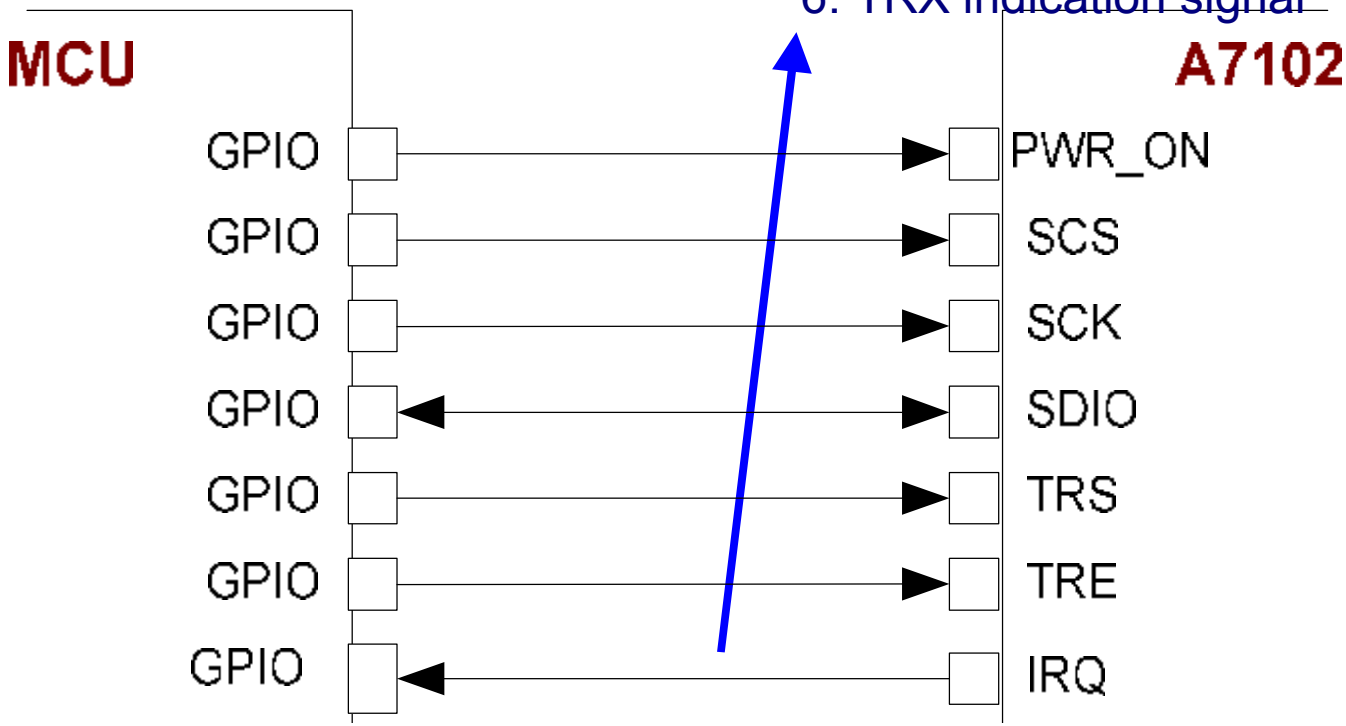
1. Enable regulator (high, 0.3ms)
2. Reset IC
3. R/W RF CTRL REG
4. R/W ID & FIFO
5. TRX select / enable TRX



RF interface

- Serial bus function

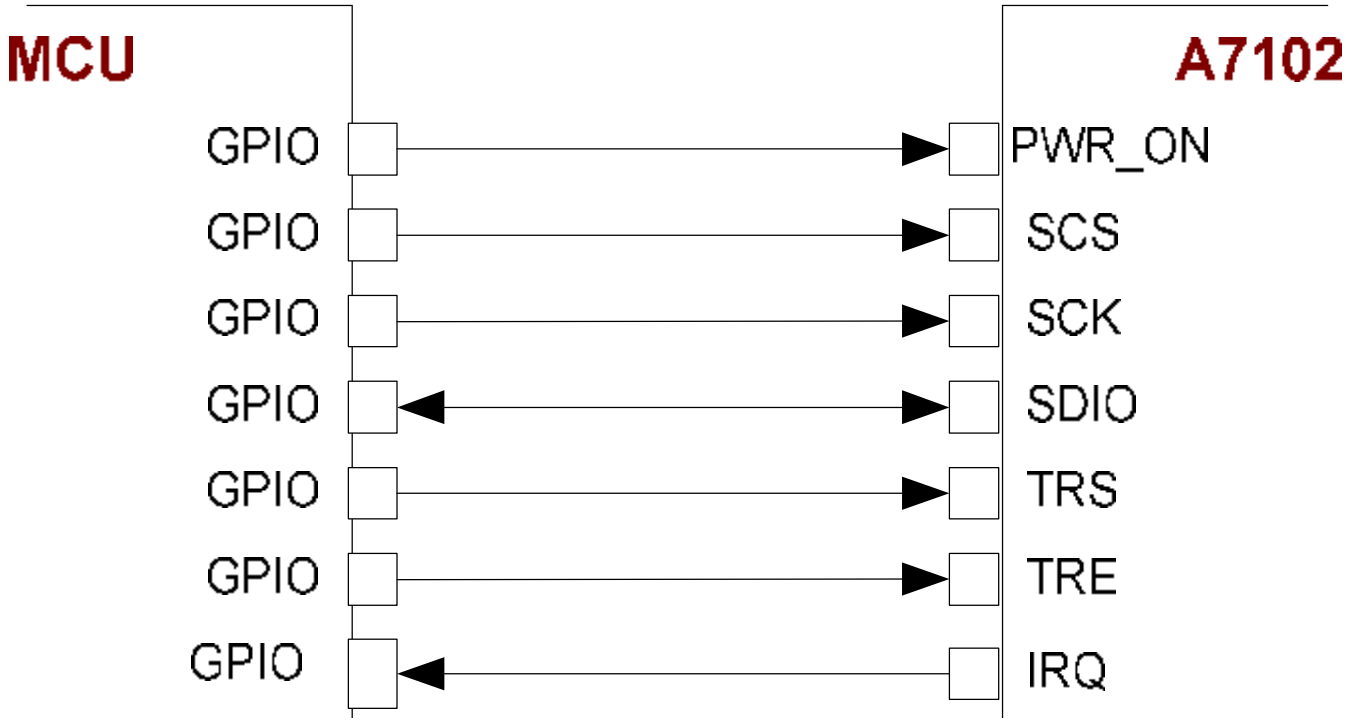
1. Enable regulator (high, 0.3ms)
2. Reset IC
3. R/W RF CTRL REG
4. R/W ID & FIFO
5. TRX select / enable TRX
6. TRX indication signal



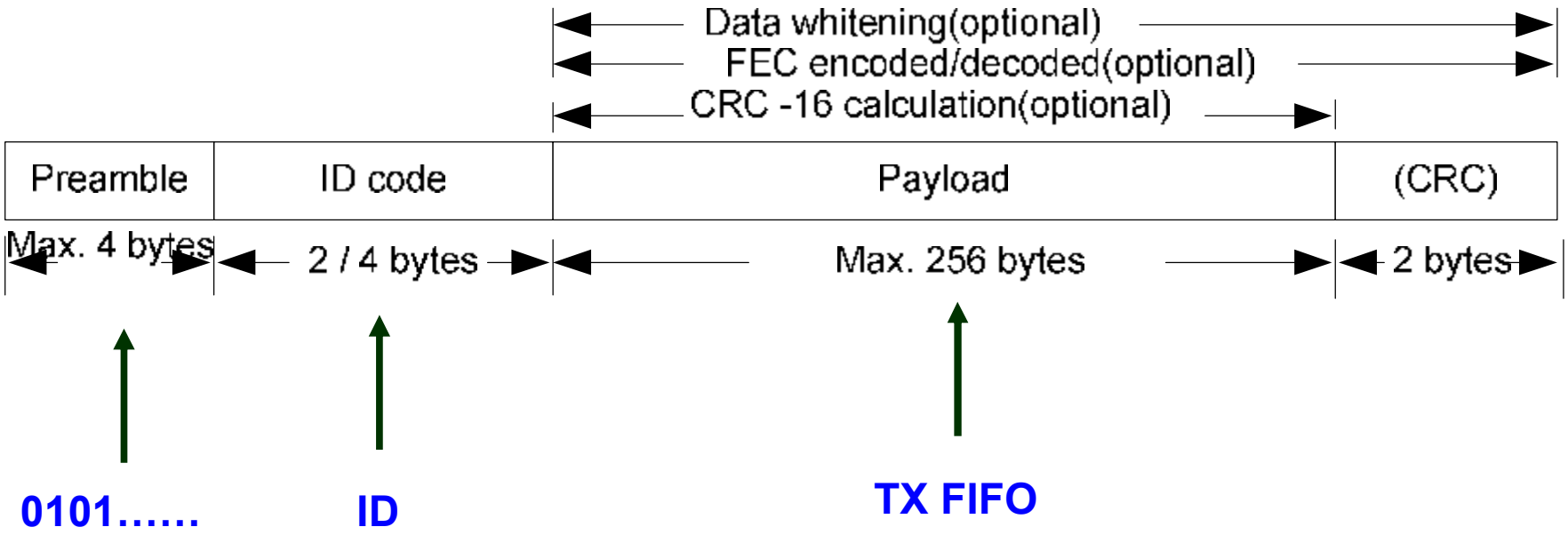
RF interface

Sleep mode, pull all pins to low except SCS pin.

* DIO pin pull to low.

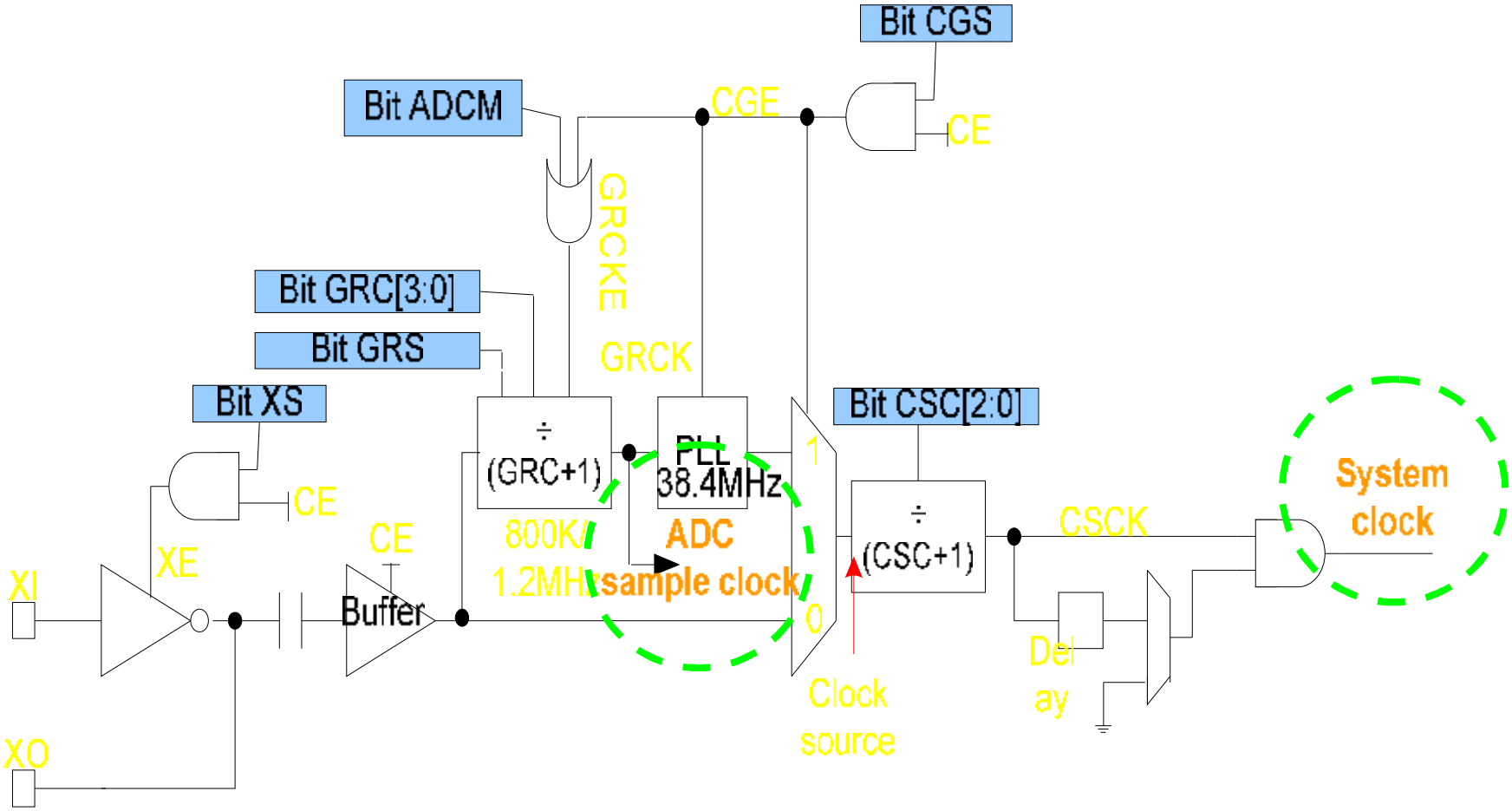


RF Format


Data whitening(optional)
FEC encoded/decoded(optional)
CRC -16 calculation(optional)
Preamble
ID code
Payload
(CRC)
Max. 4 bytes
2 / 4 bytes
Max. 256 bytes
2 bytes
0101……
ID
TX FIFO

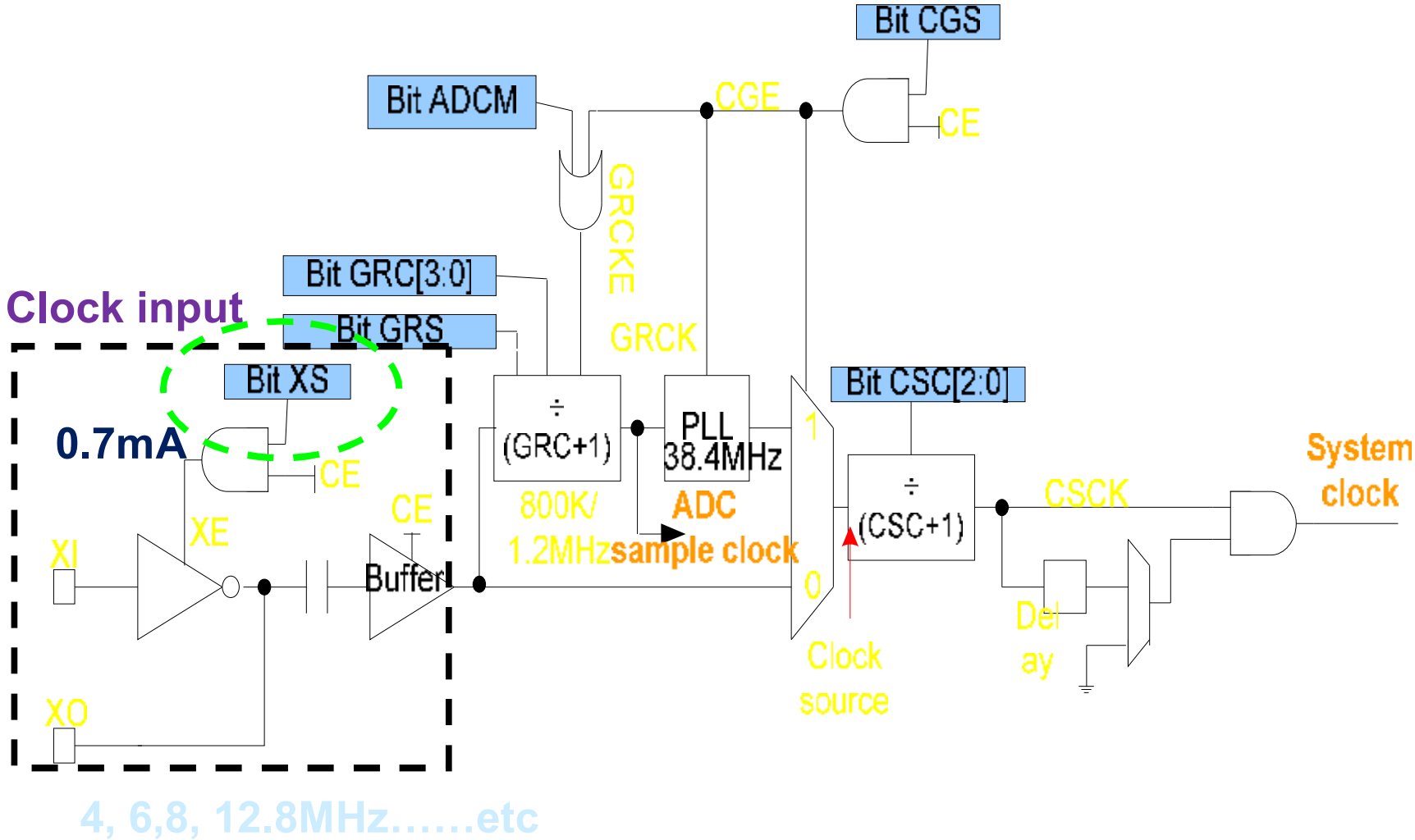
RF System Clock

Clock general circuit : ADC sample clock, system clock



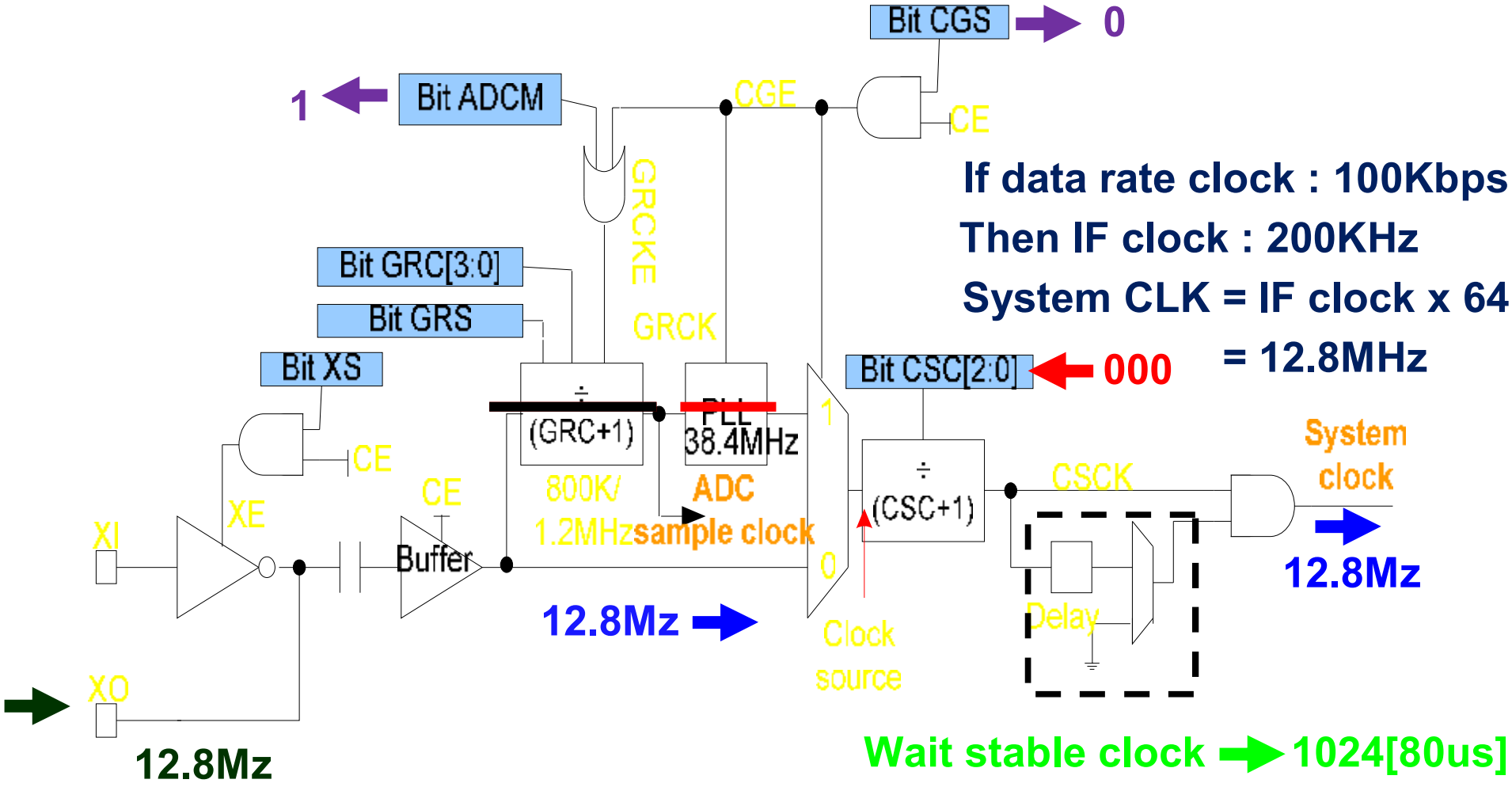
RF System Clock

Clock general circuit : ADC sample clock, system clock



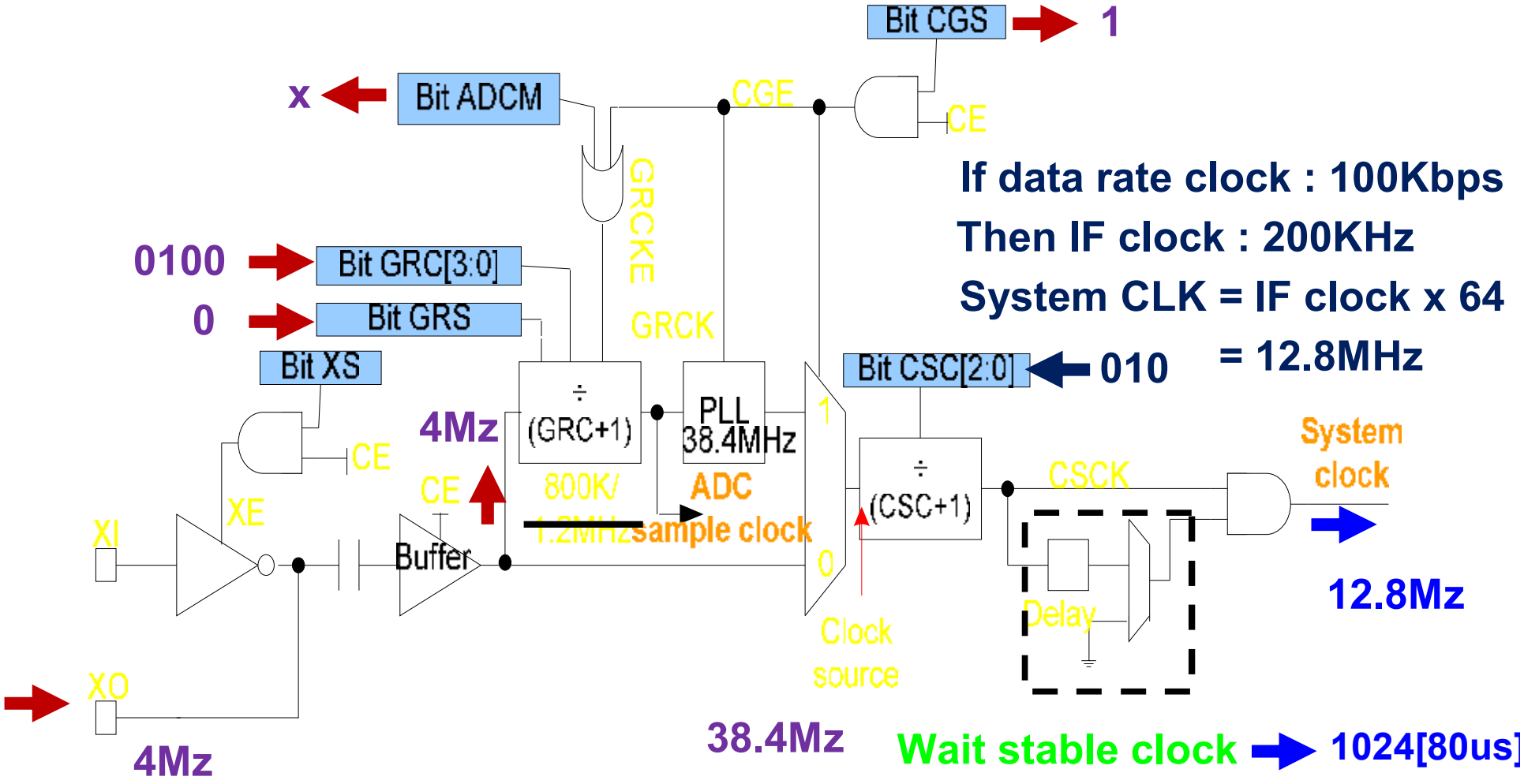
RF System Clock(12.8MHz)

Clock general circuit : ADC sample clock, system clock

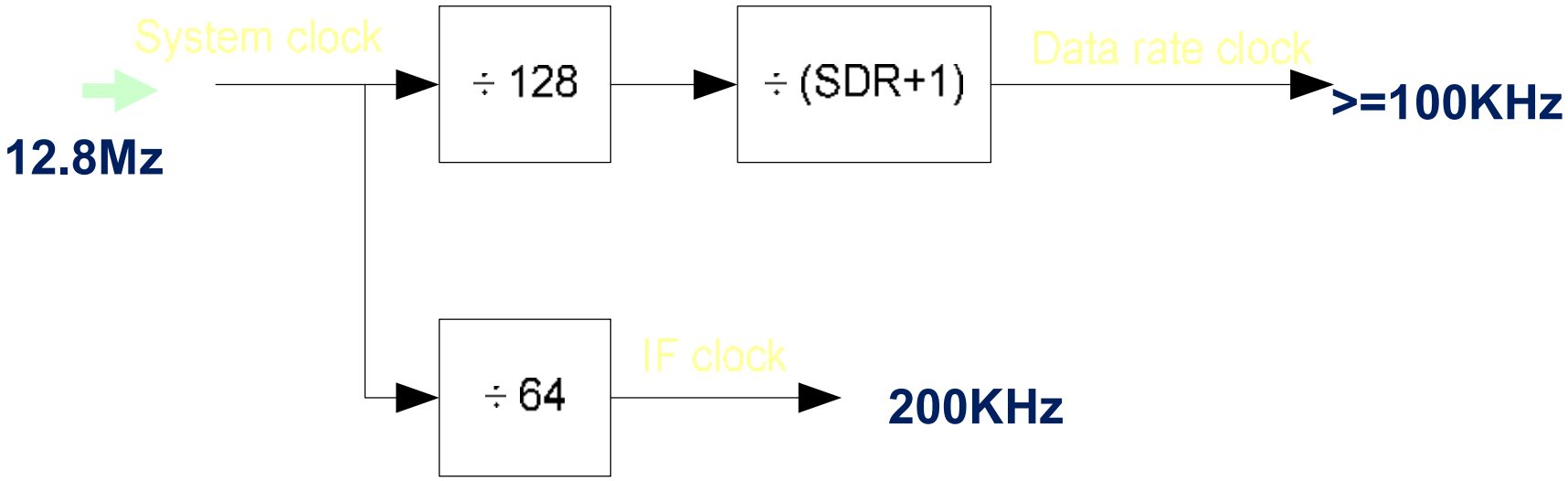


RF System Clock(4MHz)

Clock general circuit : ADC sample clock, system clock



RF Carry Clock



Difference Data Rate

X'stal = 12.8MHz

Data Rate	System Clock B2-0 / Crystal B1	System Clock / IF clock	Data Rate Veriation / SDR	TX deviation / TX I.B7-0	RX BPF / RX I.B3-2
150Kbps	000 / 1	19.2MHz / 300KHz	150Kbps / 0	56.25KHz / 0x90	150KHz / 10
100Kbps	000 / 0	12.8MHz / 200KHz	100Kbps / 0	37.5KHz / 0x60	100KHz / 01
50Kbps	001 / 0	12.8MHz / 100KHz	50Kbps / SDR+1	18.75KHz / 0x30	50KHz / 00

Difference Data Rate

X'stal = 12.8MHz, 100Kbps

Data Rate	System Clock B2-0 / Crystal B1	System Clock / IF clock	Data Rate Veriation / SDR	TX deviation / TX I.B7-0	RX BPF / RX I.B3-2
100Kbps	000 / 0	12.8MHz / 200KHz	100Kbps / 0	37.5KHz / 0x60	100KHz / 01

Adv. = X'stal, tolerance

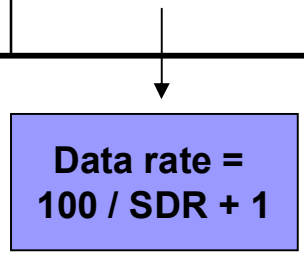
Data rate = 100 / SDR + 1

Data rate(Kbps)	Deviation(KHz)	IF Freq(KHz)	Gaussian	Sensitivity (dBm)	
				#2	#3
2	12.5	100	off	-117	-118
2	12.5	200	off	-113	-114
10	18.75	100	off	-112	-112
10	18.75	200	off	-111	-111

Difference Data Rate

X'stal = 12.8MHz, 100Kbps

Data Rate	System Clock B2-0 / Crystal B1	System Clock / IF clock	Data Rate Veriation / SDR	TX deviation / TX I.B7-0	RX BPF / RX I.B3-2
100Kbps	000 / 0	12.8MHz / 200KHz	100Kbps / 0	37.5KHz / 0x60	100KHz / 01

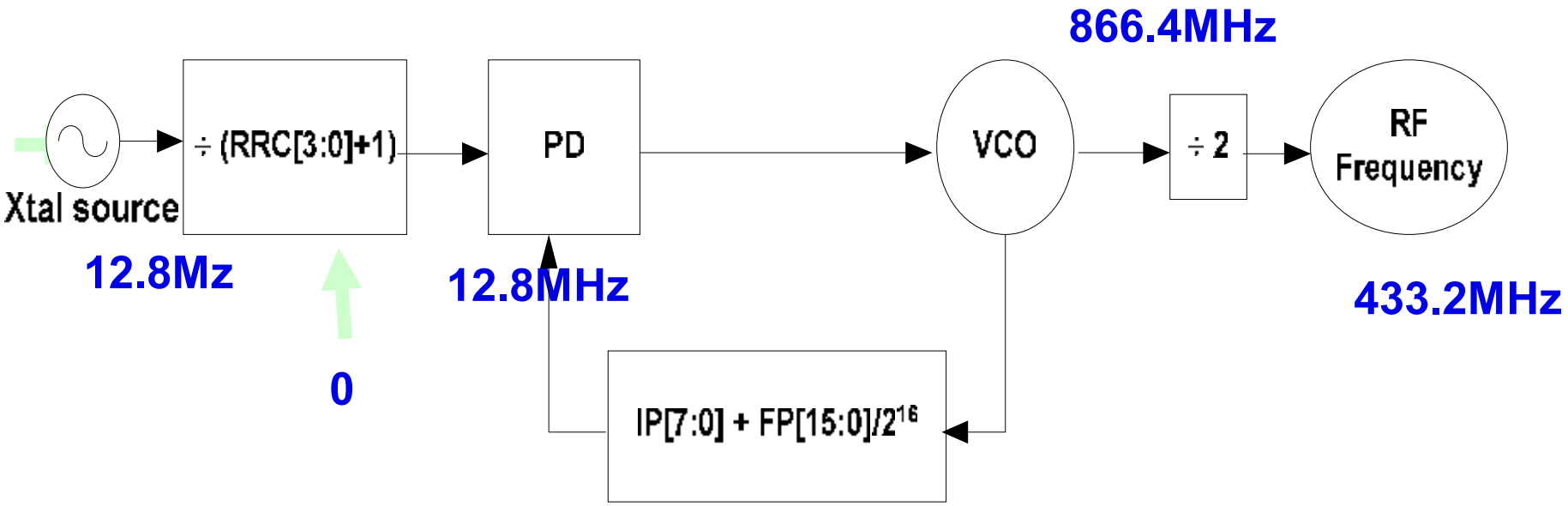


IF cal. Fail :

1. Standby mode
2. System CLK / 128 RX BPF

➔ 12.8MHz / 128 = 100KHz

RF Carry Clock



866.4MHz / 12.8MHz = 67.6875

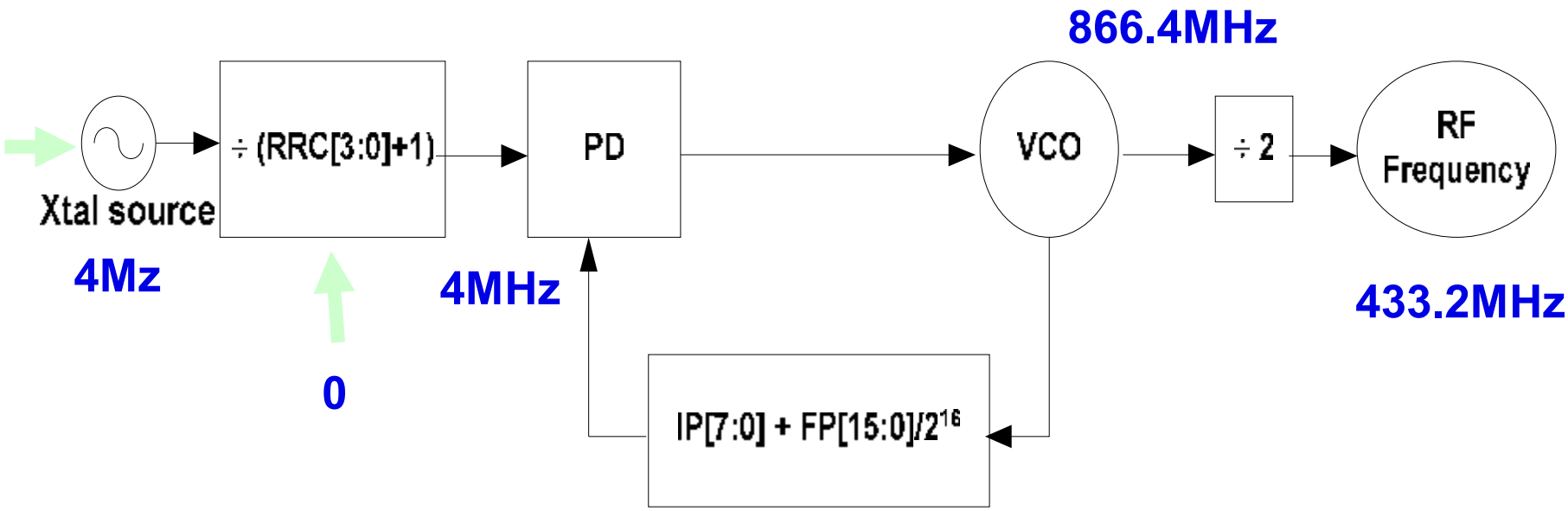
Integer part

Frac. part

IP[7:0] = 67 = 01000011_2 = 0x43

FP[15:0] = 0.6875 x 2^{16} = 45056 = 1011000000000000_2 = 0xB000

RF Carry Clock



866.4MHz / 4MHz = 216.6

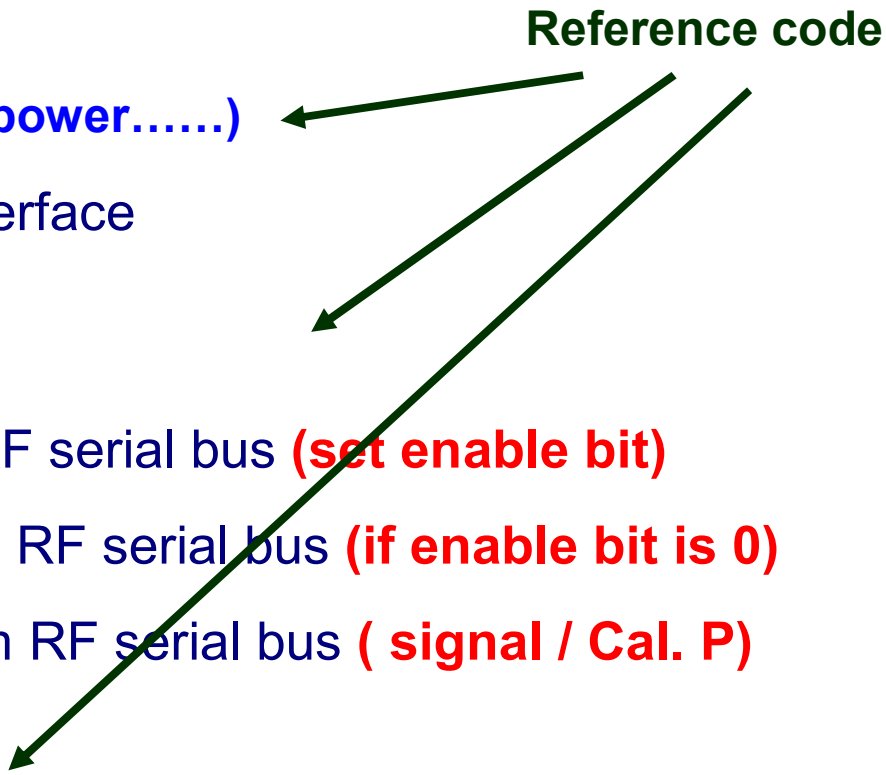
Integer part

Frac. part

$IP[7:0] = 216 = 11011000_2$

$FP[15:0] = 0.6 \times 2^{16} = 39321.6 = 1001100110011001_2$

RF Program Structure



- **Initial RF(ID, RF Freq, TX power……)**
  - Write data to RF SPI interface
- **Cal. RF(IF, VCO band)**
  - Begin → Write data to RF serial bus **(set enable bit)**
  - End → Read data from RF serial bus **(if enable bit is 0)**
  - Result→ Read data from RF serial bus **(signal / Cal. P)**
- **Run system program**
  - TX / RX / standby → Set/Clr TRS/TRE pin / Write RF CMD
  - Scan RSSI → Write RF CMD
  - Change Freq. → Write RF channel CMD

RF Debug

- Check SPI W/R
- Check Cal. Status
- Check TX Output / Frequency
- Check RX Carry Detection / RX Syn.

(315/433MHz x 4) / (868/915MHz x 2)

- Check RX Data(direct mode)
- VCO cal. fail

1.standby mode

2.Module

3.IC test ➔ VCO band 0/7[fail]

RF Debug

● Sleep current

1.PGM : initial / power down procedures

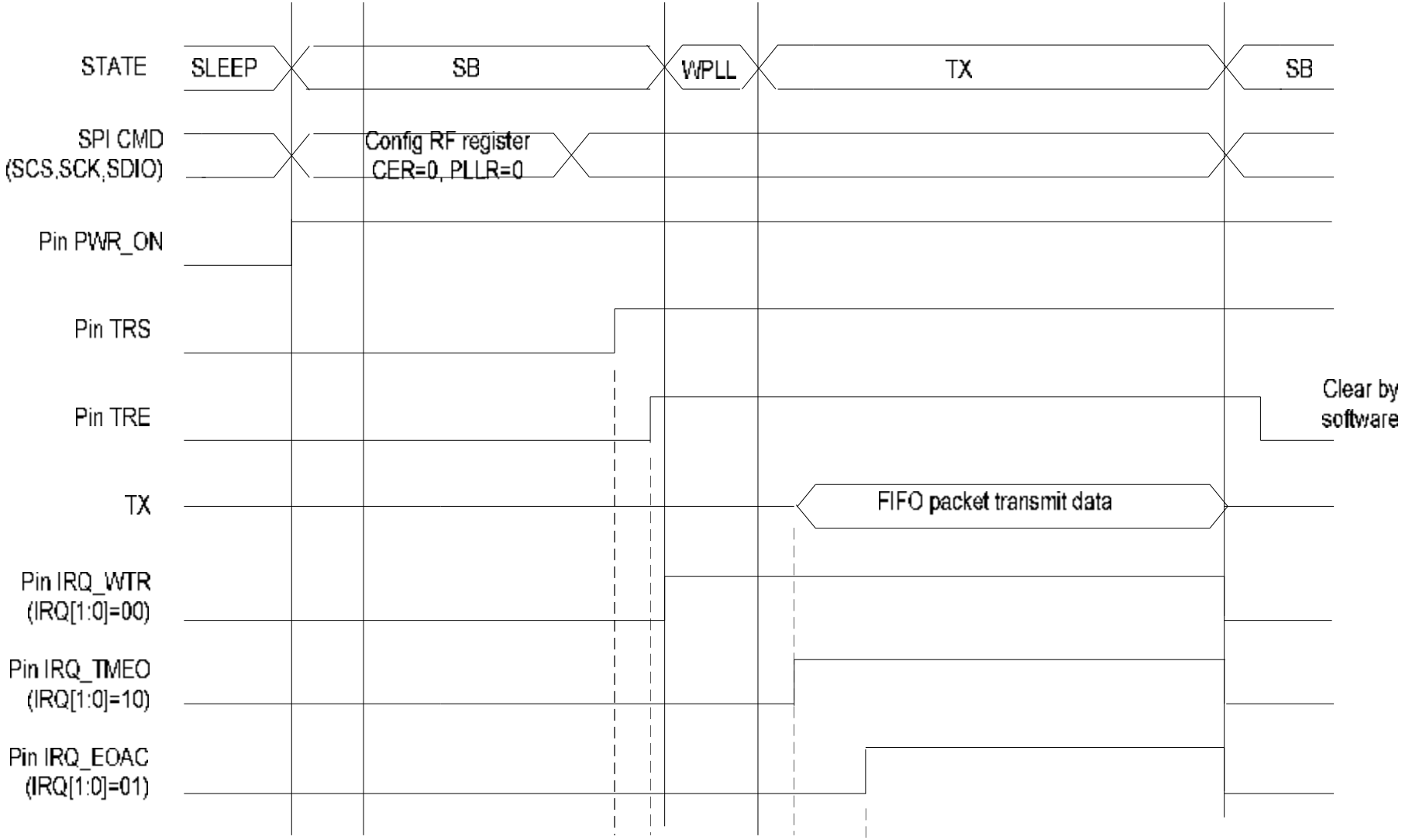
2.I/O : all CTRL I/O to low[exclude SCS] / floating I/O

```
/*********************************************************************
** initRF_M
*********************************************************************/
void initRF_M(void)
{
   //init io pin
   SCS = 1;
   SCK = 0;
   SDIO = 1;
                        PIN_TRS= 0;
                        PIN_TRE = 0;

                        PWR_ON = 1;
                        Delay100us(5);//for regulator stabilized

   A7102_Reset();//reset A7102 chip

   //Enable crystal oscillator
   A7102_WriteReg(CRYSTAL_REG, 0x0011);
   A7102_WriteReg(MODE_REG, 0x00C0);
   Delay100us(5);//for crystal stabilized

                        A7102_WriteID();//write ID code
                        A7102_Config_M();//config A7102 chip
                        A7102_Cal();//calibration IF,vco
                        A7102_FIFOInit();//init T/RX FIFO
                        InitTemp = MeasureTemp();//record init temperature
}
```

```
/*********************************************************************
** A7102_PowerDown
*********************************************************************/
void A7102_PowerDown(void)
{
  A7102_WriteReg(MODE_REG, 0x00C0);
  A7102_WriteReg(MODE_REG, 0x0080);//CER=0
  A7102_WriteReg(PIN_REG, 0x0000);//IRQE=0, CKOE=0
  A7102_WriteReg(SYSTEMCLOCK_REG, 0x0078);//clear SDR[6:0]=0, CSC[2:0]=0
  A7102_WriteReg(CRYSTAL_REG, 0x0010);//XS=0
  SCK  = 0;
  SDIO = 0;
  CKO = 0;
  IRQ = 0;
  PIN_TRS = 0;
  PIN_TRE = 0;
  //DIO = 0; //hardware pin DIO=0
  PWR_ON = 0;
}
```

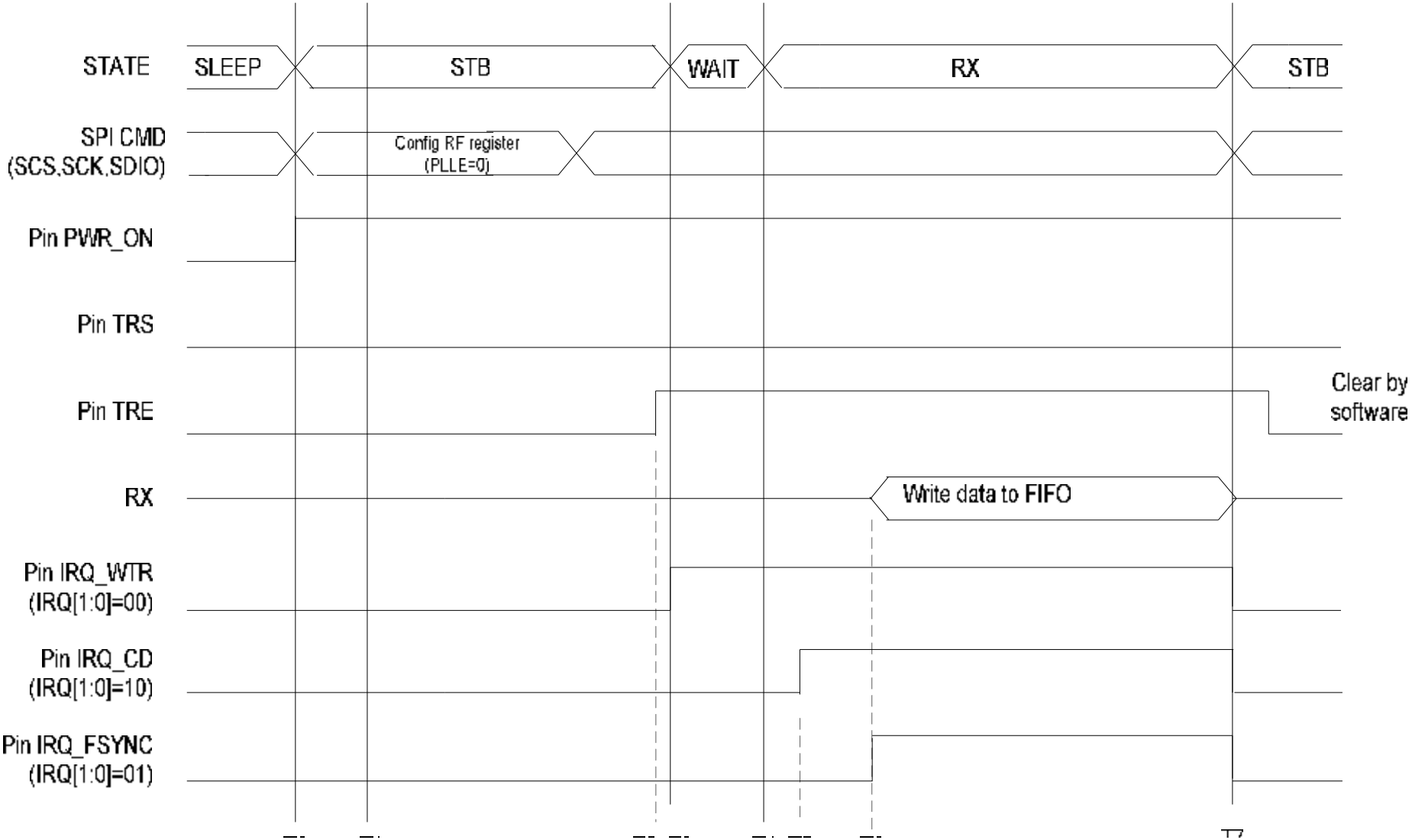
RF Operation

- **FIFO TX**

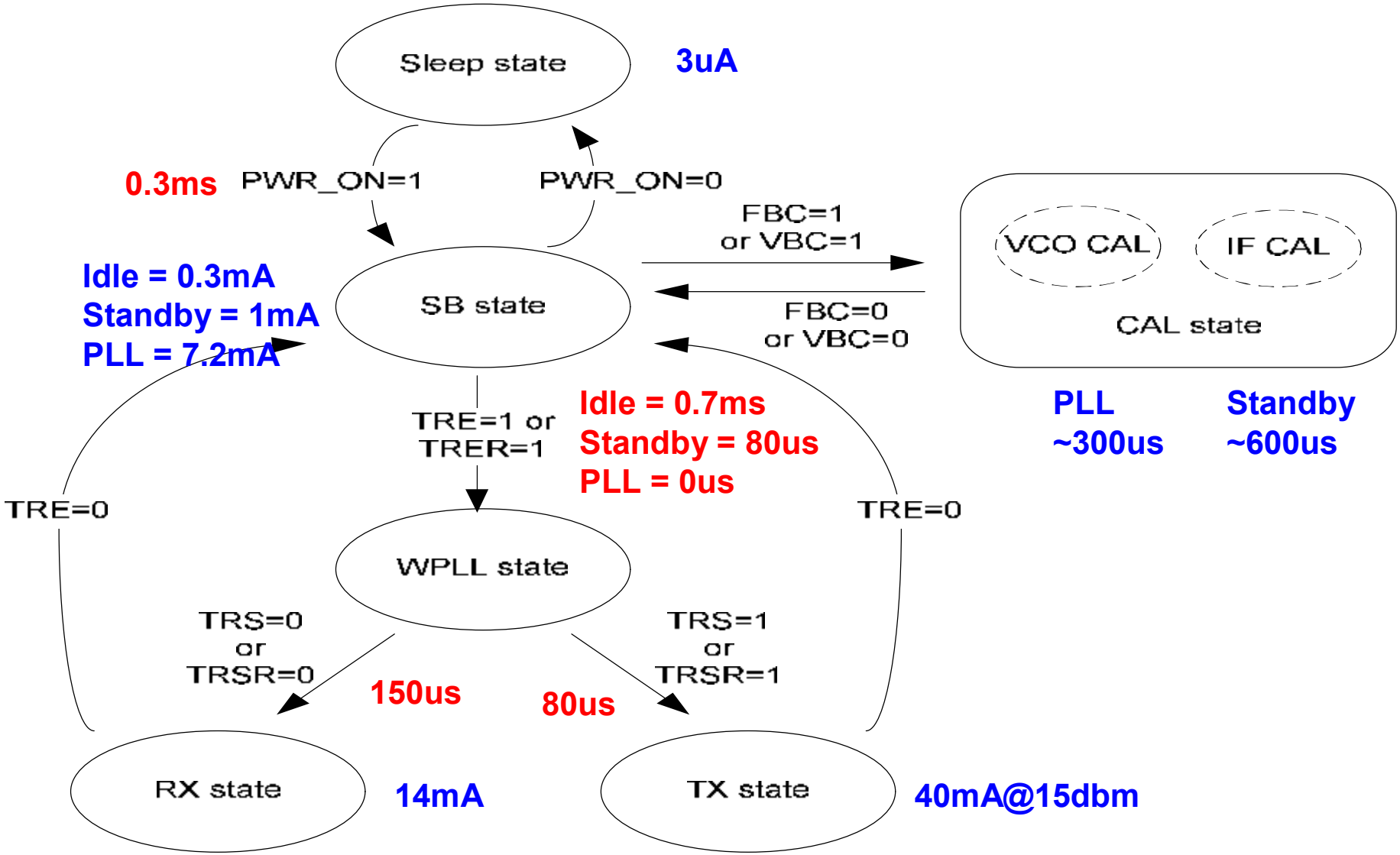


RF Operation

- **FIFO RX**



RF State Machine



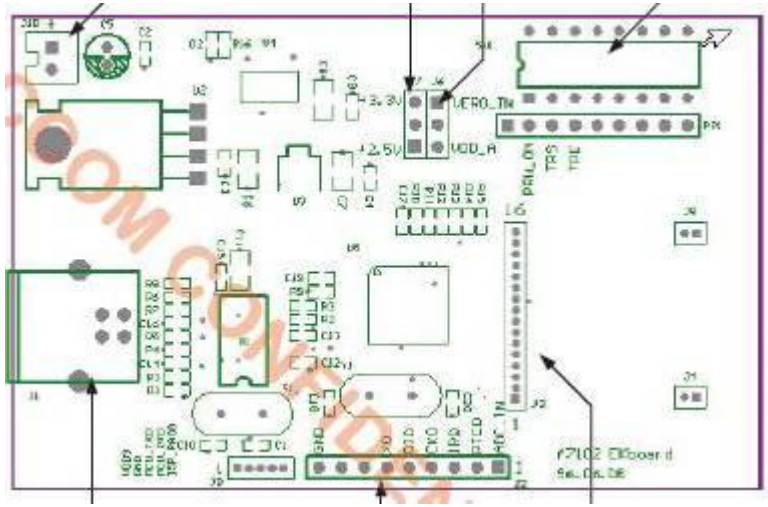
RF System Development tool

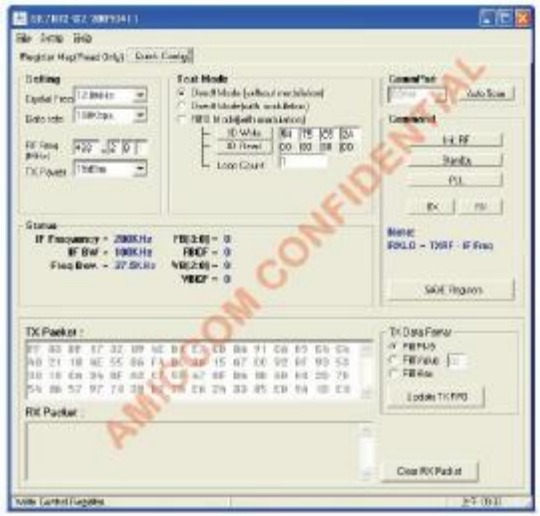
RF Module x 4 type

➔3xx, 4xx, 8xx, 9xxMHz

RF DK kit(demo, develop)

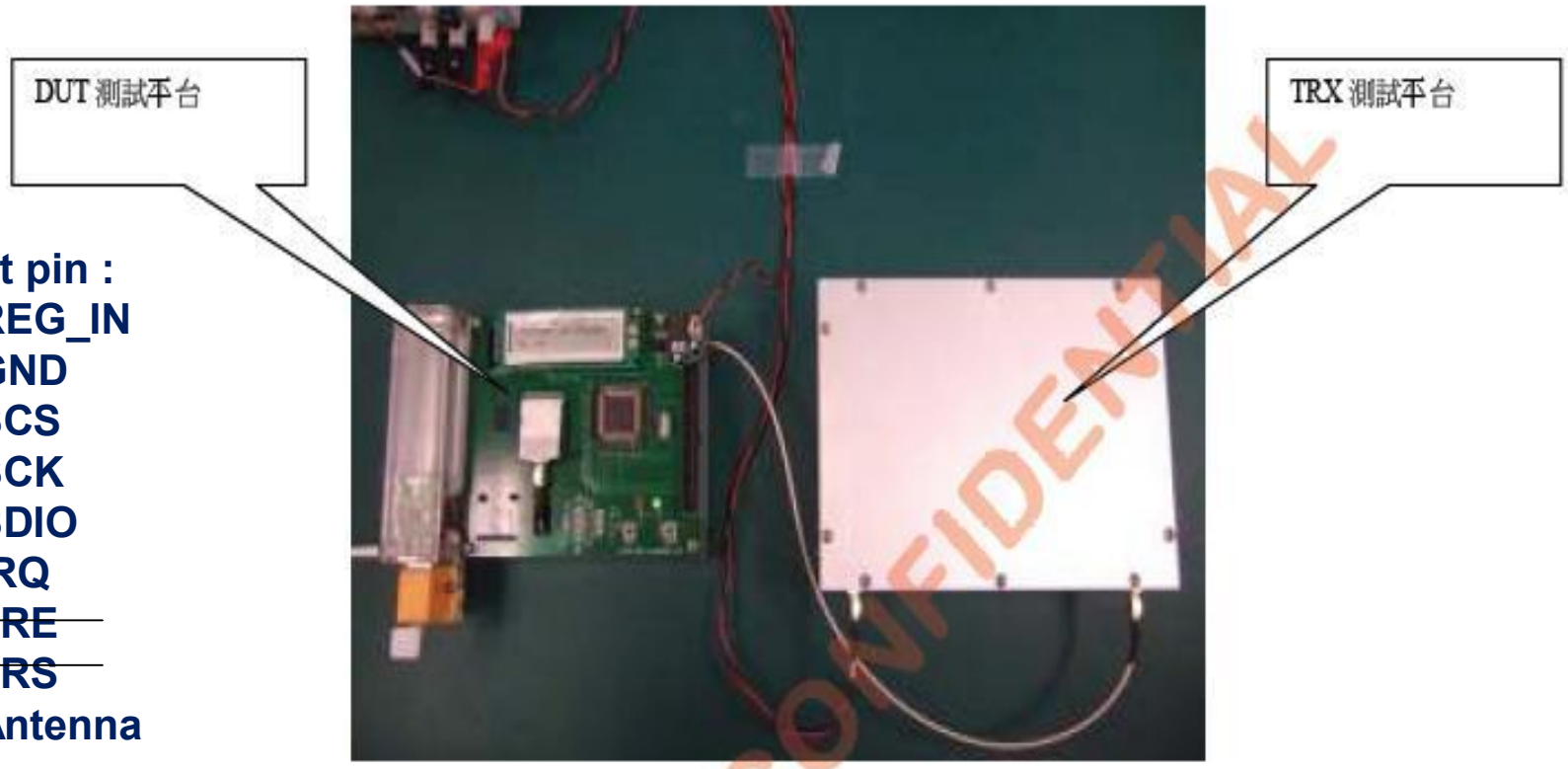
RF EK kit(test RF performance)





RF System Development tool

Testfixture for Mass production



Test pin :

1. REG_IN
2. GND
3. SCS
4. SCK
5. SDIO
6. IRQ
7. ~~TRE~~
8. ~~TRS~~
9. Antenna