19ECE382 COMMUNICATION SYSTEMS LABORATORY

REPORT

ELECTRONICS AND COMMUNICATION ENGINEERING

AMRITA SCHOOL OF ENGINEERING

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January - 2022

Certified that this is the bonafide record of work done by

Mr/Ms……………………M.R.NIGIL……………………………………….

RollNo……CB.EN.U4ECE19136………of………B.TECH…………………….Semester……5……...

(Branch)…ELECTRONICS AND COMMUNICATION ENGINEERING……………….in the

……………19ECE382 COMMUNICATION SYSTEMS……………………………………Lab

oratory of this institute during the academic year………2019 - 2023…………

Faculty-in-Charge

Chairman of the Department

The candidate is examined by me/us.

on………01-02-2022…………………

(Date)

Examiner 1

Name: **M.R.NIGIL**

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19ECE382 Communication Systems Lab.

Exp No:1 20-01-2022

Amplitude Modulation and Demodulation

Nigil. MR
CB.EN.U4ECE19136.

RHS:-

Aim:-

To set up and study simple circuit using a transistor to demonstrate the concepts of modulation and demodulation.

Components Required:-

Equipment	Specification/ Range	Quantity
Transistor	SL100	1
Diode	OA79/IN4007	1 each
Resistors	220kΩ, 56kΩ, 1kΩ, 330kΩ	1 each
capacitors	1nF, 100nF, 1μF	1, 1, 3
Inductors	100 μH	1
Regulated Power supply	0-30V	1
Digital storage Oscilloscope		1.
Function Generator		2.

Theory:

Amplitude modulation is defined as the process in which the amplitude of the carrier wave c(t) is varied linearly with the instantaneous amplitude of the message signal m(t). The standard form the amplitude modulated wave is defined as

$$\boxed{s(t) = A_c\,[1 + k_a m(t)] \cos 2\pi F_c t}$$

where k_a is called amplitude sensitivity of the modulator.

The Demodulation is the process of recovering the message signal from the incoming AM wave at the receiver. An Envelop detector is simple and yet highly effective device that is well suited for the demodulation of AM wave for which the % of modulation is less than 100%. An envelop detector produces an output signal that follows the envelop of the input wave exactly.

$$\boxed{\text{Modulation Index } (m) = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}}$$

Procedure:

1. Consider the circuit shown in Fig1. Set up the amplifier consisting of the BJT Q_1 and the resistors R_1 and R_2 along with R_E and bypass capacitor C_B. The tuned circuit / tank circuit is formed by L and C and is part of the load impedance of the amplifier.

2. Set $V_{CC} = 10V$. The values of the various components are as follows : $R_1 = 220\,k\Omega$; $R_2 = 56\,k\Omega$; $R_E = 1k\Omega$ $L = 100\mu H$; $C = 100nF$. The emitter bypass capacitance may be assumed to be as large as $1\mu F$. Please Note all capacitors are of ceramic type. For measuring the "operating points" fc and fm which are the two function generator need not be connected.

3. Determine the quiescent point (Q) of the transistor and note down your readings in Table 1.

4. Now, connect up the function generator fc and fm as shown in Fig 1, where fc stands for the carrier frequency and fm represent the modulating frequency. The function generator fc may be set to an amplitude of 5V and a frequency close to 500KHz as possible.

Similarly fm may be adjusted to provide a single signal of amplitude 2V or less and of frequency 1KHz. Verify both fc and fm using the oscilloscope.

5. The coupling capacitor Cc may be taken as $1\mu F$ (ceramic).

6. Note down the waveform at V_o (you might have to adjust fc and fm to obtain a clean waveform at V_o).

7. For different values of the amplitude of fm. calculate the modulation index in each case.

8. For demodulation, connect the output of the modulator (Fig 1) to the input of Fig 2. Plot the waveform obtained at the output. V_o'.

For the Fig 2 The diode D_1 is the OA79/IN914. R' is chosen as 330kΩ and C' as 1nF.

9. Replace the diode D_1 with IN4007/IN4148 and plot the output waveform.

LHS :-

Table 1 :-

Operating point of Transistor

V_B	1.8632 V
V_C	10 V
V_E	1.20509 V
I_E	0.0012059 mA

Circuit Diagram :-

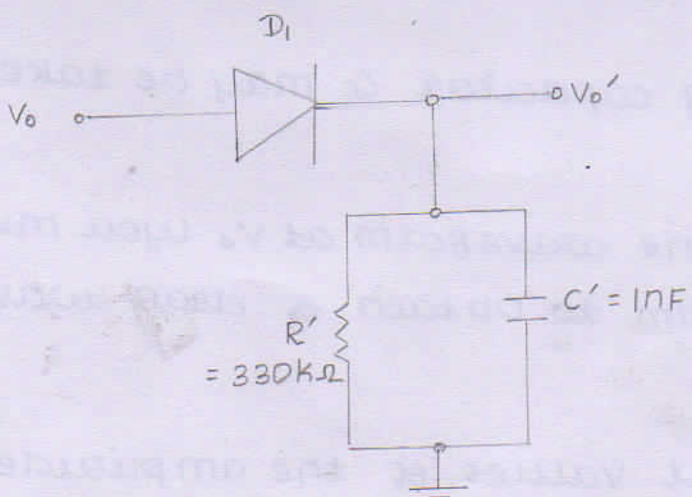

Fig 2

Circuit Diagram :-

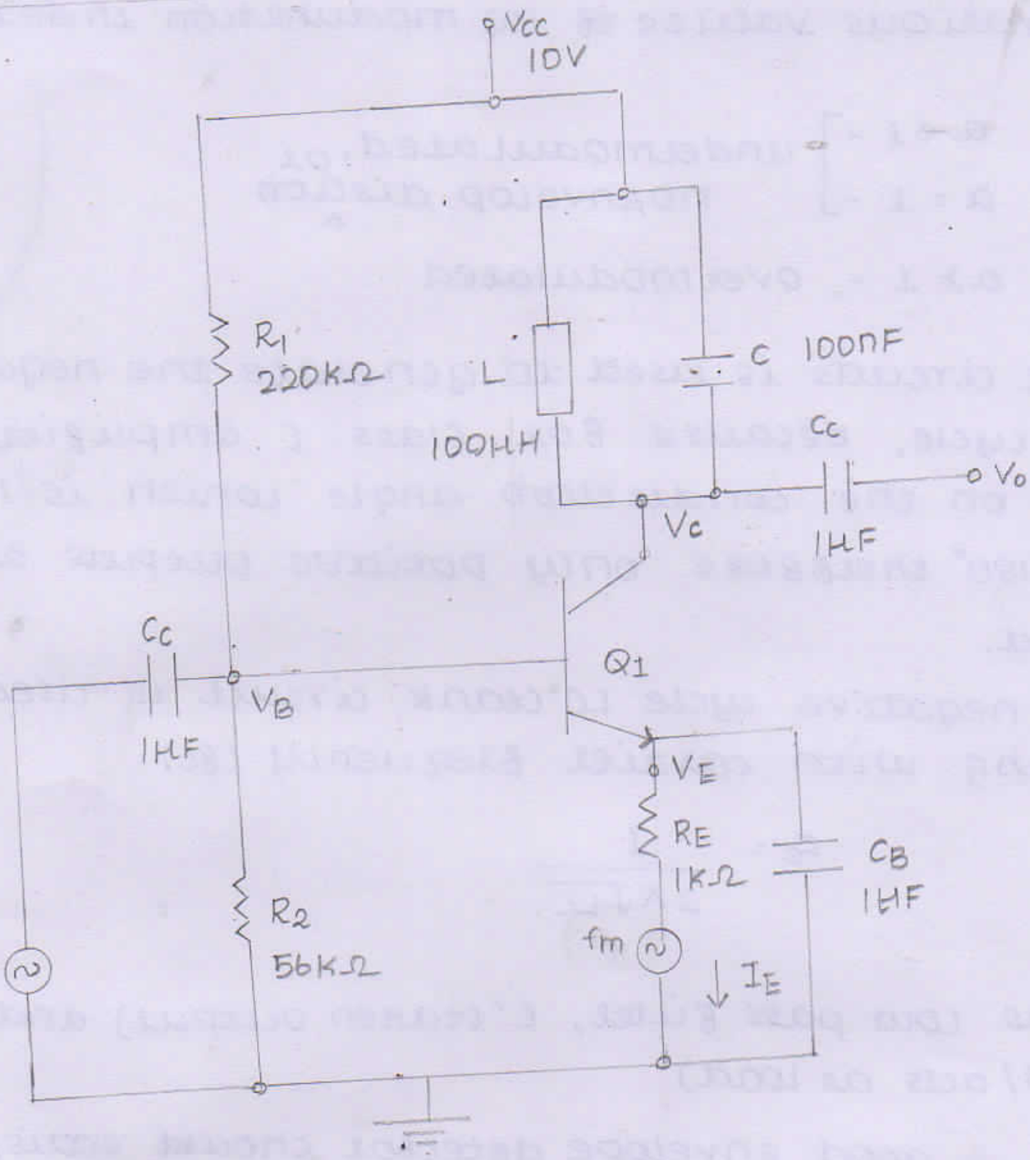

Fig 1

Results :-

Answer the following :-

1. In which region is the transistor Q_1 biased ? What would be gain of the amplifier ? What class of amplifier?

Ans :-

* Class C, Power Amplifier.
* switches between active & cutoff because biasing signal varies. with fm.

Results

Operating Points

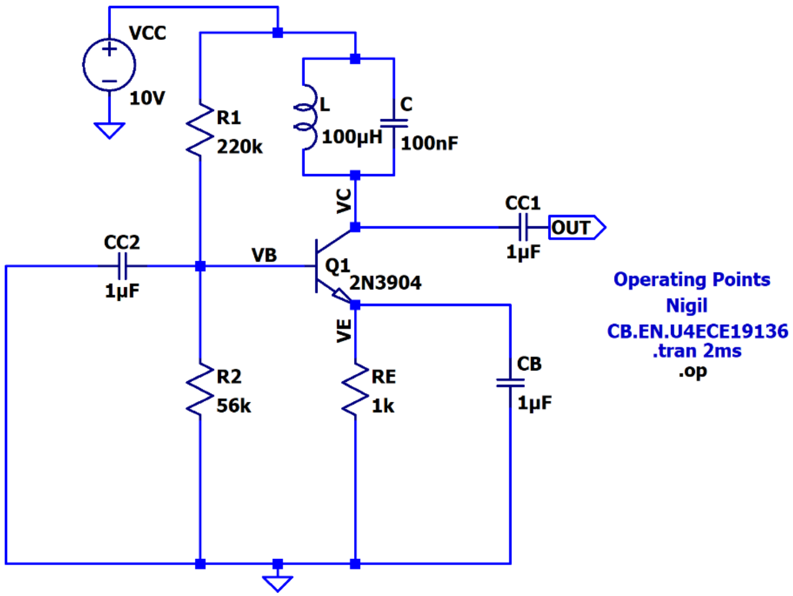

Fig 1 Circuit Diagram

* C:\Users\amrit\Documents\LTspiceXVII\ECE382 Experiment 1 - Amplitude Modulation Operating Points.asc

--- Operating Point ---

V(vc):	10	voltage
V(vb):	1.86322	voltage
V(ve):	1.20509	voltage
V(n001):	10	voltage
V(out):	9.99999e-006	voltage
Ic(Q1):	0.00120138	device_current
Ib(Q1):	3.71353e-006	device_current
Ie(Q1):	-0.00120509	device_current
I(Cc2):	1.86322e-018	device_current
I(Cc1):	-9.99999e-018	device_current
I(Cb):	1.20509e-018	device_current
I(C):	1.20138e-025	device_current
I(L):	0.00120138	device_current
I(R1):	3.69854e-005	device_current
I(R2):	3.32718e-005	device_current
I(Re):	0.00120509	device_current
I(Vcc):	-0.00123836	device_current

Fig 2 Operating Points

Amplitude Modulation

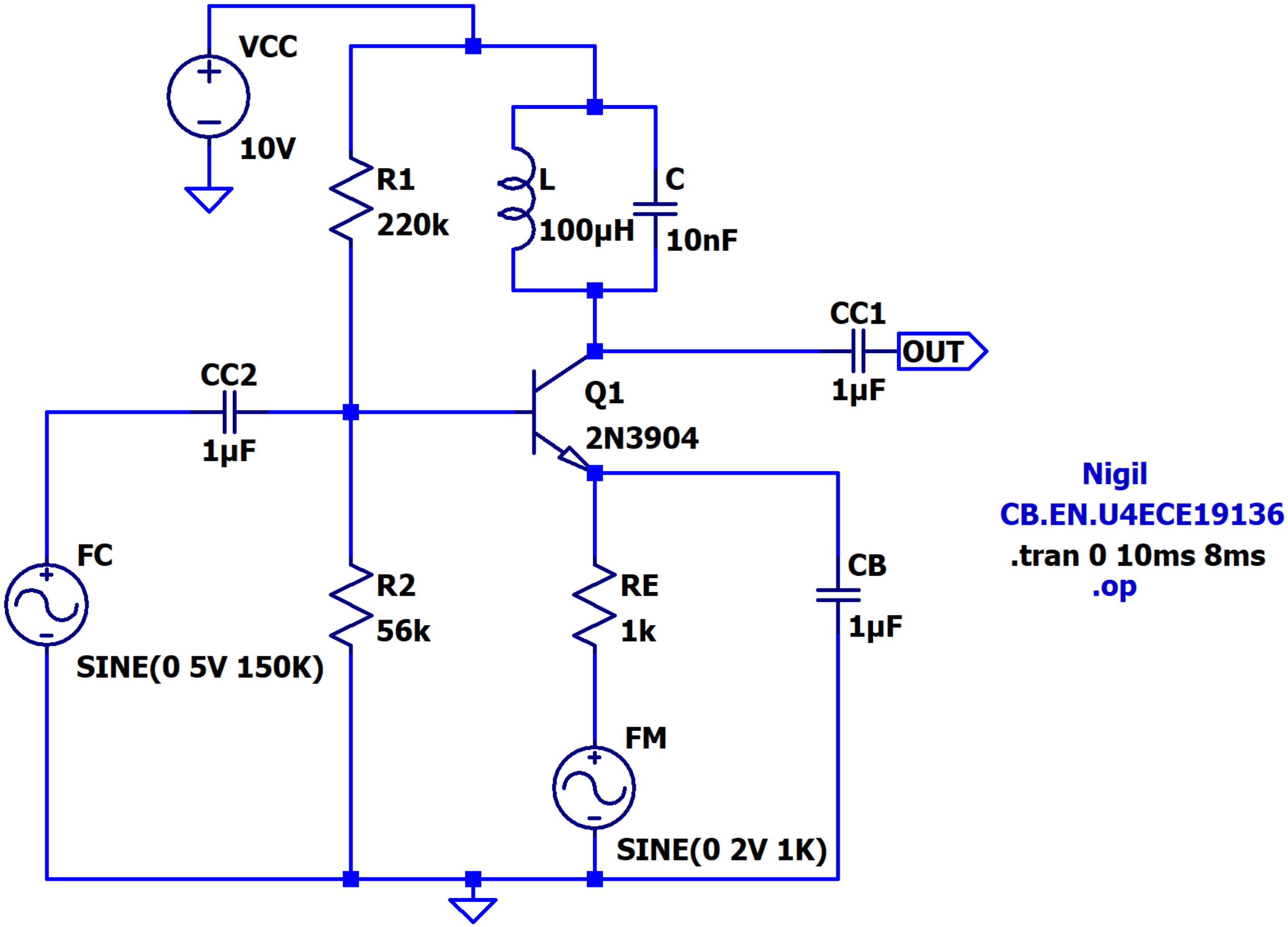

Fig 3 Circuit Diagram – Amplitude Modulator

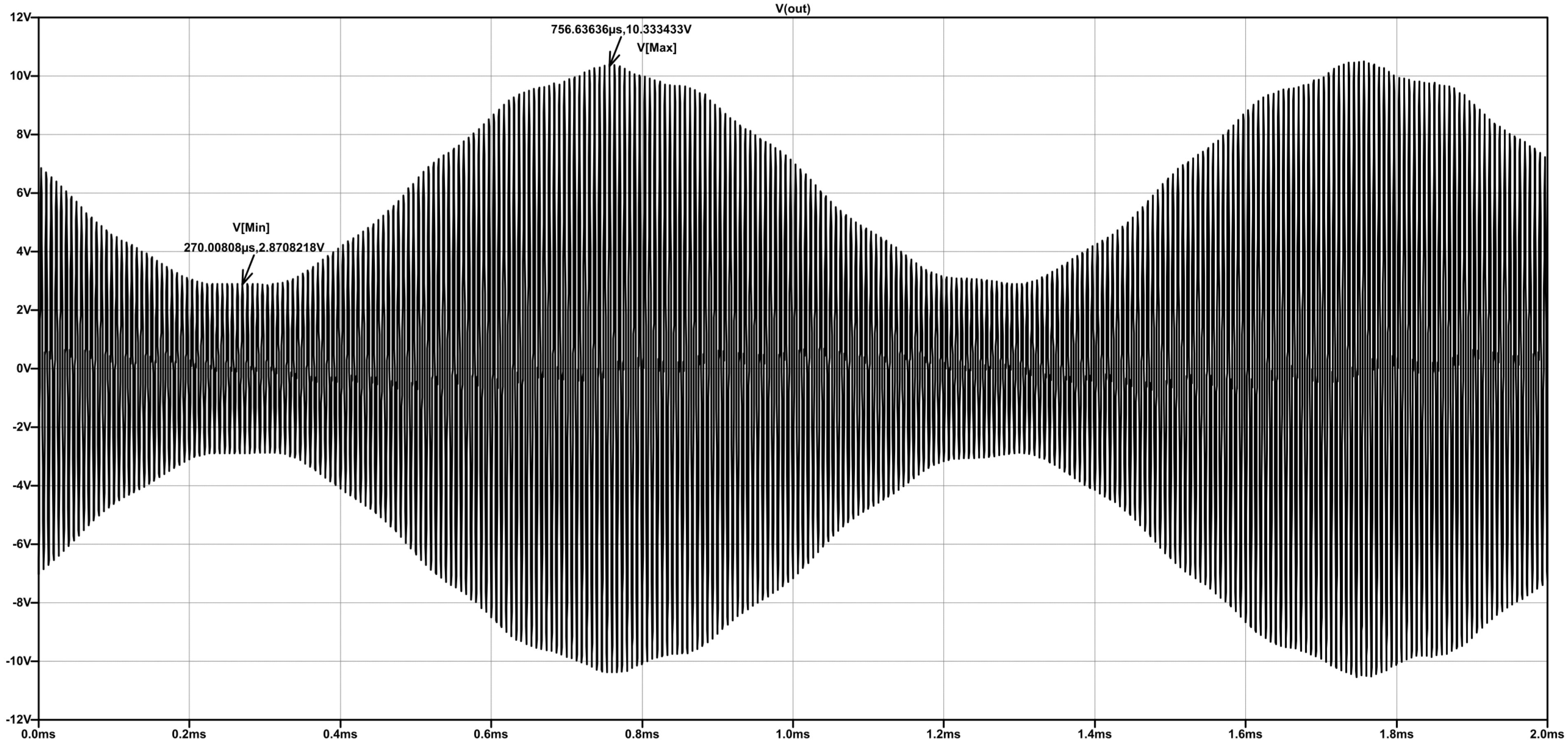

Fig 4 Modulated Output Modulated Waveform

Modulation Index - 53.4 %

Amplitude Demodulation – Envelope Detector

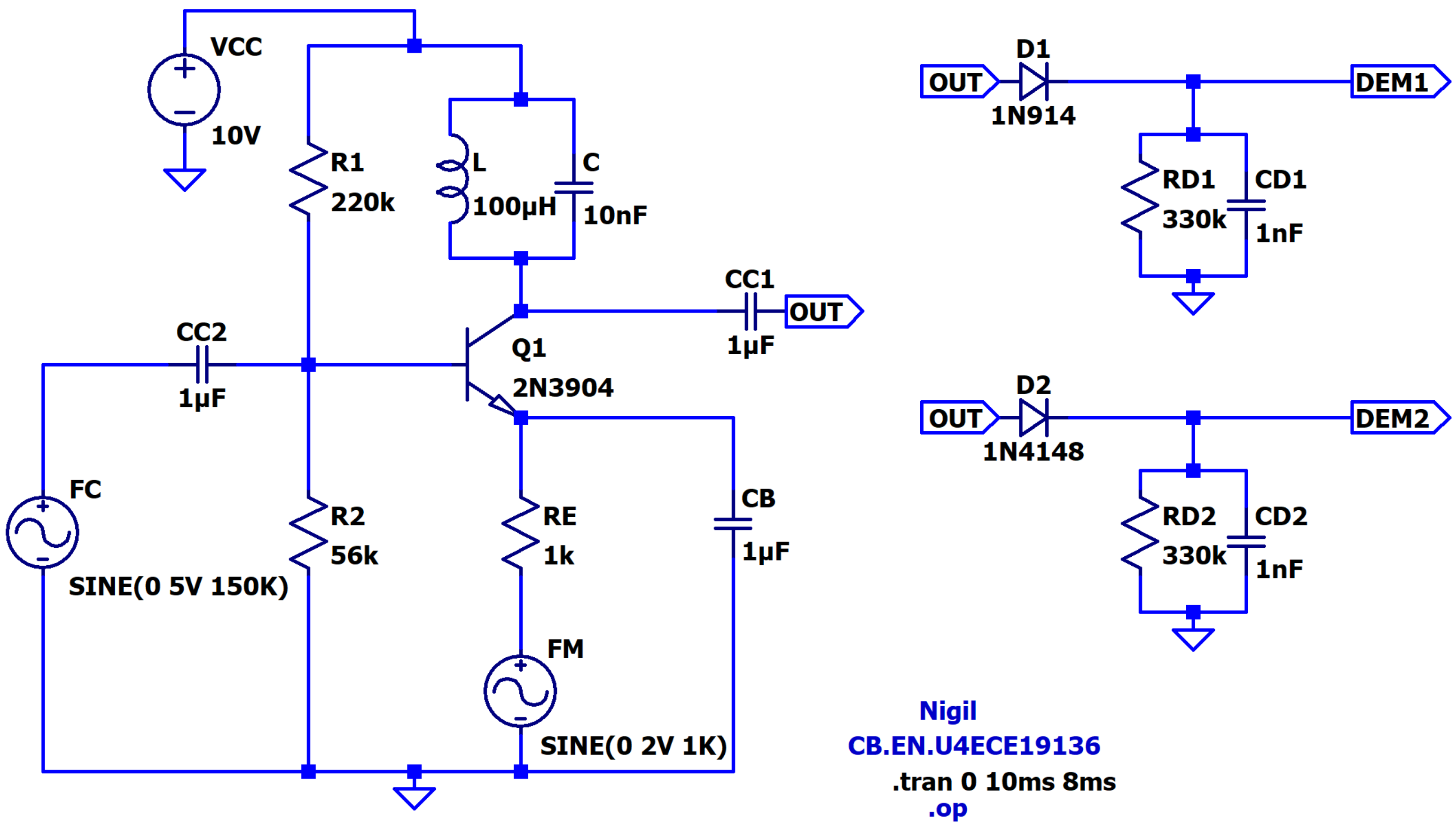

Fig 5 Circuit Diagram - AM Demodulation using Envelope Detector Circuit

Case 1 - Using Diode 1N914

Case 2 - Using Diode 1N4148

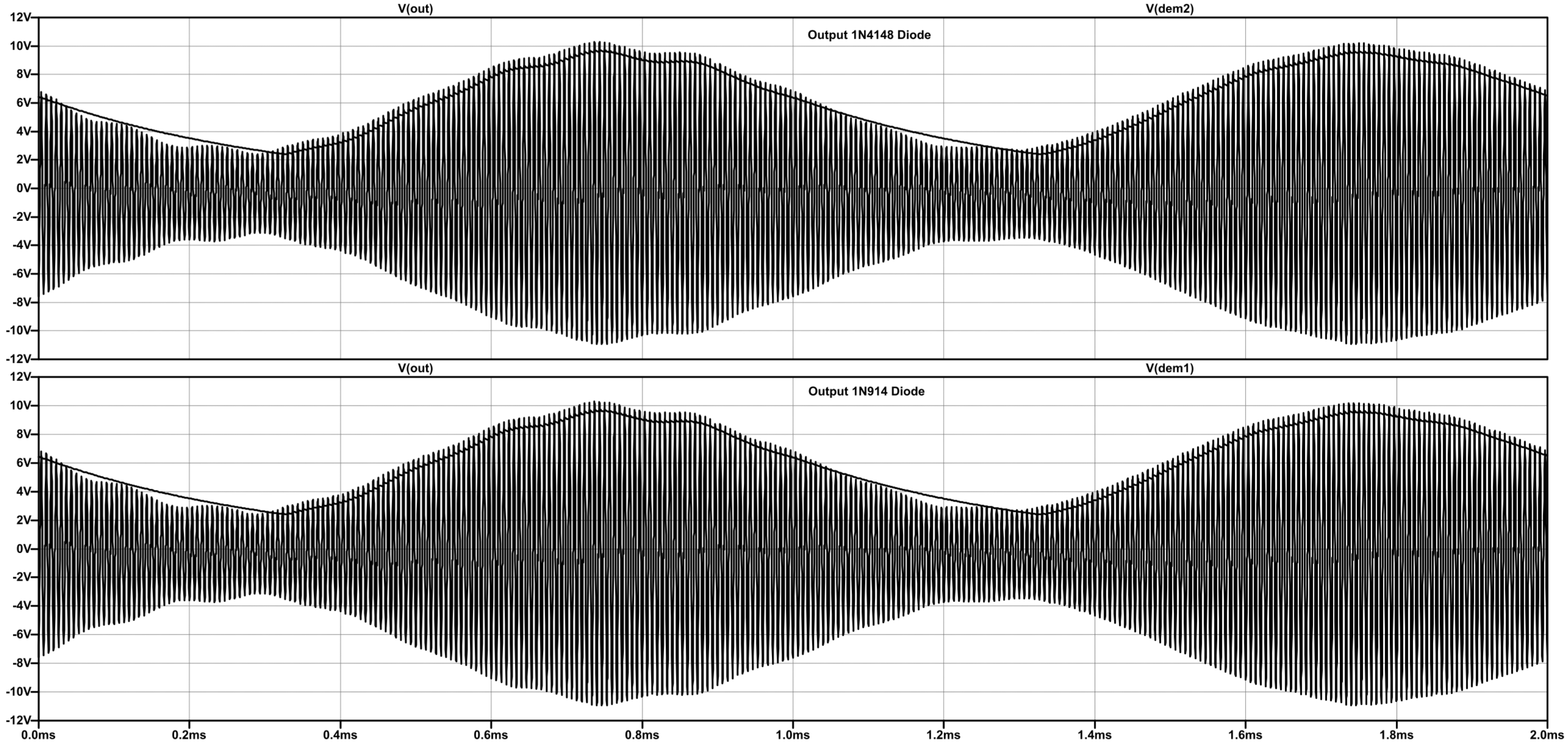

Fig 6 - Envelope Detector Demodulated Output Waveform for Case1 & Case 2

* Output should have an amplitude $A(t) = A_c + A_m$.

2. For various values of (a) modulation index.

$a < 1$ -] undermodulated, or
$a = 1$ -] no envelop distortion

$a > 1$ - overmodulated

3. The LC circuits is used to generate the negative half cycle, because for class C amplifier based on the conduction angle which is less than 180° therefore only positive outputs are reached.

For negative cycle LC (tank circuit is used) matching with carrier frequency (f_c).

$$F_c = \frac{1}{2\pi\sqrt{LC}}.$$

4. Acts as low pass filter, C' (taken output) and R' (affects / acts as load)

good envelope detector should satisfy this condition.

$$\frac{1}{F_c} << R_c << \frac{1}{W} \quad ; W \text{ (Bandwidth)}$$

Inference :-

The modulation & demodulation (envelope detector) and the modulation index were calculated from the class C amplifier implemented circuit.

Exp NO. 2

Frequency Modulation

Nigil. M. R
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Aim:-

To set up a Frequency Modulator circuit, utilizing the NE555 Timer IC.

Components Required:-

Equipments	Specification/ Range	Quantity
NE555 - Timer	-	1
Diode	.IN4148	1
Resistors	1.5kΩ, 10kΩ	2, 1
capacitors	0.1μF, 10μF	1, 1
Regulated Power Supply	0-30V	1
Digital storage oscilloscope	-	1
Function Generator.	1MHZ.	1.

Theory :-

FM is a system in which the amplitude of the modulated signal is kept constant, while frequency of the carrier is modulated by message signal m(t).

By the definition of FM, the amount by which the carrier frequency is varied from its unmodulated value, called the deviation. is proportional to the instantaneous amplitude of the modulating voltage.

The rate at which this frequency variation occurs is equal to the modulation frequency. FM is a form of angle modulation in which the instantaneous frequency fi(t) is varied linearly with message signal m(t).

$$u(t) = m(t) \cdot c(t)$$

$$u(t) = m(t) \cdot A_c \cos(2\pi F_c t + \phi_c(t))$$

$$\boxed{f_i(t) = f_c + K_F m(t).}$$

F_c is the unmodulated carrier frequency and K_F is the frequency deviation constant.

Procedure :-

1. Using the NE555 Timer, we configure it in the Astable Multivibrator mode to provide square wave output of equal ON and OFF Time.

2. The Astable configuration using a integrator circuit made of a capacitor and resistor as shown in Fig 1.

3. The output changes based on the charging and discharging of the capacitor.

4. PIN 8 and PIN1 are connected to (Vcc 5V) and Ground respectively. The PIN 4, reset is connected to the power supply because it is an active low input.

5. The Astable mode is achieved using the integrator circuit and connecting it to the Discharge (PIN) and threshold (PIN respectively).

6. Now, to make the circuit work as FM modulator we override the constant square wave output, which is considered as the carrier signal by using the control Pin (PIN5). The message signal m(t) is fed into control voltage Pin.

7. Because of the override input rather than output changing at 2Vcc/3 and Vcc/3, it changes for V and V/2 voltages of capacitor charge with respect to message signal.

8. so, here by overriding we achieve an VCO (voltage controlled oscillator). that is the time period is proportional to the input voltage V. so as V increases, the time period of the output wave increases. and V decreases the time also decreases.

Formula:

$$T_{OFF} = 0.693\ (R_1 + R_2)C$$

$$T_{ON} = 0.693\ (R_2)C$$

$$T = T_{ON} + T_{OFF}$$

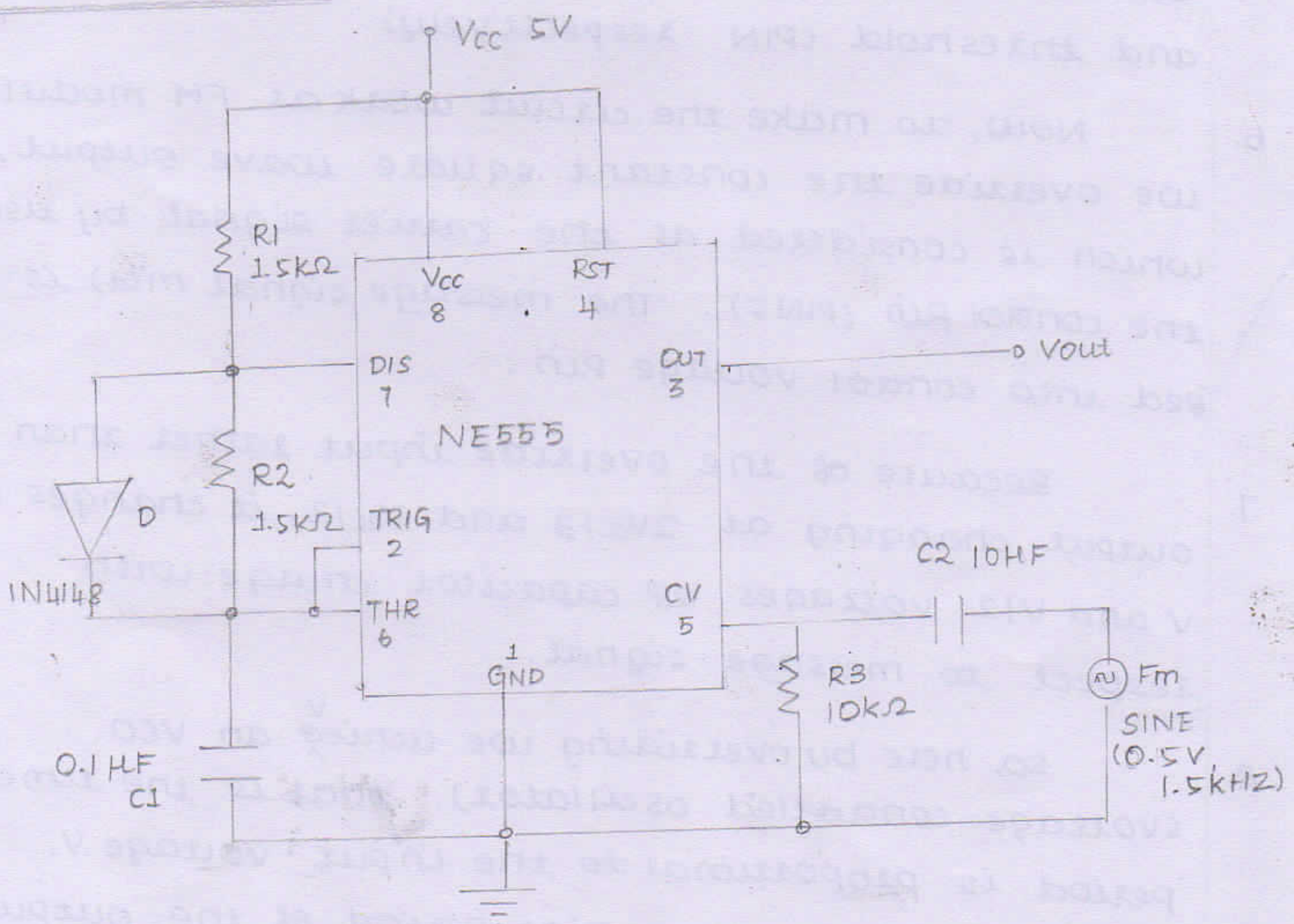
$$= 0.693(2R_1 + R_2)\ C$$

$R_1 = R_2 = R$; $C1 = C$

$$\boxed{T = 0.693\ (3R)\ C}$$

$$\boxed{F = \frac{1}{0.693\ (3RC)}}$$

Circuit Diagram:-



Results :-

(simulation attached)

Results

NE555 Timer - Astable Configuration

Unmodulated Carrier Signal Generated

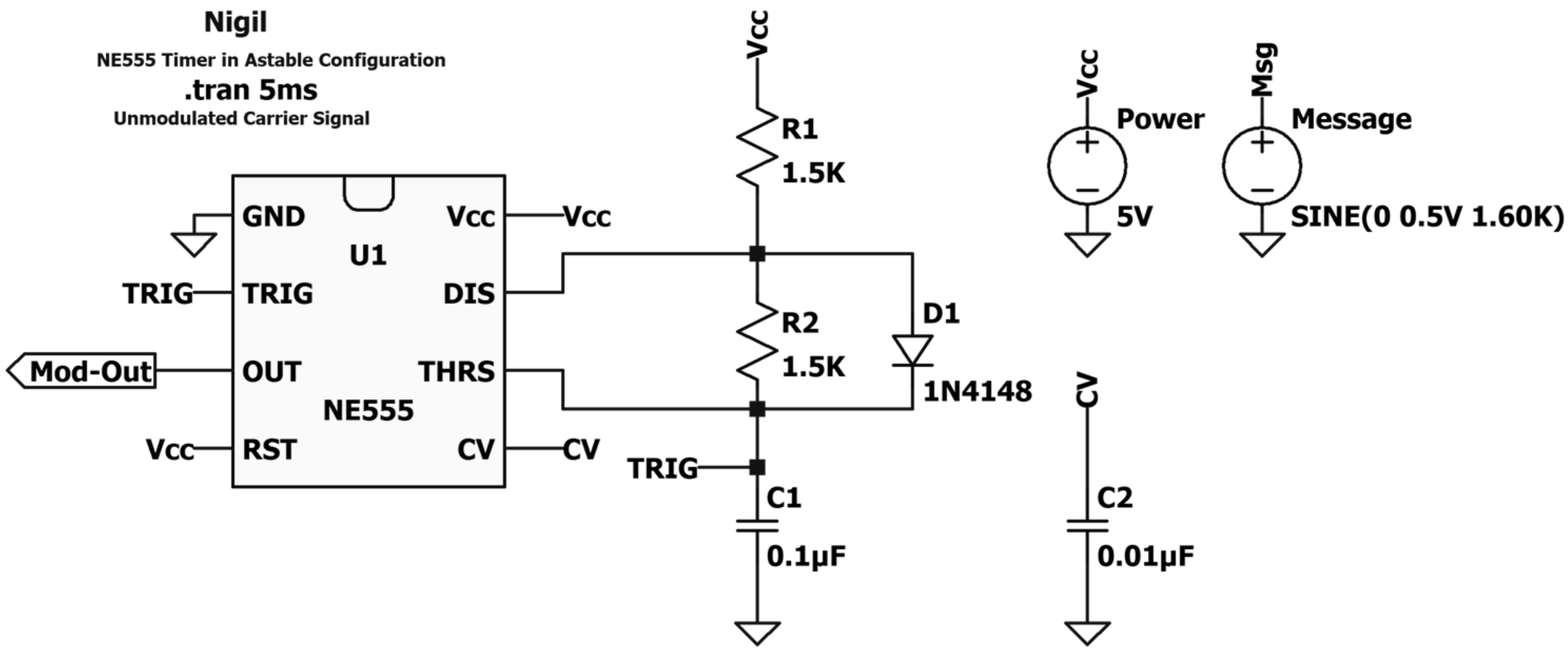


Fig 1 Circuit Diagram

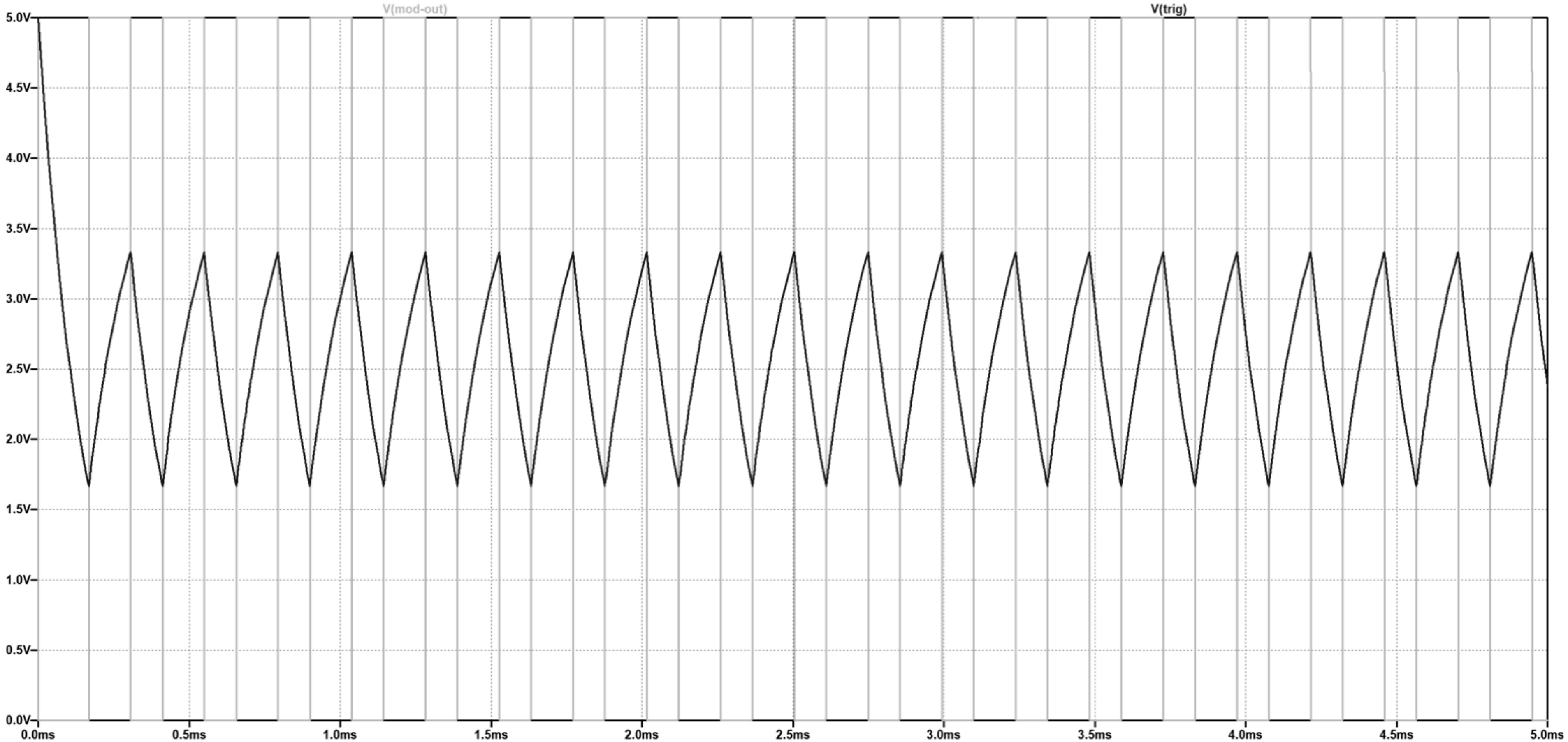


Fig 2 Astable Output Waveform

Based on the charging of the capacitor the output pulse waveform changes from positive saturation to negative saturation and vice versa. Since, the output waveform is used as carrier frequency the frequency of the pulse can be calculated using the formula given below.

$$T = T_{ON} + T_{OFF} = 0.693[R1 + R2]C1 + 0.693[R2]C1 = 0.318 \text{ ms}$$

$$F = 3000 \text{ kHz appx.}$$

NE555 Timer - Frequency Modulator

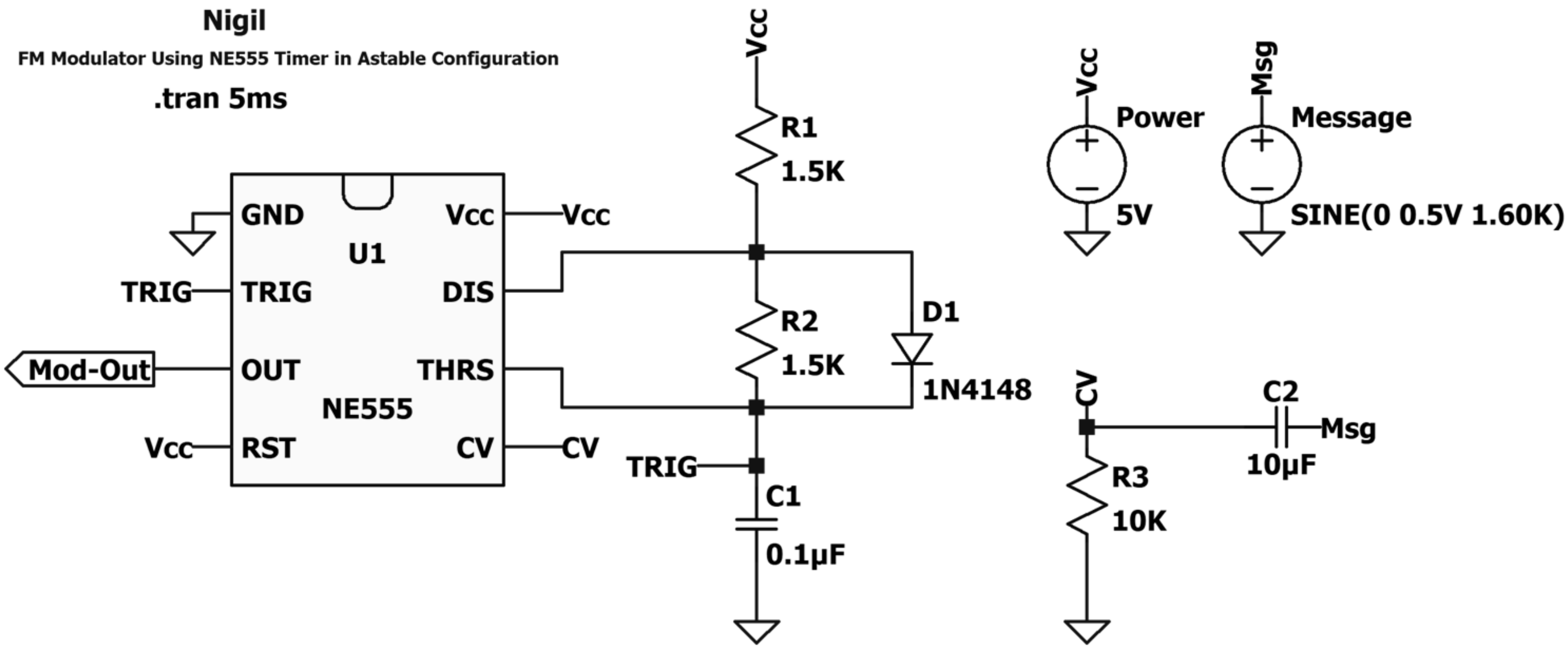


Fig 3 Circuit Diagram

The message signal given to the Control Voltage Pin (CV) alters the reference voltages of the timer to V and V/2. So, when the capacitor voltage foes below V/2, the output becomes high and the capacitor starts charging towards the power supply and when the capacitor voltage becomes greater than V, output becomes low and the capacitor starts discharging.

So, the time period is proportional to the input voltages V. So as V increases, time period of the output wave increases and when V decreases time period of the output wave decreases. Thus, achieving a Voltage Controlled Oscillator (VCO) required for FM Modulation.

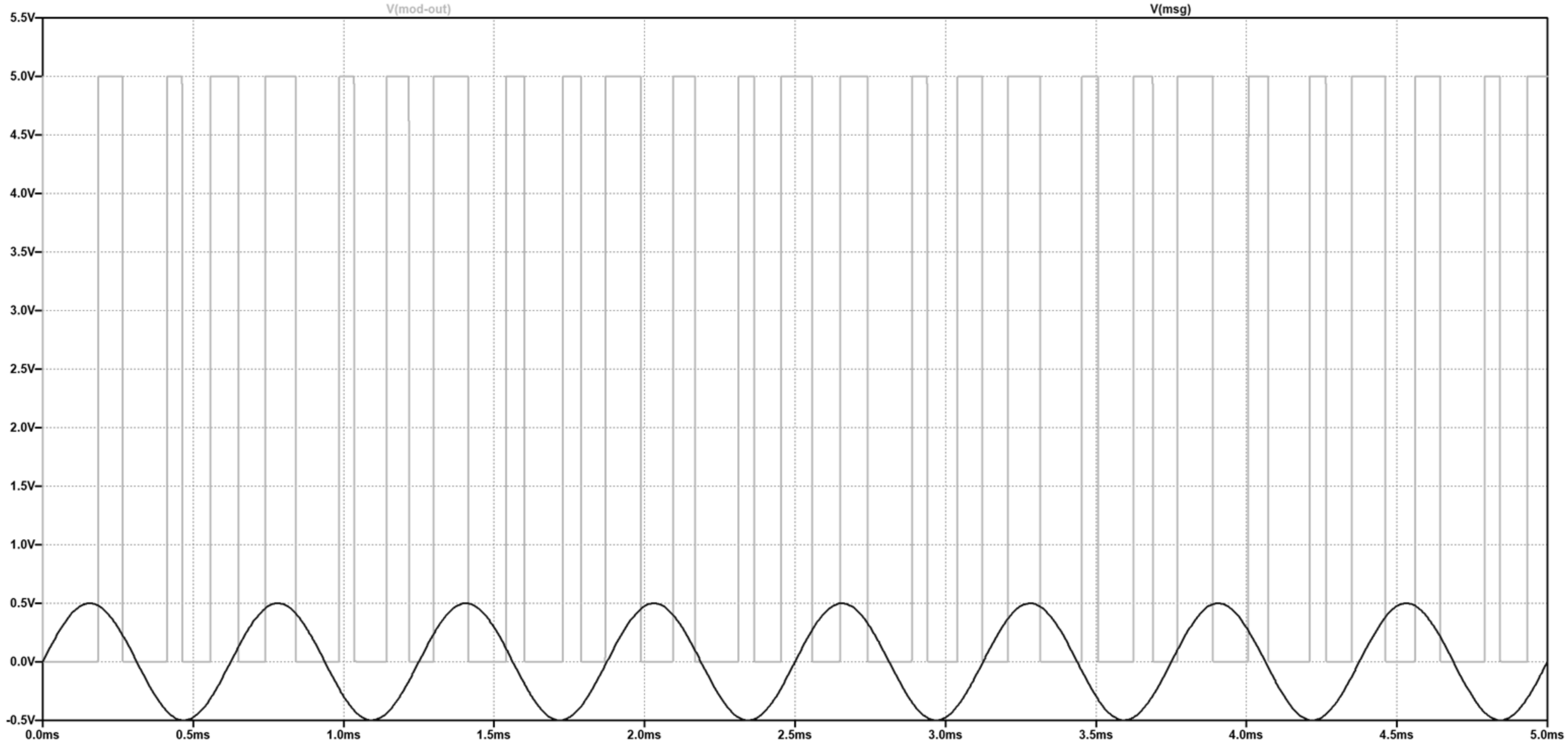


Fig 4 Frequency Modulated Output Waveform

Inference :-

The FM Modulation for a given message signal was implemented using a NE555 Timer in Astable Mode to achieve a VCO operation when m(t) was given to control voltage PIN.

The output was observed and plotted.

Exp No: 3

Time Division Multiplexing (TDM).

Nigil. M.R

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Aim:-

To design and implement Time Division Multiplexer and plot the output waveform.

Components Required:-

Equipments	Specification/ Range	Quantity
Transistors	2N3904, NPN 2N3906, PNP	1, 1
Resistors	47kΩ	2
capacitors	0.1μF	1
Function Generator	1MHz	3

Theorey :-

Time-division multiplexing (TDM) is a method of transmitting multiple data streams in a single signal by seperating the signal into many segnments, each having a very short duration. Each individual data stream is reassembled at the receiving end based on the timing.

The circuit that combines signals at the the source (transmitting) end of a communication link is known as multiplexer. It accepts the input from each individual end user, breaks each signal into segnments/samples and assigns the segnments to the composite signal in a rotating, repeating sequence. Thus the composite signal contains data from multiple senders.

At the receiver end, the individual signals are seperated out by means of a circuit called demultiplexer.

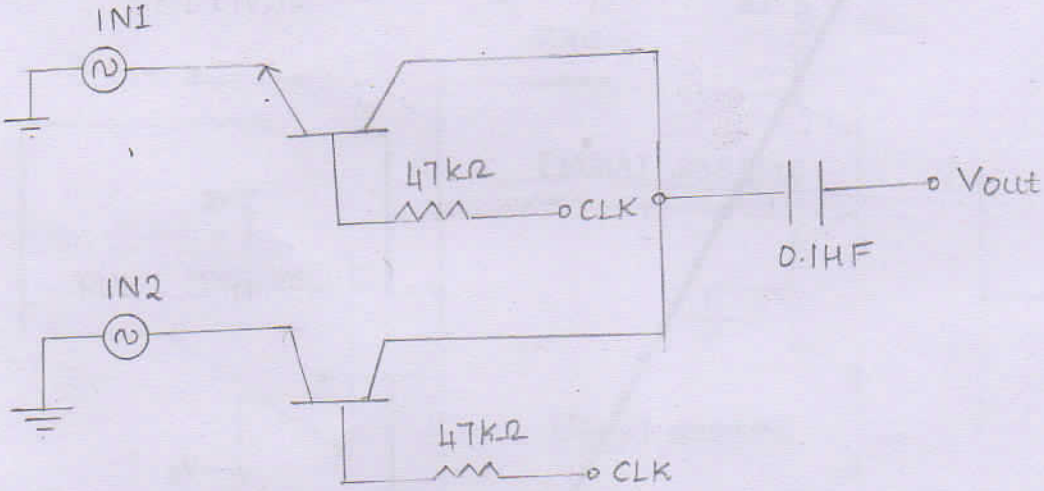
Procedure :-

1. Set up the circuit of Fig 1. with appropriate input signals and clock.
2. connect 15Vpp, 2KHz square wave signal as the clock signal
3. connect 2Vpp, 100Hz sine wave as signal 1 and same 2Vpp, 100Hz with 50% duty cycle square wave as signal 2.

4. Note that, the clock frequency should be atleast twice the maximum frequency of the input signal frequency.

5. Plot the input and output waveform.

Circuit Diagram :-



IN1	sine (2Vpp, 100Hz)
IN2	pulse (2Vpp, 100Hz)
CLK	pulse (30Vpp, 2kHz)

Fig 1.

Design Equation :-

TDM

$R_B = V_{RB} / I_B$

$V_{IN} + V_{BE} + V_{RB} = 5V$

Working :-

1. The circuit in Fig 1 consists of switches realized using BJT and capacitor.

2. The (T_1) called the sampling switch is closed (ON) for a short duration by a short pulse applied to the base of the T_1 transistor.

During this period, the capacitor is quickly charged up to a voltage equal to the instantaneous sample value of the input signal 1.

3. Similarly for the negative clock pulse the PNP transistor switches (ON) and charges till the flat top of the rectangular pulse (input 2).

Results :-

... (simulations attached) ....

Results

Time Division Multiplexer (TDM)

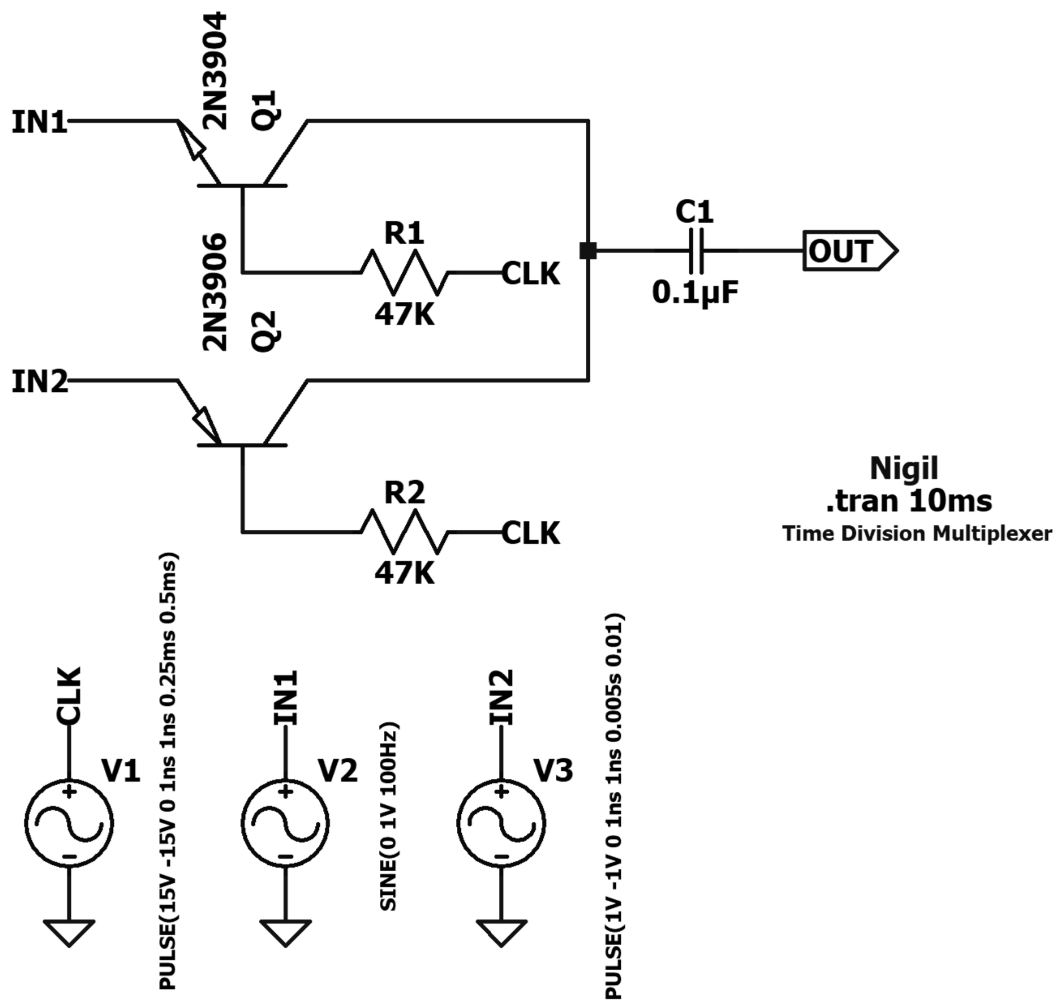


Fig 1 Circuit Diagram

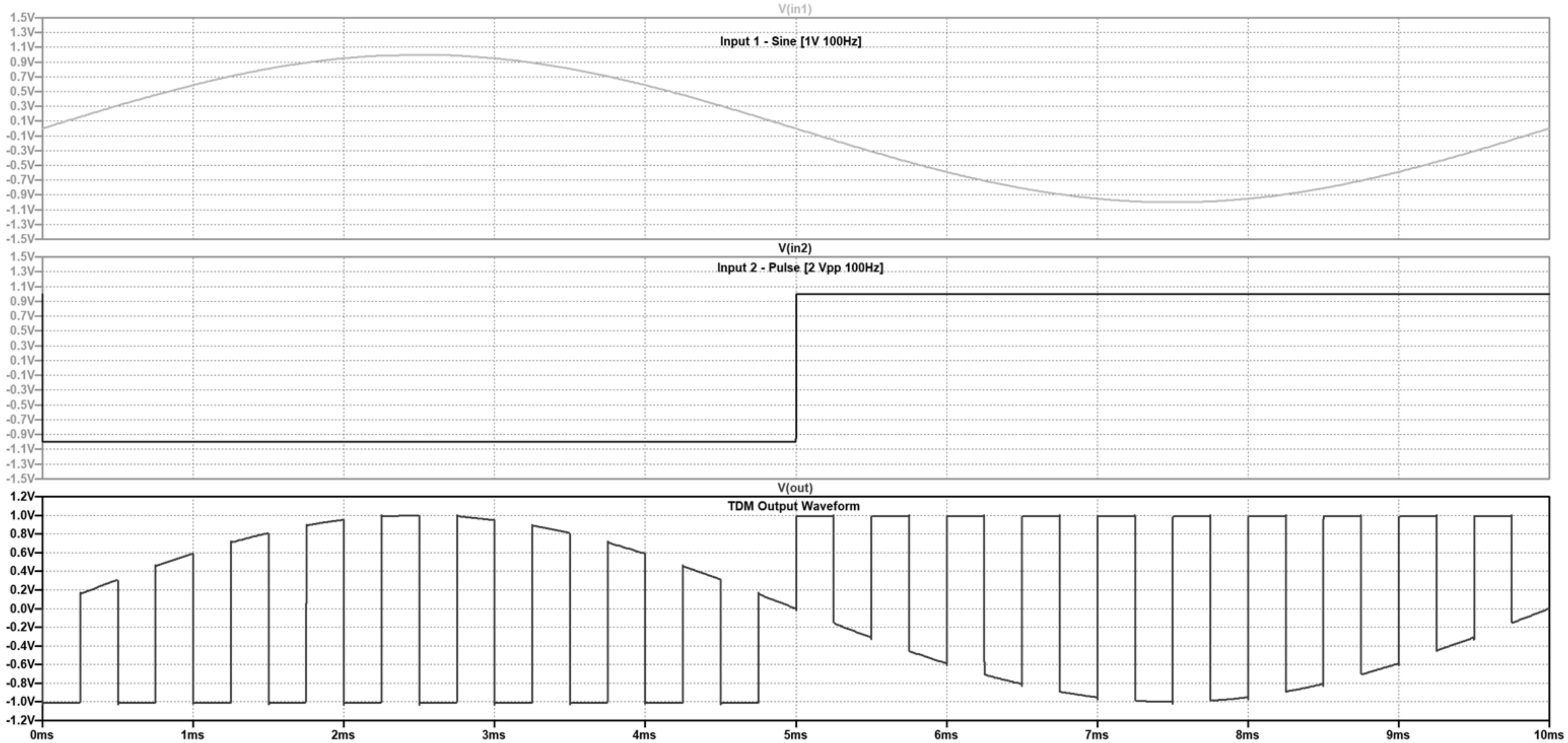


Fig 2A Output Waveform

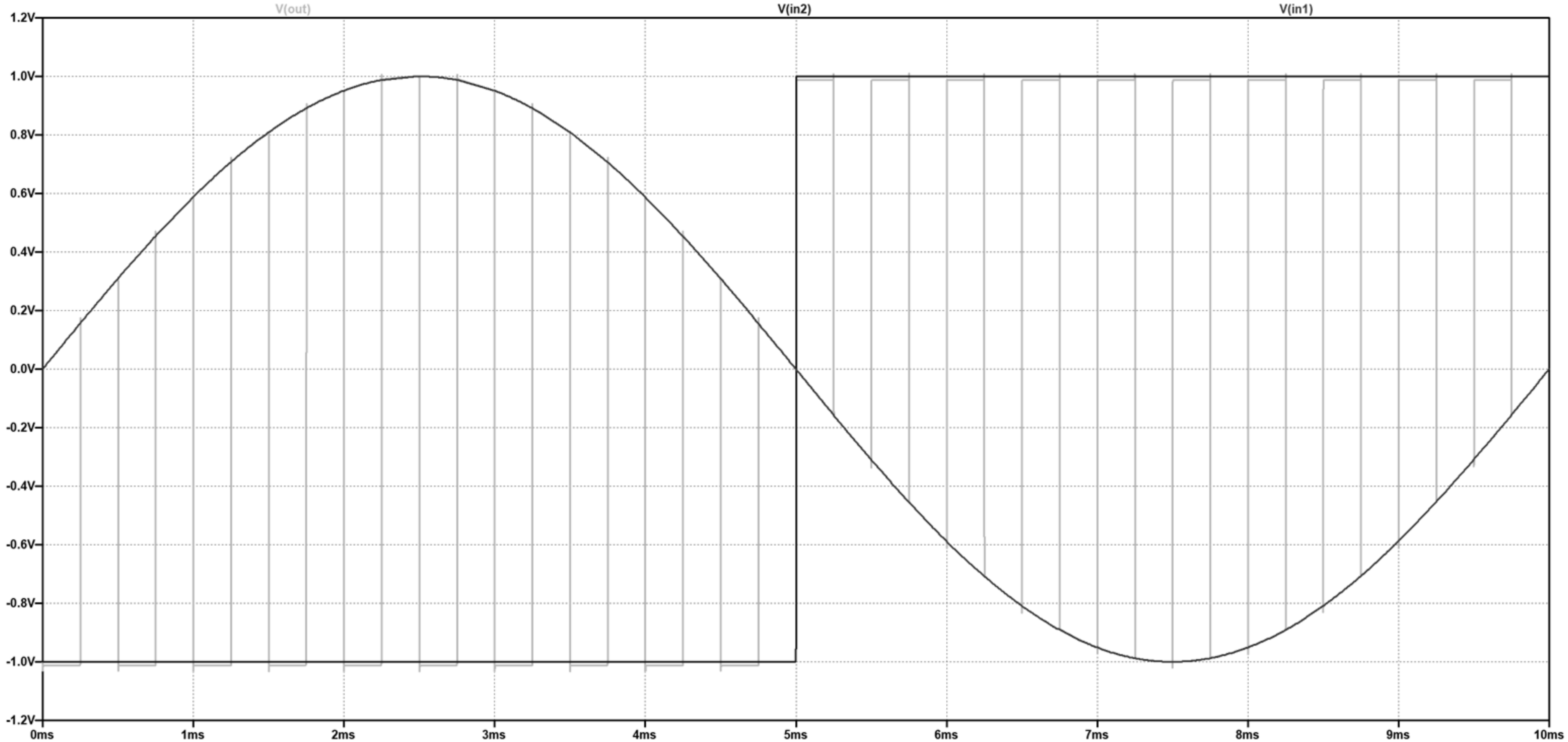


Fig 2B Output Waveform

Perfectly Time Multiplexed output with respect to the input signal 1 and input 2 is shown in Fig 2A and 2B.

Fig 2B combines both inputs and output waveform in a single plot.

Inference :-

1. For different type of inputs, multiplexed output with respect to clock are observed and analysed.

Exp No. 4 24-01-2022

Pulse Amplitude Modulation and Demodulation

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Aim:-

To design and implement pulse Amplitude Modulator (PAM) and demodulator.

Theory:-

Modulation of PAM:-

Pulse amplitude modulation is a technique in which the amplitude of each pulse is controlled by the instantaneous amplitude of the modulation signal. It is a modulation system in which the signal is sampled at regular intervals and each sample is made appropriately proportional to the amplitude of the signal at the instant of samping. This technique transmits the data by encoding in the amplitude of a series of signal pulses.

Demodulation of PAM:-

For the demodulation the PAM signal, the PAM signal is fed to the low pass filter. The LPF eliminates the high frequency ripples and generates the demodulated signal. This signal is then applied to the inverting amplifier to amplify its signal level to have the demodulated output with almost equal amplitude with the modulating signal.

Components Required :-

Equipment	Specification	Quantity
BC547 / Transistor	-	1
Resistors	47kΩ, 4.7kΩ, 470kΩ	2, 1, 1
Regulated power supply	0 - 30V	1
capacitor	0.1μF	1
DSO	-	1

Circuit Diagram :-

Modulator :-

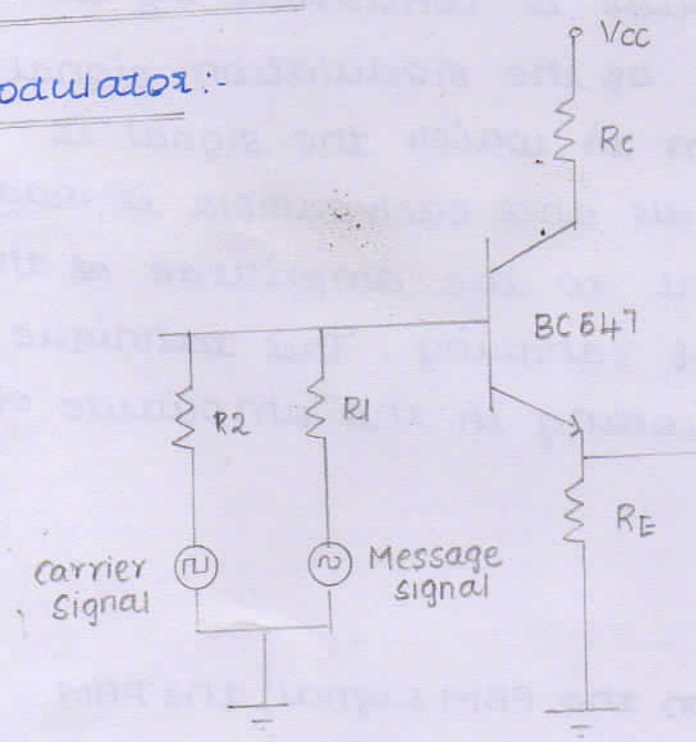
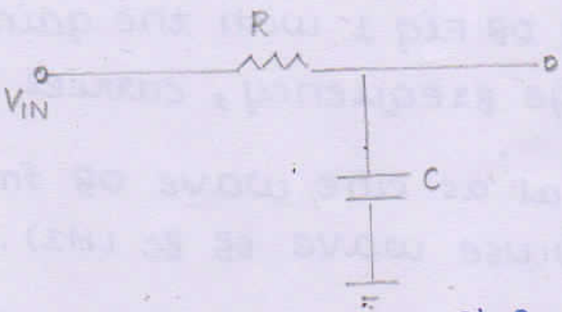


Fig 1.

Demodulators:-

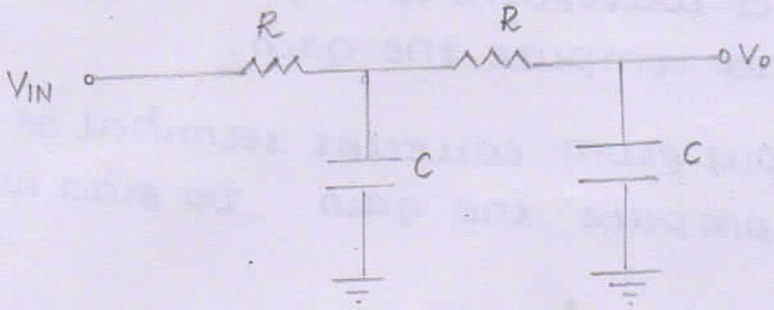


$F_m = \dfrac{1}{2\pi RC}$

$R = 150k\Omega$

$C = 10nF$

Fig 2.



Filter order (N) = 2

Fig 3.

circuit Design:-

$B = 300$ (For BC547)

$V_{CC} = 15V$

gain = 10

$R_B = 20k\Omega$ (assummed)

$R1 \| R2 = R_B = 47k\Omega$ (standard value)

$$A_V = \frac{-g_m(R_C)}{1+g_m R_E} = \frac{R_C}{R_E} = 10 \text{ (appx.)}$$

Bias at Middle (Q).

$\dfrac{V_{CC}}{2} = V_{CE} = 7.5V$

$V_{CE} = V_{CC} - I_C(R_C)$

$R_C = 5k\Omega$ (assummed)

$I_C = 1.5mA$

$I_B = \dfrac{I_C}{B} = 5\mu A$

Design values

$R_C = 4.7k\Omega$ (standard E32 series)

$R_E = 470\Omega$

$R1 = R2 = 47k\Omega$

$V_{CC} = 15V$.

* (O/P) taken at emitter circuit changes to common collector (CC)/ Emitter Follower.

Procedure :-

1. Set up the circuit of Fig 1 with the gain (Av 10 with appropriate message frequency, carrier frequency).

2. Set Message signal as sine wave of fm (Hz) and carrier signal as pulse wave of fc (Hz).

3. Plot the output waveform of Fig 1 and mark all salient points and compute the gain.

4. Now, take output from collector terminal of the transistor and compute the gain. Do find any difference, why.

5. Now, change the carrier signal to square wave. Do you find any difference, why ?

6. Set carrier signal back to sine wave and change message signal to square wave, ramp signal and pulse signal. Write your observation.

7. Set up the circuit of Fig 2. using appropriate R,C values.

8. Plot the output waveform of Fig 2 and mark all salient points.

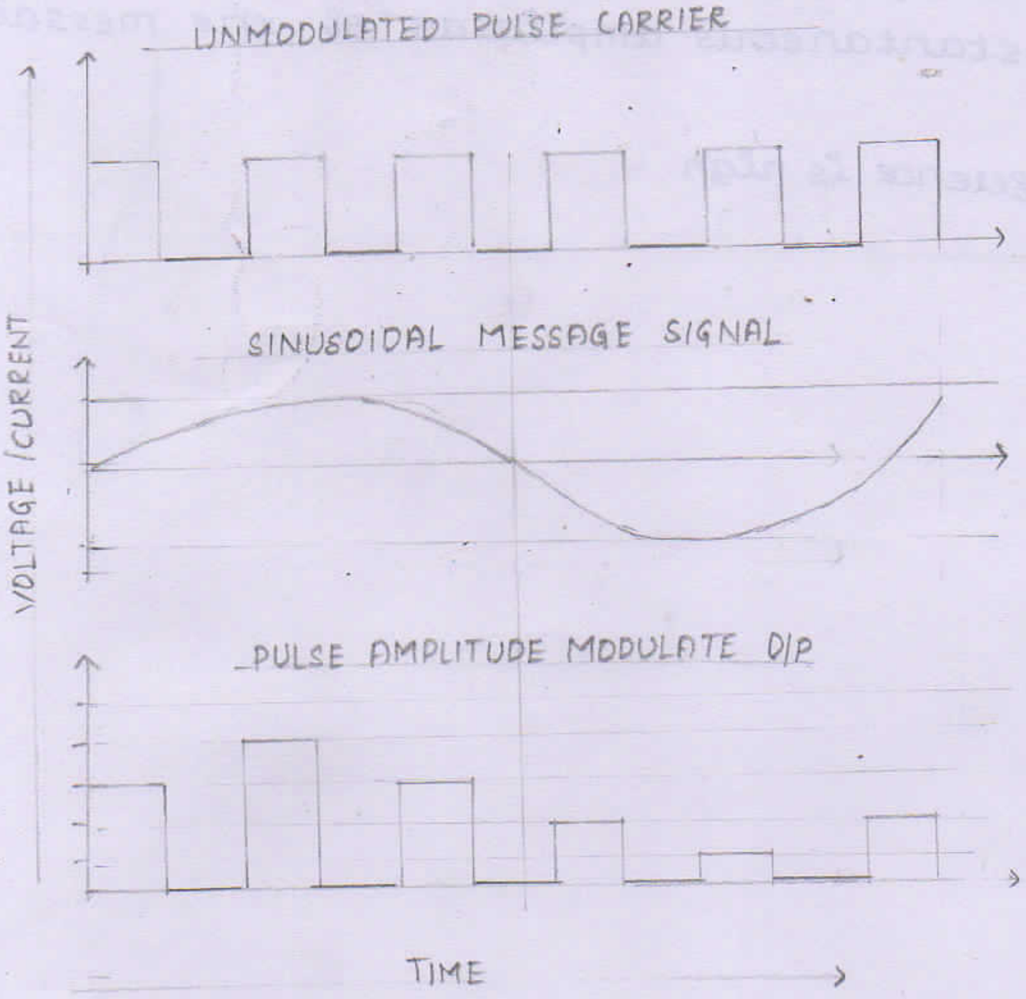
9. Calculate frequency and amplitude of the first order filter from the output plot of DSO.

10. Now, set up another first order filter with same R and C values and cascade it as shown in Fig 3.

11. Calculate frequency and amplitude of the second order filter. from the output and DSO plot.

12. Increase the carrier frequency fc and find the value of fc such that modulated waves get distorted.

Model Graph :-



Result :-

(simulations and answers attached).

Results

PULSE AMPLITUDE MODULATION (PAM) - COMMON COLLECTOR / EMITTER FOLLOWER

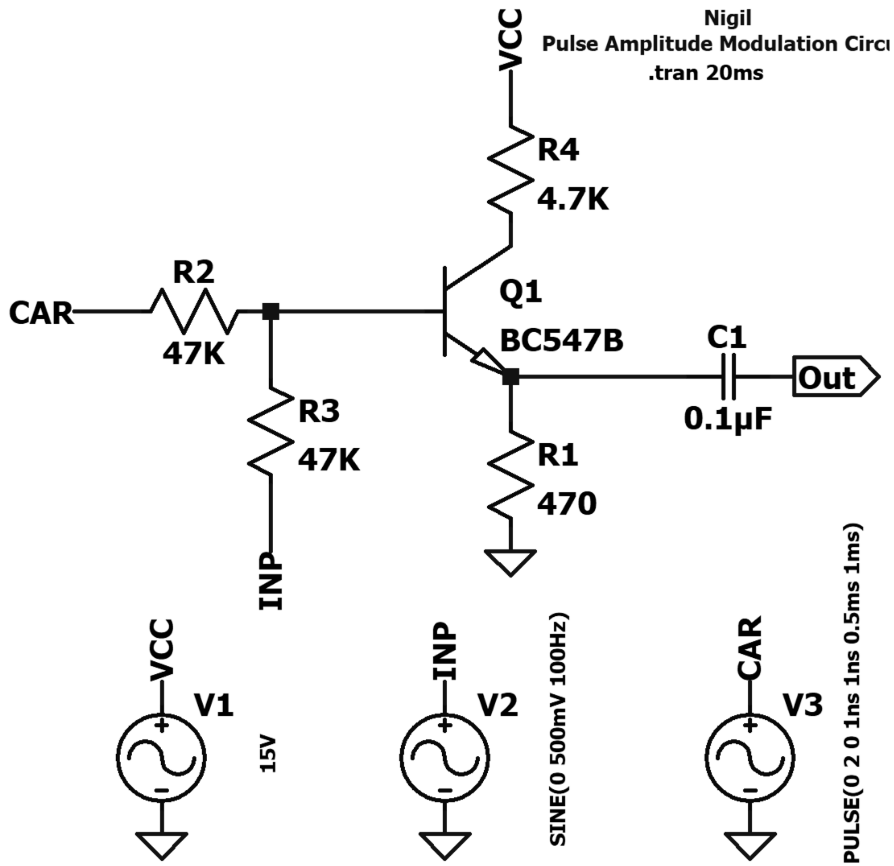


Fig 1 Circuit Diagram

Circuit Construction

1. For design purpose the R_B which R1 || R2 is assumed 20 kOhms. So, 47 kOhms was assumed as R1 and R2 values.
2. Ratio R_C and R_E should be 10 V/V.
3. For biasing the circuit in the middle of the active region V_{CE} should half of the given power supply that is 7.5 V and collector current I_C is calculated by assuming R_C as 4.7 kOhms (Standard Value).
4. From the BC547 datasheet, the DC current gain was found as 300,
5. The final circuit constructed works as Single Polarity PAM
6. Also, when output is taken across 'emitter' the circuit switches to common collector mode and becomes a unity gain follower.
7. PAM or Binary ASK works similar to a convolution circuit.

Procedure Step 2 - Message Signal - Sine Wave (1Vpp) & Carrier Signal Pulse (2Vpp)

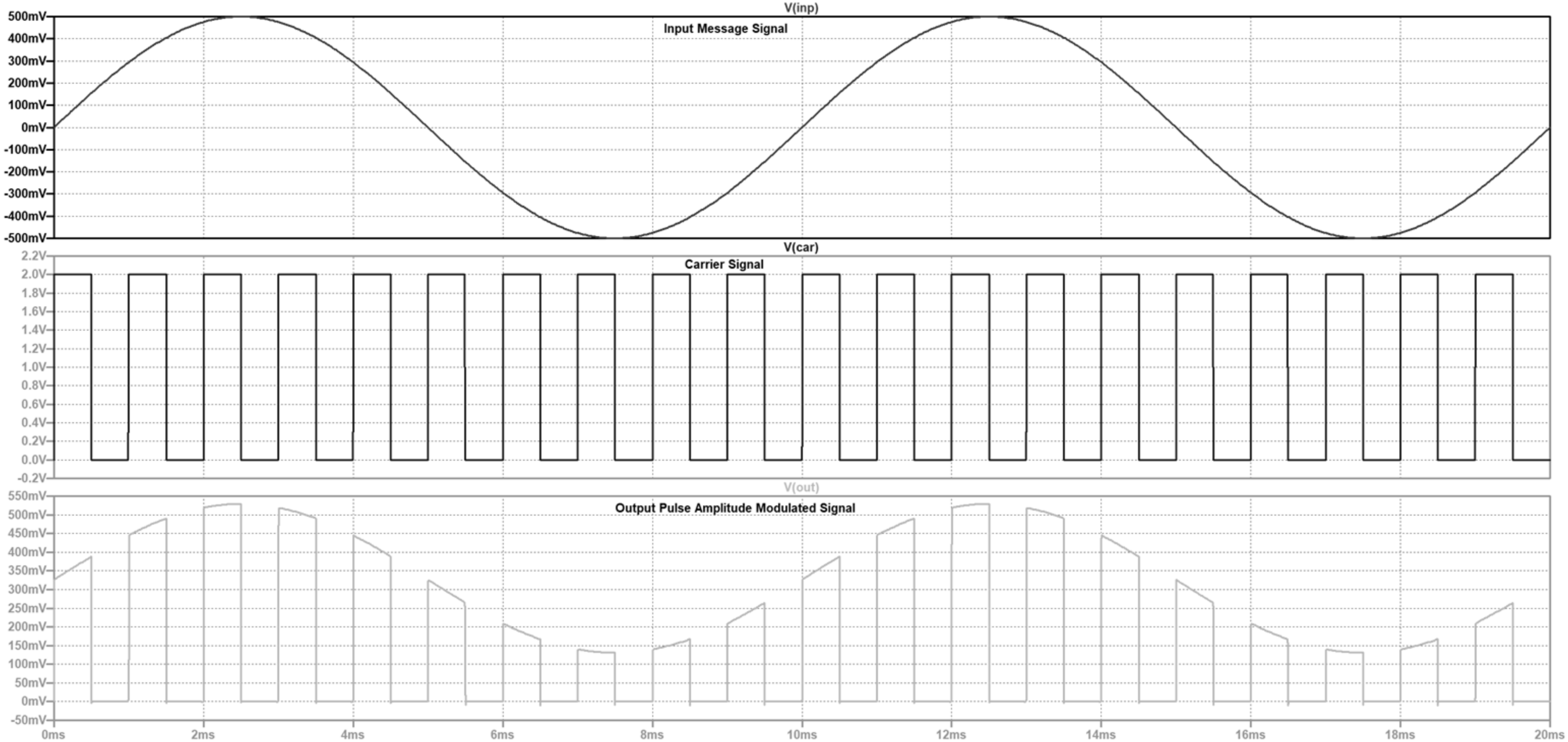


Fig 2 Pulse Amplitude Modulated - Output Waveform

<u>Procedure Step 4</u> - Now, take the output waveform from the collector terminal of the transistor and compute the gain. Do you find any difference, why?

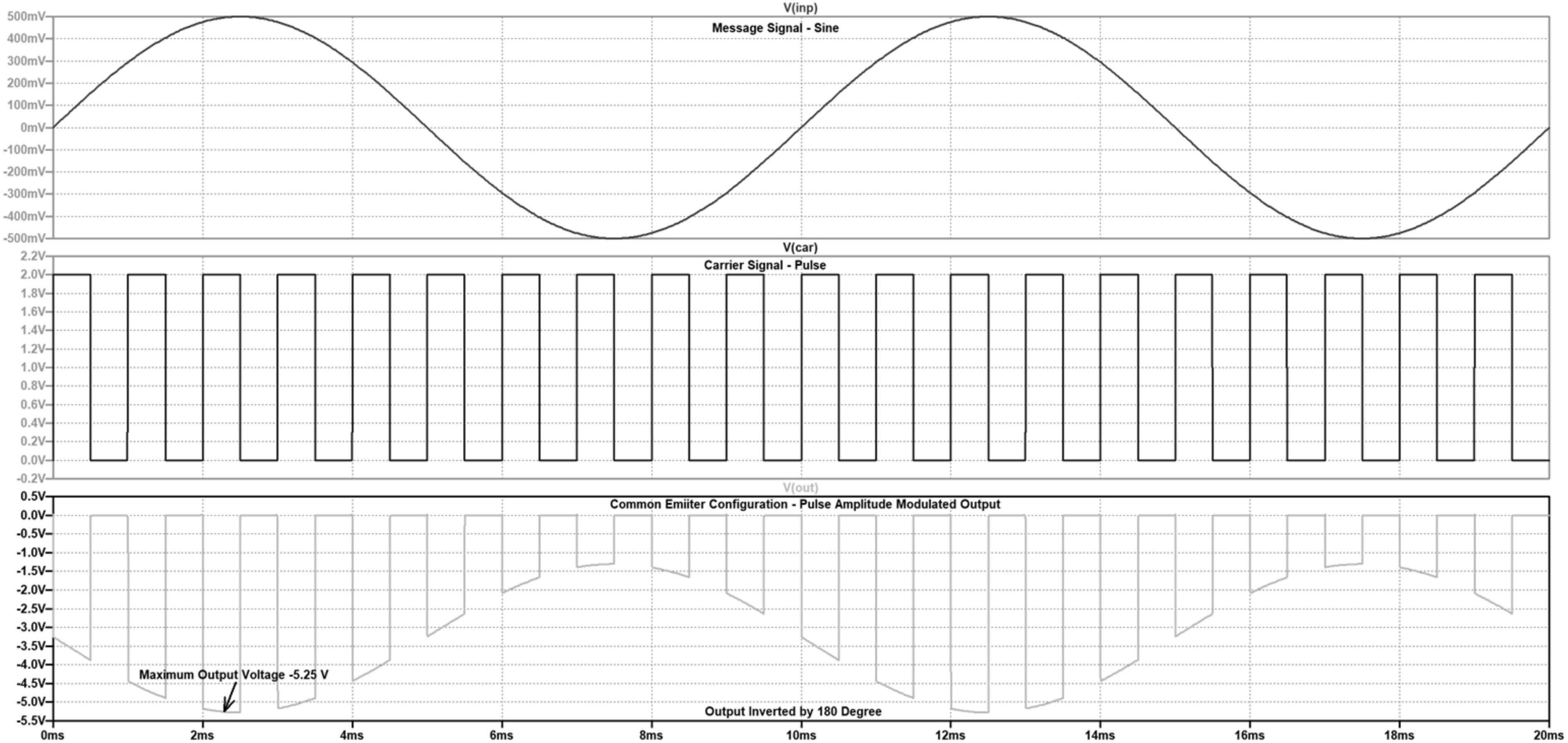


Fig 3 Common Emitter Configuration - Output Waveform Across the Collector

Observation *- The output when taken across the collector the output wave form is inverted by 180^o because the gain formula for a common emitter amplifier is $A_v = -R_C/R_E$. The negative sign indicated the inversion. The gain of the circuit can be found theoretical from the formula $A_v = -R_C/R_E$, which is approximately 10V/V. From the output waveform from Fig 3, for the sinusoid wave of 1Vpp, during the conduction phase of the transistor only positive half gets amplifier so the out is approximately -5.2 V and the Gain is as calculated which is 10 V/V.*

<u>Procedure Step 5</u> - Now change the carrier signal to sine wave, do you find any difference, why?

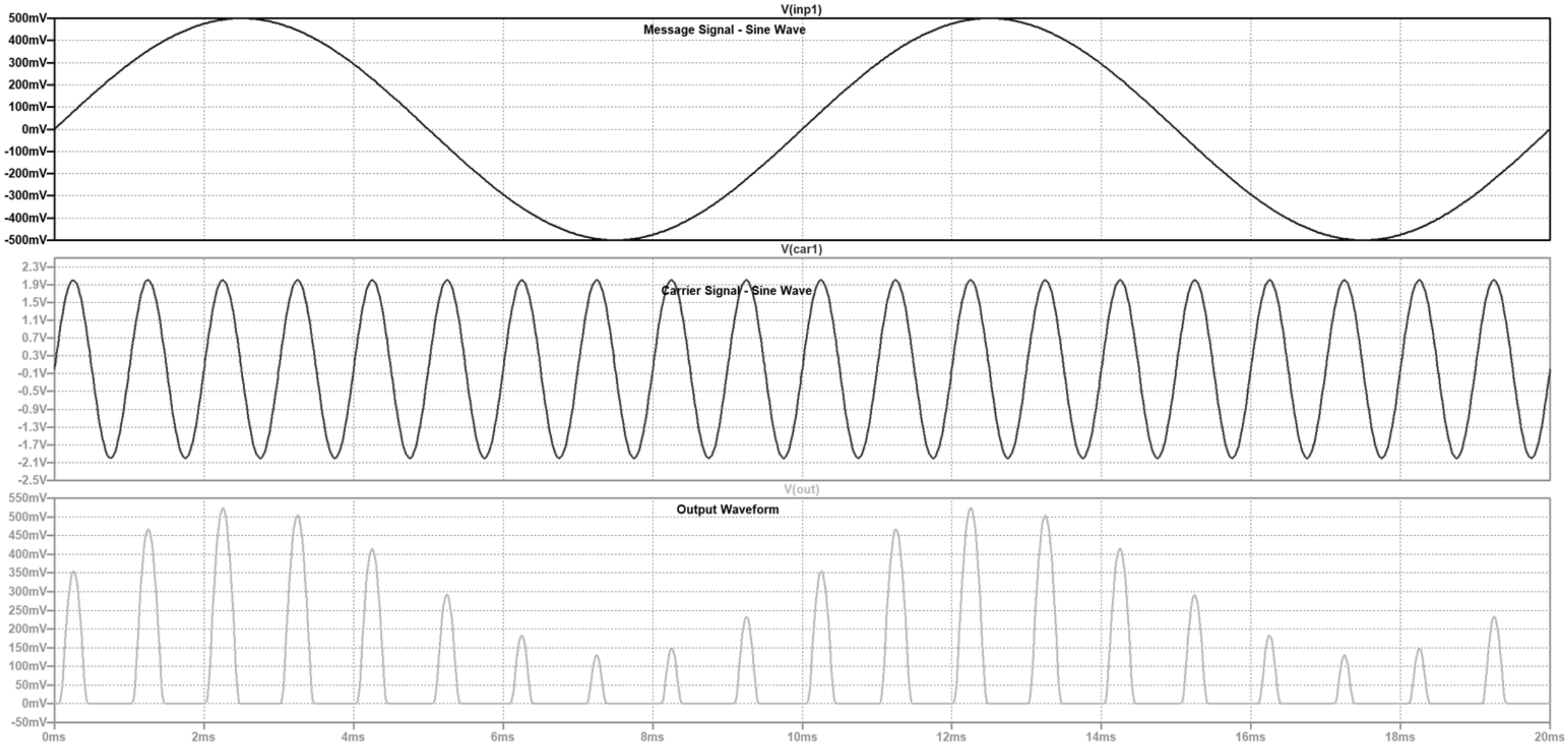


Fig 4 - Output Waveform for Sine Wave Carrier Signal

Observation *- Since, the working the circuit is still similar to the carrier pulse but here, the amount of overlap (convolution) occurring due to the sampling of the circuit between the message signal and the carrier signal is comparatively lesser. This explains the larger gaps between each peak.*

Procedure Step 6 - Fix the carrier signal to the square wave and change the message signal to square wave and ramp signal. Write your observations and similarly repeat for sine as carrier signal.

(Only Output Waveforms Attached Circuit Connection Refer Fig 1)

Case 1 - Message Signal - Square & Carrier Signal - Square

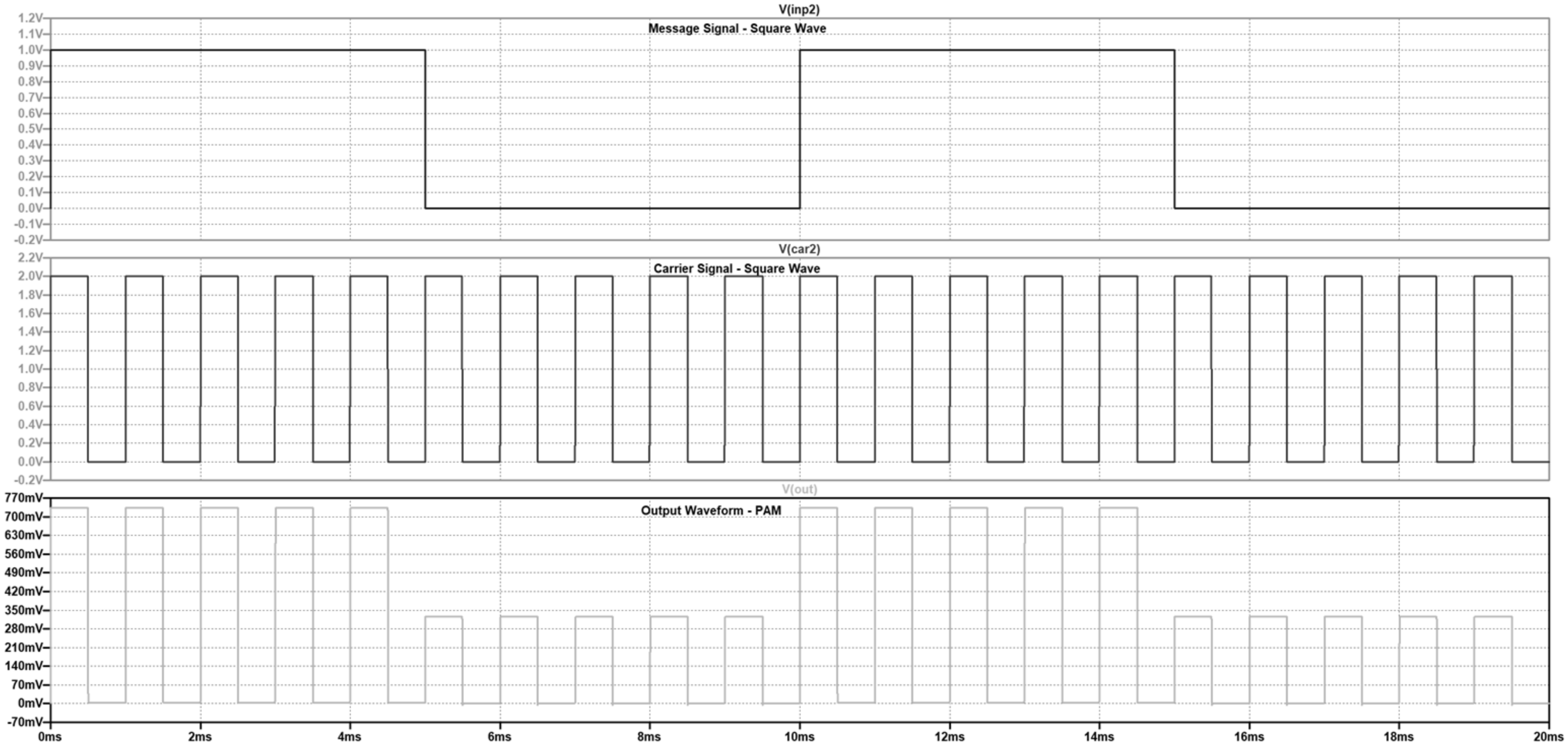


Fig 5 - PAM Output Waveform for Message Signal - Square & Carrier Signal - Square

Case 2 - Message Signal - Ramp & Carrier Signal - Square

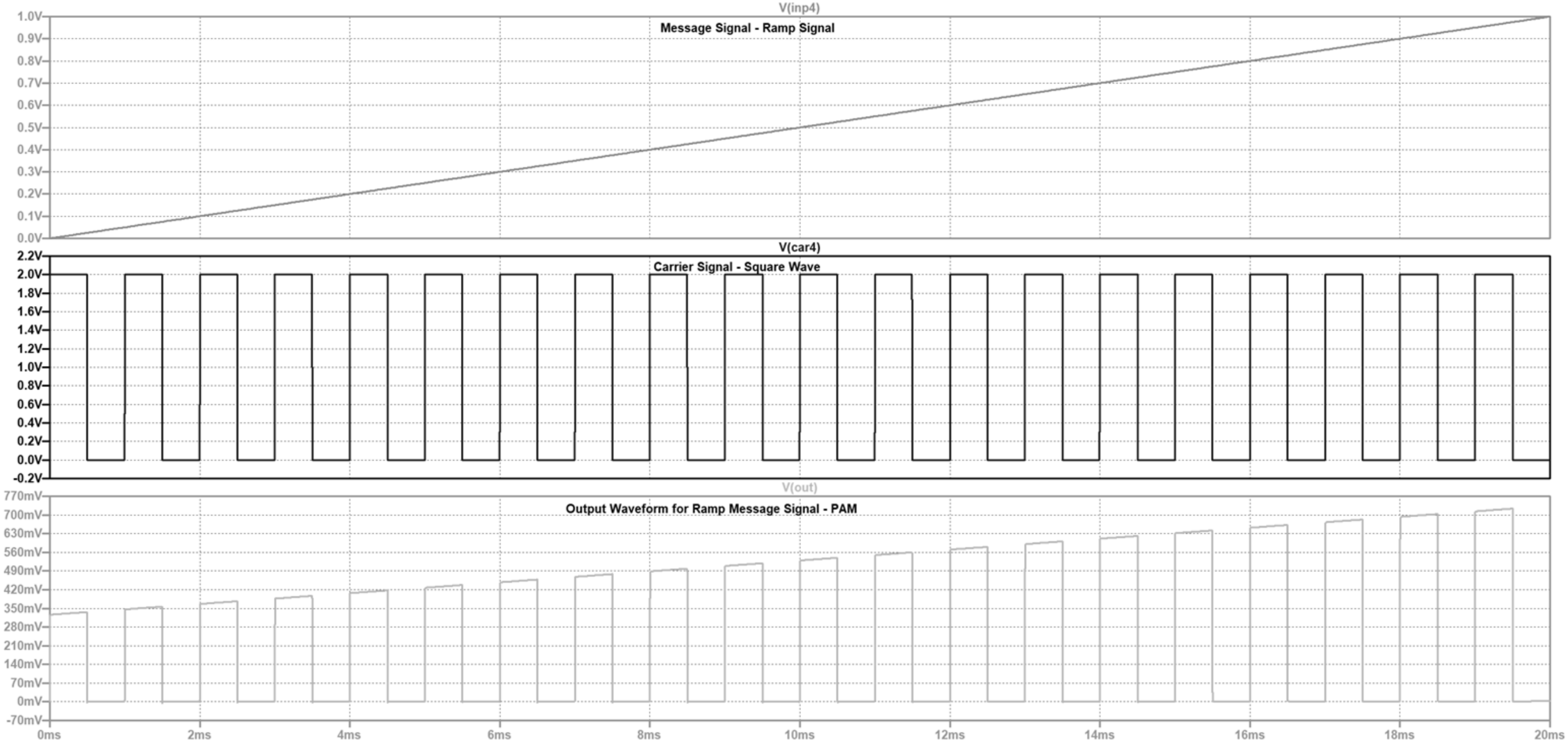


Fig 6 - PAM Output Waveform for Message Signal - Ramp & Carrier Signal - Square

Case 3 - Message Signal - Square Wave & Carrier Signal - Sine Wave

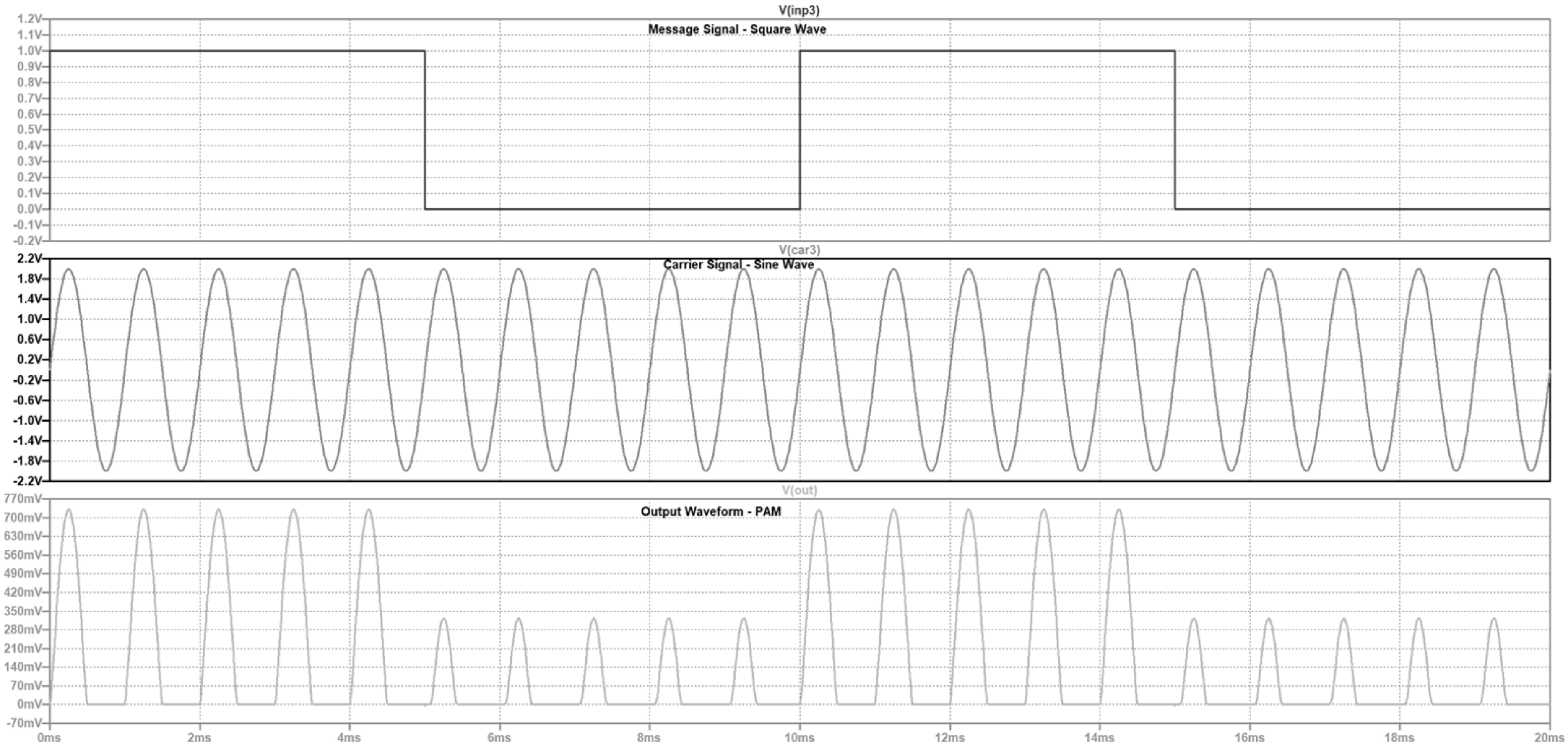


Fig 7 - PAM Output Waveform for Message Signal - Square Wave & Carrier Signal - Sine Wave

Case 4 - Message Signal - Ramp & Carrier Signal - Sine Wave

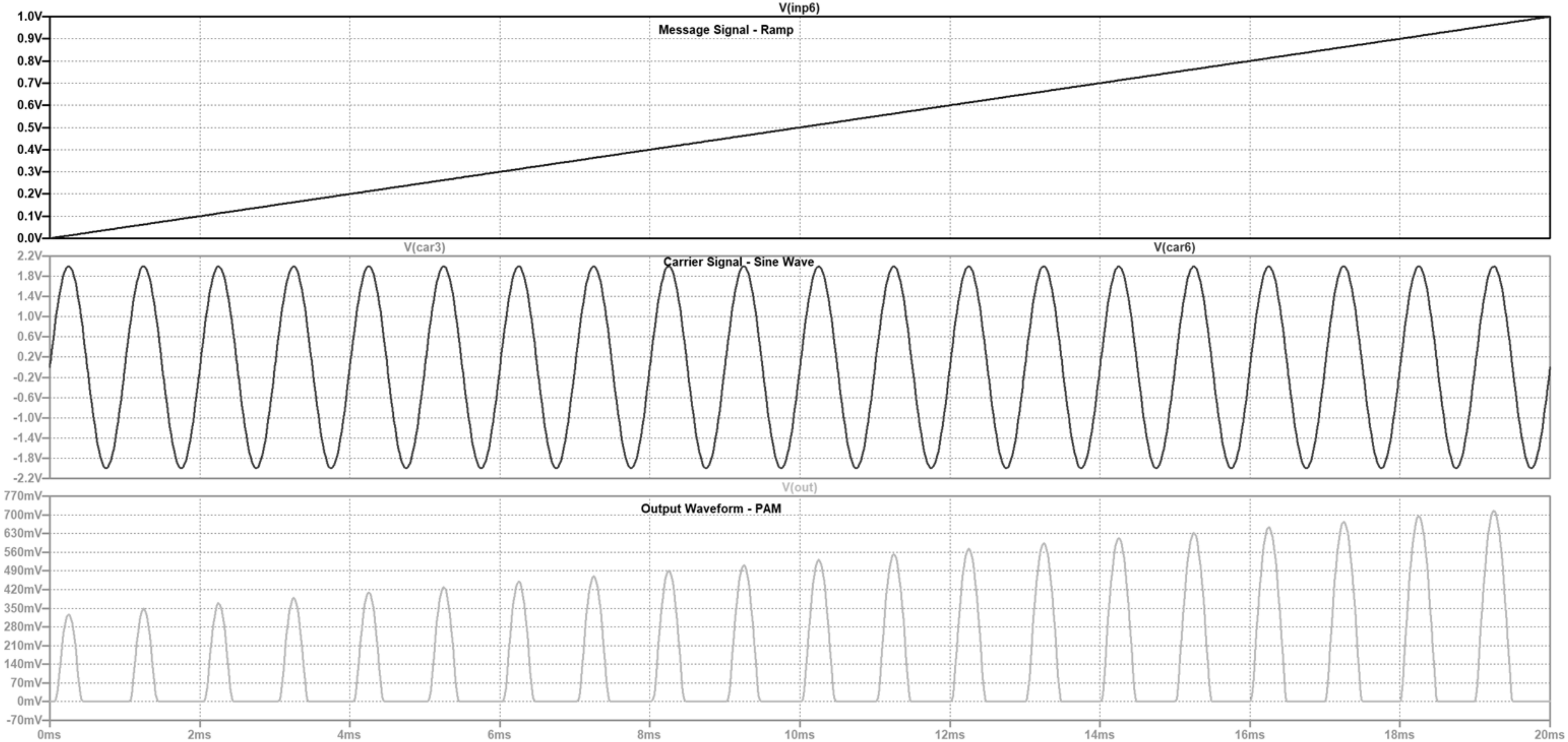


Fig 8 - PAM Output Waveform for Message Signal - Ramp & Carrier Signal - Sine Wave

Observation *- From the Figures 5 to 8 we can conclude the carrier signal controls the switching on and off of the circuit. This circuit for Pulse Amplitude Modulation is otherwise called as Sampling/Holding Circuit. And based on the switching on and off, the message signal follows the amplitude of the carrier signal (message signal modulated the carrier signal).*

PULSE AMPLITUDE DE-MODULATION - LOW PASS FILTERS - FIRST ORDER

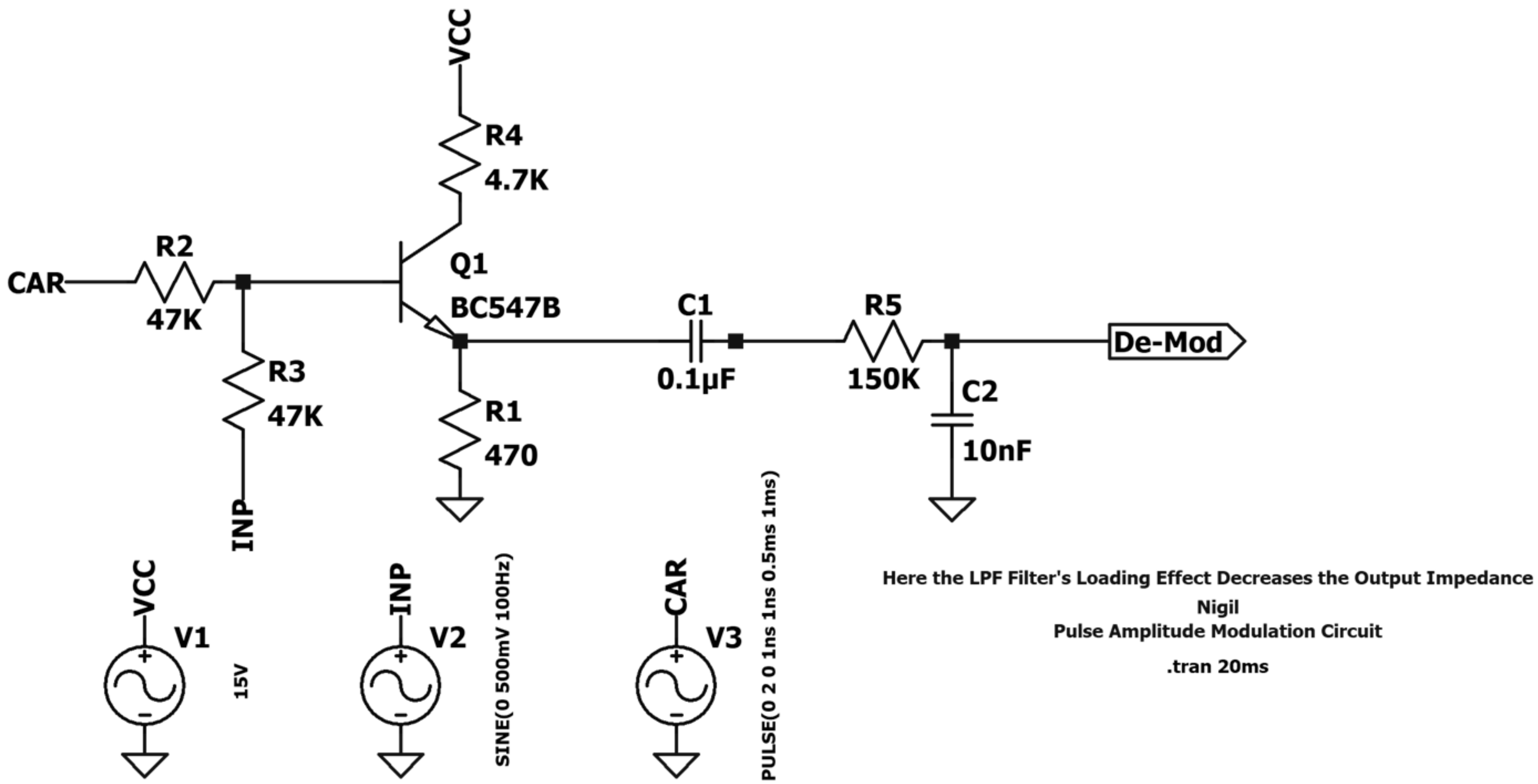


Fig 9 Demodulation Circuit with LPF First Order

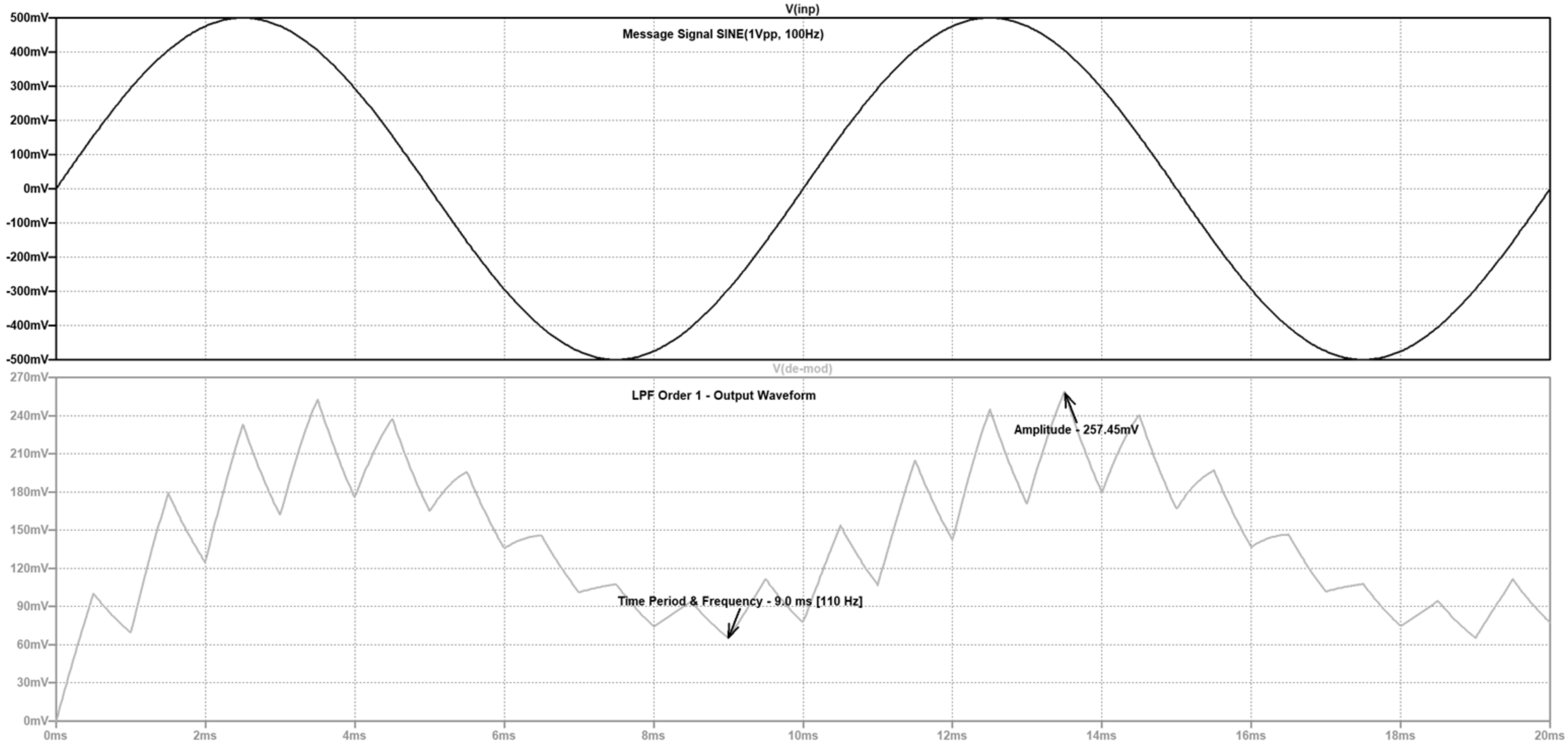


Fig 10 Low Pass Filter **First** Order - Demodulated Output Waveform

PULSE AMPLITUDE DE-MODULATION - LOW PASS FILTERS - SECOND ORDER

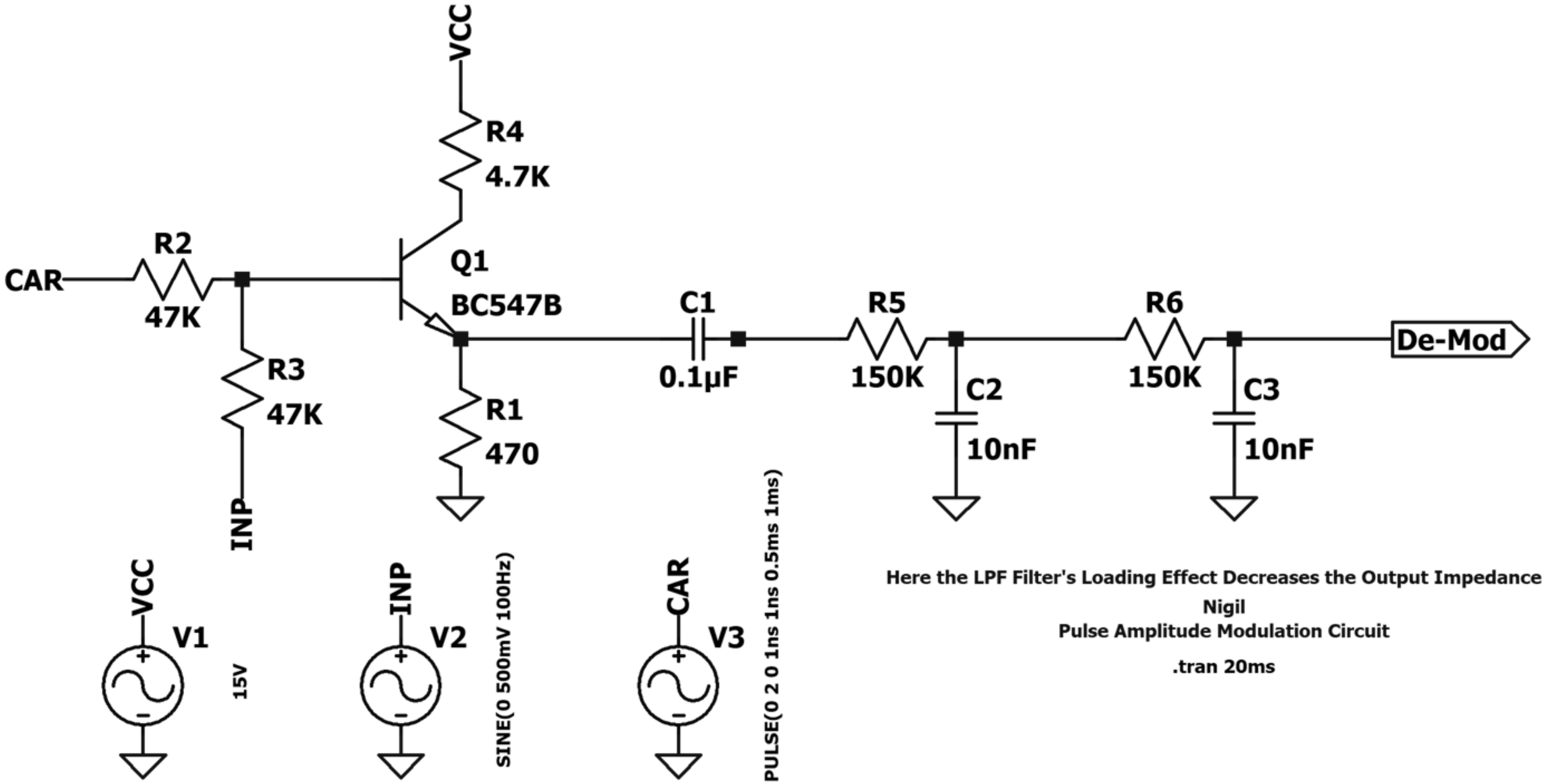


Fig 11 Demodulation Circuit with LPF Second Order

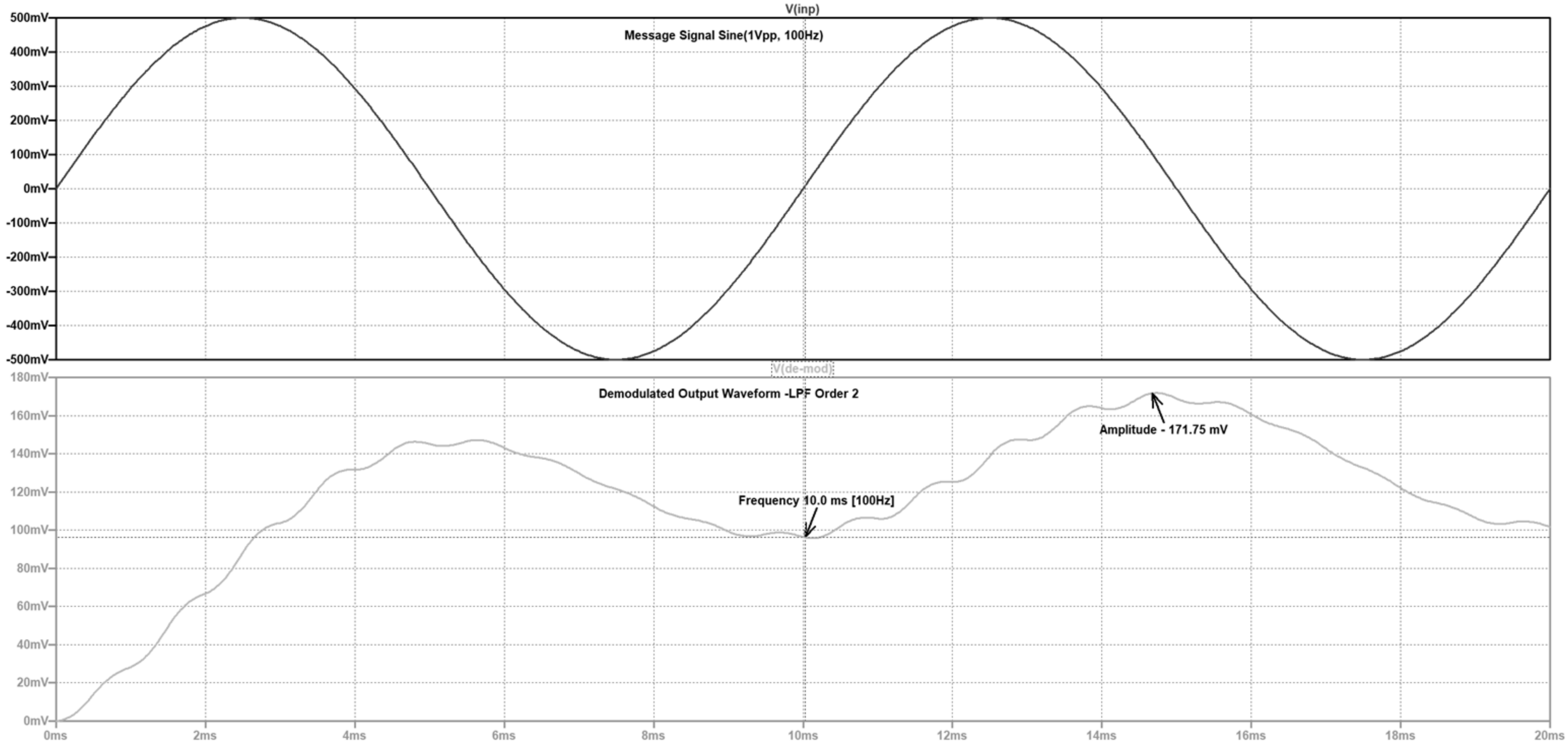


Fig 12 Low Pass Filter **Second** Order - Demodulated Output Waveform

Procedure Step 12

Observation *- The output starts to get distorted at carrier frequency above 100kHz. Because the amplifier is designed to operate only in the midband region and at high frequencies due to the internal capacitance effect of the parasitic capacitances the gain starts to decrease by 20dB/decade. This affects bias in turn affecting the gain thus producing distorted output.*

Inference :-

1. Amplitude of the pulse carrier varies proportional to the instantaneous amplitude of the message signal.

2. Noise inference is high.

ECE382 Communication Systems Lab.

Exp No. 5 2022-01-25

Amplitude Shift Keying Modulation and Demodulation

Nigil. M. R
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Aim:-

To design and implement amplitude shift keying modulator and demodulator.

Theory:-

Modulator:-

ASK is one of the digital modulation process, sinusoidal amplitudes are changed to two or more discrete amplitude levels. These are related to the number of levels adopted by the digital message.

For binary 0 and 1, the carrier switches between these two levels. In its simplest form a carrier is sent during one with amplitude A_1 and other one sent with amplitude A_2.

Demodulator:-

The demodulator consists of an envelope detector circuit and a comparator. The diode selects the positive half cycle of ASK modulated wave. The comparators then converts this detected signal to logic levels. This reference voltages may be varied to set a suitable reference voltage to this comparator.

Components Required:-

Component	Specification	Quantity
BC107 Transistor	-	1
Resistors	2.4K, 2.7K, 1K, 100Ω, 220KΩ	1 each
Regulated power supply	0-30V	1
capacitor	0.1μF, 0.68nF	1 each
Opamp (HA741)	-	2
Diode (1N4007)	-	1
DSO	-	

Procedure :-

1. Set up the circuit as in Fig 1.

2. Calculate G_{ON}, G_{OFF}, $I_C = 2mA$ at B (used transistor) and $R_1 = 1K\Omega$, Design R_C, R_B and R_2, such that

$$G(ON) = 1 + \frac{R_2}{R_1} \quad \text{and} \quad G(OFF) = 1 + \frac{R_2}{R_1 + R_C}$$

3. Derive the 5V supply from 12V using voltage divider circuit and use it for transistor.

4. Set message signal m(t) as square wave with $f_m = 1KHz$ and plot the output wave form at V_o and mark all salient points.

5. Set carrier signal c(t) as sine wave and plot the output waveform at pin 6 and mark all salient points.-

6. Now, set up the circuit as in Fig 2.

7. Given $C = 0.1\mu F$ and f_m as 1KHz, design value of R such that $f_m = \frac{1}{2\pi RC}$.

8. Plot the output waveform at V_F and measure peak-to-peak (V_{pp}) amplitude.

9. Vary V_{REF} from 0 to $V_{pp}/2$. Compute the values of V_{REF} such that you get the original message signal.

10. Plot the output waveform at PIN6 and mark all salient points. Do you see any difference between original signal and demodulated signal? If so; why?

11. Now, remove your voltage divider circuit (i.e disable Vcc and ground) and plot the output at PIN.

Do you find any difference between the waveform obtained at step 9 and step 10. If so, why?

Parameters and Design Equations :-

Modulation :-

G(ON) - ON time gain

G(OFF) - OFF time gain

$$G(ON) = 1 + \frac{R2}{R1} \quad \text{and} \quad G(OFF) = 1 + \frac{R2}{R1+RC}$$

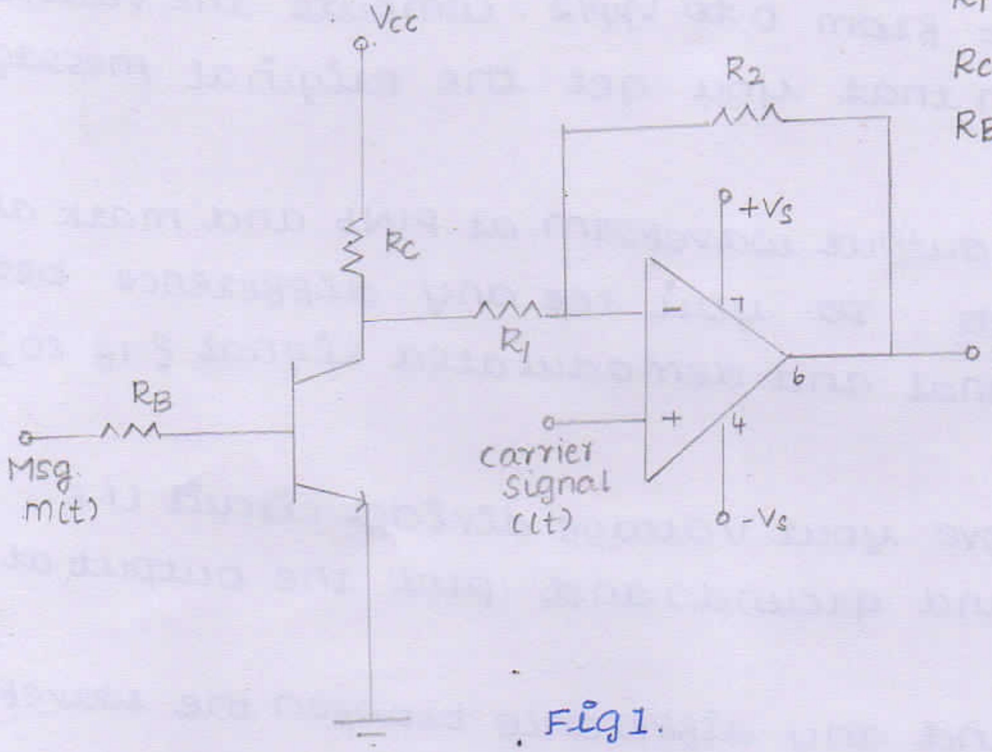
$$R_C = \frac{V_{CC} - 0.3}{I_C}, \quad R_B = \frac{V_{IN} - 0.7}{I_B'}$$

$$I_B' = 10\frac{I_C}{B}$$

Demodulation :-

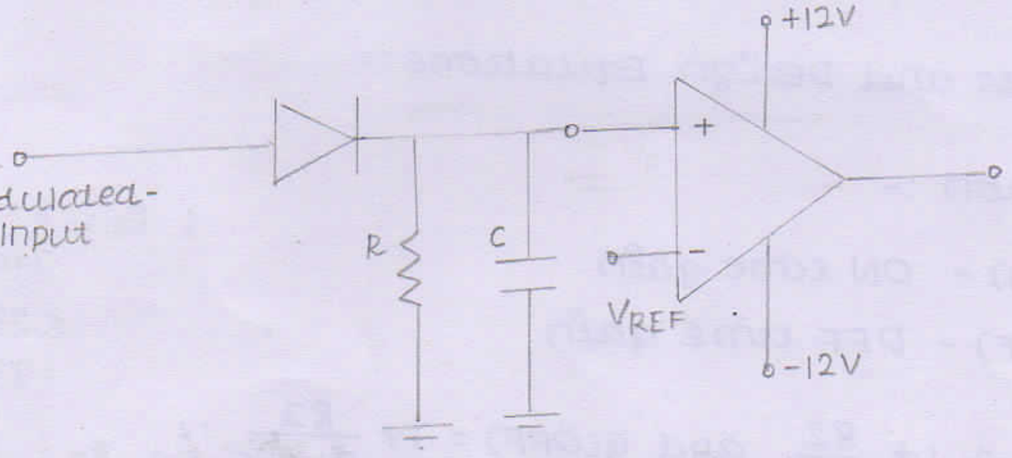
$$F_m = \frac{1}{2\pi RC}. \qquad \text{For } C = 0.1\mu F \quad R = 1.6K\Omega.$$

Circuit Diagram :-



Values :-
$R_2 = 0.1K$
$R_1 = 1K$
$R_C = 2.4K$
$R_B = 2.7K$

Fig 1.

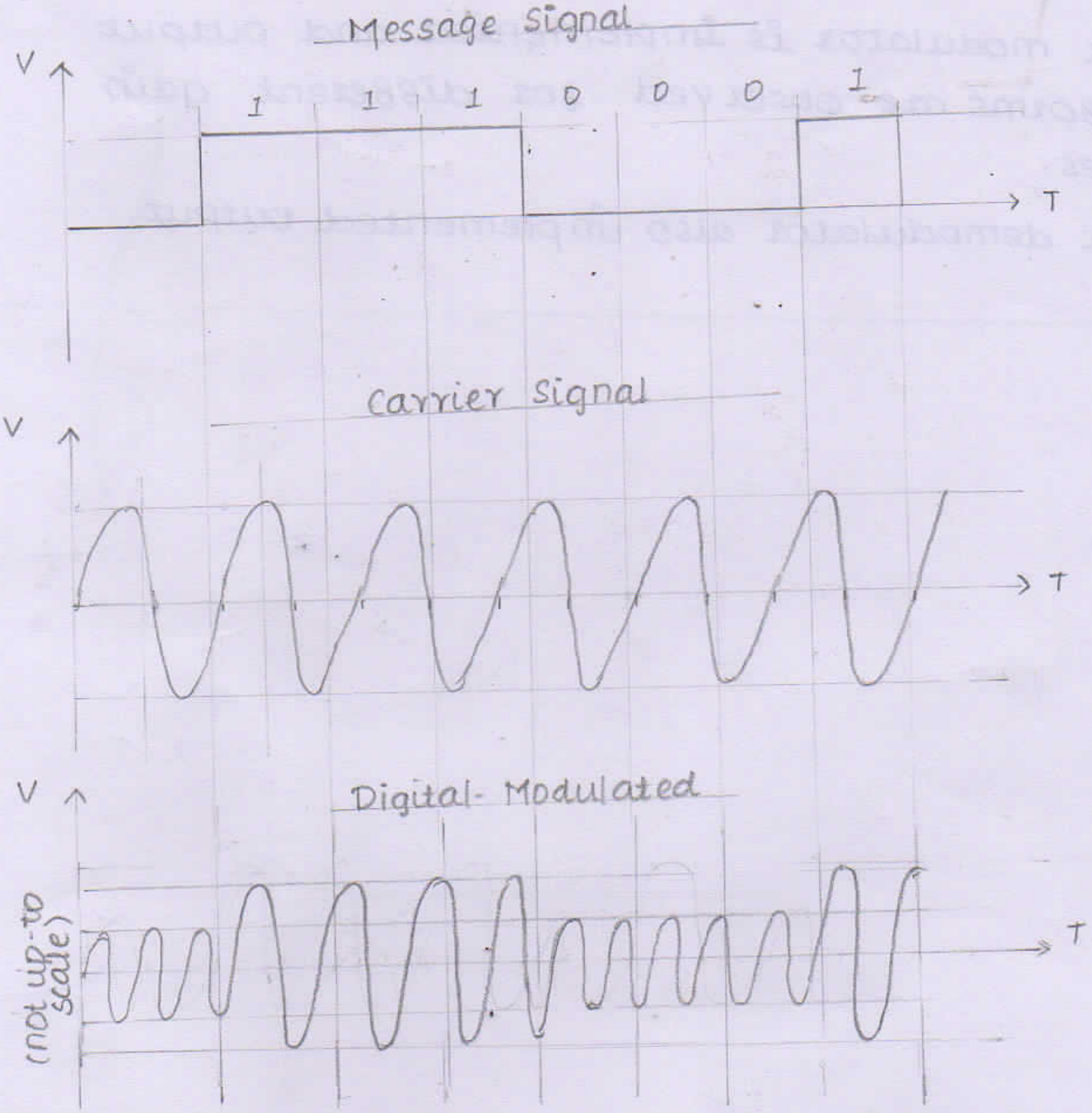


Values
$R = 1.6K$
$C = 0.1\mu F$

Fig 2.

* For All simulations ASK, PSK and FSK the message signal/ pulses are considered to be with 1 KHZ.

Model Graph:-



Results:-

(simulations attached).

Results

AMPLITUDE SHIFT KEYING MODULATION

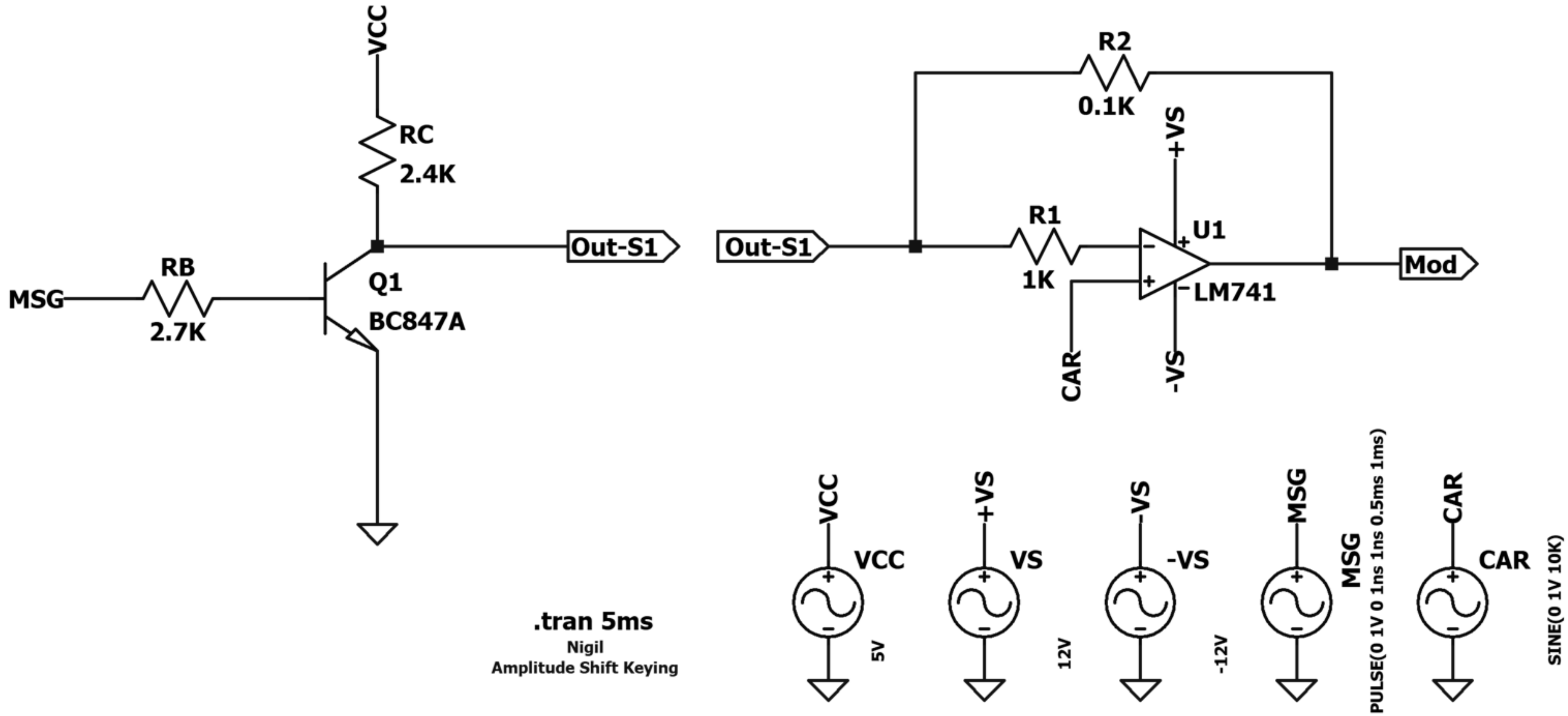


Fig 1 Circuit Diagram

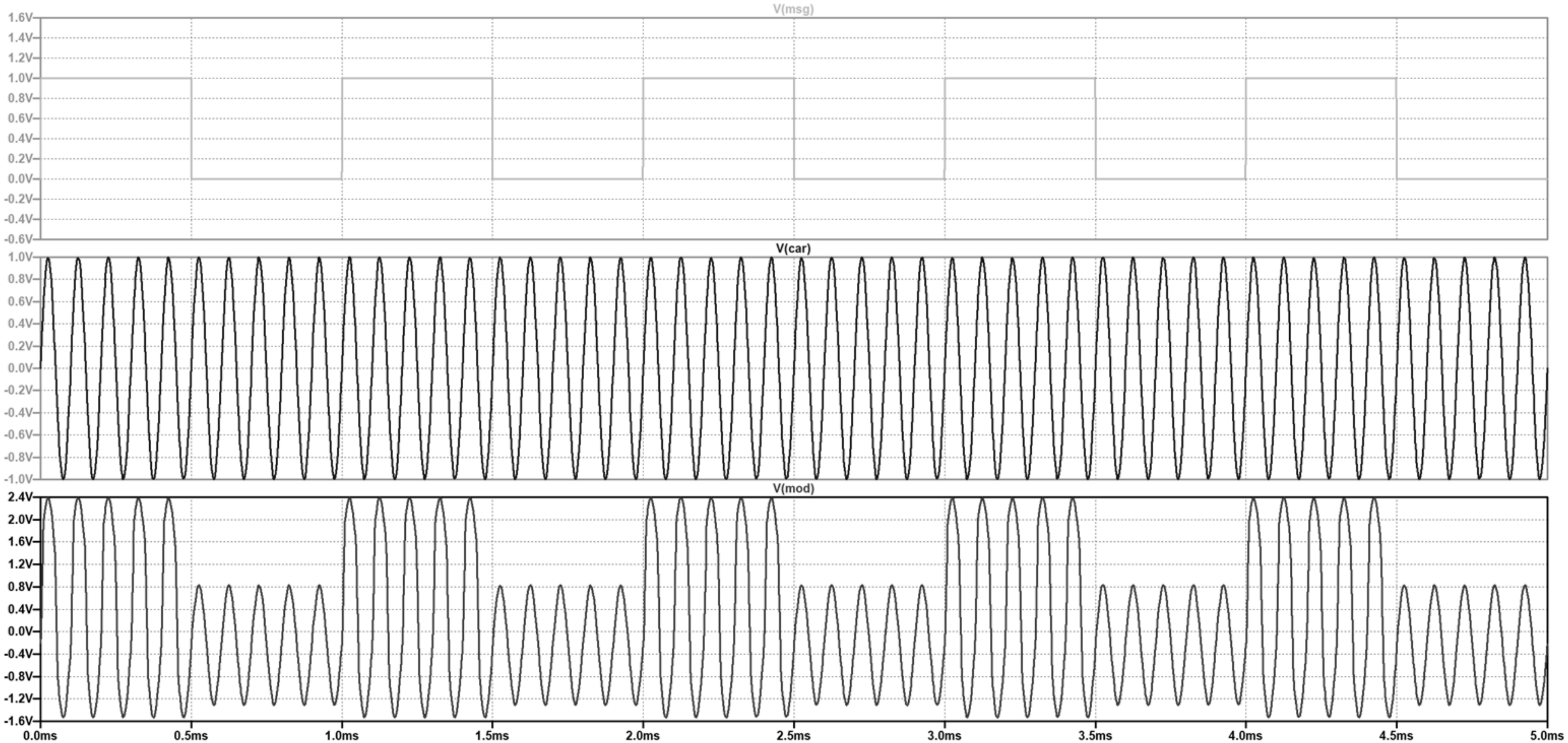


Fig 2 Output Waveform - Digital Amplitude Modulated Bandpass Signal

AMPLITUDE SHIFT KEYING DE-MODULATION

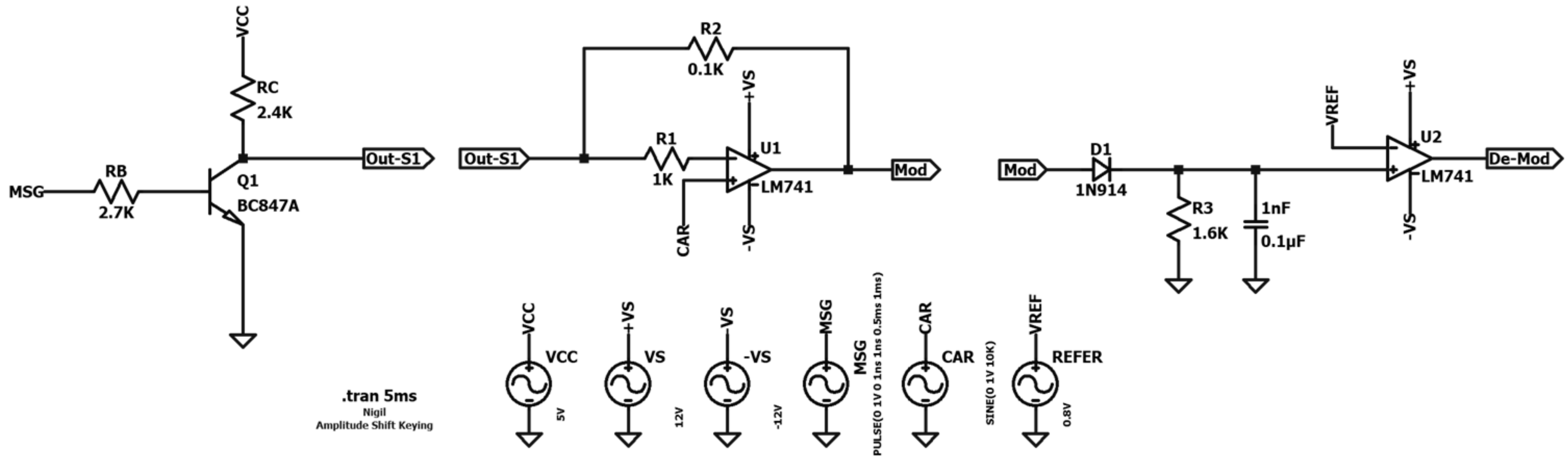


Fig 3 Circuit Diagram - Digital Amplitude Demodulator

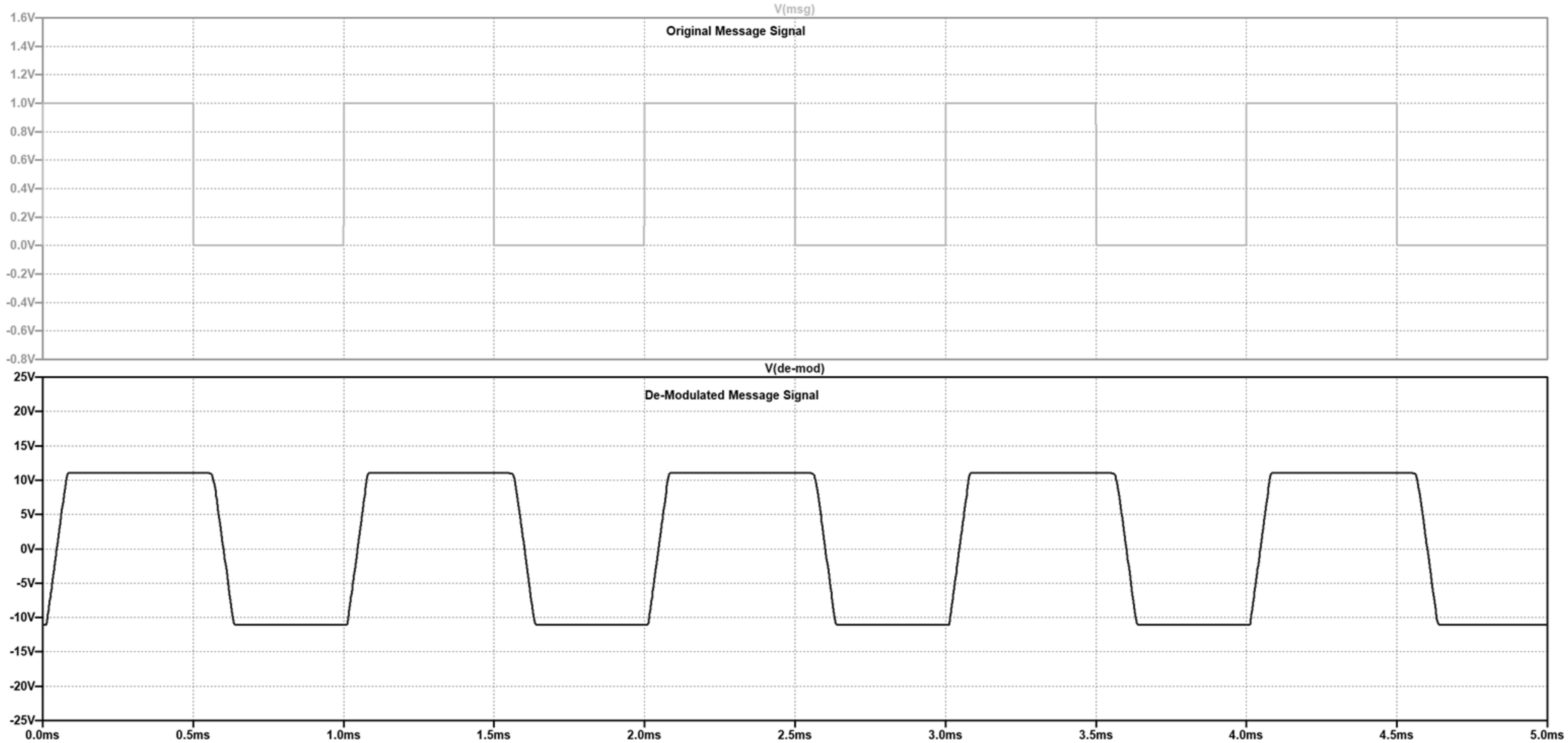


Fig 4 - Digital Amplitude Demodulator Output Waveform

Observation *- The OPAMP has a slew rate 0.5V/µs. So, the OPAMP when working as a comparator has to swing from +12V to -12V of the power supply and this takes time. This is the reason the output seems to be time shifted and the rising and falling edges has a slope less than 90 degrees.*

Inference:-

1. ASK modulator is implemented and output waveforms are observed for different gain values.

2. ASK demodulator also implemented output.

ECE382 Communication Systems Lab

Exp No. 6 27-01-22

Phase Shift Keying (PSK) Modulation.

Nigil. M.R

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Aim :-

To design and implement PSK circuit and verify the results.

Phase shift keying :-

Theory :-

The PSK is one kind of digital pass band modulation method. This kind of method is used to transmit data by modulating otherwise changing the phase of the carrier signal which is known as reference signal. This kind of modulation methods use a limited number of phases where each phase can be assigned with binary digitals. Generally, every phase codes and equivalent number of bits. Every bit pattern forms the symbol that is denoted by different phases of the carrier signal.

The PSK method can be represented by constellation diagram. In this kind of communication, the points of the constellation can be selected and are generally placed by uniform angular spacing in the region of circle. So that utmost phase seperation can be offered among nearby points & therefore given better performance of the system. These are arranged in a circle so they can all be transmitted by similar energy.

Components Required :-

Components	Specification	Quantity
Transistor	SL100, SK100	1;1
Opamp	741	1
Resistors	47kΩ	2
capacitor	0.1μF	1

Circuit Diagram :-

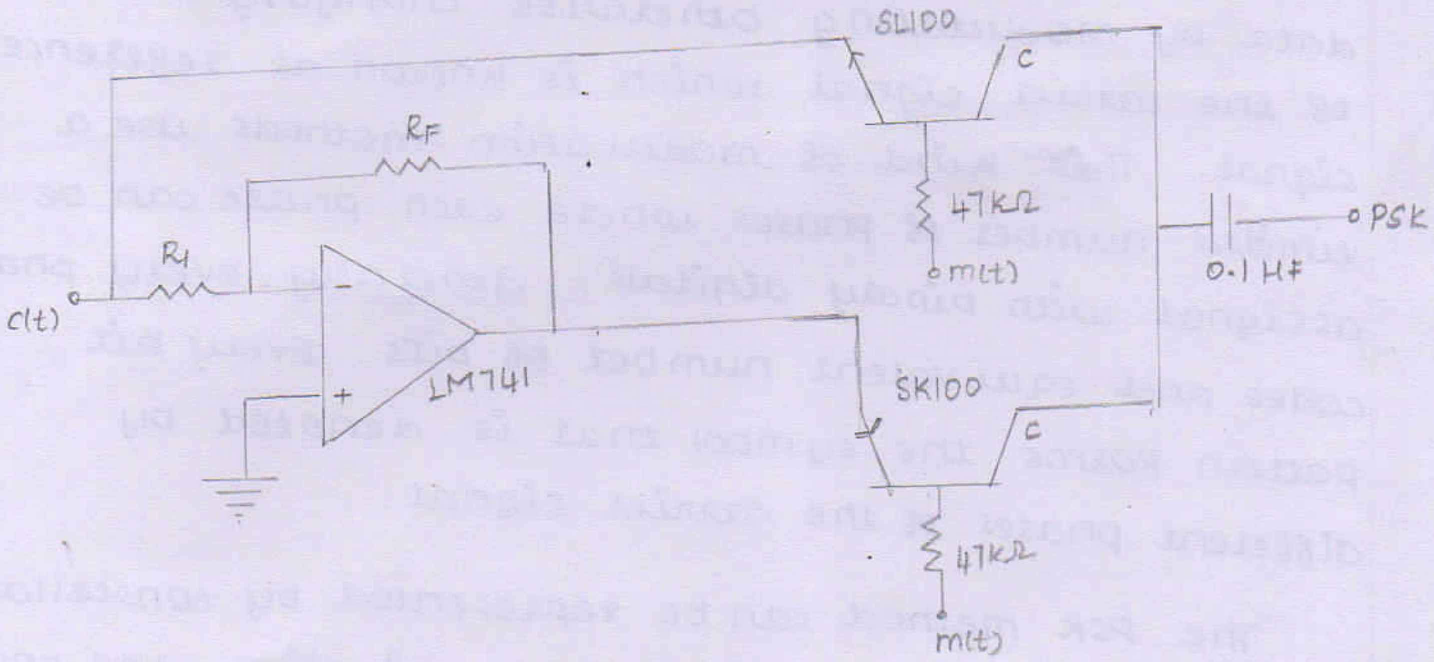


Fig 1.

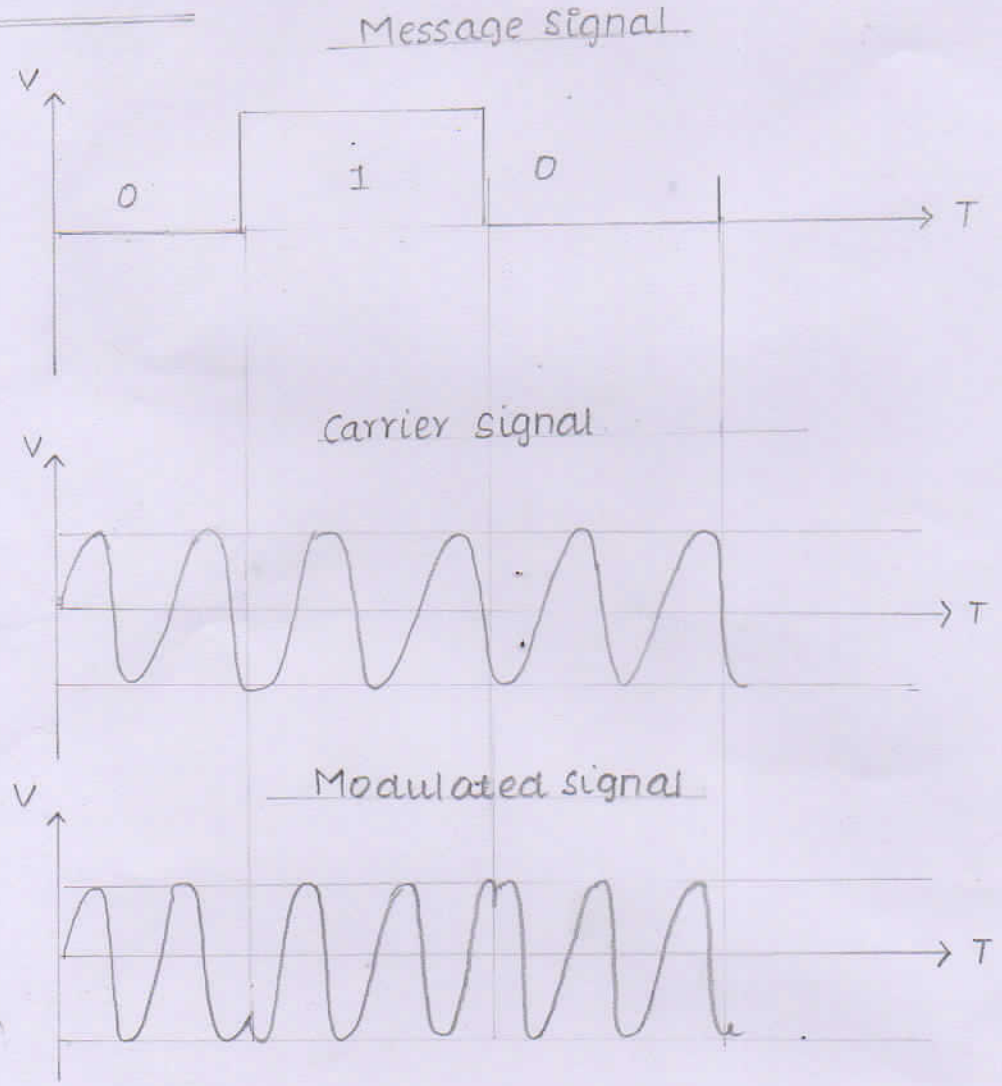
Design Equation :-

Inverting amplifier $(A_V) = -\frac{R_F}{R_1}$

Procedure :-

1. Set upthe circuit as Fig1. with appropriate message signal and carrier signal.
2. Design the inverting amplifier with the unity gain.
3. Plot the input and output waveform.

Model Graph :-



Results :-

(simulations attached).

Results

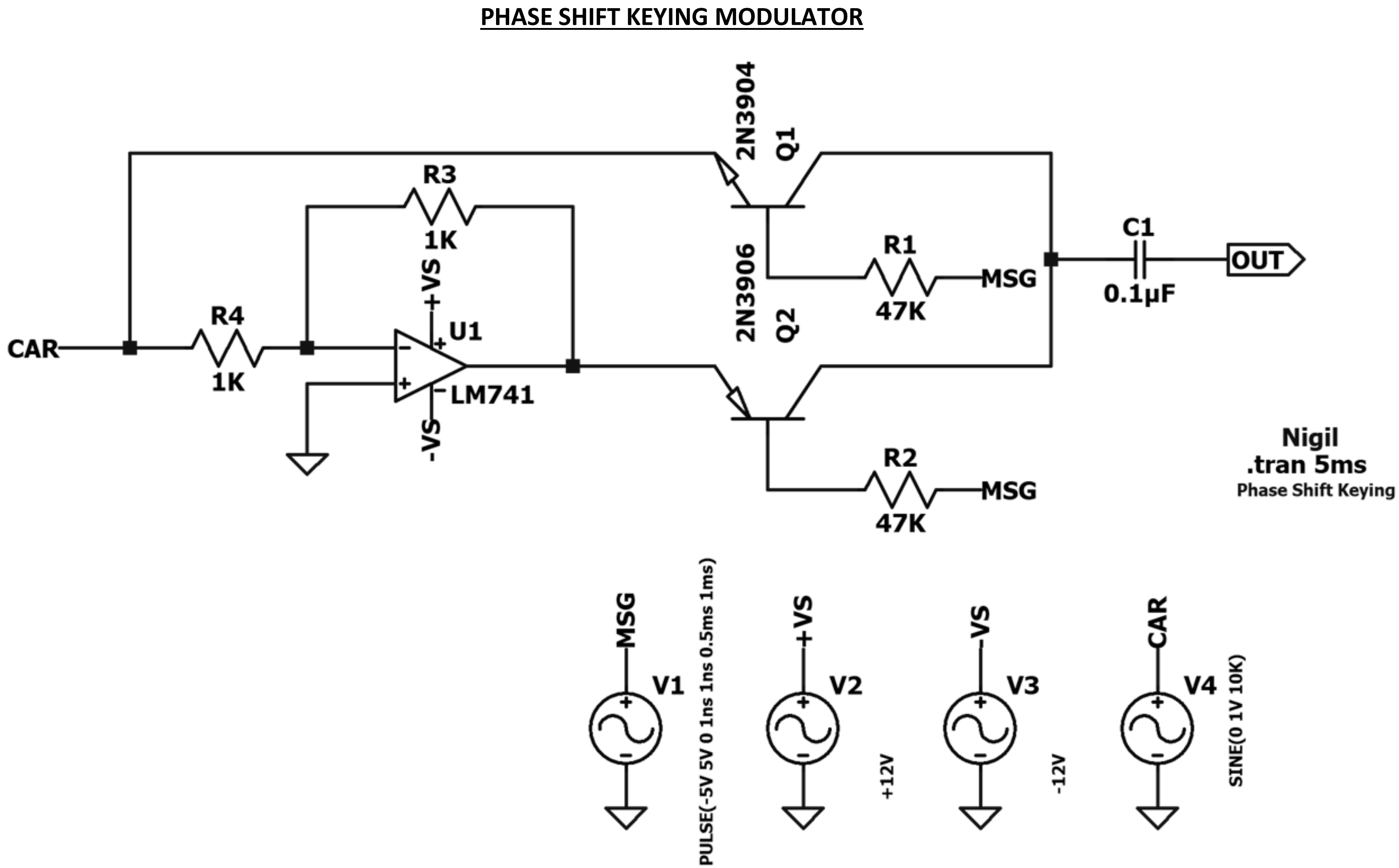


Fig 1 - Digital Phase Modulator Circuit Diagram

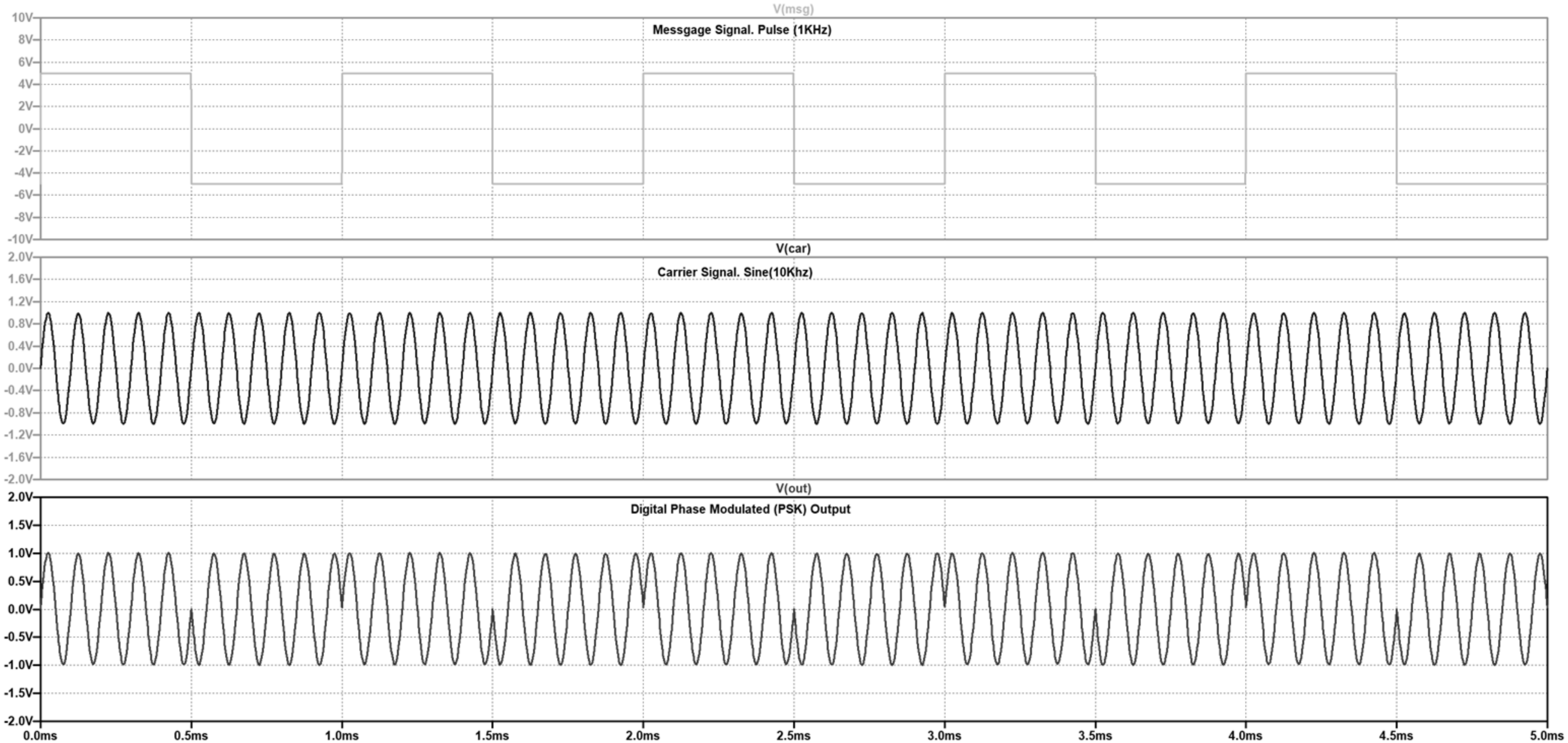


Fig 2 - Digital Phase Modulated Output Waveform

Inference:-

PSK Modulated signal analysed.

ECE 382 Communication systems Lab.

Exp No. 7 28-01-22

Frequency shift keying (FSK).

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Aim :-

To design and implement FSK modulator and verify the results.

Theory:-

Frequency shift keying is the digital modulation technique in which the frequency of the carrier signal varies according to the digital signal changes. FSK is a scheme of frequency modulation. The output of FSK modulated wave is high in frequency for a binary High input and is low in frequency for a binary Low input. The binary 1s and 0s are called Mark and space frequencies.

Components Required:-

component	specification	Quantity
Transistor	BC107	1
IC 555 Timer	-	1
Regulated Power supply	0-30V	1
Digital storage oscilloscope	-	1

Function Generator	-	2
Resistors	2.4K, 330K, 0.5K, 0.5K	4
capacitors	0.1HF, 10HF	2

Circuit Diagram :-

Resistor Values

R_A - 0.5K

R_B - 0.5K

R_C - 2.4K

R_b - 330KΩ

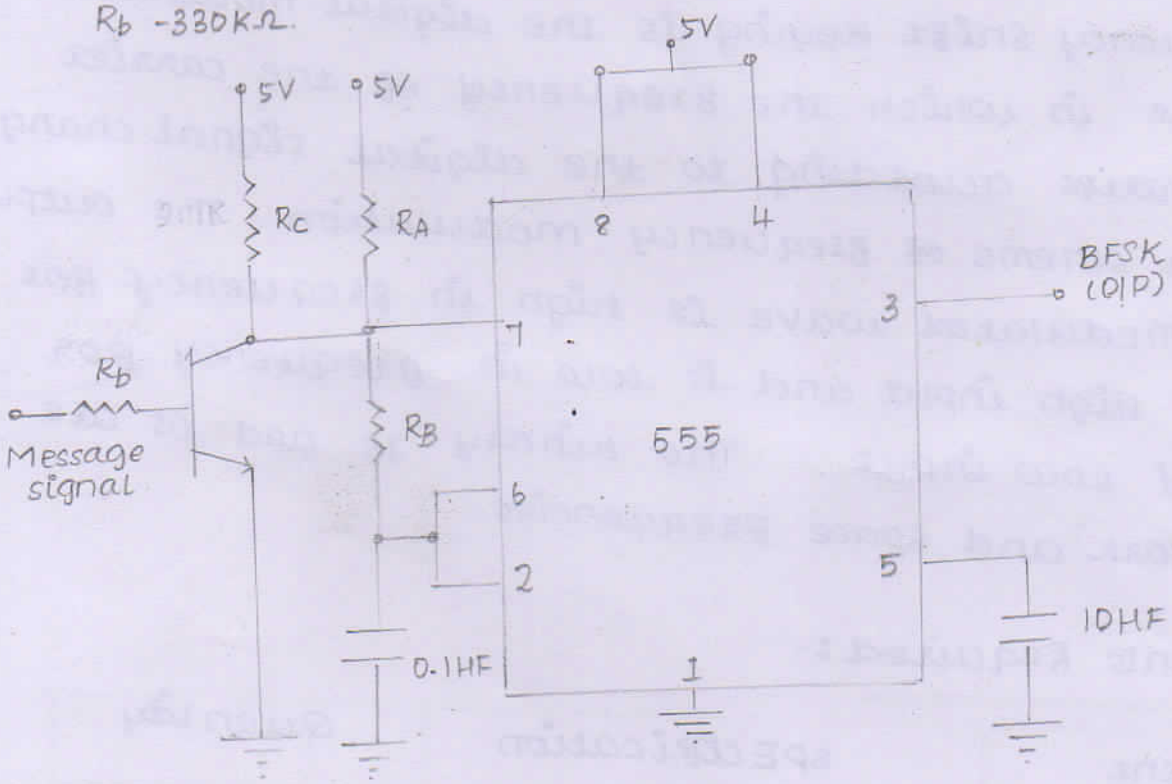


Fig 1.

Design Equation :-

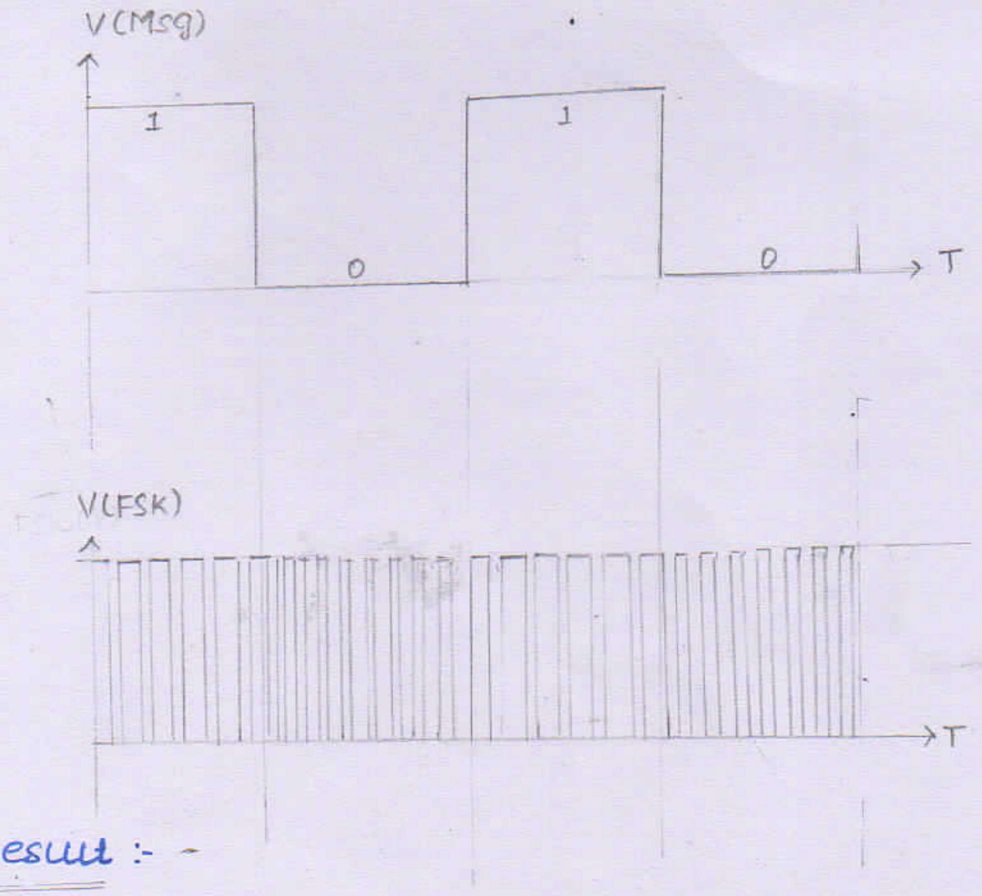
1. $$F_2 = \frac{1.45}{(R_A + 2R_B)C_1} \doteq 9666.67\,Hz \simeq 10KHz$$

$$F_1 = \frac{1.45}{((R_A \| R_C) + 2R_B)C_1} = 10.5KHz \text{ (appx).}$$

Procedure :-

1. Set up the circuit in Fig 1 for given frequencies.
2. Take the output at PIN3 of IC555 Timer without modulating signal. What is the output? Why?
3. Repeat step 2 by connecting the modulated (square wave) through switch and plot the waveform at PIN3.

Model Graph :-



Result :-

(simulation attached).

Results

FREQUENCY SHIFT KEYING MODULATOR

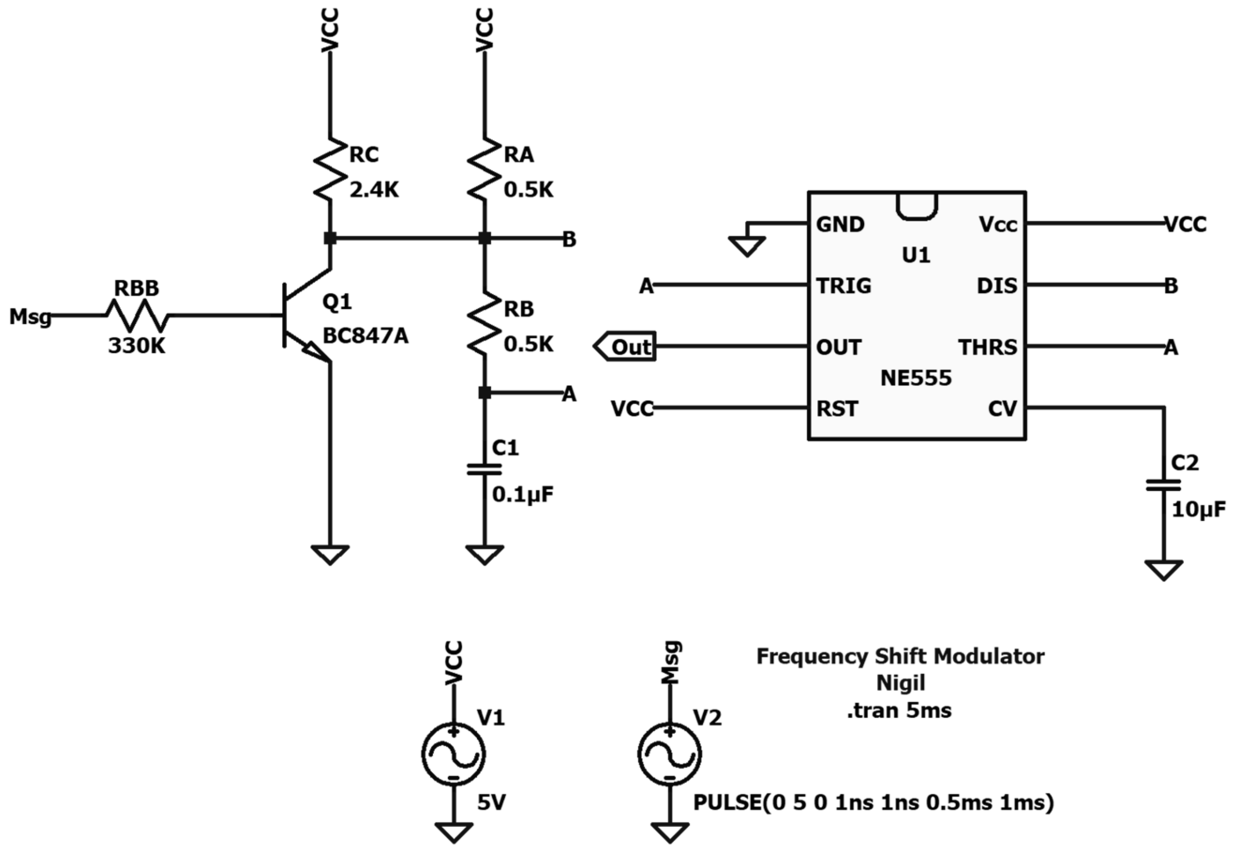


Fig 1 - Circuit Diagram FSK Modulator

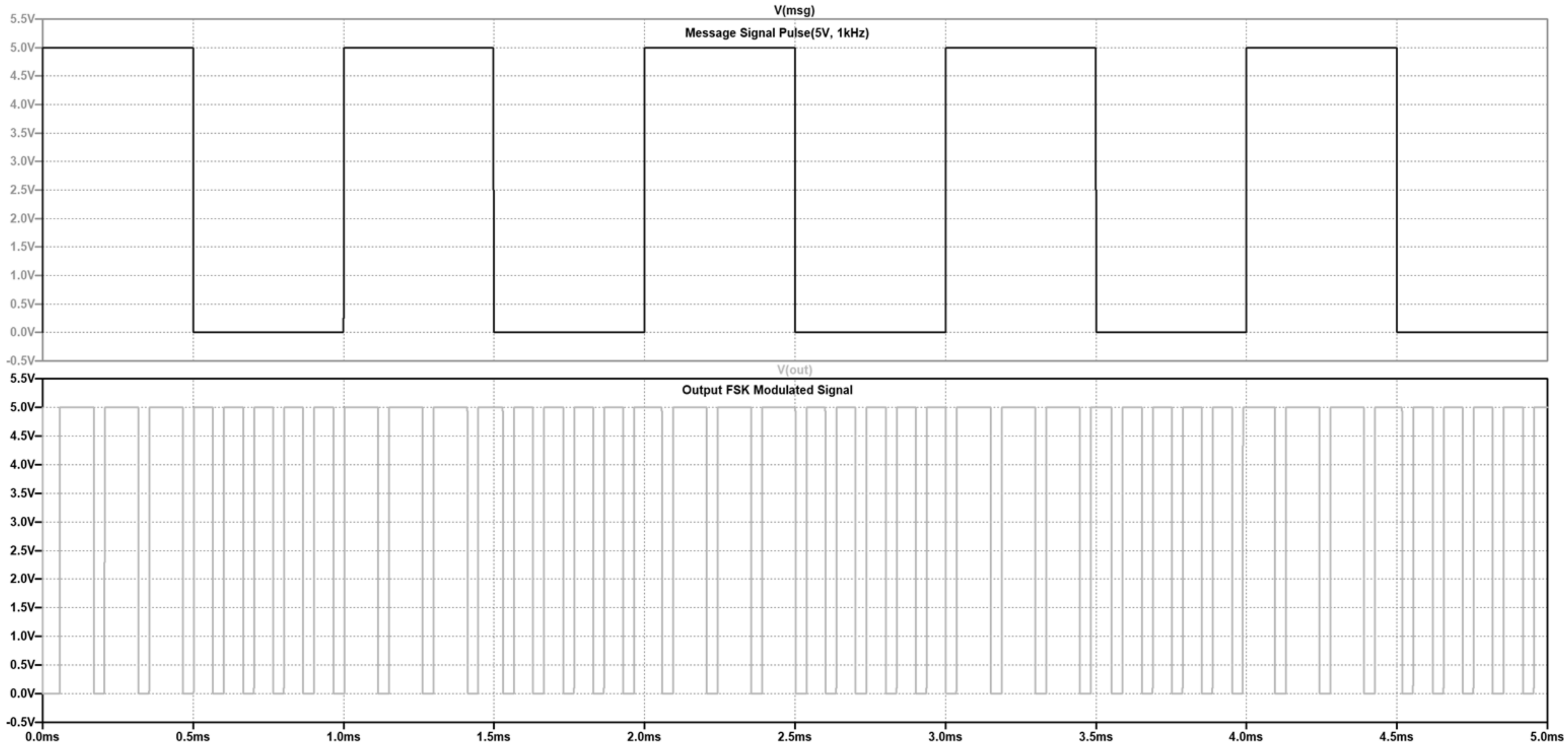


Fig 2 - Output Waveform - Digital Frequency Modulated Signal

Procedure Step 2 - Take the output at PIN3 of the IC555 Timer without the modulating signal. What is the output, why?

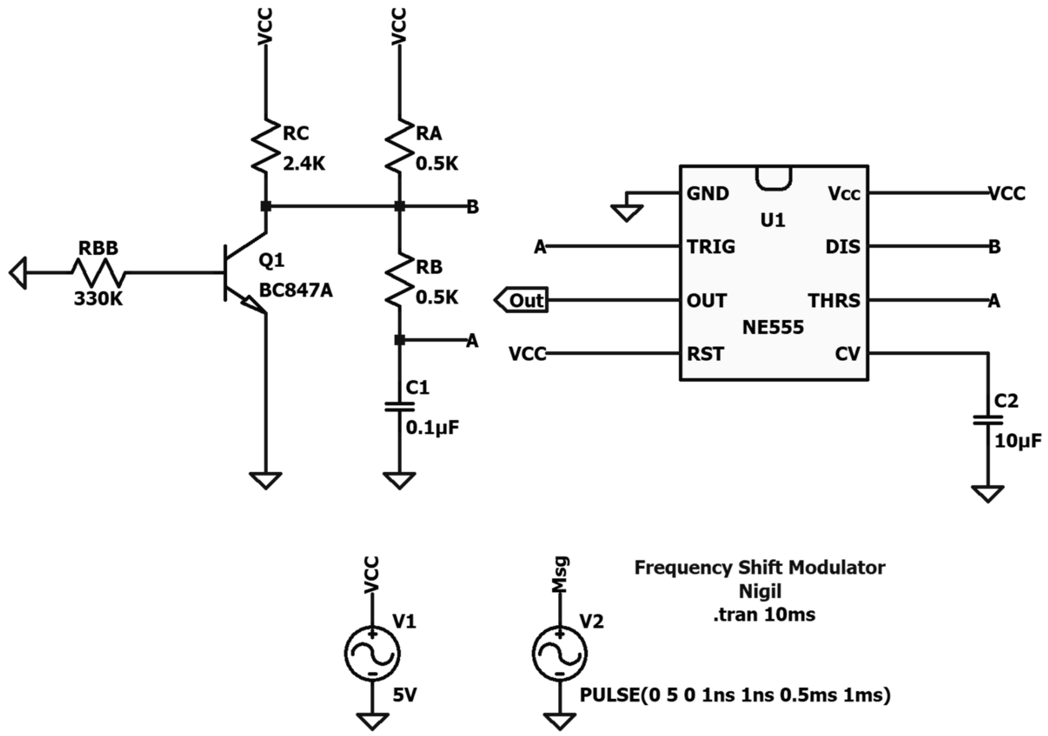


Fig 3 - Circuit Diagram (No Modulating Signal)

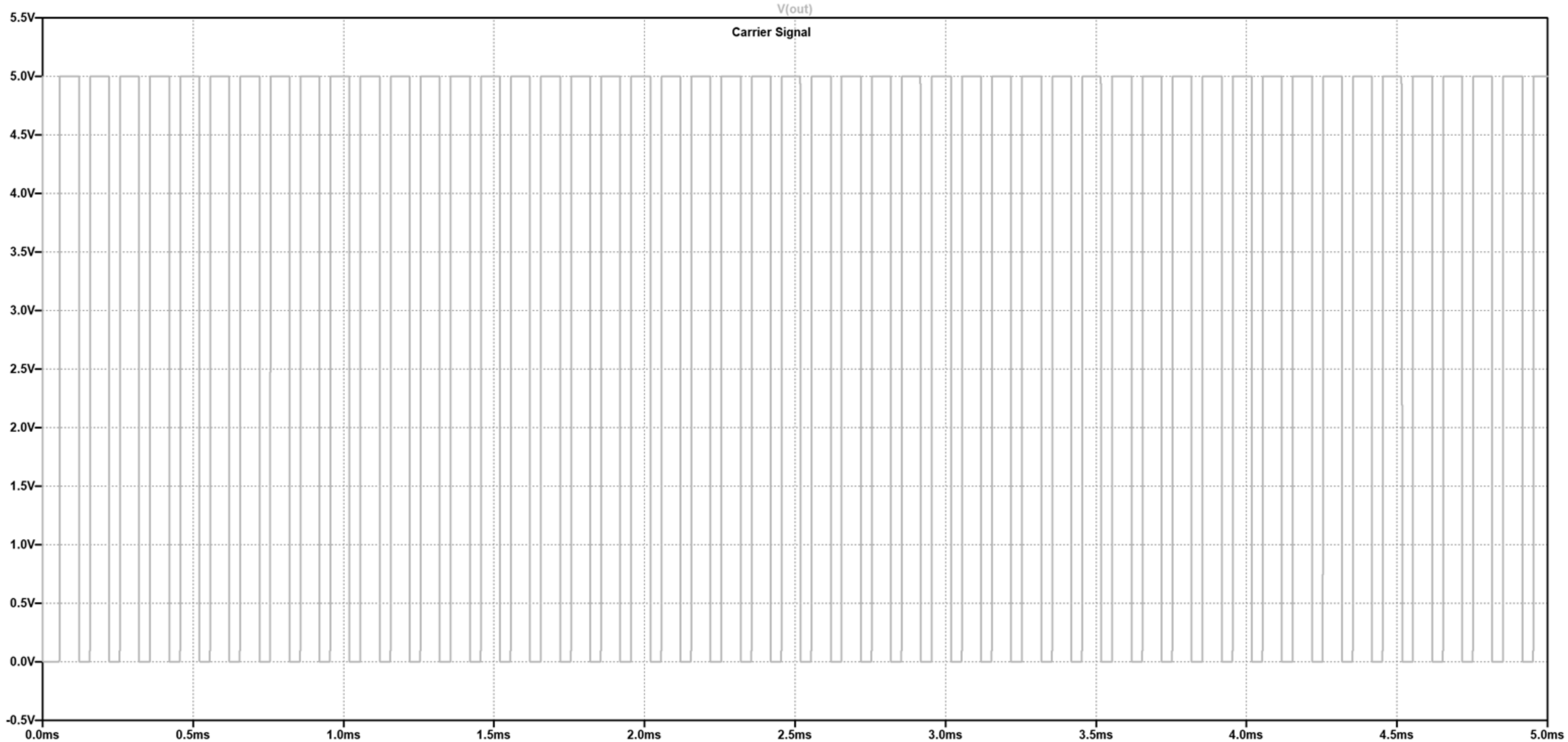


Fig 4 - Output Waveform (No Modulating Signal)

Observation - *Without the modulating signal the BJT does not act as a switch. So, the whole circuit operated as a astable multivibrator. Therefore, for value of 0.67*V_{CC} *&* *0.33*V_{CC} *the output keeps on changing. Note that this is the carrier frequency before getting modulated.*

Inference :-

FSK modulator is implemented and output waveforms are observed.