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Laboratory 6 - Superposition and Thevenin Equivalent

Simulation

<u>Problem 1</u>

Superposition Theorem

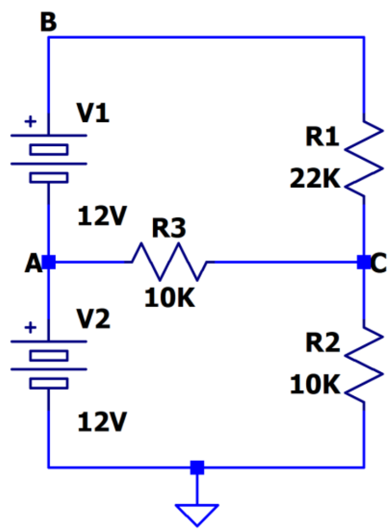

Fig 1. Circuit Diagram

```
--- Operating Point ---

V(c):        9.33333        voltage
V(b):        24             voltage
V(a):        12             voltage
I(R3):       0.000266667    device_current
I(R2):       -0.000933333   device_current
I(R1):       -0.000666667   device_current
I(V1):       -0.000666667   device_current
I(V2):       -0.000933333   device_current
```

Fig 2. Operating Points

Superposition: Voltage Source V2 Short Circuited

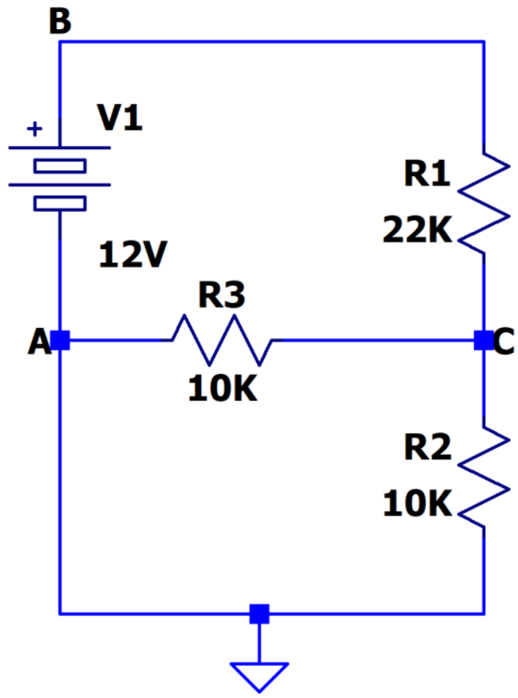

Fig 3a. Circuit Diagram

```
--- Operating Point ---

V(c):          2.22222         voltage
V(b):          12              voltage
I(R3):         -0.000222222    device_current
I(R2):         -0.000222222    device_current
I(R1):         -0.000444444    device_current
I(V1):         -0.000444444    device_current
```

Fig 3b. Operating Points

<u>Superposition: Voltage Source V1 Short Circuited</u>

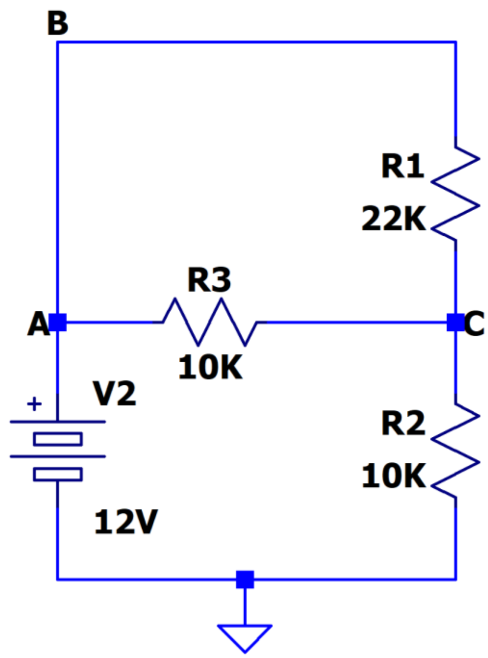

Fig 4a. Circuit Diagram

```
--- Operating Point ---

V(c):          7.11111        voltage
V(a):          12             voltage
I(R3):         0.000488889    device_current
I(R2):         -0.000711111   device_current
I(R1):         -0.000222222   device_current
I(V2):         -0.000711111   device_current
```

Fig 4b. Operating Points

Note that adding the voltages in Fig 3b and 4b. gives the same value as in Fig 2. Hence for a linear network superposition theorem is successfully proved.

<u>Problem 2</u>

Thevenin Network Theorem

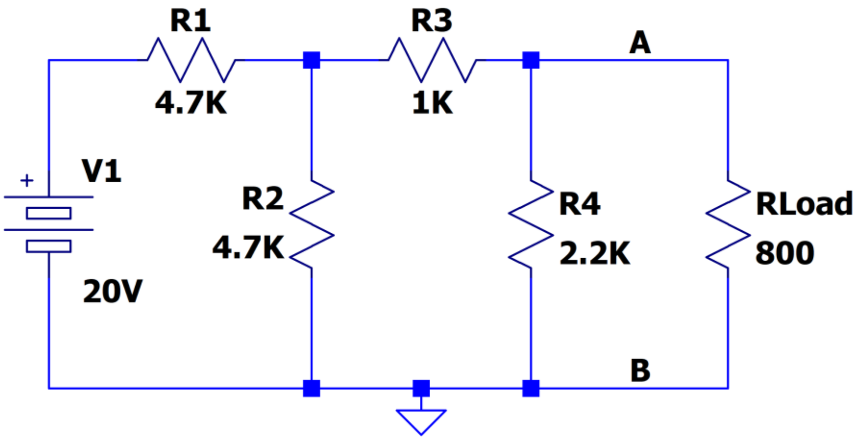

Fig 5. Circuit Diagram

--- Operating Point ---

V(n001):	20	voltage
V(n002):	4.03048	voltage
V(a):	1.49026	voltage
I(Rload):	0.00186283	device_current
I(R4):	0.000677392	device_current
I(R3):	0.00254022	device_current
I(R2):	-0.000857549	device_current
I(R1):	-0.00339777	device_current
I(V1):	-0.00339777	device_current

Fig 6. Operating Points

Here V_A is the voltage across the load resistor R_L

Problem 3

Thevenin Voltage (V_{TH})

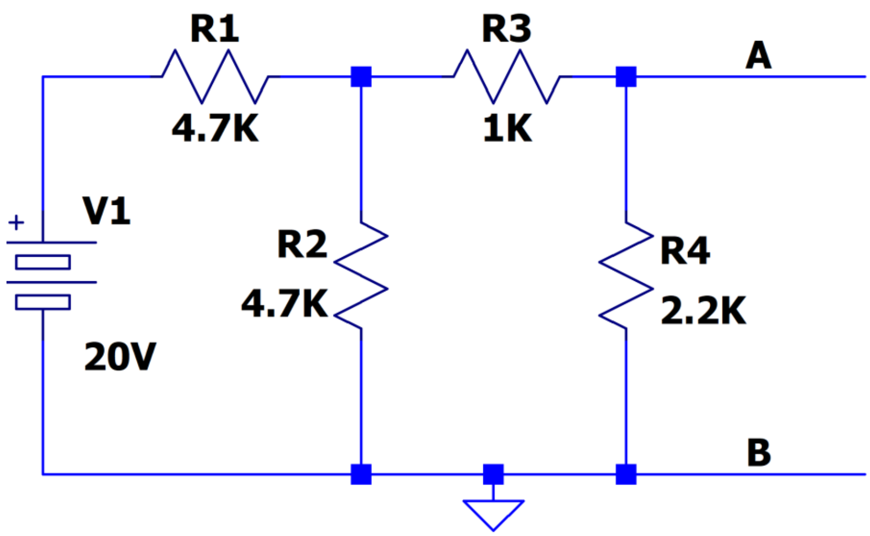

Fig 7. Circuit Diagram

--- Operating Point ---

V(n001):	20	voltage
V(n002):	5.76577	voltage
V(a):	3.96396	voltage
I(R4):	0.0018018	device_current
I(R3):	0.0018018	device_current
I(R2):	-0.00122676	device_current
I(R1):	-0.00302856	device_current
I(V1):	-0.00302856	device_current

Fig 8. Operating Point

Here V_A is the Thevenin Voltage.

In analytical case the Thevenin voltage is calculated by setting sources to zero and connecting a 1V test voltage source at the output to find the resistance seen by the load.

Here R_{TH} is around 1.327 kOhms. This can be approximated as E32 series standard resistor of 1.3 kOhms.

<u>Problem 4</u>

Thevenin Equivalent Model

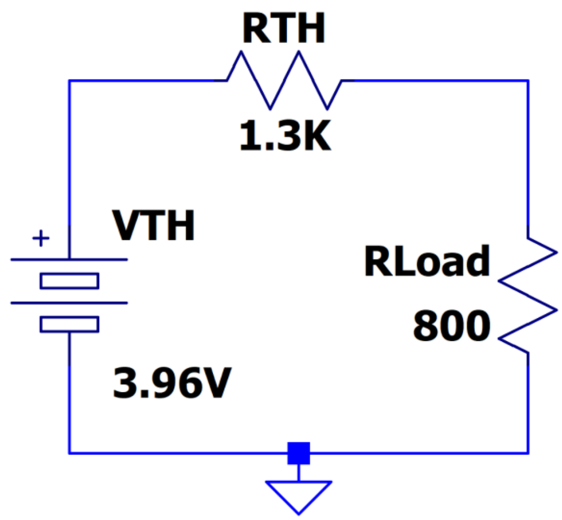

Fig 9. Circuit Diagram

```
--- Operating Point ---

V(n002):        1.50857         voltage
V(n001):        3.96            voltage
I(Rload):       -0.00188571     device_current
I(Rth):         -0.00188571     device_current
I(Vth):         -0.00188571     device_current
```

Fig 10. Operating Point

Here V_{N002} is the voltage across the load resistor which is same as the V_A of Fig 5 which is around 1.49026V. This difference is due to the assumption of standard E32 resistor series. Hence the Thevenin theorem is proved.

Error Percentage is around 0.667%

In case of LTSpice simulation the components are ideal and does not pose any resistance or parasitic capacitance. So, both the simulated value and calculated value will be the same.