Nihal Singh

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Work Authorization U.S. Citizenship

Research Interests Probabilistic Computing, Hardware-Software Co-design, AI Accelerators, Physics-inspired Generative AI

Education

University of California, Santa Barbara
Santa Barbara, CA

M.S./Ph.D, Electrical and Computer Engineering — *expected June 2026*

GPA: 3.96/4.0

Coursework: Fundamentals of Probabilistic Computing, From Statistical Mechanics to Quantum Computing, Uncertainty Quantification and Scientific Machine Learning, Neuromorphic Computing Systems, High-Speed Digital IC Design, Modeling and Simulation of VLSI Circuits, VLSI Project Design, Tensor Computation for ML and Big Data, Advanced Computer Architecture

Birla Institute of Technology and Science, Pilani
Pilani, India

B.E. (Hons.), Electrical and Electronics Engineering — *July 2021*

Relevant Coursework: Analog and Digital VLSI Design, Analog Electronics, Microelectronic Circuits, Electronic Devices, Computer Architecture, Neural Networks and Fuzzy Logic, Digital Design, Microprocessor Programming and Interfacing, Signals & Systems, Electromagnetic Theory

Recent Talks and Awards

- **Awarded the 2025 Misha Mahowald Prize for our work on Stochastic Neuromorphic Computing with Probabilistic Bits**
- **In-person Oral Presentation at International Workshop on Ising Machines (IISM) 2025**
- **In-person Oral Presentation at IEEE International Electron Devices Meeting (IEDM) 2024**
- **Invited Talk at the 20th RIEC International Workshop on Spintronics 2023**
- **In-person Oral Presentation at IEEE International Electron Devices Meeting (IEDM) 2023**
- **In-person Oral Presentation at APS March Meeting 2023**
- **Awarded UCSB ECE Outstanding TA Award with a $1,300 reward 2023**
- **Awarded UCSB ECE Department Fellowship for the first quarter of graduate studies 2022**

Experience

Hewlett Packard Enterprise
Santa Barbara, CA

Physics-based Generative AI Research Intern — *Jun 2025 - Sep 2025*

- Designed a Generative AI pipeline to model the thermodynamic properties of spin glasses and enable efficient generation of equilibrium states for accelerated sampling and optimization workflows
- Co-inventor on two invention disclosures (patent applications in progress); manuscript in preparation

University of California, Santa Barbara
Santa Barbara, CA

Graduate Research Assistant (Ph.D. Candidate) — *Sep 2022 - Present*

- Researching the hetero-integration of stochastic MTJs with CMOS for resource-efficient and scalable probabilistic computing techniques
- Working on hardware-software co-design approaches to map Ising machines and neural networks to p-computers enabling emerging optimization and generative AI algorithms

EPFL (École polytechnique fédérale de Lausanne)
Lausanne, Switzerland

Research Assistant — *Sep 2021 - Mar 2022*

- Funded Research Assistantship to work on developing GeSn-based single-photon avalanche diodes (SPADs) for efficient single-photon detection
- Contributed towards the molecular-beam epitaxy nanofabrication, simulation, and comprehensive characterization of sensing nanodevices
- Received comprehensive cleanroom training for machines and softwares needed for a wide range of process flows

QpiAI
Bengaluru, KA

Quantum Circuit Design Intern — *Dec 2020 - Jun 2021*

- Member of the team working on designing an Analog/RF-based cryogenic electronic chip for qubit control and readout
- Worked on the schematic, layout and simulations of a cryogenic trans-impedance amplifier and a cryogenic RF Mixer
- Developed novel architectures and control methodologies for scalable qubit design (aided by the use of nanodevice simulations)

Steradian Semiconductors (acquired by Renesas Electronics)
Bengaluru, KA

Research Intern (Radar System Engineering Team) — *Jul 2020 - Dec 2020*

- Bachelor's Thesis: Processing Stack Development for 4D MIMO mmWave Imaging Radars
- Coded custom GPU accelerated parallel algorithms for filtering, clustering, instantaneous velocity determination, heading angle estimation, etc.

Micron Technology
Hyderabad, TG

Design Verification Intern (DRAM Engineering Group) — *May 2020 - Jul 2020*

- Major Project: Accurate re-creation of vectors in Random Verification Methodology immune to testbench and environment modifications.
- Minor Project: Developed directed testcases for DDR4 corner case performance analysis.
- Training: Analysis of DDR4 architecture, protocols and datapaths using Cadence Virtuoso and SimVision.

Hyperloop India *Pilani, RJ*

Team Lead (Electrical and Electronics and LIM Propulsion) *Jun 2019 - Jul 2020*

- Led the team in engineering a custom on-board electrical and electronics architecture for the canceled 2020 SpaceX Hyperloop Pod Competition.

Team Anant *Pilani, RJ*

Executive Committee Member (Electrical Power System) *Mar 2018 - May 2021*

- Team of undergraduate students building a 3U Hyperspectral Imaging CubeSat under the guidance of the Indian Space Research Organisation.
- Working extensively on the design of EPS hardware architecture, circuit simulation and microcontroller programming.

Publications

Beyond Ising: Mixed Continuous Optimization with Gaussian Probabilistic Bits using Stochastic MTJs

N. S. Singh, C. Delacour, S. Niazi, K. Selcuk, D. Golenchenko, H. Kaneko, S. Kanai, H. Ohno, S. Fukami, K. Y. Camsari, IEEE International Electron Devices Meeting, 2024

CMOS plus stochastic nanomagnets enabling heterogeneous computers for probabilistic inference and learning

N. S. Singh, K. Kobayashi, Q. Cao, K. Selcuk, T. Hu, S. Niazi, N. A. Aadit, S. Kanai, H. Ohno, S. Fukami, K. Y. Camsari, Nat Commun 15, 2685 (2024).

Connecting physics to systems with modular spin-circuits

K. Selcuk, S. Bunaiyan, **N. S. Singh**, S. Sayed, S. Ganguly, G. Finocchio, S. Datta, K. Y. Camsari, npj Spintronics, 2024

Hardware Demonstration of Feedforward Stochastic Neural Networks with Fast MTJ p-bits

N. S. Singh, S. Niazi, S. Chowdhury, K. Selcuk, H. Kaneko, K. Kobayashi, S. Kanai, H. Ohno, S. Fukami, K. Y. Camsari, IEEE International Electron Devices Meeting, 2023

Parallelized Instantaneous Velocity and Heading Estimation of Objects using Imaging Radar

N. Singh, D. Sil and A. Sharma, 2021 IEEE Radar Conference (RadarConf21), Atlanta, GA, USA, 2021, pp. 1-6

Design and Comparative Analysis of a Two-Stage Ultra-Low-Power Subthreshold OpAmp

S. Nitundil, **N. Singh**, R. Balaji and P. Arora, 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 36-40

On-board Electrical, Electronics and Pose Estimation System for Hyperloop Pod Design

N. Singh, J. Karhade, I. Bhattacharya, P. Saraf, P. Kattamuri and A. M. Parimi, 2021 7th International Conference on Control, Automation and Robotics (ICCAR), 2021, pp. 223-230

Hardware Architecture of Electrical Power System for 3U Hyperspectral Imaging CubeSat

N. Singh, N. Raman, J. Parikh and V. Goradia, 2019 70th International Astronautical Congress Proceedings, 2019, pp. 446-456

Patents

Method and system for controlling a qubit for obtaining a scalable structure of a hybrid quantum-classical architecture

Authors: Pinakin Padalia, **Nihal Singh**, Umang Garg, Amlan Mukherjee, Nagendra Nagaraja

Publication Number: US20220398484A1, Date of Publication: 2022-12-15

Method and system for generating and regulating local magnetic field variations for spin qubit manipulation using micro-structures in integrated circuits

Authors: Umang Garg, Pinakin Padalia, Amlan Mukherjee, **Nihal Singh**, Nagendra Nagaraja

Publication Number: US20220269971A1, Date of Publication: 2022-08-25

Relevant Projects

Hardware Compatible Predictive Coding Model for SNN Training

- Developed a synthesizable Predictive Coding Model in Verilog to train spiking neural networks (SNNs)

Computational Modeling and Analysis of Large Brain Models

- Designed a scalable MATLAB model capable of simulating different regions of the brain by specifying the local neuronal types and dynamics

100MHz 256b SRAM Processing-in-Memory (PIM) Macro Design

- Worked on an area-efficient layout subsequent to the completion of schematic design and extensive simulations of the macro using Cadence tools

3.2GHz Oct-phase Phase-Locked Loop (PLL) Design

- Optimized the Oct-phase PLL through schematic design and circuit simulations using Cadence tools

Space-grade Frequency Re-configurable Antenna with Scalar Network Analyzer

Payload Design Proposal for Indian Space Research Organisation's (ISRO) PS4 Orbital Platform Initiative

- Prepared a proposal detailing the design of a multipurpose dynamically reconfigurable patch antenna with realtime verification and analysis using a Scalar Network Analyzer