SUMMER-2023

UNIT-1

Q.1 a) With the help of characteristics, explain the operation of PN Junction diode. What is the effect of forward & reverse biasing on depletion region? **(7)**

b) Explain how BJT can be used as amplifier. **(7)**

Q.2 a) Draw & explain input and output characteristics of common emitter configuration of BJT. **(7)**

b) Explain in brief

i) Cut in voltage of diode

ii) Reverse Breakdown voltage.

iii) Peak inverse voltage. **(7)**

UNIT-2

Q.3 a) Give the comparison of JFET & MOSFET. **(7)**

b) Explain the structure & operation of N-channel depletion type MOSFET. **(6)**

Q.4 a) Explain JFET parameters.

i) Saturation current

ii) Pinch off voltage

iii) Output Admittance **(6)**

b) What are Enhancement & Depletion MOSFETS? Explain construction & operation of Enhancement MOSFET. **(7)**

UNIT-3

Q.5 a) Convert following numbers to decimal

i) $(1E2)_{16}$ ii) $(214)_8$ **(7)**

b) Find subtraction of 110 & 101 using 2's complement method. **(6)**

Q.6 a) Explain decimal number system, Binary number system, octal number system & Hexadecimal number system with example. **(6)**

b) Convert following binary to

i) $(110110001010)_2$ = octal

ii) $(100110)_2$ = Gray code

iii) $(11110)_2$ to Excess – 3 code. **(7)**

UNIT-4

Q.7 a) Solve following logic function using quine McCluskey method.

$F(x_1,x_2,x_3,x_4) = \Sigma m(0,1,3,8,9,11,15)$ **(13)**

Q.8 a) Reduce following fuction using k-map & also draw the logic diagram

$f(x_1,x_2,x_3,x_4) = \Sigma m(0,1,3,4,5,7,10,13,14,15)$ **(7)**

b) Minimize following switching function using k-map

$f(A,B,C,D) = \Sigma m(1,3,7,11,15) + d(0,2,5)$ **(6)**

UNIT-5

Q.9 a) Describe the steps of combinational logic design. Explain with suitable example. **(7)**

b) Implement following function using suitable multiplexer

$f(A,B,C,D) = \Sigma m(0,1,3,4,8,12,14)$ **(7)**

Q.10 a) Explain in detail 4-bit parallel subtractor. **(7)**

b) Implement following expression using decoder.

i) $f_1 = M(0,1,5,8,9)$ ii) $f_2 = M(1,2,3,7,12,14)$ **(7)**

UNIT-6

Q.11 a) Explain synchronous & Asynchronous counter in detail. **(7)**

b) Convert D flip flop to

i) SR flip-flop ii) T flip-flop **(6)**

Q.12 a) Design synchronous MOD-6 counter using JK flip flop. **(6)**

b) Convert S-R flip-flop to J-K flip-flop. **(7)**