Sipna College of Engineering & Technology, Amravati
Department of Computer Science & Engineering
Question Bank
Unit V & VI

UNIT-V

Q1: Design BCD to Excess-3 code converter using minimum number of logic gates
Q2: Realise 5-line to 32-line decoder using 4-line to 16-line decoder.
Q3: Design 9-bit odd parity checker using IC 74180 and explain working.
Q4: Design 10-bit even parity generator using single 74180 and inverter.
Q5: Design a logic circuit to generate an even parity bit for 3-bit binary input.
Q6: Design 1:32 D-MUX using 1:16 D-MUX
Q7: Explain decimal to BCD priority encoder.
Q8: Design a hexadecimal to binary priority encoder using 74148 ICs and one 74157 MUX.
Q9: Design 32:1 MUX using 16:1 MUX ICs and an OR gate.
Q10: Design 5-bit comparator using a single 7485 and one gate.
Q11: Design Binary to Gray code converter
Q12: Design 4-bit Look Ahead Carry adder and explain its operation.
Q13: Design Full Adder using MUX.
Q14: Design 32: l multiplexer using 8: 1 multiplexer
Q15: Implement the following function using 4- line to l6- line decoder.
F1 =∑ m (0.1,2,5,7), F2 = ∑m (7,9,10,1l, l2), F3 =∑m (8,11,13,14,15).
Q16: Implement the following Boolean expression using multiplexer

i) $Y = \bar{A}B\bar{C} + A\bar{B}\bar{C}D + \bar{A}\bar{B}D + \bar{A}CD$
ii) $Y = (A + B)(\bar{A} + B + C)(A + \overline{B})$

UNIT-VI

Q1: What is Shift Register? Explain 3-bit shift register along with neat Timing diagram.
Q2: Draw a mod - 8 synchronous counter using T flip - flop. Explain the same with the help of Timing diagram.
Q3: What is race around condition? How does it get eliminated in a master slave J - K flip flop? Explain.
Q4: With the help of neat diagram. explain the working of 4-bit ring counter, also give the timing diagram.
Q5: Draw and explain the operation of 4-bit Bidirectional shift Register
Q6: State different types, of shift registers. Explain the operation of 3-bit shift register with neat diagram.
Q7: Design a 3-bit synchronous counter using J-K F/F.
Q8: Explain the operation of 4- stage twisted ring counter using D F/F.
Q9: Design Universal Shift Register and explain its operation.
Q10: Draw and explain the circuit diagram for M-S-J-K F/F and explain its advantages over JK F/F.
Q11: Explain performance comparison of counters and shift registers.
Q12: Design 3 bit synchronous up/down counter.
