Page No.
Date

5. Combinational Circuits.

A Digital system consist of two types of circuits namely i) combinational logic circuit ii) sequential logic circuit.
In Any logic circuit if output depends only on present input such type of logic circuit is called as combinational logic circuit.
e.g code Converter
Mux (Multiplexer) / DeMux
Encoder, Decoder etc.

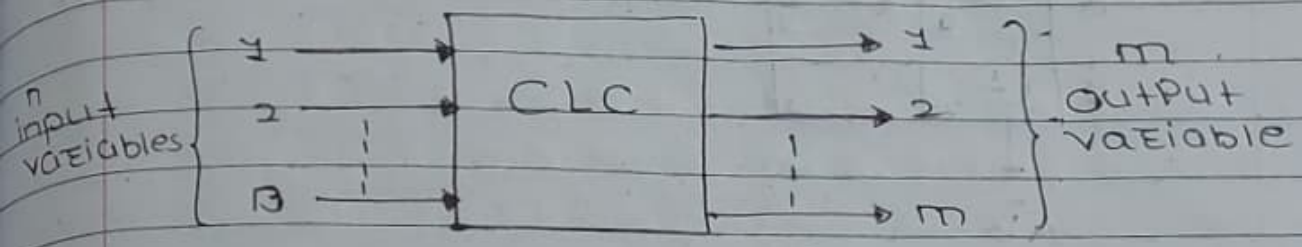
On the other hand if output of logic circuit depend not only on the present input but also on the past outputs such type of logic circuit is called Sequential logic circuit.
e.g

A combinational logic circuit consist of input variable, logic gates and output variable. The logic gates accepts input from
and produces output signals.

Page No.
Date : / /

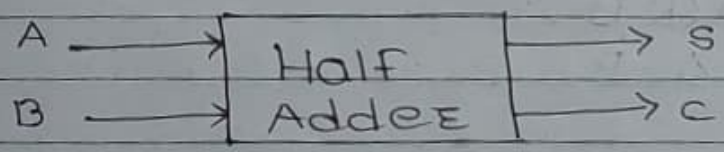
$A \oplus B = \bar{A}B + A\bar{B}$

$\overline{A \oplus B} = A \odot B = \bar{A}\bar{B} + AB$



Half Adder

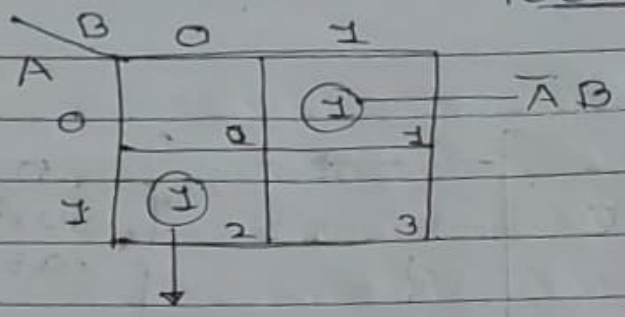
A logic circuit that performs the Arithmatic addition of two bits is called Half Adder. The Half Adder needs to inputs and two binary output i.e Sum and carry. fig shows the block diagram of Half adder.



I/P		O/P	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Page No.
Date : / /

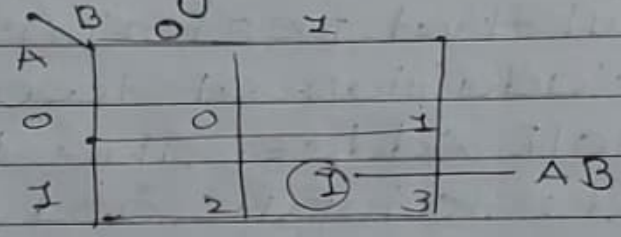
FOR SUM



$\therefore S = A\bar{B} + \bar{A}B$

$S = A \oplus B$

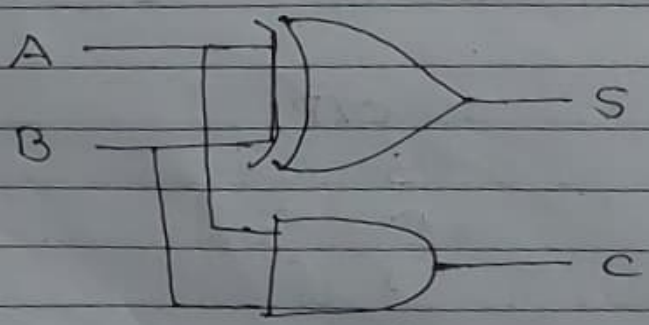
FOR CARRY.



$\therefore C = AB$

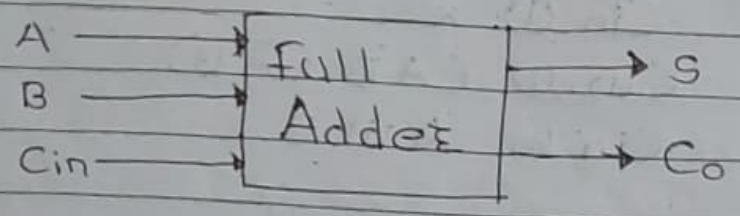
$S = A \oplus B$

$C = A \cdot B$



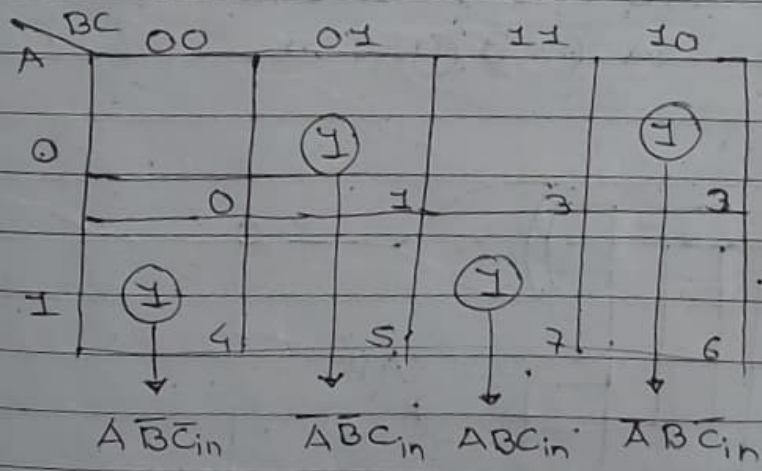
Page No.
Date : / /

• Full Adder



I/P			O/P	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

for Sum



$$S = A\bar{B}\bar{C}in + \bar{A}\bar{B}Cin + \bar{A}B\bar{C}in + ABCin$$
$$= \bar{C}in(A\bar{B} + \bar{A}B) + Cin(\bar{A}\bar{B} + AB)$$

EX-OR EX NOR

$$=$$ Assume $A\bar{B} + \bar{A}B = X$

Page No.
Date : / /

$= \bar{C}in\, x + Cin\, \bar{x}$ $\quad (A \oplus B = A\bar{B} + \bar{A}B)$

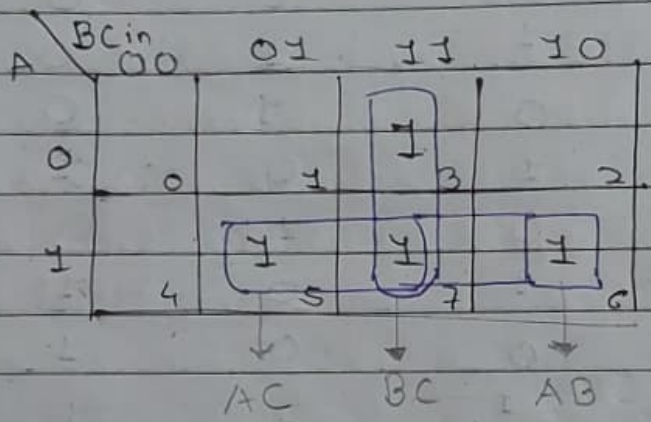
$= Cin \oplus x$

$= Cin \oplus (A\bar{B} + \bar{A}B)$

$= Cin \oplus A \oplus B$

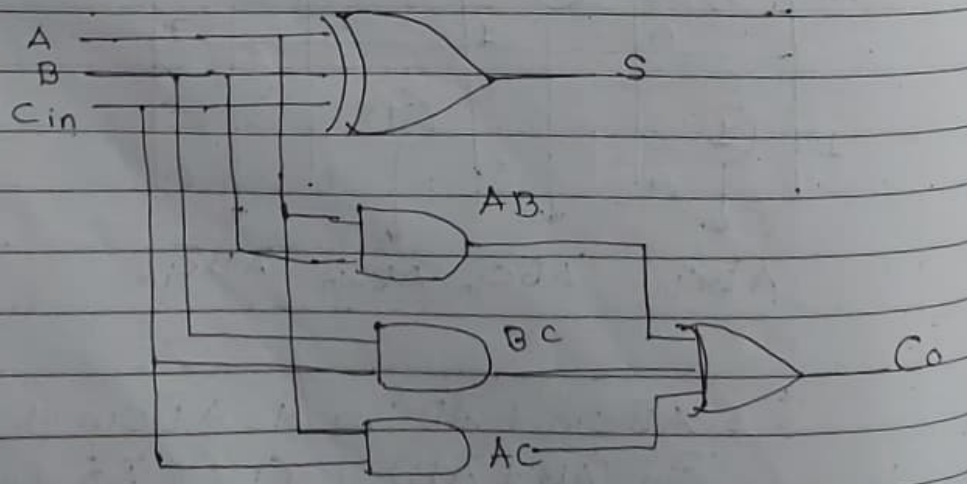
$\therefore S = A \oplus B \oplus Cin$

For Carry :-



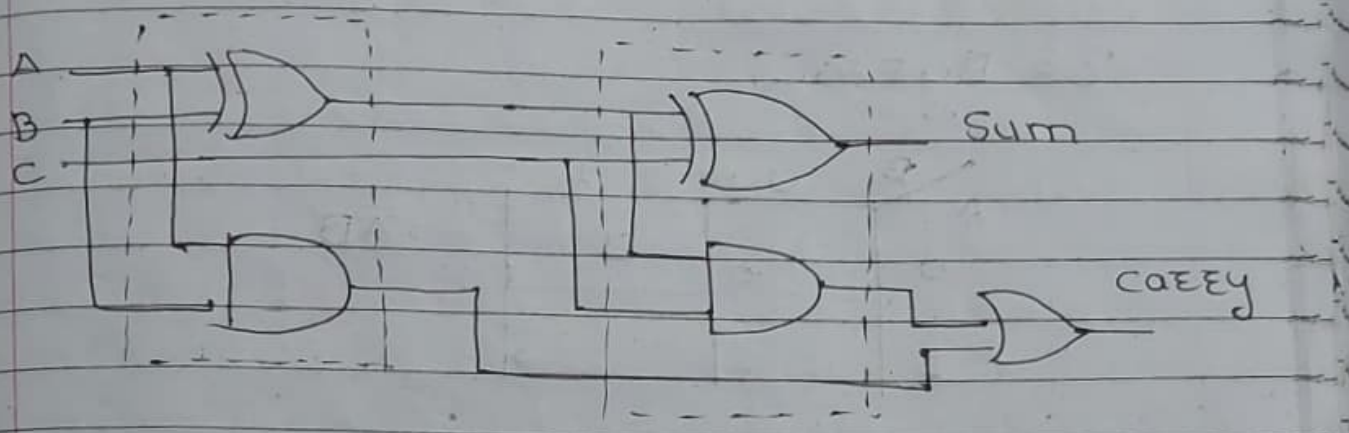
$C = AB + BC_{in} + ACin$

$S = A \oplus B \oplus Cin.$

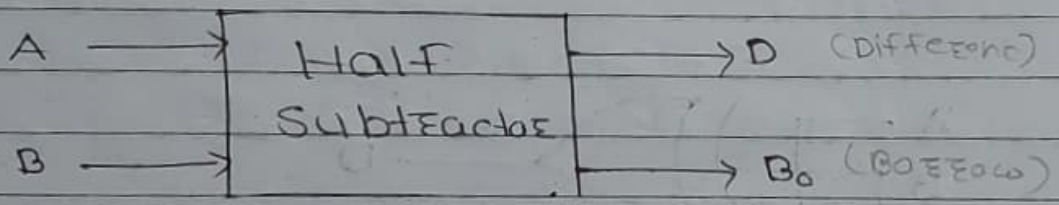


Page No.
Date : / /

- Realisation of full Adder using two half Adder

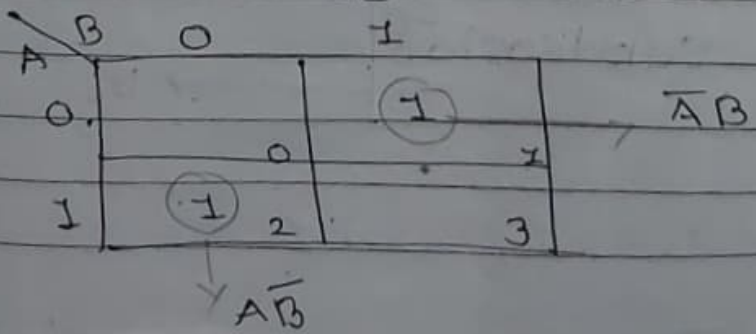


* Half Subtractor



I/P		O/P B	
A	B	D	B_o
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

⇒ for Difference

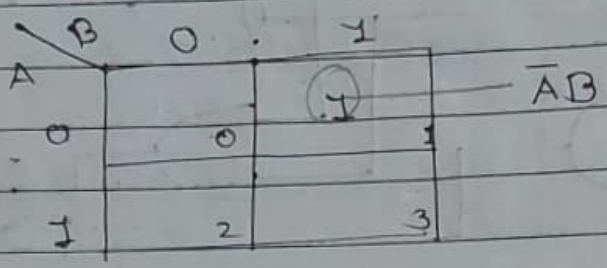


Page No.
Date : / /

$\therefore D = A\bar{B} + \bar{A}B$

$D = A \oplus B$

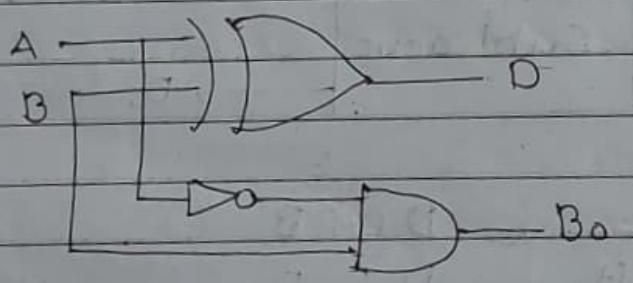
for Borrow



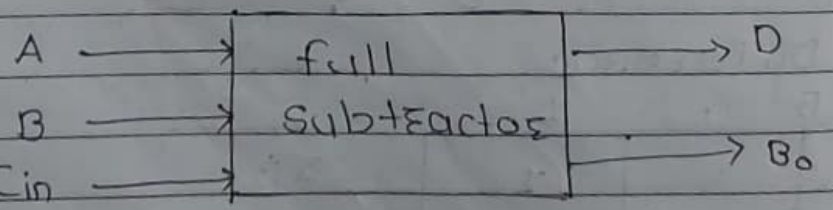
$B_0 = \bar{A}B$

$D = A \oplus B$

$B_0 = \bar{A}B$



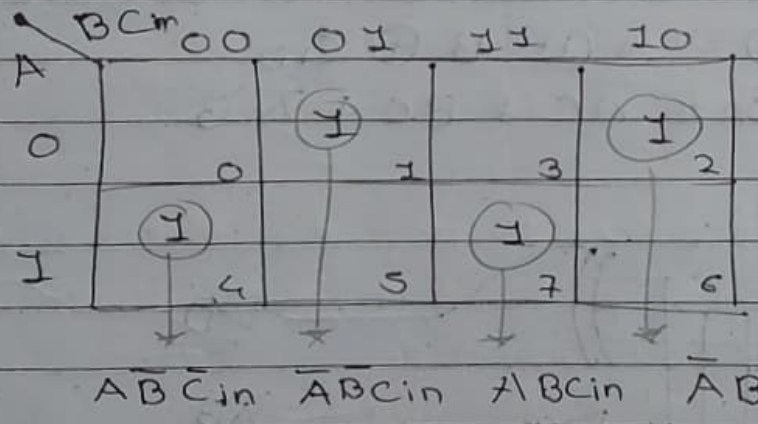
* Full Subtractor



Page No.
Date :

I/P				O/P	
A	B	C	Cin	D	Bo
0	0	1	0	0	0
0	0	0	1	1	1
0	1	1	0	1	1
0	1	0	1	0	1
1	0	1	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0
1	1	0	1	1	1

⇒ for Difference



$S = D = A\bar{B}\bar{C}in + \bar{A}\bar{B}Cin + ABCin + \bar{A}B\bar{C}in$

$= \bar{C}in\,(A\bar{B} + \bar{A}B) + Cin\,(\bar{A}\bar{B} + AB)$

Assume $A\bar{B} + \bar{A}B = x$

$= \bar{C}in\,x + Cin\,\bar{x}$

$= Cin \oplus x$

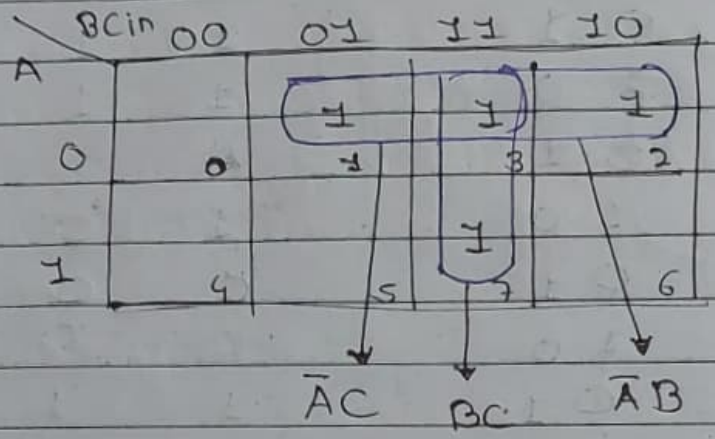
$= Cin \oplus (A\bar{B} + \bar{A}B)$

$= Cin \oplus A \oplus B$

Page No.
Date : / /

$\therefore D = A \oplus B \oplus C_{in}$

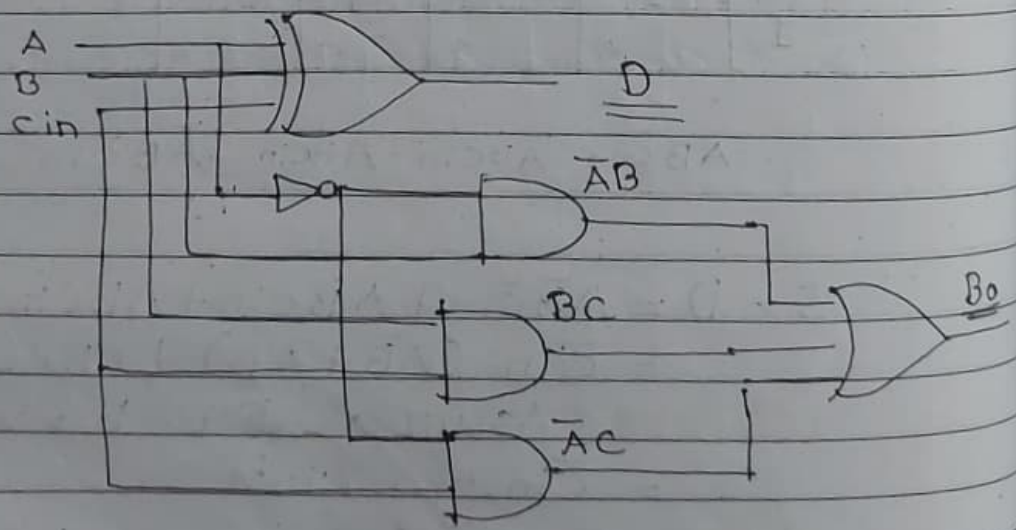
FOR BORROW



$B_0 = \bar{A}C + BC + \bar{A}B$

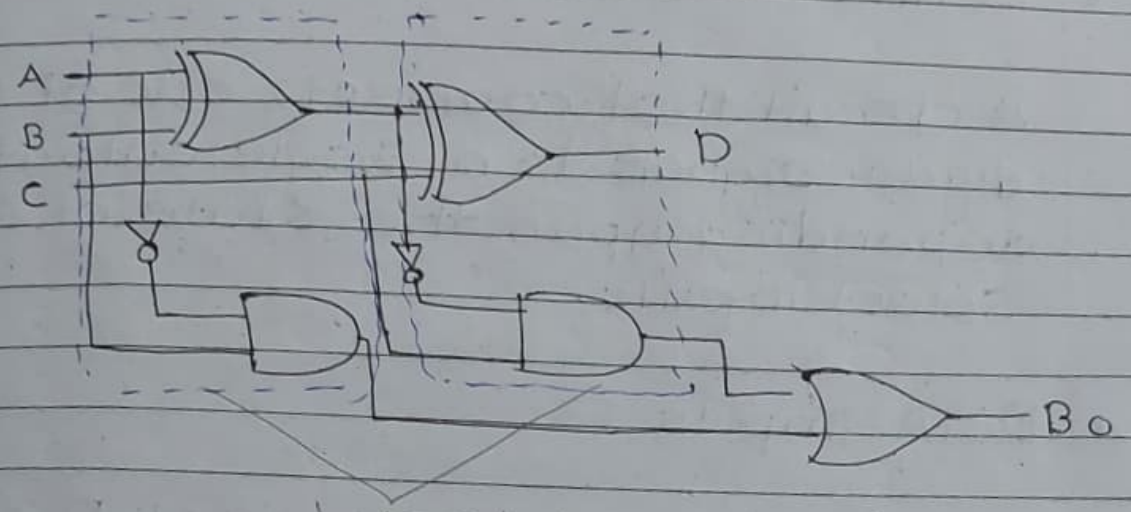
$\therefore D = A \oplus B \oplus C_{in}$

$B_0 = \bar{A}C + BC + \bar{A}B$



Page No.
Date : / /

- Realisation of full Subtractor using two half Subtractor



Page No.
Date : / /

inp

* Multiplexer (MUX)

- Defination of Multiplexer :-

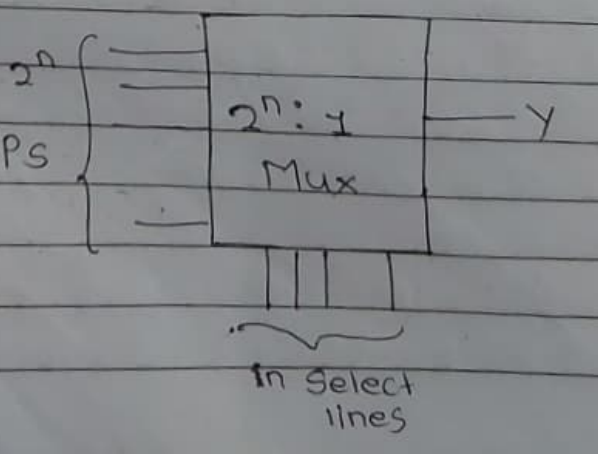
A circuit that connects one of several digital signals to a single output depending upon the state of several select inputs.

- DATA Inputs :-

The multiplexer inputs that feed a digital signal to the output when selected. (maximum of inputs is 2^n)

- Select Inputs :- (Select lines)

The multiplexer inputs that selects the digital inputs. (maximum n select lines)

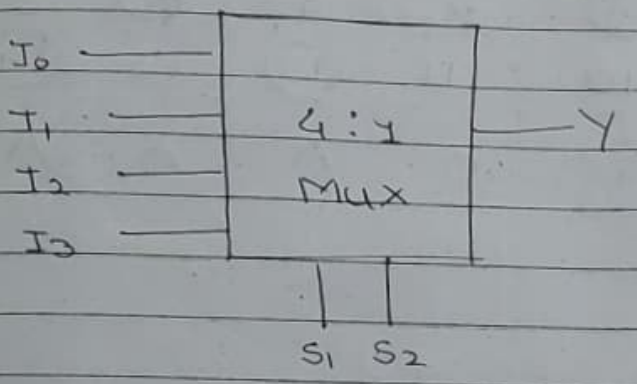


Page No.
Date : / /

e.g Put n=2

i/p = $2^n = 2^2 = 4$

n Select lines = 2



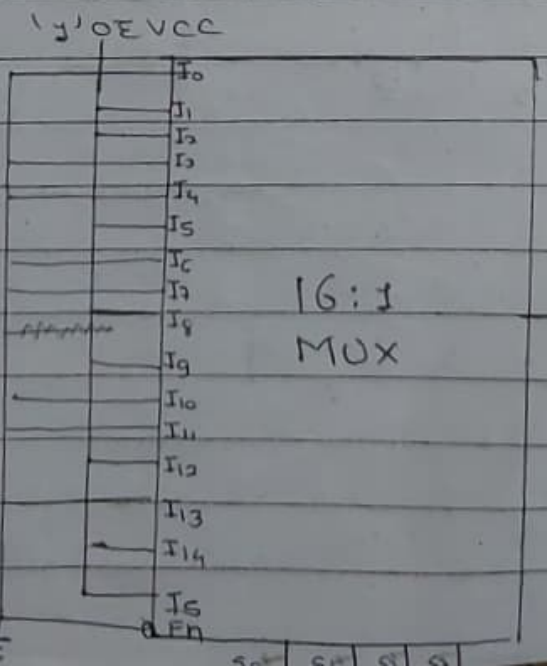
Select lines		O/P
S_1	S_2	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

- Implement the following Boolean expression using i) 16:1 Mux
  2) ~~to~~ 8:1 Mux.

$F = \Sigma m (1, 2, 5, 8, 9, 12, 14, 15)$

Ans:-

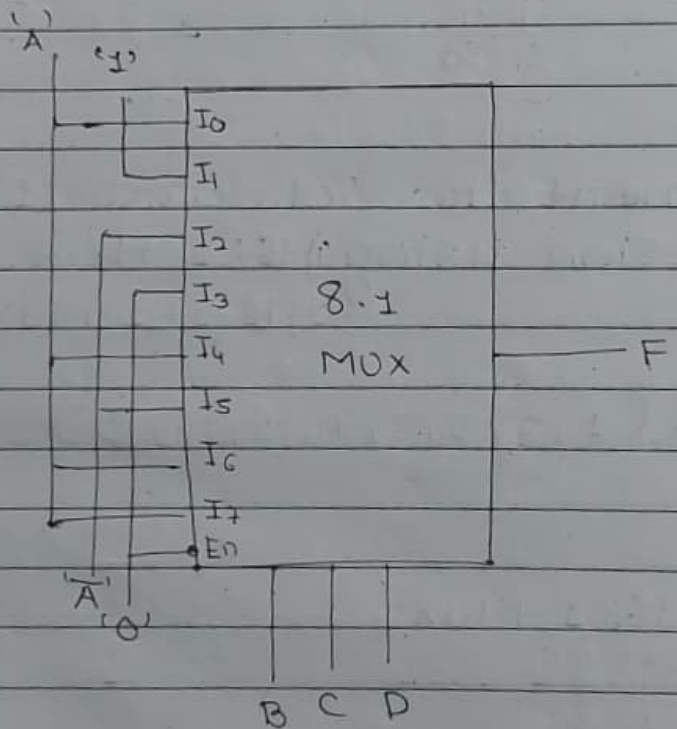
i) for 16:1 Mux.



Page No.
Date : / /

ii] for 8 : 1 MUX

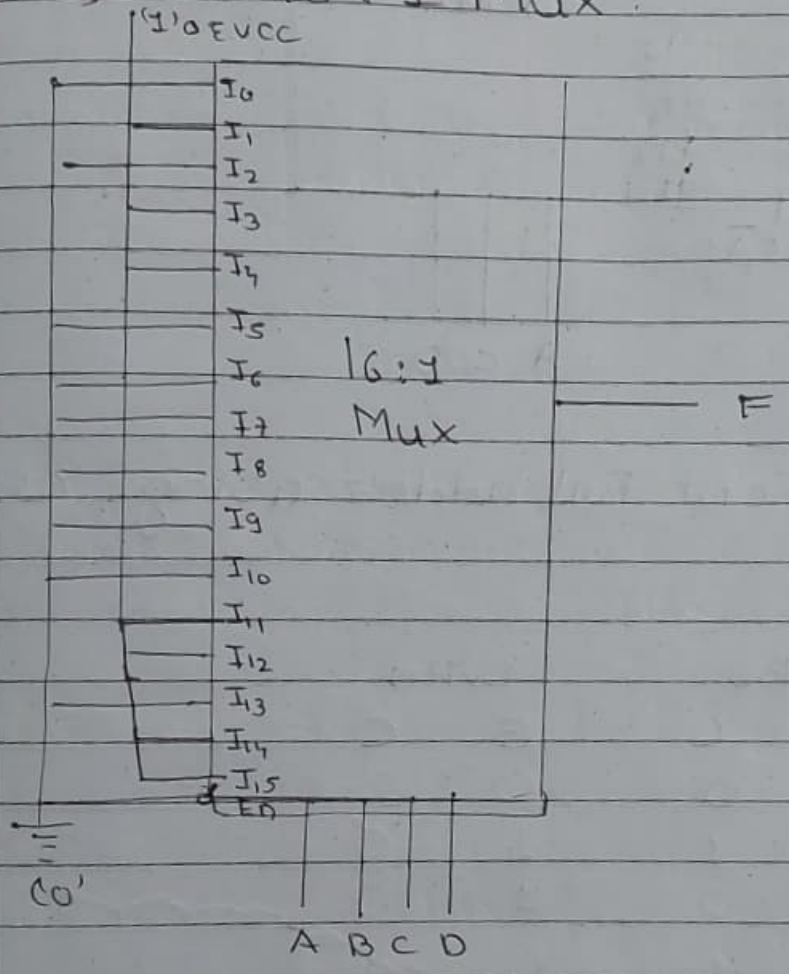
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	(1)	(2)	3	4	(5)	6	7
A	(8)	(9)	10	11	(12)	13	(14)	(15)
	A	1	$\bar{A}$	0	A	$\bar{A}$	A	A



Page No.
Date : / /

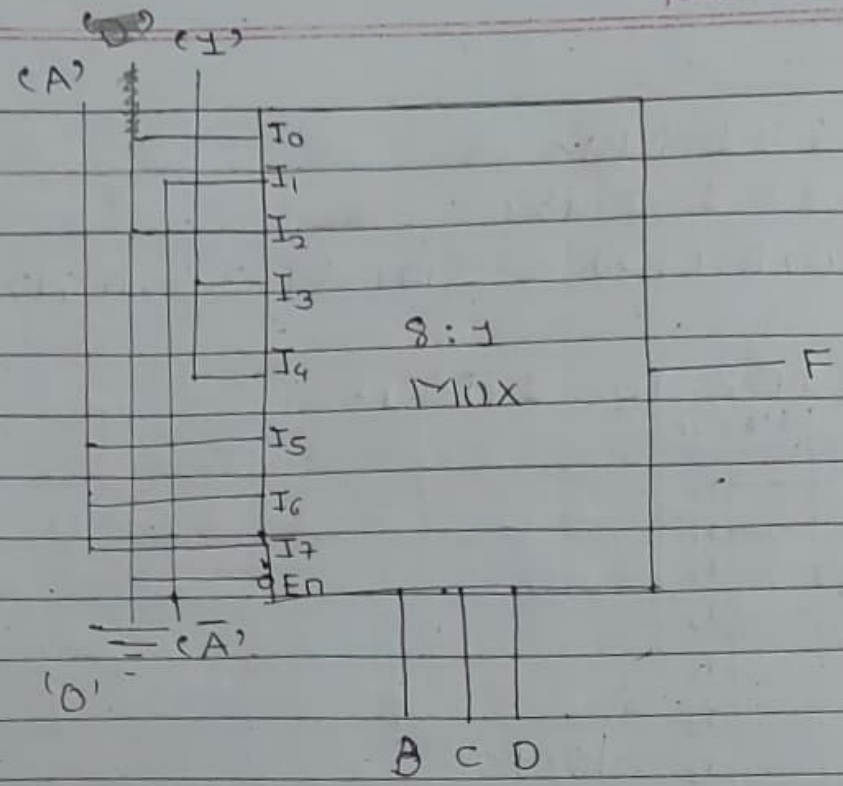
Q. i) 16 : 1 Mux.
ii) 8 : 1 Mux.
$F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$

soln:- i) FOR 16 : 1 MUX.



ii) FOR 8 : 1 MUX.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	(1)	2	(3)	(4)	5	6	7
A	8	9	10	(11)	(12)	(13)	(14)	(15)
	0	$\bar{A}$	0	1	1	A	A	A

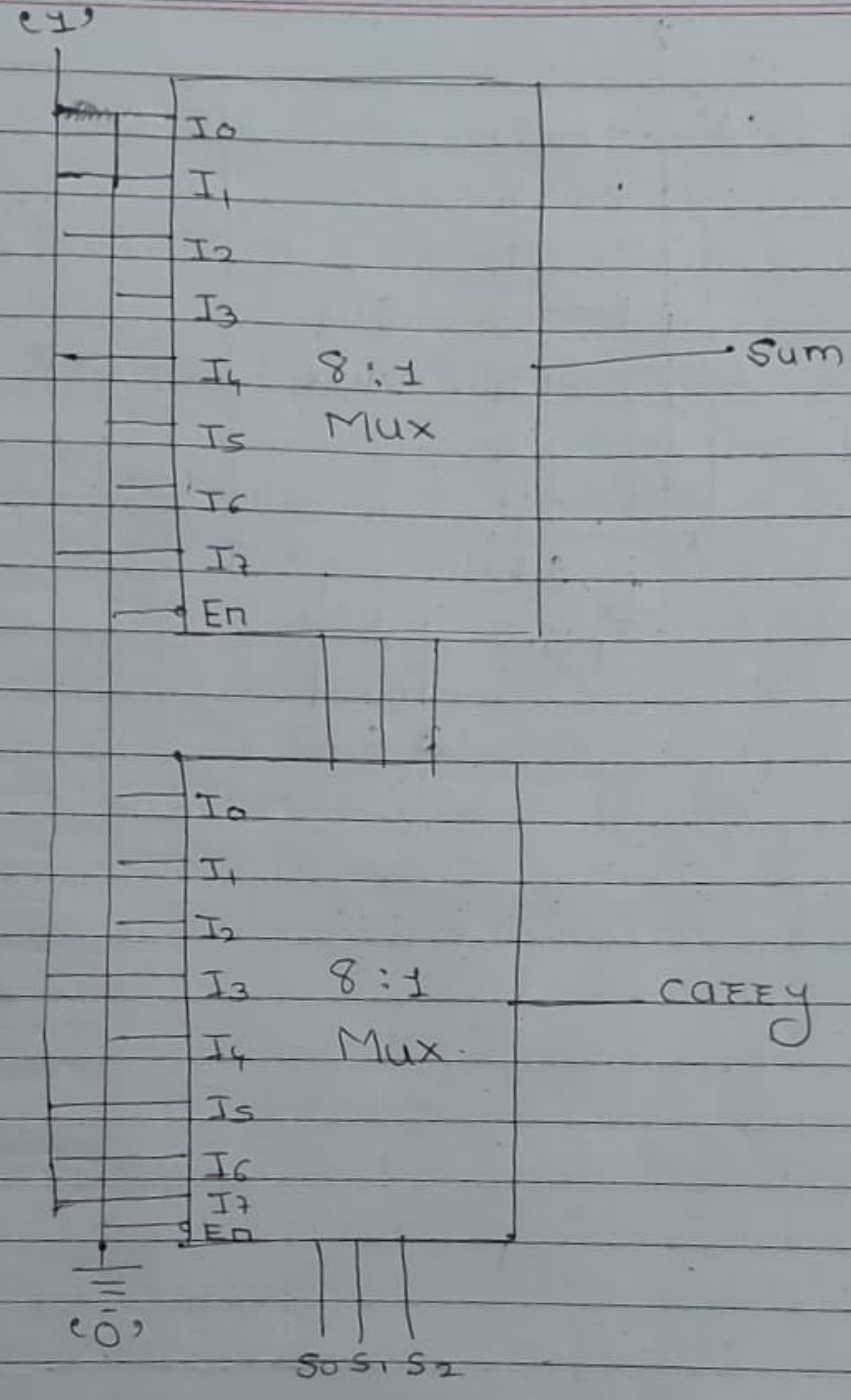


Q. Implement full adder using 8:1 Mux

I/Ps			O/Ps	
A	B	C	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \Sigma m(1,2,4,7)$

$C = \Sigma m(3,5,6,7)$

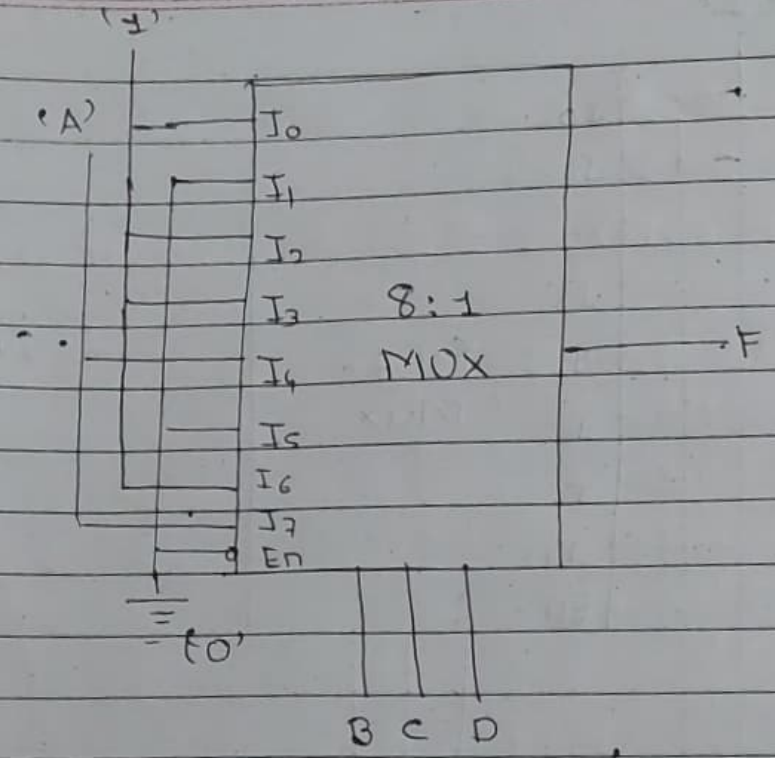


Q. $F(A,B,C,D) = \Sigma m(0,2,6,10,11,12,15) + d(3,8,14)$.

i) 8 : 1 MUX.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	(0)	1	(2)	(3)	4	5	(6)	7
A	(8)	9	(10)	(11)	(12)	13	(14)	(15)
	1	0	1	1	A	0	1	A

Page No.
Date : / /



Page No.
Date : / /

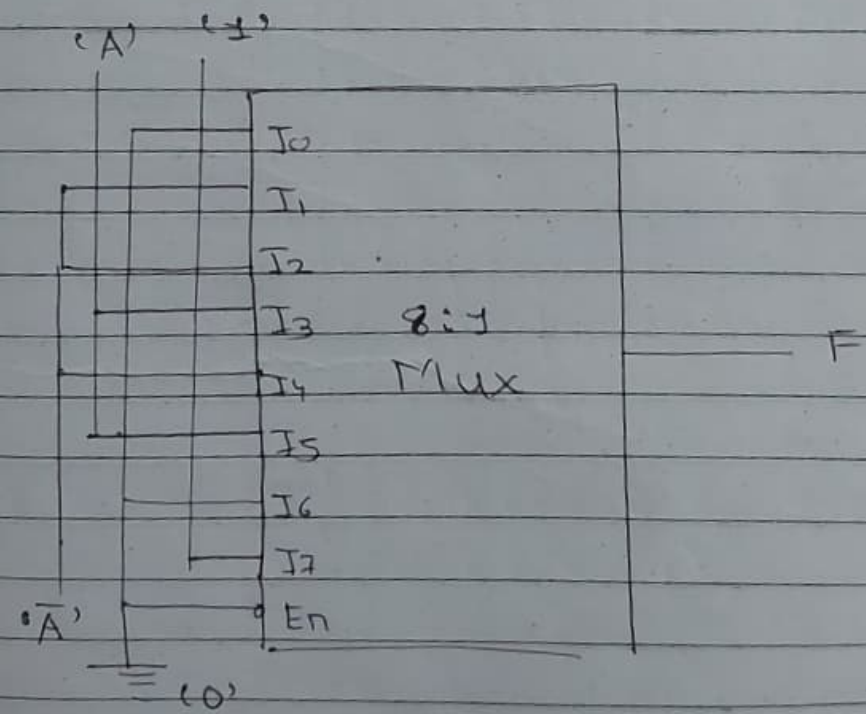
Q. $F(A,B,C,D) = \Pi M(0,3,5,6,8,9,10,12,14)$.

i) 8:1 MUX.

$\Rightarrow F(A,B,C,D) = \Sigma M(1,2,4,7,11,13,15)$

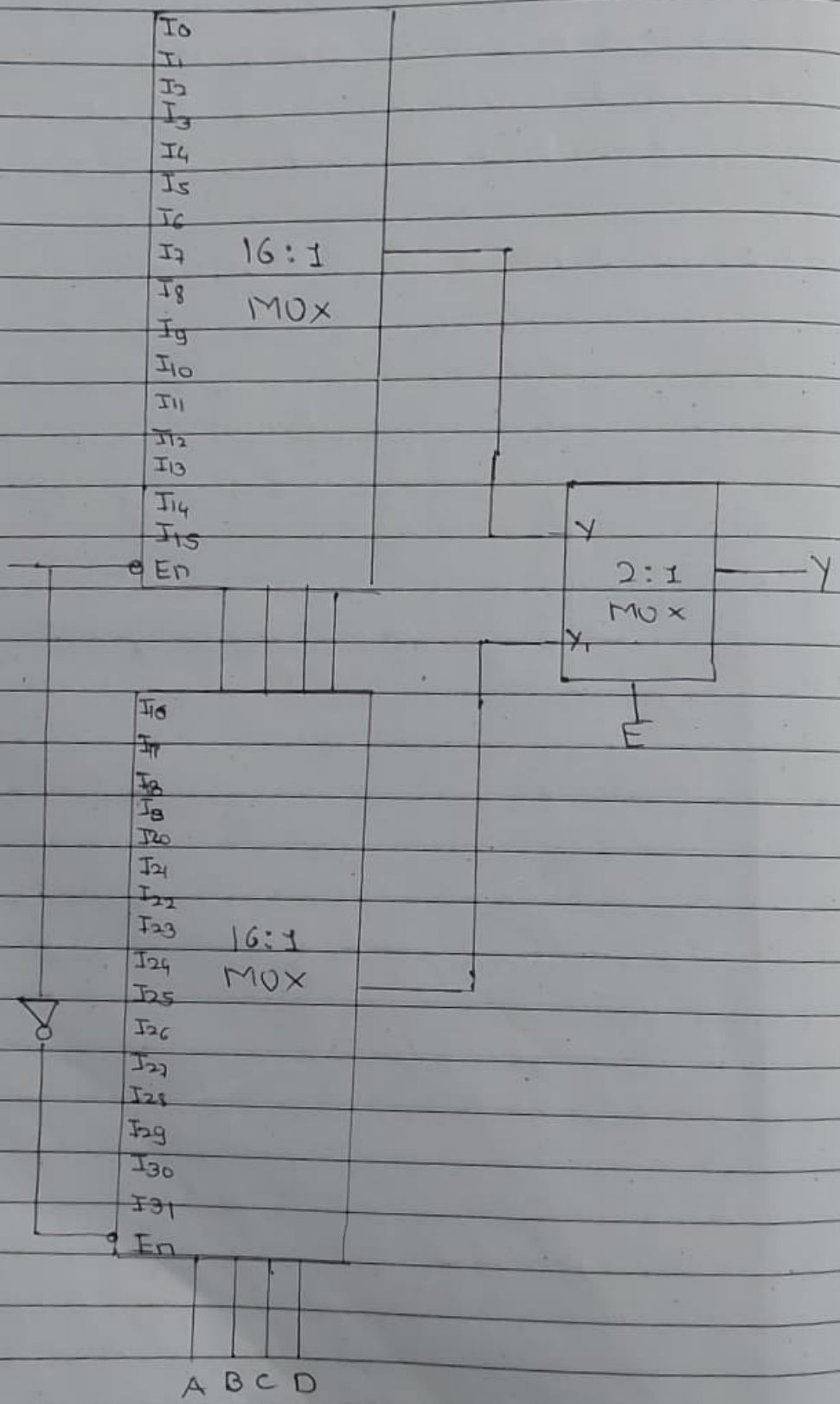
	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
A	(0)	(1)	(2)	(3)	(4)	(5)	(6)	7
$\bar{A}$	(8)	(9)	(10)	11	(12)	13	(14)	15

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
$\bar{A}$	0	(1)	(2)	3	(4)	5	6	(7)
$\bar{A}$	8	9	10	(11)	12	(13)	14	(15)
	0	$\bar{A}$	$\bar{A}$	$\bar{A}$	$\bar{A}$	$\bar{A}$	0	1



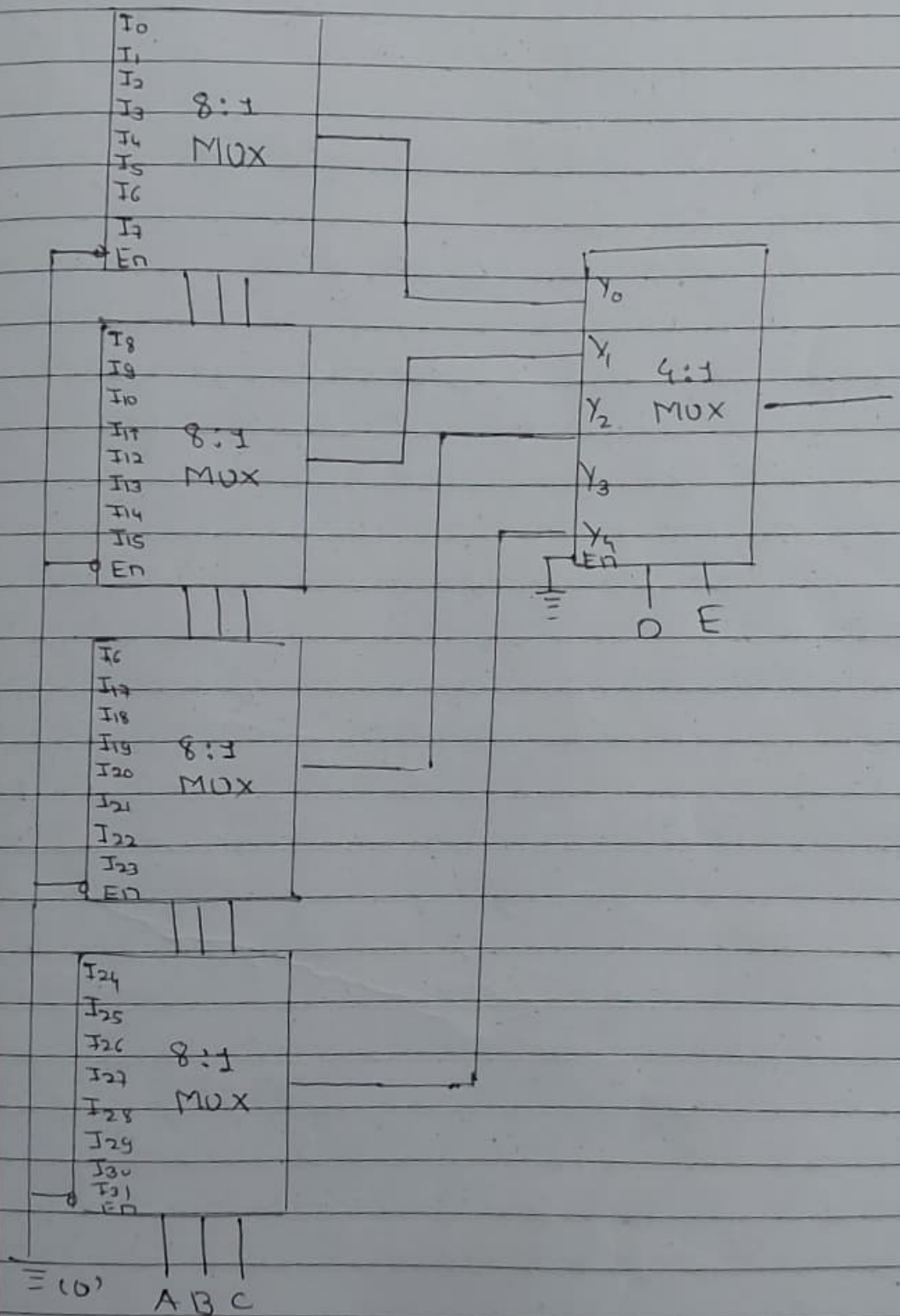
Page No.
Date : / /

Ans:- 2] 16 : 1 MUX & 2 : 1 MUX



Page No.
Date : / /

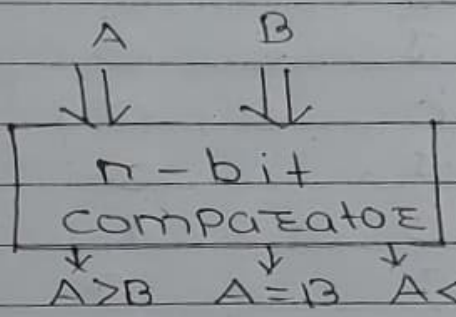
Ans: 3) 8:1 MUX and 4:1 MUX



Page No.
Date : / /

Comparator

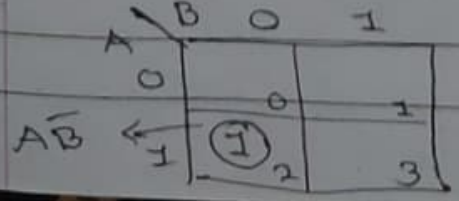
A comparator is the special combinational circuit design to compared the relative magnitude of two binary numbers
The fig shows the block diagram of n bit comparator that recives n bits numbers A and B as inputs and outputs are A>B A=B and A<B



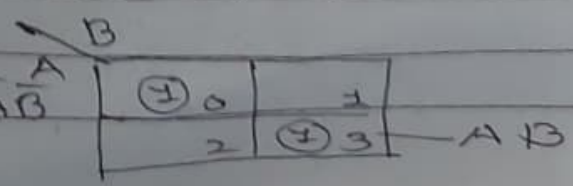
Q. Design one bit comparator

I/PS		O/PS		
A	B	A>B	A=B	A<B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

for A>B



for A=B

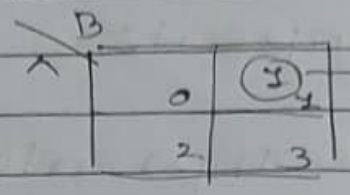


Page No.
Date : / /

$= \bar{A}\bar{B} + AB$

$= A \odot B$

for $A < B$

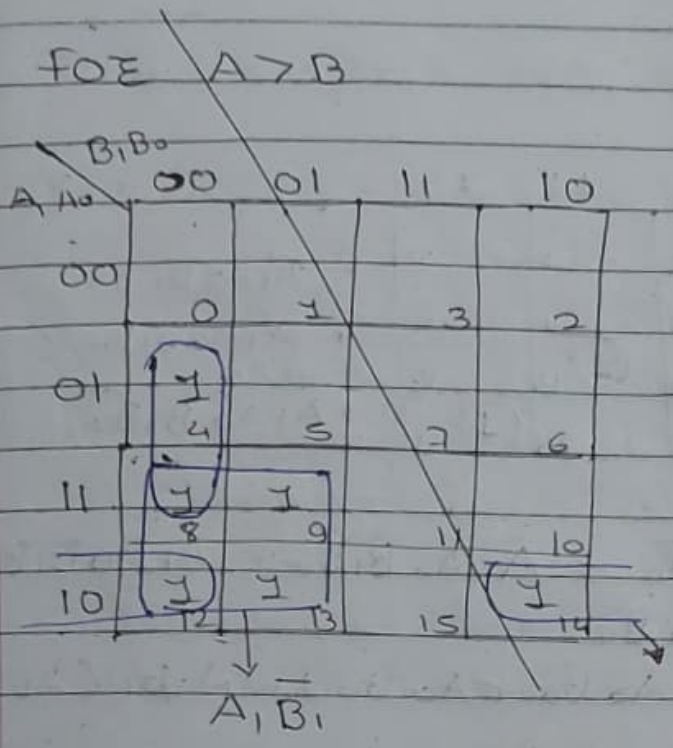


Q. Design two bit comparator

A_1	A_0	B_1	B_0	$A > B$	$A = B$	$A < B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

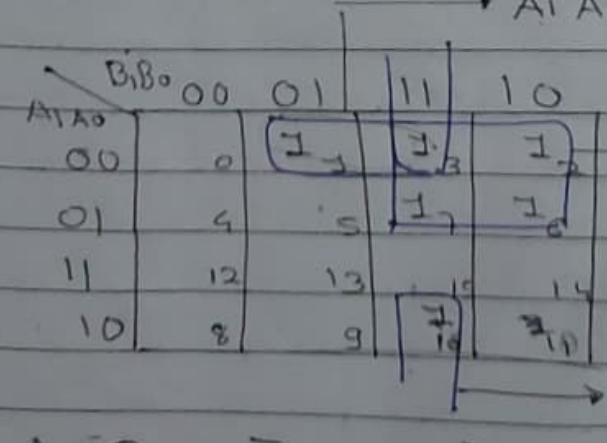
Page No.
Date : / /

FOR A > B



FOR A > B

FOR A < B



$A<B = \overline{A_1}B_1 + \overline{A_0}B_1B_0 + \overline{A_1}\,\overline{A_0}B_0$

Page No.
Date : / /

for $A = B$

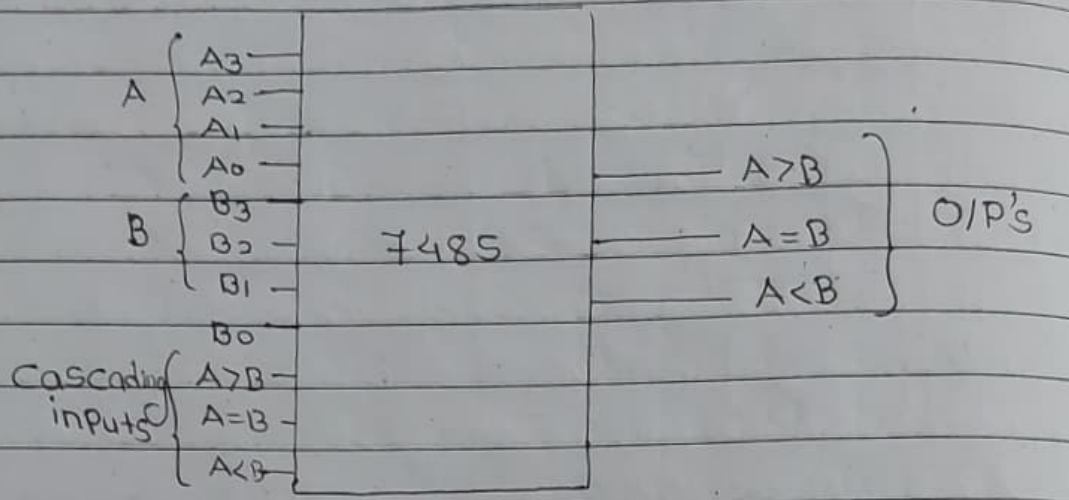
A_1A_0 \ B_1B_0	00	01	11	10	
00	(1) 0	1	3	2	→ $\bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0$
01	4	(1) 5	7	6	→ $\bar{A}_1 A_0 \bar{B}_1 B_0$
11	11	12	(1) 14	13	→ $A_1 A_0 B_1 B_0$
10	7	8	10	(1) 9	→ $A_1 \bar{A}_0 B_1 \bar{B}_0$

$$Y = \bar{A}_1 A_0 B_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$$

$$= \bar{A}_1 B_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0) + A_1 B_1 (A_0$$

Page No.
Date : / /

Q. Design four Bit comparator



I/P's	Cas I/P's			O/P's		
A, B	A>B	A=B	A<B	A>B	A=B	A<B
A>B	x	x	x	1	0	0
A=B	1	0	0	1	0	0
	0	1	0	0	1	0
	0	0	1	0	0	1
A<B	x	x	x	0	0	1

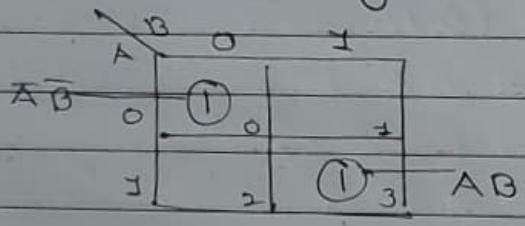
Page No.
Date : / /

- Parity checker CKT :-
- Design a circuit to check the parity of two incoming two bits words using logic gates

⇒

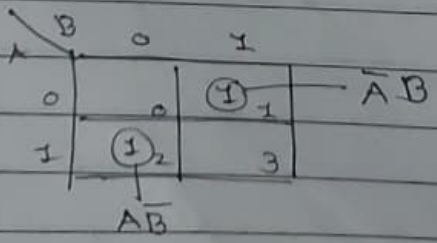
I/P's		O/P's	
A	B	ΣE	ΣO
0	0	1	0
0	1	0	1
1	0	0	1
1	1	1	0

for even Parity :-

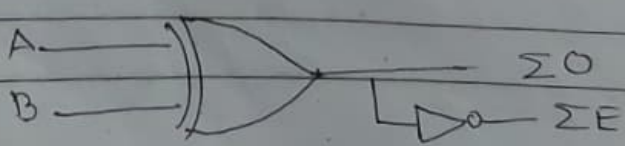


$$Y = \bar{A}\bar{B} + AB$$
$$= A \odot B = \overline{A \oplus B}$$

for odd parity :-



$$Y = \bar{A}B + A\bar{B} = A \oplus B$$

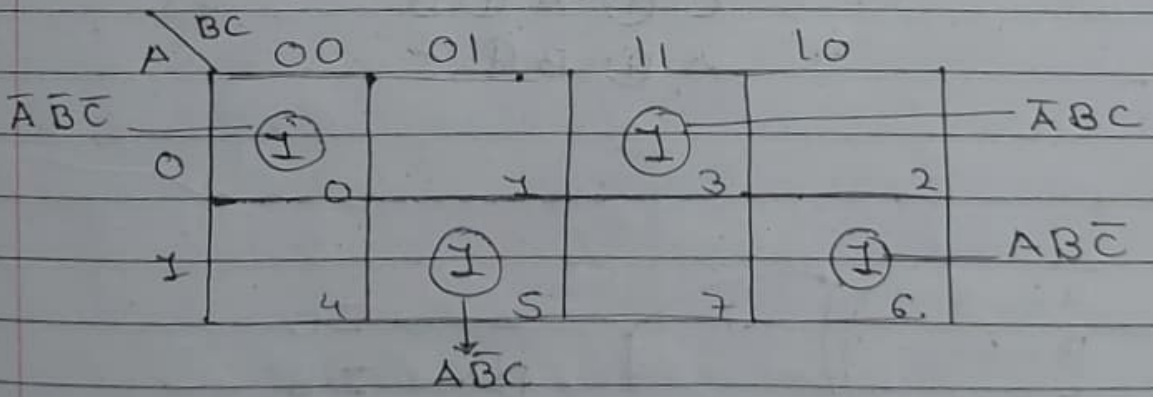


Page No.
Date : / /

Q. Design a logic ckt to check the odd even parity for three input bits

I/P's			O/P's	
A	B	C	ΣE	ΣO
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

for even parity.



$Y = \bar{A}\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + AB\bar{C}$

$= \bar{B}(\bar{A}\bar{C} + AC) + B(\bar{A}C + A\bar{C})$

$= \bar{B}.(A \odot C) + B(A \oplus B)$

$= \bar{B}(\overline{A \oplus C}) + B(A \oplus C)$

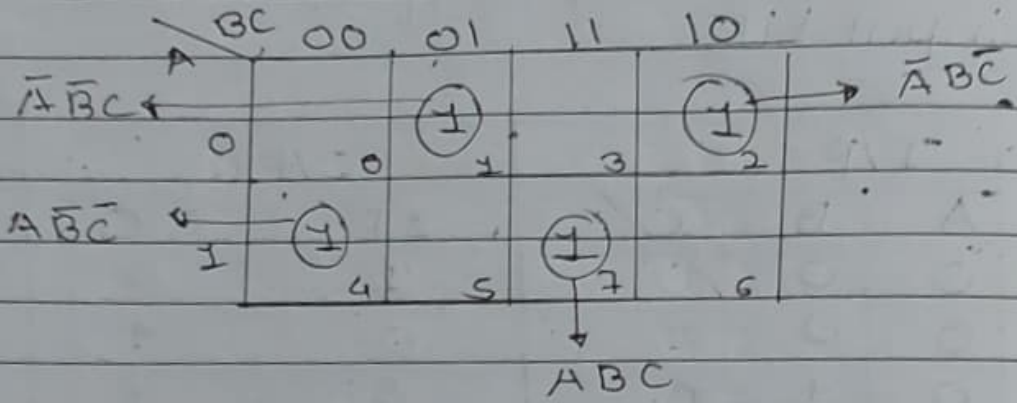
$= \bar{B}\bar{X} + BX$

$= B \odot X \quad = \overline{B \oplus X}$

$= B \odot A \oplus C \quad = \overline{B \oplus A \oplus C} = A \odot B \odot C$

Page No.
Date : / /

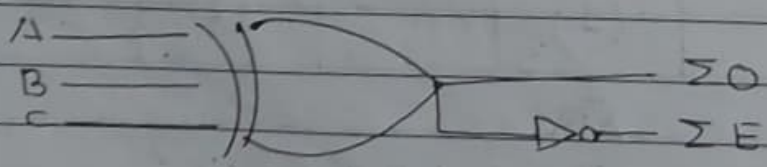
For odd parity :-



$$Y = A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + \bar{A}B\bar{C}$$
$$= \bar{C}(A\bar{B} + \bar{A}B) + C(\bar{A}\bar{B} + AB)$$
$$= \bar{C}(A \oplus B) + C(A \odot B)$$
$$= \bar{C}(A \oplus B) + C(\overline{A \oplus B})$$

Let $A \oplus B = x$.

$$= \bar{C}\bar{x} + C\bar{x}$$
$$= C \oplus x$$
$$= C \oplus A \oplus B$$
$$= A \oplus B \oplus C.$$



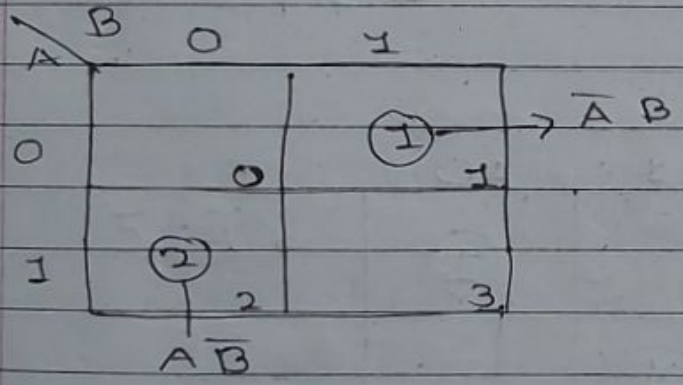
Page No.
Date : / /

: Parity generator

Q. Design two bit even parity generator using logic gates

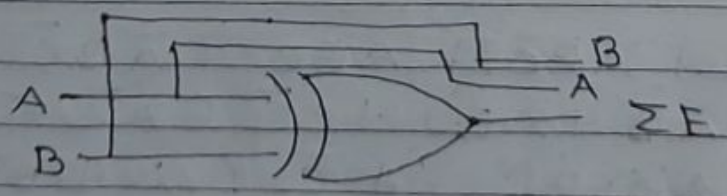
Soln:

I/P's		O/P
A	B	ΣE
0	0	0
0	1	1
1	0	1
1	1	0



$= \bar{A}B + A\bar{B}$

$= A \oplus B$

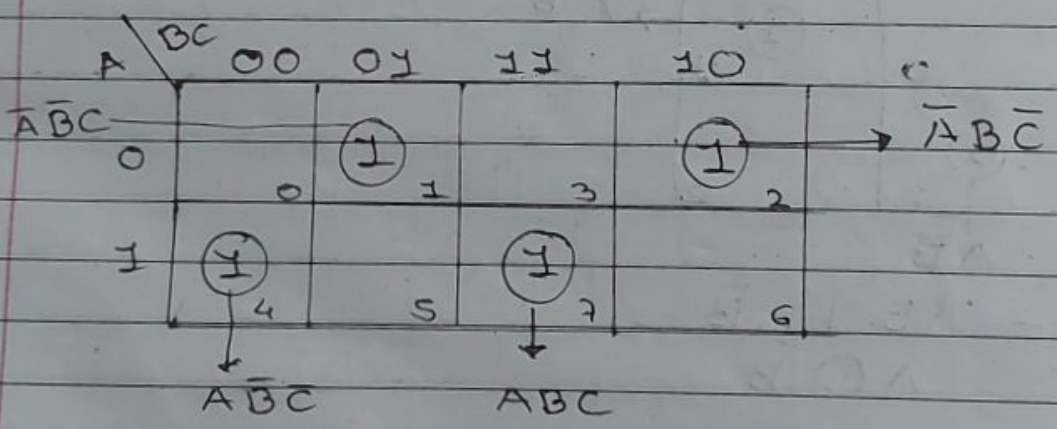


Page No.
Date : / /

Q.5 Design three bit even parity generator using logic gates

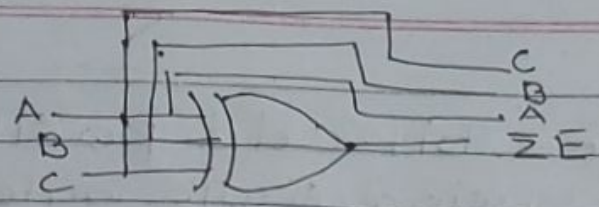
Soln:-

I/P's			O/P's
A	B	C	ΣE
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



$$= \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC + \bar{A}B\bar{C}$$
$$= C(\bar{A}\bar{B} + AB) + \bar{C}(A\bar{B} + \bar{A}B)$$
$$= C(A \odot B) + \bar{C}(A \oplus B)$$
$$= C\bar{X} + \bar{C}X$$
$$= C \oplus X$$
$$= C \oplus A \oplus B$$
$$= A \oplus B \oplus C$$

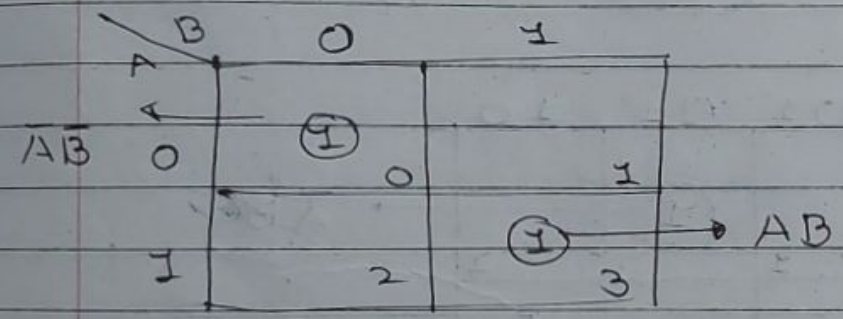
Page No.
Date : / /



Q. Design two bit odd parity generator using logic gates.

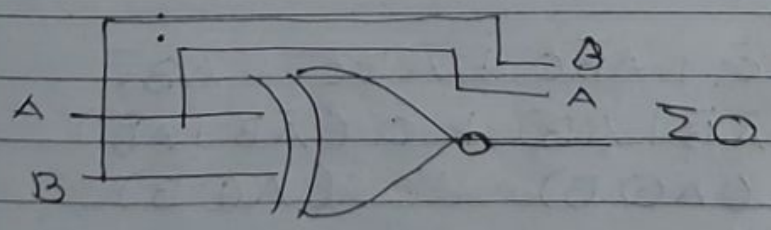
Soln:-

I/P's		O/P's
A	B	ΣO
0	0	1
0	1	0
1	0	0
1	1	1



$= \bar{A}\bar{B} + AB$

$= A \odot B$

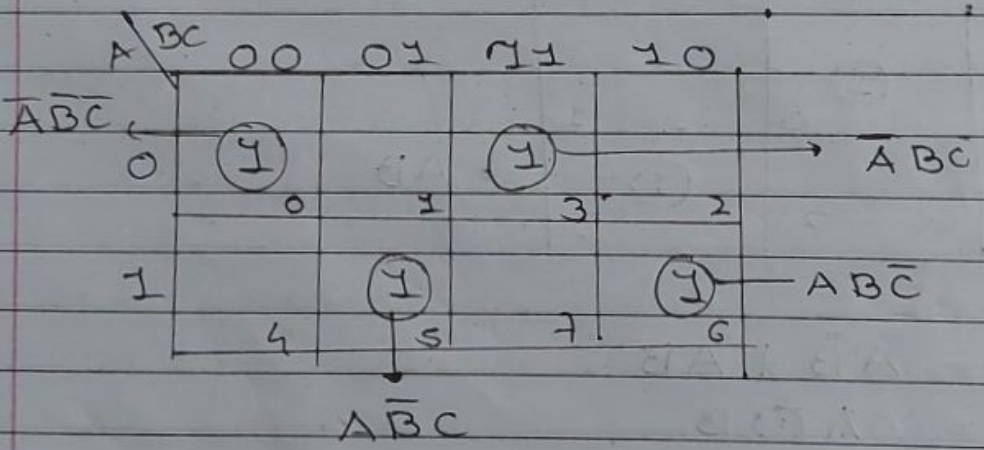


Page No.
Date : / /

Q. Design three bit odd parity generator using logic gates

Soln:-

I/P's			O/P's
A	B	C	ΣO
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0



$= \bar{A}\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + AB\bar{C}$

$= \bar{C}(\bar{A}\bar{B} + AB) + C(\bar{A}B + A\bar{B})$

$= \bar{C}(A \odot B) + C(A \oplus B)$

Let $x = A \oplus B$

$= \bar{C}\bar{x} + Cx$

$= C \odot x$

$= C \odot (A \oplus B)$

Page No.
Date : / /

$$= \overline{C}\,(\overline{A \oplus B}) + C\,(A \oplus B)$$

$$\Rightarrow \text{Let } A \oplus B = x$$

$$\therefore = \overline{C}\,\overline{x} + Cx$$

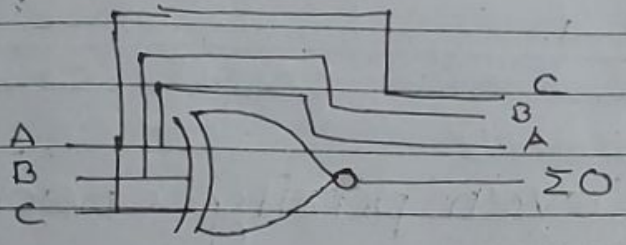
$$= C \odot x$$

$$= \overline{C \oplus x}$$

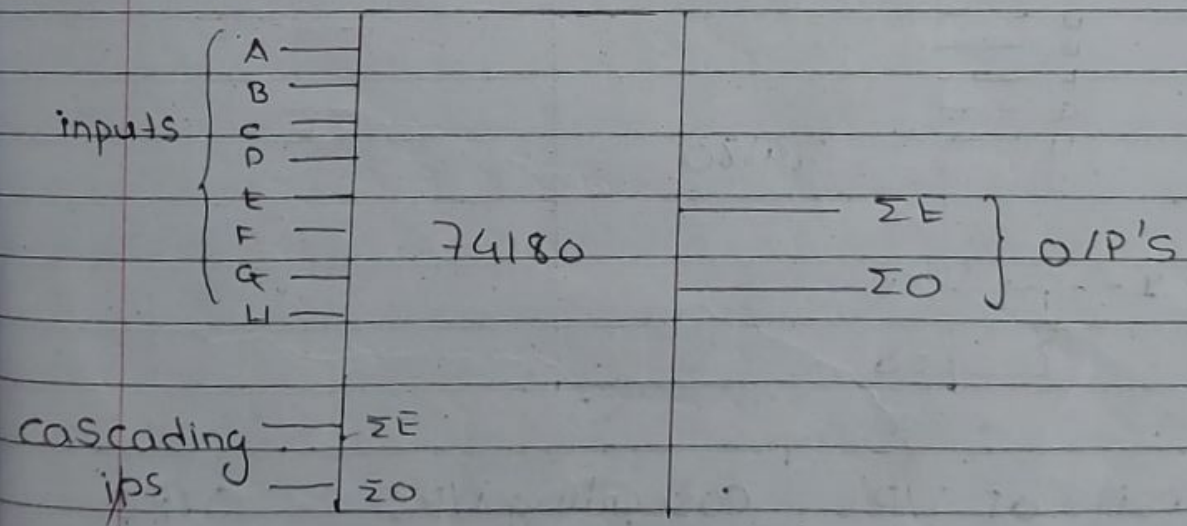
$$= \overline{C \oplus A \oplus B}$$

$$= C \odot A \odot B$$

$$= A \odot B \odot C$$



- Design Using 74180

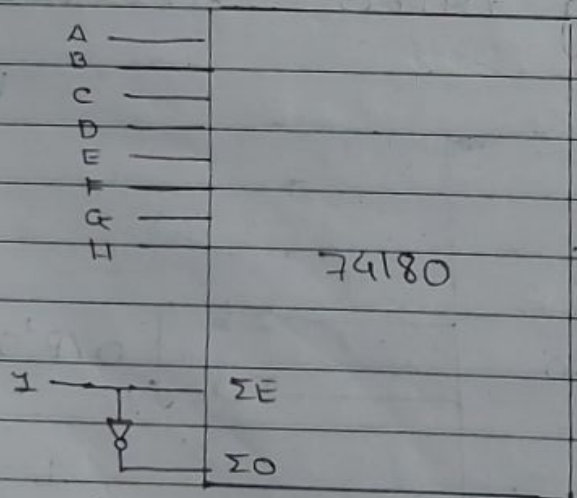


even + even = even
odd + odd = even
even + odd = odd
odd + even = odd

Page No.
Date : / /

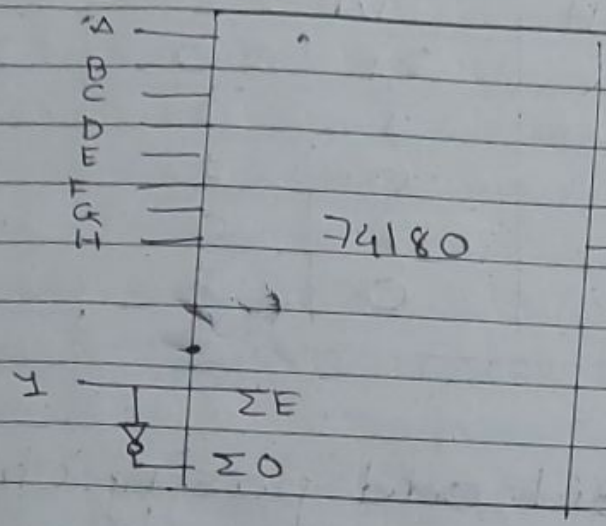
parity of i/p's A through H	cascading i/p's		o/p's	
	ΣE	ΣO	ΣE	ΣO
Even	1	0	1	0
Even	0	1	0	1
ODD	1	0	0	1
ODD	0	1	1	0

- Design 8 bit even parity checker using IC 74180



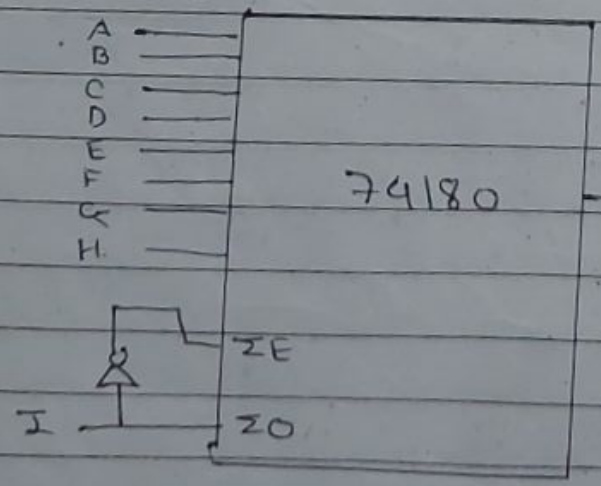
Parity of i/p's A through H	cascading i/p's		o/p's	
	ΣE	ΣO	ΣE	ΣO
Even	1	0	1	0
odd	1	0	0	1

Q. Design 8 bit odd parity checker



Parity of i/P's A through H	cascading i/p's		o/p's	
	ΣE	ΣO	ΣE	ΣO
Even	1	0	1	0
Odd	1	0	0	1

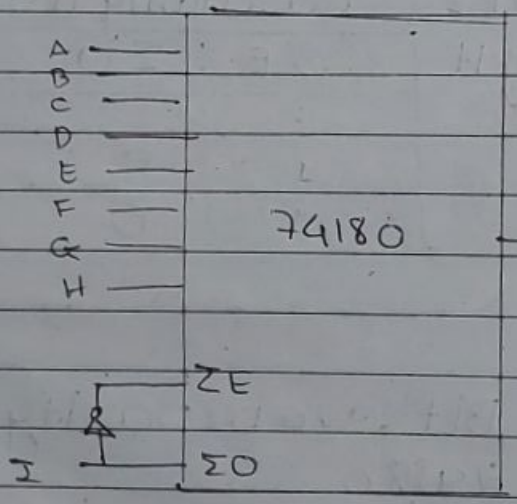
Q. Design 9-Bit even parity checker using IC 74180



Page No.
Date : / /

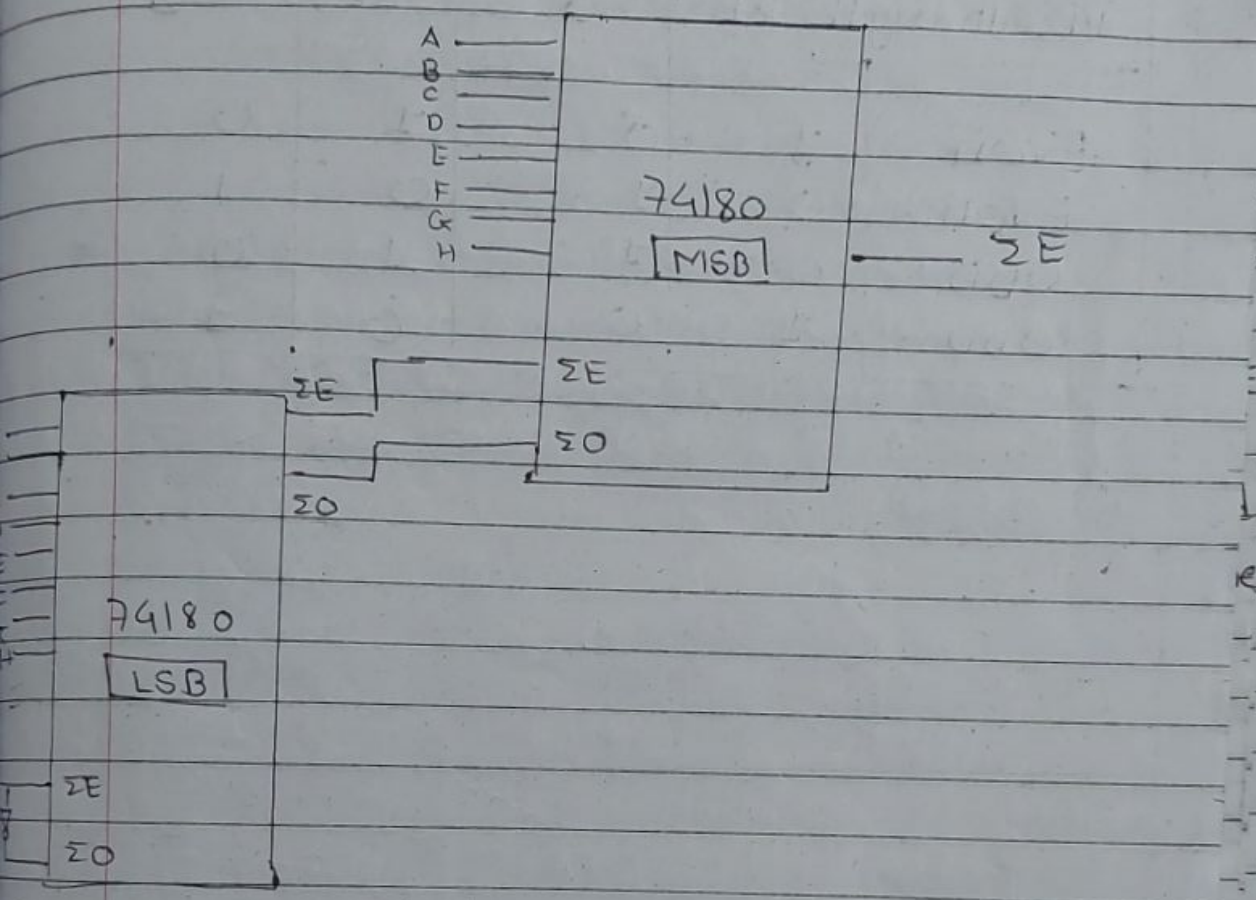
Parity of i/P's A through H	cascading i/P's		o/P's	
	ΣE	ΣO	ΣE	ΣO
Even	1	0	1	0
Even	0	1	0	1
ODD	1	0	0	1
ODD	0	1	1	0

Q. Design 9-Bit odd parity checker Using IC 74180



Page No.
Date : / /

Q. Design 16-Bit even parity checker.



- FOR LSB

Parity of i/P's A through H	cascading i/P's		O/PS	
	ΣE	ΣO	ΣE	ΣO
Even	1	0	1	0
Even Even	0	1	0	1
ODD	1	0	0	1
ODD ODD	0	1	1	0

Page No.
Date : / /

FOR MSB

Parity of i/p's Although	cascading i/p's		o/p's	
	ΣE	ΣO	ΣE	ΣO
Even	1	0	1	0
Even	0	1	0	1
ODD	0	1	1	0
ODD	1	0	0	1

Page No.
Date : / /

• 4 bit Parallel Adder (Binary)

Comparison of Serial.

Sr. no	Parameter of comparesion	Parallel Adder	Serial Adder
1.	Clock pulse	Not Essential	Essential
2.	principle of operation	All the bits are added simultaneously	One pair of bits is added at a time
3.	Result is in	parallel form	Serial form
4.	Time taken to complete addtion	very short	long
5.	No. of components	less	more
6.	cost	less	more
7.	circuit complexicity	less	more

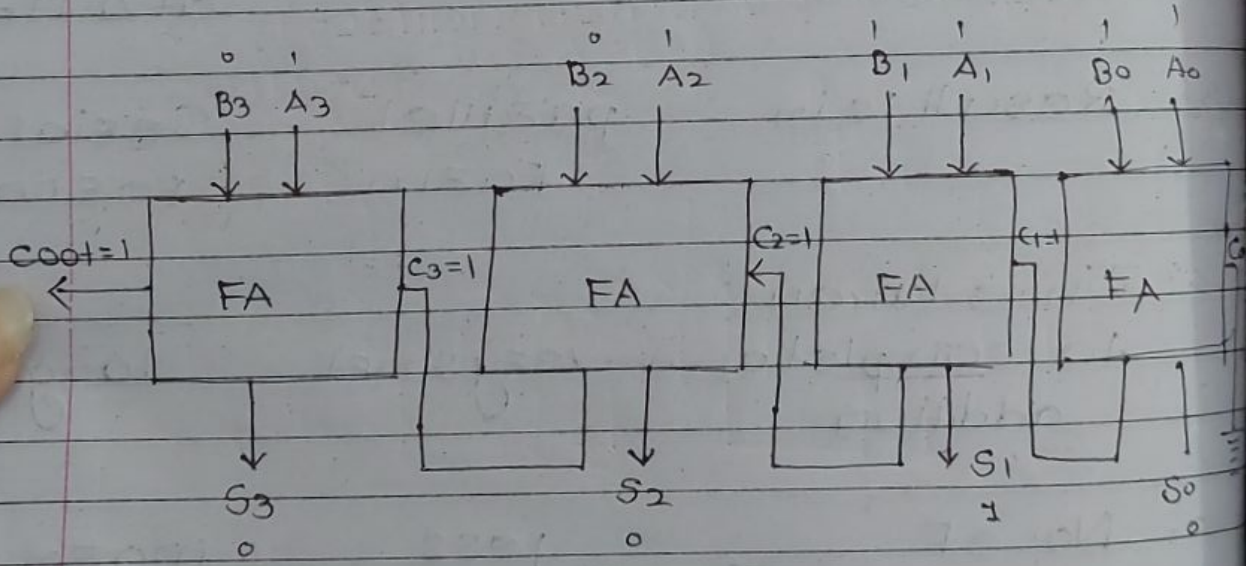
Page No.
Date : / /

Parallel Binary Adder

A circuit consisting of 'n' full adders that will add to 'n' bit nos. the output consist of 'n' sum bit & a carry bit

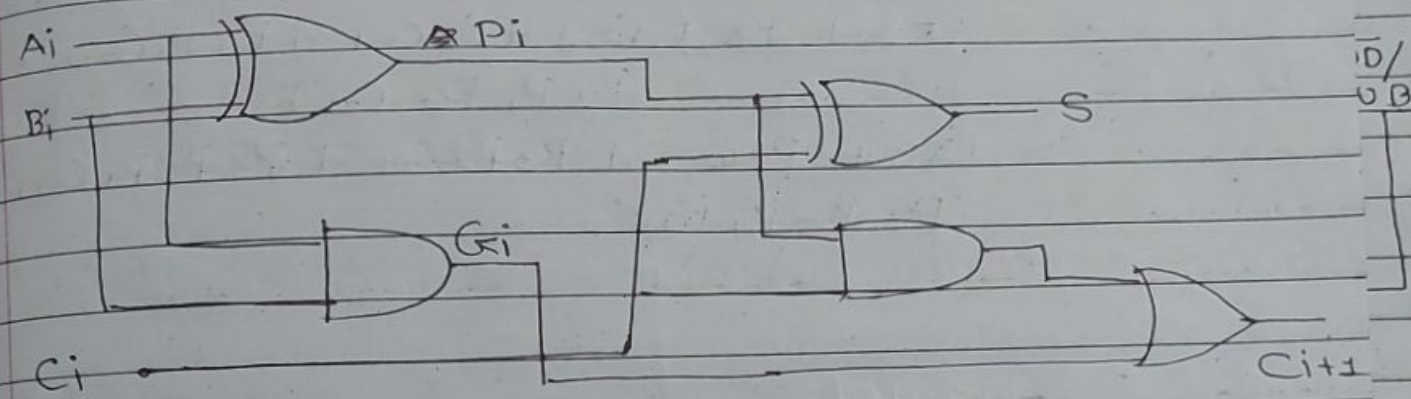
Cascade

To connect an output of device to input of another device often for the purpose of expanding the no. of bits available for particular function.



Page No.
Date : / /

Carry look ahead adder. (a bit)



$$C_{i+1} = A_i \oplus B_i + C$$

$$C_{i+1} = A_i \cdot B_i + (A_i \oplus B_i) C_i$$

$$P_i = A_i \oplus B_i \quad \& \quad G_i = A_i \cdot B_i$$

$$\therefore \boxed{C_{i+1} = G_i + (P_i) C_i}$$

if $i = 0$

$\therefore C_1 = G_0 + P_0 C_0$

if $i = 1$

$C_2 = G_1 + P_1 C_1$

$= G_1 + P_1 (G_0 + P_0 C_0)$

if $i = 2$

$C_3 = G_2 + P_2 C_2$

$= G_2 + P_2 (G_1 + P_1 (G_0 + P_0 C_0))$

$= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

Page No.
Date : / /

if i = 3

$C_4 = G_3 + P_3 C_3$

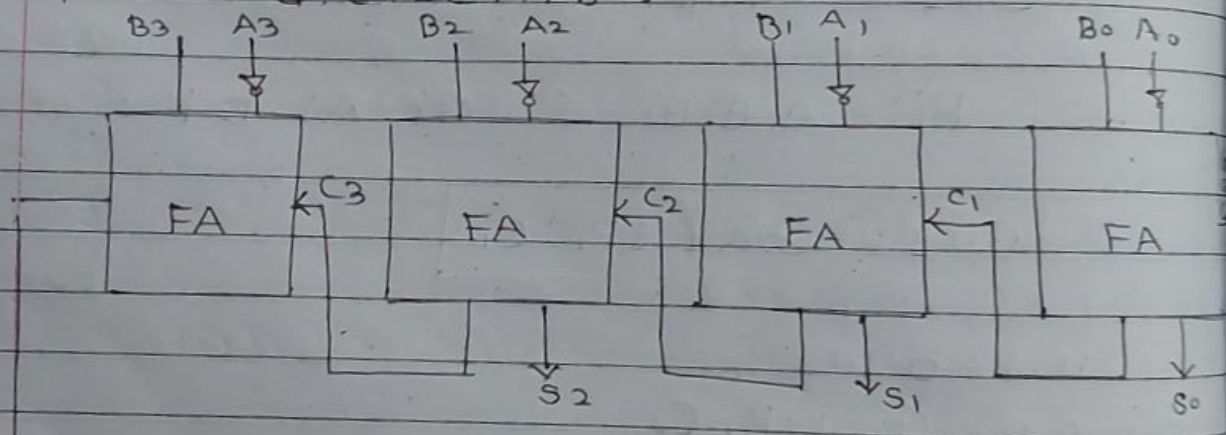
$= G_3 + P_3 (G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0)$

$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

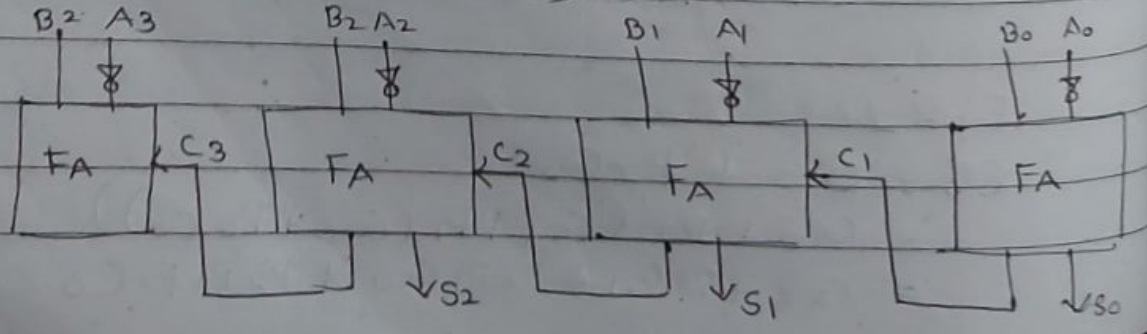
Parallel

- 4-bit Substractor (A>B)

Substraction using 1's complement method (for A>B)



Substraction using 2's complement method (for A>B)



Page No.
Date : / /

4 bit parallel Adder / Substractor