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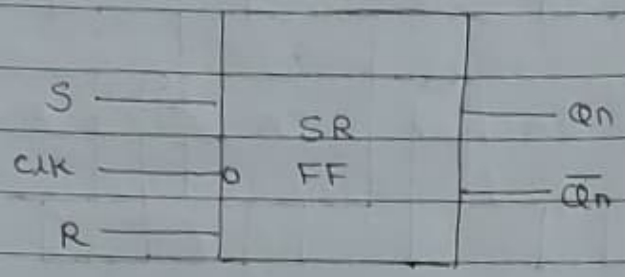
6. Sequential Circuit

- Flip flop (1 bit) Storage device 1-SR
No. of flip flop connected called Register

1. S-R Flip flop



- Truth Table

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	? (undefine)

- Excitation Table

S	R	Q_n	Q_{n+1}	
0	0	0	0	Hold state
0	0	1	1	
0	1	0	0	Reset state
0	1	1	0	
1	0	0	1	set state
1	0	1	1	
1	1	0	?	not define
1	1	1	?	

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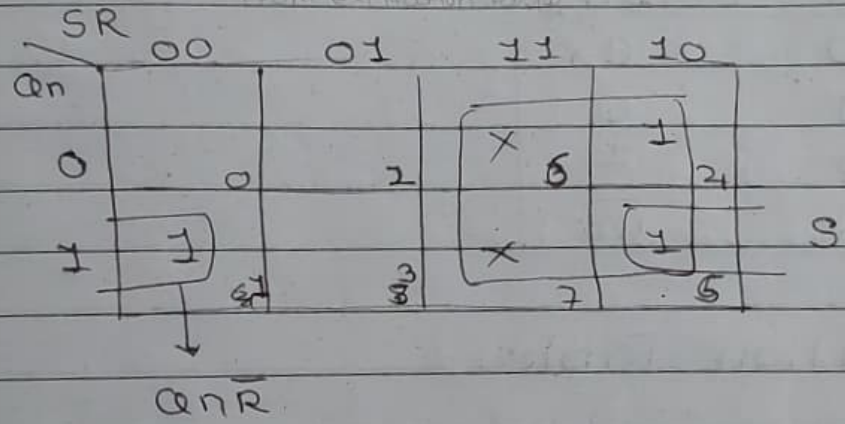
- Application Table. (for it is use conversion)

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	1	0

- Equation form :-

from excitation table



$$Q_{n+1} = S + Q_n\bar{R}$$

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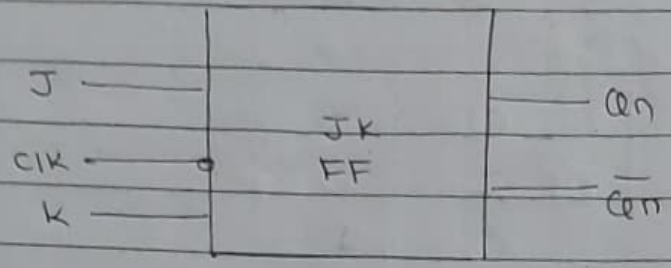
2. J.K Flip flop



Truth table

J	K	Qn+1
0	0	Qn
0	1	0
1	0	1
1	1	$\overline{Qn}$

Exicitation Table

J	K	Qn	Qn+1	
0	0	0	0	Hold State
0	0	1	1	
0	1	0	0	Reset State
0	1	1	0	
1	0	0	1	Set State
1	0	1	1	
1	1	0	1	Toggling State
1	1	1	0	

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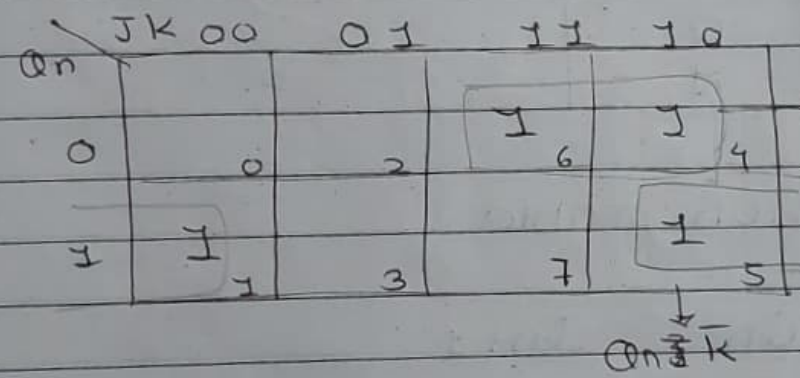
- Application Table

Qn	Qn+1	S J	R K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

- Equation form.



$$Q_{n+1} = J\bar{Q_n} + \bar{K}Q_n$$

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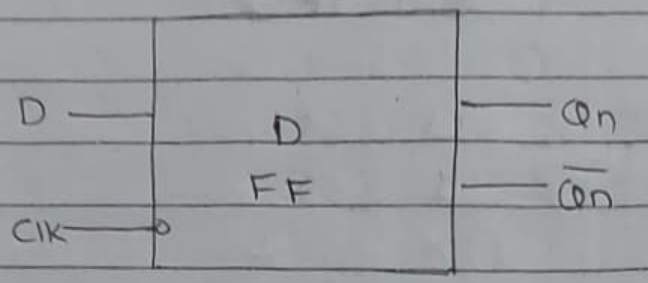
3. D Flip flop



- Truth table

D	Q_{n+1}
0	0
1	1

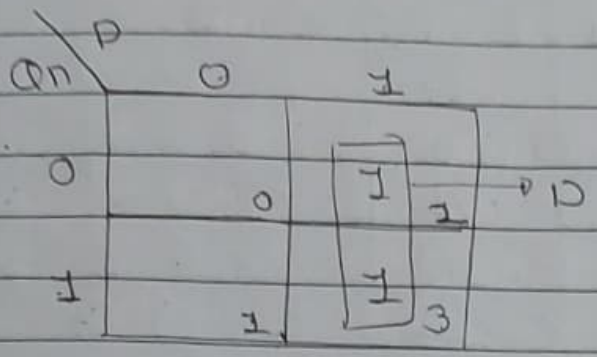
- Excitation Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

- Application Table

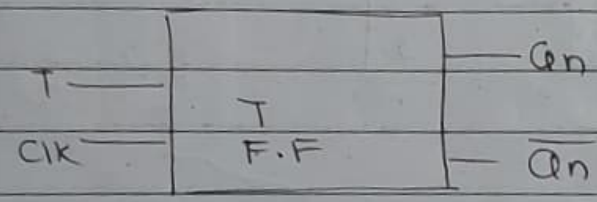
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

· Equation form



$$Q_{n+1} = D$$

4. T Flip Flop



Truth table

T	Q_{n+1}
0	Q_n
1	$\overline{Q_n}$

· Excitation Table.

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

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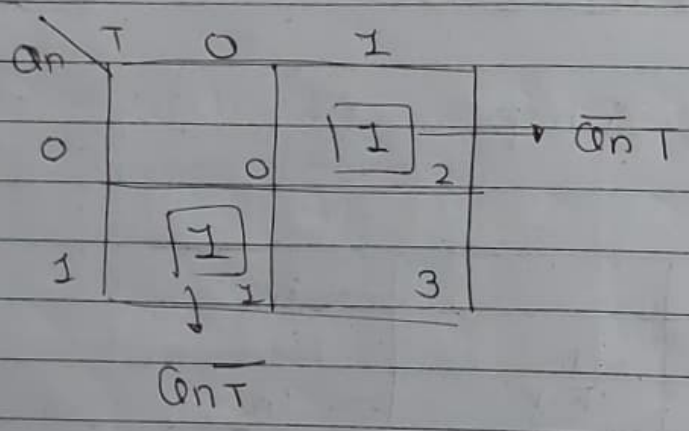
Application Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

- Equation form



$$Q_{n+1} = Q_n\bar{T} + \bar{Q_n}T$$

Q_n	Q_{n+1}	S	R	J	K	D	$\bar{S}$
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	0	1	x	1	0	1
1	1	x	0	x	0	1	0

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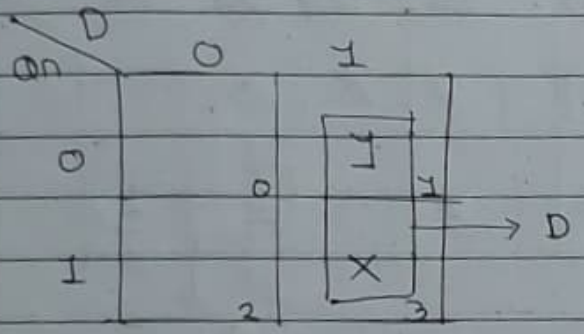
• Flip Flop conversion.

Q. Convert SR Flip flop into D Flip flop.

⇒

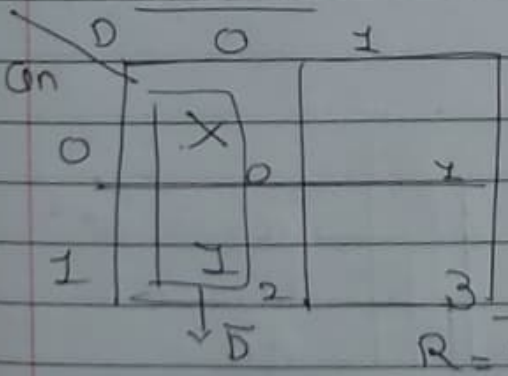
Q_n	Q_{n+1}	D	S	R
0	0	0	0	X
0	1	1	1	0
1	0	0	0	1
1	1	1	X	0

for S



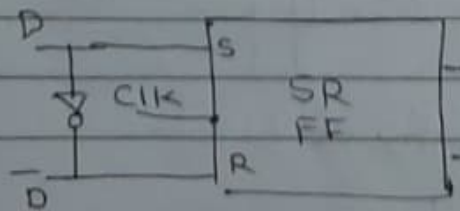
$S = D$

for R



$R = \bar{D}$

⇒



[D-Flip flop]

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Q.2 Convert SR Flip flop into JK flip flop

⇒

Q_n	Q_{n+1}	J	K	S	R
0	0	0	X	0	X
0	1	1	X	1	0
1	0	X	1	0	1
1	1	X	0	X	0

X = 0 or 1

For S

Q_n \ JK	00	01	11	10
0			1	1
1	X			X

$\bar{Q_n}J$

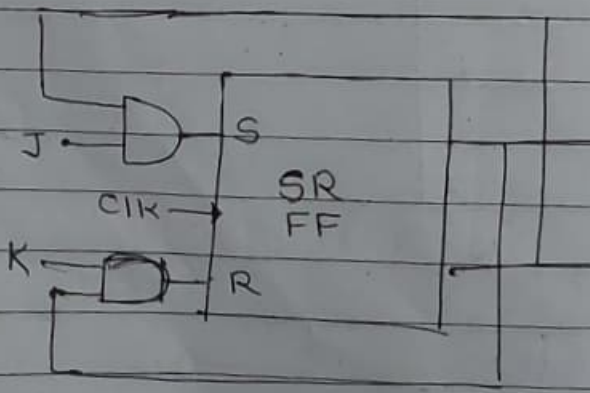
$S = \bar{Q_n}\,J$

For R

Q_n \ JK	00	01	11	10
0	X	X		
1		1	1	

$Q_n K$

$R = Q_n K$



JK flip flop

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Q.3 convert SR Flip flop into T Flip flop.

⇒

Q_n	Q_{n+1}	T	S	R
0	0	0	0	x
0	1	1	1	0
1	0	1	0	1
1	1	0	x	0

FOR S

Q_n \ T	0	1
0		1
1	x	

$\overline{Q_n}T$

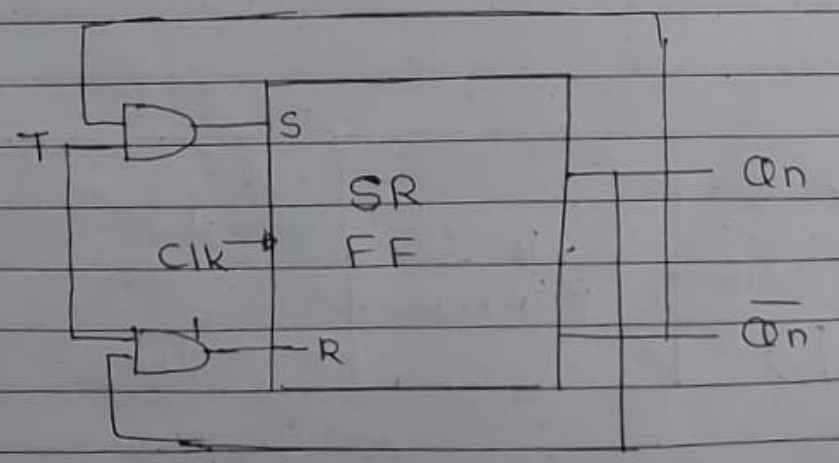
$S = \overline{Q_n}\,T$

FOR R

Q_n \ T	0	1
0	x	
1		1

Q_nT

$R = Q_n\,T$



T Flip flop

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Q.4 Convert JK flipflop into SR Flip Flop

Q_n	Q_{n+1}	S	R	J	K
0	0	0	X	0	X
0	1	1	0	1	X
1	0	0	1	X	1
1	1	X	0	X	0

For J

Q_n \ SR	00	01	11	10
0				1
1	X	X		X

$\bar{S}R$

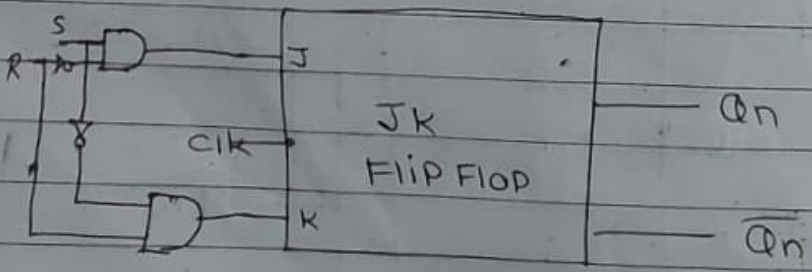
$J = S\bar{R}$

For K

Q_n \ SR	00	01	11	10
0	X	X		X
1		1		

$\bar{S}R$

$K = \bar{S}R$



[SR Flip Flop]

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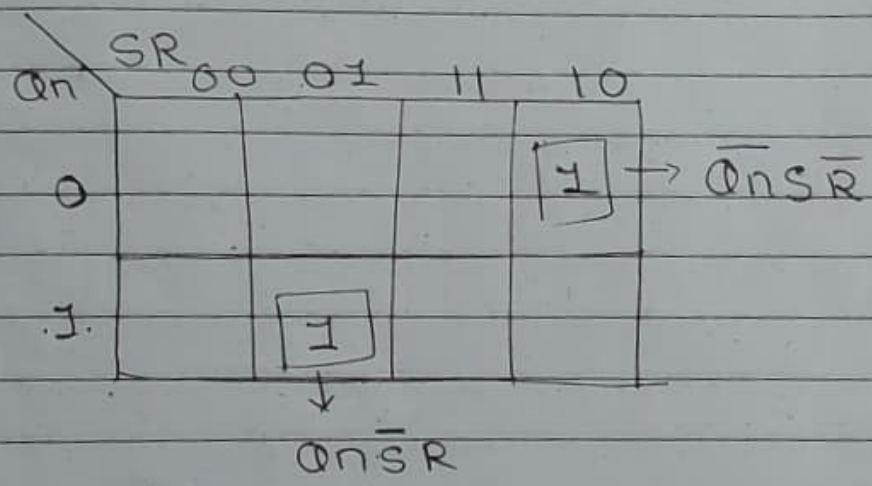
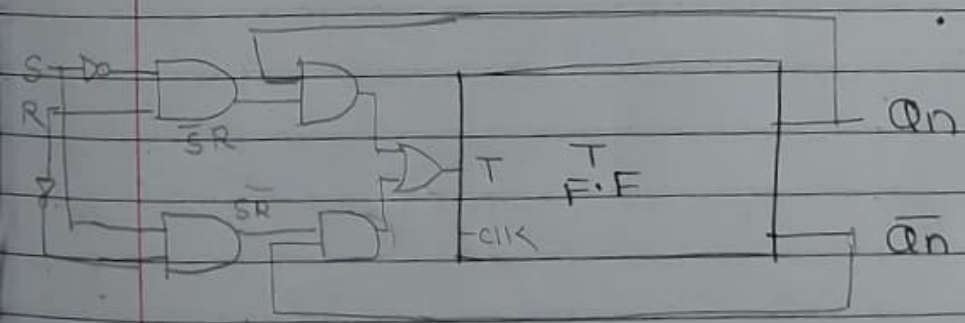
Q.5) Convert T Flip Flop into SR Flip

Q_n	Q_{n+1}	S	R	T
0	0	0	X	0
0	1	1	0	1
1	0	0	1	1
1	1	X	0	0

For T



$\therefore T = Q_n \bar{S} R + \bar{Q}_n S \bar{R}$



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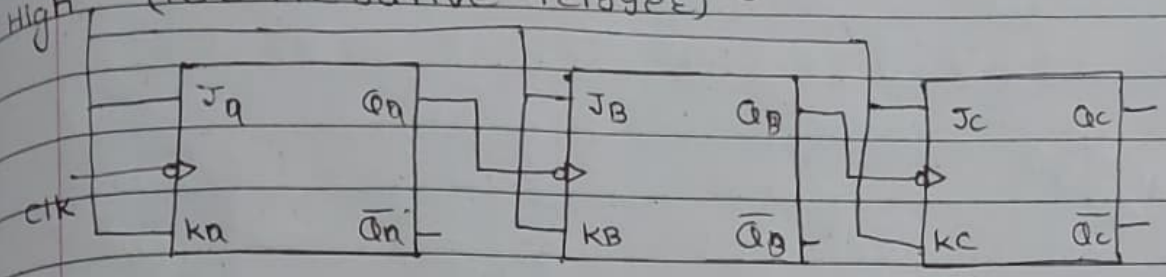
+ve edge triggered → |
-ve edge triggered → ○|

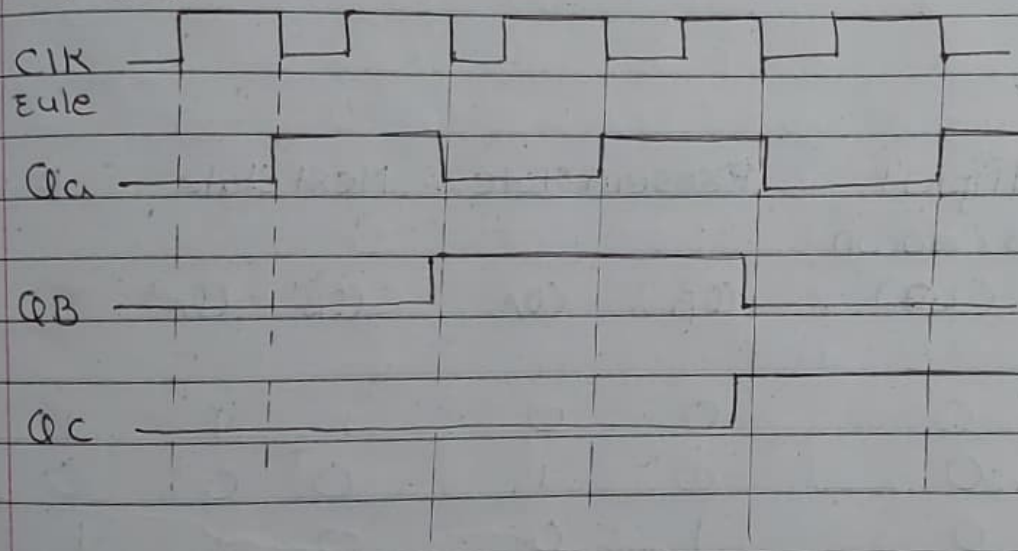
• Ripple counter (Asynchronous counter)

High (for negative trigger)



+ve Q → down
-ve Q → up

→ up (Diff polarity)
down (same polarity)



(2-bit)
• Up / Down Synchronous counter.

00 ↓up
01 ↓up
10 down
11 ↑ down

Input up/down (UB)	Present state Q_B	Q_A	Next State Q_B^+	Q_A^+	F.F T_B	T_A
0	0	0	1	1	1	1
0	0	1	0	0	0	1
0	1	0	0	1	1	1
0	1	1	1	0	0	1
1	0	0	0	1	0	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	0	0	1	1

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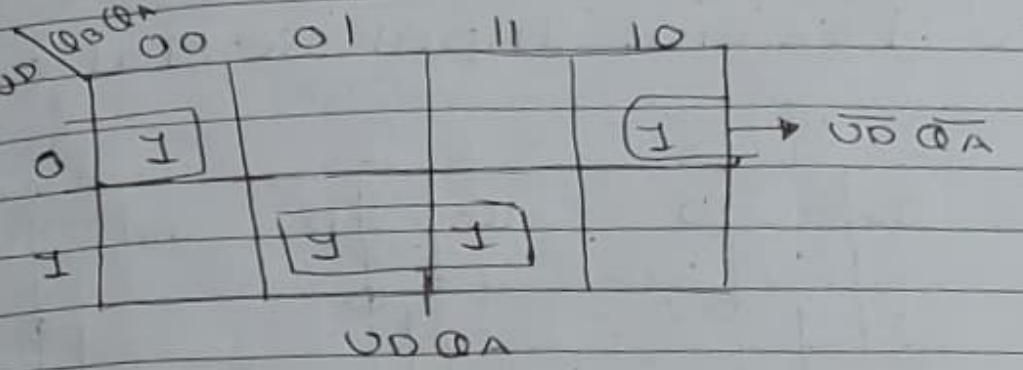
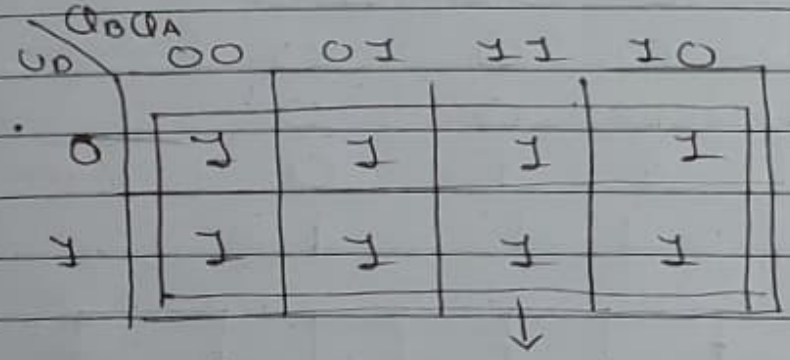
FOR T_B

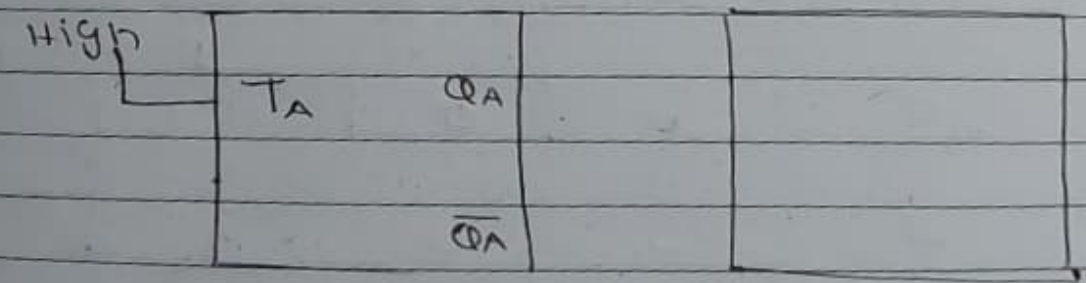


$$T_B = U_D Q_A + \overline{U_D}\,\overline{Q_A}$$

FOR T_A



$$T_A = 1$$



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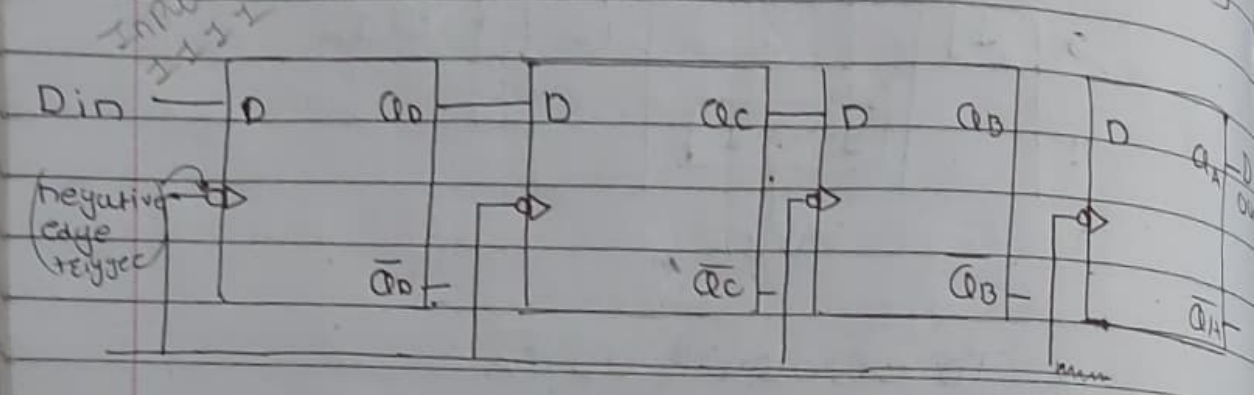
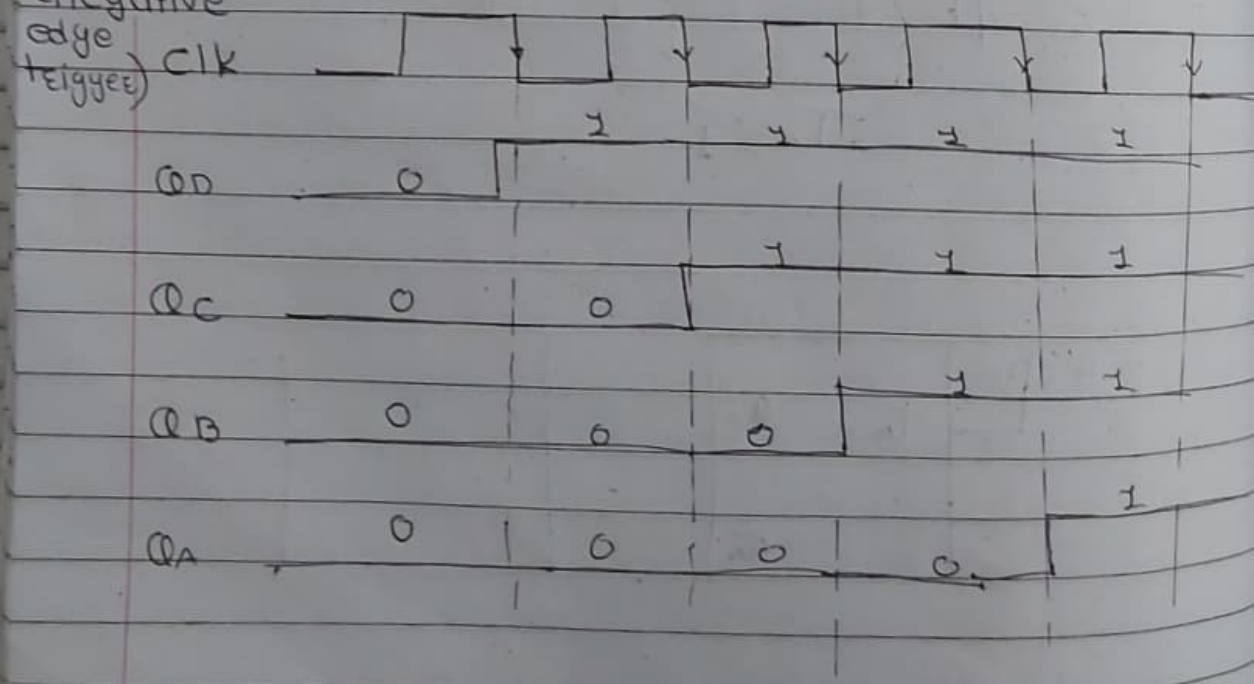
for Input bit shift
for output n-1 clock plus
D-flipflop is use to design it use for
operation

• Shift Registers :- To perform arithmetic

1] SISO [Serial Input Serial output]



CLK	Q_D	Q_C	Q_B	Q_A
Input	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1



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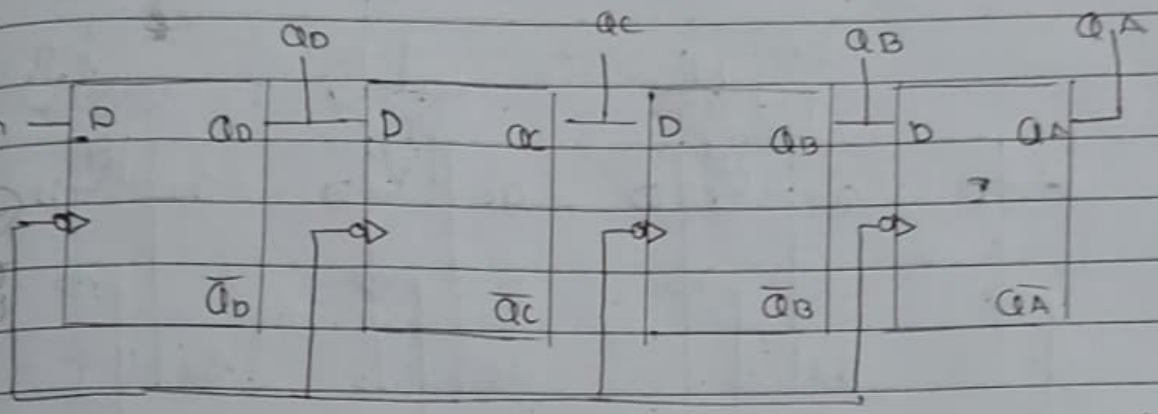
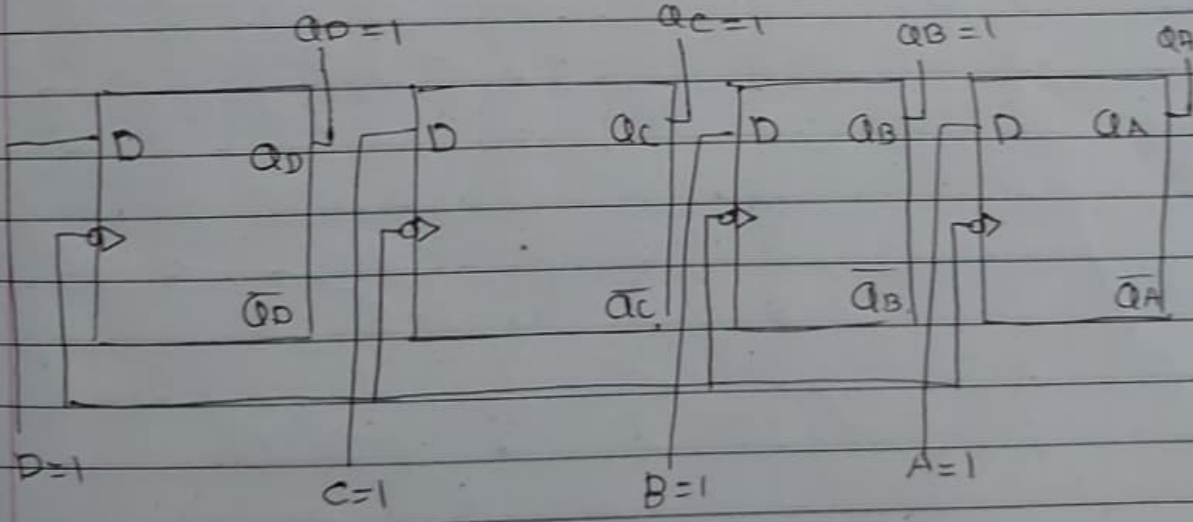
Input :=
for n bit n clockplus required
output = 0 clockpluses

2] SIPO (Serial Input Parallel output)



3] PIPO (Parallel Input parallel output) (fastest Shift Register)

for Input 4 clockplus required
for output 0 clockplus required



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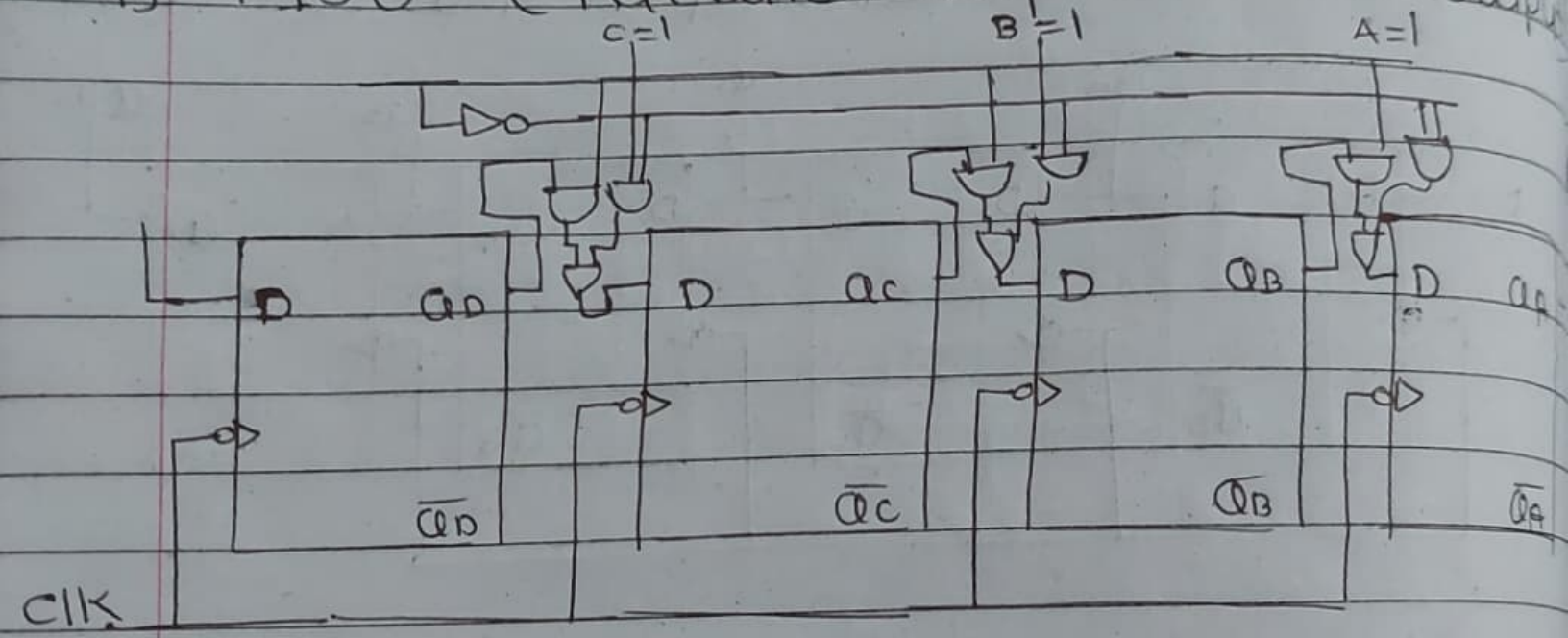
4) PISO (Parallel Input Serial outp



Input clockplus required (1)
Out clockplus requires (n-1)
Total = 4 (n)

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Imp If no the flop is not given [JK or T] is used

Q. Design 3-bit up-down Synchronous counter

Input UP/down (UB)	Present State			Net State			F.F		
	Q_C	Q_B	Q_A	Q_C^+	Q_B^+	Q_A^+	T_C	T_B	T_A
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	1	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1
0	1	1	0	1	0	1	0	1	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

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Input ani Present state vichar ghyachya k map

Tor K maping Next state

4 variable k-map

for Tc

UD Qc \ QB QA	00	01	11	10
00	1 (0)	(1)	(3)	(2)
01	1 (4)	(5)	(7)	(6)
11	(8)	(9)	1 (11)	(10)
10	(12)	(13)	1 (15)	(14)

Group of cells 0, 4 → $\overline{UD}\,\overline{Q_A}\,\overline{Q_B}$

Group of cells 11, 15 → $UD\,Q_A\,Q_B$

$$T_C = \overline{UD}\,\overline{Q_A}\,\overline{Q_B} + UD\,Q_A\,Q_B$$

for TB

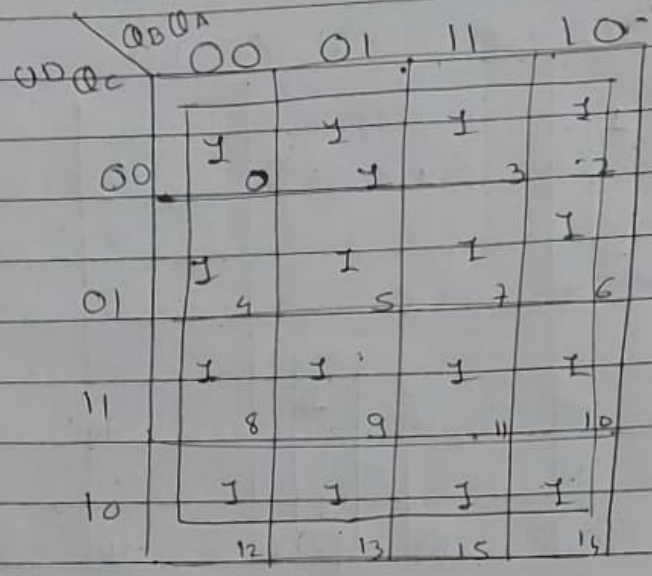
UD Qc \ QB QA	00	01	11	10
00	1 (0)	(1)	(3)	1 (2)
01	1 (4)	(5)	(7)	1 (6)
11	(8)	1 (9)	1 (11)	(10)
10	(12)	1 (13)	1 (15)	(14)

Group of cells 2, 6 → $\overline{UD}\,\overline{Q_A}$

Group of cells 9, 11, 13, 15 → $UD\,Q_A$

$$T_B = UD\,Q_A + \overline{UD}\,\overline{Q_A}$$

FOR T_A



$\therefore T_A = 1$