SIPNA COLLEGE OF ENGINEERING AND TECHNOLOGY, AMRAVATI
Department of Computer Science and Engineering

- **Year/Sem: 2nd/3rd**
- **Subject: A&DE**
- **Session: 2022-23**

Question Bank

Unit-III

Q1. Convert the given hexadecimal number $(1E.53)_{16}$ into equivalent binary, octal & decimal.

Q2. Represent $(32)_{10}$ in
a) BCD code b) Excess-3 Code

Q3. Convert the following binary to Gray code $(11001100)_2$.

Q4. Compute using 2's complement
$(42)_{10} - (68)_{10}$

Q5. Convert the following octal number into its equivalent hexadecimal, binary & decimal.
a) $(0.7634)_8$ b) $(65.64)_8$

Q6. Perform following subtraction using 2's Compliments method
a) $(2A)_{16} - (1C)_{16}$ b) $(28)_{10} - (16)_{10}$

Q7. Convert $(20)_{10}$ to Gray code

Q8. Represent the decimal number 62 in following various codes:
i) Binary ii) BCD iii) Excess - 3 iv) Gray Code v) Octal vi) Hexadecimal

Q9. Perform following subtraction using 9's Compliments method
a) $(28)_{10} - (16)_{10}$ b) $(34)_{10} - (29)_{10}$

Q10. Perform following subtraction using 10's Compliments method
a) $(268)_{10} - (347)_{10}$ b) $(69)_{10} - (32)_{10}$

Q11. Convert the following numbers:
i) $(117)_{10} = (\ )_2$
ii) $(37.31)_{10} = (\ )_2$
iii) $(3000.45)_{10} = (\ )_8$
iv) $(2003.31)_{10} = (\ )_{16}$

Q12. Convert the following numbers to its decimal equivalent:
i) $(475.25)_8 = (\ )_{10}$
ii) $(9B2.1A)_{16} = (\ )_{10}$
iii) $(3102.12)_8 = (\ )_{10}$
iv) $(614.15)_8 = (\ )_{10}$

Unit-IV

Q1. Simplify the following function using k-map
f=∑ m (0,1,2,3,5,7,9) + d (11,13,14,15)

Q2. Simplify the following Boolean function by using k-map
F (A, B, C, D) =∑ m (0,1,2,3,5,7,8,9) + d (11, 13, 14, 15)

Q3. Simplify the following function using tabulation method
f (A, B, C, D) = π M (0,2,4,6,8,9,12,13)

Q4. Implement following function with NOR-NOR logic:
f = π M (0,2,4,5,6)

Q5. Implement following function with NAND-NAND logic:
f =∑ m (0,2,4,5,6)

Q6. Simplify the following three variable expression using Boolean function
F= ∑m (1,3,5,7)

Q.7 Simplify the following Boolean function by using tabulation method
F (A, B, C, D) =∑ m (0,1,2,3,5,7,8,9,11,14)

Q8. Simplify the following Boolean function by using tabulation method
F (A, B, C, D, E) =∑ m (0,1,2,3,5,7,8,9,11,14,16,18,20,23,27,28,29,31)

Q9. Simplify the following Boolean function by using K-map
F (A, B, C, D, E) =∑ m (0,1,2,3,5,7,8,9,11,14,16,18,20,23,27,28,29,31)

Q10. Simplify the following Boolean function by using k-map
F (A, B, C, D) = π M (0,1,2,3,5,7,8,9) + d (11, 13, 14, 15)

Q11. Prove the following: -

1. $A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}E = A + B + C + D + E$
2. (A + B) (A + C) = A + BC
3. AB + CD = (A+C) (A+D) (B+C) (B+D)

Q12. Solve Using De-Morgans Theorm:

1. $Z = \overline{(A + BC)(D + EF)}$
2. $Z = \overline{A + \bar{B} + \bar{C}D}$
3. $Z = \overline{(A + \overline{BC})}\ (A\bar{B} + ABC)$

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Question Bank
Unit V & VI

UNIT-V

Q1: Design BCD to Excess-3 code converter using minimum number of logic gates
Q2: Realise 5-line to 32-line decoder using 4-line to 16-line decoder.
Q3: Design 7-bit odd parity checker using IC 74180 and explain working.
Q4: Design a binary to 7-segment decoder using 4:16 line decoder.
Q5: Design 10-bit even parity generator using single 74180 and inverter.
Q6: Design a logic circuit to generate an even parity bit for 3-bit binary input.
Q7: Design 1:32 D-MUX using 1:16 D-MUX
Q8: Explain decimal to BCD priority encoder.
Q9: Design a hexadecimal to binary priority encoder using 74148 ICs and one 74157 MUX.
Q10: Design 32:1 MUX using 16:1 MUX ICs and an OR gate.
Q11: Design 5-bit comparator using a single 7485 and one gate.
Q12: Design Binary to Gray code converter
Q13: Design 4-bit Look Ahead Carry adder and explain its operation.
Q14: Design Full Adder using K-Map.
Q15: Design 40: l multiplexer using 8: I multiplexers
Q16: Implement the following function using 4- line to l6- line decoder.
F1 =∑ m (0.1,2,5,7), F2 = ∑m (7,9,10,11, l2), F3 =∑m (8,11,13,14,15).

UNIT-VI

Q1: What is Shift Register? Explain 3-bit shift register along with neat Timing diagram.
Q2: Draw a mod - 5 synchronous up - counter using T flip - flop. Explain the same with the help of Timing diagram.
Q3: What is race around condition? How does it get eliminated in a master slave J - K flip flop? Explain.
Q4: With the help of neat diagram. explain the working of 4bit ring counter, also give the timing diagram.
Q5: Draw and explain the operation of 4-bit Bidirectional shift Register
Q6: Stale different types, of shift registers. Explain the operation of 3-bit shift register with neat diagram.
Q7: Design a 3-bit synchronous counter using J-K F/F.
Q8: Explain the operation of 5- stage twisted ring counter using D F/F.
Q9: Design Universal Shift Register and explain its operation.
Q10: Draw and explain the circuit diagram for M-S-J-K F/F and explain its advantages over JK F/F.
Q11: Explain performance comparison of counters and shift registers.

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Question Bank
Unit I & II

UNIT-I

Q1: Explain the forward and reverse characteristics of p-n junction diode. How it depends on temperature.
Q2: With respect to a P-N junction explain depletion region.
Q3: Compare CB, CC, CE with respect to current gain, voltage gain, I/p. resistance, o/p resistance and plot their i/p., o/p characteristics, explain them. Discuss any one application of each configuration
Q4: State different parameter of BJT. How BJT use as switch in CE mode?
Q5: Draw and Explain I/p &o/p characteristics of CE configuration amplifier and indicate active, saturation and cut-off region.
Q6: Derive expression between α and β. Explain $IC = \beta IB + (1+\beta) ICEO$
Q7: Explain the operation of PNP and NPN transistor.
Q8: For a transistor $\alpha = 0.98$; $IE = 20\mu A$; $ICBO = 1mA$ find the value of total IC, IB, β and ICEO.
Q9: Draw and Explain I/p &o/p characteristics of CB configuration.
Q10: Explain the operation of transistor in details.
Q11: Explain the concept of leakage current ICBO and ICEO. How are they related with each other
Q12: For CB configuration if i) $\alpha = 0.95$ and $IE = 1mA$ find the values of IC and IB, ii) $IE = 2mA$ and $IB = 20\mu A$ compute the values of α and IC.

UNIT-II

Q1: Static characteristics of JFET explain in detail.
Q2: With the help of suitable diagram explain Enhancement type MOSFET.
Q3: With the help of suitable diagram explain depletion type MOSFET.
Q4: A FET has following parameters, IDSS=32mA; VGS (off)= -8V; VGS= - 4.5V find the value of ID.
Q5: Compare MOSFET with JFET.
Q6: Derive $\mu = gm \times rd$ from the characteristic of JFET.
Q7: Compare JFET with BJT.
Q8: Define the various parameters of JFET.
Q9: A FET has a driven current of 4mA. If IDSS= 8mA and VGS (off)= -6V. Find VGS & VP.
Q10: What is a complementary metal-oxide semiconductor (CMOS)?
