STIMULATION AND CHARACTERIZATION OF NANO SCALED FET

Submitted

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DECLARATION

I/We declare that the project work contained in this report is original and it has been done by me under the guidance of my project guide.

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CERTIFICATE

This is to certify that (Student Name) bearing (Regd. No.:) has satisfactorily completed Mini Project Entitled in partial fulfillment of the requirements as prescribed by University for VIIIth semester, Bachelor of Technology in "Electrical, Electronics and Communication Engineering" and submitted this report during the academic year 2024-2025.

[Signature of the Guide] **[Signature of HOD]**

Table of contents

Chapter 1: Introduction:

Nanoscaled Field-Effect Transistors (FETs) are tiny electronic components used in modern devices like smartphones and computers. As technology advances, these FETs are becoming smaller and more complex, making their behavior harder to predict and understand,also reaching the nanometer scale (less than 100 nm). However, making these tiny transistors work efficiently is challenging due to issues like leakage current, short-channel effects, and power dissipation. To solve these problems, we are trying to test and study different types of Field Effect Transistors (FETs) and test their performance using simulation and characterization techniques.To address this,we use simulation and characterization techniques to make it easier.

- **Simulation**: We used TCAD (Technology Computer-Aided Design) software to predict how FETs will behave before manufacturing.
- If the simulation results show any problems, the design can be modified before manufacturing, saving time and cost,like

❖ How much current flows through the transistor?
❖ How much power does it consume?
❖ Does it heat up too much?

- **Characterization**: Involves real-world testing of FETs to measure their electrical, structural, and thermal performance.

❖ **Electrical performance**: How efficiently does it switch on and off?
❖ **Thermal behavior**: Does it overheat during operation?

1.1 Overview of the problem statement:

"To analyze and compare the performance of DGIM-FET, IM-FET, JL-FET, and DGJL-FET using simulation and characterization techniques, identifying their advantages, limitations, and suitability for advanced semiconductor applications."

1.2 Objectives and goals:

- Simulate nanoscale FETs (DGIM-FET, IM-FET, JL-FET, DGJL-FET) using TCAD tools to predict their behavior.
- Compare their performance in terms of current control, leakage, power efficiency, and scalability.
- Identify the best FET design for different applications based on simulation and real-world data.

Main Goals

- Performance Optimization
- Understanding Behavior
- Scaling Down Further
- Exploring New Materials

Comparison Table:

Parameter	IM-FET	DGIM-FET	JL-FET	nDGJL-FET
Size	Moderate	Smaller than IMFET	Very Small	Smallest among all
Speed	Moderate	Fast	Fast but slower than DGIM	Fastest
Thermal Stability	Moderate	Better than IMFET	lower stability	Best
Majority Carriers	Electrons (n-type) / Holes (p-type)	Electrons (n-type) / Holes (p-type)	Electrons (n-type) / Holes (p-type)	Electrons (n-type) / Holes (p-type)
Minority Carriers	Few due to inversion layer	Fewer than IMFET	Not Available(no junction)	Almost negligible
Leakage Current	High	Low	Low	Very Low
Threshold Voltage (Vth)	Moderate	Lower than IMFET	Lowest among all	Optimal (better than JL but controlled)

Parameter	IM - FET	DGIM-FET	JL-FET	nDGJL-FET
ID vs VG Plot	Standard like MOSFET	Steeper than IMFET	Slower rise	Steepest increase
Doping Profile	Normal doping	High doping in channel region	Uniform doping throughout	Ultra-thin uniform doping
Fabrication Complexity	Standard CMOS	More complex due to double-gate	Easier than DGIM but has leakage issues	Most complex but best performance
power consumption	High	Moderate	Low	Lowest
scalability	Low	Medium	High	Very high
Heat Dissipation	High	Medium	Low	Lowest
Applications	General MOSFET applications	High-speed and low-power applications	Low-power but high-leakage applications	Ultra-low power, high-performance applications

Chapter 2 : Literature Review:

TITLE	AUTHOR	YEAR	TECHNOLOGY USED	SUMMARY	PRO	LIMITATION
Device and circuit performance analysis of double gate junctionless transistors at Lg = 18 nm	Chitrakant Sahu, Jawar Singh	2014	ATLAS TCAD mixed-mode simulator	JL DG devices outperform IM FETs with better speed and stability.	Faster performance and improved SRAM stability	JL design complexity compared to conventional CMOS.
Analysis of Delta-Doped and Uniformly Doped AlGaAs/GaAs HEMTs by Ensemble Monte Carlo Simulations	Ki Wook Kim, Hong Tian, Michael A. Littlejohn	1991	Uniformly doped AlGaAs/GaAs high electron mobility transistors (HEMTs)	Delta-doped HEMTs outperform uniform ones in electron density and speed.	Improved transconductance and drain current drive	Increased complexity in device structure and fabrication.
A Physics-Based Threshold Voltage Model for Junctionless Double Gate FETs Having Vertical Structural and Doping Asymmetry	A. Kumar, J. N. Roy	2019	Synopsys Sentaurus Device simulation tool, MATLAB	Model for asymmetric JL DG FETs simplifies analysis while maintaining accuracy	Simplifies complex calculations with improved accuracy.	May not account for all real-world device variations.

TITLE	AUTHOR	YEAR	TECHNOLOGY USED	SUMMARY	PRO	LIMITATION
Thermo-magnetic effects on MOSFETs simulated and experimentally characterized for reliability	Gabriela A. Rodríguez-Ruiz et al.	2015	Thermo-magnetic modeling and simulation in nano-scaled MOSFETs.	The paper introduces a simulation method for studying the effects of temperature and magnetic fields on the gate tunneling current in MOSFET devices.	Provides a new method for mapping electronic properties in nanoscaled MOSFETs.	Simulation and experimental setup are complex and require precise control.
Impact of Single Charged Gate Oxide Defects on the Performance and Scaling of Nanoscaled FETs	J. Franco, B. Kaczer, M. Toledano-Luque, et al.	2012	Nanoscaled Field-Effect Transistors (FETs) particularly pFinFETs and planar pMOSFETs, which include SiGe channel devices	NBTI reliability in nanoscaled FETs varies by technology, impacting scaling	SiGe channel devices exhibit reduced time-dependent variability, enhancing NBTI robustness.	The severe 1/area scaling rule complicates reliability predictions for further scaling.

Chapter 3 : Strategic Analysis and Problem Definition:

3.1 SWOT Analysis:

SWOT Analysis is defined as Strengths,Weaknesses,Opportunities & Threats. Here's the SWOT Analysis:

Strengths:

1.Precise Analysis
2.Time-Saving
3.Enhanced Optimization

Weaknesses:

1.Simulation Accuracy
2.Assumptions Approximations

Opportunities:

1.Technology Advancement
2.Integration with AI/ML
3.Miniaturization Trend
4.Cross-Disciplinary Collaboration

Threats:

1.Rapid Technological Changes
2.High Competition
3.Data Security Risks

3.2 Refinement of Problem Statement:

Nanoscale Field-Effect Transistors (FETs) are being investigated as a result of the growing need for low-power, high-performance semiconductor devices. The simulation and characterization of various nanoscale FET structures, such as IM-FET, DGIM-FET, JL-FET, and DGJL-FET, are the main objectives of this project.

Comparing their electrical performance in terms of important parameters like drain current, leakage current, subthreshold slope, and threshold voltage

is the goal. The study's goal is to use simulation-based analysis to determine the benefits and drawbacks of each transistor design, offering information about how well they might work in upcoming nanoelectronics applications.

Chapter 4 : Methodology:

4.1 Description of the approach:

1.Device Modelling:

Since nanoscale transistors are extremely small, their behavior is affected by quantum mechanical effect**s** (like electron tunneling and charge confinement). To study these effects, researchers use computational models instead of directly fabricating the transistors.

How It helps in our Project:

- We used TCADsoftware to create virtual models of DGIM-FET, IM-FET, JL-FET, and DGJL-FET.
- These models will simulate how electrons move through the transistor and predict key properties like current flow, leakage, and power efficiency.
- The simulation will help you understand which transistor type performs better before manufacturing.

Electrical Characterization:

- **I-V Characteristics** : It measures how current (I) changes with voltage (V) to see how efficiently the transistor switches ON and OFF.

- **Threshold Voltage (Vth):** The minimum voltage needed to turn the transistor ON.
- **Subthreshold Slope** : Tells how quickly the transistor turns ON from an OFF state (important for power efficiency).

4.2 Tools and techniques utilized

- **Design Specifications:** Define key parameters such as channel length, width, and material properties.Use CAD tools like TCAD.
- **Material Selection:** Choose suitable semiconductor materials (e.g., silicon, graphene, MoS2) based on desired electrical properties and scalability.
- **Current-Voltage (I-V) Testing**: Measures how much current flows through the FET at different voltages. This shows how well the FET turns on and off,like

IV Curve Tracing Techniques:

- **Sweep Measurement**: Applying a voltage/current sweep and measuring response.
- **Pulsed I-V Measurement**: Reduces heating effects for accurate testing.
- **Logarithmic Sweeps**: Used for low-current devices like MOSFETs.

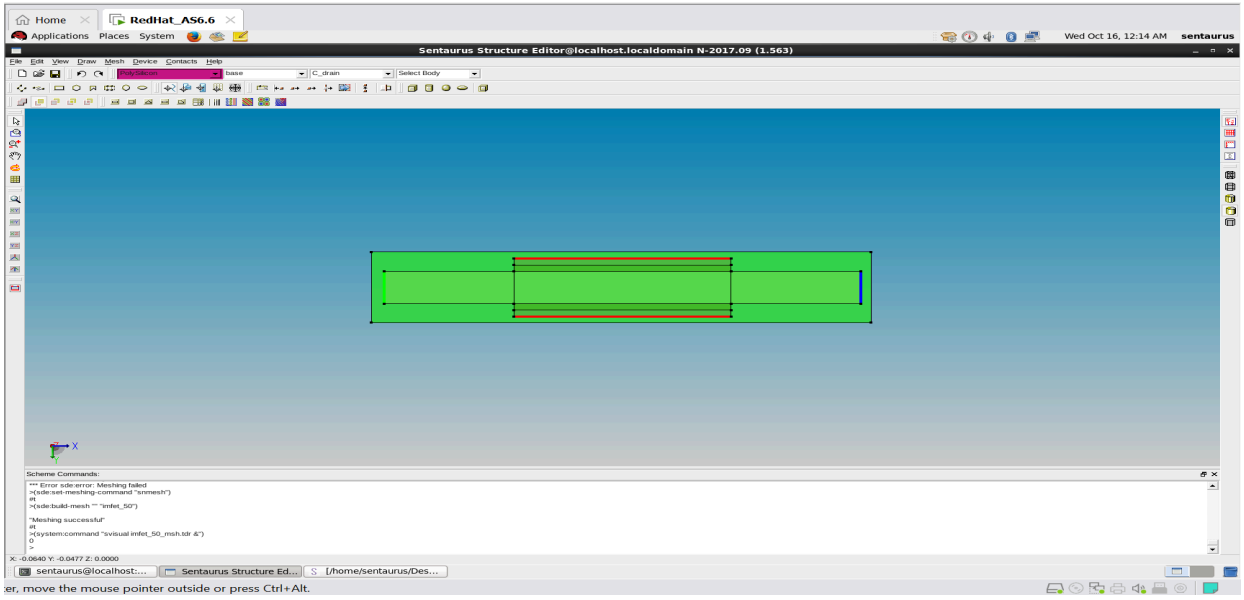
4.3 Design considerations:

- **Scaling and Size**: As transistors get smaller, controlling short-channel effects like leakage current and Drain-Induced Barrier Lowering becomes more difficult. Proper scaling is essential to maintain efficiency.
- **Material Selection**: Using advanced materials, such as high-k dielectrics (for gate insulation) or new semiconductors like GaN or

Graphene can enhance performance by reducing leakage and improving speed.

- **Quantum Effects**: At the nanoscale, quantum mechanical effects like tunneling and electron confinement significantly impact device behavior, so they need to be considered in design.
- **Power Consumption**: Reducing power consumption is critical, especially for low-power applications. Techniques like using multi-gate architectures help reduce power while maintaining high performance.

Chapter 5 : Implementation:



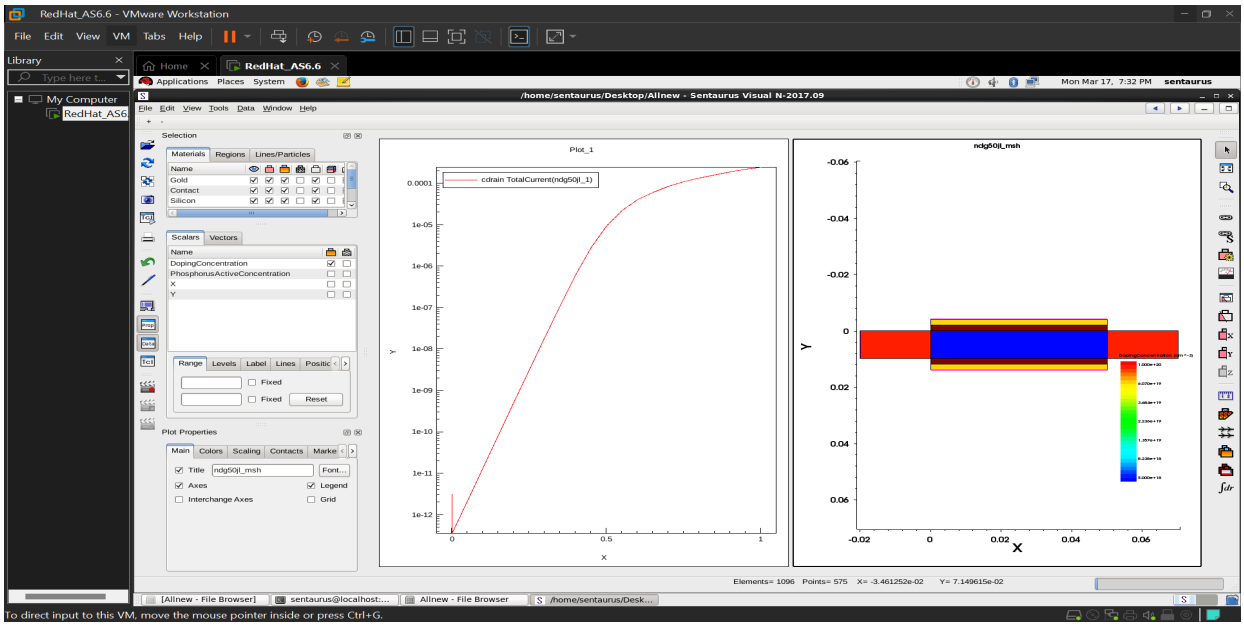
5.1 Description of how the project was executed

The image shows a TCAD Sentaurus Structure Editor interface, used to design and simulate a nanoscale FET (Field-Effect Transistor). The structure is created by defining materials, doping regions, and device contacts. Here's how it is implemented:

1. **Device Creation**:
    - The substrate (green region) represents the semiconductor (e.g., silicon).
    - The red and blue lines indicate different layers, likely gate, source, and drain.
2. **Meshing Process**:
    - A simulation grid (mesh) is applied to divide the structure into small elements for solving equations.
    - The error message suggests an initial meshing failure, but later it was successfully generated.
3. **Simulation Preparation**:
    - After meshing, the device undergoes electrical simulations like I-V characteristics, capacitance, and leakage current analysis.
    - It helps study transistor behavior under different voltages.

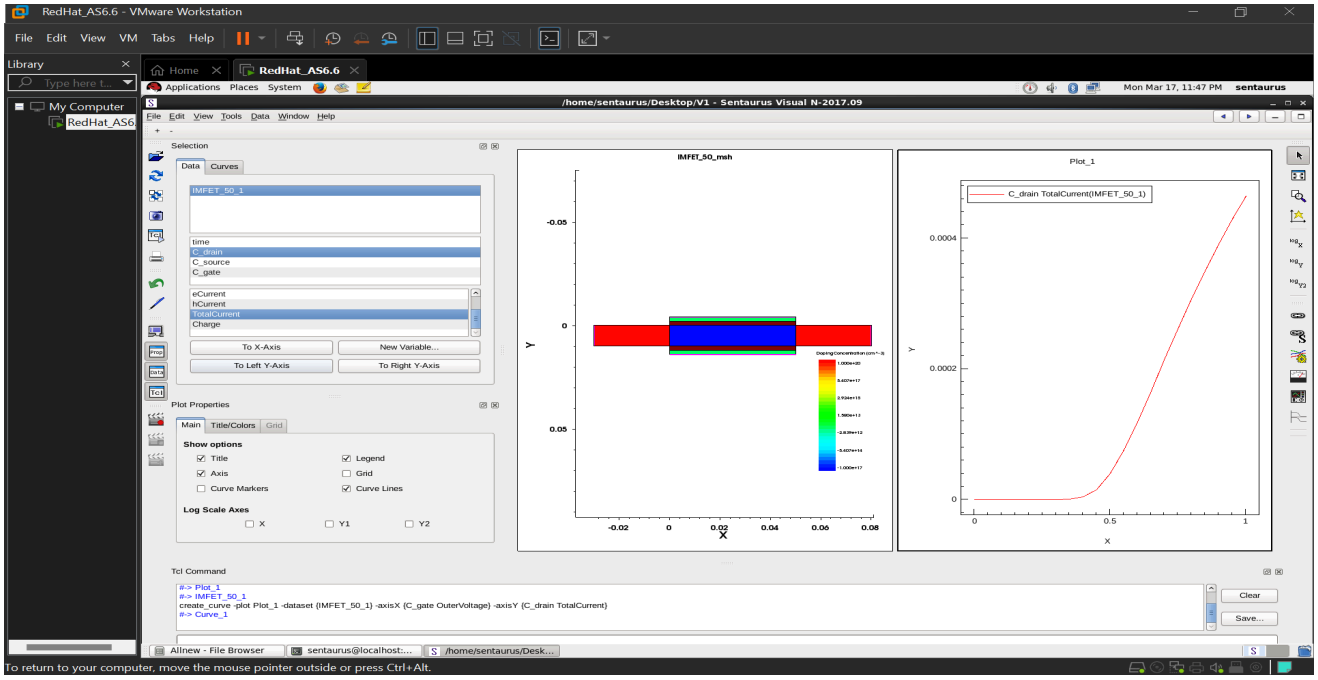
This is the common structure of all the types of MOSFETs that we are going to study and compare.

1.DGJLFET:



- The above picture is the structure and plot of an n-type double gate junctionless FET of 50 nm channel length(nDGJL50) . Here,
- Blue colored region - Channel(doping conc - 5 x 10^18) also it is the lowest doping concentration.
- Red colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
- Yellow is the metal region where we used gold.
- Brown represents the metal oxide.
- The graph is between gate voltage and drain current and it increases as the voltage increases.

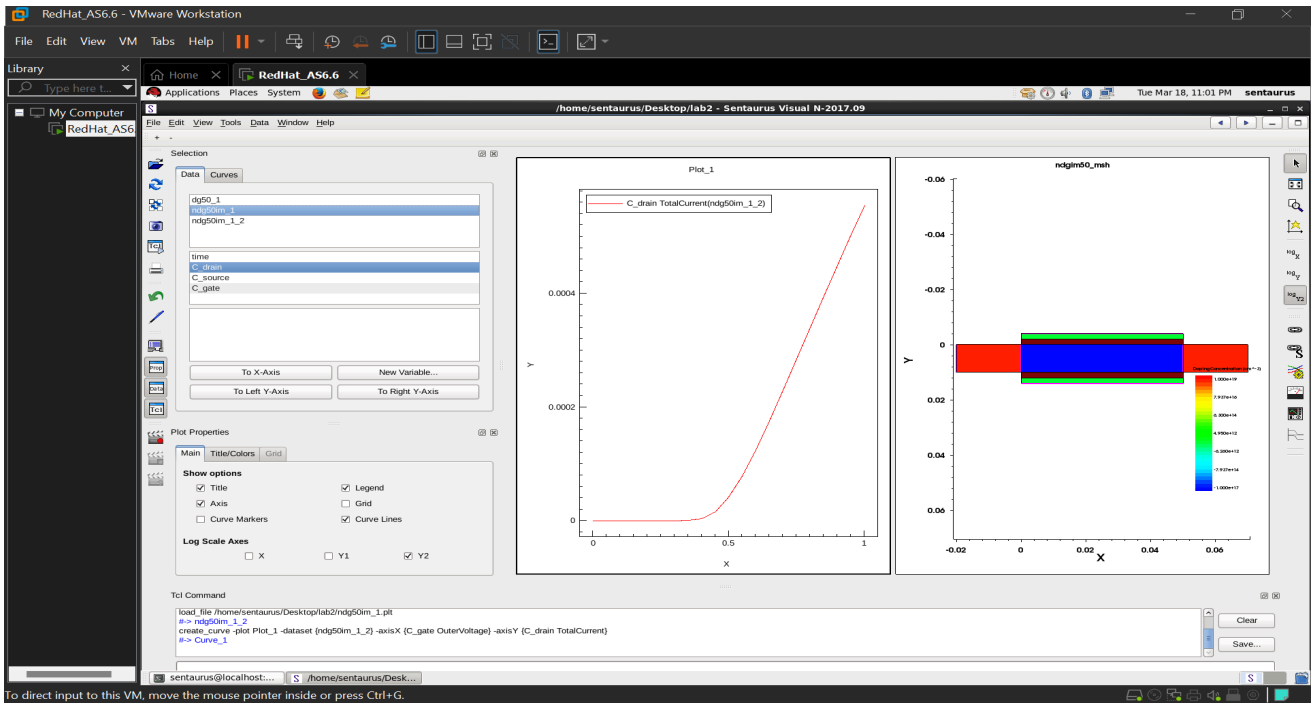
2.IMFET_50:



- The above picture is the structure and plot of an IMFET(inversion mode) of 50 nm channel length(nDGJL50) . Here,

- Blue colored region - Channel(doping conc - 5 x 10^17) also it is the lowest doping concentration.
- Red colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
- Green is the metal region where we used polysilicon.
- Brown represents the metal oxide(SiO2).
- The graph is between gate voltage and drain current and it increases as the voltage increases.

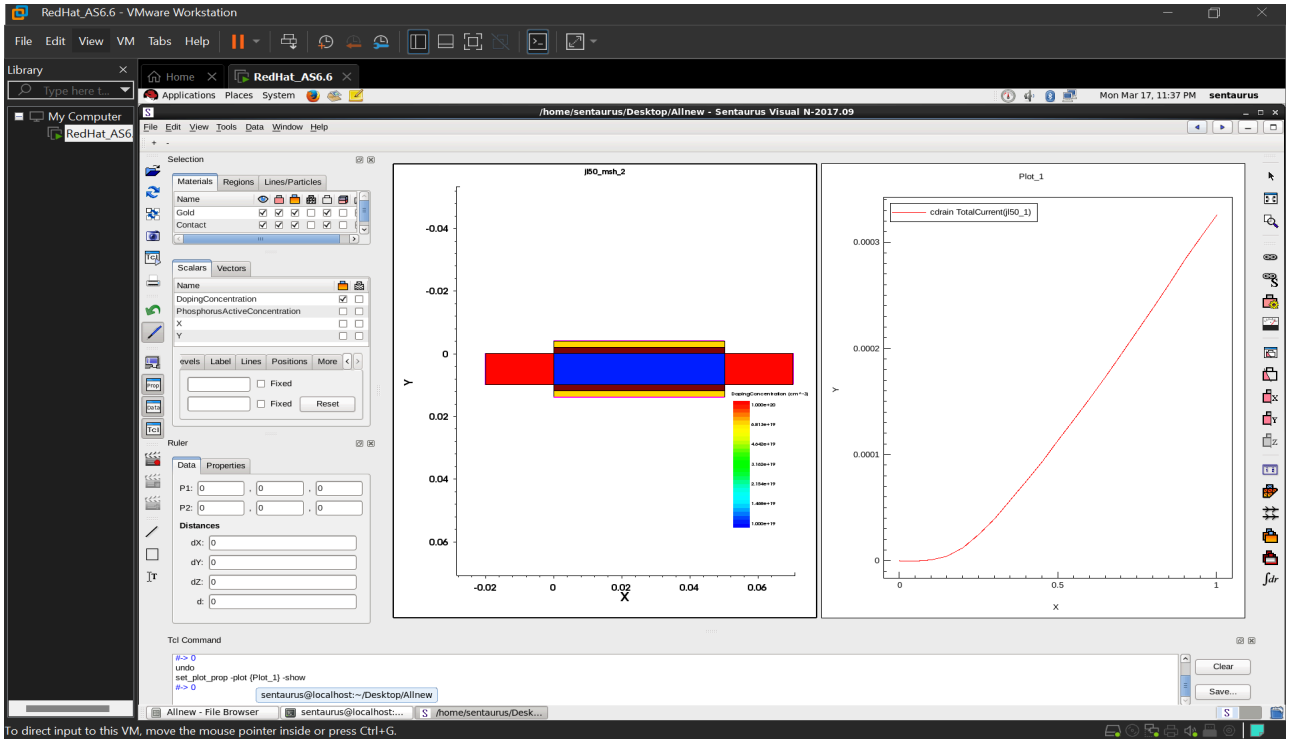
3. DGIM50:



- The above picture is the structure and plot of a double gate inversion mode FET of 50 nm channel length(nDGIM50) . Here,
- Yellow colored region - Channel(doping conc - 5 x 10^17) also it is the lowest doping concentration.
- Red ,Orange colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
- Yellow is the metal region where we used gold.

- Blue represents the metal oxide.
- The graph is between gate voltage and drain current and it increases as the voltage increases.

4.JL50:



- The above picture is the structure and plot of a junctionless FET of 50 nm channel length(JL50) . Here,
- Blue colored region - Channel(doping conc - 1 x 10^19) also it is the lowest doping concentration.
- Red colored region- Source,drain(doping conc - 1x10^20) highest doping concentration.
- Yellow is the metal region where we used gold.
- Brown represents the metal oxide.
- The graph is between gate voltage and drain current and it increases as the voltage increases.

Chapter 6:Results :

Name	IM-FET	DGIM-FET	JL-FET	nDGJL-FET
Threshold Voltage	0.474346V	0.472654V	0.27251V	0.5539V
GmMax	0.000950	0.00110	0.0004529	0.00055
Ioff(Id at Vg=0)	2.49 x 10^ -18 A	1.75 x 10^ - 19 A	5.28 x 10 ^ -17 A	3.17 x 10^-12 A
Id sat	0.000465 A	0.000555 A	0.000326 A	0.000246 A
R out	1.839 x 10 ^ 6	1.655 x 10 ^ 6	2.130 x 10 ^ 6	2.054 x 10 ^ 6
R On	0	0	0	0

Based on all the given parameters, **DGJL-FET is the best choice** for your project. Here's why:

1.Fastest Switching Speed

- nDGJL-FET offers the fastest operation due to its optimized structure and minimal parasitic effects.
- This makes it ideal for high-speed applications in modern electronic circuits.

2. Maximum Threshold Voltage (Vth = 0.5539V)

- In low-power applications, a transistor with a higher threshold voltage can offer greater stability and is less likely to leak.
- It is helpful in applications where power control is crucial because it guarantees dependable switching.

3. Moderate Transconductance (GmMax = 0.00055)

- It still provides a decent balance between efficiency and switching speed, despite not being the best.
- Ideal for mixed-signal and low-power digital applications.

4. Greater Leakage Current (Ioff = 3.17 × 10^{-12} A)

- Compared to other FETs, the leakage current is higher, which could have an impact on power efficiency.
- In high-speed applications, where speedier operation is more crucial, this trade-off might be justified.

5. Reduced Saturation Current (Id,sat = 0.000246 A)

- Compared to DGIM-FET, it can manage a lower current drive because it has the lowest Id,sat.

6. High Output Resistance (Rout = 2.054 × 10^{6} Ω)

- Better voltage stability and reduced signal degradation are associated with higher routing.
- beneficial for RF and analog applications where stability is essential.

7. R On = 0Ω, or zero on-resistance

- Its zero on-resistance ensures effective conduction in the ON state, just like all the other FETs in the comparison.

It works best for:

1. Ideal for low-power, high-speed applications such as AI processors, the Internet of Things, and next-generation semiconductor devices.
2. It is perfect for upcoming nanoscale electronics because it is highly scalable.
3. It is beneficial in RF and precision analog circuits due to its superior voltage stability.
4. Excellent performance for applications where stability and energy efficiency are more important than raw current drive.

Chapter 7: Conclusion:

In this study, we compared important parameters such as threshold voltage, transconductance, leakage current, saturation current, and output resistance at 50 nm technology in order to analyze four different types of FETs: IM-FET, DGIM-FET, JL-FET, and nDGJL-FET.

The best option after weighing all the variables is nDGJL-FET because of its exceptional stability, speed, and scalability at the nanoscale. It is extremely power-efficient because it provides the highest threshold voltage, which guarantees improved control and less leakage. It is ideal for low-power applications because of its optimized structure, which reduces energy loss. Its high output resistance also ensures steady performance, which is necessary for precision circuits. The nDGJL-FET is perfect for next-generation VLSI and IoT because it offers the best combination of speed, efficiency, and power optimization at 50 nm, even though other FETs have their advantages.

Chapter 8 : Challenges & Future Work:

Challenges :

1. Comparing with Other FETs:

- You must simulate and contrast other devices in order to demonstrate that NDGJLFET is superior.
- This requires more validation and adds to the workload.

2. Optimization Problems:

- It can be challenging to determine the ideal doping concentration and material characteristics.
- Current flow and threshold voltage (Vth) can be impacted by slight variations.

3. Material Properties:

- Results can be altered by even slight changes in doping or gate material.
- needs to be carefully calibrated using actual data.

4. Mesh Optimization:

- Accurate results require a fine mesh, but striking the correct balance can be challenging.

5. Long Simulation Time:

- We must exercise extra caution when running simulations because TCAD simulations typically take a long time.
- A small mistake could result in the structure being built from the ground up.

Future Work :

1. Optimize Mesh for Faster Simulation:

- To strike a balance between speed and accuracy, enhance mesh refinement methods.
- Reduce needless computation by using adaptive meshing.

2. Improve Material Models:

- Use cutting-edge material characteristics to increase precision.
- For better performance, investigate novel gate and channel materials.

3. Exploring New Materials:

- To improve transistor efficiency, look into high-k dielectrics or 2D materials (such as graphene or MoS_2).

4. Compare with Experimental Data:

- Verify the simulation by contrasting it with actual manufactured devices.
- Parameters should be changed to reflect experimental findings.

5. Expand to 3D Simulation:

- For more lifelike outcomes, switch from 2D to 3D modeling.
- Examine the behavior of short-channel effects in three dimensions.

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Github Link:

https://github.com/niharikasidaa/Simulation-characterisation-of-nanoscale-FET