Probelm1: Write a VHDL function that creates the 2's complement of an n-bit vector. In the main code, you call it as: **COMLEMENT (DataVec, N);** Where N: the length of the vector.

if A<="1101" then B<= ***COMLEMENT (A, 4) returns: "0011".***
if A<="11010001" then B<= ***COMLEMENT (A, 8) returns: "00101111".***

Problem2: Write a VHDL procedure that will add two ***nxm*** matrices of integers. C<=A+B. The procedure name is **ADDMATRIX(A, B,C).** Your procedure should check if the number of rows of A, and B are the same. Also, the number of columns of A, and B are the same. If not, then it should return ERROR(***hint: use Assert, report***).

$$\begin{matrix}1&1\\1&3\\3&4\end{matrix}+\begin{matrix}1&1\\1&3\\3&4\end{matrix}=\begin{matrix}2&2\\2&6,\\6&8\end{matrix}\qquad\begin{matrix}1&1\\1&3\\3&4\end{matrix}+\begin{matrix}1&2&4\\4&5&5\end{matrix}=returns\ Error$$

Problem3: Write a VHDL modules using "***Structural model***" that has two inputs: an N-bit vector A, and a control signal (1 bit) B. The output is N-bit vector C. When B='1' then C<= A. When B='0', C is all 0's.
Use **Generic** to specify the value of N (default = 4). Use **generate** statement to instantiate an N 2-input (1 bit) AND gates.

Problem4: Subtype X01LH of std_logic has the values 'X','0','1','L', and 'H'. Complete the following resolution function for this type. (Hint: Ch8, section 8.7).

	'X'	'0'	'1'	'L'	'H'
'X'					
'0'					
'1'					
'L'					
'H'					

Problem5: Given the following 3 concurrent statements, where R is of type X01Z. Draw the queue/multiple drivers and develop the **resolved** values of R. ***Assume R is initially 'Z'***.
R <= transport '0' after 1 ns; '1' after 3 ns; 'Z' after 7 ns;
R <= transport 'Z' after 2 ns; '1' after 4 ns; 'Z' after 8 ns;
R <= transport '0' after 1 ns; '1' after 5 ns; 'Z' after 9 ns;

Problem6: Write a complete package named "ECE4250_HW6" that includes function in Problem 1, and the procedure in Problem 2, and the module in Problem 3, and the subtype in problem 4. Your code should include: Package declaration, body and complete description of the entities, function and procedures.

Write a test code that will show your package working. *Hint: in your main code:* **use work.ECE4250_HW6.all**;

Note: Your code should compile and you should attach sample run of your test code.