**ECE 4250/ 7250: VHDL and Programmable Logic Devices**

**Laboratory**

**Lab #: 03**

**Lab Title: 4 Bit Full Adder Implementation on Xilinx Spartan-3**

**Group #: 5**

**Names: John Kelly | Zach Rump**

**Teaching Assistant Use Only:**

**Points Earned Reasons for Deduction**

**Pre-lab:**

**Post Lab report**:

**Demonstration:**

**Final Lab Grade:**

**Comments to students:**

Objective

The objective of Lab 03 is to become familiar with the Xilinx ISE and Spartan-3 FPGA. Specifically, learn how to synthesize, implement and download a design onto the board. This lab uses a 4-bit full adder as an example design.

Lab work

Implementation: write a note on how the .vhd files involved in the code and

the working of the program in general.

Post lab questions:

1. What is the function of the UCF file?

ii. Explain the role of “NET”A<0>” LOC = “F12”;” from the UCF file.

Conclusion:

what went wrong? Why? How was it solved?